ECSS-E-ST-20-20C
15 April 2016

Space engineering

Electrical design and interface requirements for power supply

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-E-ST-20-20 Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

Disclaimer

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Introduction

This standard identifies the requirements needed to specify, procure or develop a space power distribution based on Latching Current Limiters, both from source and load perspective.

For a reference architecture description, it is possible to refer to ECSS-E-HB-20-20.

ECSS-E-HB-20-20 includes a clarification of the principles of operation of a power distribution based on LCLs, identifies important issues related to LCLs and explains the requirements of the present standard.

Note that the present issue of the standard covers electrical design and interface requirements for power distribution based on Latching Current Limiters only. Future issues of the present standard will cover additional power interfaces.

1
Scope

The target applications covered by this standard are all missions traditionally provided with power distribution and protection by LCLs/RLCLs (science, earth observation, navigation) with exclusion of applications for which the power distribution and protection is provided by fuses (e.g. most of the GEO telecom satellites).

The present standard applies to power distribution by LCLs/RLCLs for power systems, and in general for satellites, required to be Single Point Failure Free.

The present standard document applies exclusively to the main bus power distribution by LCLs/RLCLs to external satellite loads.

A particular case of LCLs (Heater LCLs, or HLCLs) is also treated. The HLCLs are the protections elements of the power distribution to the thermal heaters in a spacecraft.

Internal power system protections of LCLs/RLCLs are not covered.

Paralleling of LCLs to increase power supply line reliability is not covered by the present standard, since this choice does not appreciably change the reliability of the overall function (i.e. LCL plus load).

In fact, a typical reliability figure of the LCL (limited to the loss of its switch-on capability) is 20 FIT or less.

If the load to be connected to the LCL line has a substantial higher failure rate than this, it is not necessary to duplicate the LCL to supply that load.

This standard may be tailored for the specific characteristic and constrains of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system - Glossary of terms
ECSS-E-ST-20	Space engineering - Electrical and electronic

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, in particular for the following terms:

1. redundancy
2. active redundancy
3. hot redundancy
4. cold redundancy
5. fault
6. fault tolerance

3.2 Terms specific to the present standard

3.2.1 centralised

feature that serves a number of elementary functions in a system

3.2.2 current overshoot decay time

maximum time constant decay time from current overshoot peak to actual limitation current after an overcurrent event, under the assumption that the decay time is modelled by an exponential law

3.2.3 current overshoot recovery time

time needed for the to reduce from its maximum value to ±10% of the excess current, at the application of an overload to the LCL/RLCL/HLCL

NOTE 1 See Figure 3-1 and Figure 3-2.

NOTE 2 Excess current is intended as overshoot peak minus actual limitation current value.

3.2.4 fault condition

internal failure of one of the following devices: LCL, RLCL or HLCL

NOTE This definition is aimed at clarifying that the fault condition is not the one relevant to the load.

3.2.5 fault current emission

maximum current emission of a given circuit at external interface under abnormal conditions

NOTE Abnormal in this context can cover fault condition or operator error.

3.2.6 fault current tolerance

minimum abnormal interface current that a circuit can sustain without being damaged

3.2.7 fault voltage emission

maximum voltage emission of a given circuit at external interface under abnormal conditions

NOTE Abnormal condition can cover fault condition or operator error.

3.2.8 fault voltage tolerance

minimum abnormal interface voltage that a circuit can sustain without being damaged

3.2.9 feature

part of a function to which a specific requirement refers

3.2.10 heater latching current limiter (HLCL)

LCL used as protection element in a power distribution to satellite thermal heaters

3.2.11 input filter charge time

time required for the LCL to charge the load input filter

NOTE See Figure 3-3.

3.2.12 input overshoot charge

charge requested at the LCL/RLCL/HLCL input at the application of an overload, for current in excess of the actual limitation current

NOTE See Figure 3-1 and Figure 3-2.

3.2.13 latching current limiter (LCL)

switchable and latching protection placed between a power source and the relevant load, causing a trip-off after having achieved at its output an overcurrent limitation for a definite trip-off time

3.2.14 LCL class

maximum allowable current that can flow through the LCL itself, under given standard conditions

NOTE LCL classes are defined in Table 3-1.

3.2.15 LCL switch dissipative failure

failure corresponding to an equivalent gate to drain short circuit on a MOSFET

NOTE The voltage across is approximately 4V to 5V maximum.

3.2.16 nominal condition

operative condition of the LCL/RLCL/HLCL, with no internal failure

3.2.17 repetitive overload

overcurrent event that repeats for a number of cycles or indefinitely

3.2.18 retriggerable latching current limiter (RLCL)

LCL that automatically attempts to switch ON when powered or after a retrigger interval when a trip-off event occurred

3.2.19 retriggerability

characteristic of an RLCL protection to be able to restart automatically after being triggered

3.2.20 retrigger interval

time duration in high impedance state of a RLCL after a permanent overcurrent event occurred and the relevant trip-off time elapsed

NOTE 1 See Figure 3-4.

NOTE 2 High impedance state is equivalent to OFF condition.

3.2.21 RLCL class

maximum allowable current that can flow through the RLCL itself, under given standard conditions

NOTE RLCL classes are defined in Table 3-2.

3.2.22 sub-feature

sub-part of a function to which a specific requirement refers

3.2.23 switch-on capability

See “Switch-on response time”.

3.2.24 switch-on response time

time needed to enable actual ON command reception, under specified conditions

3.2.25 UVP switch-off response time

time to achieve UVP action in dynamical conditions, when under voltage excitation is achieved under standard conditions

NOTE The UVP action is the OFF of the relevant function.

3.2.26 time to current overshoot

maximum time from max limitation current to actual current overshoot peak after an overcurrent event

NOTE See Figure 3-1 and Figure 3-2.

3.2.27 trip-off

event occurring when a current protection latch flips and opens the protected distribution line after an overcurrent condition

NOTE To open a distribution line means to set the distribution line in high impedance status.

3.2.28 trip-off time

time in between LCL crossing actual current limitation value and the trip-off event, in permanent overcurrent condition.

NOTE See Figure 3-1 and Figure 3-2.

3.2.29 undervoltage protection (UVP)

protection that is triggered when the voltage provided to a function falls below a predefined threshold

NOTE LCL and RLCL are examples of functions for which UVP is activated.

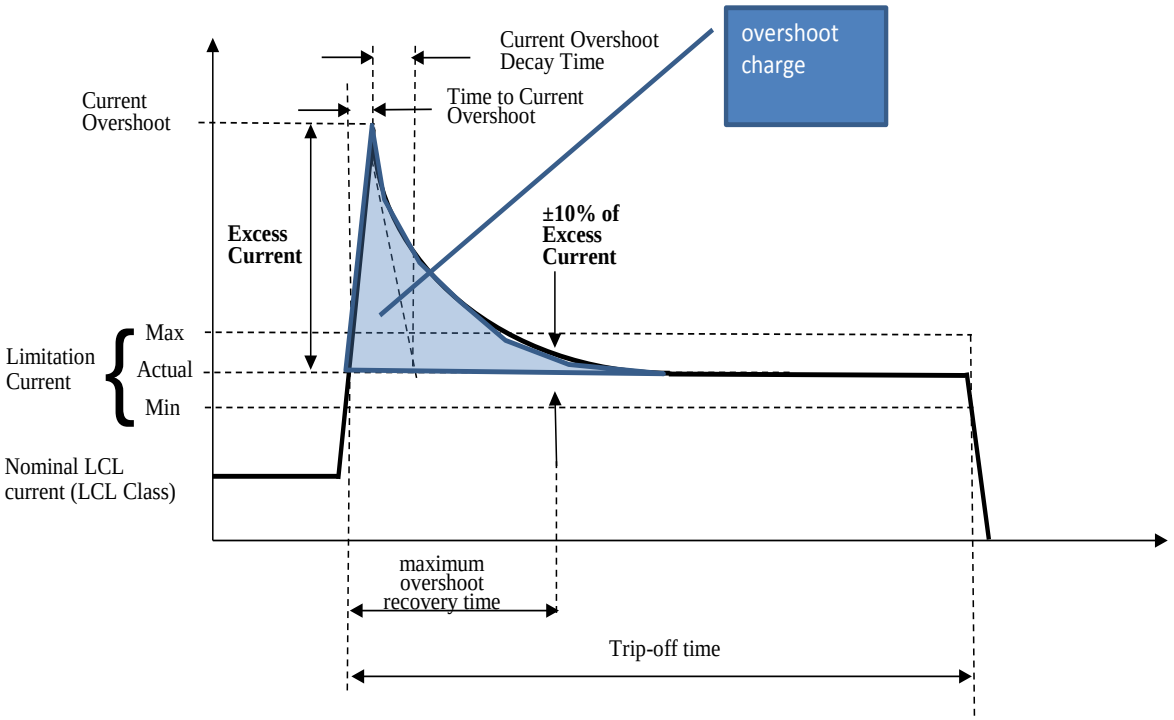

Figure 3-1: LCL overload timing diagram (case 1)

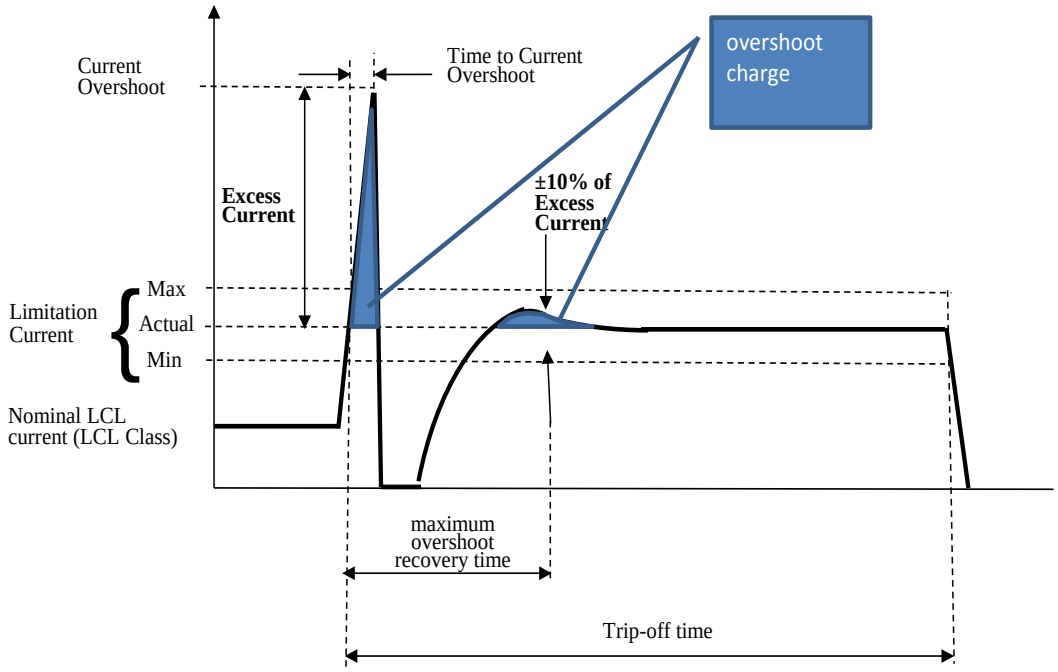

Figure 3-2: LCL overload timing diagram (case 2)

NOTE Figure 3-1 and Figure 3-2 show typical current diagrams expected when an LCL/RLCL/HLCL are subject to an overload. They can represent either the LCL/RLCL/HLCL input or output current.

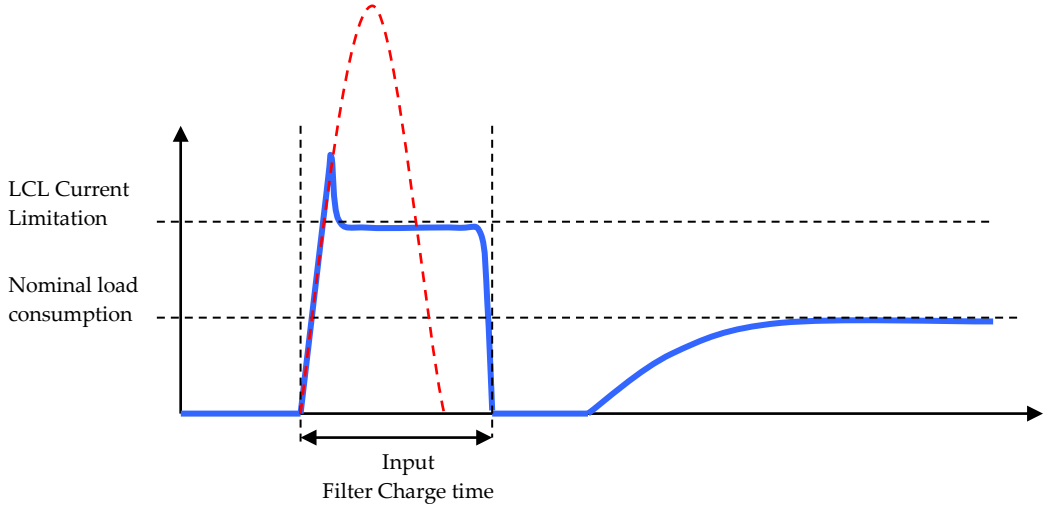

Figure 3-3: Typical start-up current profile of a DC/DC converter attached to a LCL

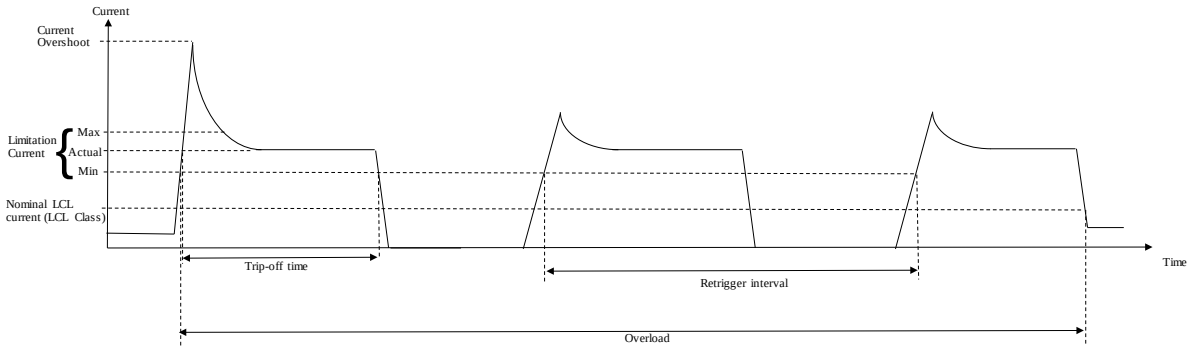

Figure 3-4: RLCL overload timing diagram

Table 3-1: LCL classes

Characteristic	LCL class								LCL class								
	1	**2**	**3**	**4**	**5**	**6**	**8**	**10**	**1**	**2**	**3**	**4A**	**4B**	**5**	**6**	**8**	**10**
Regulated Bus voltage [V]	28								50								
Unregulated Bus voltage [V]	22 to 38								32 to 52								
Class current [A]	1	2	3	4	5	6	8	10	1	2	3	4	4	5	6	8	10
Min limitation current [A]	1,1	2,2	3,3	4,4	5,5	6,6	8,8	11	1,1	2,2	3,3	4,4	4,4	5,5	6,6	8,8	11
Max limitation current [A]	1,4	2,8	4,2	5,6	7	8,4	11,2	14	1,4	2,8	4,2	5,6	5,6	7	8,4	11,2	14
Trip-off min [ms]	10	10	6	6	4	2	2	1,5	10	6	4	2	4	2	2	2	1,5
Trip-off max [ms]	20	20	12	12	8	4	4	3	20	12	8	4	8	4	4	4	3
Max load capacitance [µF]																	
Regulated bus	272	545	490	653	545	327	436	408	152	183	183	122	244	152	183	244	229
Unregulated bus	203	405	365	486	405	243	324	304	148	178	178	118	237	148	178	237	222

Table 3-2: RLCL classes

Characteristic	LCL class				LCL class			
	0,5	**1**	**2A**	**2B**	**0,5**	**1A**	**1B**	**2**
Regulated Bus voltage [V]	28				50			
Unregulated Bus voltage [V]	22 to 38				32 to 52			
Class current [A]	0,5	1	2	2	0,5	1	1	2
Min limitation current [A]	0,55	1,1	2,2	2,2	0,55	1,1	1,1	2,2
Max limitation current [A]	0,7	1,4	2,8	2,8	0,7	1,4	1,4	2,8
Trip-off min [ms]	10	10	4	10	10	4	6	4
Trip-off max [ms]	20	20	8	20	20	8	12	8
Max load capacitance [µF]								
Regulated bus	136	272	218	545	76	61	91	122
Unregulated bus	101	203	162	405	74	59	89	118

Table 3-3: HLCL classes

Characteristic	LCL class								LCL class								
	1	**2**	**3**	**4**	**5**	**6**	**8**	**10**	**1**	**2**	**3**	**4**		**5**	**6**	**8**	**10**
Regulated Bus voltage [V]	28								50								
Unregulated Bus voltage [V]	22 to 38								32 to 52								
Class current [A]	1	2	3	4	5	6	8	10	1	2	3	4		5	6	8	10
Min limitation current [A]	1,1	2,2	3,3	4,4	5,5	6,6	8,8	11	1,1	2,2	3,3	4,4		5,5	6,6	8,8	11
Max limitation current [A]	1,4	2,8	4,2	5,6	7	8,4	11,2	14	1,4	2,8	4,2	5,6		7	8,4	11,2	14
Trip-off min [ms]	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5		0,5	0,5	0,5	0,5
Trip-off max [ms]	2	2	2	2	2	2	2	2	2	2	2	2		2	2	2	2
Max parasitic capacitance [µF]																	
Regulated bus	1	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1
Unregulated bus	1	1	1	1	1	1	1	1	1	1	1	1		1	1	1	1

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
EMC	electromagnetic compatibility
ESD	electrostatic discharge
FDIR	failure detection, isolation and recovery
FIT	failure in time
FMECA	failure modes, effects, and criticality analysis
HLCL	heater latching current limiter
LCL	latching current limiter
MB	main bus
PCDU	power conditioning and distribution unit
RLCL	retriggerable latching current limiter
SC	short circuit
SEE	single event effect
SSE	space segment element
SSS	space segment subsystem
UVP	undervoltage protection

3.4 Nomenclature

The following nomenclature applies throughout this document:

a. The word “shall” is used in this Standard to express requirements. All the requirements are expressed with the word “shall”.

b. The word “should” is used in this Standard to express recommendations. All the recommendations are expressed with the word “should”.

NOTE It is expected that, during tailoring, recommendations in this document are either converted into requirements or tailored out.

c. The words “may” and “need not” are used in this Standard to express positive and negative permissions, respectively. All the positive permissions are expressed with the word “may”. All the negative permissions are expressed with the words “need not”.

d. The word "can" is used in this Standard to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS "may" and "can" have completely different meanings: "may" is normative (permission), and "can" is descriptive.

e. The present and past tenses are used in this Standard to express statements of fact, and therefore they imply descriptive text.

4
Principles

4.1 General

The indicated requirements verification (see clause 5) identifies the overall applicable methods to confirm compliance to the requirements, without explicitly explaining how the verification is split at applicability level (equipment, SSE/SSS or SSE/SSS/equipment). The verification methods suggested for the verification of the requirements are listed in Annex A.

4.2 Standard assumptions

a. The assumption for the maximum qualification temperature of the unit hosting the power distribution LCLs/RLCLs/HLCLs is 70 °C.

b. The bus voltage time derivative at bus application or removal varies from 0 V/μs to 0,1 V/ μs.

5
Requirements

5.1 Reference power bus specifications

a. The power distribution by LCLs/RLCLs shall work nominally for applicable nominal DC bus voltage range, nominal bus ripple voltage and voltage transients according to Table 5-1.

NOTE Nominally means "within the nominal functional and performance requirements".

b. The power distribution by LCLs/RLCLs shall survive for applicable abnormal DC bus voltage range and abnormal bus voltage transients according to Table 5-1.

NOTE A component is meant to survive if its rating is respected.

c. The power distribution by LCLs/RLCLs for unregulated 28V and 50V bus cases shall work nominally for applicable abnormal DC bus voltage range according to Table 5-1.

NOTE 1 The requirement 5.1c is explained by the same applicable minimum and maximum voltage limits both for nominal and abnormal (emission) DC bus voltage range for unregulated 28 V and 50 V bus cases.

NOTE 2 Nominally means "within the nominal functional and performance requirements".

d. LCLs/RLCLs shall not trip off up to maximum abnormal DC bus voltage limits as per to Table 5-1, unless the application of such limits result in an overload.

NOTE The load short circuit in presence of abnormal DC bus voltage (fault tolerance) is not taken into account.

Table 5-1: Reference Power Bus Specifications

Power Bus type :		**28V regulated bus [V]**	**50V regulated bus [V]**	**28V unregulated bus [V]**	**50V unregulated bus [V]**
Nominal DC Bus Voltage Range at regulation point	Min	28 -1%	50 -1%	22	32
	Max	28 +1%	50 +1%	38	52
Nominal DC Bus Voltage Range at load side	Min	28 -5%	50 -5%	22	38
	Max	28 +1%	50 +1%	38	52
Abnormal DC Bus voltage range	Min	0	0	0	0
	Max (fault tolerance)	N/A	N/A	40	55
	Max (fault emission)			38	52
Nominal Bus ripple voltage	Max	According to ECSS-E-ST-20		Up to ± 500 mVpp in the range of 30 Hz to 50 MHz	Up to ± 500 mVpp in the range of 30 Hz to 50 MHz
Nominal Bus voltage transients	Max	According to ECSS-E-ST-20		±1,4V for load steps of 50%, with dI/dt=1A/µs	±2,5V for load steps of 50%, with dI/dt=1A/µs
Abnormal Bus voltage transients	Max	0 to 34 max	0 to 60 max	Within Power Bus abnormal DC limits	

5.2 Functional/Source interface requirements

5.2.1 LCL/HLCL class

5.2.1.1 LCL/HLCL class

5.2.1.1.1 Nominal condition

a. The LCL class shall be selected among one shown in Table 3-1 and comply with related class performance.

NOTE The performance of the LCL classes can be achieved by using several MOSFETs in parallel.

b. The HLCL class shall be selected among one shown in Table 3-3 and comply with related class performance.

5.2.2 RLCL class

5.2.2.1 RLCL class

5.2.2.1.1 Nominal condition

a. The RLCL class shall be selected among one shown in Table 3-2 and comply with related class performance.

NOTE The performance of the LCL classes are typically achieved by using several MOSFET switches.

5.2.3 Current limitation section

5.2.3.1 Range

5.2.3.1.1 Nominal condition

a. The LCL/RLCL/HLCL shall limit the output current between the minimum and maximum limitation values.

5.2.3.2 Switch element, position

5.2.3.2.1 Nominal condition

a. For LCL/RLCL/HLCL, the switch element shall be on the hot main bus side.

5.2.3.3 Current sensing element, position

5.2.3.3.1 Nominal condition

a. For LCL/RLCL/HLCL, the current sensor element shall be on the hot main bus side.

5.2.3.4 Current limitation, LCL rating

5.2.3.4.1 Nominal condition

a. In current limitation mode, the LCL/HLCL components application shall respect the relevant rating limits.

5.2.3.5 Current limitation, RLCL derating

5.2.3.5.1 Nominal condition

a. In current limitation mode, the RLCL components application shall respect the relevant derating limits.

5.2.4 Trip-off section

5.2.4.1 Range

5.2.4.1.1 Nominal condition

a. In case the load current exceeds the relevant limit, the LCL/RLCL/HLCL shall switch-off within its trip-off time min to max range defined in Table 3-1, Table 3-2 and Table 3-3

5.2.5 UVP section

5.2.5.1 Provision

5.2.5.1.1 Nominal condition

a. The LCL/RLCL/HLCL shall be provided with an input UVP.

5.2.5.2 Unregulated bus case

5.2.5.2.1 Nominal condition

a. For RLCL, UVP shall be provided with hysteresis.

b. For LCL/HLCL, UVP should be provided with hysteresis.

5.2.5.3 Centralised protection

5.2.5.3.1 Nominal condition

a. In case of centralised protection for several LCLs/RLCLs/HLCLs, UVP shall be implemented as Single Point Failure Free.

5.2.6 Telecommand section features

5.2.6.1 Commandability

5.2.6.1.1 Nominal condition

a. The LCL/HLCL shall be ON/OFF commandable.

5.2.6.2 Retrigger function

5.2.6.2.1 Nominal condition

a. It shall be possible to enable or disable the retriggering function of the RLCL.

5.2.6.3 Retrigger ENABLE

5.2.6.3.1 Nominal condition

a. The retrigger function of an RLCL shall be enabled by default.

5.2.6.4 Retrigger DISABLE

5.2.6.4.1 Nominal condition

a. The disable command to a retrigger function of an RLCL feeding an essential load shall only be provided by ground.

NOTE 1 Provision by ground command does not imply necessarily a discrete direct command or similar, but just that the command is not issued as a result of an automatic procedure (e.g. FDIR).

NOTE 2 Examples of essential loads are the receiver and the decoder.

5.2.7 Conditions at start-up/ switch-off

5.2.7.1 Auto ON

5.2.7.1.1 Nominal condition

a. An RLCL shall always start in ON condition.

5.2.7.2 Auto OFF

5.2.7.2.1 Nominal condition

a. An LCL/HLCL should always start in OFF conditions.

5.2.7.3 LCL start-up with an internal failure

5.2.7.3.1 Fault condition

a. After a failure, no propagation outside the failed LCL/RLCL/HLCL shall occur. For this purpose in this case, LCL/RLCL/HLCL components blocking failure propagation shall meet their applicable derating.

NOTE When an internal failure of the LCL caused the trip-off of the LCL, the power bus needs to be protected if the operator or an automatic restart circuit or routine attempts to turn it on again, or at the next occurrence of bus power-up.

5.2.7.4 LCL status at start-up

5.2.7.4.1 Nominal condition

a. The actual LCL/RLCL/HLCL status shall not deviate from the programmed/intended one during MB start-up or recovery from zero volt.

5.2.7.5 LCL start-up on SC 1

5.2.7.5.1 Nominal condition

a. The LCL/RLCL/HLCL shall start up correctly, and within applicable rating/derating limits, when an overload or short circuit is already present at its output.

5.2.7.6 LCL start-up on SC 2

5.2.7.6.1 Nominal condition

a. Requirement 5.2.7.5.1a shall apply both in case of the LCL/HLCL being commanded ON by telecommand and when the bus voltage rises for the RLCL.

5.2.7.7 Switch-off

5.2.7.7.1 Nominal condition

a. The LCL/RLCL/HLCL shall contain a provision to free wheel the current circulating in the load or harness inductance, when the LCL/RLCL is either commanded OFF or when it opens the line after an overload.

5.2.8 Telemetry section

5.2.8.1 LCL status

5.2.8.1.1 Nominal condition

a. The LCL/HLCL/RLCL ON/OFF status shall confirm that the LCL/RLCL/HLCL output voltage is within its nominal range.

5.2.8.2 Current telemetry

5.2.8.2.1 Nominal condition

a. An LCL/RLCL/HLCL shall provide current telemetry.

5.2.8.3 Current telemetry, full scale reading

5.2.8.3.1 Nominal condition

a. Full scale of current TM shall be at least equal to the maximum LCL/RLCL/HLCL limitation current.

5.2.8.4 Current telemetry, linearity and accuracy

5.2.8.4.1 Nominal condition

a. For LCL/RLCL/HLCL, the current TM shall be linear and have an absolute accuracy referred to the class current and applicable on the full range of the TM.

NOTE Telemetry accuracy is detailed in 5.4.7.1.1a.

5.2.8.5 Current telemetry, offset

5.2.8.5.1 Nominal condition

a. For LCL/RLCL/HLCL, the current TM offset shall be referred to the class current.

NOTE Offset performance is defined in 5.4.8.1.1a.

5.2.8.6 Current telemetry, reading at zero current

5.2.8.6.1 Nominal condition

a. For LCL/RLCL/HLCL, the current TM should be able to read down to zero current within the specified accuracy.

NOTE Telemetry accuracy is detailed in requirement 5.4.7.1.1a.

5.2.8.7 Current telemetry, verification

5.2.8.7.1 Nominal condition

a. For LCL/RLCL/HLCL, if requirement 5.2.8.6.1a is met, then the accuracy shall be verified at 0%, 50% and 100% of the class current, else the accuracy shall be verified at 0%, 10%, 50% and 100% of the class current.

5.2.9 Status section

5.2.9.1 LCL status under failed conditions

5.2.9.1.1 Fault condition

a. The capability of reading the correct LCL/RLCL/HLCL status shall not be impacted by any failure in the command interface of the LCL/RLCL/HLCL itself.

5.2.10 Repetitive overload

5.2.10.1 LCL case

5.2.10.1.1 Nominal case

a. The LCL shall correctly operate the application of repetitive overload conditions within the applicable rating/derating limits.

NOTE For instance hiccup between LCL and UVP of the function supplied by the LCL. In absence of specific needs, the approach described in ECSS-E-HB-20-20 section 5.7.2.6 can conveniently be used (e.g. ensuring a ratio of 30 between the countdown and count up time constant of the LCL trip-off counter).

5.2.10.2 RLCL case

5.2.10.2.1 Nominal case

a. The RLCL shall correctly operate the application of repetitive overload conditions within the applicable derating limits.

NOTE For instance hiccup between RLCL and UVP of the function supplied by the RLCL. In absence of specific needs, the approach described in ECSS-E-HB-20-20 section 5.7.2.6 can conveniently be used (e.g. ensuring a ratio of 30 between the count down and count up time constant of the RLCL trip-off counter).

5.2.11 Reverse current tolerance

5.2.11.1 Reverse current tolerance

5.2.11.1.1 Nominal case

a. The LCL design should be capable to withstand the application of reverse current by the load, both in ON and in OFF conditions.

5.2.12 Parallel connection

5.2.12.1 LCLs in parallel

5.2.12.1.1 Nominal case

a. It should be possible to put LCLs/HLCLs in parallel.

5.2.12.2 LCLs in parallel and current sharing

5.2.12.2.1 Nominal case

a. When two or more LCLs/RLCLs/HLCLs are put in parallel, the current sharing accuracy shall be correctly assessed to avoid unwanted tripping-off of the LCLs themselves.

NOTE The overall limitation current of two or more LCLs in parallel is usually smaller than the sum of the individual LCLs limitation currents.

5.2.12.3 LCLs in parallel and trip-off

5.2.12.3.1 Nominal case

a. When two or more LCLs/RLCLs/HLCLs are put in parallel, the overall trip-off time shall be correctly assessed to avoid unwanted tripping-off of the LCLs/RLCLs/HLCLs themselves.

5.2.12.4 LCLs in parallel and ON/OFF command

5.2.12.4.1 Nominal case

a. When two or more LCLs/HLCLs are put in parallel, the ON/OFF command shall be made common to all of them.

5.2.12.5 LCLs in parallel and current telemetry

5.2.12.5.1 Nominal case

a. When two or more LCLs/RLCLs/HLCLs are put in parallel, the current telemetry shall provide the overall current flowing through them.

5.2.13 Switching options

5.2.13.1 No additional switching capability

5.2.13.1.1 Fault case

a. For LCL/HLCL, if no additional switching capability is provided as per 5.2.13.3.1a, the power budget shall cover the LCL/HLCL switch failure by considering the actual MB maximum load, plus eventually the unwanted load connected to the failed LCL/HLCL, in the following cases:

1. all the load operational modes imply a non-negligible power consumption;

2. the load operational modes cannot be directly commanded by an autonomous, on board load shedding routine to be triggered by abnormal bus load consumption.

NOTE 1 In case the load power consumption is negligible, refer to requirement 5.2.13.2.1a.

NOTE 2 The LCL switch is the only switch in the relevant distribution line.

5.2.13.2 No additional switching capability, negligible load power consumption mode

5.2.13.2.1 Nominal case

a. For LCL/HLCL, the load power consumption considered as negligible in terms of power budget shall be specified by the system integrator.

NOTE The "negligible" power consumption is intended as the one that can be drawn from the power bus without the system integrator or system responsible being forced to disconnect it.
Such power level is indeed added to the power budget.

5.2.13.3 Additional switching capability

5.2.13.3.1 Nominal and fault cases

a. For LCL/HLCL, in case that there is an additional switch that can be commanded open in any case when the LCL/HLCL switch is in ON state or fails ON or in short circuit, requirements 5.2.13.4.1a and 5.2.13.5.1a should be fulfilled.

b. It shall be possible to command the LCL/HLCL and the relevant additional switch in series by a different, individual command, or a different commanding path.

5.2.13.4 Additional switching capability, location of additional switch

5.2.13.4.1 Nominal and fault cases

a. For LCL, the additional switch should be put on power system LCL side.

5.2.13.5 Additional switching capability, UVP acting on additional switch

5.2.13.5.1 Nominal and fault cases

a. For LCL, the UVP should act both on the LCL switch and on the additional switch provided by an independent memory cell.

NOTE Each switch which is supposed to maintain its ON (or OFF) status is provided with a memory cell (a flip-flop or other). See Figures 5-29 and 5-30 of ECSS-E-HB-20-20.

5.2.14 LCL Switch dissipative failure

5.2.14.1 Steady state condition

5.2.14.1.1 Fault case

a. In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case no other protection removes the failure, all the surrounding components shall be within derating.

NOTE Surrounding components are the ones not relevant to the failed LCL.

5.2.14.2 Transient condition

5.2.14.2.1 Fault case

a. In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case the "on board system" removes the failure by reducing the load or commanding OFF an additional switch, all the surrounding components shall be within rating during the on board system reaction time.

5.2.14.3 Local protection

5.2.14.3.1 Fault case

a. In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case requirements 5.2.14.1.1a and 5.2.14.2.1a cannot be fulfilled, a protection shall be embedded in the LCL or in the Distribution Unit to avoid a failure propagation due to the abnormal heat dissipation.

5.2.15 Loss of LCL lines

5.2.15.1 Loss of LCL lines

5.2.15.1.1 Fault case

a. In case of a single failure, no more than one LCL/RLCL/HLCL line shall be lost.

5.2.16 Noise immunity

5.2.16.1 General

5.2.16.1.1 Nominal case

a. The LCL/RLCL/HLCL state shall not change from the commanded one due to spurious perturbations, including:

1. EM emissions, both conducted and radiated,
2. SEE,
3. ESD,
4. ON/OFF commands to other LCL/RLCL lines, and
5. Overcurrent events to other LCL/RLCL lines.

5.2.16.2 Verification

5.2.16.2.1 Nominal case

a. Requirement 5.2.16.1.1a shall be verified at unit level and/or at system level: points 1, 3, 4, 5 at unit level and points 1, 4 at system level.

b. Requirement 5.2.16.1.1a point 2 shall be verified by analysis.

5.2.17 Output impedance envelope, when in limitation

5.2.17.1 Value

5.2.17.1.1 Nominal case

a. The LCL/RLCL/HLCL output impedance in terms of both gain and phase shall be provided per LCL/RLCL/HLCL class, between 100 Hz and 1 MHz.

NOTE Tests cases are described in ECSS-E-HB-20-20.

5.2.17.2 Verification

5.2.17.2.1 Nominal case

a. The LCL/RLCL/HLCL output impedance shall be provided for a voltage across the LCL/RLCL/HLCL equal to (4 ±1) V.

NOTE Tests cases are defined in ECSS-E-HB-20-20.

5.2.18 Noise immunity feature

5.2.18.1 RLCL spurious switch-off

5.2.18.1.1 Nominal case

a. The RLCL state shall automatically be recovered to ON conditions after a spurious switch-off.

NOTE The status recovery can be implemented by hardware or software means, at system, subsystem or unit level.

5.2.18.2 RLCL spurious effects

5.2.18.2.1 Nominal case

a. Spurious disable of RLCL retriggering memory cell and of RLCL ON/OFF status memory cell shall not result in the loss of the relevant load.

5.2.19 Output LCL load (Input load characteristic)

5.2.19.1 Load inductance

5.2.19.1.1 Nominal case

a. The LCL/RLCL/HLCL shall work nominally for any load inductance from zero to the maximum specified in 5.5.2.1.1a for LCL/RLCL or in 5.5.2.1.1b for HLCL.

NOTE Test verification is made with some inductance values (e.g. min/avg/max) and not for all values from 0 to max.

5.2.19.2 Load capacitance

5.2.19.2.1 Nominal case

a. The LCL/RLCL/HLCL shall work nominally for any load capacitance from zero to the maximum specified in Table 3-1, Table 3-2 and Table 3-3 respectively.

NOTE Test verification is made with some capacitance values (e.g. min/avg/max) and not for all values from 0 to max.

5.3 Functional/Load interface requirements

5.3.1 Nominal feature

5.3.1.1 Load behaviour

5.3.1.1.1 Nominal case

a. During nominal operation after switch-on, the load current for LCL/RLCL/HLCL shall always be smaller than the correspondent class current.

b. Requirement 5.3.1.1.1a shall be valid also in the following conditions:

1. the bus voltage transients are applied, and
2. the MB voltage ripple is considered, and
3. there are load-conducted emissions as per the EMC specification.

NOTE Further details can be found in ECSS-E-HB-20-20 section 5.7.3.4.1.

5.3.2 Switch-on

5.3.2.1 Load behaviour 1

5.3.2.1.1 Nominal case

a. During Switch-on, the load current shall not exceed the LCL/RLCL class current except for charging the relevant input filter.

5.3.2.2 Load behaviour 2

5.3.2.2.1 Nominal case

a. Converters contained in the load shall start up without the load current to exceed the LCL/RLCL class current.

5.3.2.3 Input filter charging

5.3.2.3.1 Nominal case

a. If the LCL/RLCL current limit is reached, the load input filter shall be completely charged within the relevant LCL/RLCL maximum charge time defined in requirement 5.4.2.3.1a.

5.3.3 LCL switch dissipative failure

5.3.3.1 Steady state condition, load

5.3.3.1.1 Fault case

a. In case the LCL/RLCL switch fails in a dissipative failure mode, the load shall perform one of the following actions:

   1. work nominally,
   2. enter autonomously a safe operating condition, or
   3. survive the condition without abnormal conducted or radiated emissions.

      NOTE The issue in an LCL/RLCL switch failing in dissipative mode is the additional power line voltage drop.

5.3.4 Load test condition

5.3.4.1 Load test condition

5.3.4.1.1 Nominal case

a. A representative LCL/RLCL interface should be used during the standalone tests of any load connected to it.

   NOTE The specific LCL/RLCL load compatibility tests are defined on a case-by-case basis.

5.3.5 User UVP at bus input side

5.3.5.1 User UVP at bus input side

5.3.5.1.1 Nominal case

a. In case an UVP at load side is present, the repetitive overload pattern that can result from the interaction with the LCL/RLCL shall be studied as part of the FMECA.

5.4 Performance/Source interface requirements

5.4.1 Overall requirements

5.4.1.1 Current overshoot

5.4.1.1.1 Nominal case

a. The input or output current overshoot when an overload is applied to the LCL/RLCL/HLCL shall be lower than 50 A, when evaluated in the conditions specified in req. 5.4.1.1.1b.

NOTE Refer to Figure 3-1 and/or Figure 3-2.

b. The worst case overload condition applied for the verification shall be a sudden short-circuit applied at the LCL Distribution Unit connector interface.

c. The time to current overshoot for LCL/RLCL/HLCL shall be 5 µs maximum, when evaluated in the conditions specified in req. 5.4.1.1.1b.

NOTE Refer to Figure 3-1 and/or Figure 3-2.

d. The current overshoot recovery time for LCL/RLCL/HLCL shall be 300 µs maximum, when evaluated in the conditions specified in req. 5.4.1.1.1b.

NOTE Refer to Figure 3-1 and/or Figure 3-2.

e. The maximum LCL/RLCL input overshoot charge due to any overload shall be limited to 1 mC maximum.

NOTE Refer to Figure 3-1 and/or Figure 3-2.

f. The maximum input overshoot charge due to an overload, as per 5.4.1.1.1e., shall be complied for any load inductance value from zero to the maximum specified in 5.5.2.1.1a for LCL/RLCL, or in 5.5.2.1.1b for HLCL.

NOTE Test verification is made with some inductance values (e.g. min/avg/max) and not for all values from 0 to max.

5.4.1.2 Reverse current tolerance

5.4.1.2.1 Nominal case

a. In case the reverse current functional requirement 5.2.11.1.1a is applied, the reverse current peak tolerance shall be equal to the LCL class current, with linear decay of 10 minutes maximum.

NOTE Linear decay time is indicative, the thermal situation for the LCL is close to the steady state during this transient.

5.4.1.3 Leakage current

5.4.1.3.1 Nominal case

a. Maximum leakage current for LCL/RLCL/HLCL shall be 100 μA.

b. The voltage appearing at the LCL/RLCL/HLCL output in OFF state shall be lower than 1V.

5.4.1.4 Time interval between successive ON commands

5.4.1.4.1 Nominal case

a. The minimum time between two successive external LCL/HLCL ON commands shall be 1 s.

5.4.2 Start-up/Switch-off requirements

5.4.2.1 Start-up current rate

5.4.2.1.1 Nominal case

a. Maximum LCL/RLCL/HLCL start-up current rate dI/dt shall be 1A/μs.

5.4.2.2 Switch-off current rate

5.4.2.2.1 Nominal case

a. Maximum LCL/RLCL/HLCL switch-off current rate dI/dt shall be 1A/μs.

5.4.2.3 Load input filter charge time

5.4.2.3.1 Nominal case

a. The load input filter charge time shall be maximum 80 % of LCL/RLCL class minimum trip-off time when:

1. operating in worst-case conditions;
2. the minimum LCL/RLCL class limitation current is chosen.

5.4.2.4 Output, auto start OFF, amplitude

5.4.2.4.1 Nominal case

a. The amplitude of the pulse appearing at LCL/HLCL output during main bus start-up shall not exceed 5 V.

b. Requirement 5.4.2.4.1a shall be valid for any applicable main bus voltage derivative at start-up and when minimum load is applied.

NOTE See clause 4.2 to have an insight into the standard assumptions.

5.4.2.5 Output, auto start OFF, duration

5.4.2.5.1 Nominal case

a. The duration of the pulse appearing at LCL/HLCL output during main bus start-up shall not exceed 1 ms.

b. Requirement 5.4.2.5.1a shall be valid for any applicable main bus voltage derivative at start-up and when minimum load is applied.

NOTE See clause 4.2 to have an insight into the standard assumptions.

5.4.3 UVP

5.4.3.1 Switch-off threshold, regulated bus

5.4.3.1.1 Nominal case

a. The LCL/RLCL/HLCL switch-off threshold shall be configurable on ground from 80 % of the nominal bus voltage value.

5.4.3.2 Switch-off threshold, unregulated bus

5.4.3.2.1 Nominal case

a. The LCL/RLCL/HLCL switch-off threshold shall be configurable on ground from 50 % of the nominal DC maximum bus voltage value.

5.4.3.3 UVP noise immunity

5.4.3.3.1 Nominal case

a. For LCL/RLCL/HLCL, the UVP shall not react for an undervoltage event lasting less than 500 μs.

5.4.3.4 UVP noise immunity, verification

5.4.3.4.1 Nominal case

a. For LCL/RLCL/HLCL, the UVP noise immunity shall be verified by applying a voltage step from nominal bus voltage to 80 % of nominal DC switch-off threshold with a fall time equal or smaller than 1 % of the actual UVP reaction time.

NOTE The test point is selected taking into account that the reaction time does not include the delay between the UVP output and the OFF command issuing the LCL output voltage cut-off.

5.4.3.5 UVP hysteresis

5.4.3.5.1 Nominal case

a. If UVP hysteresis is implemented, the difference between the actual UVP switch-off threshold, and relevant enabled ON threshold, shall be higher than 0,5 V.

5.4.4 Switch-on capability

5.4.4.1 Enable ON threshold Voltage, regulated bus

5.4.4.1.1 Nominal case

a. The LCL/RLCL/HLCL enable ON threshold shall be configurable up to 95 % of the nominal main bus voltage.

5.4.4.2 Enable ON threshold Voltage, unregulated bus

5.4.4.2.1 Nominal case

a. The LCL/RLCL/HLCL enable ON threshold shall be configurable up to 90 % of the nominal DC maximum bus voltage value.

5.4.4.3 Switch-on response time, value

5.4.4.3.1 Nominal case

a. The RLCL shall not switch ON when relevant threshold is reached for less than 500 μs.

5.4.4.4 Switch-on response time, verification

5.4.4.4.1 Nominal case

a. The RLCL Switch-on response time shall be verified by the application of a voltage step from 80 % of nominal DC switch-off threshold to nominal bus voltage with a rise time equal or smaller than 1 % of the actual Switch-on response time.

NOTE The test point is selected taking into account that the reaction time does not include the delay between the switch-on circuitry signal output and the actual RLCL output voltage increase.

5.4.5 Voltage drop

5.4.5.1 Voltage drop

5.4.5.1.1 Nominal case

a. The voltage drop of LCL/RLCL line shall not exceed 1 % of the nominal main bus voltage at the relevant class current.

b. The voltage drop of an HLCL/LCL with an additional switch shall not exceed 2 % of the nominal main bus voltage at the relevant class current.

c. The LCL/RLCL/HLCL voltage drop shall be measured from central regulation point to the output connector.

5.4.6 Stability

5.4.6.1 Frequency domain, phase margin

5.4.6.1.1 Nominal case

a. Minimum phase margin for LCL/RLCL/HLCL shall be 50°, under the following conditions:

1. a zero Ohm impedance load is applied, and
2. the DC voltage across the LCL/RLCL/HLCL equals (4 ±1) V.

NOTE The zero Ohm impedance is implemented by a voltage source with current sink capability.

5.4.6.2 Frequency domain, gain margin

5.4.6.2.1 Nominal case

a. Minimum gain margin for LCL/RLCL/HLCL shall be 10 dB under the following conditions:

1. a zero Ohm impedance load is applied, and
2. the DC voltage across the LCL/RLCL/HLCL equals (4 ±1) V.

NOTE The zero Ohm impedance is implemented by a voltage source with current sink capability.

5.4.6.3 Time domain, transient from non-limiting mode to current limitation mode

5.4.6.3.1 Nominal case

a. For any specified inductive load, no persistent voltage or current oscillation shall occur when the LCL/RLCL/HLCL is applied a sudden overload.

NOTE Requirements on inductive load are detailed in 5.2.19.1.1a , 5.5.2.1.1a and 5.5.2.1.1b.

b. The period of observed oscillation as per requirement 5.4.6.3.1a shall be greater or equal to the envelope decay time.

NOTE Test verification for 5.4.6.3.1a and 5.4.6.3.1b is done on the basis of the analysis, which is used to identify the worst case inductance to be applied.

5.4.6.4 Time domain, start-up transient to current limitation mode

5.4.6.4.1 Nominal case

a. For any specified inductive or capacitive load, no persistent voltage or current oscillation shall occur when the LCL/RLCL/HLCL is starting up in current limitation.

NOTE Requirements on inductive and capacitive loads are detailed in 5.2.19.1.1a, 5.5.2.1.1a, 5.5.2.1.1b, 5.2.19.2.1a and 5.5.2.2.1a.

b. The period of observed oscillation as per requirement 5.4.6.4.1a shall be greater or equal to the envelope decay time.

NOTE Test verification for 5.4.6.4.1a and 5.4.6.4.1b is done on the basis of the analysis, which is used to identify the worst case capacitance and inductance to be applied

5.4.7 Current Telemetry, accuracy

5.4.7.1 Current Telemetry, accuracy

5.4.7.1.1 Nominal case

a. For LCL/RLCL/HLCL, the accuracy of the current telemetry shall be equal or better than ±4 % of the full scale value in worst case.

5.4.8 Current Telemetry, offset

5.4.8.1 Current Telemetry, offset

5.4.8.1.1 Nominal case

a. If functional requirement 5.2.8.6.1a is not met, for LCL/RLCL/HLCL the offset of the current telemetry shall be equal or better than ±4 % of the full scale value in worst case.

5.4.9 Retrigger interval

5.4.9.1 Retrigger interval

5.4.9.1.1 Nominal case

a. For RLCL, the minimum retrigger interval shall be 20 s unless a specific RLCL memory cell for latched trip-off status is provided.

5.4.10 dI/dt limit on retrigger ON edge

5.4.10.1 dI/dt limit on retrigger ON edge

5.4.10.1.1 Nominal case

a. For RLCL, the maximum value of dI/dt rate on retrigger ON edge shall be 1 A/μs.

5.4.11 dI/dt limit on retrigger OFF edge

5.4.11.1 dI/dt limit on retrigger OFF edge

5.4.11.1.1 Nominal case

a. For RLCL, the maximum value of dI/dt rate on retrigger OFF edge shall be 1 A/μs.

5.4.12 Status, accuracy

5.4.12.1 Nominal condition

a. The LCL/RLCL/HLCL ON/OFF status shall confirm that the LCL/RLCL/HLCL output voltage is within its nominal range with an accuracy of ±10 %.

5.5 Performance/Load interface requirements

5.5.1 Load reverse current

5.5.1.1 Avoidance

5.5.1.1.1 Nominal case

a. For LCL/RLCL, a load should not reinject current into the bus.

5.5.1.2 Reinjection current

5.5.1.2.1 Nominal case

a. In case requirement 5.2.11.1.1a is complied, the maximum current reinjected to the LCL shall be equal to the LCL class current, with linear decay of 10 minutes maximum.

NOTE Linear decay time is indicative, the thermal situation for the LCL is close to the steady state during this transient.

5.5.2 Load characteristic

5.5.2.1 Maximum inductance

5.5.2.1.1 Nominal case

a. The maximum inductance, including the harness between LCL/RLCL and load, and including the input load filter, shall be 300 μH.

b. The maximum inductance, including the harness between HLCL and load, and including the input load filter, shall be 50 μH.

5.5.2.2 Maximum capacitance

5.5.2.2.1 Nominal case

a. The maximum capacitance for LCL and RLCL shall be compatible with the one shown in Table 3-1 and Table 3-2 respectively.

b. The maximum capacitance for HLCL shall be compatible with the one shown in Table 3-3.

5.5.2.3 Load impedance envelope

5.5.2.3.1 Nominal case

a. For LCL/RLCL, the supplier shall provide to the customer the load impedance envelope, expressed in terms of magnitude and phase, for a frequency range from 100 Hz to 1 MHz.

5.5.3 Source-load characteristic

5.5.3.1 Source-load impedance phase margin

5.5.3.1.1 Nominal case

a. For LCL/RLCL, at those frequencies in which the load and the source impedance are equal in magnitude, the difference between the load impedance phase and the source impedance phase shall be greater than abs(±150°±n*360°).

NOTE n is a positive integer including 0,
abs is the absolute value operator.

5.5.3.2 Source-load impedance gain margin

5.5.3.2.1 Nominal case

a. For LCL/RLCL, at those frequencies in which the difference between the load impedance phase and the source impedance phase is equal to -180°±n*360°, the difference between the load impedance gain and the LCL impedance gain shall be greater than 5 dB.

NOTE n is a positive integer including 0.

5.5.4 Start-up surge input current

5.5.4.1 Start-up surge input current

5.5.4.1.1 Fault case

a. In case of an LCL/RLCL failure causing a sudden application of nominal voltage to the load, the relevant peak current shall be lower than 20 A or 5 times the class current, whichever is greater.

b. The peak current shall be compatible with the electrical and thermal stress of:

1. the LCL/RLCL,
2. the load input filter components, and
3. the relevant main bus disturbance.

5.5.5 Internal load Input current limitation

5.5.5.1 Internal load Input current limitation

5.5.5.1.1 Nominal case

a. If an internal current limitation is used in the load, the relevant overall current limit shall be at maximum equal to the class current of the relevant LCL/RLCL.

Annex A (informative) Requirements mapping

Table A-1 to Table A-4 provide a compact view of the requirements of the present standard, including the verification method suggested for each of them. According to ECSS-E-ST-10-02, the verification is accomplished by one or more of the following verification methods:

a. Test (T),

b. Analysis (A),

c. Review-of-design (RoD), and

d. Inspection (I).

In addition to the methods of verification specified in ECSS-E-ST-10-02, the present annex includes the test verification at design qualification level (T*).

The test verification at design qualification level (T*) is intended to be performed on an electrical representative version of the hardware, on a set up not necessarily equal to the final flight one, to be established for the LCL distribution product line by the relevant manufacturer.

NOTE If not stated otherwise, any reference to the handbook inside the tables, is a reference to ECSS-E-HB-20-20.

Level 3 heading in this standard (for example, 5.2.14 “LCL Switch dissipative failure”) is reported as “feature” in Table A-1 to Table A-4.

Level 4 heading in this standard (for example, 5.2.14.1 “Steady state condition”) is reported as “sub-feature” in Table A-1 to Table A-4.

The suggested applicability level indicated in Table A-1 to Table A-4 (SSE/SSS/Equipment) is intended in and/or-option (SSE and/or SSS and/or Equipment).

Table A-1: Functional/Source requirements list

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.1.1.1a	The LCL class shall be selected among one shown in Table 3-1 and comply with related class performance.	LCL/HLCL class	LCL/HLCL class	Nominal	LCL	SSE/SSS	RoD
5.2.1.1.1b	The HLCL class shall be selected among one shown in Table 3-3 and comply with related class performance.	LCL/HLCL class	LCL/HLCL class	Nominal	HLCL	SSE/SSS	RoD
5.2.2.1.1a	The RLCL class shall be selected among one shown in Table 3-2 and comply with related class performance.	RLCL class	RLCL class	Nominal	RLCL	SSE/SSS	RoD
5.2.3.1.1a	The LCL/RLCL/HLCL shall limit the output current between the minimum and maximum limitation values.	Current limitation section	Range	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	RoD, A, T
5.2.3.2.1a	For LCL/RLCL/HLCL, the switch element shall be on the hot main bus side.		Switch element, position	Nominal	LCL/RLCL/HLCL	Equipment	RoD
5.2.3.3.1a	For LCL/RLCL/HLCL, the current sensor element shall be on the hot main bus side.		Current sensing element, position	Nominal	LCL/RLCL/HLCL	Equipment	RoD
5.2.3.4.1a	In current limitation mode, the LCL/HLCL components application shall respect the relevant rating limits.		Current limitation, LCL rating	Nominal	LCL/HLCL	Equipment	A
5.2.3.5.1a	In current limitation mode, the RLCL components application shall respect the relevant derating limits.		Current limitation, RLCL derating	Nominal	RLCL	Equipment	A
5.2.4.1.1a	In case the load current exceeds the relevant limit, the LCL/RLCL/HLCL shall switch-off within its trip-off time min to max range defined in Table 3-1, Table 3-2 and Table 3-3	Trip –off section	Range	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	RoD, A, T
5.2.5.1.1a	The LCL/RLCL/HLCL shall be provided with an input UVP.	UVP section	Provision	Nominal	LCL/RLCL/HLCL	Equipment	RoD
5.2.5.2.1a	For RLCL, UVP shall be provided with hysteresis.		Unregulated bus case	Nominal	RLCL	Equipment	RoD
5.2.5.2.1b	For LCL/HLCL, UVP should be provided with hysteresis.		Unregulated bus case	Nominal	LCL/HLCL	Equipment	RoD
5.2.5.3.1a	In case of centralised protection for several LCLs/RLCLs/HLCLs, UVP shall be implemented as Single Point Failure Free.		Centralised protection	Nominal	LCL/RLCL/HLCL	Equipment	RoD, A
5.2.6.1.1a	The LCL/HLCL shall be ON/OFF commandable.	Telecommand section features	Commandability	Nominal	LCL/HLCL	SSE/SSS/Equipment	RoD
5.2.6.2.1a	It shall be possible to enable or disable the retriggering function of the RLCL.		Retrigger function	Nominal	RLCL	SSE/SSS/Equipment	RoD, T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.6.3.1a	The retrigger function of an RLCL shall be enabled by default.		Retrigger ENABLE	Nominal	RLCL	SSE/SSS/Equipment	RoD, T
5.2.6.4.1a	The disable command to a retrigger function of an RLCL feeding an essential load shall only be provided by ground.		Retrigger DISABLE	Nominal	RLCL	SSE/SSS	RoD, T
5.2.7.1.1a	An RLCL shall always start in ON condition.	Conditions at start-up / switch-off	Auto ON	Nominal	RLCL	SSE/SSS/Equipment	RoD, T
5.2.7.2.1a	An LCL/HLCL should always start in OFF conditions.		Auto OFF	Nominal	LCL/HLCL	SSE/SSS/Equipment	RoD, T
5.2.7.3.1a	After a failure, no propagation outside the failed LCL/RLCL/HLCL shall occur. For this purpose in this case, LCL/RLCL/HLCL components blocking failure propagation shall meet their applicable derating.		LCL start-up with an internal failure	Fault	LCL/RLCL/HLCL	Equipment	A
5.2.7.4.1a	The actual LCL/RLCL/HLCL status shall not deviate from the programmed/intended one during MB start-up or recovery from zero volt.		LCL status at start-up	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	A,T
5.2.7.5.1a	The LCL/RLCL/HLCL shall start up correctly, and within applicable rating/derating limits, when an overload or short circuit is already present at its output.		Start-up on short circuit 1	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.7.6.1a	Requirement 5.2.7.5.1a shall apply both in case of the LCL/HLCL being commanded ON by telecommand and when the bus voltage rises for the RLCL.		Start-up on short circuit 2	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.7.7.1a	The LCL/RLCL/HLCL shall contain a provision to free wheel the current circulating in the load or harness inductance, when the LCL/RLCL is either commanded OFF or when it opens the line after an overload		Switch-off	Nominal	LCL/RLCL/HLCL	Equipment	RoD
5.2.8.1.1a	The LCL/HLCL/RLCL ON/OFF status shall confirm that the LCL/RLCL/HLCL output voltage is within its nominal range.	Telemetry Section	LCL status	Nominal	LCL/RLCL/HLCL	Equipment	T
5.2.8.2.1a	An LCL/RLCL/HLCL shall provide current telemetry.		Current telemetry	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	RoD
5.2.8.3.1a	Full scale of current TM shall be at least equal to the maximum LCL/RLCL/HLCL limitation current.		Current telemetry, full scale reading	Nominal	LCL/RLCL/HLCL	Equipment	RoD
5.2.8.4.1a	For LCL/RLCL/HLCL, the current TM shall be linear and have an absolute accuracy referred to the class current and applicable on the full range of the TM.		Current telemetry, linearity and accuracy	Nominal	LCL/RLCL/HLCL	Equipment	A,T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.8.5.1a	For LCL/RLCL/HLCL, the current TM offset shall be referred to the class current.		Current telemetry, offset	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.8.6.1a	For LCL/RLCL/HLCL, the current TM should be able to read down to zero current within the specified accuracy.		Current telemetry, reading at zero current	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.8.7.1a	For LCL/RLCL/HLCL, if requirement 5.2.8.6.1a is met, then the accuracy shall be verified at 0%, 50% and 100% of the class current, else the accuracy shall be verified at 0%, 10%, 50% and 100% of the class current.		Current telemetry, verification	Nominal	LCL/RLCL/HLCL	Equipment	A, T
5.2.9.1.1a	The capability of reading the correct LCL/RLCL/HLCL status shall not be impacted by any failure in the command interface of the LCL/RLCL/HLCL itself.	Status section	LCL status under failed conditions	Fault	LCL/RLCL/HLCL	Equipment	A
5.2.10.1.1a	The LCL shall correctly operate the application of repetitive overload conditions within the applicable rating/derating limits.	Repetitive overload	LCL case	Nominal	LCL	Equipment	A,T*
5.2.10.2.1a	The RLCL shall correctly operate the application of repetitive overload conditions within the applicable derating limits.		RLCL case	Nominal	RLCL	Equipment	A,T*
5.2.11.1.1a	The LCL design should be capable to withstand the application of reverse current by the load, both in ON and in OFF conditions.	Reverse Current Tolerance	Reverse Current Tolerance	Nominal	LCL	Equipment	RoD
5.2.12.1.1a	It should be possible to put LCLs/HLCLs in parallel.	Parallel connection	LCLs in parallel	Nominal	LCL/HLCL	Equipment	RoD
5.2.12.2.1a	When two or more LCLs/RLCLs/HLCLs are put in parallel, the current sharing accuracy shall be correctly assessed to avoid unwanted tripping-off of the LCLs themselves.		LCLs in parallel and current sharing	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.12.3.1a	When two or more LCLs/RLCLs/HLCLs are put in parallel, the overall trip-off time shall be correctly assessed to avoid unwanted tripping-off of the LCLs/RLCLs/HLCLs themselves.		LCLs in parallel and trip-off	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.2.12.4.1a	When two or more LCLs/HLCLs are put in parallel, the ON/OFF command shall be made common to all of them.		LCLs in parallel and ON/OFF command	Nominal	LCL/HLCL	Equipment	A,T
5.2.12.5.1a	When two or more LCLs/RLCLs/HLCLs are put in parallel, the current telemetry shall provide the overall current flowing through them.		LCLs in parallel and current telemetry	Nominal	LCL / RLCL/HLCL	Equipment	A,T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.13.1.1a	For LCL/HLCL, if no additional switching capability is provided as per 5.2.13.3.1a, the power budget shall cover the LCL/HLCL switch failure by considering the actual MB maximum load, plus eventually the unwanted load connected to the failed LCL/HLCL, in the following cases: 1. all the load operational modes imply a non-negligible power consumption 2. the load operational modes cannot be directly commanded by an autonomous, on board load shedding routine to be triggered by abnormal bus load consumption.	Switching options	No additional switching capability	Fault	LCL/HLCL	SSE/SSS	RoD
5.2.13.2.1a	For LCL/HLCL, the load power consumption considered as negligible in terms of power budget shall be specified by the system integrator.		No additional switching capability, negligible load power consumption mode	Nominal	LCL/HLCL	SSE/SSS	RoD, A
5.2.13.3.1a	For LCL/HLCL, in case that there is an additional switch that can be commanded open in any case when the LCL/HLCL switch is in ON state or fails ON or in short circuit, requirements 5.2.13.4.1a and 5.2.13.5.1a should be fulfilled.		Additional switching capability	Nominal/ Fault	LCL/HLCL	SSE/SSS/Equipment	RoD
5.2.13.3.1b	It shall be possible to command the LCL/HLCL and the relevant additional switch in series by a different, individual command, or a different commanding path.		Additional switching capability	Nominal/ Fault	LCL/HLCL	SSE/SSS/Equipment	RoD
5.2.13.4.1a	For LCL, the additional switch should be put on power system LCL side.		Additional switching capability, location of additional switch	Nominal/ Fault	LCL	Equipment	RoD
5.2.13.5.1a	For LCL, the UVP should act both on the LCL switch and on the additional switch provided by an independent memory cell.		Additional switching capability, UVP acting on additional switch	Nominal/ Fault	LCL	Equipment	RoD
5.2.14.1.1a	In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case no other protection removes the failure, all the surrounding components shall be within derating.	LCL Switch Dissipative failure	Steady state condition	Fault	LCL/RLCL/HLCL	Equipment	A

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.14.2.1a	In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case the "on board system" removes the failure by reducing the load or commanding OFF an additional switch, all the surrounding components shall be within rating during the on board system reaction time.		Transient condition	Fault	LCL/RLCL/HLCL	Equipment	A
5.2.14.3.1a	In case the LCL/RLCL/HLCL switch fails in a dissipative failure and in case requirements 5.2.14.1.1a and 5.2.14.2.1a cannot be fulfilled, a protection shall be embedded in the LCL or in the Distribution Unit to avoid a failure propagation due to the abnormal heat dissipation.		Local protection	Fault	LCL/RLCL/HLCL	Equipment	A,T*
5.2.15.1.1a	In case of a single failure, no more than one LCL/RLCL/HLCL line shall be lost.	Loss of LCL lines	Loss of LCL lines	Fault	LCL/RLCL/HLCL	Equipment	RoD, A
5.2.16.1.1a	The LCL/RLCL/HLCL state shall not change from the commanded one due to spurious perturbations, including: 1. EM emissions, both conducted and radiated, 2. SEE, 3. ESD, 4. ON/OFF commands to other LCL/RLCL lines, and 5. Overcurrent events to other LCL/RLCL lines.	Noise immunity	General	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	see 5.2.16.2.1a and 5.2.16.2.1b
5.2.16.2.1a	Requirement 5.2.16.1.1a shall be verified at unit level and/or at system level: points 1, 3, 4, 5 at unit level and points 1, 4 at system level.		Verification	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	T
5.2.16.2.1b	Requirement 5.2.16.1.1a point 2 shall be verified by analysis.		Verification	Nominal	LCL/RLCL/HLCL	Equipment	A
5.2.17.1.1a	The LCL/RLCL/HLCL output impedance in terms of both gain and phase shall be provided per LCL/RLCL/HLCL class, between 100 Hz and 1 MHz.	Output impedance envelope (when in limitation)	Value	Nominal	LCL/RLCL/HLCL	Equipment	T*
5.2.17.2.1a	The LCL/RLCL/HLCL output impedance shall be provided for a voltage across the LCL/RLCL/HLCL equal to (4 ±1) V.		Verification	Nominal	LCL/RLCL/HLCL	Equipment	T*
5.2.18.1.1a	The RLCL state shall automatically be recovered to ON conditions after a spurious switch-off.	Noise immunity	RLCL spurious switch-off	Nominal	RLCL	Equipment	RoD, A, T*

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.2.18.2.1a	Spurious disable of RLCL retriggering memory cell and of RLCL ON/OFF status memory cell shall not result in the loss of the relevant load.		RLCL spurious effects	Nominal	RLCL	Equipment	RoD, A, T*
5.2.19.1.1a	The LCL/RLCL/HLCL shall work nominally for any load inductance from zero to the maximum specified in 5.5.2.1.1a for LCL/RLCL or in 5.5.2.1.1b for HLCL	Output LCL Load (Input load characteristic)	Load inductance	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.2.19.2.1a	The LCL/RLCL/HLCL shall work nominally for any load capacitance from zero to the maximum specified in Table 3-1, Table 3-2 and Table 3-3 respectively.		Load capacitance	Nominal	LCL/RLCL/HLCL	Equipment	A

Table A-2: Functional/Load requirements list

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.3.1.1.1a	During nominal operation after switch-on, the load current for LCL/RLCL/HLCL shall always be smaller than the correspondent class current.	Nominal	Load behaviour	Nominal	LCL/RLCL/HLCL	SSE/SSS/Equipment	A,T
5.3.1.1.1b	Requirement 5.3.1.1.1a shall be valid also in the following conditions: 1. the bus voltage transients are applied, and 3. there are load-conducted emissions as per the EMC specification.						
5.3.2.1.1a	During Switch-on, the load current shall not exceed the LCL/RLCL class current except for charging the relevant input filter.	Switch-on	Load behaviour 1	Nominal	LCL/RLCL	SSE/SSS/Equipment	A,T
5.3.2.2.1a	Converters contained in the load shall start up without the load current to exceed the LCL/RLCL class current.		Load behaviour 2	Nominal	LCL/RLCL	SSE/SSS/Equipment	A,T
5.3.2.3.1a	If the LCL/RLCL current limit is reached, the load input filter shall be completely charged within the relevant LCL/RLCL maximum charge time defined in requirement 5.4.2.3.1a.		Input filter charging	Nominal	LCL/RLCL	SSE/SSS/Equipment	A,T
5.3.3.1.1a	In case the LCL/RLCL switch fails in a dissipative failure mode, the load shall perform one of the following actions: 1. work nominally, 2. enter autonomously a safe operating condition, or 3. survive the condition without abnormal conducted or radiated emissions.	LCL switch dissipative failure	Steady state condition, load	Fault	LCL/RLCL	Equipment	A,T
5.3.4.1.1a	A representative LCL/RLCL interface should be used during the standalone tests of any load connected to it.	Load test condition	Load test condition	Nominal	LCL/RLCL	Equipment	T
5.3.5.1.1a	In case an UVP at load side is present, the repetitive overload pattern that can result from the interaction with the LCL/RLCL shall be studied as part of the FMECA.	User UVP at bus input side	User UVP at bus input side	Nominal	LCL/RLCL	SSE/SSS/Equipment	A

Table A-3: Performance/Source requirement list

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.4.1.1.1a	The input or output current overshoot when an overload is applied to the LCL/RLCL/HLCL shall be lower than 50 A, when evaluated in the conditions specified in req. 5.4.1.1.1b.	Overall requirements	Current overshoot when an overload is applied to the LCL.	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.1.1.1b	The worst case overload condition applied for the verification shall be a sudden short-circuit applied at the LCL Distribution Unit connector interface.						
5.4.1.1.1c	The time to current overshoot for LCL/RLCL/HLCL shall be 5 µs maximum, when evaluated in the conditions specified in req. 5.4.1.1.1b.		Time to current overshoot	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.1.1.1d	The current overshoot recovery time for LCL/RLCL/HLCL shall be 300 µs maximum, when evaluated in the conditions specified in req. 5.4.1.1.1b.		Current overshoot recovery time	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.1.1.1e	The maximum LCL/RLCL input overshoot charge due to any overload shall be limited to 1 mC maximum.		Input overshoot charge	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.1.1.1f	The maximum input overshoot charge due to an overload, as per 5.4.1.1.1e., shall be complied for any load inductance value from zero to the maximum specified in 5.5.2.1.1a for LCL/RLCL, or in 5.5.2.1.1b for HLCL.		Input overshoot charge and load inductance	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.1.2.1a	In case the reverse current functional requirement 5.2.11.1.1a is applied, the reverse current peak tolerance shall be equal to the LCL class current, with linear decay of 10 minutes maximum.		Reverse Current Tolerance	Nominal	LCL	Equipment	A
5.4.1.3.1a	Maximum leakage current for LCL/RLCL/HLCL shall be 100 µA.		Leakage current	Nominal	LCL/RLCL/HLCL	Equipment	A
5.4.1.3.1b	The voltage appearing at the LCL/RLCL/HLCL output in OFF state shall be lower than 1V.		Leakage voltage	Nominal	LCL/RLCL/HLCL	Equipment	T
5.4.1.4.1a	The minimum time between two successive external LCL/HLCL ON commands shall be 1 s.		Minimum time between two successive ON commands	Nominal	LCL/HLCL	SSE/SSS	A,T
5.4.2.1.1a	Maximum LCL/RLCL/HLCL start-up current rate dI/dt shall be 1A/µs.	Start-up / switch-off	LCL start-up current rate	Nominal	LCL/RLCL/HLCL	Equipment	A,T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.4.2.2.1a	Maximum LCL/RLCL/HLCL switch-off current rate dI/dt shall be 1A/µ	requirements	LCL switch-off current rate	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.2.3.1a	The load input filter charge time shall be maximum 80 % of LCL/RLCL class minimum trip-off time when: 1. operating in worst-case conditions; 2. the minimum LCL/RLCL class limitation current is chosen.		Load Input Filter Charge time	Nominal	LCL/RLCL	SSE/SSS/Equipment	A,T
5.4.2.4.1a	The amplitude of the pulse appearing at LCL/HLCL output during main bus start-up shall not exceed 5 V.		Output, auto start OFF, amplitude	Nominal	LCL/HLCL	Equipment	A, T*
5.4.2.4.1b	Requirement 5.4.2.4.1a shall be valid for any applicable main bus voltage derivative at start-up and when minimum load is applied.						
5.4.2.5.1a	The duration of the pulse appearing at LCL/HLCL output during main bus start-up shall not exceed 1 ms.		Output, auto start OFF, duration	Nominal	LCL/HLCL	Equipment	A, T*
5.4.2.5.1b	Requirement 5.4.2.5.1a shall be valid for any applicable main bus voltage derivative at start-up and when minimum load is applied.						
5.4.3.1.1a	The LCL/RLCL/HLCL switch-off threshold shall be configurable on ground from 80 % of the nominal bus voltage value.	UVP	Switch-off threshold, regulated bus	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.3.2.1a	The LCL/RLCL/HLCL switch-off threshold shall be configurable on ground from 50 % of the nominal DC maximum bus voltage value.		Switch-off threshold, unregulated bus	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.3.3.1a	For LCL/RLCL/HLCL, the UVP shall not react for an undervoltage event lasting less than 500 µs.		UVP noise immunity	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.3.4.1a	For LCL/RLCL/HLCL, the UVP noise immunity shall be verified by applying a voltage step from nominal bus voltage to 80 % of nominal DC switch-off threshold with a fall time equal or smaller than 1 % of the actual UVP reaction time.		UVP noise immunity, verification	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.3.5.1a	If UVP hysteresis is implemented, the difference between the actual UVP switch-off threshold, and relevant enabled ON threshold, shall be higher than 0,5 V.		UVP hysteresis	Nominal	LCL/RLCL/HLCL	Equipment	A,T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.4.4.1.1a	The LCL/RLCL/HLCL enable ON threshold shall be configurable up to 95 % of the nominal main bus voltage.	Switch-on capability	LCL enable ON threshold Voltage, regulated bus case	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.4.2.1a	The LCL/RLCL/HLCL enable ON threshold shall be configurable up to 90 % of the nominal DC maximum bus voltage value.		LCL enable ON threshold Voltage, unregulated bus case	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.4.3.1a	The RLCL shall not switch ON when relevant threshold is reached for less than 500 µs.		Switch-on response time, value	Nominal	RLCL	Equipment	A,T
5.4.4.4.1a	The RLCL Switch-on response time shall be verified by the application of a voltage step from 80 % of nominal DC switch-off threshold to nominal bus voltage with a rise time equal or smaller than 1 % of the actual Switch-on response time.		Switch-on response time, verification	Nominal	RLCL	Equipment	T
5.4.5.1.1a	The voltage drop of LCL/RLCL line shall not exceed 1 % of the nominal main bus voltage at the relevant class current.	Voltage drop	Voltage drop	Nominal	LCL/RLCL	Equipment	A,T
5.4.5.1.1b	The voltage drop of an HLCL/LCL with an additional switch shall not exceed 2 % of the nominal main bus voltage at the relevant class current.	Voltage drop	Voltage drop	Nominal	LCL//HLCL	Equipment	A,T
5.4.5.1.1c	The LCL/RLCL/HLCL voltage drop shall be measured from central regulation point to the output connector.	Voltage drop	Voltage drop	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.6.1.1a	Minimum phase margin for LCL/RLCL/HLCL shall be 50°, under the following conditions: 1. a zero Ohm impedance load is applied, and 2. the DC voltage across the LCL/RLCL/HLCL equals (4 ±1) V.	Stability	Frequency domain, phase margin	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.6.2.1a	Minimum gain margin for LCL/RLCL/HLCL shall be 10 dB under the following conditions: 1. a zero Ohm impedance load is applied, and 2. the DC voltage across the LCL/RLCL/HLCL equals (4 ±1) V.		Frequency domain, gain margin	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.6.3.1a	For any specified inductive load, no persistent voltage or current oscillation shall occur when the LCL/RLCL/HLCL is applied a sudden overload.		Time domain, transient from non-limiting mode to current limitation mode.	Nominal	LCL/RLCL/HLCL	Equipment	A,T*

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.4.6.3.1b	The period of observed oscillation as per requirement 5.4.6.3.1a shall be greater or equal to the envelope decay time.						
5.4.6.4.1a	For any specified inductive or capacitive load, no persistent voltage or current oscillation shall occur when the LCL/RLCL/HLCL is starting up in current limitation.		Time domain, start-up transient to current limitation mode	Nominal	LCL/RLCL/HLCL	Equipment	A,T*
5.4.6.4.1b	The period of observed oscillation as per requirement 5.4.6.4.1a shall be greater or equal to the envelope decay time.						
5.4.7.1.1a	For LCL/RLCL/HLCL, the accuracy of the current telemetry shall be equal or better than ±4 % of the full scale value in worst case.	Current telemetry, accuracy	Current telemetry, accuracy	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.8.1.1a	If functional requirement 5.2.8.6.1a is not met, for LCL/RLCL/HLCL the offset of the current telemetry shall be equal or better than ±4 % of the full scale value in worst case.	Current telemetry, offset	Current telemetry, offset	Nominal	LCL/RLCL/HLCL	Equipment	A,T
5.4.9.1.1a	For RLCL, the minimum retrigger interval shall be 20 s unless a specific RLCL memory cell for latched trip-off status is provided.	Retrigger interval	Retrigger interval	Nominal	RLCL	Equipment	A,T
5.4.10.1.1a	For RLCL, the maximum value of dI/dt rate on retrigger ON edge shall be 1 A/µs.	dI/dt limit on retrigger ON edge	dI/dt limit on retrigger ON edge	Nominal	RLCL	Equipment	A,T
5.4.11.1.1a	For RLCL, the maximum value of dI/dt rate on retrigger OFF edge shall be 1 A/µs.	dI/dt limit on retrigger OFF edge	dI/dt limit on retrigger OFF edge	Nominal	RLCL	Equipment	A,T
5.4.12.1a	The LCL/RLCL/HLCL ON/OFF status shall confirm that the LCL/RLCL/HLCL output voltage is within its nominal range with an accuracy of ±10 %.	Status, accuracy	Status, accuracy	Nominal	LCL/RLCL/HLCL	Equipment	A, T*

Table A-4: Performance/Load requirements list

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
5.5.1.1.1a	For LCL/RLCL, a load should not reinject current into the bus.	Load reverse current	Avoidance	Nominal	LCL/RLCL	Equipment	RoD
5.5.1.2.1a	In case requirement 5.2.11.1.1a is complied, the maximum current reinjected to the LCL shall be equal to the LCL class current, with linear decay of 10 minutes maximum.		Reinjection current	Nominal	LCL	Equipment	A,T
5.5.2.1.1a	The maximum inductance, including the harness between LCL/RLCL and load, and including the input load filter, shall be 300 μH.	Load characteristic	Maximum inductance	Nominal	LCL/RLCL	SSE/SSS/Equipment	RoD, A
5.5.2.1.1b	The maximum inductance, including the harness between HLCL and load, and including the input load filter, shall be 50 μH.		Maximum inductance	Nominal	HLCL	SSE/SSS/Equipment	RoD, A
5.5.2.2.1a	The maximum capacitance for LCL and RLCL shall be compatible with the one shown in Table 3-1 and Table 3-2 respectively.		Maximum capacitance	Nominal	LCL/RLCL	Equipment	A,T
5.5.2.2.1b	The maximum capacitance for HLCL shall be compatible with the one shown in Table 3-3.		Maximum capacitance	Nominal	HLCL	Equipment	A,T
5.5.2.3.1a	For LCL/RLCL, the supplier shall provide to the customer the load impedance envelope, expressed in terms of magnitude and phase, for a frequency range from 100 Hz to 1 MHz.		Load impedance envelope	Nominal	LCL/RLCL	Equipment	A,T*
5.5.3.1.1a	For LCL/RLCL, at those frequencies in which the load and the source impedance are equal in magnitude, the difference between the load impedance phase and the source impedance phase shall be greater than abs(±150°±n*360°).	Source-load characteristic	Source-load impedances phase margin	Nominal	LCL/RLCL	SSE/SSS	A
5.5.3.2.1a	For LCL/RLCL, at those frequencies in which the difference between the load impedance phase and the source impedance phase is equal to -180°±n*360°, the difference between the load impedance gain and the LCL impedance gain shall be greater than 5 dB.		Source-load impedances gain margin	Nominal	LCL/RLCL	SSE/SSS	A
5.5.4.1.1a	In case of an LCL/RLCL failure causing a sudden application of nominal voltage to the load, the relevant	Start-up Surge Input Current	Start-up surge input Current	Fault	LCL/RLCL	Equipment	A,T

Reference	Text of the requirement	Feature	Sub-feature	Conditions	Applicability	Applicability level	Verification
	peak current shall be lower than 20 A or 5 times the class current, whichever is greater.						
5.5.4.1.1b	The peak current shall be compatible with the electrical and thermal stress of: 1. the LCL/RLCL, 2. the load input filter components, and 3. the relevant main bus disturbance						
5.5.5.1.1a	If an internal current limitation is used in the load, the relevant overall current limit shall be at maximum equal to the class current of the relevant LCL/RLCL.	Internal load Input current limitation	Internal load input current limitation	Nominal	LCL/RLCL	Equipment	A,T

Bibliography

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ECSS-E-ST-10-02	Space engineering - Verification
ECSS-E-HB-20-20	Space engineering – Guidelines for electrical design and interface requirements for power supply