ECSS-E-ST-50-14C
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Space engineering

Spacecraft discrete interfaces

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-E-ST-50-14C Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

Disclaimer

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Scope

This standard specifies a common set of spacecraft onboard electrical interfaces for sensor acquisition and actuator control. The interfaces specified in this standard are the traditional point-to-point interfaces that are commonly used on modern spacecraft.

The interfaces specified in this standard include analogue and discrete digital interfaces used for status measurement and control, as well as point-to-point serial digital interfaces used for digital data acquisition and commanding of devices.

This standard specifies:

- interface signal identification;
- interface signal waveforms;
- signal timing requirements;
- signal modulation;
- voltage levels;
- input and output impedance;
- overvoltage protection requirements;
- bit ordering in digital data words;
- cabling requirements where appropriate.

This standard does not cover:

- connector requirements;
- digital data word semantics;
- message or block formats and semantics.

Connector requirements are not covered because these are normally mission or project specific. The goal of this standard is to establish a single set of definitions for these interfaces and to promote generic implementations that can be re-used throughout different missions.

When referred, the present standard is applicable as a complement of the already existing interface standards ANSI/TIA/EIA-422B-1994 and ITU-T Recommendation V.11 (Previously "CCITT Recommendation") – (03/93).

Guidance for tailoring of the present standard can be found in Annex A.

This Standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications, do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system - Glossary of terms
ANSI/TIA/EIA-422B-1994	Electrical characteristics of balanced voltage digital interface circuits
ITU-T Recommendation V.11 (Previously "CCITT Recommendation") – (03/93)	Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s

NOTE This document is technically equivalent to ANSI/TIA/EIA/422B-1994.

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 accuracy

closeness of a measurement to the actual quantity being measured

NOTE For the purposes of this Standard it is expressed as percentage of the full measurement range or as an absolute value.

3.2.2 circuit

conducting path which conveys a signal across the interface from the signal source to the signal destination

NOTE A circuit includes the cable conductor, any intervening connectors, and any circuit elements such as protection resistors and coupling capacitors, which make up the signal path.

3.2.3 DHS data interchange bus

underlying communication medium which connects the DHS core elements

NOTE This can consist of more than one physical bus.

3.2.4 DHS core element

component of a data handling system which has a direct connection to the DHS data interchange bus

NOTE E.g.: bus controllers and remote terminals.

3.2.5 DHS peripheral element

component of a data handling system which does not have a direct connection to the DHS data interchange bus

NOTE E.g.: sensors and actuators.

3.2.6 ground displacement voltage

voltage difference between source and receiver ground references

NOTE Users are encouraged to use this definition instead of 'common mode voltage' that is not correct when referring to the academic definition.

3.2.7 time reference point

point at which a time interval starts or ends

NOTE It is the mid point between the nominal high and nominal low signal voltages.

3.3 Abbreviated terms

For the purpose of this standard, the abbreviated terms of ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
A/D	analogue to digital
ADC	analogue digital converter
ASM	analogue signal monitor
BDM	bi-level discrete monitor
BSD	bi-directional serial digital
BSM	bi-level switch monitor
CM	common mode
DHS	data handling system
HPC	high power command
HC-HPC	high current high power command
HV-HPC	high voltage high power command
ISD	input serial digital
LPC	low power command
LPC-P	low power command, pulsed
LPC-S	low power command, static
LSB	least significant bit
LV-HPC	low voltage high power command
MSB	most significant bit
OBDH	on-board data handling
OSD	output serial digital
TSM	temperature sensors monitor

3.4 Conventions

3.4.1 Bit numbering convention

The most significant bit of an n-bit field is:

- numbered bit 0 (zero),
- the first bit transmitted, and
- the leftmost bit on a format diagram.

The least significant bit of an n-bit field is:

- numbered bit n-1,
- the last bit transmitted, and
- the rightmost bit on a format diagram.

This convention is illustrated in Figure 3-1.

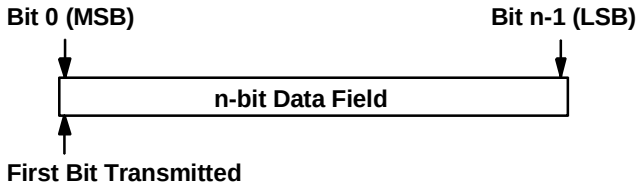

Figure 3-1: Bit numbering convention

3.4.2 Timing diagram conventions

Timing diagrams are always drawn with the earliest time on the left and time advancing to the right.

Where an event, such as a transition, in one signal causes an event in another, the two events are linked by an arrow with the tail of the arrow on the causal event and the head of the arrow on the resultant event.

Where an event in one signal is the result of an event in another signal and a qualifying condition in one or more other signals, the connecting arrow is associated with the governing condition using a bull's eye.

These conventions, together with other timing diagram symbols, are shown in Figure 3-2.

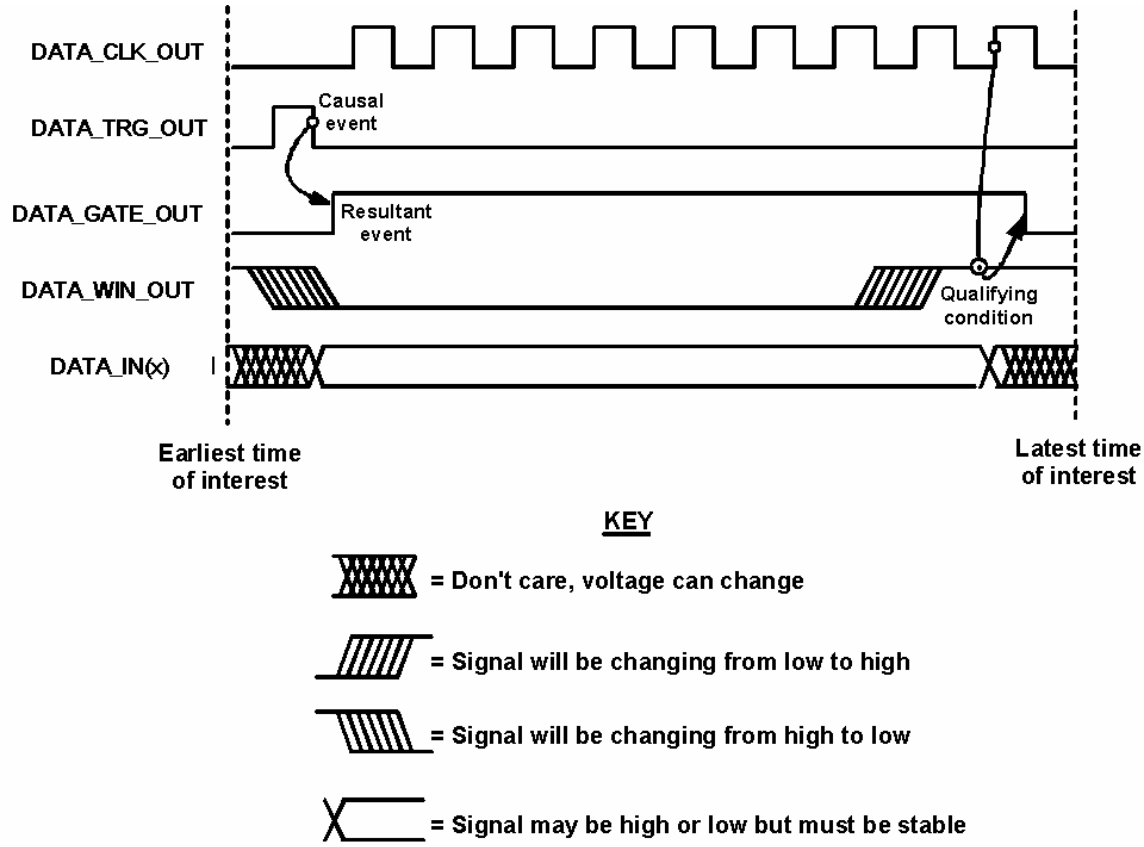

Figure 3-2: Timing diagram conventions

3.4.3 Signal and signal event naming convention

Signals are named in a manner which indicates the function of that signal. For example, a clock used for data bit sampling can be called DATA_CLK.

Control signal naming is meaningful with the function of the signal, its direction, and its assertion levels all indicated. The direction is indicated with respect to the DHS core element so that an OUT signal is an output, i.e. driven from the core element. An IN signal is an input to the core element. For example, a signal carrying data out of the core element is named DATA_OUT.

Control signal assertion or validity levels are indicated within brackets. For example, a gate output signal which is asserted when low is named GATE_OUT(L). Similarly, an input signal which indicates that a device is ready when it is high is named READY_IN(H).

Signal events such as transitions and pulses are also named symbolically using "*UP*" and "*DOWN*" indication. For example, START*UP* indicates a rising edge event on the start signal, and STOP*DOWN* indicates a falling edge on the stop signal. RUN*UPDOWN* indicates a positive going pulse on the run signal, while HALT*DOWNUP* indicates a negative going pulse on the halt signal.

3.4.4 Signal timing and measurement references

Signal rise and fall times, which are shown in Figure 3-3, are measured between 10 % and 90 % of the difference between the nominal low and nominal high signal voltages, as it can be seen in the mentioned figure.

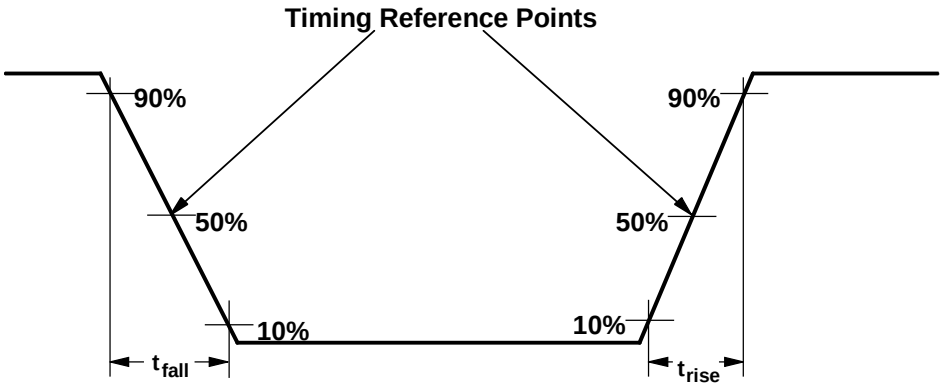

Figure 3-3: Signal timing and measurement references

4
General

4.1 Introduction

This standard defines electrical interfaces for use onboard spacecraft to connect simple devices such as sensors and actuators to the data handling system. The interfaces defined are:

- analogue signal interfaces (clause 5)
  - analogue signal monitor
  - temperature sensor monitor
- bi-level discrete input interfaces (clause 6)
  - bi-level discrete monitor
  - bi-level switch status monitor
- command interfaces (clause 7)
  - high power pulse command
  - low power command
- serial digital interfaces (clause 8).

Each interface is defined in terms of the electrical and timing characteristics of the signals comprising that interface. Connectors for the interfaces are not defined because these are often highly project dependent. Cabling characteristics are defined where appropriate.

For the serial digital interfaces, the data content of the digital words is not defined since this is the subject of higher level protocol standards beyond the scope of this Standard.

Unless otherwise stated, specified performances are applicable when both source and receiver are powered.

4.2 Architectural concepts

4.2.1 Overview

The interfaces specified in this Standard are intended to connect DHS core elements to DHS peripheral elements as shown in Figure 4-1. However, there are no technical reasons to prevent these interfaces being used between core

elements where it is appropriate to do so, and this Standard does not preclude such a configuration.

A peripheral element can have more than one user interface and also user interfaces of different types, depending on its function and design. For example, some sensors can set threshold levels or sensitivities by means of data written to them. In this case that sensor can use an output serial digital interface to write the data in addition to an input serial digital interface to read the sensor value. Alternatively, some devices are signalled to indicate that they are commanded to acquire a data sample. In that case they can use a serial digital interface together with a pulse interface.

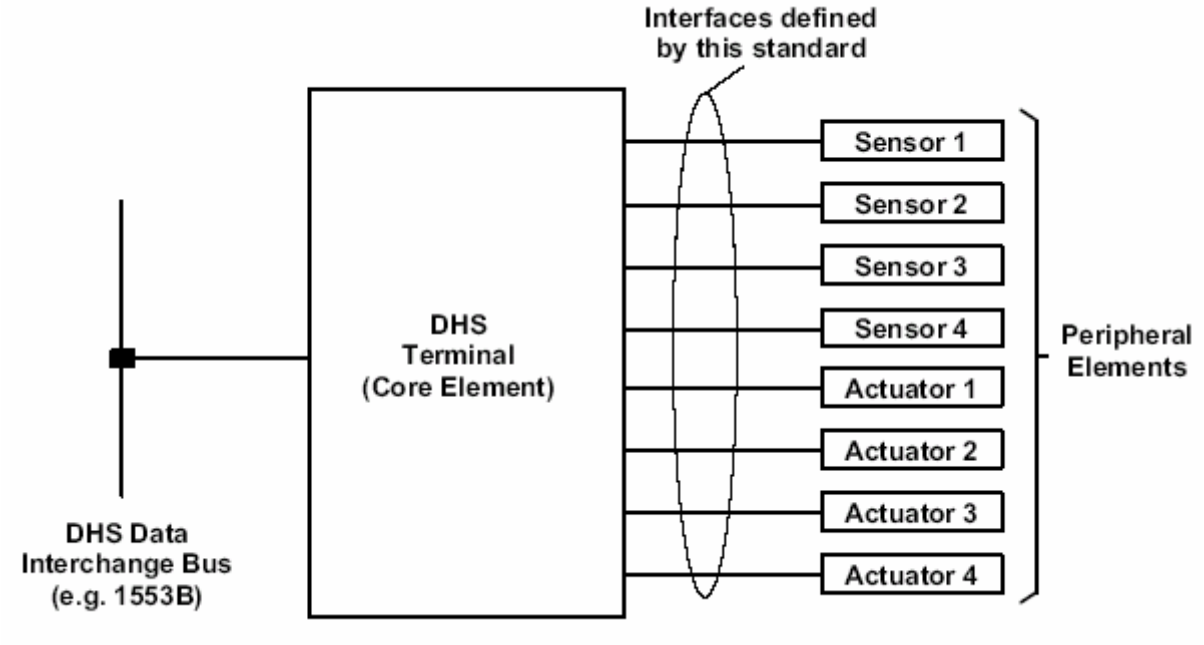

Figure 4-1: Architectural context of interfaces defined in this standard

4.2.2 General failure tolerance

4.2.2.1 Input interfaces

a. Among other failure cases, receivers shall:

1. Not be stressed and not show degraded performance when input is open circuit except on the input I/F that is open circuit.

2. Not be stressed and not show degraded performance when input is short circuit to ground except on the input I/F that is short circuit.

NOTE No specific performance requirements are imposed while in this status.

4.2.2.2 Output interfaces

a. Among other failure cases, transmitters shall:

1. Not be stressed and not show degraded performance when output is open circuit except on the output I/F that is open circuit.

2. Not be stressed when output is short circuit to ground.

NOTE No specific performances requirement is imposed while in this status.

4.2.3 Interface control during power cycling

4.2.3.1 Input interfaces

a. Input interfaces shall not be damaged or harmed during power cycling conditions taking the transmitting side state into account in any normal state or applicable failure condition.

b. Receivers shall not deliver power to the other circuits or be stressed when the unit is OFF while connected to an active driver.

NOTE No specific performance requirements are imposed while in this status.

4.2.3.2 Output interfaces

a. Output interfaces shall not be damaged or harmed during power cycling conditions when the receiving side state is in any normal state or specified failure condition.

NOTE No specific performance requirements are imposed while in this status.

b. For pulse commands it shall be ensured that spurious commands are not emitted during power cycling that exceed activation limits for the receivers.

NOTE 1 For pulse commands, see Clause 7.

NOTE 2 This requirement does not specify the prevention of spurious pulses, but ensures either that:

- spurious pulses are below the threshold for the receiver, or
- the spurious pulse duration is short enough to not drive the load into activation (for example a relay coil or opto-coupler diode).

4.2.4 Cross-strapping

4.2.4.1 General

a. For 2 units (UNIT_1 & UNIT_2), that can be used in redundancy, the cross-strapping of drivers and receivers shall be as specified in Figure 4-2, and meet the following conditions:

1. The UNIT_2_A I/F is capable to receive:
   (a) A signal from the UNIT_1_A I/F through a dedicated link
   (b) A signal from the UNIT_1_B I/F through a dedicated link
2. The UNIT_2_B I/F shall is capable to receive:
   (a) A signal from the UNIT_1_A I/F through a dedicated link
   (b) A signal from the UNIT_1_B I/F through a dedicated link
3. The UNIT_1_A I/F is capable to deliver:
   (a) A signal to the UNIT_2_A I/F through a dedicated link
   (b) A signal to the UNIT_2_B I/F through a dedicated link
4. The UNIT_1_B I/F is capable to deliver:
   (a) A signal to the UNIT_2_A I/F through a dedicated link.
   (b) A signal to the UNIT_2_B I/F through a dedicated link.

b. To achieve full cross-strapping benefits, in terms of reliability, any potential common failure of UNIT_1_A and UNIT_1_B drivers and UNIT_2_A and UNIT_2_B receivers shall be avoided.

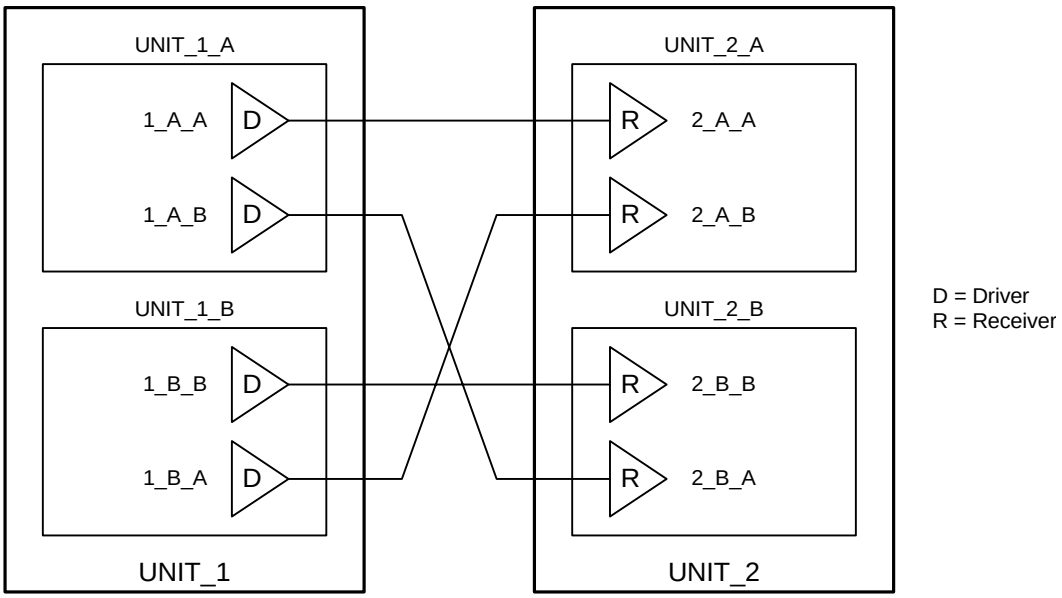

Figure 4-2: General scheme of redundant unit's cross-strapping

4.2.4.2 Immunity at UNIT_2 level

a. Under the condition (Receiver = ON linked to Transmitter = OFF of UNIT_1), in the configuration where UNIT_1 driver is OFF and UNIT_2 receiver is ON, the information received by this receiver shall not disturb the valid information received by the other receiver (linked to a Transmitter ON).

NOTE In this configuration the electrical status at receiver output is stable (due to hysteresis) but possibly unknown (logical "1" or "0").

b. It should be ensured that any input signal is in a known (inactive) stable state when driver is OFF.

c. If 4.2.4.2b is not met, a validation / inhibition stage at the receiver output of UNIT_2 should be implemented.

NOTE For example, the validation of the path can be made by a dedicated direct command arriving from UNIT_1, which inhibits the UNIT_2 receiver output unused (if such a configuration has been thoroughly designed with respect to failure cases).

4.2.4.3 Protections at UNIT_1 driver level

a. Under the condition (Transmitter = OFF linked to Receiver = ON of UNIT_2), whether powered or not, UNIT_1 drivers shall withstand any receiver characteristics as described in Clauses 5 to 8.

4.2.4.4 Protections at UNIT_2 receiver level

a. Under the condition (Receiver = OFF linked to Transmitter = ON of UNIT_1), whether powered or not, UNIT_2 receivers shall withstand any driver characteristics as described in Clauses 5 to 8.

4.2.5 Harness cross-strapping

4.2.5.1 Overview

Harness cross-strapping is applied when heritage units, without classical cross-strapping interfaces, are used, in the case that a single redundant unit is interfaced to both a nominal and redundant system. If the spacecraft is severely mass-limited, harness cross-strapping can be used instead.

Harness cross-strapping can be used in two configurations:

- Single source – Dual receiver configuration, as shown in Figure 4-3.
- Dual source – Single receiver configuration, as shown in Figure 4-4.

The Single source – Dual receiver configuration is typically applied for BSM interfaces as described in clause 6.2.

The Dual source – Single Receiver configuration is typically applied for HPC interfaces as described in clause 7.1.

Note that this harness cross-strapping can be performed by galvanic connections in harness, as indicated in Figure 4-3 and Figure 4-4. However, the equivalent configuration applies in case the physical inter-connection is performed either within the source or within the receiver unit. The general rules and protections as mentioned in this clause 4.2.5 apply then also for those cases.

Possible problems that can be introduced by harness cross-strapping include failure propagation, loading and leakage injection of the active I/F by the redundant, inactive circuit such that the active circuit does not meet its performance requirements, incompatibility of protection circuitry of a given circuit with either the Receiver I/F circuit or the Driver (see Figure 4-4) I/F circuit. Note that in general it is important to consider loading by the redundant, inactive circuit also when powered off, even if the inactive circuit is normally powered (hot redundancy).

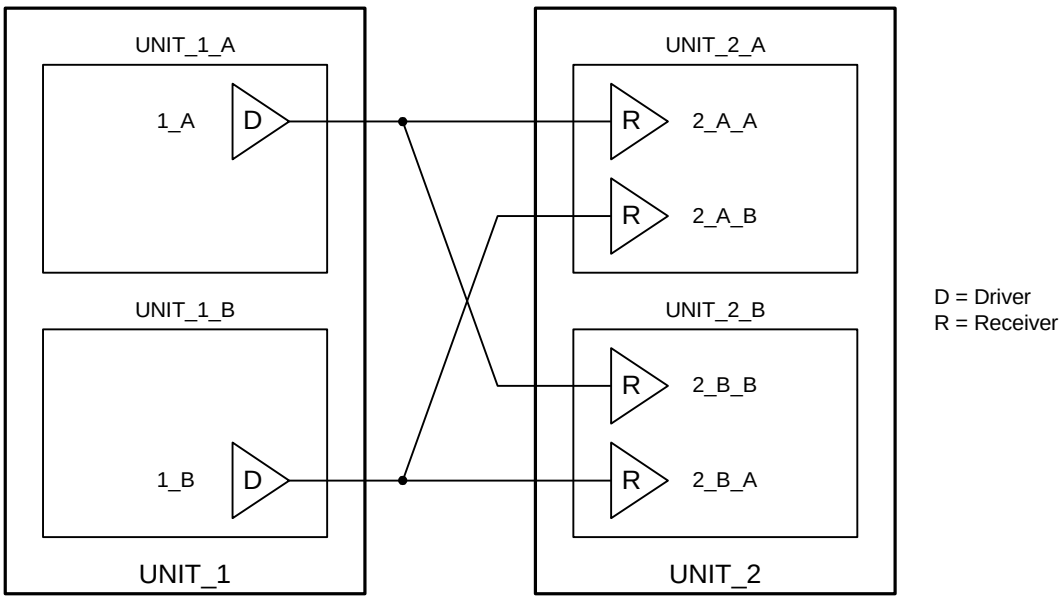

Figure 4-3: Example scheme for Single source – Dual receiver cross-strapping

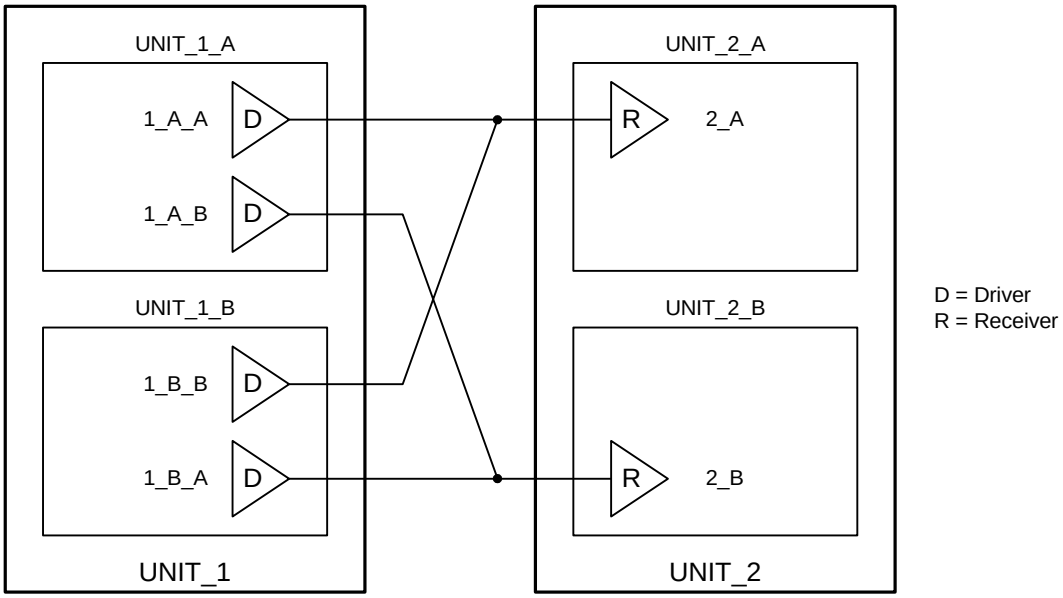

Figure 4-4: Example scheme for Dual source – Single receiver cross-strapping

4.2.5.2 Provisions

a. If harness cross-strapping is used, there shall be no mechanism whereby the failure of either the receiver or unit interface can propagate to the I/F of another, unrelated unit.

NOTE This requirement refers to a common mode failure where a failure of one interface then propagates inside the receiver thereby affecting units unrelated to the original failure.

b. If harness cross-strapping is used, the calculation of the overall system reliability shall include the potential degradation or damage of the I/F of a redundant unit due to the failure of other interface.

NOTE This requirement refers to the failure on a nominal unit causing the inoperability of the cross-strap. This means that there is a reduction in the possible reliability of the cross-strap.

c. If harness cross-strapping is used, the capability shall be provided to shut down the inoperable unit regardless of the failure mode

NOTE This implies that the power can be removed from the unit by independent means such as disabling the power interface at the power distribution unit (e.g. with the means described in clause 4.2.4.2)

d. Under the condition (Transmitter = OFF linked to Receiver = ON of UNIT_2), whether powered or not, UNIT_1 drivers shall withstand any receiver characteristics as described in Clauses 5 to 8.

e. Under the condition (Receiver = OFF linked to Transmitter = ON of UNIT_1), whether powered or not, UNIT_2 receivers shall withstand any driver characteristics as described in Clauses 5 to 8.

4.2.6 Cable capacitance

It is important that the DHS interfaces consider the capacitive loading by the harness. Figure 4-5 defines the capacitances involved for a twisted shielded pair cable.

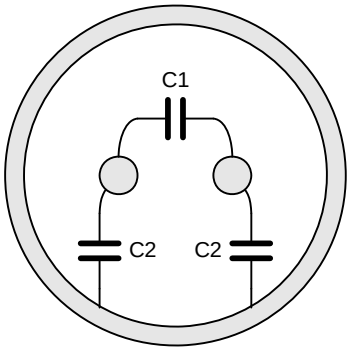

Figure 4-5: Cable capacitance definitions

Effective capacitances can then be calculated according to:

- Core to core capacitance $C_{CC} = C1 + \frac{C2}{2}$
- Core to shield capacitance $C_{CS} = C2 + \frac{C1 \cdot C2}{C1 + C2}$
- Core to core capacitance with shield connected to one core $C_{CT} = C1 + C2$

Note that the latter case applies typically when either the source or the receiver is single ended, which implies that both the shield and one of the core wires are grounded.

5
Analogue signal interfaces

5.1 Overview

The analogue signal interfaces are used for direct connection to a device which produces a continuous variable analogue voltage to indicate the value of the parameter being measured.

Usually, the analogue voltage produced by the sensor or a peripheral element is converted into a digital value within the core element to which it is connected. This Standard specifies the electrical characteristics of the analogue signal interfaces.

Two types of analogue interfaces are specified:

- Analogue signal monitor interface, ASM (see 5.2)
- Temperature sensors monitor interface, TSM (see 5.3)

5.2 Analogue signal monitor (ASM) interface

5.2.1 General

5.2.1.1 Overview

The analogue signal monitor interface is based on differential receiver circuit where both the high and low analogue signal lines are floating with respect to the receiver signal ground; the source interface can be either single ended or differential.

The analogue voltage provided is sampled intermittently by the core element. The precise frequency and the duration of the sampling interval depend on the A/D conversion service being used. However, the input impedance and capacitance exhibited by an analogue signal interface can differ when the input signal is actually being sampled compared with when it is not. As a consequence, different input impedance and capacitance requirements are provided for the different configurations.

In addition, the impedance seen when the receiver element is powered off is specified.

5.2.1.2 Basic application scenario

The interface specified in this clause 5.2.1.2 is defined on the basis of a typical analogue signal monitoring application scenario, i.e.

- differential voltage range: 0 to 5 V or optionally 0 to 5,12 V;
- signal bandwidth: ≤ 1 Hz;

  NOTE This means that accuracy requirements are specified here assuming only slowly changing (quasi-static) signals. That does not prohibit, for instance, rapid transitions in signals, but accuracy is unspecified during such events.

- ground displacement voltage: ≤ ±1 V in the frequency range 0 to 1 kHz, falling at 20 dB per decade up to 1 MHz;
- conversion resolution: 12 bits.

  NOTE 1 The specified 12 bits resolution is not incompatible with use of ADC having 14 or even 16 bits resolution. In that case, LSB are "not significant".

  NOTE 2 Even if the overall channel accuracy requirement in 5.2.1.4 can be met also with an 8 bit ADC, it is important to note that in this case the ADC quantization error contributes ±0,2 % to the overall channel accuracy, thus normally a good practice is to use a 12 bit ADC.

5.2.1.3 Applications other than the basic scenario

a. If the actual scenario differs from the one defined in 5.2.1.2, the interface shall not be directly used.

   NOTE 1 For example, if the specific application uses higher conversion accuracy or has different operational conditions, e.g. higher displacement.

   NOTE 2 In particular, ground displacement heavily affects the achievable conversion accuracy. Different scenario or specified performances can, for instance, ask for source impedance balancing.

b. The modified interface shall be supported by an analysis of the overall system, including both interface source and receiver as well as interconnecting wiring.

5.2.1.4 Acquisition of the analogue channels by the core element

a. The errors introduced by the DHS receiver analogue acquisition chain, including temperature, ground displacement voltage rejection, A/D conversion inaccuracy, herein specified source impedance and cable capacitance, supply voltage variations, lifetime and radiation effects shall be less than 1 % of the full scale.

5.2.2 Analogue signal monitor interface

5.2.2.1 Source circuit

a. The source circuit shall meet the characteristics specified in Table 5-1.

Table 5-1: Analogue signal monitor source circuit characteristics

Reference	Characteristic	Value
5.2.2.1 a.1	Circuit type	Single ended or differential
5.2.2.1 a.2	Transfer	DC coupled
5.2.2.1 a.3	Zero reference	Signal ground – in case of differential source (ref Figure 5-2), the return signal's potential shall be equal to unit's chassis ground.
5.2.2.1 a.4(a)	Nominal output voltage range, V_{out}	0 V to +5 V [a]
5.2.2.1 a.4(b)		0 V to +5,12 V
5.2.2.1 a.5	Output impedance, Z_{out}	≤ 5 kΩ
5.2.2.1 a.6	Fault voltage tolerance, V_{sft}	-17,5 V to +17,5 V with an overvoltage source impedance > 1,0 kΩ
5.2.2.1 a.7	Fault voltage emission, V_{sfe}	-16,5 V to +16,5 V

[a] The range 0 V – 5 V is the preferred one. 5,12 V can be used if straightforward A/D conversion is necessary.

5.2.2.2 Receiver circuit

a. The receiver circuit shall meet the characteristics specified in Table 5-1.

Table 5-2 Analogue signal receiver circuit characteristics

Reference	Characteristic	Value
5.2.2.2 a.1	Circuit type	Differential
5.2.2.2 a.2	Transfer	DC coupled
5.2.2.2 a.3(a)	Nominal input voltage range, V_{in}	differential: 0 V to +5 V [a]
5.2.2.2 a.3(b)		differential: 0 V to +5,12 V
5.2.2.2 a.4	Ground displacement voltage, V_{GD}	-1 V to 1 V up to 1 kHz rolling-off at 20 dB/decade up to 1 MHz
5.2.2.2 a.5	Differential input impedance (sampling), Z_{is}	≥ 1 MΩ
5.2.2.2 a.6	Differential input impedance (not sampling), Z_{ins}	≥ 10 MΩ
5.2.2.2 a.7	Differential input impedance (powered off), Z_{ioff}	≥ 10 kΩ
5.2.2.2 a.8	Differential input capacitance (sampling), C_{is}	≤ 1,5 µF
5.2.2.2 a.9	Differential input capacitance (not sampling), C_{ins}	≤ 1,5 µF
5.2.2.2 a.10	Differential input capacitance (powered off), C_{ioff}	≤ 1,5 µF
5.2.2.2 a.11	Fault voltage emission, V_{rfe}	-16,5 V to +16,5 V with a series impedance ≥ 1,0 kΩ
5.2.2.2 a.12	Fault voltage tolerance, V_{rft}	-17,5V to +17,5 V

[a] The range 0 V – 5 V is the preferred one. 5,12 V can be used if straightforward A/D conversion is necessary

NOTE When prime and (cold) redundant configurations are used and implemented by cross-strapping as defined in clause 4.2.5, care should be taken to ensure that the impendence of the off device does not unduly influence that of the powered device.

5.2.2.3 Harness

5.2.2.3.1 Wire type

a. The wire type should be twisted shielded lines.

b. If 5.2.2.3.1a is not met, n-tuples shall be used.

c. The shield shall be connected to the structure ground both on source and receiver sides.

5.2.2.3.2 Core to shield capacitance

a. The capacitance C_{CT} shall be less than 2 nF.

5.2.2.4 Interface arrangement

The electrical interface arrangement is depicted in Figure 5-1 and Figure 5-2, which show specific implementation to be taken as examples, but other implementations compliant to requirements are not excluded.

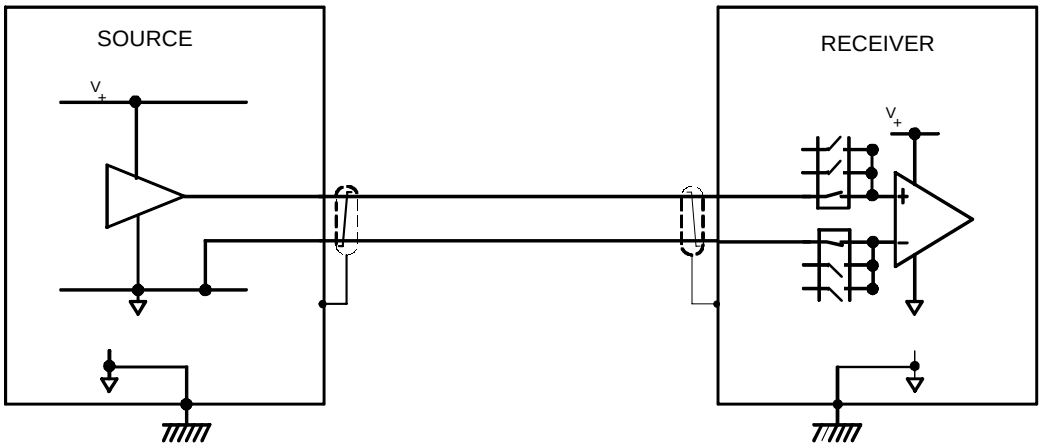

Figure 5-1: Analogue signal monitor (single ended source) interface arrangement

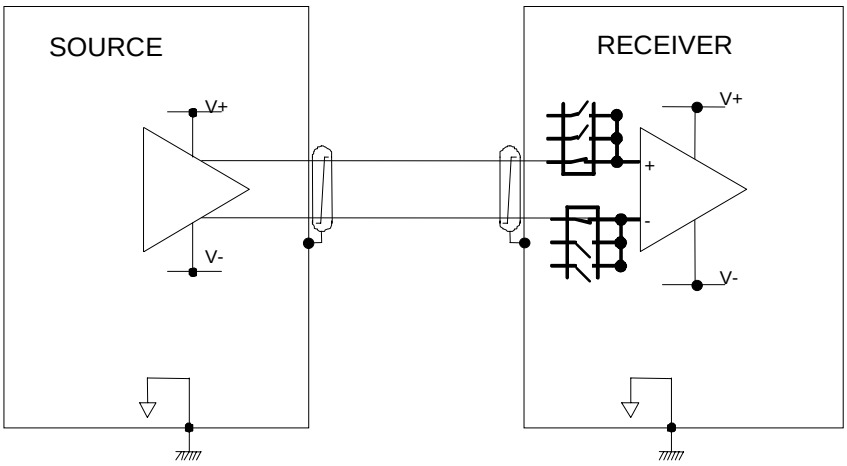

Figure 5-2: Analogue signal monitor (differential source) interface arrangement

5.3 Temperature sensors monitor (TSM) interface

5.3.1 Overview

Temperature monitor channels are resistance measurement channels used for resistive temperature sensor acquisition.

The word "thermistor" is derived from the description "thermally sensitive resistor". Thermistors are further classified as "Positive Temperature

Coefficient" devices (PTC devices) or "Negative Temperature Coefficient" devices (NTC devices):

- PTC devices are devices whose resistance increases as their temperature increases.
- NTC devices are devices whose resistance decreases as their temperature increases.

Two types of temperature monitor channels are addressed herein, referring to the two main classes of transducers available on the market:

- TSM1: Wide range resistance acquisition, suitable for NTC thermistors (negative temperature characteristic).
- TSM2: Limited range resistance acquisition, suitable for platinum (PT) type.

The conditioning configuration to be used depends on the transducer used. Both TSM1 and TSM2 interfaces are specified in terms of resistance measurement accuracy.

NOTE TSM1 can be used for platinum type sensors (PT), but that generally shows worse accuracy than a well adapted TSM2. Also, TSM2 can be used for NTC type of sensor, but the temperature range is then restricted.

Examples of corresponding measurement error in terms of temperature are given in clause 5.3.5.5.

5.3.2 TSM acquisition layout

a. The thermistors shall be powered by the receiver, and

b. The resulting voltage shall be utilised to feed a dedicated analogue channel.

NOTE The objective of these requirements is that the receiver is able to directly interface with a passive thermistor:

5.3.3 TSM acquisition resolution

a. At least 12-bit resolution shall be used.

NOTE Even if the overall channel accuracy requirement can be met also with an 8-bit ADC, it is important to note that in this case the ADC quantization error alone contributes ±0,2% to the overall channel accuracy.

5.3.4 TSM wire configuration

a. Dedicated input and return line from the current source to each thermistor channel shall be provided.

5.3.5 TSM electrical characteristics

5.3.5.1 TSM1

5.3.5.1.1 Overview

The TSM1 interface has the following features:

- The measurable resistance range is specified from 0 to ∞ Ω.
- The interface is normalized with a parameter R_{NORM} (Ω), selectable within a specific range, where R_{NORM} is the resistance of the thermistor at a specified temperature point, where the highest temperature measurement accuracy is needed (the centre of the measurement range).

  NOTE R_{NORM} is selected per group of channels as a function of the sensor type and the temperature range of interest.

- The specified accuracy is expressed as a maximum error ±Δx.
- The specified accuracy in terms of resistance is obtained from a formula including R_{NORM} and Δx.
- The resistance accuracy is specified at the DHS unit terminals, i.e. excluding any error contribution from the thermistor or harness.

5.3.5.1.2 TSM1 error model

a. The maximum error in R_{th}, ΔR_{th}, shall be calculated as follows:

$$\Delta R_{th} = \frac{(R_{th} + R_{NORM})^2}{R_{NORM} - \Delta x \cdot (R_{th} + R_{NORM})} \cdot \Delta x, \quad \text{if } R_{NORM} > \Delta x \cdot (R_{th} + R_{NORM}),$$

$$\Delta R_{th} = \infty \quad \text{otherwise}$$

NOTE This calculation is based on the model of the TSM1 interface shown in Figure 5-3. $R_{th}(T)$ symbolizes the resistance of the thermistor as a function of temperature T.

The output from the ADC, x, has the range 0 to 1. The formula to express x as a function of $R_{th}(T)$ is then:

$$x = \frac{V_{in}}{V_{ref}} = \frac{R_{th}(T)}{R_{th}(T) + R_{NORM}}$$

Figure 5-4 shows how the relative error in R_{th}, $\Delta R_{th}/R_{th}$, varies with R_{th} with examples of R_{NORM} and Δx.

Examples have been evaluated for some specific thermistor types in clause 5.3.5.5, showing the error in terms of temperature.

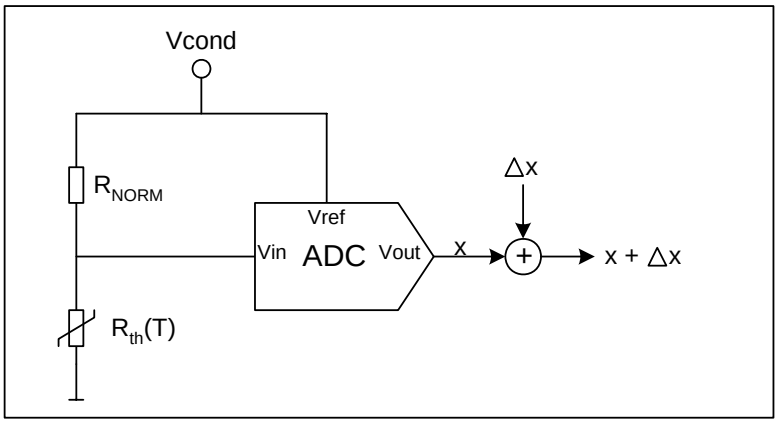

Figure 5-3: TSM1 reference model

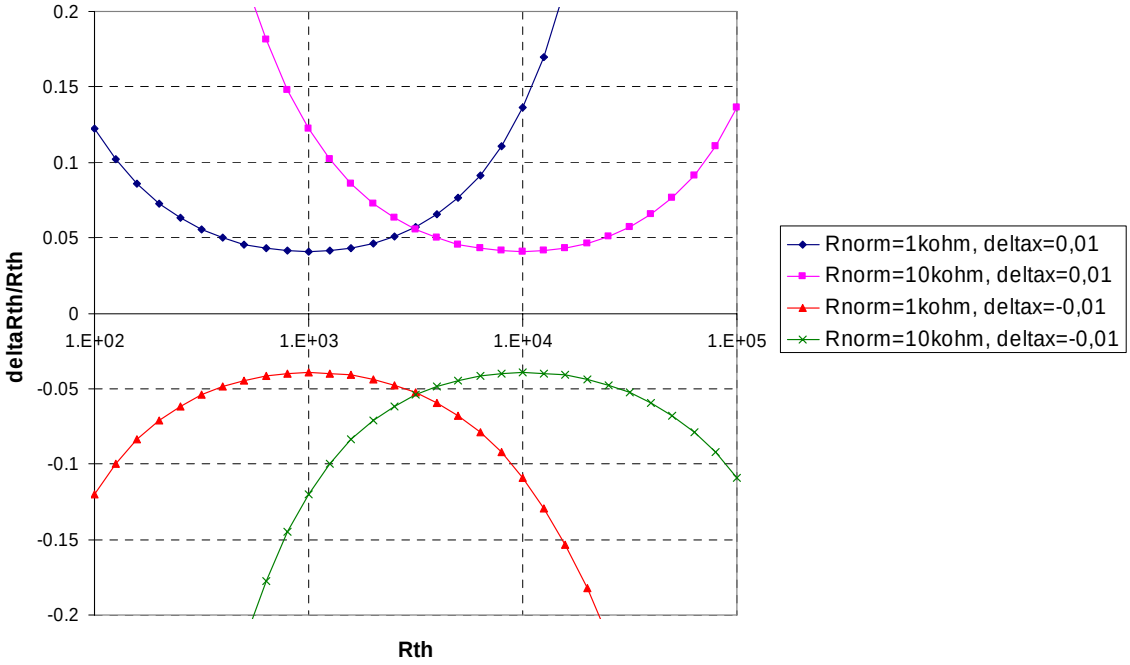

Figure 5-4: Requirement for $\Delta R_{th}/R_{th}$ as a function of R_{NORM} and R_{th}. $\Delta x = \pm 0{,}01$

5.3.5.1.3 TSM1 source electrical characteristics

a. The characteristics in Table 5-3 shall be provided.

Table 5-3: TSM1 source circuit characteristics

Reference	Characteristic	Value
5.3.5.1.3 a.1	Circuit type	Floating Resistive sensor
5.3.5.1.3 a.2	Transfer	DC coupled
5.3.5.1.3 a.3	Resistance range, R_s	0 to ∞ Ω
5.3.5.1.3 a.4	Fault voltage tolerance, V_{sft}	-17,5 V to +17,5 V with an overvoltage source impedance ≥ 1 kΩ

5.3.5.1.4 TSM1 receiver electrical characteristics

a. The characteristics in Table 5-4 shall be provided.

Table 5-4: TSM1 receiver circuit characteristics

Reference	Characteristic	Value
5.3.5.1.4 a.1	Circuit type	Single ended receiver with multiplexed inputs
5.3.5.1.4 a.2	Transfer	DC coupled
5.3.5.1.4 a.3	Sensor injected power, P_i	≤ 1 mW
5.3.5.1.4 a.4	Measurement error, Δx	< ±0,01
5.3.5.1.4 a.5	Parameterized resistance range, R_{NORM}	1 kΩ, to 10 kΩ, to be specified per group of channels
5.3.5.1.4 a.6	Fault voltage emission, V_{rfe}	-16,5 V to +16,5 V with a source impedance of ≥ 1kΩ
5.3.5.1.4 a.7	Fault resistance tolerance, R_{rft}	Short circuit to ground
NOTE	The low resistance range of R_{NORM} is suitable for TSM receiver systems using power switched thermistor conditioning, where low impedance is of special interest to achieve fast settling. The high resistance range of R_{NORM} is more suitable for TSM receiver systems using continuous thermistor conditioning, where low power is crucial, but fast settling is of less concern	

5.3.5.1.5 Harness

a. The wiring type shall be twisted n–tuple.

b. The capacitance C_{CC} measured between the two core wires shall be less than or equal to 1 nF.

5.3.5.1.6 Interface arrangement

The electrical I/F arrangement is specified in Figure 5-5.

NOTE 1 Circuitry and resistors are indicative only; other implementations meeting the above requirements are not excluded.

NOTE 2 In practical implementations a resistance to ground in the receiver is often used.

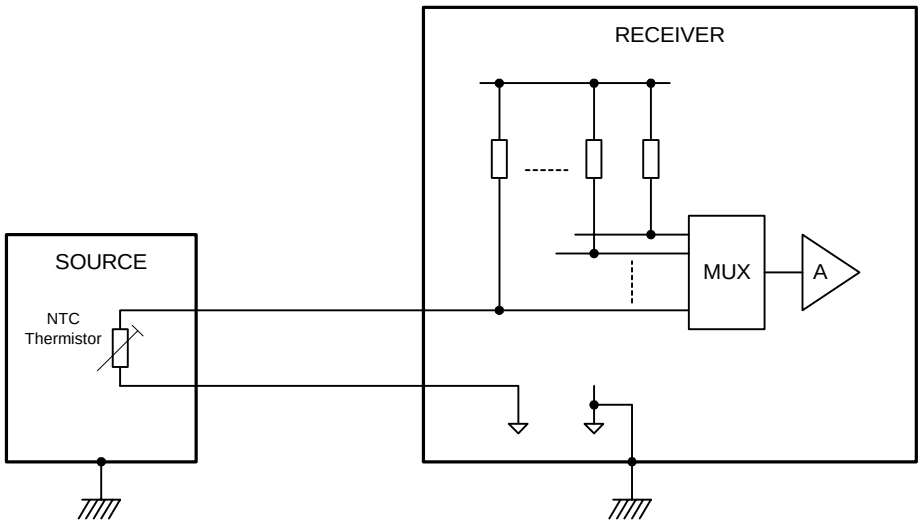

Figure 5-5: TSM1 interface arrangement

5.3.5.2 TSM2

5.3.5.2.1 Overview

The TSM2 interface has the following features:

- The measurable resistance range is specified from 0 Ω to up to R_{MAX}.

  NOTE R_{MAX} can be seen as the maximum resistance of the thermistor in the temperature range of interest.

- R_{MAX} can be chosen as characteristic of a group of channels within a specific range.
- The specified accuracy is expressed as a maximum error ±Δx.
- The specified accuracy in terms of resistance is expressed as $\Delta x \cdot R_{MAX}$.
- The resistance accuracy is specified at the DHS unit terminals, i.e. excluding any error contribution from the thermistor or harness.

5.3.5.2.2 TSM2 error model

a. The maximum error in R_{th}, ΔR_{th}, expressed as a function of Δx, shall be:

$$\Delta R_{th} = R_{MAX} \cdot \Delta x$$

5.3.5.2.3 TSM2 source electrical characteristics

a. The source shall meet the characteristics specified in Table 5-5.

Table 5-5: TSM2 source characteristics

Reference	Characteristic	Value
5.3.5.2.3 a.1	Circuit type	Floating Resistive sensor
5.3.5.2.3 a.2	Transfer	DC coupled
5.3.5.2.3 a.3	Resistance range, R_s	0 Ω to R_{MAX} R_s is selected per group of channels as a function of the sensor type and the temperature range of interest
5.3.5.2.3 a.4	Fault voltage tolerance, V_{sft}	-17,5 V to +17,5 V with an overvoltage source impedance ≥ 1 kΩ

5.3.5.2.4 TSM2 receiver electrical characteristics

a. The receiver shall meet the characteristics specified in Table 5-6.

Table 5-6: TSM2 receiver characteristics

Reference	Characteristic	Value
5.3.5.2.4 a.1	Circuit type	Single ended receiver with multiplexed inputs
5.3.5.2.4 a.2	Transfer	DC coupled
5.3.5.2.4 a.3	Sensor injected power, P_i	≤ 1 mW
5.3.5.2.4 a.4	Measurement error, Δx	< ±0,01
5.3.5.2.4 a.5	Parameterized resistance range, R_{MAX}	1 kΩ to 5 kΩ, to be specified per group of channels
5.3.5.2.4 a.6	Fault voltage emission, V_{rfe}	-16,5 V to +16,5 V with a source impedance of ≥ 1,0 kΩ
5.3.5.2.4 a.7	Fault tolerance, R_{rft}	Short circuit to ground

5.3.5.3 Harness

5.3.5.3.1 Wire type

a. The wire type shall be twisted n-tuple.

5.3.5.3.2 Core to core capacitance

a. The capacitance C_{CC} measured between the two core wires shall be less than or equal to 1 nF.

5.3.5.4 Interface arrangement

The electrical interface arrangement is specified in Figure 5-6.

NOTE Circuitry is indicative only; other implementations meeting the above requirements are not excluded.

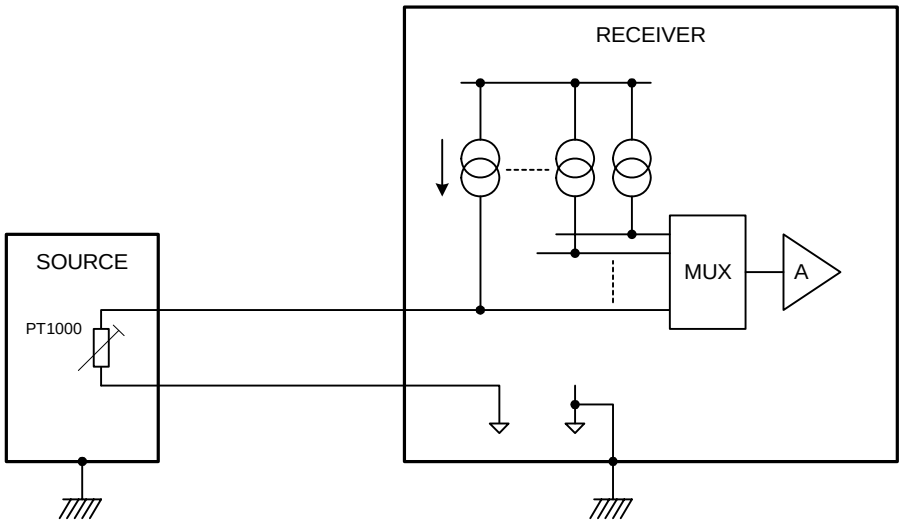

Figure 5-6: TSM2 interface arrangement

5.3.5.5 TSM examples

5.3.5.5.1 TSM1 examples

All thermistors of NTC type show a quasi-exponential temperature sensitivity in $\Delta R_{th}/R_{th}$ of roughly 4 %/°C or one decade per 60 °C. That means that when using an NTC thermistor for a TSM1 channel, Figure 5-4 can be used as a general indication of accuracy in temperature by:

- rescaling the y-axis by a factor 1°C/0,04,
- exchanging the logarithmic x-axis with a linear temperature scale where minimum point of $|\Delta R_{th}/R_{th}|$ is set to thermistor temperature at R_{NORM} and one decade corresponds to 60°C.

4K3A354 (ESCC Detail Specification No. 4006/013, variant 04) is a thermistor with nominally 4 kΩ resistance at 25°C. Figure 5-7 shows temperature accuracy specifically of a 4K3A354 thermistor connected to a TSM1 channel specified with RNORM = 4 kΩ . The figure does not include any inaccuracy of the sensor itself

YSI44907 is a thermistor with nominally 10 kΩ resistance at 25 °C. Figure 5-8 shows temperature accuracy specifically of a YSI44907 thermistor connected to a TSM1 channel specified with RNORM = 10 kΩ .

As shown in the two examples, the accuracy in terms of temperature becomes quite similar for different NTC thermistor types, provided that R_{NORM} is selected per type for the same temperature range.

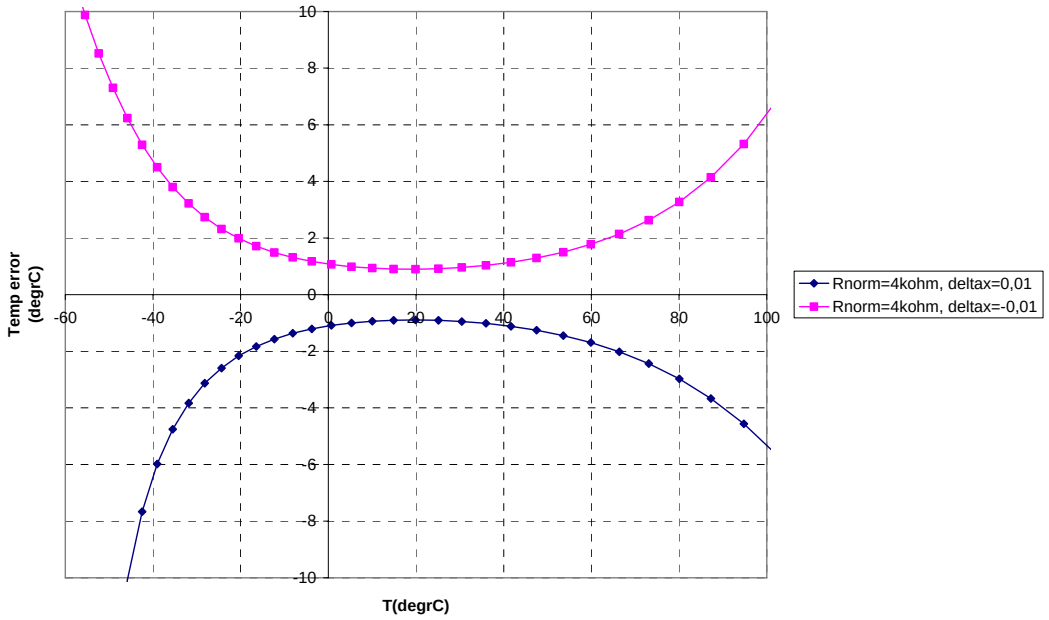

Figure 5-7: Example TSM1 and 4K3A354 thermistor

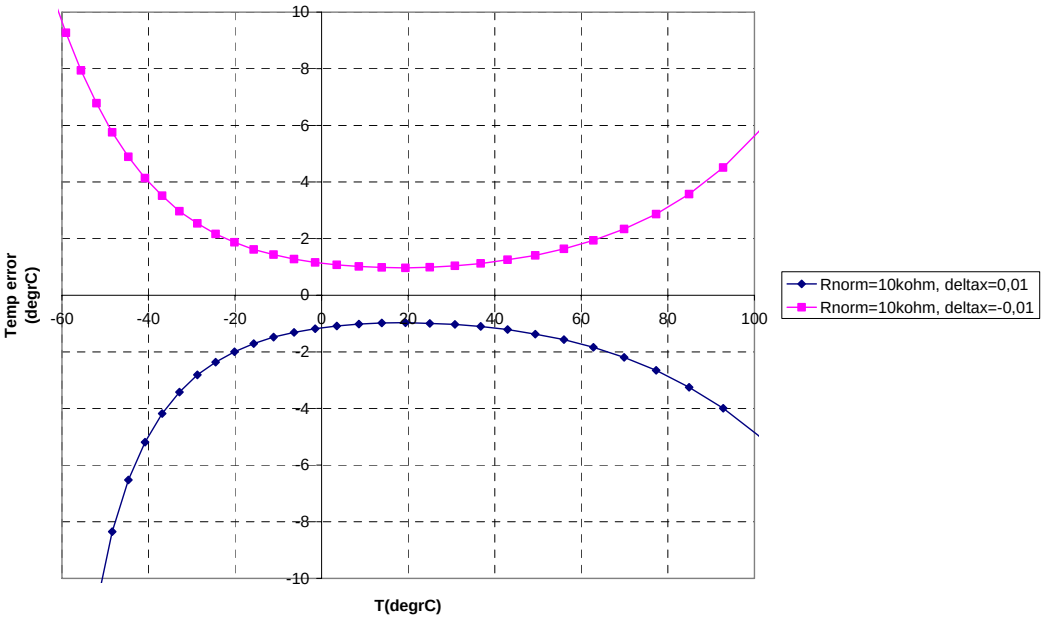

Figure 5-8: Example TSM1 and YSI44907 thermistor

5.3.5.5.2 TSM2, PT1000

The platinum temperature sensors show fairly constant temperature sensitivity in R_{th} of roughly $0.004 \cdot R_0/°C$, where R_0 is the nominal resistance (at 0 °C).

PT1000 is a platinum sensor with nominally 1000 Ω resistance at 0 °C. Figure 5-9 shows temperature accuracy specifically of a PT1000 connected to a TSM2 channel specified with R_{MAX} = 1700 Ω. The figure does not include any inaccuracy of the sensor itself.

R_{MAX} = 1700 Ω for the PT1000 sensor covers the temperature range up to +183 °C.

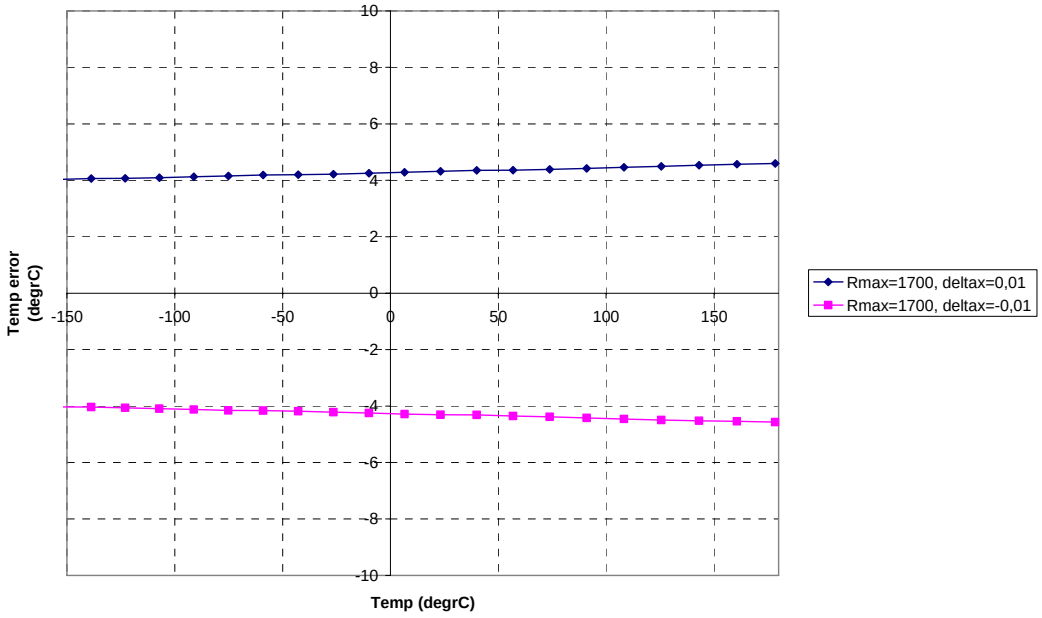

Figure 5-9: Example TSM2 and PT1000 thermistor

6
Bi-level discrete input interfaces

6.1 Bi-level discrete monitor (BDM) interface

6.1.1 Overview

The bi-level discrete monitor (BDM) interfaces are used for reasonably static, discrete status and telemetry monitoring by the core element. The monitored signal is bi-level discrete in that it can take only two values, high or low, indicated by the signal voltage.

The bi-level discrete interface consists of a signal, BL_DATA_IN, which is generated by the peripheral element. This signal is sampled periodically by the core element.

In a practical implementation, a number of bi-level discrete interfaces can be aggregated to form a multiple bit data word in the core element.

The bi-level discrete input interface consists of a signal, BL_DATA_IN, which can assume two values, high or low, with respect to the signal reference. This signal is maintained continuously by the peripheral element and can be sampled at any time by the core element.

On sampling, the core element encodes the BL_DATA_IN value into a single binary bit of data which can be embedded in a larger data word.

There are no timing parameters associated with this interface. The BL_DATA_IN signal is maintained continuously by the peripheral element and can generally be regarded as static. However, if the BL_DATA_IN signal is sampled during a transition from one level to the other, the result determined by the core element can be invalid.

6.1.2 Bi-level discrete monitor interface

6.1.2.1 Bi-level discrete monitor input interface - BL_DATA_IN signal

a. The peripheral element shall

   1. provide a BL_DATA_IN signal, and
   2. continually maintain such signal in one of two states, high (logical ‘1’) or low (logical ‘0’).

6.1.2.2 BDM electrical characteristics

6.1.2.2.1 Source circuit

a. The source circuit shall meet the characteristics specified in Table 6-1.

Table 6-1: BDM source characteristics

Reference	Characteristic	Value
6.1.2.2.1 a.1	Circuit type	Single ended
6.1.2.2.1 a.2	Transfer	DC coupled
6.1.2.2.1 a.3	Zero reference	Signal ground
6.1.2.2.1 a.4	Low output voltage, V_{Lout}	0 V to +0,5 V
6.1.2.2.1 a.5	High output voltage, V_{Hout}	2,4 V to +5,5 V, into a load of 100 kΩ or greater
6.1.2.2.1 a.6	Output impedance, Z_{out}	≤ 5 kΩ
6.1.2.2.1 a.7	Fault voltage emission, V_{sfe}	-1 V to +7 V
6.1.2.2.1 a.8	Fault voltage tolerance, V_{sft}	-17,5 V to +17,5 V with an overvoltage source impedance of 1,0 kΩ

6.1.2.2.2 Receiver circuit

a. The receiver circuit shall meet the characteristics specified in Table 6-2.

Table 6-2: BDM receiver characteristics

Reference	Characteristic	Value
6.1.2.2.2 a.1	Circuit type	Differential receiver with multiplexed inputs
6.1.2.2.2 a.2	Transfer	DC coupled
6.1.2.2.2 a.3	Low level differential input voltage, V_{Lin}	0 V to 0,9 V
6.1.2.2.2 a.4	High level differential input voltage, V_{Hin}	2,0 V to 5,5 V
6.1.2.2.2 a.5	Ground displacement voltage, V_{GD}	-1 V to 1 V up to 1 kHz rolling-off at 20 dB/decade up to 1 MHz
6.1.2.2.2 a.6	Input impedance, Z_{in}	During acquisition: ≥ 100 kΩ Outside acquisition: ≥ 100 kΩ DHS with power off: ≥ 10 kΩ
6.1.2.2.2 a.7	Fault voltage emission, V_{rfe}	-16,5 V to +16,5 V with a series impedance of ≥ 1,0 kΩ
6.1.2.2.2 a.8	Fault voltage tolerance, V_{rft}	-2 V to +8 V

6.1.2.3 Harness

6.1.2.3.1 Wire type

a. Both twisted pair and twisted shielded pair lines may be used.

b. Shields shall be connected to structure ground on source and receiver side.

6.1.2.3.2 Core to shield capacitance

a. If shielded pair is used, the capacitance C_{CS} measured between the core wire and the shield shall be ≤ 2 nF.

6.1.2.3.3 Core to core capacitance

a. If unshielded pair is used, the capacitance C_{CC} measured between the two core wires shall be ≤ 1 nF.

6.1.2.4 Interface arrangement

The electrical interface arrangement is depicted in Figure 6-1. The figure shows a specific implementation as example, but other implementations conforming to the requirements are not excluded.

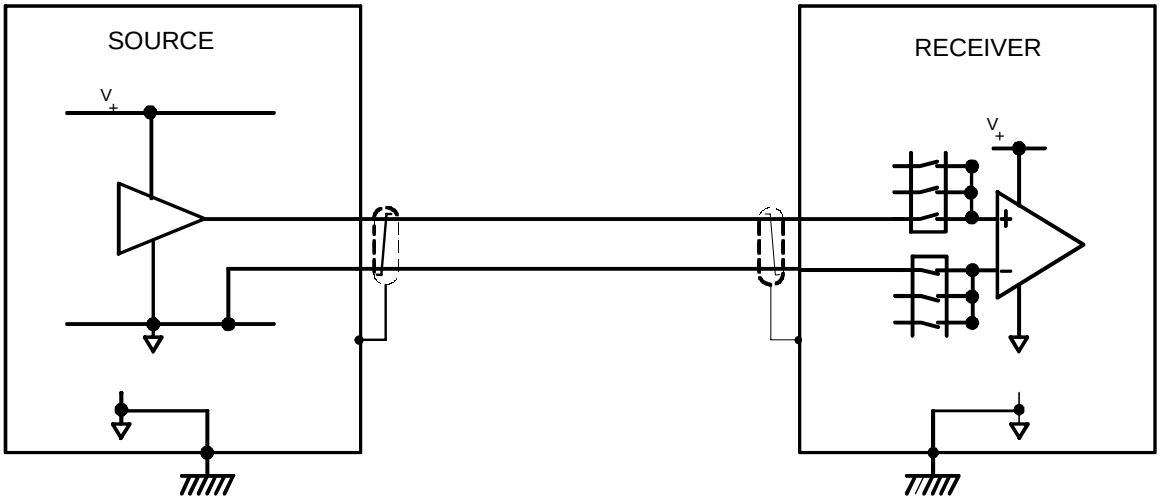

Figure 6-1: BDM Interface configuration

6.2 Bi-level switch monitor (BSM) interface

6.2.1 General principles

The bi-level switch monitor (BSM) interface is used by the core element to determine the status of a switch in the peripheral element. The peripheral element of this interface is entirely passive, consisting only of a single pole switch electrically isolated from all other components of the peripheral element.

This interface is used by the core element to determine the status of switches and relays in the peripheral element and has the advantage that it can be operated even when the peripheral element is powered down.

The switch status interface is entirely driven and operated by the core element. The core element provides a continuous reference voltage signal, and periodically samples the input signal and compares it to the reference. The result is encoded into a binary bit to indicate whether the switch was closed or open.

There are no timing constraints related to this interface since the switch status being monitored is normally static or changing infrequently. However, if the input signal is sampled while the switch status is changing, the result can be invalid.

The signal interface receiver is similar to a bi-level discrete (BDM) input with the following exceptions:

- Ground is referred to receiver (instead of source) ground.
- It is biased to a high level, when it is not being driven, by the connection of the input to a reference voltage through a resistance. When the switch contact is closed, the input signal is forced to a low level by presented low impedance.

The interface receiver converts such input signal in one of two digital states, high (logical '1') for switch source open status, or low (logical '0') for switch source closed status.

In case of specific needs, opto-couplers can be used. In that case the specific interfaces are defined on a system basis, thus they are not covered by this Standard.

6.2.2 Bi-level switch monitor interface

6.2.2.1 Source circuit

a. The source circuit shall meet the characteristics specified in Table 6-3.

Table 6-3: Switch source characteristics

Reference	Characteristic	Value
6.2.2.1 a.1	Circuit type	Floating Relay contact
6.2.2.1 a.2	Transfer	DC coupled
6.2.2.1 a.3	Operating current, I_{op}	Up to 10 mA
6.2.2.1 a.4	Operating voltage (open circuit), V_{op}	Up to 15 V
6.2.2.1 a.5	Switch closed resistance, R_C	≤ 50 Ω
6.2.2.1 a.6	Switch open resistance, R_O	≥ 1 MΩ
6.2.2.1 a.7	Fault voltage tolerance, V_{sft}	-17,5 V to +17,5 V with an overvoltage source impedance of 1,0 kΩ

6.2.2.2 Receiver circuit

a. The receiver circuit shall meet the characteristics specified in Table 6-4.

Table 6-4: Switch receiver characteristics

Reference	Characteristic	Value
6.2.2.2 a.1	Circuit Type	Single ended receiver with pull-up resistor
6.2.2.2 a.2	Transfer	DC coupled
6.2.2.2 a.3	Zero reference	Signal ground
6.2.2.2 a.4	Output current, I_{out}	0,1 mA to 10 mA (when contacts closed)
6.2.2.2 a.5	Output voltage, V_{out}	< 15 V (when contacts open)
6.2.2.2 a.6	Fault voltage emission, V_{rfe}	-16,5 V to +16,5 V with a source impedance of ≥ 1,0 kΩ
6.2.2.2 a.7	Fault tolerance, V_{rft}	Short circuit to ground

6.2.2.3 Harness

6.2.2.3.1 Wire type

a. The wire type shall be twisted n–tuple type.

6.2.2.3.2 Core to core capacitance

a. The capacitance C_{CC} measured between the two core wires shall be ≤ 1 nF.

6.2.2.4 Interface arrangement

The electrical interface arrangement is depicted in Figure 6-2, which shows specific implementation to be taken as example, but other implementations conforming to requirements are not excluded.

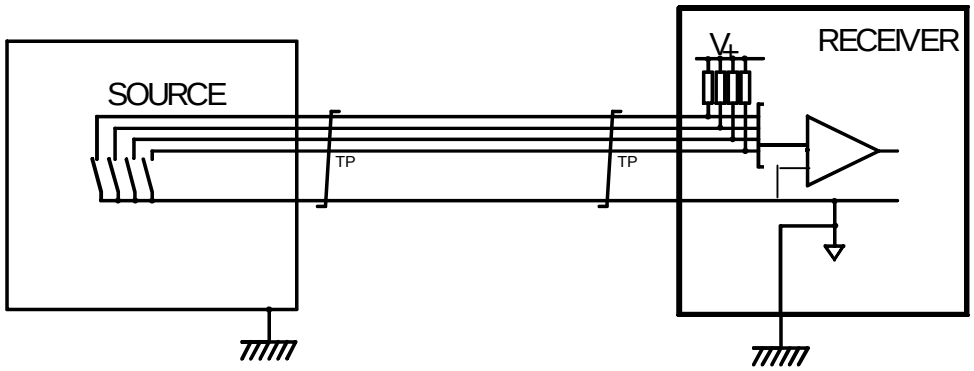

Figure 6-2: Switch status circuit interface arrangement

7
Pulsed command interfaces

7.1 High power command (HPC) interfaces

7.1.1 General principles

The high power pulse (HPC) command interfaces are intended for load driving interfaces and, for example, can be used to switch relays or similar loads. The high current capabilities of these interfaces lead to their protection against short circuiting and against failure in a high current mode.

The high power pulse command consists of a single signal, HPC_OUT(H), generated by the core element. This is connected by a single ended circuit to the input at the peripheral element. The interface is entirely controlled from the core element.

Three classes of HPC are defined here:

- LV-HPC : low voltage HPC (clause 7.1.3),
- HV-HPC : high voltage HPC (clause 7.1.4), and
- HC-HPC : high current HPC (clause 7.1.5).

7.1.2 High power command interface

7.1.2.1 High power pulse command - HPC_OUT(H) signal

a. The core element shall

1. provide an HPC_OUT(H) signal, and
2. drive such a signal.

7.1.2.2 High power pulse command - HPC_OUT(H) signal passive state

a. The passive state of the HPC_OUT(H) signal shall be low.

7.1.2.3 High power pulse command - HPC_OUT(H) signal active state

a. The active state of the HPC_OUT(H) signal shall be high.

7.1.2.4 High power pulse command output – driver unpowered

a. The HPC_OUT(H) output signal shall be in passive state when the driver is unpowered.

7.1.2.5 High power pulse command output - failure mode

a. The design of the high power pulse command interface shall ensure that no failure mode results in the output being permanently active (high state).

7.1.2.6 High power command configuration

a. The high power discrete pulse command source shall be referenced to source signal ground.

b. The load shall be isolated from any user electrical reference.

7.1.2.7 High power command transient protection

a. Both the high power pulse command source and receiver shall be equipped with circuits to suppress any switching transients.

NOTE This is particularly important to suppress transients due to inductive loads such as relays, which can cause the current drive capability, or the overvoltage capability of the source to be exceeded.

7.1.2.8 High power command short circuit protection

a. The high power pulse command source shall be short circuit proof for short circuits to source or receiver signal ground and structure.

7.1.3 Low voltage high power command (LV-HPC) electrical characteristics

7.1.3.1 Source circuit

a. The source circuit shall meet the characteristics specified in Table 7-1.

Table 7-1: LV-HPC source characteristics

Reference	Characteristics	Value
7.1.3.1 a.1	Circuit type	Single ended driver return over wire
7.1.3.1 a.2	Transfer	DC coupled
7.1.3.1 a.3	Active state output voltage, V_{Aout}	12 V to 16 V
7.1.3.1 a.4	Passive state output leakage current, I_{Pout}	< 100 µA
7.1.3.1 a.5	Pulse width, t_P	4 ms to 1024 ms (system design selectable depending on receiver characteristics)
7.1.3.1 a.6	Output voltage rise and fall times, t_r, t_f	50 µs to 2 ms when connected to a resistive load of 100 Ω
7.1.3.1 a.7	Active current drive capability, I_{Aout}	180 mA
7.1.3.1 a.8	Free-wheeling current capability (in Passive state)	I_{Aout} during t_P
7.1.3.1 a.9	Short circuit output current, I_{SC}	≤ 400 mA
7.1.3.1 a.10	Fault voltage tolerance, V_{sft}	0 V to +20 V
7.1.3.1 a.11	Fault voltage emission, V_{sfe}	0 V to +19 V

7.1.3.2 Receiver circuit

a. The receiver circuit shall meet the characteristics specified in Table 7-2.

Table 7-2: LV-HPC receiver characteristics

Reference	Characteristics	Value
7.1.3.2.a.1	Circuit type	Relay or opto-coupler
7.1.3.2 a.2	Transfer	DC coupled
7.1.3.2 a.3	Active level at unit input terminal, V_{Ain}	11 V to 16 V
7.1.3.2 a.4	Passive current at unit input terminal (no activation), I_{Pin}	200 µA
7.1.3.2 a.5	Passive level transient immunity, t_{Ptran}	No activation for pulses up to the active level 100 µs wide
7.1.3.2 a.6	Load current, I_{load}	≤ 180 mA (at 16 V)
7.1.3.2 a.7	Inputs to chassis isolation, Z_{iso}	> 1 MΩ
7.1.3.2 a.8	Fault voltage emission, V_{rfe}	0 V to +19 V
7.1.3.2 a.9	Fault voltage tolerance, V_{rft}	0 V to +20 V

7.1.4 High voltage high power command (HV-HPC) electrical characteristics

7.1.4.1 HV-HPC source circuit

a. The HV-HPC source circuit shall meet the characteristics specified in Table 7-3.

Table 7-3: HV-HPC source characteristics

Reference	Characteristic	Value
7.1.4.1 a.1	Circuit type	Single ended driver return over wire
7.1.4.1 a.2	Transfer	DC coupled
7.1.4.1 a.3	Active state output voltage, V_{Aout}	22 V to 29 V
7.1.4.1 a.4	Passive state output leakage current, I_{Pout}	< 100 µA
7.1.4.1 a.5	Pulse width, t_P	4 ms to 1024 ms (system design selectable depending on receiver characteristics)
7.1.4.1 a.6	Output voltage rise and fall times, t_r, t_f	50 µs to 2 ms when connected to a resistive load of 200 Ω
7.1.4.1 a.7	Active current drive capability, I_{Aout}	180 mA
7.1.4.1 a.8	Free-wheeling current capability (in passive state)	I_{Aout} during t_P
7.1.4.1 a.9	Short circuit output current, I_{SC}	≤ 400 mA
7.1.4.1 a.10	Fault voltage tolerance, V_{sft}	0 V to +33 V
7.1.4.1 a.11	Fault voltage emission, V_{sfe}	0 V to +32 V

7.1.4.2 HV-HPC receiver circuit

a. The HV-HPC receiver circuit shall meet the characteristics specified in Table 7-4.

Table 7-4: HV-HPC receiver characteristics

Reference	Characteristic	Value
7.1.4.2 a.1	Circuit type	Relay or opto-coupler
7.1.4.2 a.2	Transfer	DC coupled
7.1.4.2 a.3	Active level at unit input terminal, V_{Ain}	21 V to 29 V
7.1.4.2 a.4	Passive current at unit input terminal (no activation), I_{Pin}	200 µA
7.1.4.2 a.5	Passive level transient immunity, t_{Ptran}	No activation for pulses up to the active level 100 µs wide
7.1.4.2 a.6	Load current, I_{load}	≤ 180 mA (at 29 V)
7.1.4.2 a.7	Inputs to chassis isolation, Z_{iso}	> 1 MΩ
7.1.4.2 a.8	Fault voltage emission, V_{rfe}	0 V to +32 V
7.1.4.2 a.9	Fault voltage tolerance, V_{rft}	0 V to +33 V

7.1.5 High current high power command (HC-HPC) electrical characteristics

7.1.5.1 HC-HPC source circuit

a. The HC-HPC source circuit shall meet the characteristics specified in Table 7-5.

Table 7-5: HC-HPC source characteristics

Reference	Characteristic	Value
7.1.5.1 a.1	Circuit type	Single ended driver return over wire
7.1.5.1 a.2	Transfer	DC coupled
7.1.5.1 a.3	Active state output voltage, V_{Aout}	22 V to 29 V
7.1.5.1 a.4	Passive state output leakage current, I_{Pout}	< 1 mA
7.1.5.1 a.5	Pulse width, t_P	4 ms to 1024 ms (system design selectable depending on receiver characteristics)
7.1.5.1 a.6	Output voltage rise and fall times, t_r, t_f	50 µs to 2 ms when connected to a resistive load of 50 Ω
7.1.5.1 a.7	Active current drive capability, I_{Aout}	600 mA
7.1.5.1 a.8	Free-wheeling current capability (in passive state)	I_{Aout} during t_P
7.1.5.1 a.9	Short circuit output current, I_{SC}	≤ 1 A
7.1.5.1 a.10	Fault voltage tolerance, V_{sft}	0 V to +33 V
7.1.5.1 a.11	Fault voltage emission, V_{sfe}	0 V to +32 V

7.1.5.2 HC-HPC receiver circuit

a. The HC-HPC receiver circuit shall meet the characteristics specified in Table 7-6.

Table 7-6: HC-HPC receiver characteristics

Reference	Characteristic	Value
7.1.5.2 a.1	Circuit type	Relay
7.1.5.2 a.2	Transfer	DC coupled
7.1.5.2 a.3	Active level at unit input terminal, V_{Ain}	20 V to 29 V
7.1.5.2 a.4	Passive level at unit input terminal (no activation), I_{Pin}	2 mA
7.1.5.2 a.5	Passive level transient immunity, t_{Ptran}	No activation for pulses up to the active level 1 ms wide
7.1.5.2 a.6	Load current, I_{load}	≤ 600 mA (at 29 V)
7.1.5.2 a.7	Inputs to chassis isolation, Z_{iso}	> 1 MΩ
7.1.5.2 a.8	Fault voltage emission, V_{rfe}	0 V to +32 V
7.1.5.2 a.8	Fault voltage tolerance, V_{rft}	0 V to +33 V

7.1.6 Wiring type

a. Both twisted n-tuples and twisted shielded n-tuples lines may be used.

b. Shield shall be connected to structure ground on source and receiver side.

7.1.7 High power command interface arrangement

The interface arrangement is presented in Figure 7-1, which shows a specific implementation taken as an example, but other implementations conforming to requirements are not excluded.

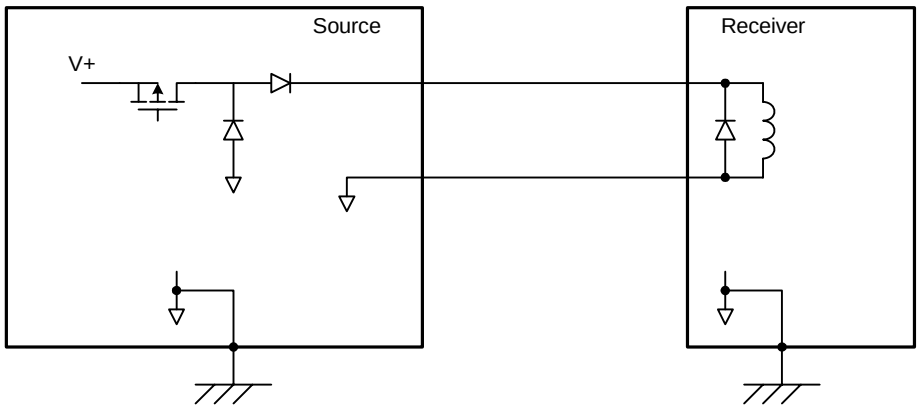

Figure 7-1: HPC interface arrangement

7.2 Low power command (LPC) interface

7.2.1 General

The low power (LPC) command interfaces are intended for driving opto-coupler channels.

Two types of opto-coupler interfaces are considered namely the opto-coupler pulse interface, LPC-P, and the opto-coupler static bi-level interface, LPC-S.

The low power command consists of a single signal, LPC_OUT(H), generated by the core element. This is connected by a single ended circuit to the input at the peripheral element. The interface is entirely controlled from the core element.

7.2.2 Low power command interface

7.2.2.1 Low power command - LPC_OUT(H) signal

a. The core element shall

1. provide an LPC_OUT(H) signal, and
2. drive such a signal.

7.2.2.2 Low power command - LPC_OUT(H) signal passive state

a. The passive state of the LPC_OUT(H) signal shall be low.

7.2.2.3 Low power command - LPC_OUT(H) signal active state

a. The active state of the LPC_OUT(H) signal shall be high.

7.2.2.4 Low power command output – driver unpowered

a. The LPC_OUT(H) output signal shall be in passive state when the driver is unpowered.

7.2.2.5 Low power command configuration

a. The low power discrete pulse command source shall be referenced to source signal ground.

b. The load shall be isolated from any user electrical reference.

7.2.2.6 Low power command short circuit protection

a. The low power pulse command source shall be short circuit proof for short circuits to source or receiver signal ground and structure.

7.2.3 LPC electrical characteristics

7.2.3.1 Source circuit

a. The source circuit shall meet the characteristics specified in Figure 7-2 and Table 7-7.

NOTE Figure 7-2 shows the LPC source high level output voltage vs. load current. A typical load is indicated as a dashed line.

Table 7-7: LPC source characteristics

Reference	Characteristics	Value
7.2.3.1 a.1	Circuit type	Single ended driver return over wire
7.2.3.1 a.2	Transfer	DC coupled
7.2.3.1 a.3	Output resistance, R_{out}	370 Ω to 430 Ω
7.2.3.1 a.4	Active signal open circuit output voltage, V_{Aout}	4,4 V to 5,5 V
7.2.3.1 a.5	Passive signal open circuit output voltage, V_{Pout}	0 V to 0,5 V
7.2.3.1 a.6	Fault voltage emission, V_{sfe}	7 V with a source impedance ≥ 350 Ω
7.2.3.1 a.7	Fault tolerance	Continuous short circuit
7.2.3.1 a.8	Pulse width for LPC-P	4 ms ≤ t_d ≤ 120 ms

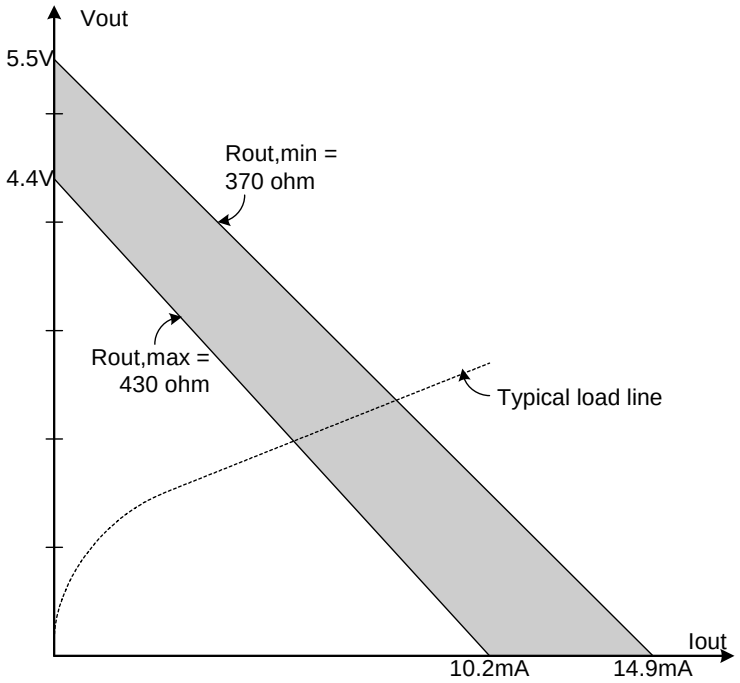

Figure 7-2: LPC active signal output voltage vs. load current

7.2.3.2 Receiver circuit

a. The receiver circuit shall meet the characteristics specified in Table 7-8.

Table 7-8: LPC receiver characteristics

Reference	Characteristics	Value
7.2.3.2 a	Circuit type	Opto-coupler, passive load
7.2.3.2 b	Transfer	DC coupled
7.2.3.2 c	Active input signal, V_{Ain}	4,4 V to 5,5 V through a 370 Ω to 450 Ω source resistance
7.2.3.2 d	Passive input signal, V_{Pin}	0 V to 0,5 V
7.2.3.2 e	Fault voltage tolerance, V_{rft}	7 V with a source impedance of ≥ 350 Ω
7.2.3.2 f	Input to chassis isolation, Z_{iso}	>1 MΩ

7.2.4 Wiring type

a. Both twisted n-tuples and twisted shielded n-tuples lines may be used.

b. Shield shall be connected to structure ground on source and receiver side.

7.2.5 Interface arrangement

The scheme depicted in Figure 7-3 is applicable to both LPC-P and LPC-S. The figure shows a specific implementation taken as an example, but other implementations compliant to requirements are not excluded.

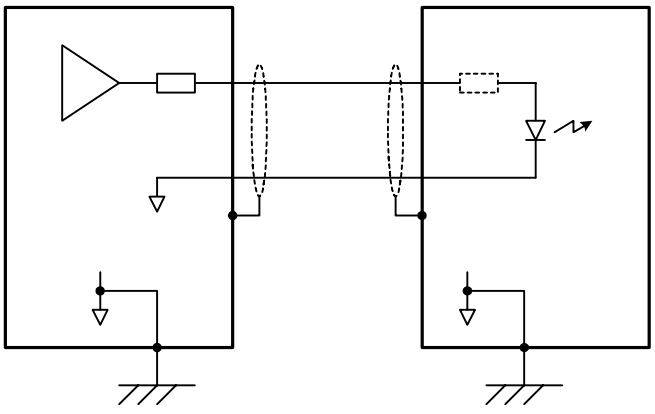

Figure 7-3: LPC-P and LPC-S interface arrangement

8
Serial digital interfaces

8.1 Foreword

This clause refers to the implementation of 16-bit serial digital point to point interfaces as specified in clause 8.2.

Other serial digital point to point interfaces may be used in space applications. They are not covered by this Standard. However, all digital interfaces referencing RS-422 as the physical layer (e.g. synchronization pulses) are recommended to comply with this specification for electrical characteristics as in clause 8.8.

8.2 General principles of serial digital interfaces

8.2.1 Overview

8.2.1.1

The serial digital interfaces are used to exchange digital data words between core and peripheral elements. The interface timing and clocking signals are controlled by the core element.

A serial digital interface which reads data from the peripheral element into the core element is called an input serial digital (ISD) interface. A serial digital interface which writes data out from the core element to the peripheral element is called an output serial digital (OSD) interface. A third class of serial digital interface is also introduced in this standard, namely the bi-directional serial digital (BSD) interface.

For space applications, serial digital interfaces shall be implemented in balanced differential form. In this form each signal is carried by a pair of conductors and the level of the signal is determined by the differential voltage between those conductors.

8.2.1.2

The serial digital interfaces are based on five signals, namely:

- GATE_WRITE provided by the core element which indicates when a write transfer (from core to peripheral) is underway,
- GATE_READ provided by the core element which indicates when a read transfer (from peripheral to core) is underway,
- DATA_CLK_OUT provided by the core element which controls the data transfer timing,
- DATA_OUT provided by the core element in the case of output and bi-directional interfaces, and
- DATA_IN provided by the peripheral element in the case of input and bi-directional interfaces.

In a practical implementation, the DATA_CLK_OUT and, for output interfaces, the DATA_OUT signal can be distributed to several devices. However, each device has its own unique GATE_WRITE (READ) signal.

Signals in Figure 8-2 and Figure 8-4 indicate the expected TRUE line waveform of the differential interface. DATA_OUT and DATA_IN low denotes a logic '0' and the corresponding HIGH denotes a logic '1'.

The serial interface timing in this standard is specified in proportion to the bit period (t_b), which is implementation dependent: once it is specified by the designer, the other characteristics are defined as a function of t_b.

As specified in 8.2.2, it is important that the peripheral element is designed to be compatible with any t_b specified in this Standard.

In addition the standard provides some recommended implementation options.

These interfaces correspond to the 16-bit digital channel telemetry interfaces and the 16-bit memory load commands described in TTC-B-01 but with some modifications. Most significantly, none of these word exchanges need be aligned with the OBDH bus interrogation slot interval.

NOTE 1 This is a relaxation of requirements and is in line with the philosophy of supporting systems which use MIL-STD-1553B instead of the ESA OBDH bus.

NOTE 2 Where an ESA OBDH bus is being used, this standard does not preclude synchronisation with the interrogation slot intervals, but does not specify its use.

NOTE 3 16-bit transfers are now preferably performed in a single burst rather than in two 8-bit.

8.2.2 General requirements

a. The physical layer of serial digital interfaces shall conform to the requirements in ANSI/TIA/EIA-422 and those specified in this clause 8 of this Standard.

b. The peripheral element should be designed to be compatible with any t_b specified in 8.3.4.8 and 8.4.4.9.

8.3 16-bit input serial digital (ISD) interface

8.3.1 16-bit input serial digital interface description

The signal arrangement for the 16-bit input serial digital interface is shown in Figure 8-2.

The 16-bit input serial digital interface consists of three signals, namely GATE_READ, DATA_CLK_OUT, and DATA_IN. The GATE_READ and DATA_CLK_OUT are used to control the operation of the interface and are driven by the core element. The DATA_IN signal is used to carry the data to be transferred and is driven by the peripheral element.

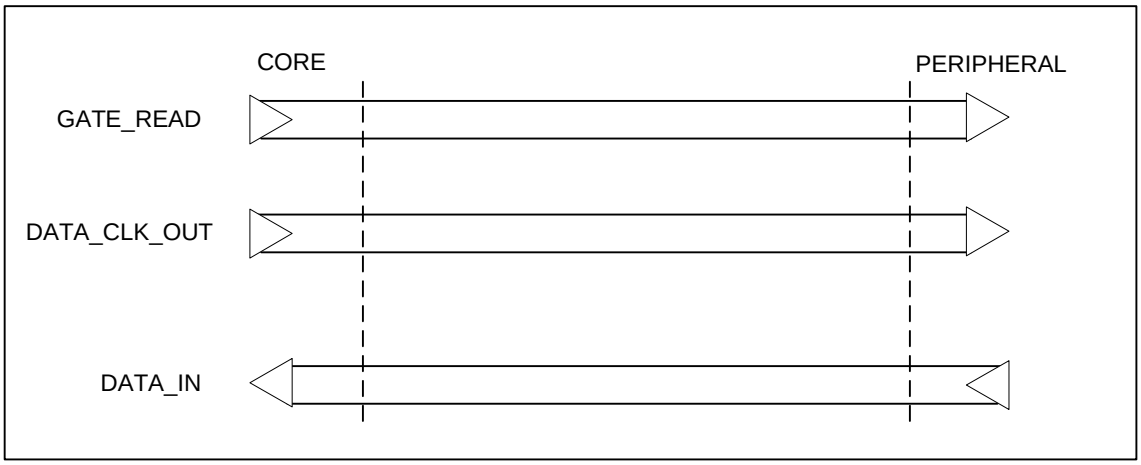

Figure 8-1: 16-bit input serial digital (ISD) interface signal arrangement

8.3.2 Signals skew

8.3.2.1 Introduction

In the values listed in Table 8-1 a skew is considered between any pair of signals or subsequent edges of the same signal to account for components characteristics and/or harness routing asymmetry.

8.3.2.2 Provisions

a. Maximum skew measured at core side shall be $\Delta t = 0{,}02 \times t_b$.

b. Maximum skew measured at peripheral side shall be $\Delta t = 0{,}04 \times t_b$.

8.3.3 ISD interface timing specification

The timing diagram shown in Figure 8-2 and the timing parameters in Table 8-1 specify the signal timing of the operational requirements specified in 8.3.4 for the 16-bit input serial digital interface.

A data transfer is initiated by the core element asserting GATE_READ. In response to this the peripheral element places the value of the most significant bit (bit 0) of the data word on the DATA_IN line.

After the GATE_READ falling edge (t_{cd}), the core element generates a sequence of sixteen low going pulses out onto the DATA_CLK_OUT line. The core element samples the DATA_IN line on the falling edge of each DATA_CLK_OUT pulse. This same falling edge causes the peripheral element to output the next bit of the data word on the DATA_IN line.

The DATA_IN line state is not sampled after the last DATA_CLK_OUT falling edge and can return to its quiescent 'don't care' state.

Sometime after the last DATA_CLK_OUT falling edge the core element de-asserts the GATE_READ signal indicating the end of the data transfer (t_{gd}).

GATE_READ$_{UP}$ can occur at the same time, or even slightly before, the last DATA_CLK_OUT$_{UP}$. The GATE_READ signal is subsequently kept de-asserted for a short period (t_{rec}) to enable the peripheral element to recover ready for the next data transfer.

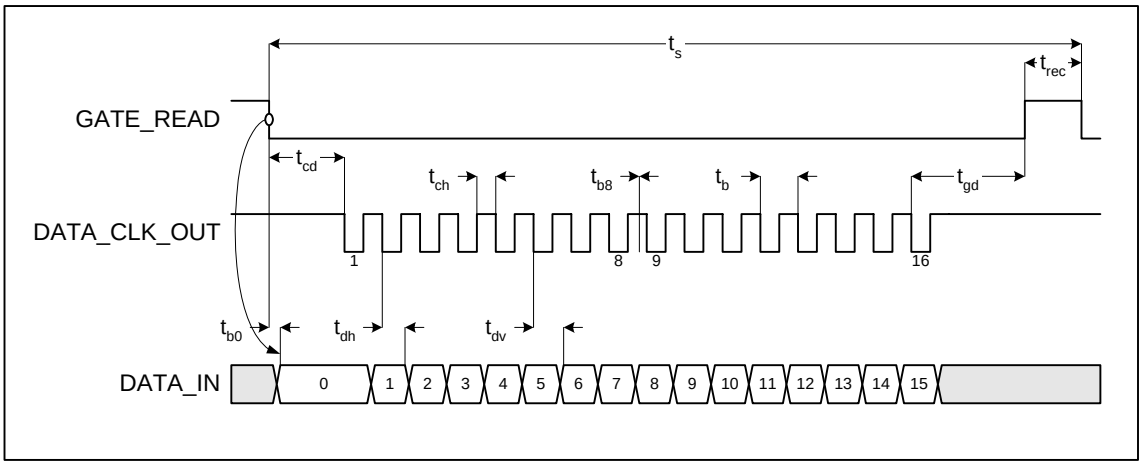

Figure 8-2: 16-bit input serial digital (ISD) interface

Table 8-1: 16-bit input serial digital (ISD) interface characteristics

Reference	Parameter	Description	Maximum	Minimum
8.3.3 a.1	t_b	Bit sampling interval	t_b (MAX)	t_b (MIN)
8.3.3 a.2	t_s	Repeated transfer period [a]	∞	$t_b \times 17$
8.3.3 a.3.(a)	t_{b0}	GATE_READ$_{DOWN}$ to bit 0 data valid, measured at peripheral element	$t_b \times 0,2$	-
8.3.3 a.3.(b)		GATE_ READ$_{DOWN}$ to bit 0 data valid, measured at core element	$t_b \times 0,3$	-
8.3.3 a.4	t_{cd}	Clock delay, GATE_ READ$_{DOWN}$ to first DATA_CLK_OUT$_{DOWN}$	$t_b \times 7 + \Delta t$	$t_b/2 - \Delta t$
8.3.3 a.5	t_{dh}	Data hold after DATA_CLK_OUT$_{DOWN}$	-	0
8.3.3 a.6.(a)	t_{dv}	Next data valid after DATA_CLK_OUT$_{DOWN}$, measured at peripheral element	$t_b \times 0,7$	-
8.3.3 a.6.(b)		Next data valid after DATA_CLK_OUT$_{DOWN}$, measured at core element	$t_b \times 0,8$	-
8.3.3 a.7.(a)	t_{ch}	Time DATA_CLK_OUT high (clock duty cycle) measured at core element	$t_b/2 \times 1,1$	$t_b/2 \times 0,9$
8.3.3 a.7.(b)		Time DATA_CLK_OUT high (clock duty cycle) measured at peripheral element	$t_b/2 \times 1,2$	$t_b/2 \times 0,8$
8.3.3 a.8	t_{gd}	Gating delay, last DATA_CLK_OUT $_{DOWN}$ to GATE_READ$_{UP}$	$t_b \times 4 + \Delta t$	$t_b/2 - \Delta t$
8.3.3 a.9	t_{rec}	Recovery interval, GATE_READ$_{UP}$ to GATE_READ $_{DOWN}$	∞	$t_b - \Delta t$
8.3.3 a.10	t_{b8}	Extension of gap [b] between clock pulse 8 and 9	$t_b \times 8$	0

[a] The transfer period is calculated as follows: $t_s = t_{cd} + t_{gd} + t_{rec} + 15 \cdot t_b$

[b] This is to allow 8-bit bursts in TTC-B-01 fashion

8.3.4 16-bit input serial digital interface: signal description

8.3.4.1 16-bit input serial digital - signals

a. The 16-bit input serial digital interface shall consist of three signals named GATE_READ, DATA_CLK_OUT, and DATA_IN.

NOTE 1 GATE_READ and DATA_CLK_OUT are active low signals.

NOTE 2 Signals are differential signals.

8.3.4.2 16-bit input serial digital - GATE_READ signal quiescent state

a. During quiescence, i.e. when no data transfer is taking place, the GATE_READ signal shall be maintained at a high logic level by the core element.

8.3.4.3 16-bit input serial digital - DATA_CLK_OUT signal

a. The DATA_CLK_OUT signal shall comprise sixteen low going pulses during each data transfer operation.

b. The DATA_CLK_OUT burst shall last 16 times the bit sampling pseudoperiod (tb) plus the optional extension of the clock gap between clock pulse 8 and 9 (tb8).

8.3.4.4 16-bit input serial digital - DATA_CLK_OUT signal quiescent state

a. Peripheral elements shall ignore the DATA_CLK_OUT signal when the GATE_READ signal is not asserted.

NOTE The reason is that during quiescence, i.e. when no data transfer is taking place, the DATA_CLK_OUT signal can oscillate (e.g. if it is shared with other peripheral elements).

8.3.4.5 16-bit input serial digital - DATA_IN signal

a. The peripheral element shall provide a DATA_IN signal.

b. The peripheral element shall ensure that the data on this signal is valid and stable on every DATA_CLK_OUT falling edge when GATE_READ is asserted.

8.3.4.6 16-bit input serial digital - DATA_IN signal quiescent state

a. During quiescence, the core element shall disregard the DATA_IN signal.

b. Peripheral element should maintain the DATA_IN signal in a stable state.

NOTE The actual level used by the peripheral element is not mandated.

8.3.4.7 16-bit input serial digital - data transfer

a. Data transfer on the 16-bit ISD shall be started by the core element, asserting the GATE_READ signal.

b. In response to the GATE_READ$_{DOWN}$ the peripheral element shall set the DATA_IN signal to the value of the most significant bit, bit 0, of the data word.

c. The core element shall then sample the DATA_IN signal on each falling edge of the DATA_CLK_OUT (DATA_CLK_OUT$_{DOWN}$).

d. After each DATA_CLK_OUT falling edge (DATA_CLK_OUT$_{DOWN}$), the peripheral element shall set the value of the DATA_IN signal to the value of the next most significant bit.

NOTE That means that if the current value of DATA_IN is bit n, the new value of DATA_IN is bit n+1.

e. When the 8th clock pulse on DATA_CLK_OUT has been generated, the gap to the next clock pulse may be increased by up to $t_b \times 8$.

f. When bit 15 of DATA_IN is reached, DATA_IN may be set to any value;

NOTE The reason is that the next value of DATA_IN is not important since the DATA_IN signal is not sampled after this.

8.3.4.8 16-bit input serial digital - bit sampling interval, t_b

a. The bit sampling interval, t_b, i.e. the interval between successive DATA_CLK_OUT rising edges, should be selected from the options shown in Table 8-2.

Table 8-2: t_b values

Reference	t_b (MIN)	t_b (MAX)	Maximum sustainable data
8.3.4.8 a	7,95 µs	8,05 µs	118,387
8.3.4.8 b	7,59 µs	7,67 µs	124,002
8.3.4.8 c	3,95 µs	4,05 µs	238,273
8.3.4.8 d	3,78 µs	3,85 µs	248,988

8.3.4.9 16-bit input serial digital - sampling period, t_s

a. The sampling period, t_s, defined as the minimum period between one GATE_READ$_{DOWN}$ and the next opportunity for a GATE_READ$_{DOWN}$, shall be not less than $t_b \times 17$.

NOTE The transfer period is calculated as follows:
$t_s = t_{cd} + t_{gd} + t_{rec} + 15 \cdot t_b$.

8.3.4.10 16-bit input serial digital - data hold after DATA_CLK_OUT$_{UP}$, t_{dh}

a. The data hold time after the DATA_CLK_OUT falling edge, t_{dh}, shall be not less than 0.

NOTE This ensures that the propagation delay always gives enough margin to hold the data.

8.4 16-bit output serial digital (OSD) interface description

8.4.1 16-bit output serial digital interface description

The signal arrangement for the 16-bit output serial digital interface is shown in Figure 8-2. Unless otherwise specified, signal properties are measured at the core interface.

The 16-bit output serial digital interface consists of three signals, namely GATE_WRITE, DATA_CLK_OUT, and DATA_OUT. All of three these signals are driven by the core element. The GATE_WRITE and DATA_CLK_OUT are used to control the operation of the interface and the DATA_OUT signal is used to carry the data to be transferred.

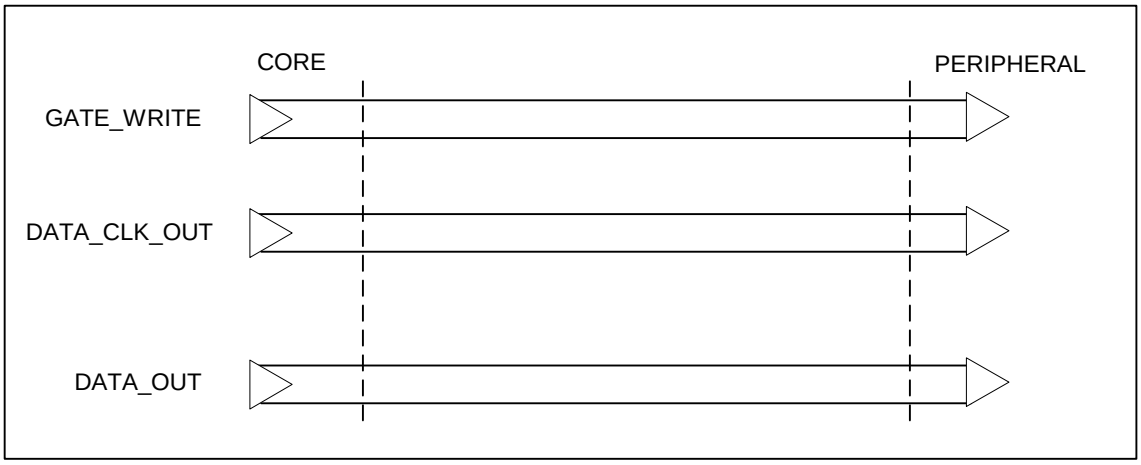

Figure 8-3: 16-bit output serial digital (OSD) interface signal arrangement

8.4.2 Signals skew

8.4.2.1 Overview

In the values listed in Table 8-3 a skew is considered between any pair of signals or subsequent edges of the same signal to account for component characteristics and/or harness routing asymmetry.

8.4.2.2 Provisions

a. Maximum skew measured at core side shall be $\Delta t = 0{,}02 \times t_b$.

b. Maximum skew measured at peripheral side shall be $\Delta t = 0{,}04 \times t_b$.

8.4.3 OSD interface timing specification

The timing diagram shown in Figure 8-4 and the timing parameters in Table 8-3 specify the timing of the operational requirements specified in 8.4.4 for the 16-bit output serial digital interface.

A data transfer is started by the core element asserting the GATE_WRITE signal to indicate that a data transfer is underway. After this (t_{b0}) the core element places the value of the most significant data bit (bit 0) on the DATA_OUT line.

Some time after the GATE_WRITE$_{DOWN}$, 16 low going pulses are output on the DATA_CLK_OUT signal. Each bit of the data word, including bit-0 is guaranteed valid on the DATA_CLK_OUT falling edge and for a given period before, data set up time t_{su}, and after it, data hold time t_{dh}.

GATE_WRITE is de-asserted after the last GATE_CLK_OUT$_{DOWN}$. This de-assertion can thus occur before the final GATE_CLK_OUT$_{UP}$. GATE_WRITE then is not reasserted before the interface recovery period has expired.

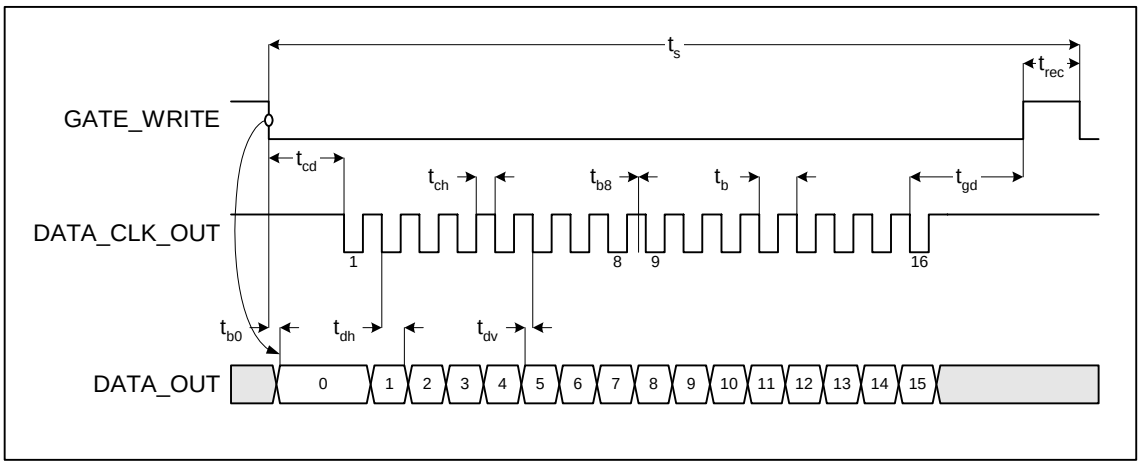

Figure 8-4: 16-bit output serial digital (OSD) interface

Table 8-3: 16-bit output serial digital (OSD) interface characteristics

Reference	Parameter	Description	Maximum	Minimum
8.4.1 a.1	t_b	Bit sampling interval	t_b (MAX)	t_b (MIN)
8.4.1 a.2	t_s	Repeated transfer period [a]	∞	$t_b \times 17$
8.4.1 a.3	t_{b0}	Bit 0 data valid after GATE_WRITE$_{DOWN}$	$t_b/4$	-
8.4.1 a.4	t_{cd}	Clock delay, GATE_WRITE$_{DOWN}$ to first DATA_CLK_OUT$_{DOWN}$	$t_b \times 7 + \Delta t$	$t_b/2 - \Delta t$
8.4.1 a.5	t_{dh}	Data hold after DATA_CLK_OUT$_{DOWN}$	-	$t_b/8 - \Delta t$
8.4.1 a.6	t_{su}	Data valid before DATA_CLK_OUT$_{DOWN}$	-	$t_b/4 - \Delta t$
8.4.1 a.7.(a)	t_{ch}	Time DATA_CLK_OUT high (clock duty cycle) measured at core element	$t_b/2 \times 1{,}1$	$t_b/2 \times 0{,}9$
8.4.1 a.7.(b)		Time DATA_CLK_OUT high (clock duty cycle) measured at peripheral element	$t_b/2 \times 1{,}2$	$t_b/2 \times 0{,}8$
8.4.1 a.8	t_{gd}	Gating delay, last DATA_CLK_OUT$_{DOWN}$ to GATE_WRITE$_{UP}$	$t_b \times 4 + \Delta t$	$t_b/2 - \Delta t$
8.4.1 a.9	t_{rec}	Recovery interval, GATE_WRITE$_{UP}$ to GATE_WRITE$_{DOWN}$	∞	$t_b - \Delta t$
8.4.1 a.10	t_{b8}	Extension of gap [b] between clock pulse 8 and 9	$t_b \times 8$	0

[a] The transfer period is calculated as follows: $t_s = t_{cd} + t_{gd} + t_{rec} + 15 \cdot t_b$

[b] This is to allow 8-bit bursts in TTC-B-01 fashion

8.4.4 16-bit output serial digital interface signal description

8.4.4.1 16-bit output serial digital - signals

a. The 16-bit output serial digital interface shall consist of three signals named GATE_WRITE, DATA_CLK_OUT, and DATA_OUT.

b. Signals shall be differential.

8.4.4.2 16-bit output serial digital - GATE_WRITE signal

a. The core element shall provide a GATE_WRITE signal asserted by the core element during a data transfer operation.

8.4.4.3 16-bit output serial digital - GATE_WRITE signal quiescent state

a. During quiescence, i.e. when no data transfer is taking place, the GATE_WRITE signal shall be maintained at a high logic level by the core element.

8.4.4.4 16-bit output serial digital - DATA_CLK_OUT signal

a. The core element shall provide a DATA_CLK_OUT signal.

b. The DATA_CLK_OUT signal shall comprise sixteen low going pulses during each data transfer operation.

c. The DATA_CLK_OUT burst shall last 16 times the bit sampling pseudoperiod (t_b) plus the optional extension of the clock gap between clock pulses 8 and 9 (t_{b8}).

8.4.4.5 16-bit output serial digital - DATA_CLK_OUT signal quiescent state

a. Peripheral elements shall ignore the DATA_CLK_OUT signal when the GATE_WRITE signal is not asserted.

NOTE The reason is that during quiescence, i.e. when no data transfer is taking place, the DATA_CLK_OUT signal can oscillate (e.g. if it is shared with other peripheral elements).

8.4.4.6 16-bit output serial digital - DATA_OUT signal

a. The core element shall provide a DATA_OUT signal used to transfer the data word bit serially.

8.4.4.7 16-bit output serial digital - DATA_OUT signal quiescent state

a. Peripheral elements shall ignore the DATA_OUT signal when the GATE_WRITE signal is not asserted.

NOTE The reason is that during quiescence, i.e. when no data transfer is taking place, the DATA_OUT signal can change (e.g. if it is shared with other peripheral elements).

8.4.4.8 16-bit output serial digital - data transfer

a. Data transfer on the 16-bit OSD shall be started by the core element, asserting the GATE_WRITE signal.

b. Shortly after the GATE_WRITE$_{DOWN}$ the core element shall set the DATA_OUT signal to the value of the most significant bit, bit 0, of the data word to be transferred.

c. The core element shall ensure that the DATA_OUT signal is valid on each falling edge of the DATA_CLK_OUT (DATA_CLK_OUT$_{DOWN}$) when GATE_WRITE is asserted.

d. The DATA_OUT signal shall meet the data set-up and hold times as specified in Table 8-3.

e. Shortly after (after t_{dh}) each DATA_CLK_OUT falling edge (DATA_CLK_OUT$_{DOWN}$), the core element shall update the value of the DATA_OUT signal to the value of the next most significant bit.

NOTE That means that if the current value of DATA_OUT is bit n, the new value of DATA_OUT is bit n+1.

f. When the 8th clock pulse on DATA_CLK_OUT has been generated, the gap to the next clock pulse may be increased by up to $t_b \times 8$.

g. When bit 15 of DATA_IN is reached, any value may be used;

NOTE The reason is that the next value of DATA_OUT is not important since the peripheral element does not sample the DATA_OUT signal after this.

8.4.4.9 16-bit output serial digital - bit sampling interval, t_b

a. The bit sampling interval, t_b, i.e. the interval between successive DATA_CLK_OUT rising edges, should be selected from the options shown in Table 8-2.

8.4.4.10 16-bit output serial digital - sampling period, t_s

a. The sampling period, t_s, defined as the minimum period between one GATE_WRITE$_{DOWN}$ and the next opportunity for a GATE_WRITE$_{DOWN}$, shall be not less than $t_b \times 17$.

NOTE The transfer period is calculated as follows:
$t_s = t_{cd} + t_{gd} + t_{rec} + 15 \cdot t_b$.

8.5 16-bit bi-directional serial digital (BSD) interface description

The 16-bit bi-directional serial digital interface provides a bi-directional serial digital data transfer capability using five signals as shown in Figure 8-5:

- GATE_WRITE,
- GATE_READ,
- DATA_CLK_OUT,
- DATA_OUT, and
- DATA_IN.

The GATE_WRITE and GATE_READ signals are used to indicate the direction of the transfer. The signal timing during output transfers is identical to that for the 16-bit output serial digital interface and during input transfers it is identical to the 16-bit input serial digital interface.

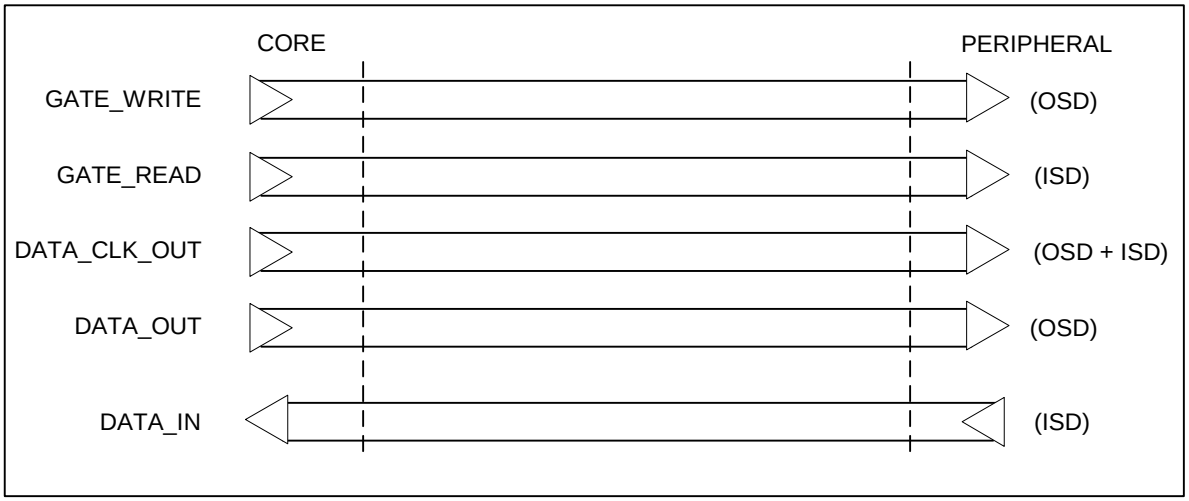

Figure 8-5: 16-bit bi-directional serial digital interface signal arrangement

There are two advantages offered by this interface.

- Firstly, it offers the possibility of writing a data value out to a peripheral element and then reading the same value back in order to verify that the write operation was performed correctly.
- Secondly, the interface can be expanded to address more than one register location within a peripheral element using only two extra signals for each additional register. The extra signals used are a dedicated GATE_WRITE(READ) signal for each new register to be accessed. All of the other signals can be common to all registers. This means that **n** registers can be accessed using only **2n + 3** signals which can lead to significant savings in terms of cables and connectors.

During an input transfer the data is input via the DATA_IN signal and the DATA_OUT signal assumes its quiescence state. During a data output transfer the data is output on the DATA_OUT signal and the DATA_IN signal assumes its quiescence state.

8.6 Serial digital interface electrical circuits description

The serial digital interface circuits are the conducting paths which convey the data and control signals which make up the interface between the core and peripheral elements. Each circuit consists of the conductors and any connectors or other components which comprise the electrical path.

Two circuits are used for each signal. These circuits operate in a balanced mode with reference to the core element differential ground potential, i.e. when one circuit carries a positive voltage, the complementary circuit carries a negative voltage of the same magnitude.

Figure 8-6 shows the relationship between circuits, signals, and the interface definition point for balanced differential serial digital interfaces.

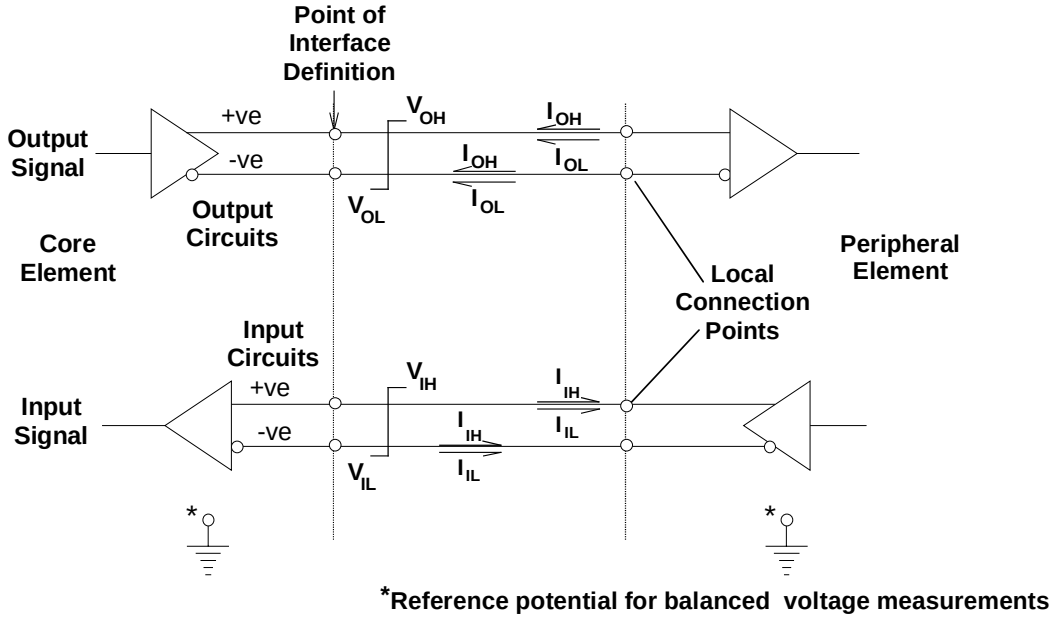

Figure 8-6: Balanced differential circuits for serial digital interfaces

8.7 Balanced differential serial digital interface signals

8.7.1 Balanced differential serial digital interface - GATE_WRITE circuits

a. A balanced differential pair of circuits called GATE_WRITE+ and GATE_WRITE- shall be provided.

b. The balanced differential pair specified in 8.7.1a shall

1. be driven by the core element, and
2. carry the GATE_WRITE signal.

8.7.2 Balanced differential serial digital interface - DATA_CLK_OUT circuits

a. A balanced differential pair of circuits called DATA_CLK_OUT+ and DATA_CLK_OUT- shall be provided.

b. The balanced differential pair specified in 8.7.2a. shall

1. be driven by the core element, and
2. carry the DATA_CLK_OUT signal.

8.7.3 Balanced differential serial digital interface - DATA_OUT circuits

a. For output serial digital interfaces, a balanced differential pair of circuits called DATA_OUT+ and DATA_OUT- shall be provided.

b. The balanced differential pair specified in 8.7.3a shall

1. be driven by the peripheral element, and
2. carry the DATA_OUT signal.

8.7.4 Balanced differential serial digital interface - DATA_IN circuits

a. For input serial digital interfaces, a balanced differential pair of circuits called DATA_IN+ and DATA_IN- shall be provided.

b. The balanced differential pair specified in 8.7.4a shall

1. be driven by the peripheral element, and
2. carry the DATA_IN signal.

8.7.5 Balanced differential serial digital interface - GATE_READ circuits

a. For bi-directional serial digital interfaces, a balanced differential pair of circuits called GATE_READ+ and GATE_READ- shall be provided.

b. The balanced differential pair specified in 8.7.5a shall

1. be driven by the core element, and
2. carry the GATE_READ signal.

8.8 Serial digital interface circuit electrical characteristics

8.8.1 Introduction

ANSI/TIA/EIA-422 (hereafter briefly RS-422) defines a balanced (differential) interface; specifying a single, unidirectional driver with multiple receivers (up to 32). RS-422 will support Point-to-Point, Multi-Drop circuits, but not Multi-Point.

Although the EIA standard does not show circuit grounding in either of the RS-422 circuits, this Standard includes recommendation on grounding in 8.8.2a.

8.8.2 Provisions

a. Serial digital interface circuits should be grounded as follows:

1. The drivers and receivers should be connected directly to circuit ground.
2. The circuit ground should be connected to chassis ground.

NOTE 1 Cabling is not specified in RS-422 but information can be found in [V11].

NOTE 2 Figure 8-7 illustrates this provision.

b. Serial digital interface circuit electrical characteristics shall meet the requirements specified in Table 8-4.

NOTE 1 Table 8-4 includes characteristics for compatibility with RS-422 (indicated with the number (422) in the table), and specific characteristics

NOTE 2 The values specified here-in grant correct operations in the following conditions:

- maximum signal frequency: 1 MHz;
- maximum cable length: 16 m;
- cable type: Twisted Shielded Pair 120 Ω Impedance.

NOTE 3 Compliance to the parameters indicated by the note (422) in Table 8-4 can be achieved by use of the following circuits:

HS-26C(T)31RH
HS-26C(T)32RH
HS-26CLV31RH
HS-26CLV32RH
Items 1 and 2 are 5 V supplied devices, items 3 and 4 are 3,3 V supplied devices. These devices can interoperate and comply with the specification in Table 8-4.

c. Serial digital interface shall be compliant to the interface arrangement specified in Figure 8-7.

d. Compliance to microcircuits characteristics others than the parameters indicated by the note (422) in Table 8-4., shall be verified on the project by Review of Design or Test.

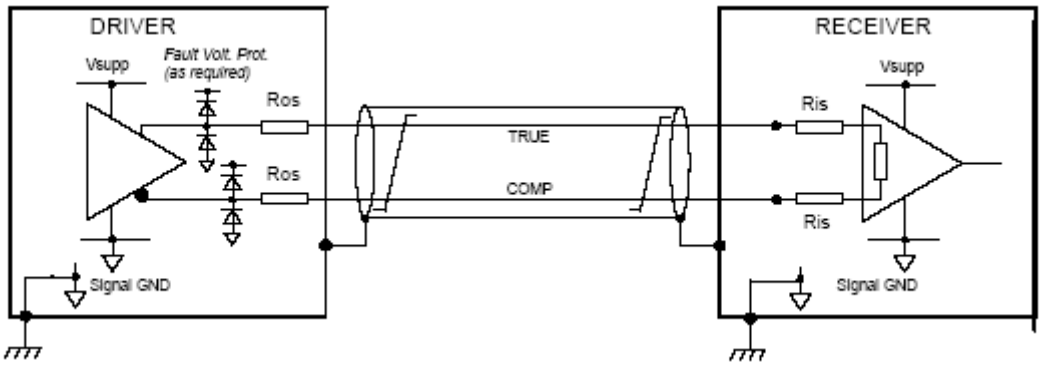

Figure 8-7: Example of serial digital interface arrangement

Table 8-4: Serial digital interface electrical characteristics

Reference	Characteristics	Value	Type	Notes
SOURCE CIRCUIT				
8.8 a.1	Electrical characteristics	Differential	(422)	
8.8 a.2	Differential output voltage open circuit, V_{OC}	1,8 V ≤ |V_{OC}| ≤ 6,0 V	Specific	
8.8 a.3	Output voltage TRUE and COMP lines, V_e	V_e ≤ 6 V	(422)	
8.8 a.4	Differential output impedance, Z_{out}	105 Ω ≤ Z_{out} ≤ 135 Ω	Specific	Note 1
8.8 a.5	Short circuit output current, I_A	|I_A| ≤ 150 mA for each terminal to ground	(422)	
8.8 a.6	Rise time, t_r	t_r ≤ 0,1 × t_b if t_b ≥ 200 ns t_r ≤ 20 ns if t_b ≤ 200 ns	(422)	Note 2
8.8 a.7	Output leakage current in power off, I_O	|I_O| ≤ 100 µA	(422)	Note 3
8.8 a.8	Fault voltage emission, V_{sfe}	0 V to 7 V (through 50 Ω minimum series resistance)	Specific	
8.8 a.9	Fault voltage tolerance, V_{sft}	-1,5 V to 7 V (applied through 1 kΩ series resistance R_{is})	Specific	
RECEIVER CIRCUIT				
8.8 a.10	Electrical characteristics	Differential	(422)	
8.8 a.11	Series protection, R_{is}	2 * 1 kΩ	Specific	
8.8 a.12	Max input voltage (each input w.r.t. ground), V_I	± 10 V	(422)	Note 4
8.8 a.13	Common mode acceptance (V1+V2)/2, V_{CM}	– 4 V to + 7 V	Specific	Note 5
8.8 a.14	Differential input voltage, V_{DI}	± |600 mV to 6 V| each voltage in this range must be interpreted as valid signal	Specific	Note 6
8.8 a.15	Fault voltage emission, V_{rfe}	0 V to 5,5 V (through 1 kΩ series resistance R_{is})	Specific	
8.8 a.16	Fault voltage tolerance, V_{rft}	-1,5 V to 8,5 V	Specific	

Note 1: Output impedance to be matched with 120 Ω cable impedance. Recommended range of the R_{os} resistors between 50 Ω and 60 Ω, considering 10 Ω typical driver output impedance, when using HS-26C(T)31RH.

Note 2: t_b time duration of the unit interval at the applicable data rate (normally 0,5 * period duration).

Note 3: –0,25 V to +6 V applied at the output terminals.

Note 4: RS-422 standard parameters given for reference only.

Note 5: This figure is compatible with both performances of 5 V and 3,3 V devices (HS26CLV32RH).

Note 6: Minimum threshold considering 1 kΩ series resistors (the devices commonly used have a threshold of ±400 mV, for reference see Figure 8-8).

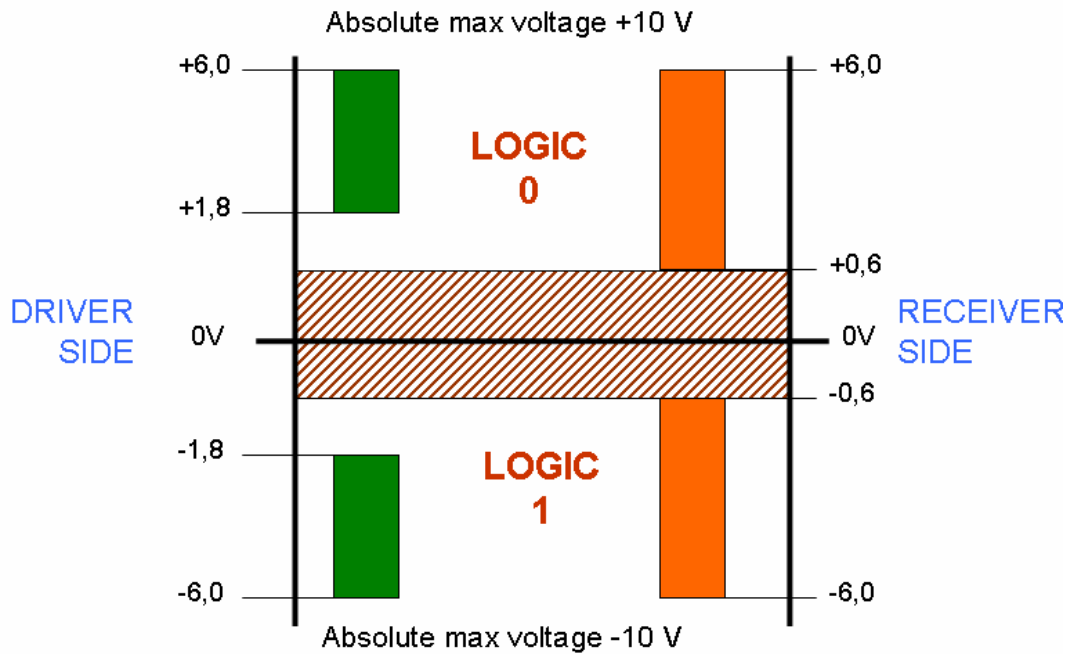

Figure 8-8: Threshold levels for ECSS-E-50-14 differential circuits

Annex A (informative)
Tailoring guidelines

Tailoring for this Standard is limited to the adoption of specific discrete interfaces listed hereby:

- Analogue signal interfaces
  - Analogue signal monitor (ASM) interface
  - Temperature sensors monitor (TSM) interfaces
- Bi-level discrete input interfaces
  - Bi-level discrete monitor (BDM) interface
  - Bi-level switch monitor (BSM) interface
- Pulsed command interfaces
  - High power command (HPC) interfaces
  - Low power command (LPC) interface
- Serial digital interfaces
  - 16-bit input serial digital (ISD) interface
  - 16-bit output serial digital (OSD) interface description
  - 16-bit bi-directional serial digital (BSD) interface description

Modification of existing or addition of requirements within a specific interface definition should not be done.

Bibliography

ECSS-S-ST-00 ECSS system - Description, implementation and general requirements