CPE 151

Digital IC Design

Project No. 2 (D Flip Flop)

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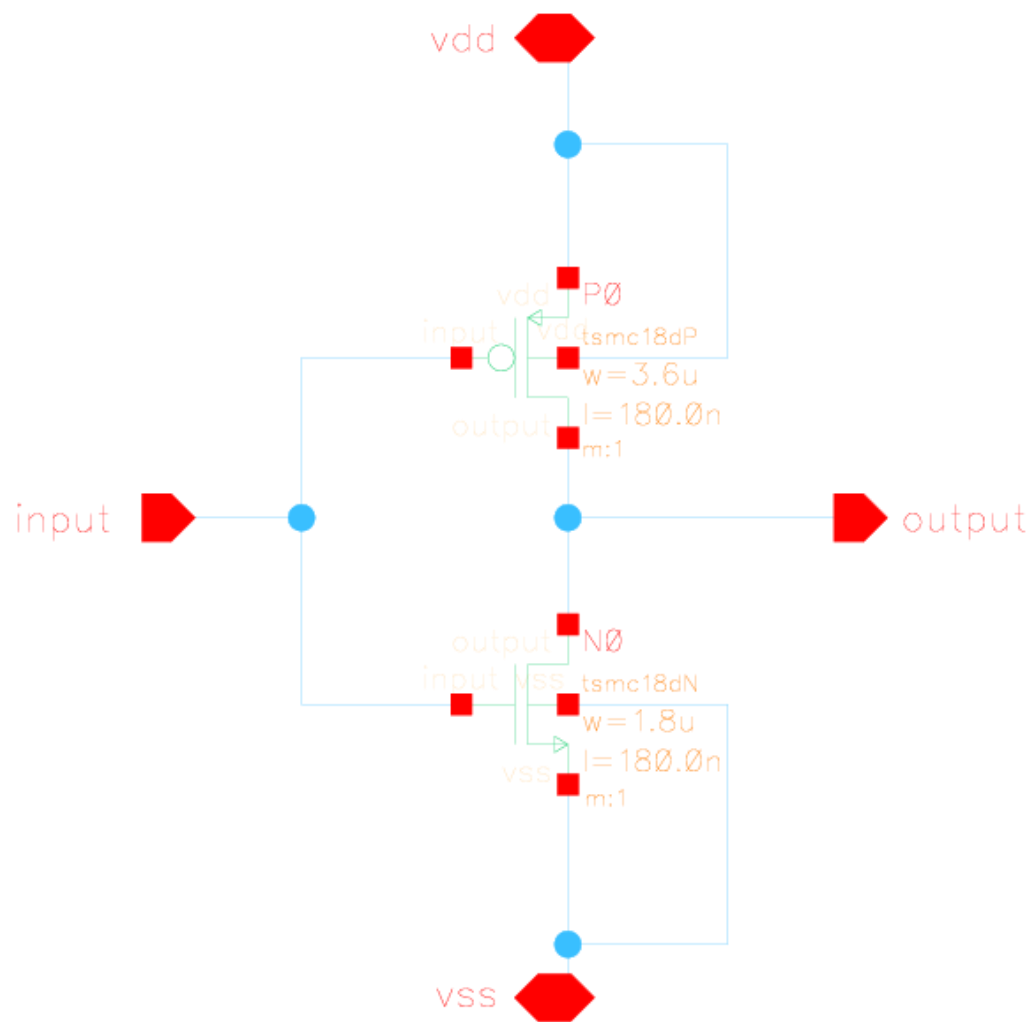Date: November 12, 2019

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Inverter

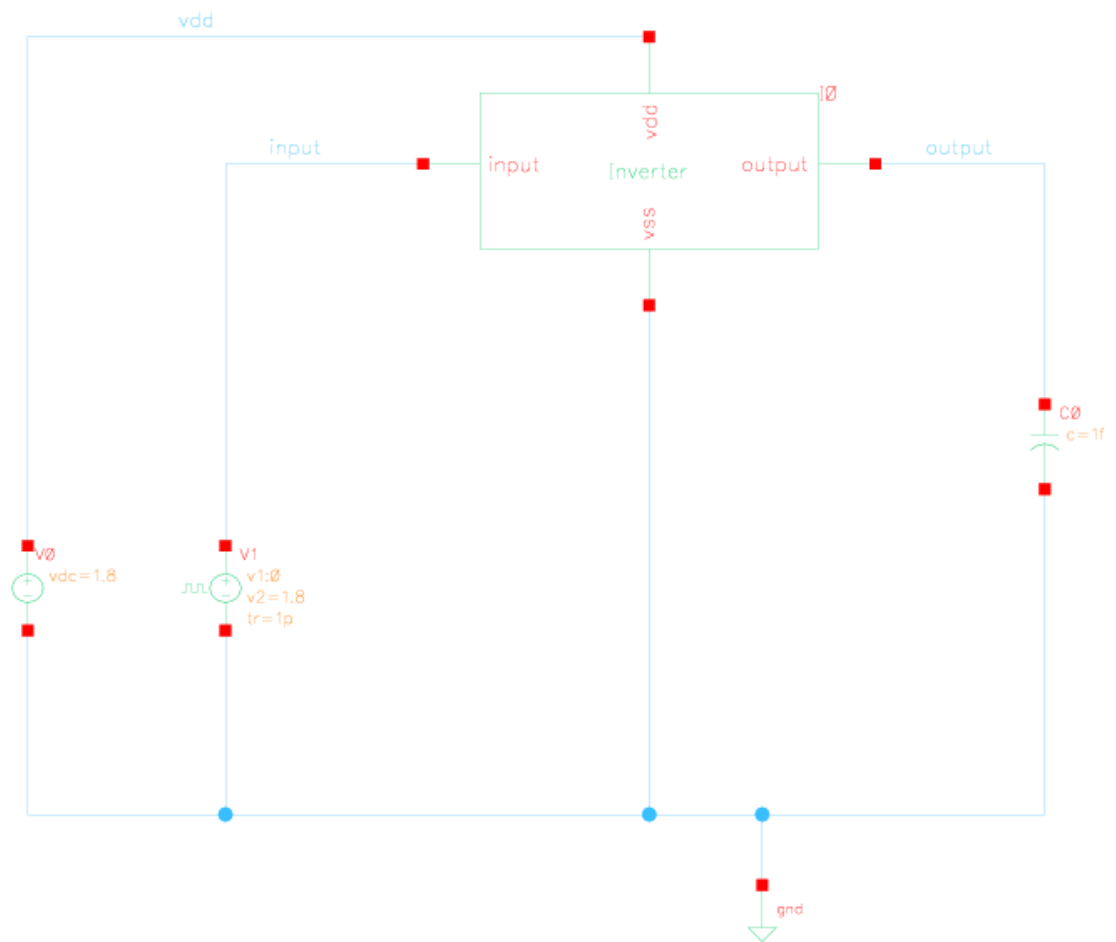(W/L)n = 1.8 /0.18

(W/L)p = 3.6/0.18

Schematic (Inverter):

Test bench (Inverter):

Test bench Waveform (Inverter):

Transient Response   **Sun Sep 29 17:03:07 2019**

Name   Vis

■ /Input   ●

M5: 5.508656ns 1.8V   M7: 154.39554ns 1.8V   M9: 317.44593ns 1.8V

M1: 25.707837ns 1.8000005V

M2: 85.31.3605ns 1.8000004V

M3: 158.74567ns 656.37349nV

M6: 92.656308ns   M8: V 92.6563ns 0.0V

■ /output   ●

M4: 285.31.361ns 1.8000004V

time (ns)
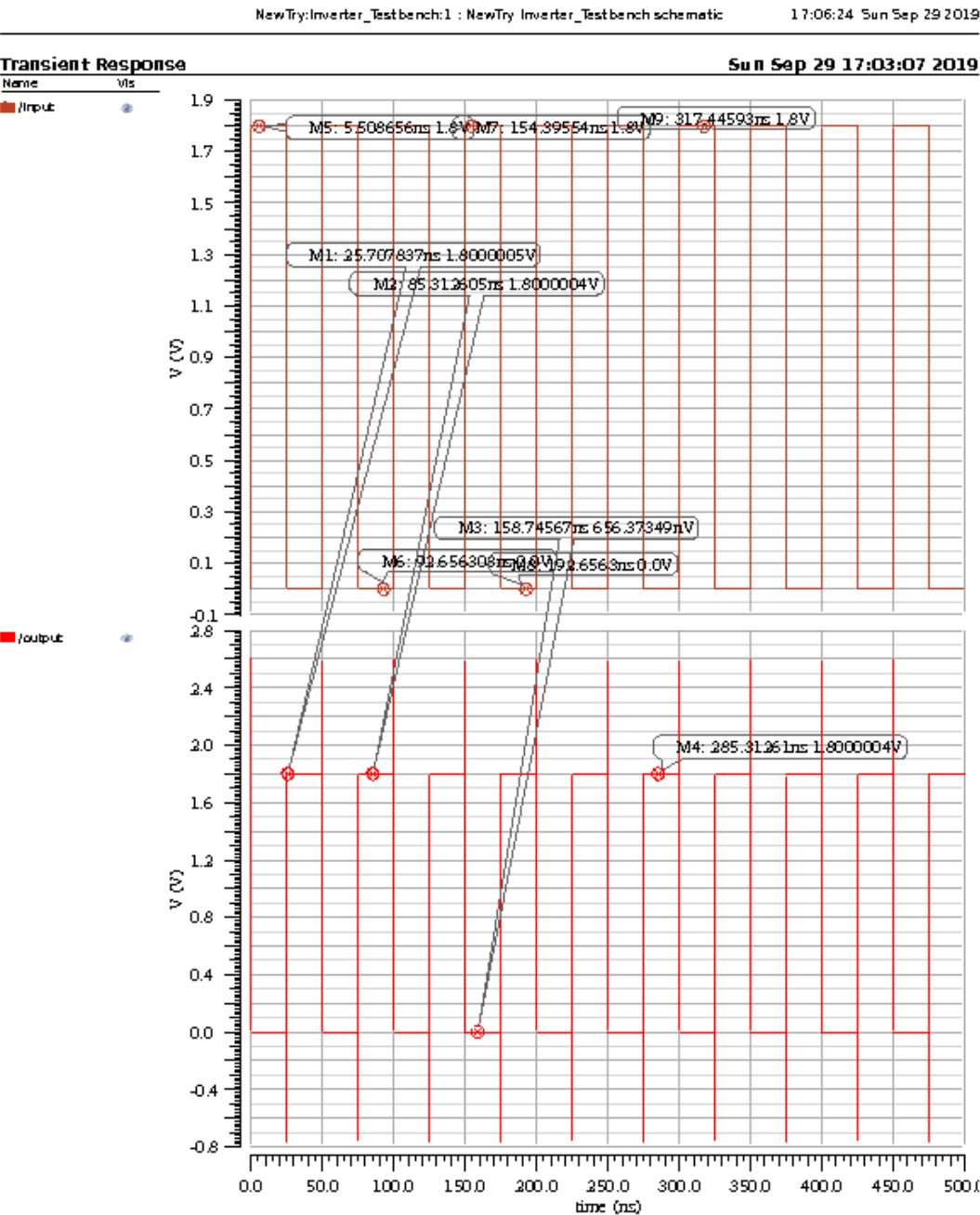
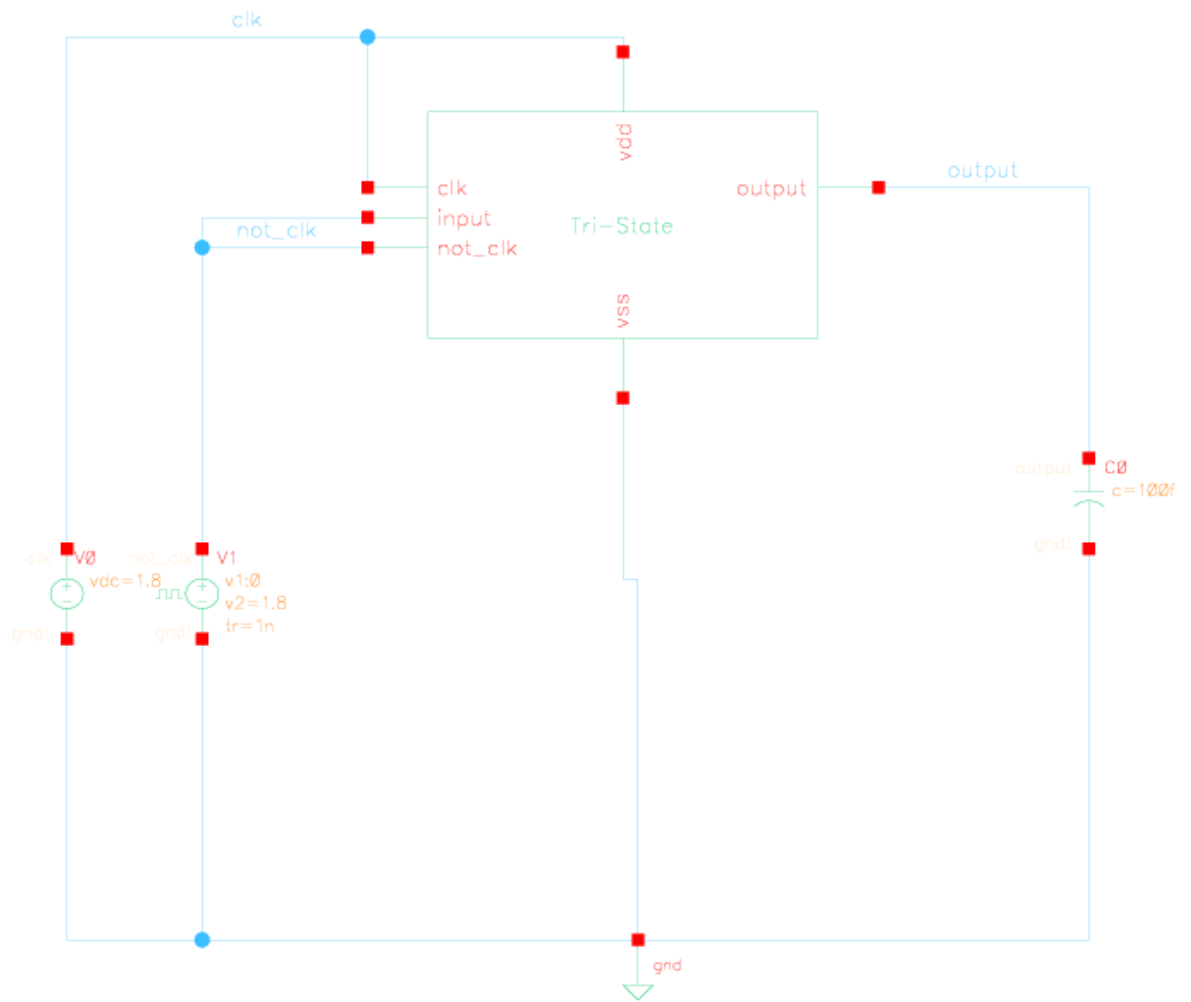Post Layout Simulation (Inverter):
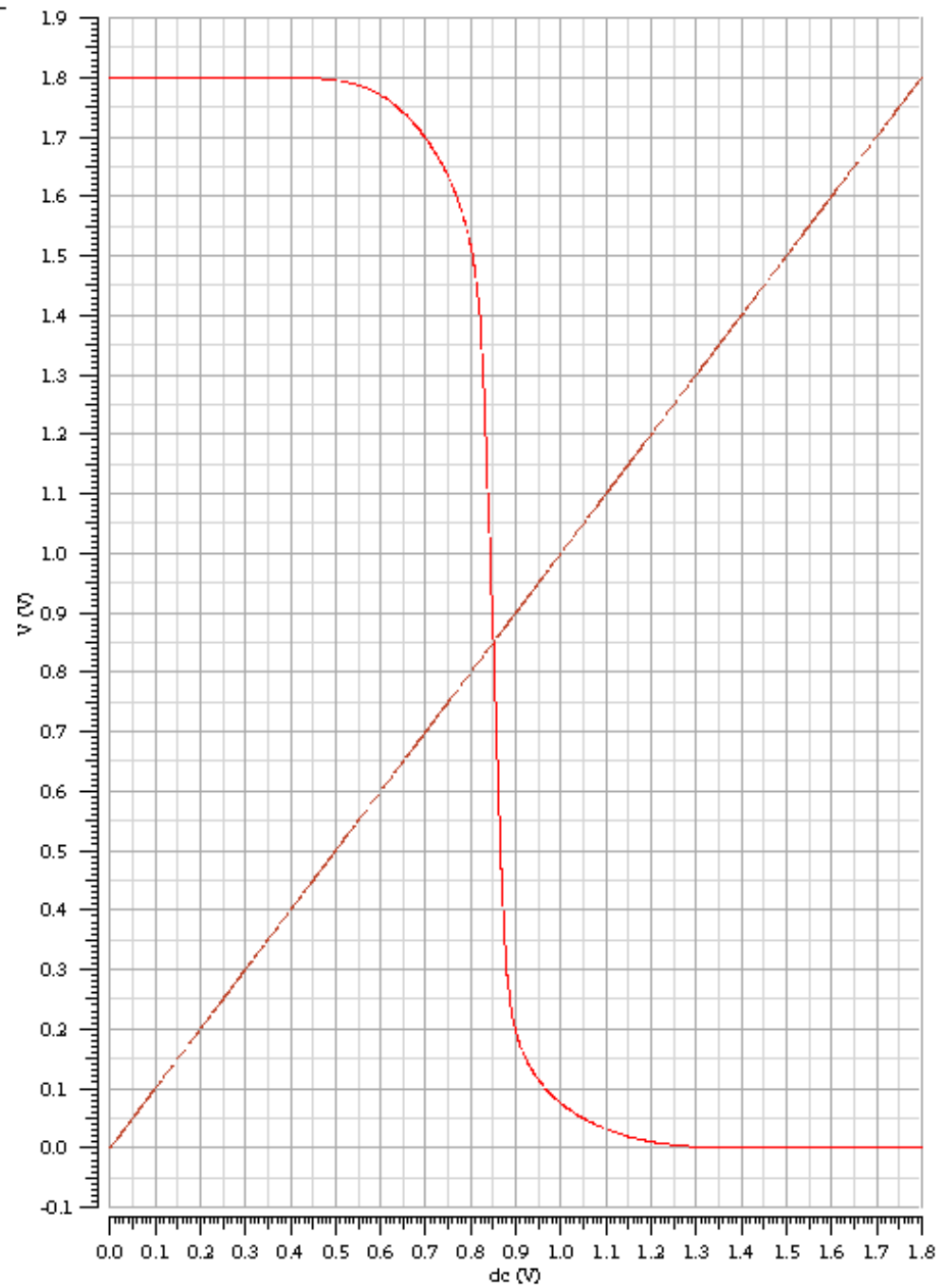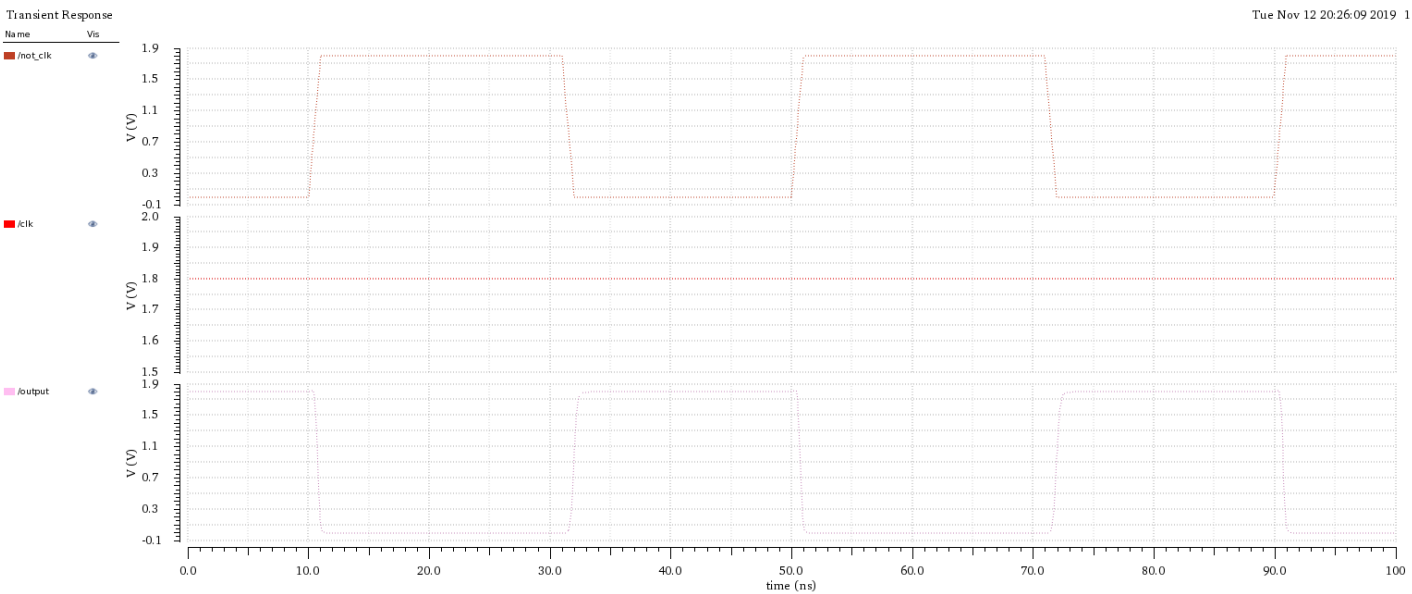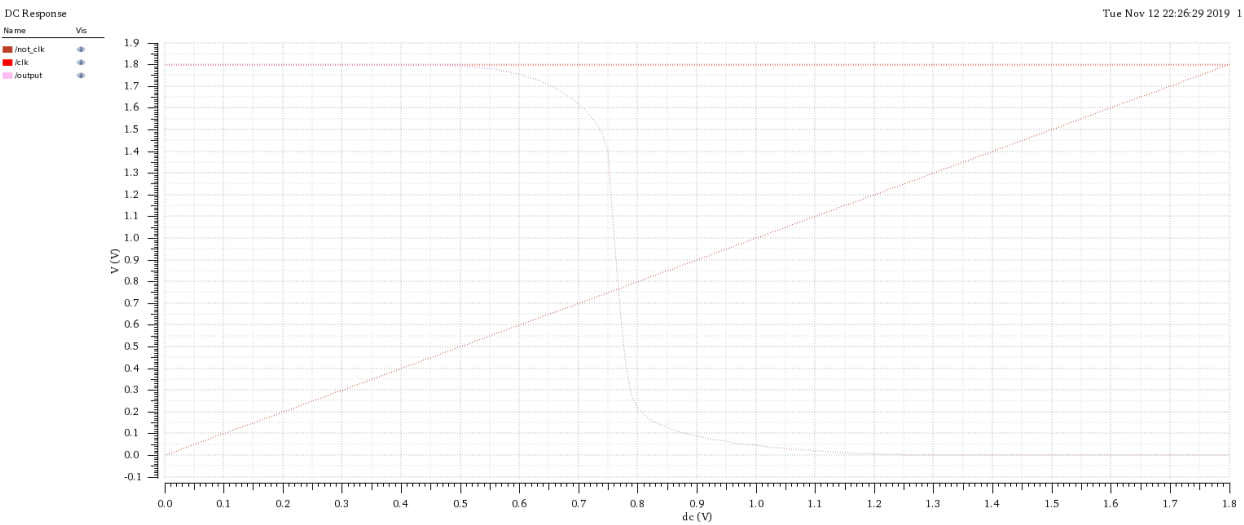
Tri State Inverter

Schematic (Tri State Inverter):
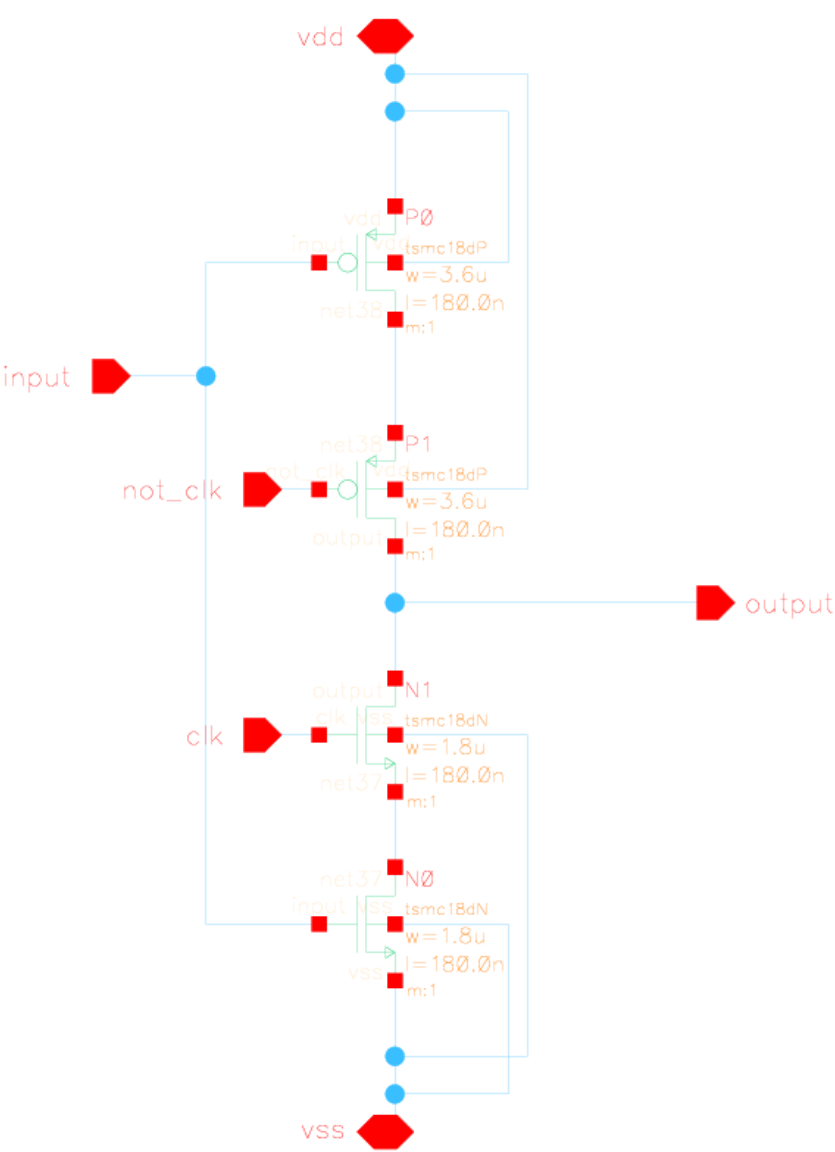
Test bench (Tri State Inverter):

Test bench Waveform (Tri State Inverter):

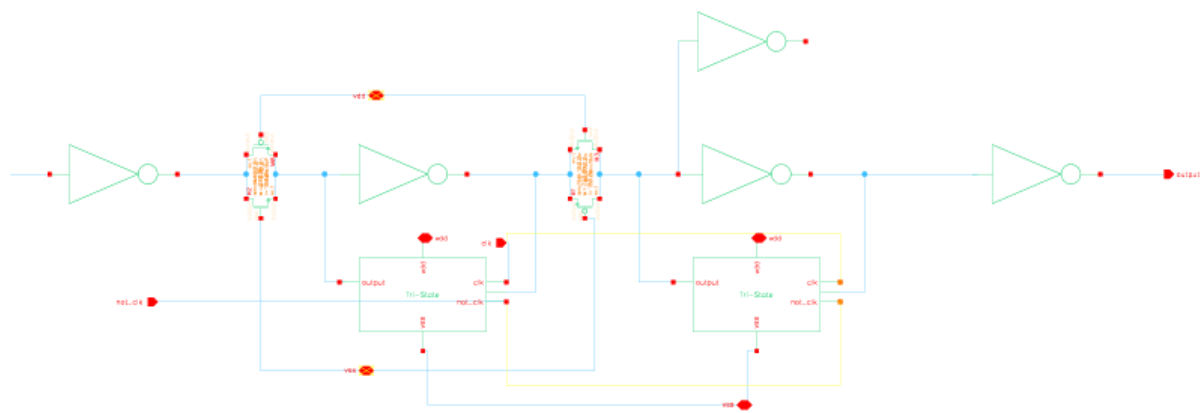## Post Simulation (Tri State Inverter):

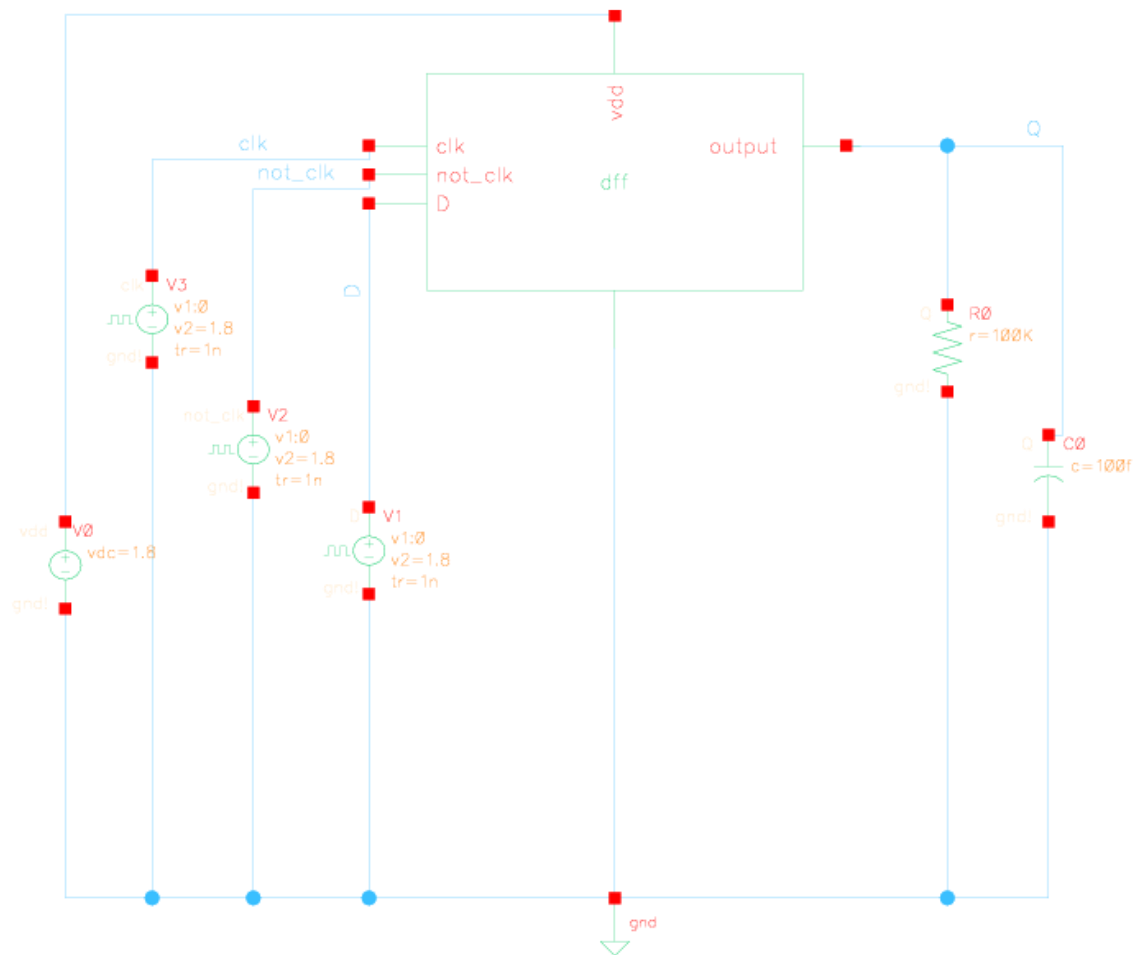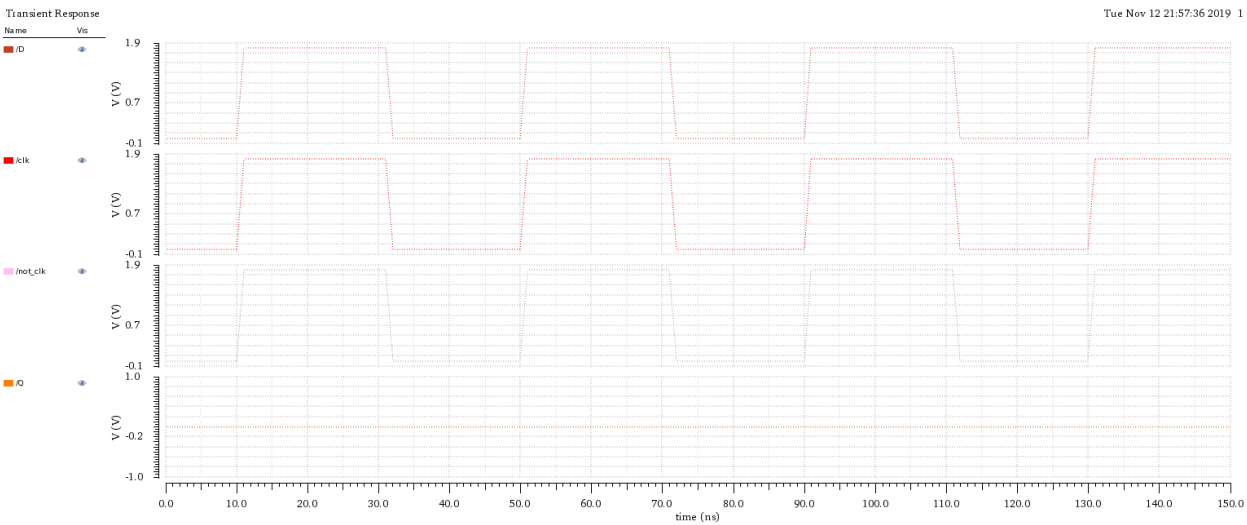| Name	Vis
/not_clk	●
/clk	●
/output	●

D Flip Flop

Schematic (D Flip Flop):

Test bench (D Flip Flop):

Test bench Waveform (D Flip Flop):

Post Simulation (D Flip Flop):

DC Response

Tue Nov 12 22:31:20 2019 1

Name	Vis
/D	
/clk	
/not_clk	
/Q	