CPE 151

Digital IC Design

Project No. 3 (Ring Oscillator)

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Contents

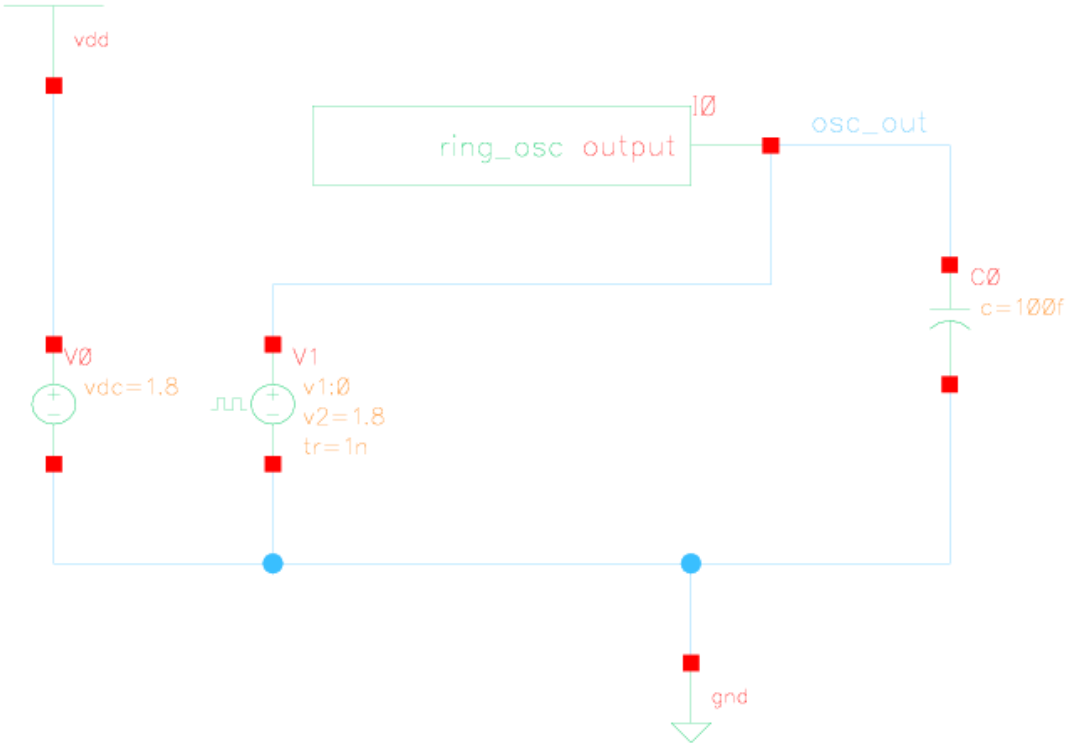
Ring Oscillator

(W/L)n = 5.4 /0.18

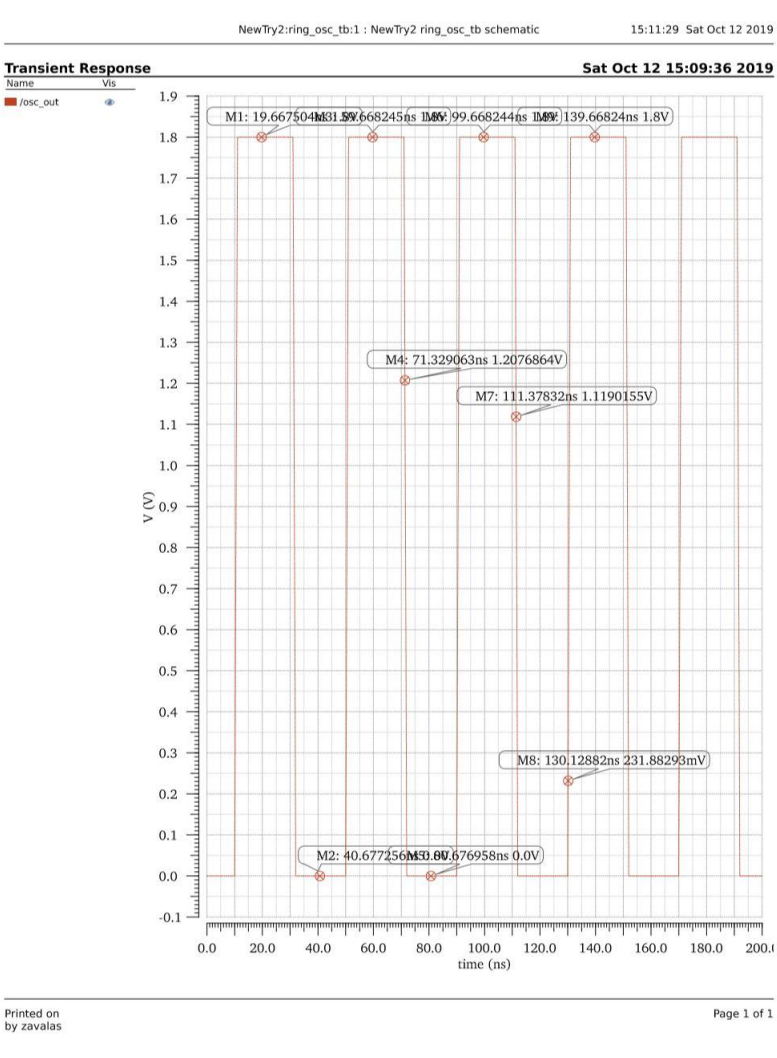
(W/L)p = 3.6/0.18

Schematic (Ring Oscillator):

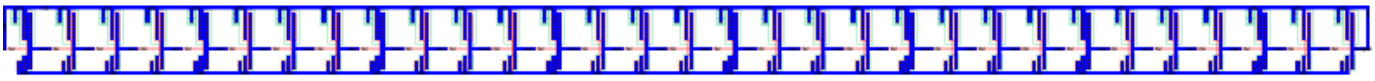
Test bench (Ring Oscillator):



Test bench Waveform (Ring Oscillator):

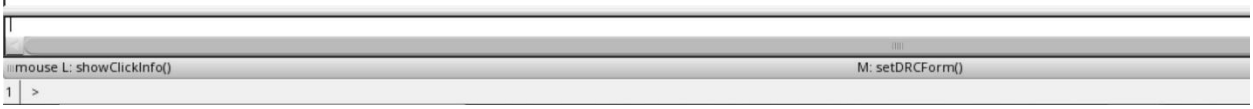


Layout (Ring Oscillator):



DRC (Ring Oscillator):

```
Validating hierarchy instantiation for:
library: NewTry2
cell:    RIngOscLayout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Sun Oct 13 21:22:23 2019
    completed ....Sun Oct 13 21:22:23 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "RIngOscLayout layout"   *********
   Total errors found: 0
```



LVS (RING OSCILLATOR):

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/zavalas/new_CPE_151/LVS -l -s -t /gaia/class/student/zavalas/new_CPE_151/LVS/layout /gaia/class/student/zavalas/new_CPE_151/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /gaia/class/student/zavalas/new_CPE_151/LVS/layout/netlist
       count
         6              nets
         0              terminals
         2              pmos
         2              nmos

    Net-list summary for /gaia/class/student/zavalas/new_CPE_151/LVS/schematic/netlist
       count
         6              nets
         5              terminals
         2              pmos
         2              nmos

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

                              layout  schematic
                                 instances
         un-matched              0       0
         rewired                 0       0
         size errors             0       0
         pruned                  0       0
         active                  4       4
         total                   4       4

                                   nets
         un-matched              0       0
         merged                  0       0
         pruned                  0       0
         active                  6       6
         total                   6       6

                                 terminals
         un-matched              0       0
         matched but
         different type          0       0
         total                   0       5


Probe files from /gaia/class/student/zavalas/new_CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:


termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /gaia/class/student/zavalas/new_CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```