CPE 151

Digital IC Design

Project No. 1 (Inverter)

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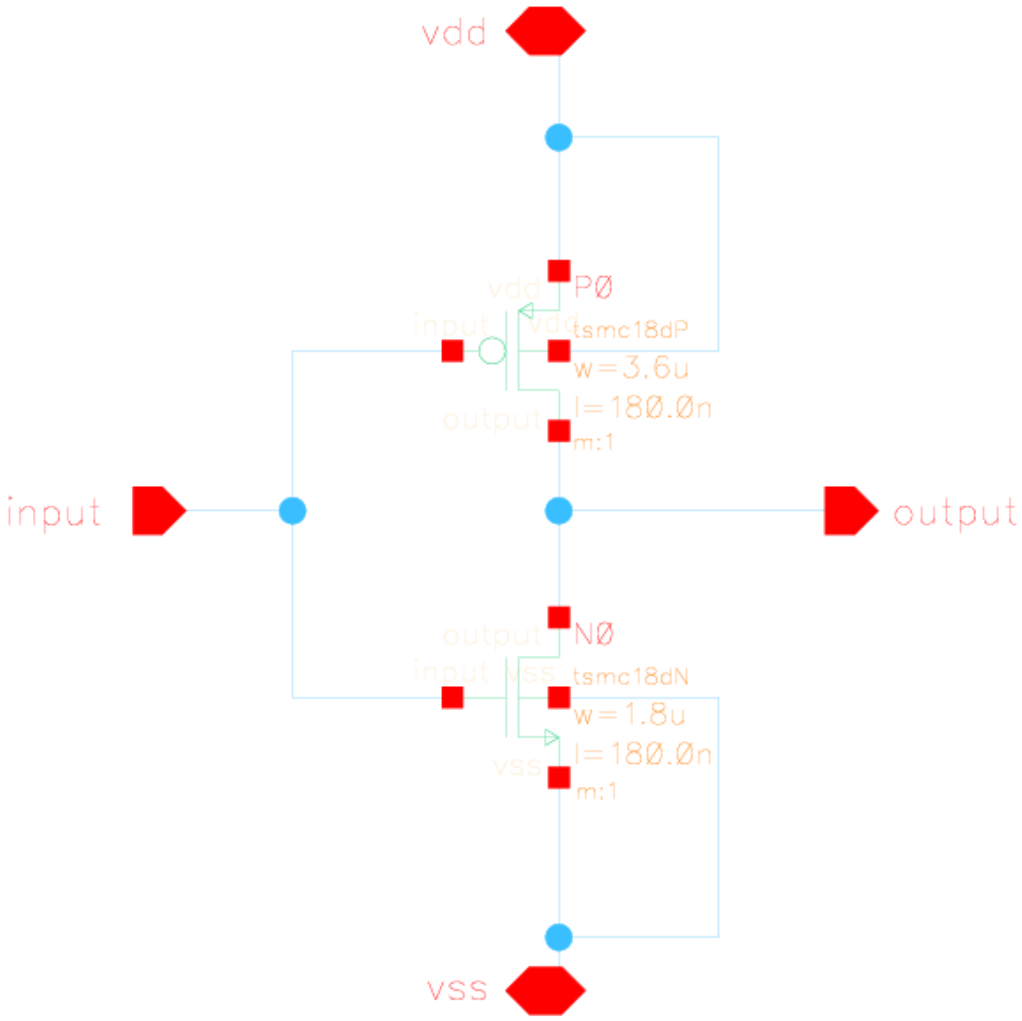
Contents

Inverter

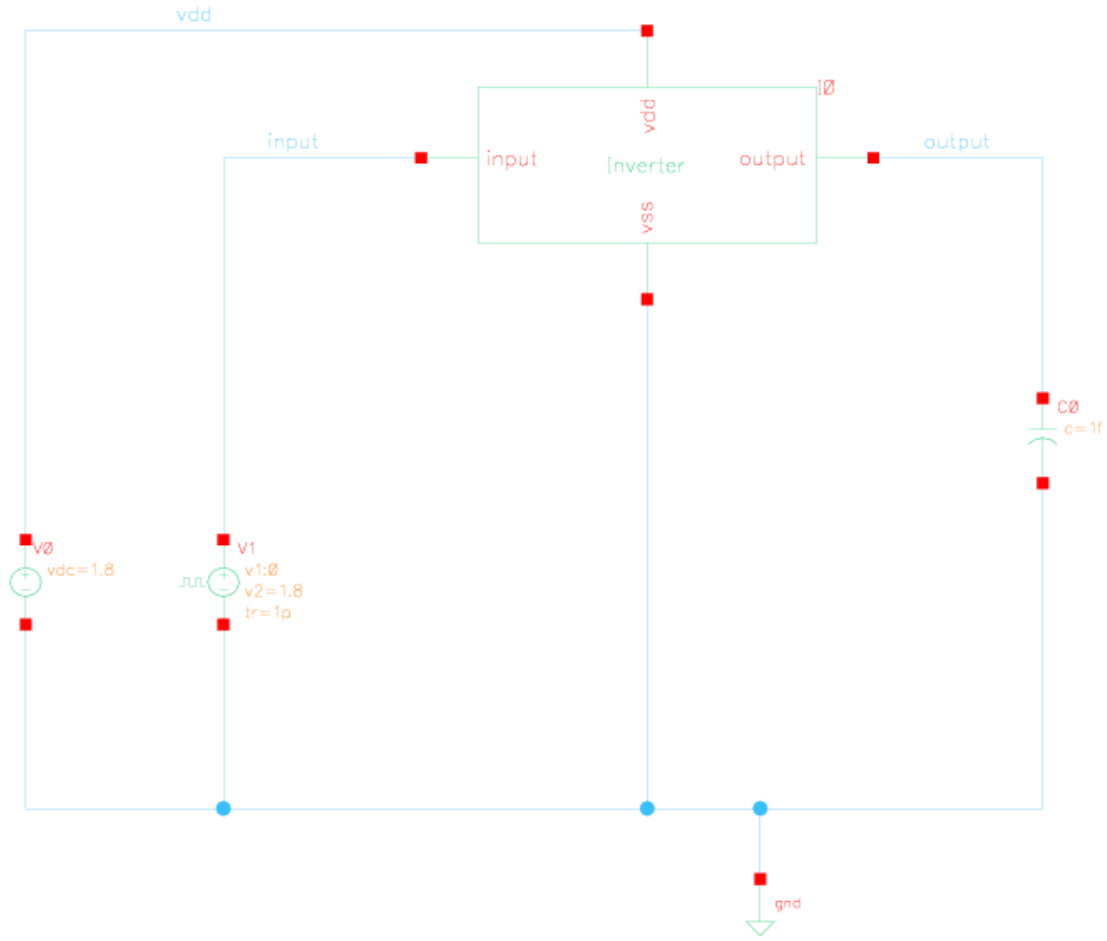
(W/L)n = 1.8 /0.18

(W/L)p = 3.6/0.18

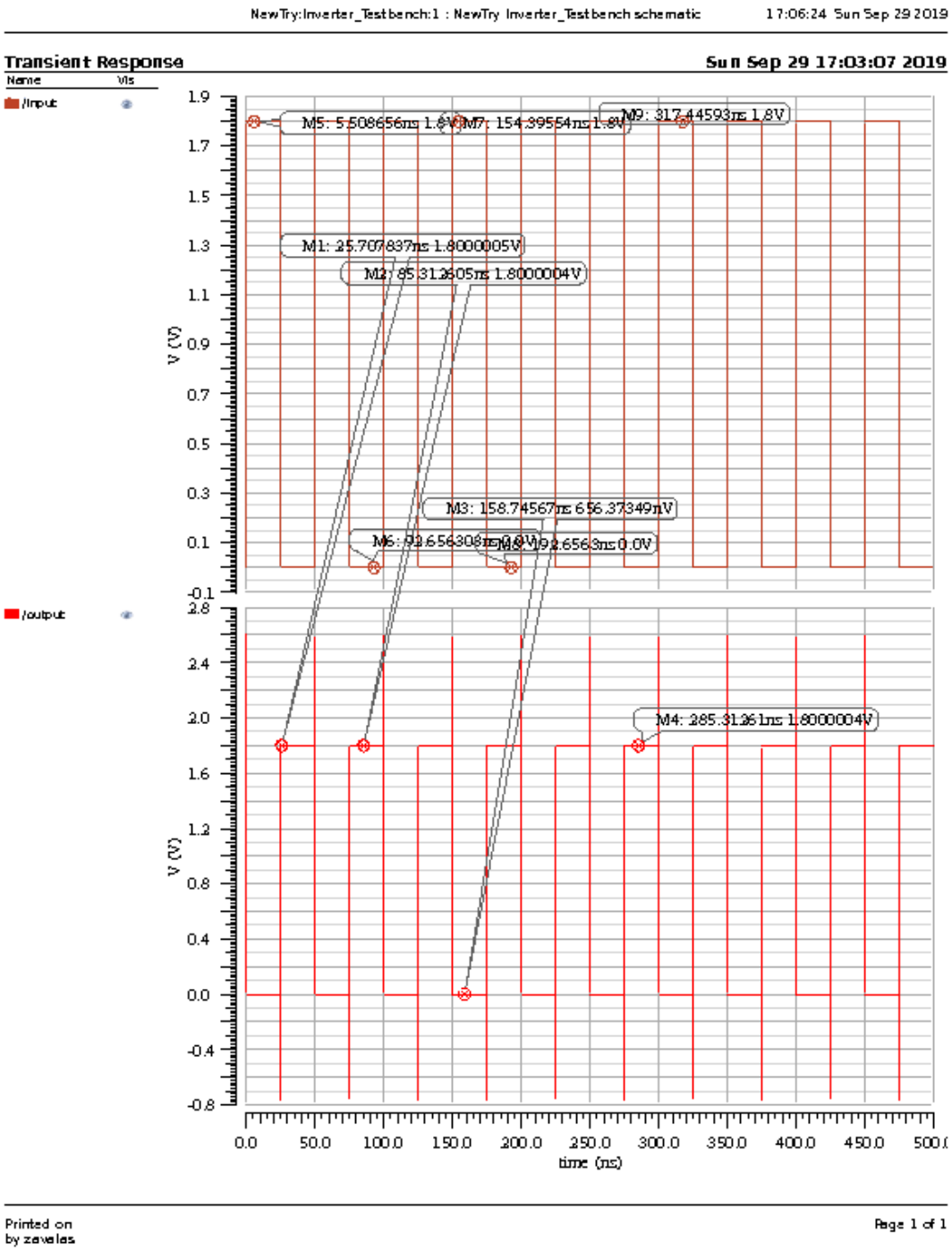
Schematic (Inverter):



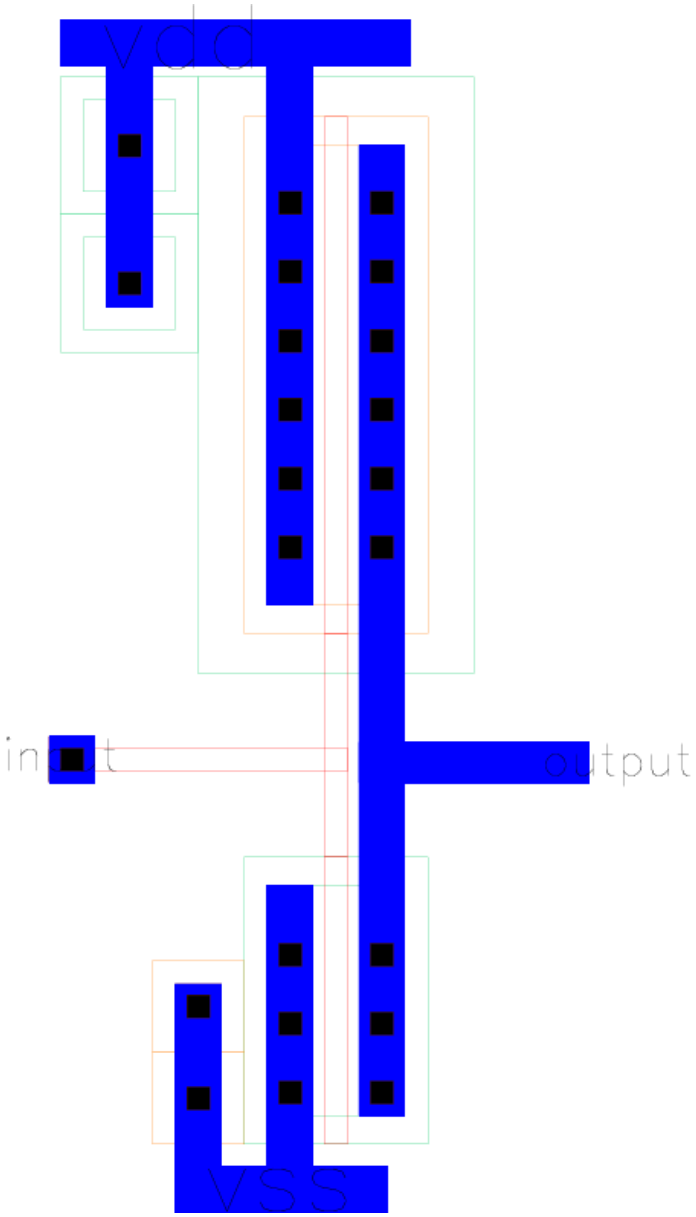
Test bench (Inverter):



Test bench Waveform (Inverter):



Layout (Inverter):



DRC (Inverter):

```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Sun Sep 29 17:20:26 2019
    completed ....Sun Sep 29 17:20:26 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "Inverter_Layout layout"   *********
   Total errors found: 0
```

LVS (Inverter):

```
Begin netlist:    Sep 29 17:25:36 2019
        view name list  = ("auLvs" "extracted" "schematic")
        stop name list  = ("auLvs")
        library name    = "NewTry"
        cell name       = "Inverter_Layout"
        view name       = "extracted"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:    Sep 29 17:25:36 2019

Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 0
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        4 nodes merged into 4 nodes


Begin netlist:    Sep 29 17:25:36 2019
        view name list  = ("auLvs" "schematic")
        stop name list  = ("auLvs")
        library name    = "NewTry"
        cell name       = "Inverter"
        view name       = "schematic"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
*WARNING* (icLic-203) Failed to check out license Virtuoso_Layout_Suite_L ("Layout L") to run Layout L because of status code -18.
Attempting to check out the next available license Virtuoso_Layout_Suite_XL ("Layout XL") per license checkout order L, XL, GXL.
*WARNING* (icLic-203) Failed to check out license Virtuoso_Layout_Suite_XL ("Layout XL") to run Layout L because of status code -18.
Attempting to check out the next available license Virtuoso_Layout_Suite_GXL ("Layout GXL") per license checkout order L, XL, GXL.
*INFO* (icLic-302) License Virtuoso_Layout_Suite_GXL ("Layout GXL") was used to run Layout L.
End netlist:    Sep 29 17:25:37 2019


Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 0
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        4 nodes merged into 4 nodes

Running netlist comparison program:  LVS
Begin comparison:    Sep 29 17:25:37 2019
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

The net-lists match.

                            layout  schematic
                              instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4


                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   4       4
End comparison:      Sep 29 17:25:37 2019
*WARNING* (icLic-203) Failed to check out license Virtuoso_Layout_Suite_L ("Layout L") to run Layout L because of status code -18.
Attempting to check out the next available license Virtuoso_Layout_Suite_XL ("Layout XL") per license checkout order L, XL, GXL.
*WARNING* (icLic-203) Failed to check out license Virtuoso_Layout_Suite_XL ("Layout XL") to run Layout L because of status code -18.
Attempting to check out the next available license Virtuoso_Layout_Suite_GXL ("Layout GXL") per license checkout order L, XL, GXL.
*INFO* (icLic-302) License Virtuoso_Layout_Suite_GXL ("Layout GXL") was used to run Layout L.


Comparison program completed successfully.
```

Post Layout Simulation (Inverter):