



SACRAMENTO STATE

CPE 151/EEE 234
Digital IC Design

Project No. 2

Student Name:
Email ID:
Date of Submission:

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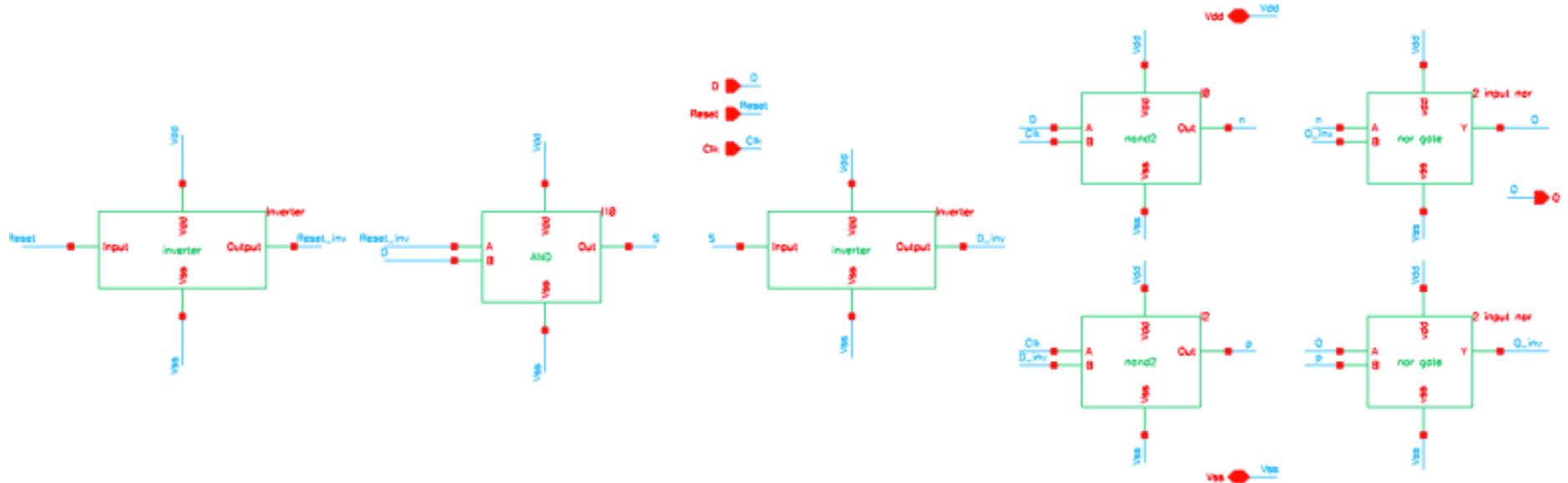
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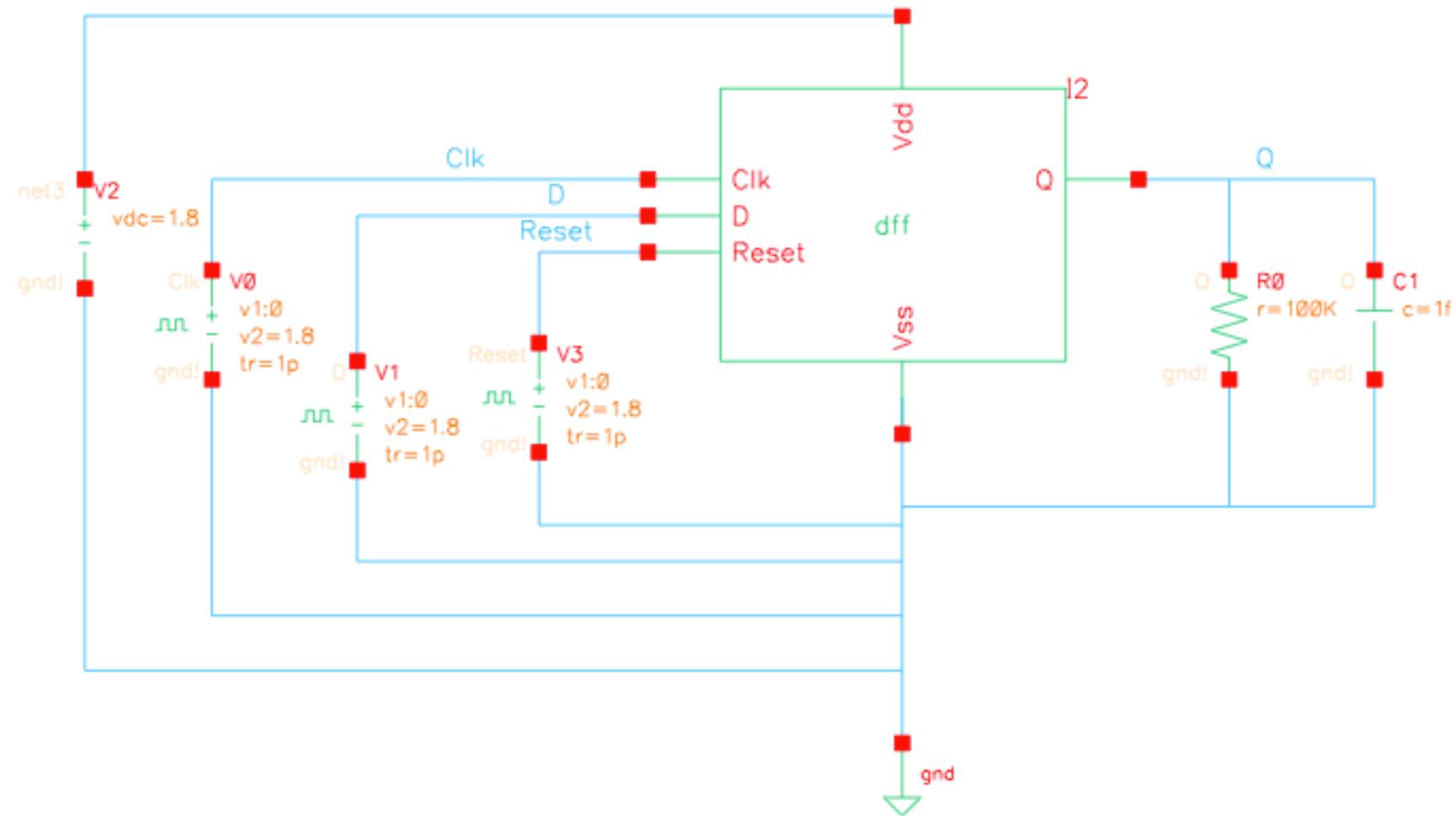
D-Type Flip Flop

Positive Clock Edge,
Synchronous Reset

D-Type Flip Flop Schematic



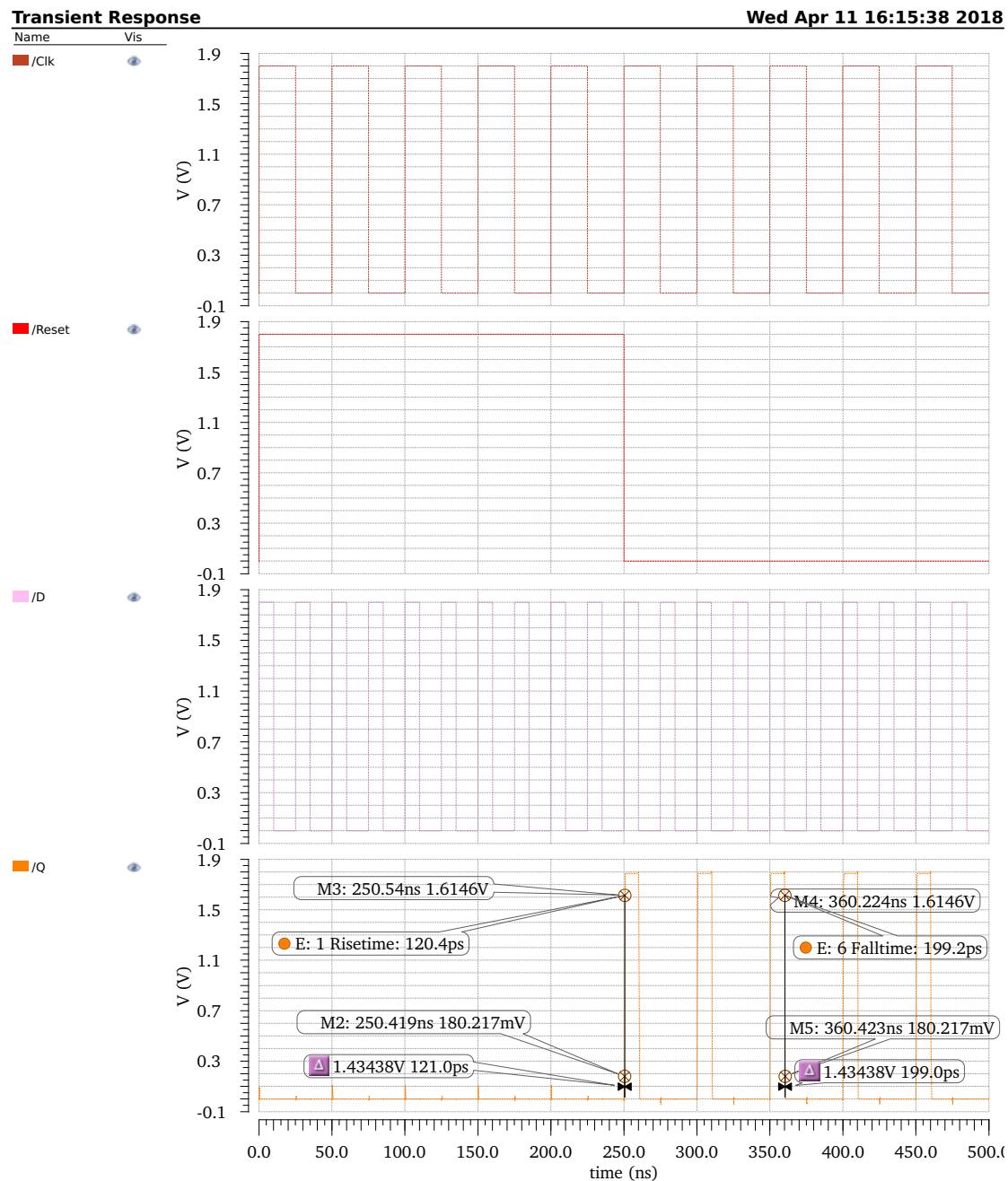
D-Type Flip Flop Testbench



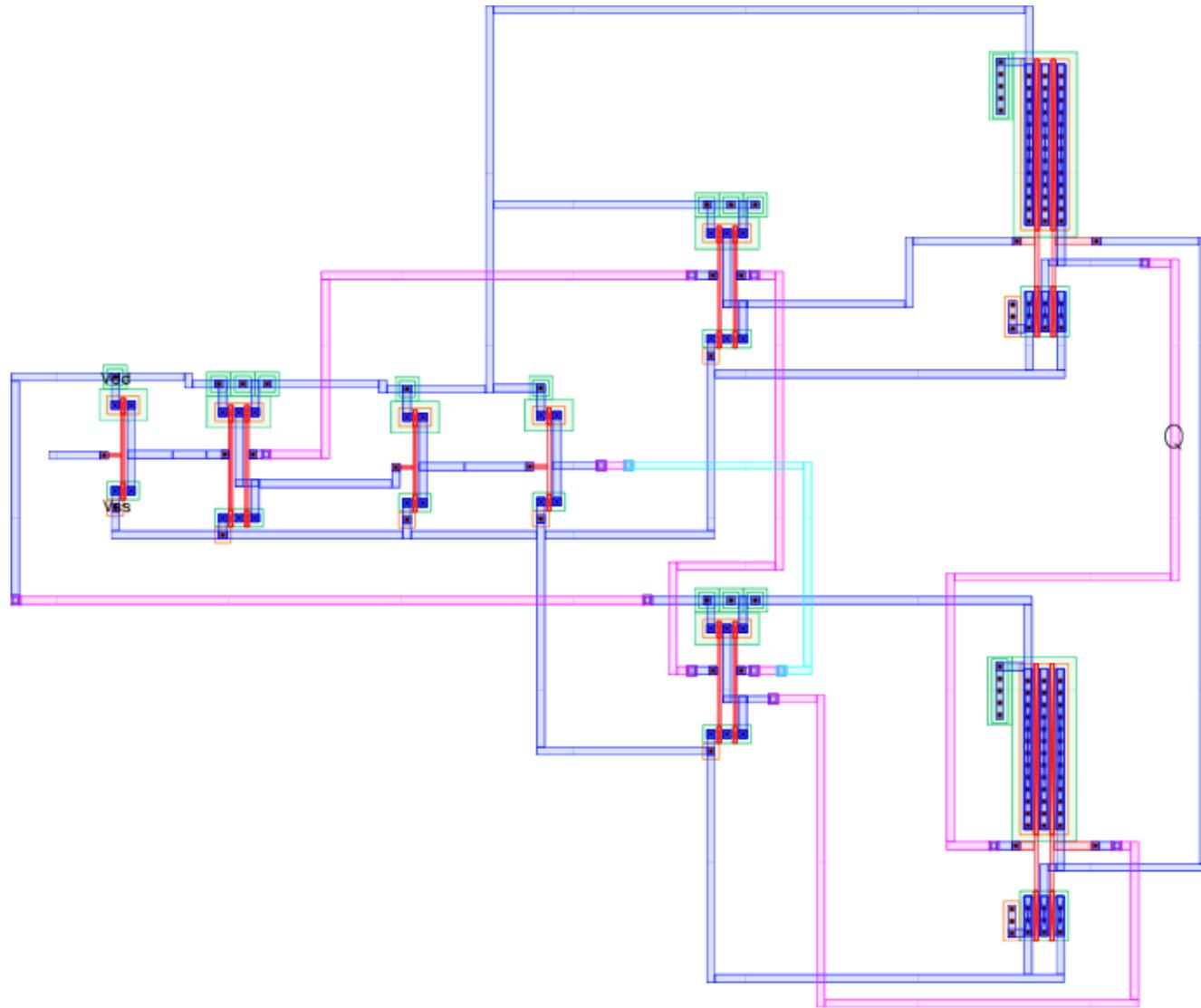
D-Type Flip Flop Testbench Waveform

project2:dff_tb:1 : project2 dff_tb schematic

16:22:25 Wed Apr 11 2018



D-Type Flip Flop Layout



D-Type Flip Flop DRC

```
Validating hierarchy instantiation for:  
library: project2  
cell:    dff_layout  
view:    layout  
Rules come from library NCSU_TechLib_tsmc02d.  
Rules path is divaDRC.rul.  
Inclusion limit is set to 1000.  
Running layout DRC analysis  
Flat mode  
Full checking.  
DRC started.....Fri May  4 19:44:51 2018  
completed ....Fri May  4 19:44:51 2018  
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "dff_layout layout" *****  
Total errors found: 0
```

D-Type Flip Flop LVS

```
@(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout
/gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count

18	nets
0	terminals
13	pmos
13	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count

18	nets
6	terminals
13	pmos
13	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26

	nets	
un-matched	0	0

merged	0	0
pruned	0	0
active	18	18
total	18	18

terminals		
un-matched	0	0
matched but		
different type	0	0
total	0	6

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

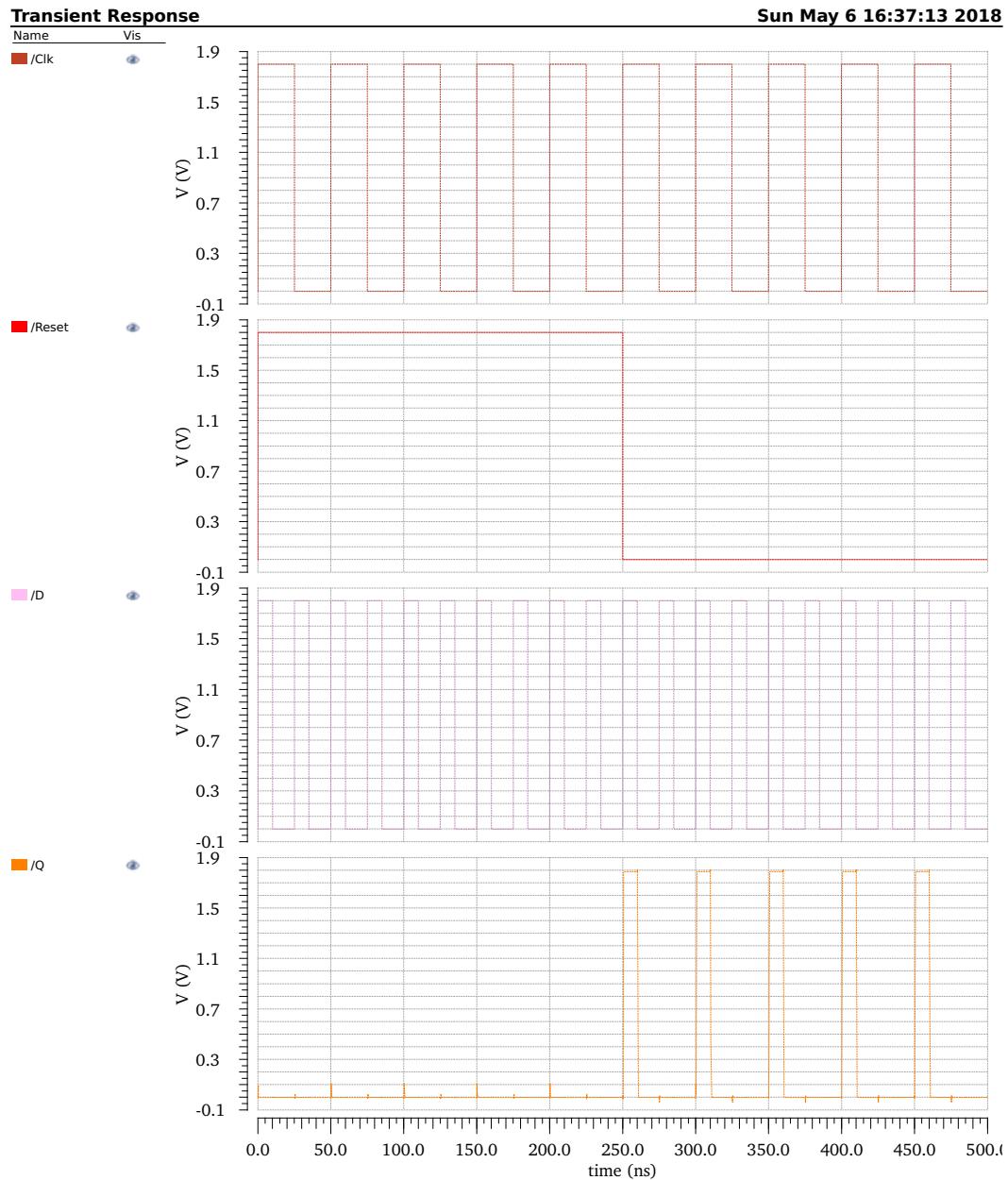
prunedev.out:

audit.out:

D-Type Flip Flop Post-Layout

project2:dff_tb:1 : project2 dff_tb schematic

16:37:32 Sun May 6 2018



DC Response**Sun May 6 16:37:13 2018**

Name Vis

/Clk

@

/Reset

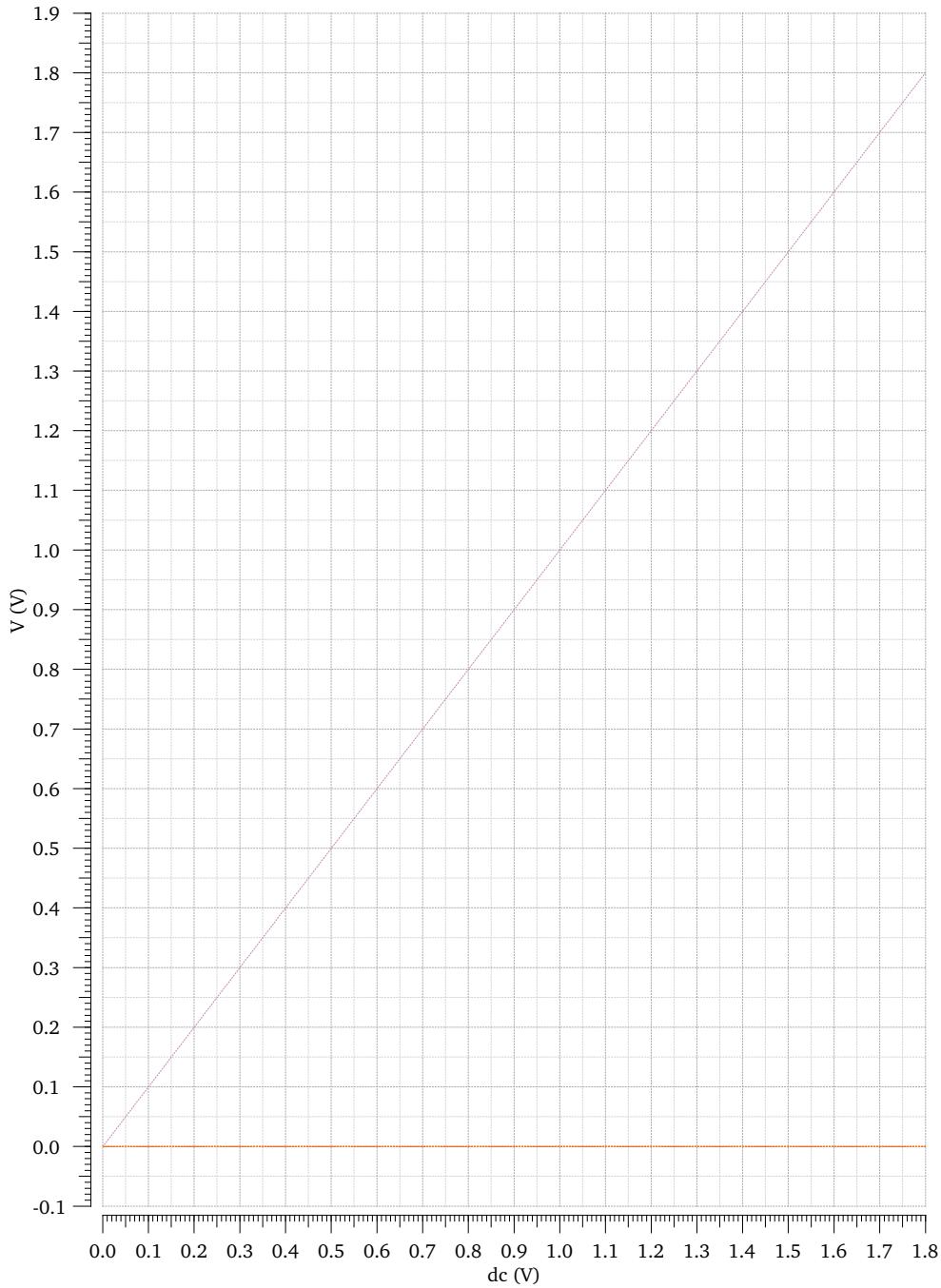
@

/D

@

/Q

@

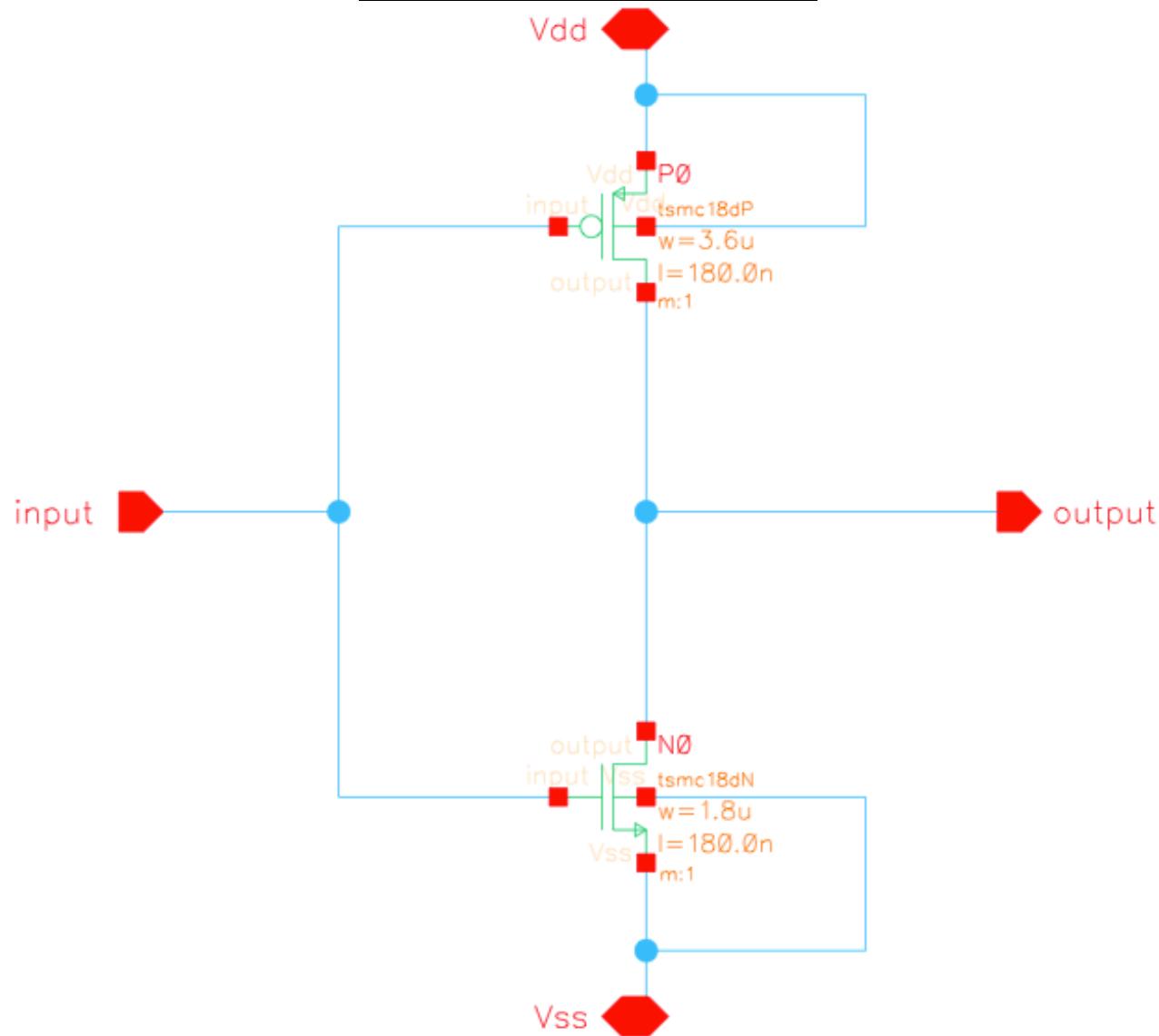


Inverter

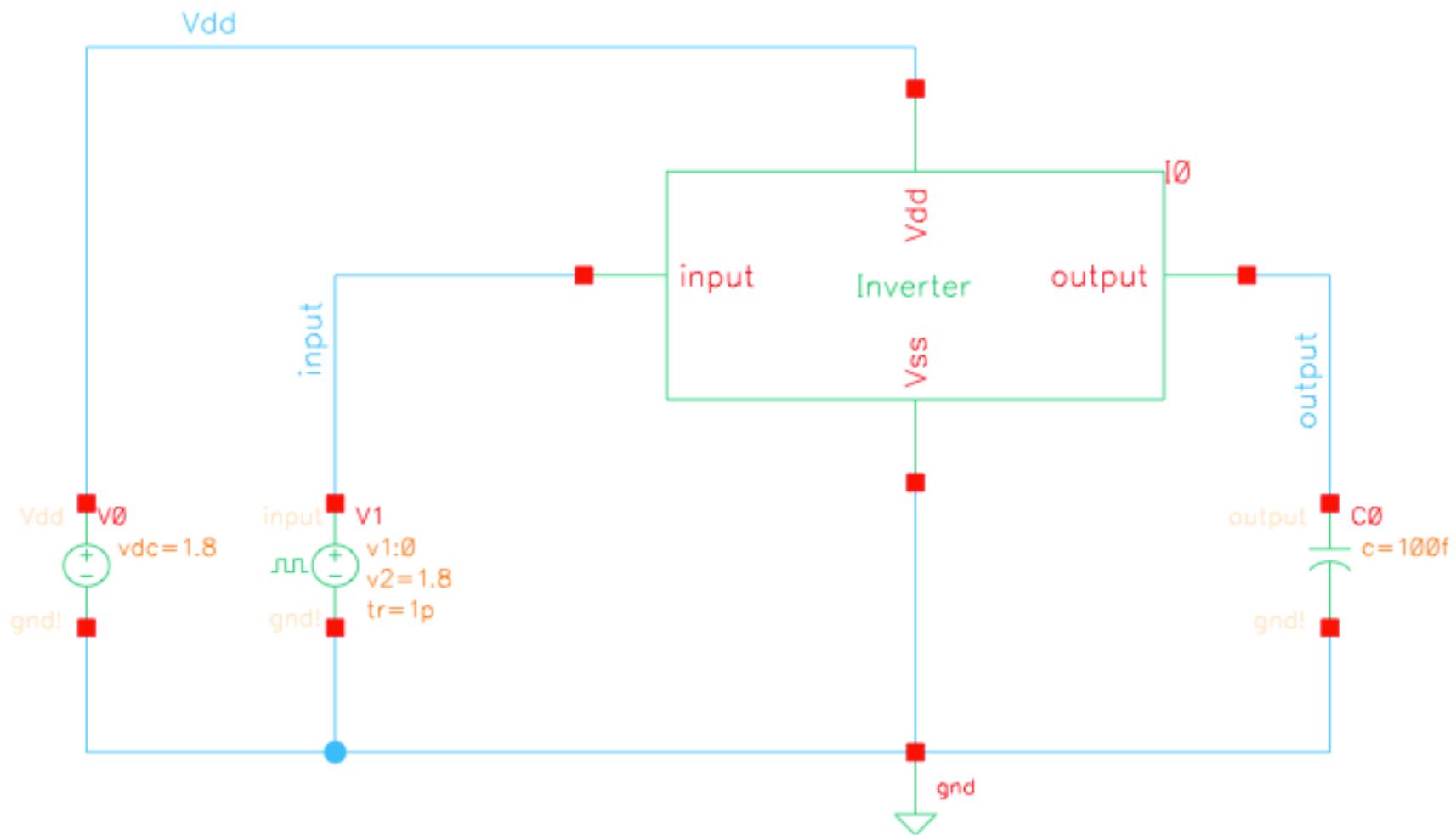
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 3.6/0.18$$

Inverter Schematic



Inverter Testbench



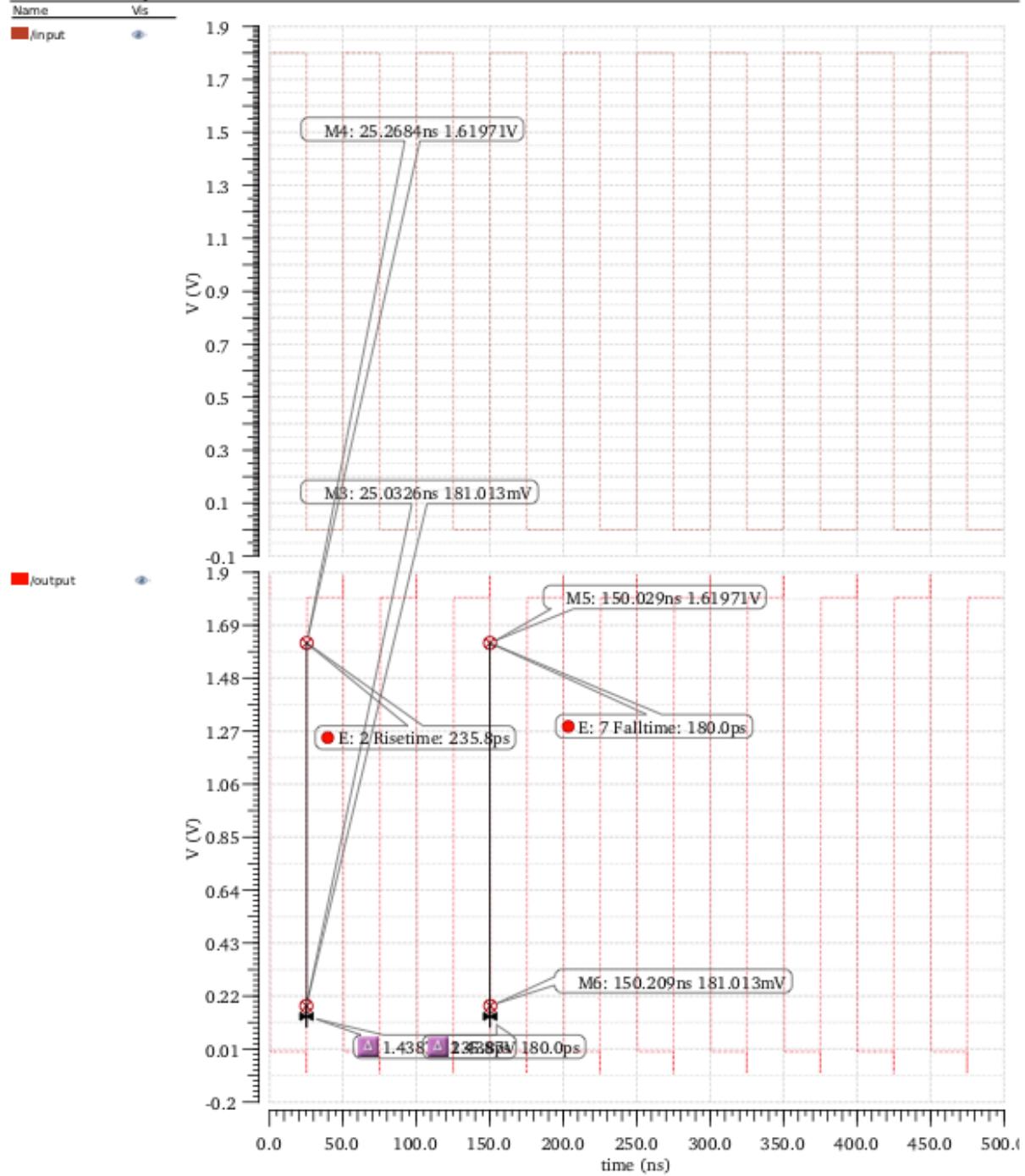
Inverter Testbench Waveform

Project1:Inverter_testbench:1 : Project1_Inverter_testbench schematic

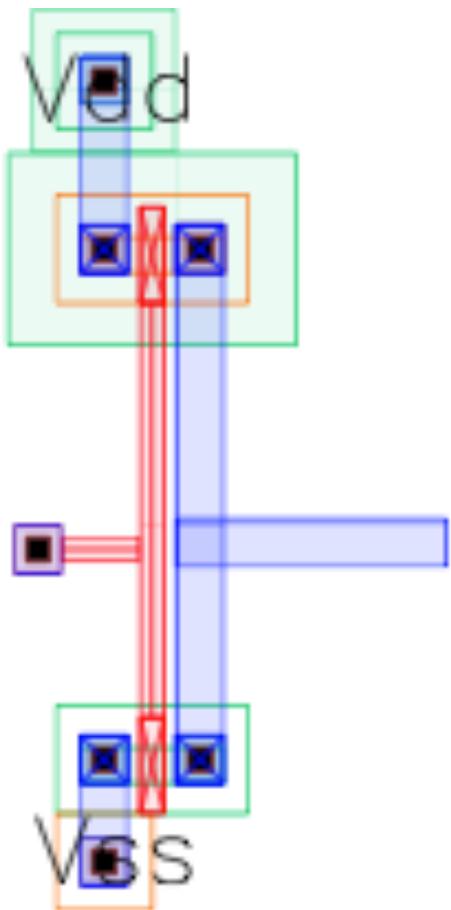
19:20:40 Wed Feb 28 2018

Transient Response

Wed Feb 28 19:14:42 2018



Inverter Layout



Inverter DRC

```
DRC started at Fri May  4 17:02:54 2018

Validating hierarchy instantiation for:
library: project2
cell:    inverter_layout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.

DRC started.....Fri May  4 17:02:54 2018
completed ....Fri May  4 17:02:54 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "inverter_layout layout" *****
Total errors found: 0
```

Inverter LVS

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout
/gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count

4	nets
0	terminals
1	pmos
1	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count

4	nets
4	terminals
1	pmos
1	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

	nets	
un-matched	0	0
merged	0	0

```
pruned      0  0
active      4  4
total       4  4
```

```
          terminals
un-matched   0  0
matched but
different type 0  0
total        0  4
```

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

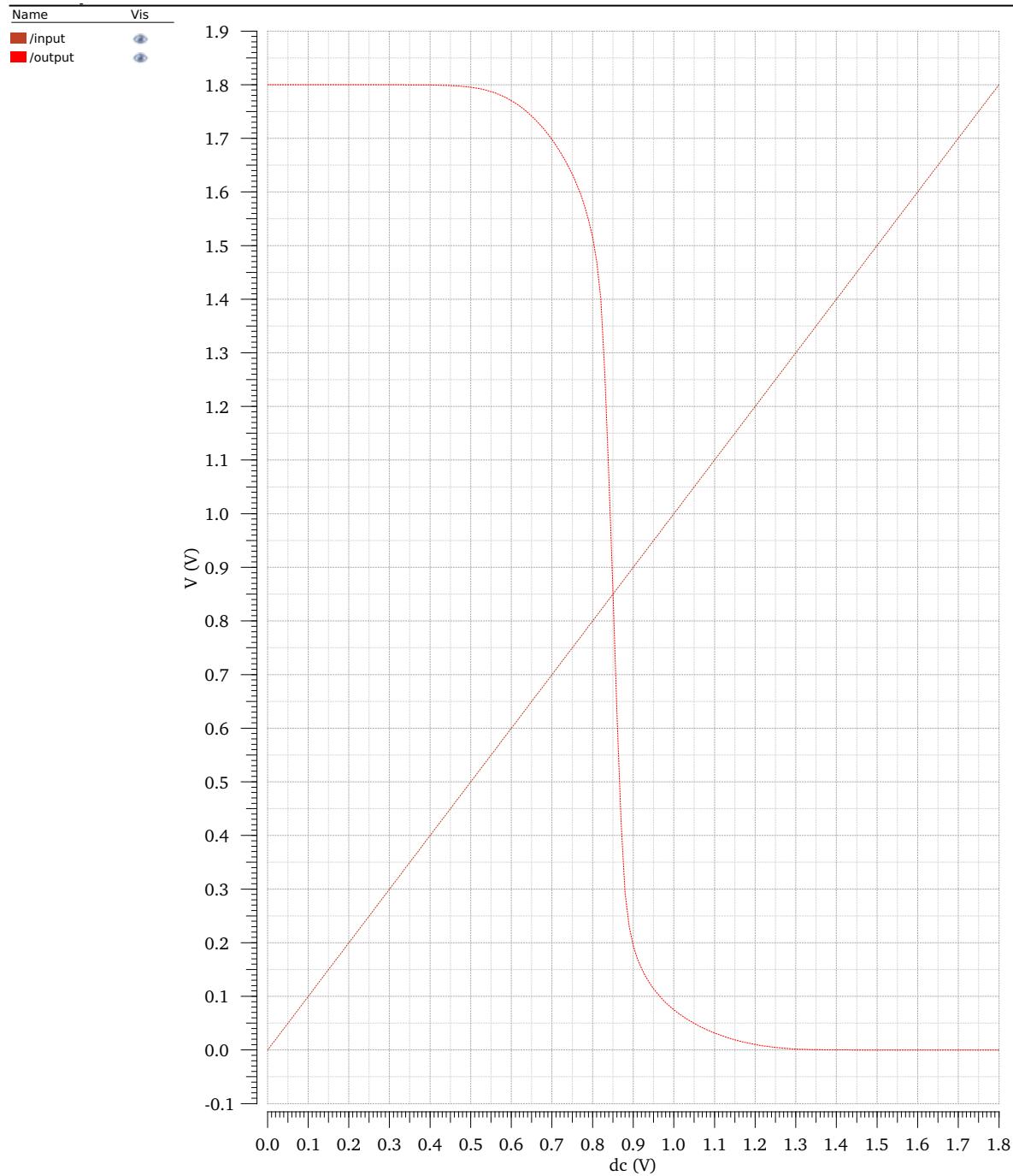
termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Inverter Post-Layout

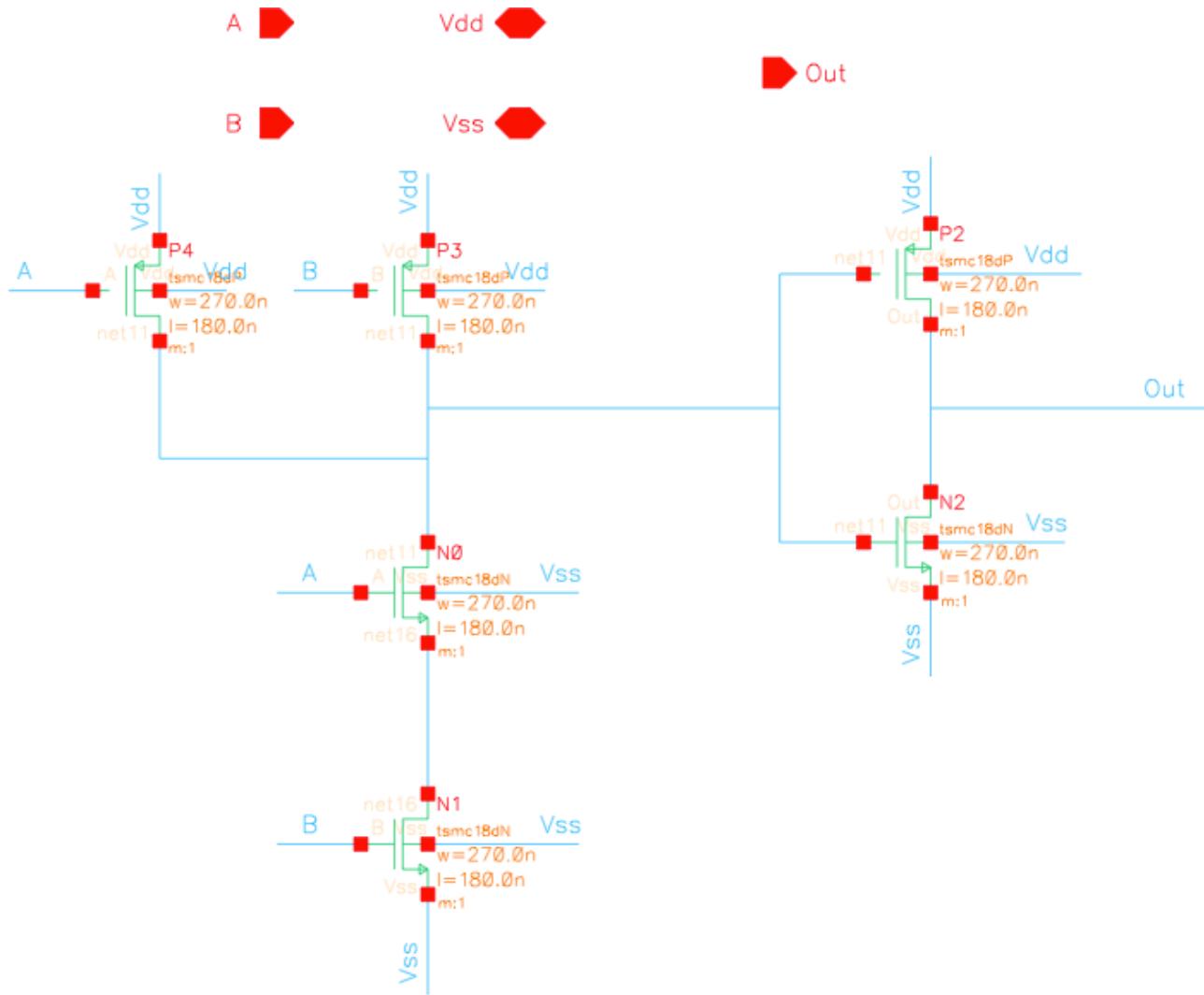


2-Input AND Gate

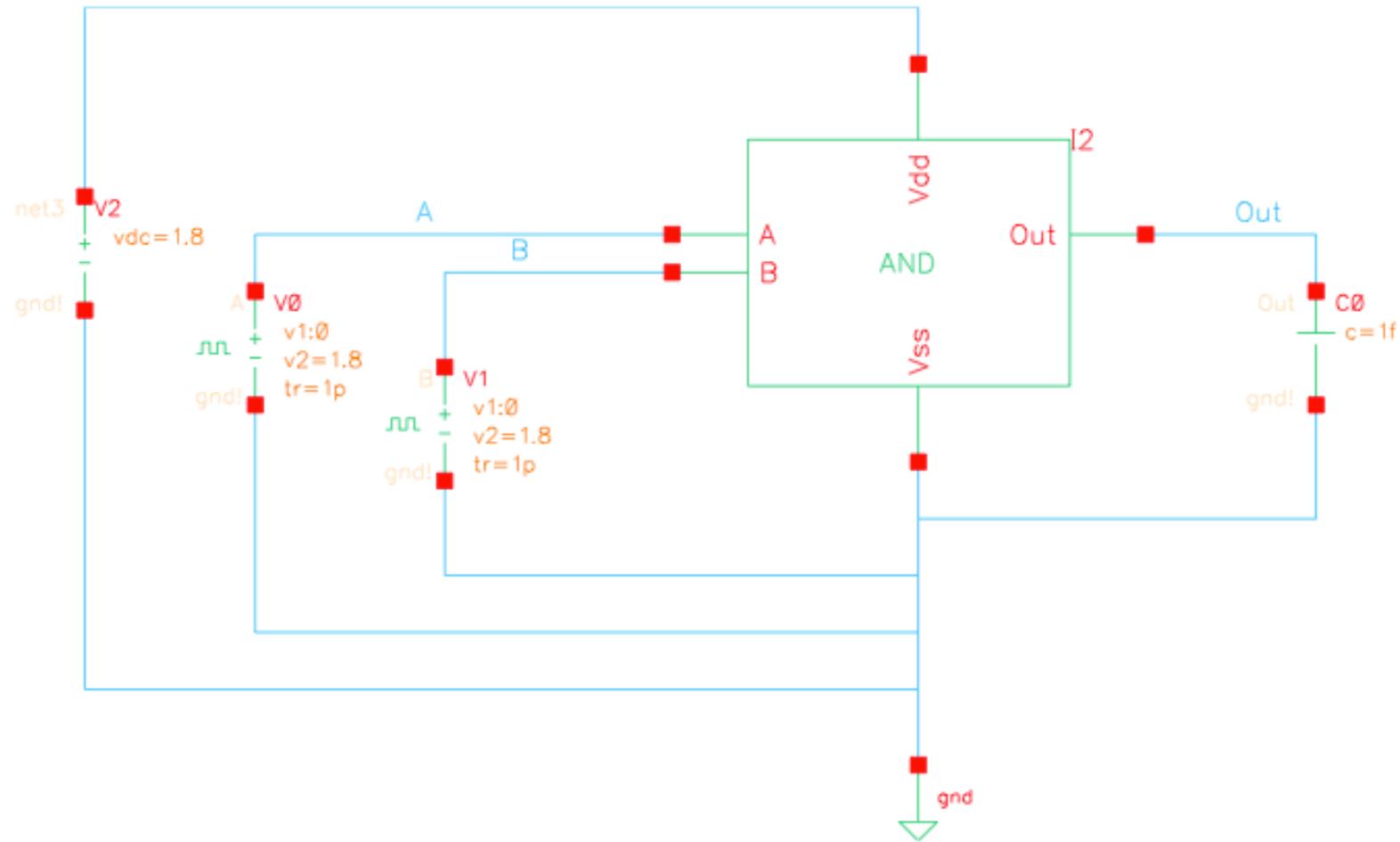
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

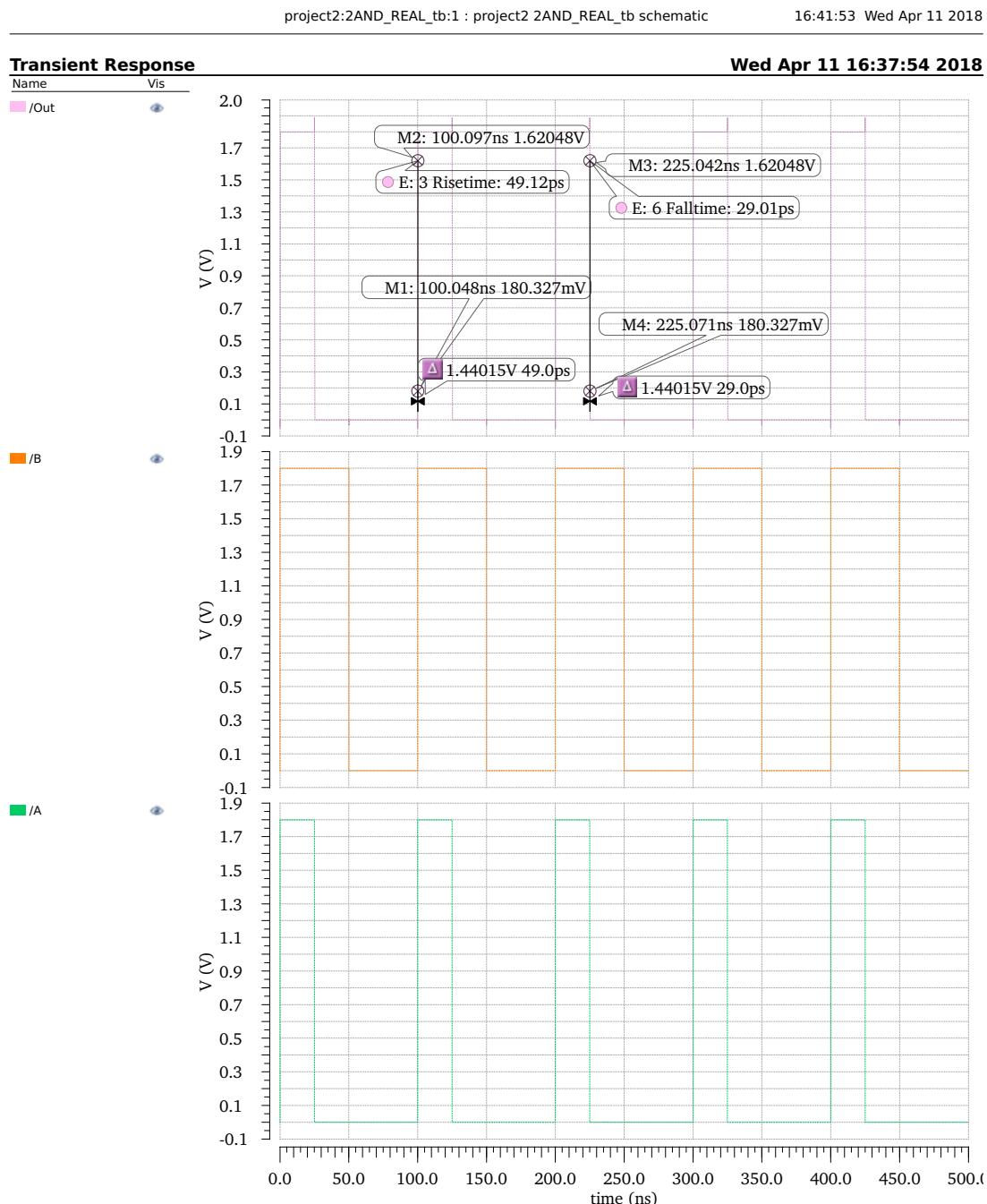
2-Input AND Gate Schematic



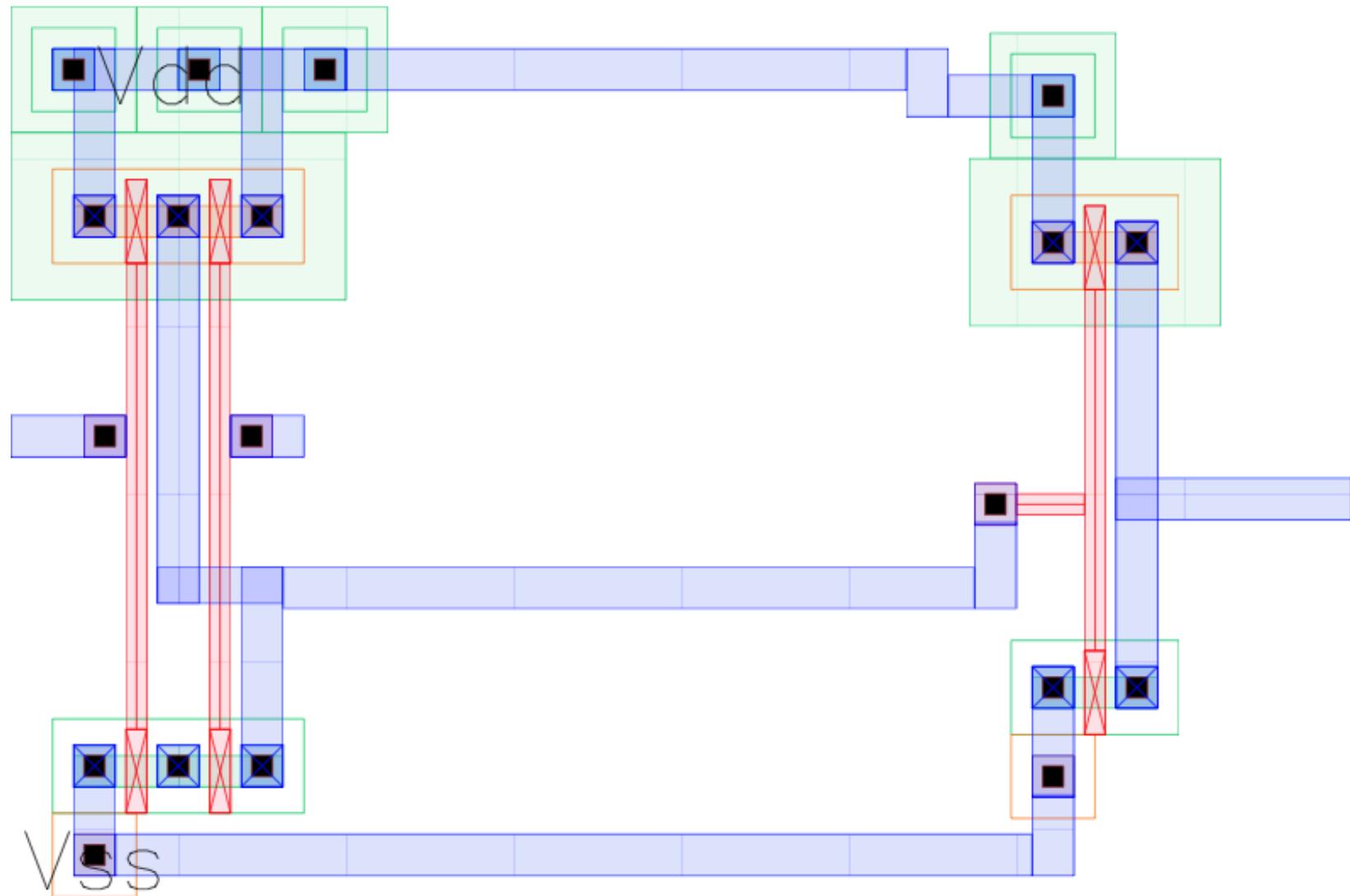
2-Input AND Gate Testbench



2-Input AND Gate Testbench Waveform



2-Input AND Gate Layout



2-Input AND Gate DRC

```
Validating hierarchy instantiation for:  
library: project2  
cell:    2AND_REAL_LAYOUT  
view:    layout  
Rules come from library NCSU_TechLib_tsmc02d.  
Rules path is divaDRC.rul.  
Inclusion limit is set to 1000.  
Running layout DRC analysis  
Flat mode  
Full checking.  
DRC started.....Fri May  4 17:43:36 2018  
completed ....Fri May  4 17:43:36 2018  
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "2AND_REAL_LAYOUT layout" *****  
Total errors found: 0
```

2-Input AND Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count

7	nets
0	terminals
3	pmos
3	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count

7	nets
5	terminals
3	pmos
3	nmos

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7

total	7	7
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

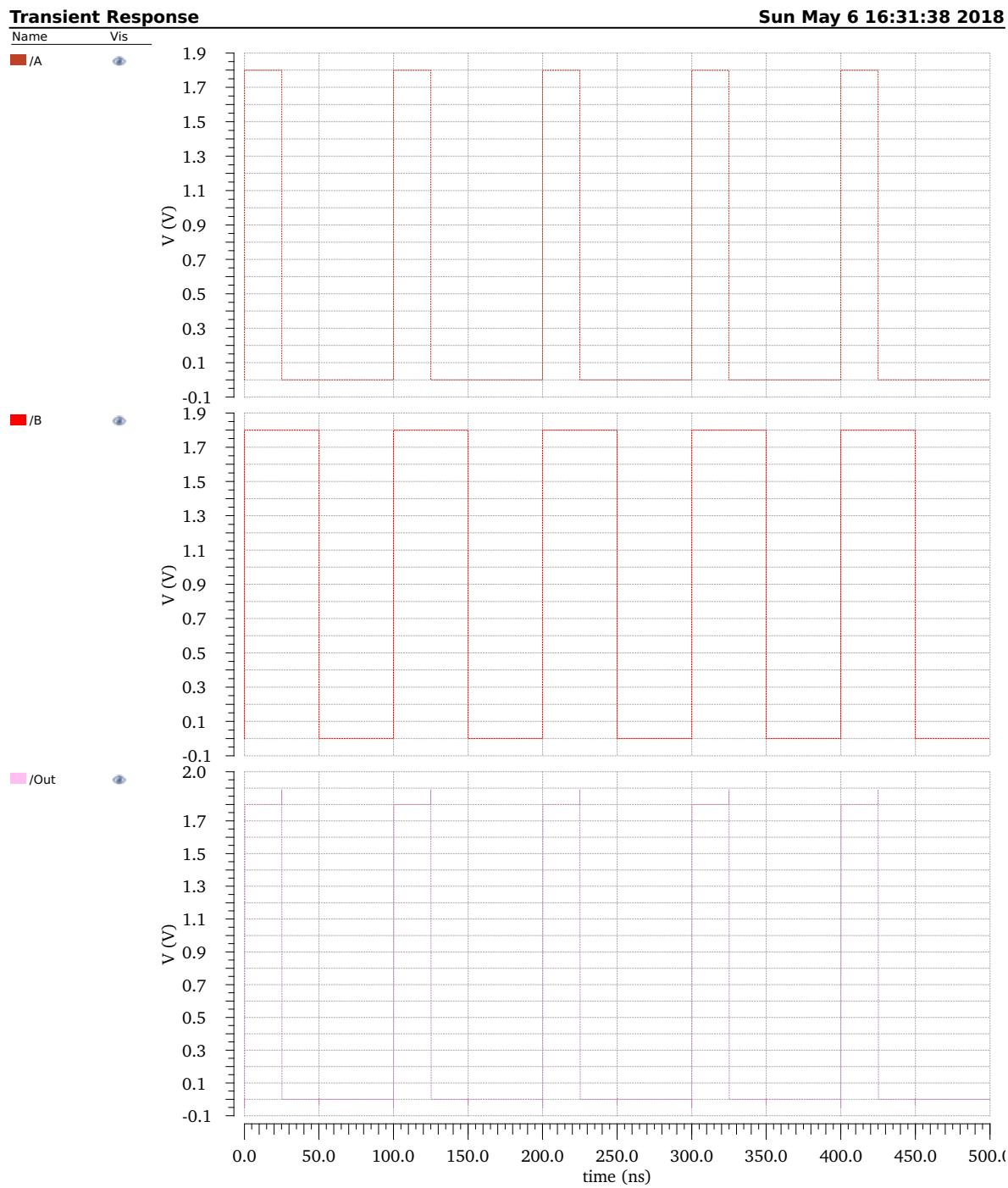
prunedev.out:

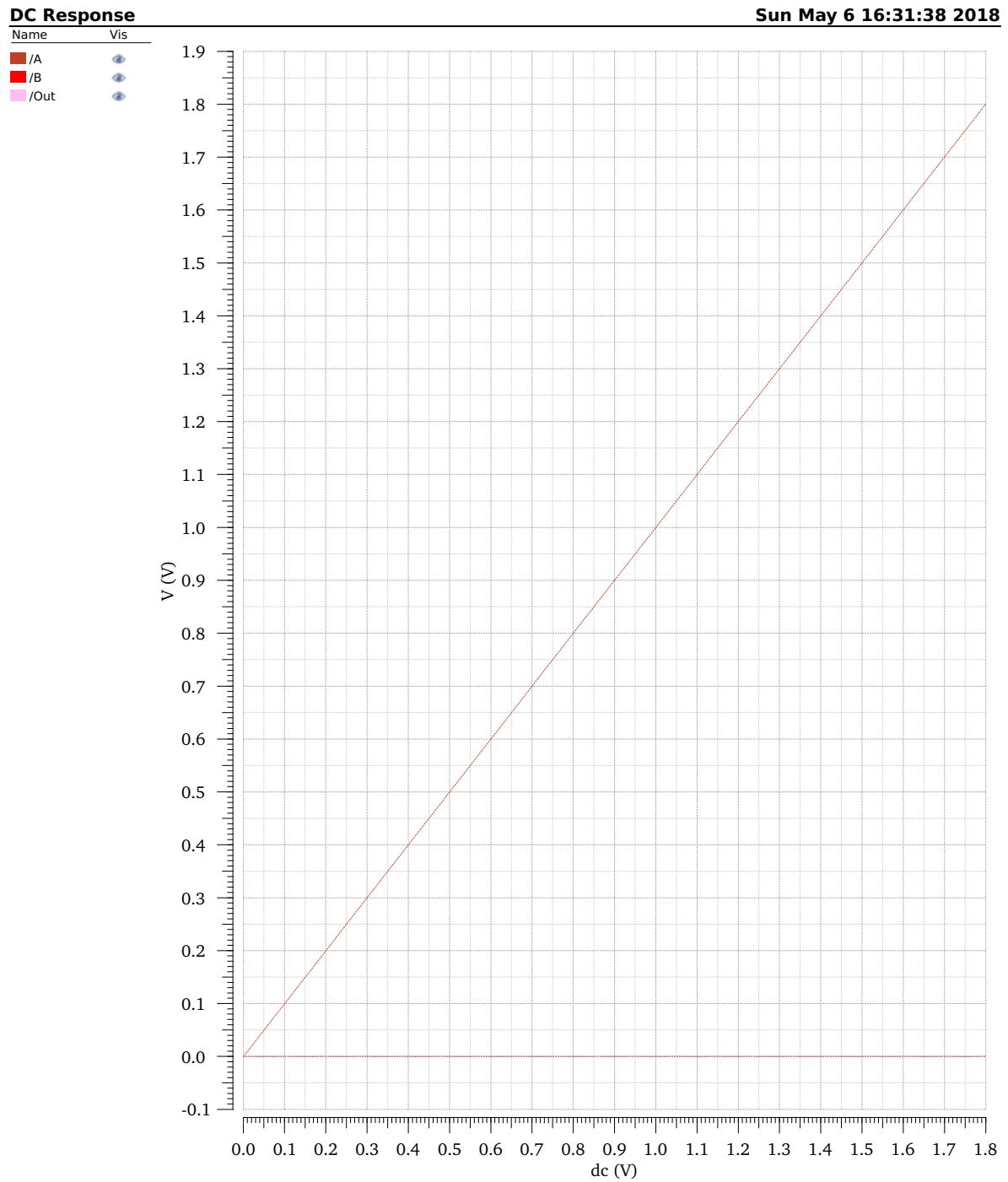
audit.out:

2-Input AND Gate Post Layout

project2:2AND_REAL_tb:1 : project2 2AND_REAL_tb schematic

16:32:26 Sun May 6 2018



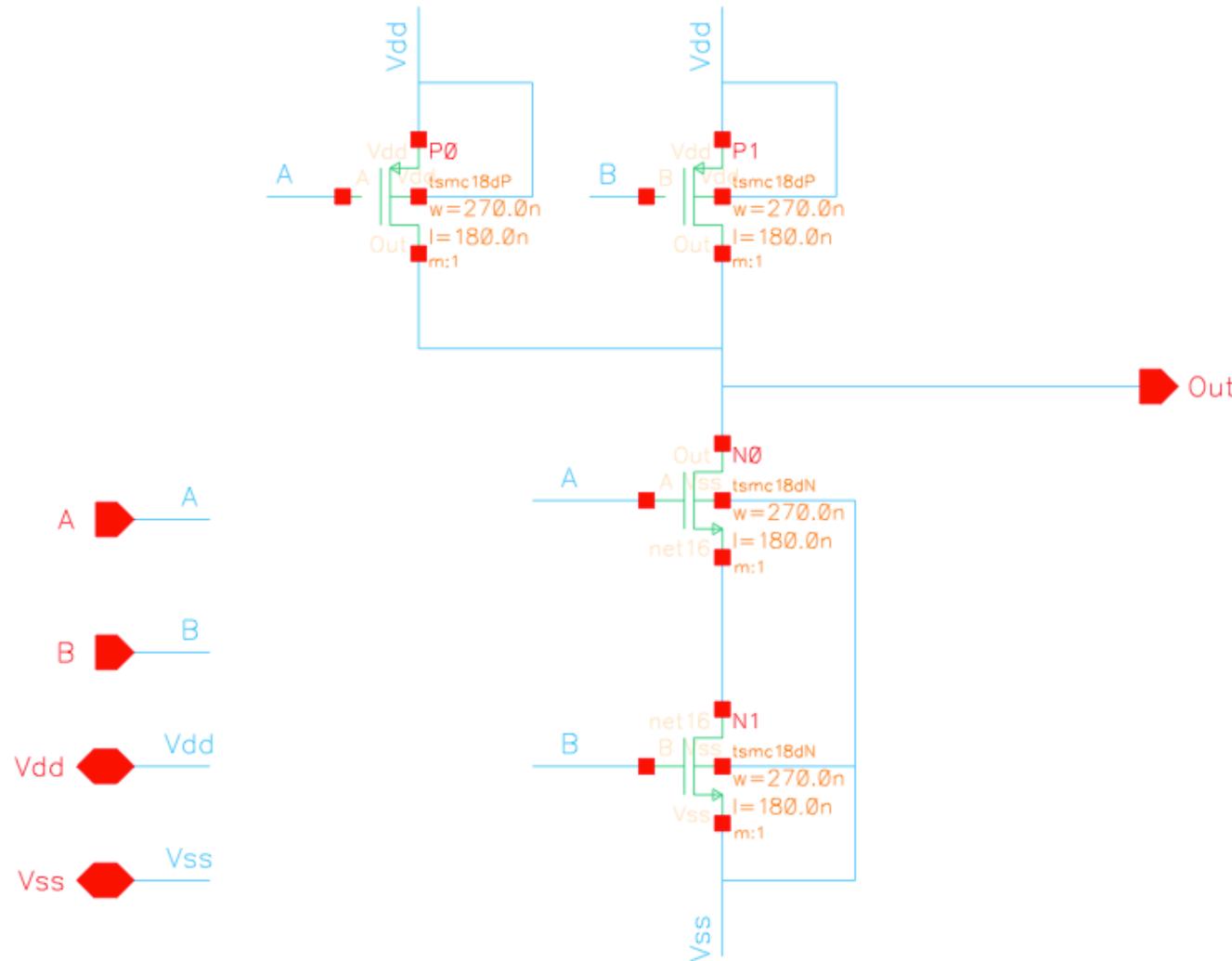


2-Input NAND Gate

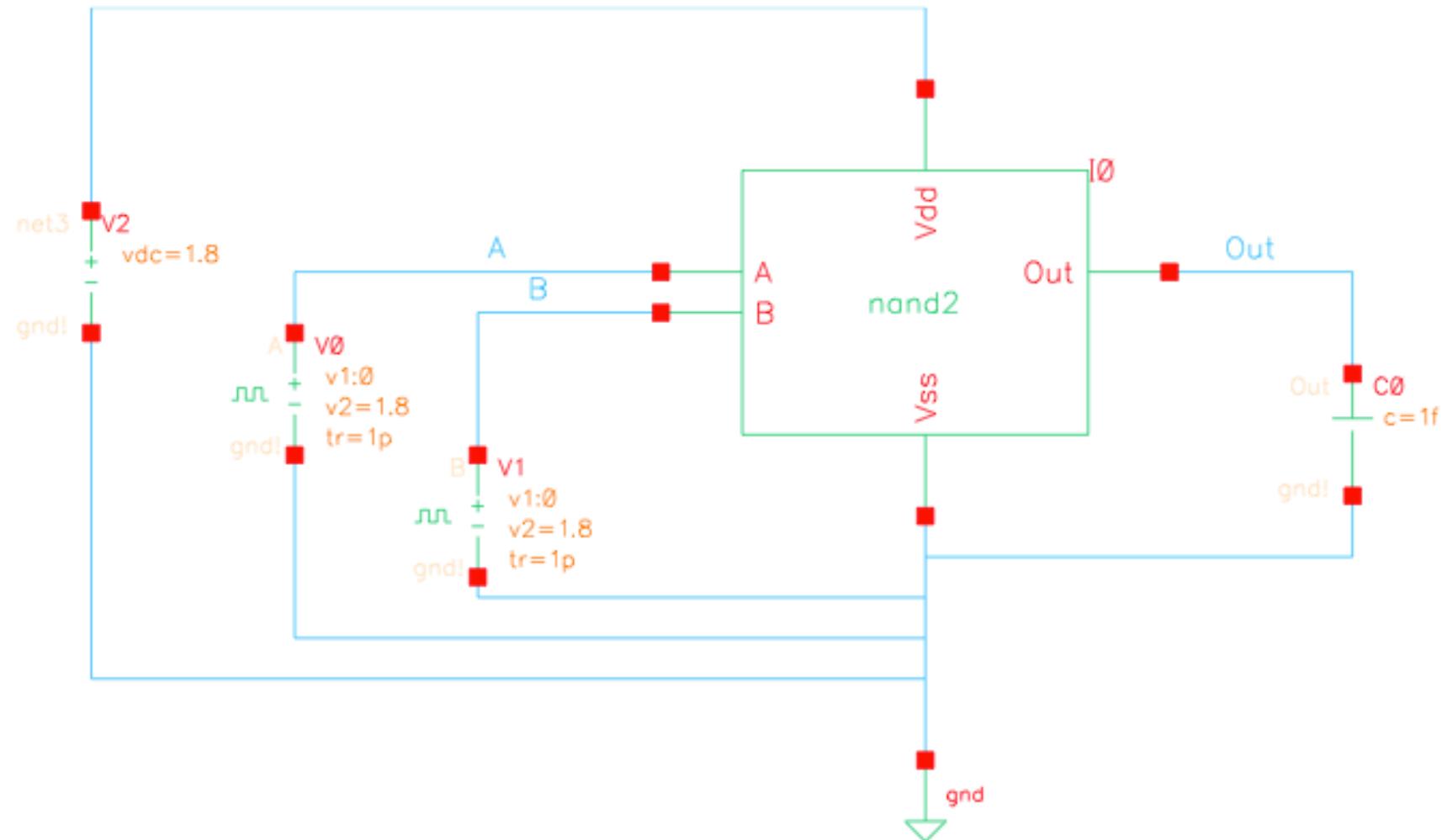
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

2-Input NAND Gate Schematic



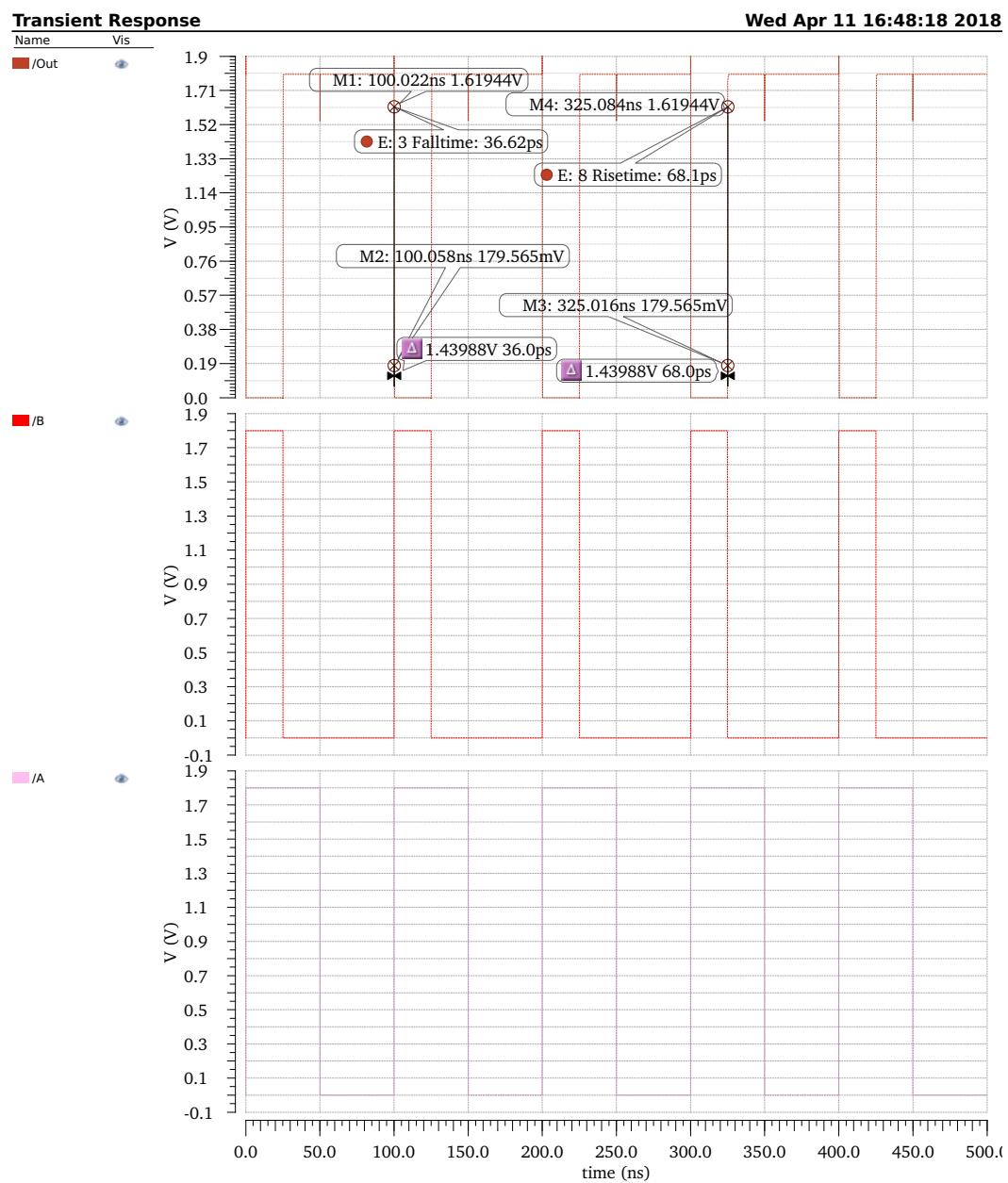
2-Input NAND Gate Testbench



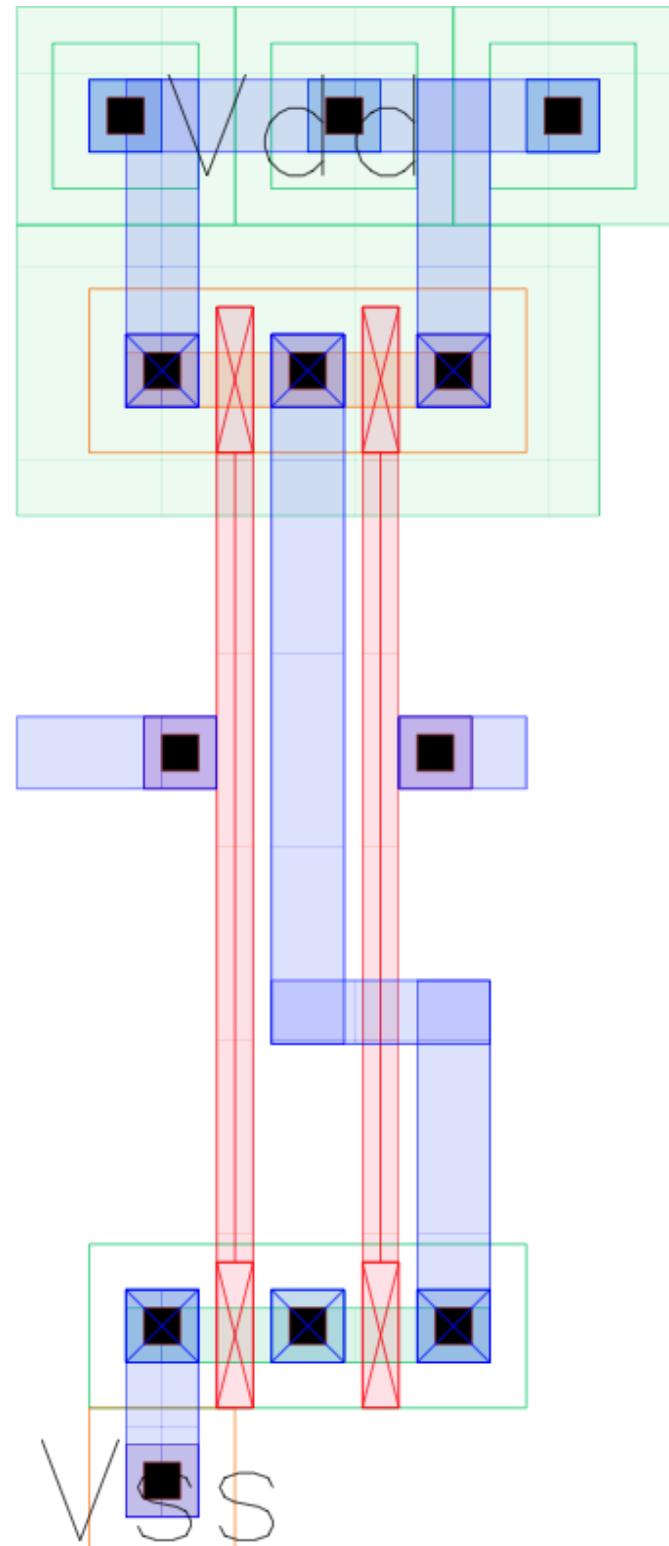
2-Input NAND Gate Testbench Waveform

project2:nand2_tb:1 : project2 nand2_tb schematic

16:52:05 Wed Apr 11 2018



2-Input NAND Gate Layout



2-Input NAND Gate DRC

```
Getting layout property bag
DRC started at Fri May  4 17:27:41 2018

Validating hierarchy instantiation for:
library: project2
cell:    nand2_layout
view:   layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Fri May  4 17:27:41 2018
completed ....Fri May  4 17:27:41 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*****      Summary of rule violations for cell "nand2_layout layout"      *****
Total errors found: 0
```

2-Input NAND Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
6	nets
0	terminals
2	pmos
2	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

layout	schematic
instances	
un-matched	0 0
rewired	0 0
size errors	0 0
pruned	0 0
active	4 4
total	4 4

nets	
un-matched	0 0

merged	0	0
pruned	0	0
active	6	6
total	6	6

terminals		
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

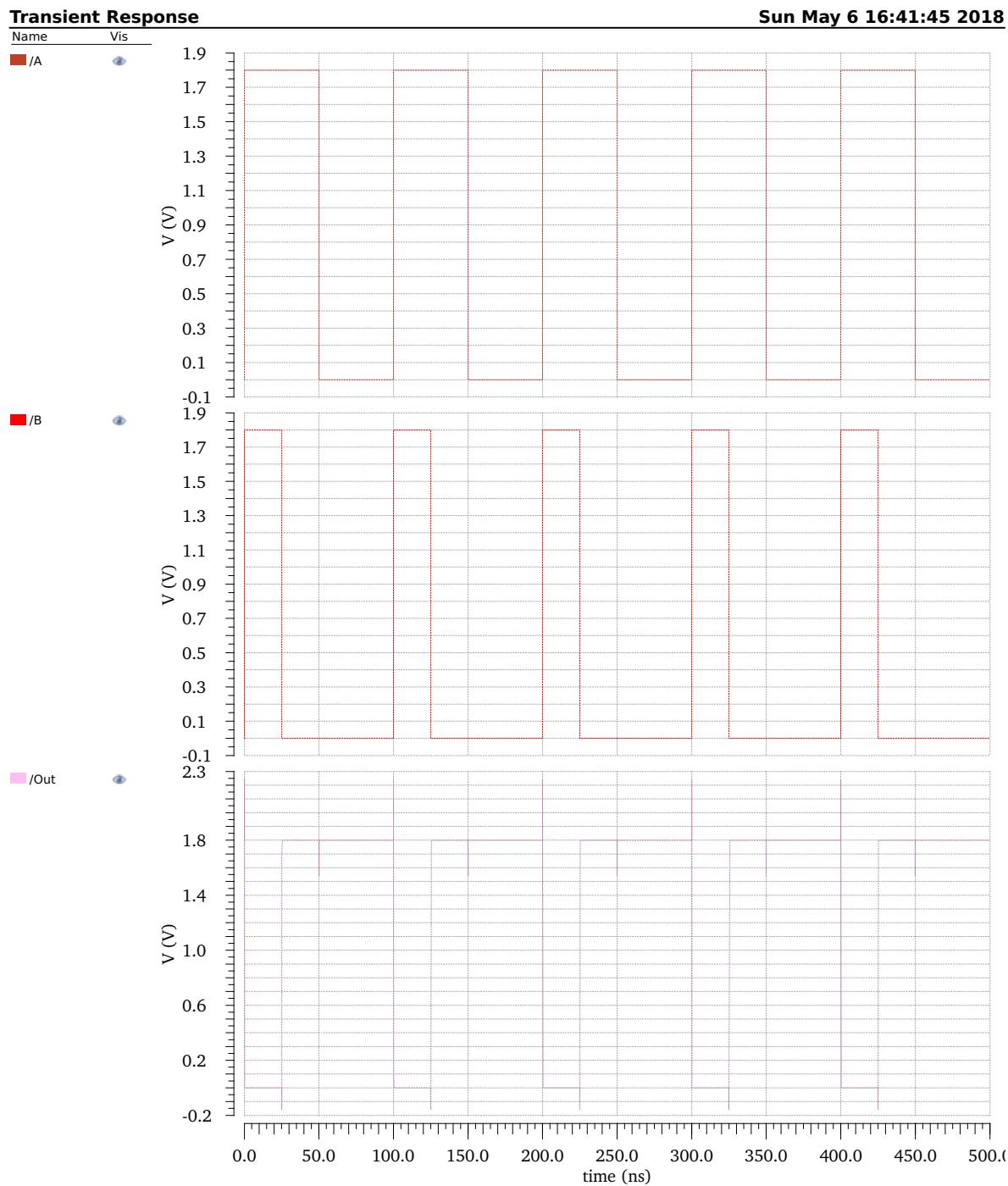
prunedev.out:

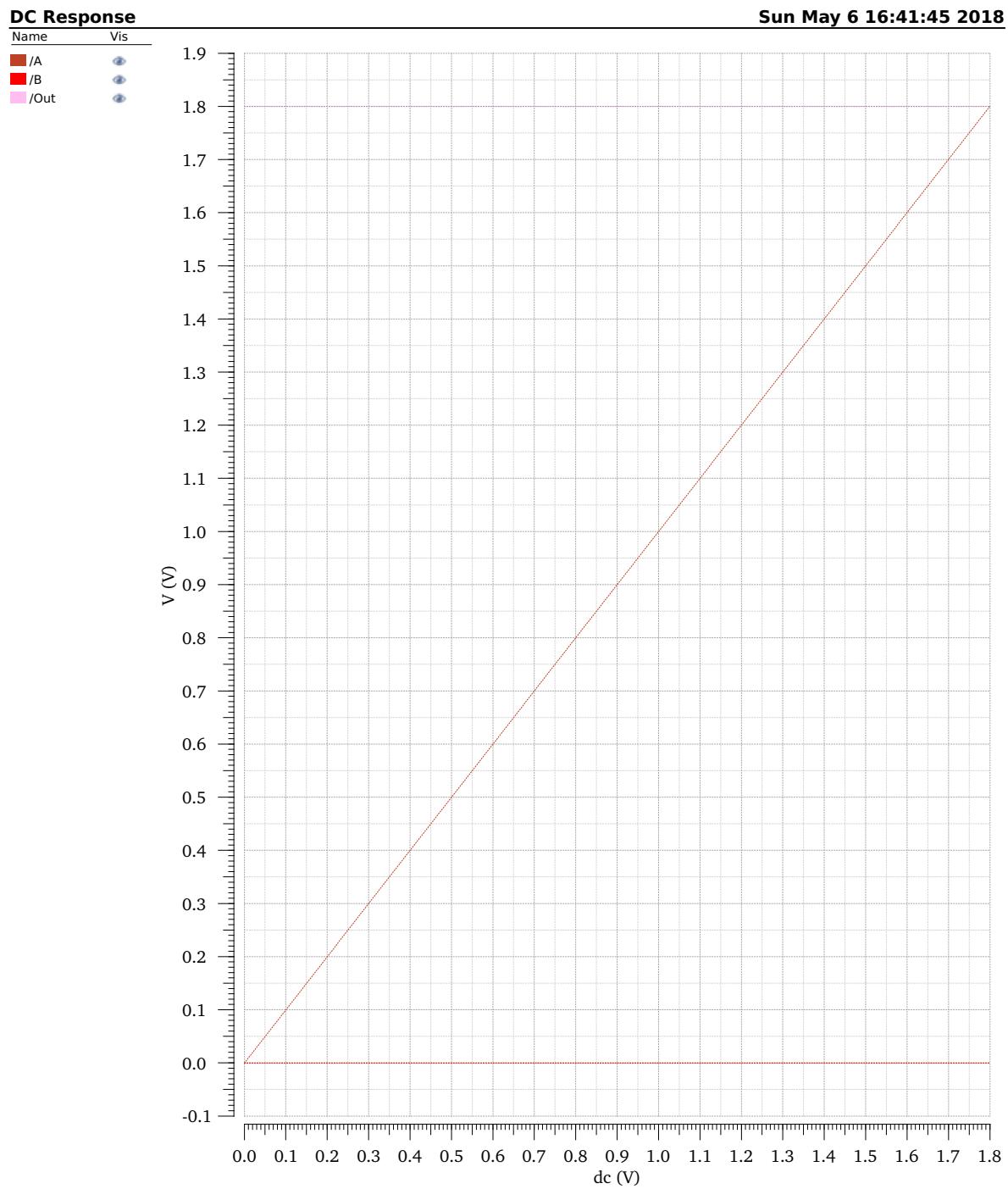
audit.out:

2-Input NAND Gate Post-Layout

project2:nand2_tb:1 : project2 nand2_tb schematic

16:42:17 Sun May 6 2018



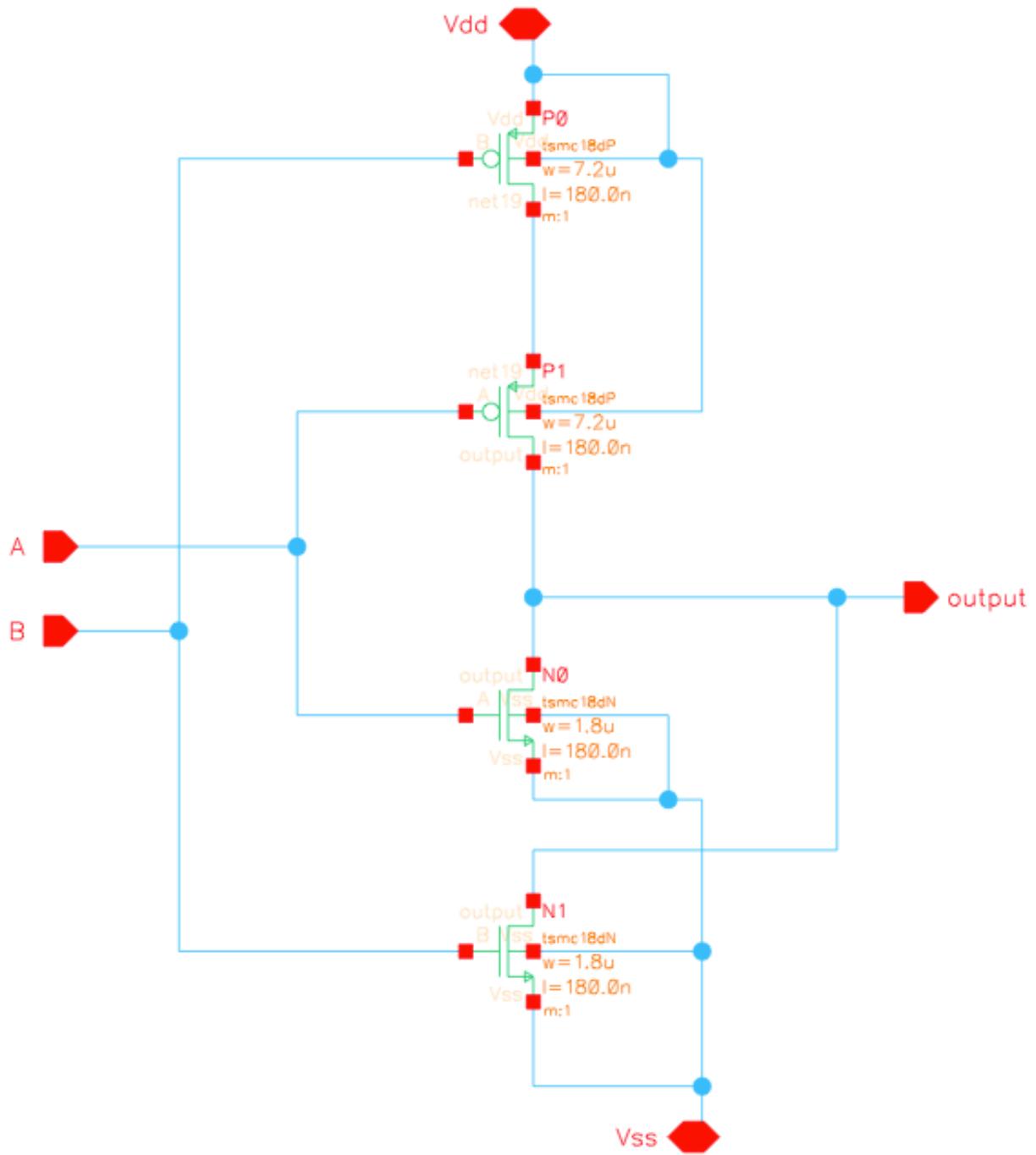


2-Input NOR Gate

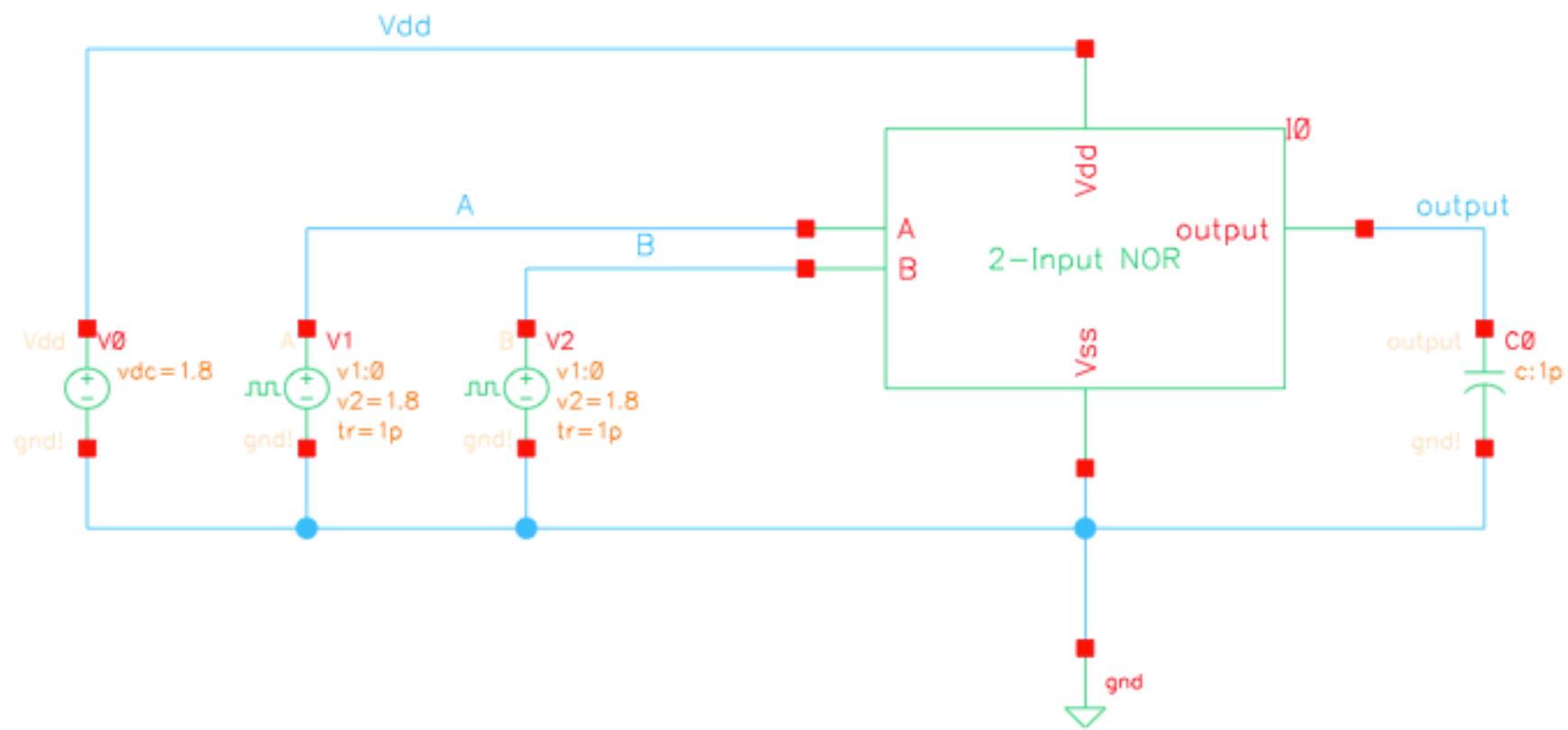
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 7.2/0.18$$

2-Input NOR Gate Schematic



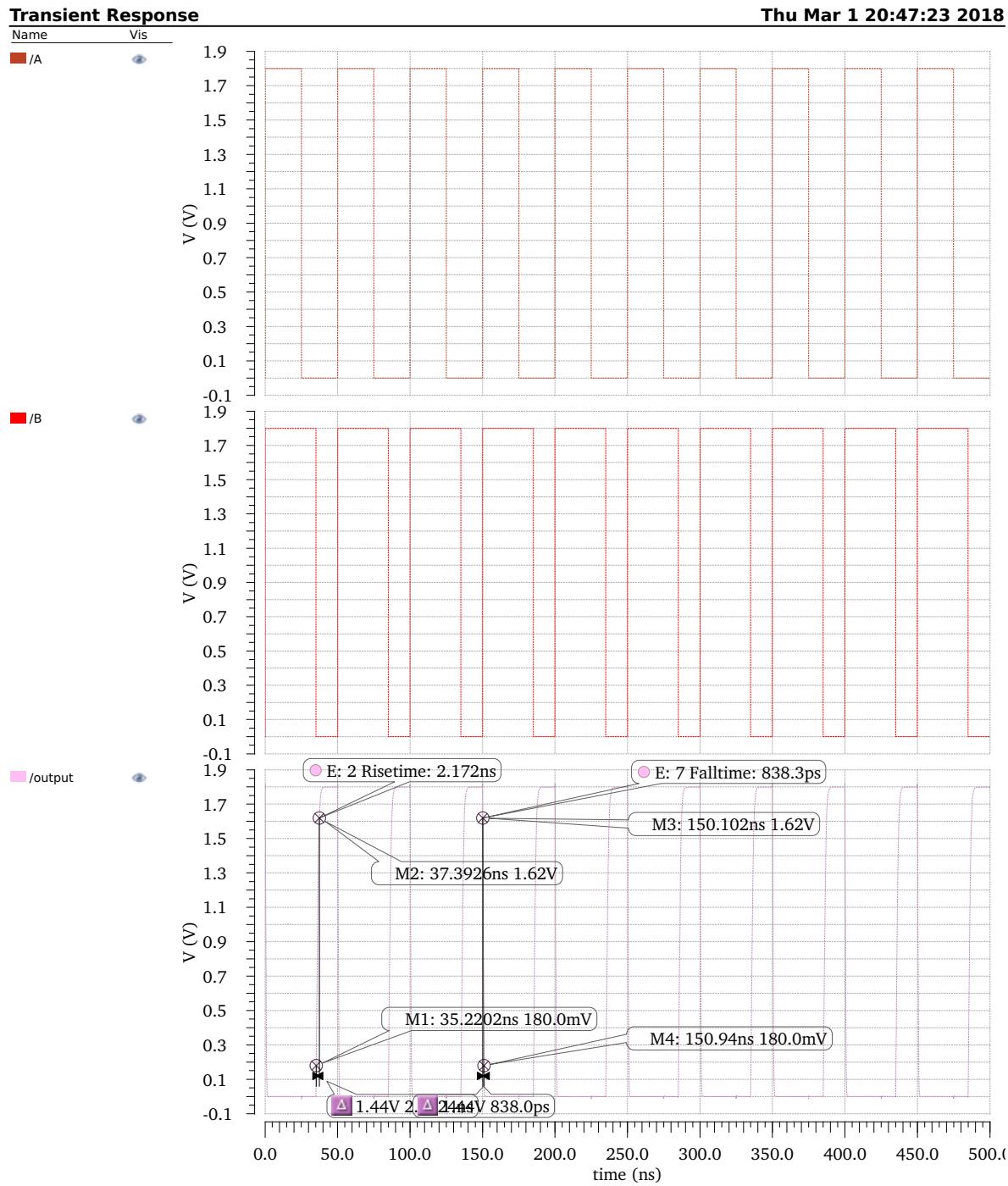
2-Input NOR Gate Testbench



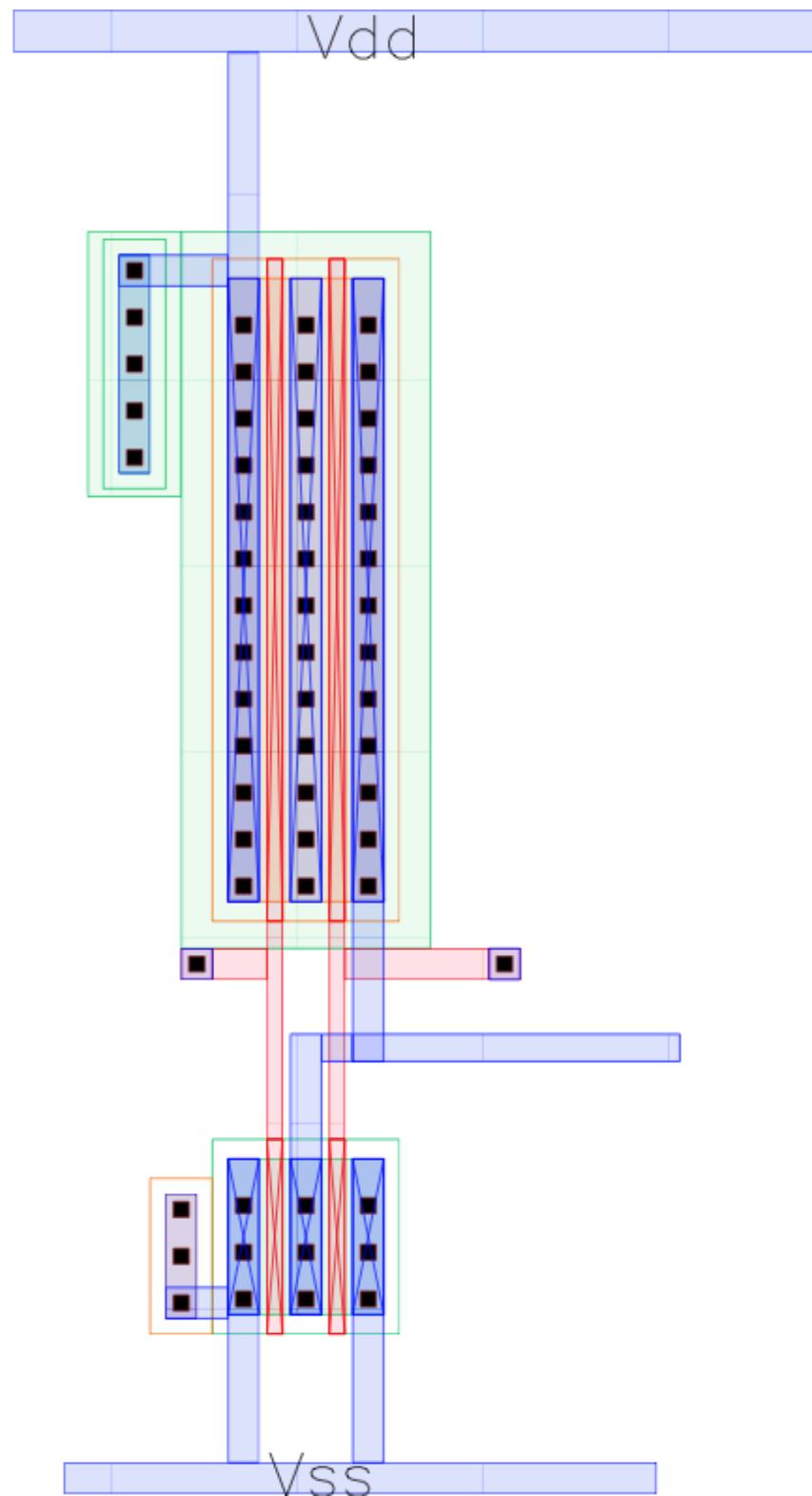
2-Input NOR Gate Testbench Waveform

NOR:NOR_testbench:1 : NOR NOR_testbench schematic

20:51:44 Thu Mar 1 2018



2-Input NOR Gate Layout



2-Input NOR Gate DRC

```
Getting layout property bag
DRC started at Fri May  4 17:20:19 2018

Validating hierarchy instantiation for:
library: project2
cell:    nor2_layout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Fri May  4 17:20:19 2018
completed ....Fri May  4 17:20:19 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*****      Summary of rule violations for cell "nor2_layout layout"      *****
Total errors found: 0
```

2-Input NOR Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
6	nets
0	terminals
2	pmos
2	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4

	nets
un-matched	0 0

merged	0	0
pruned	0	0
active	6	6
total	6	6

terminals		
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

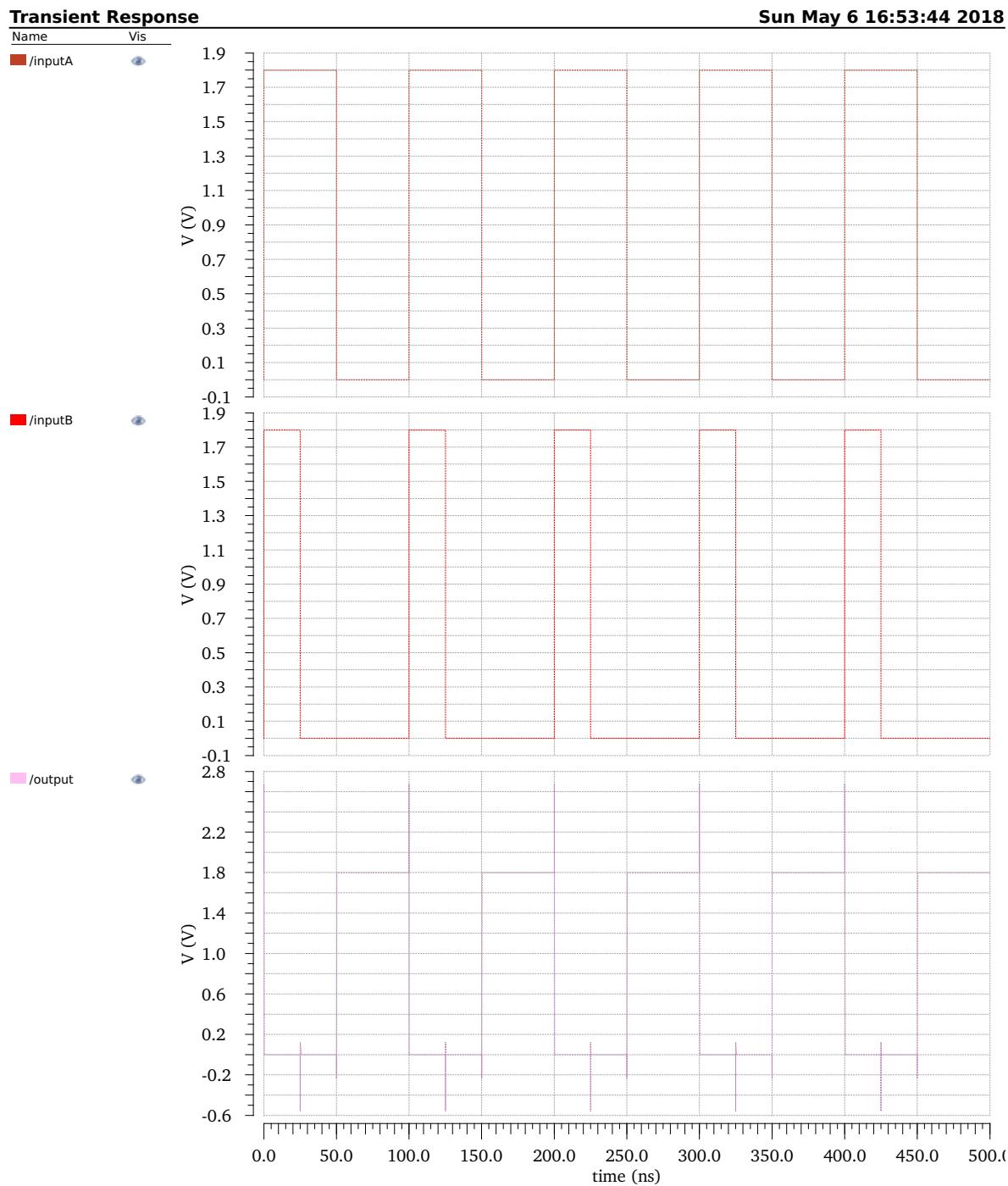
prunedev.out:

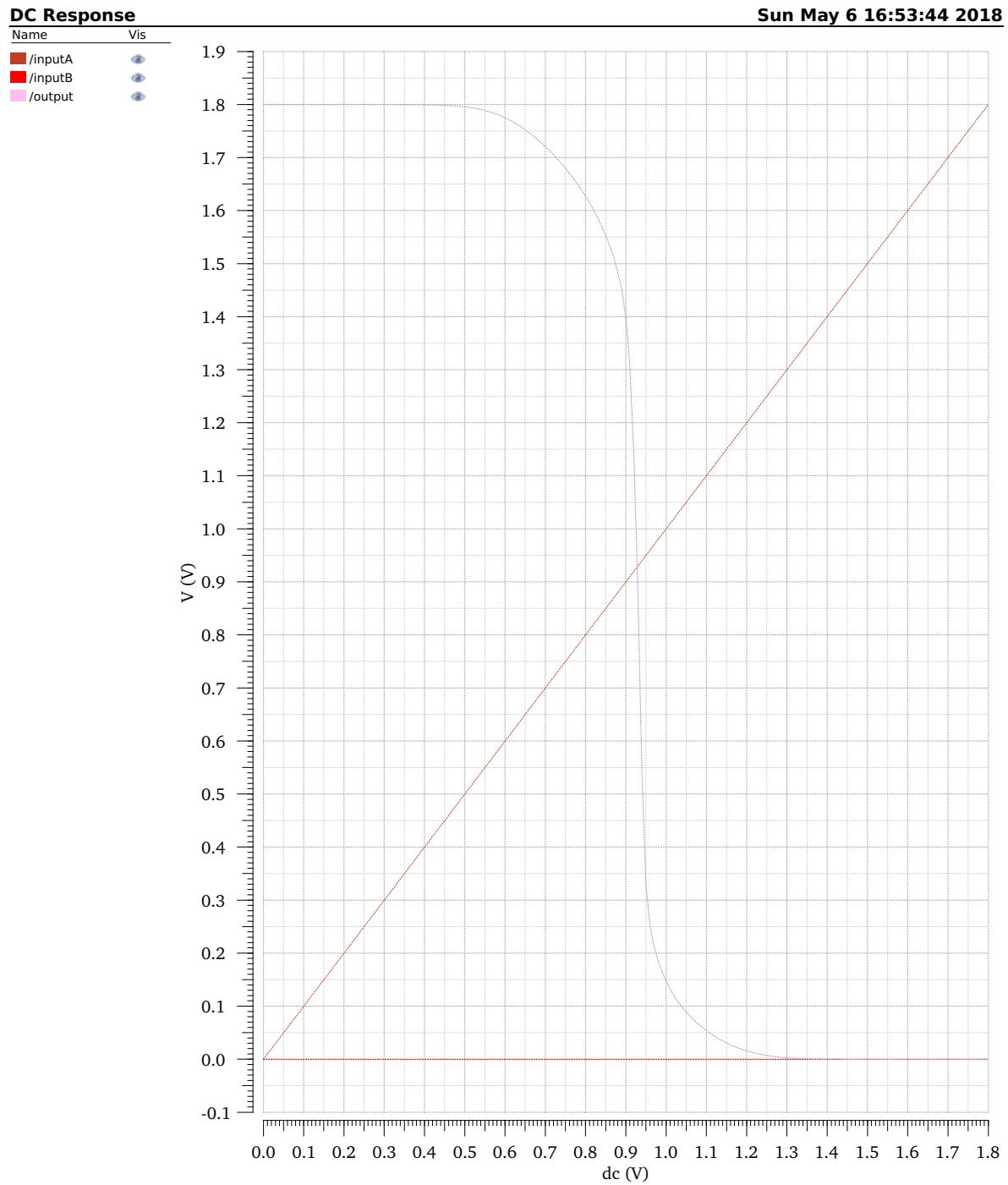
audit.out:

2-Input NOR Gate Post-Layout

project2:nor2_tb:1 : project2 nor2_tb schematic

16:54:10 Sun May 6 2018





ALU

4-Bit Addition, 2s Complement Subtraction and Multiplier

ALU Schematic

ALU Testbench

ALU Testbench Waveform

ALU Layout

ALU DRC

ALU LVS

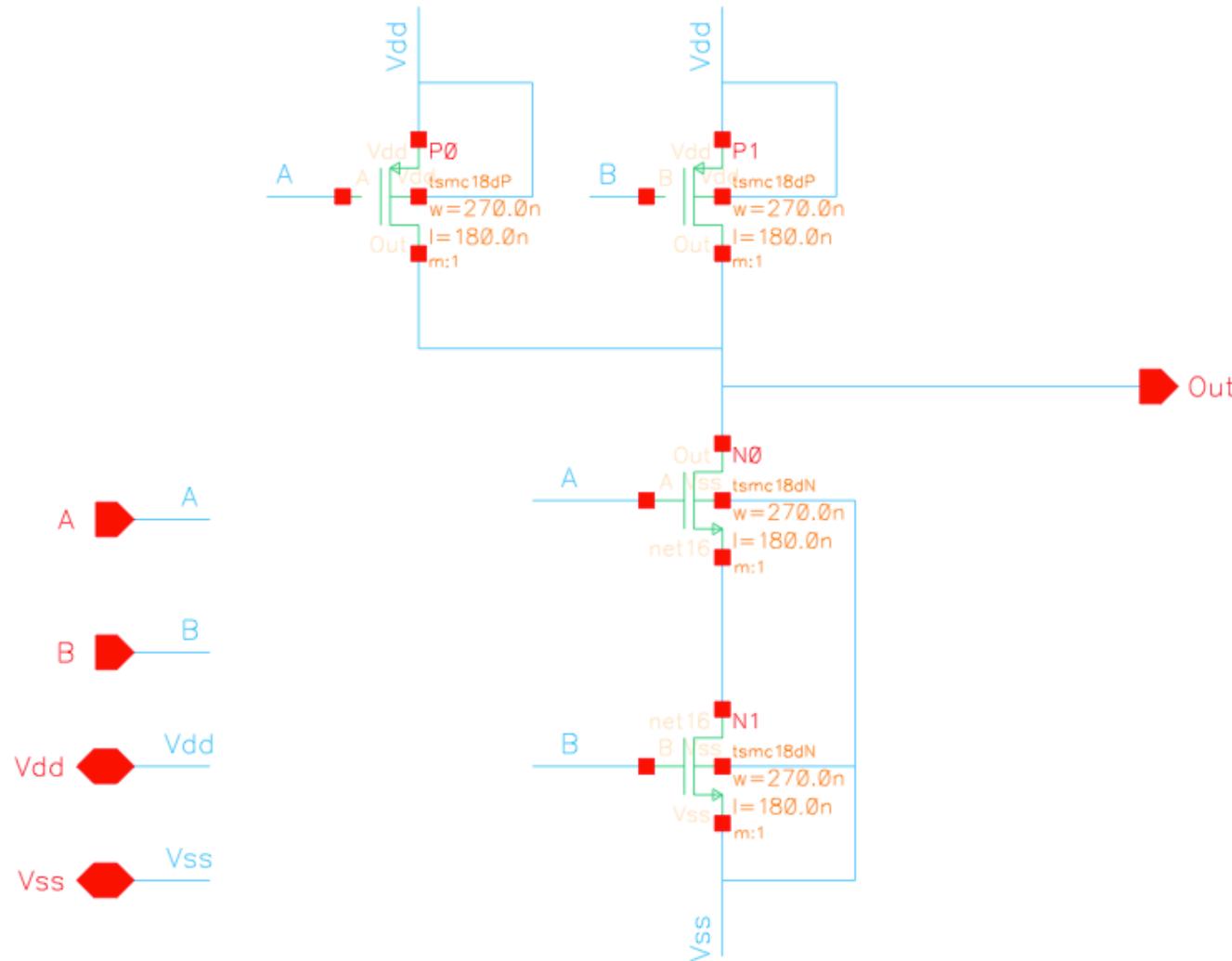
ALU Post-Layout

2-Input NAND Gate

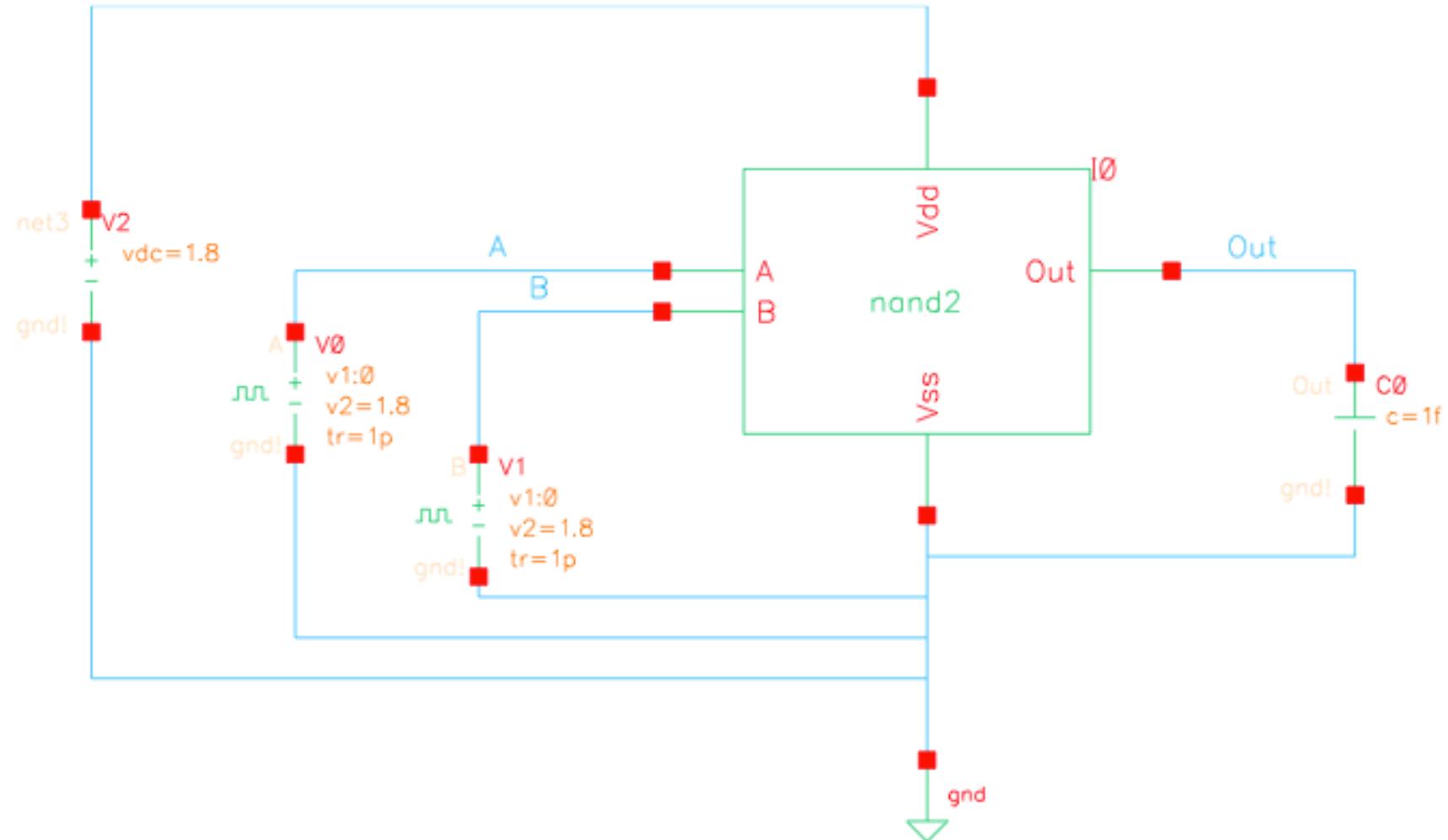
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

2-Input NAND Gate Schematic



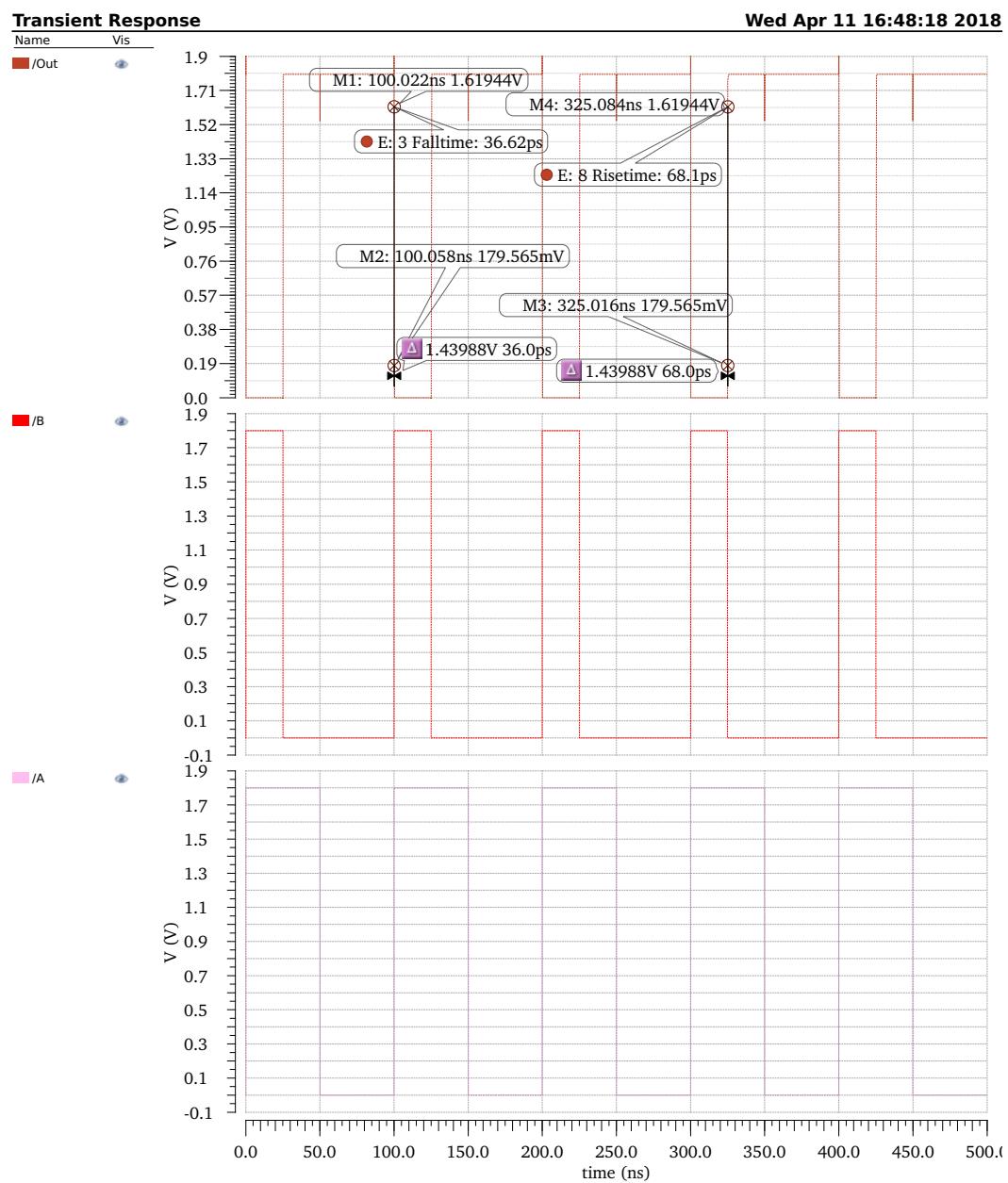
2-Input NAND Gate Testbench



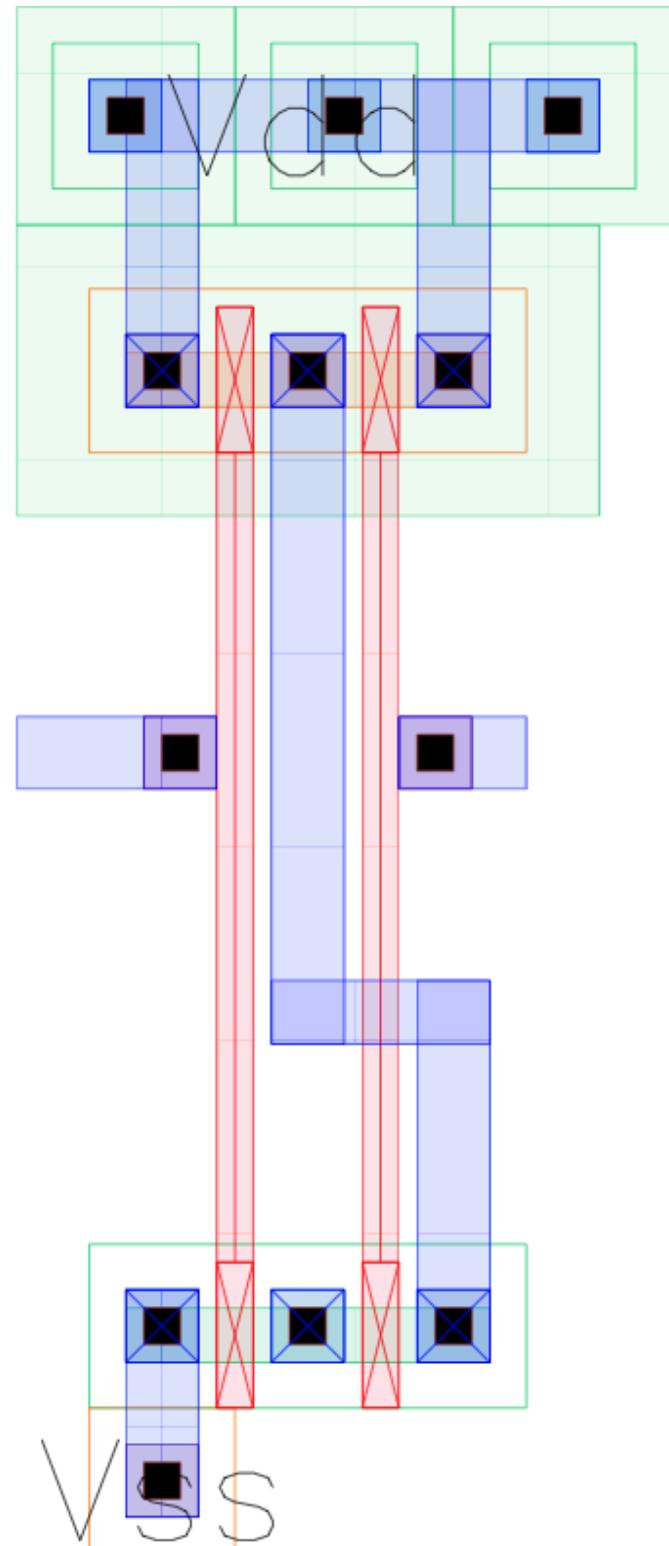
2-Input NAND Gate Testbench Waveform

project2:nand2_tb:1 : project2 nand2_tb schematic

16:52:05 Wed Apr 11 2018



2-Input NAND Gate Layout



2-Input NAND Gate DRC

```
Getting layout property bag
DRC started at Fri May  4 17:27:41 2018

Validating hierarchy instantiation for:
library: project2
cell:    nand2_layout
view:   layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Fri May  4 17:27:41 2018
completed ....Fri May  4 17:27:41 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*****      Summary of rule violations for cell "nand2_layout layout"      *****
Total errors found: 0
```

2-Input NAND Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
6	nets
0	terminals
2	pmos
2	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

layout	schematic
instances	
un-matched	0 0
rewired	0 0
size errors	0 0
pruned	0 0
active	4 4
total	4 4

nets	
un-matched	0 0

```
merged          0  0
pruned          0  0
active          6  6
total           6  6
```

```
terminals
un-matched      0  0
matched but
different type   0  0
total            0  5
```

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

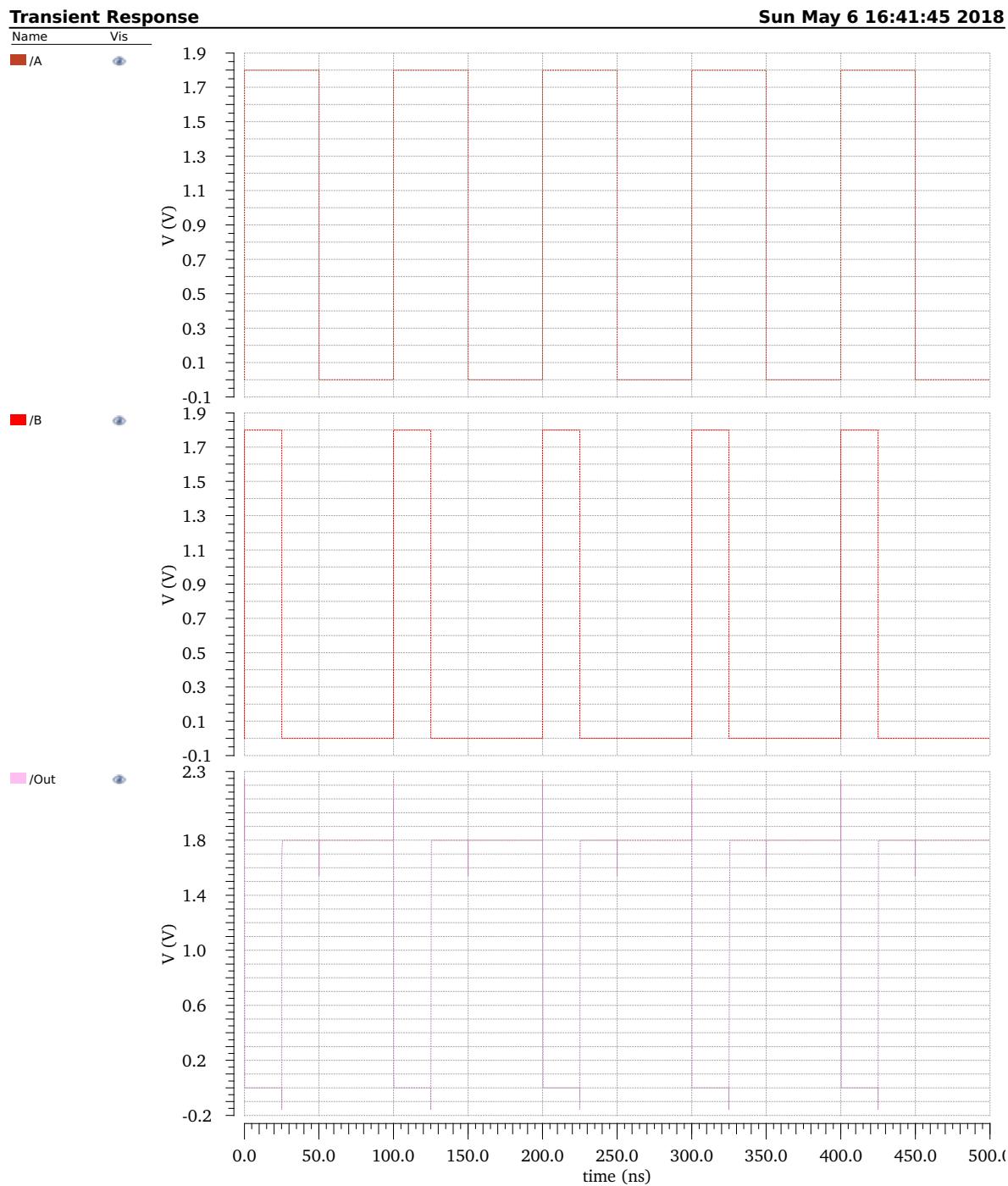
prunedev.out:

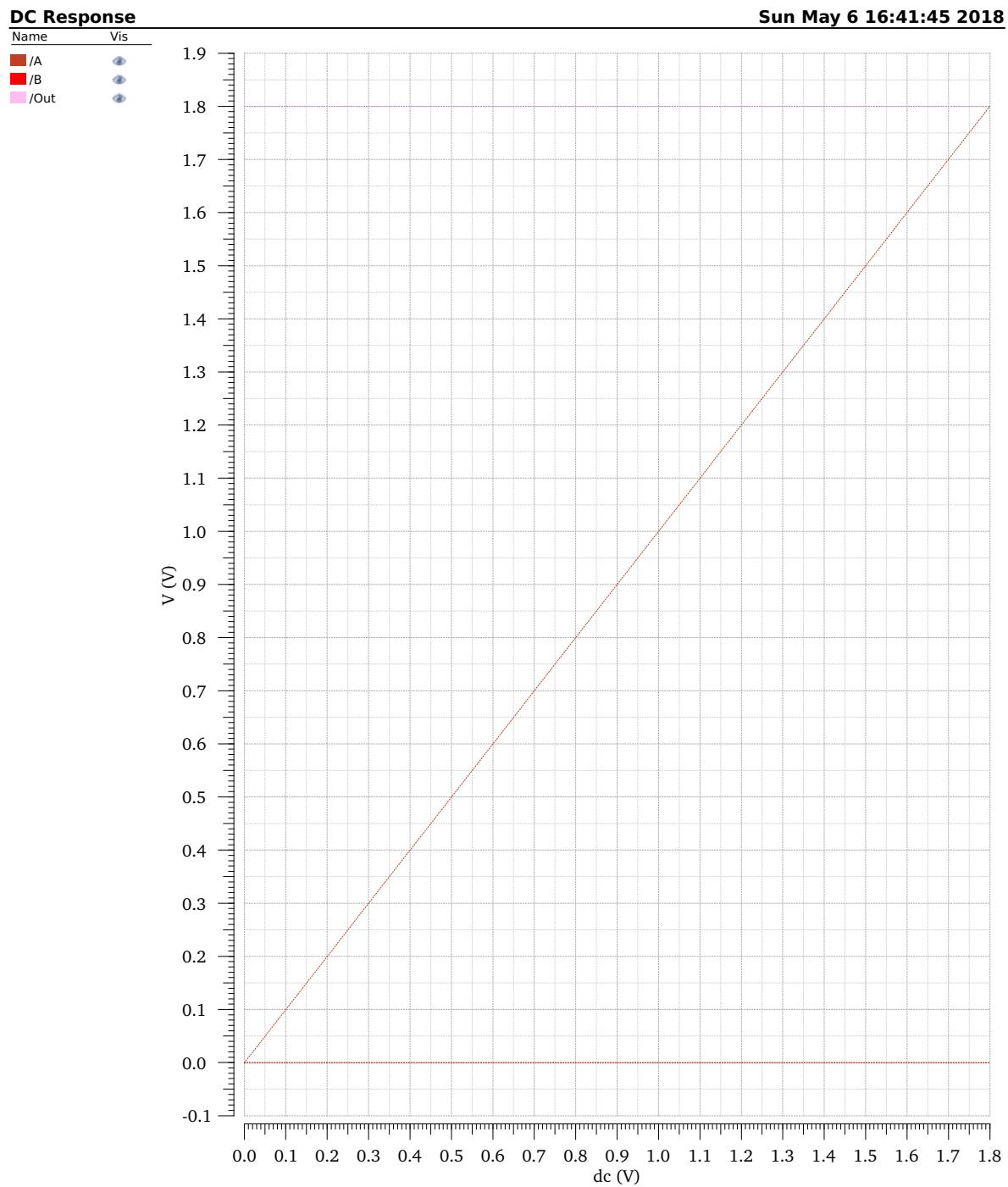
audit.out:

2-Input NAND Gate Post-Layout

project2:nand2_tb:1 : project2 nand2_tb schematic

16:42:17 Sun May 6 2018

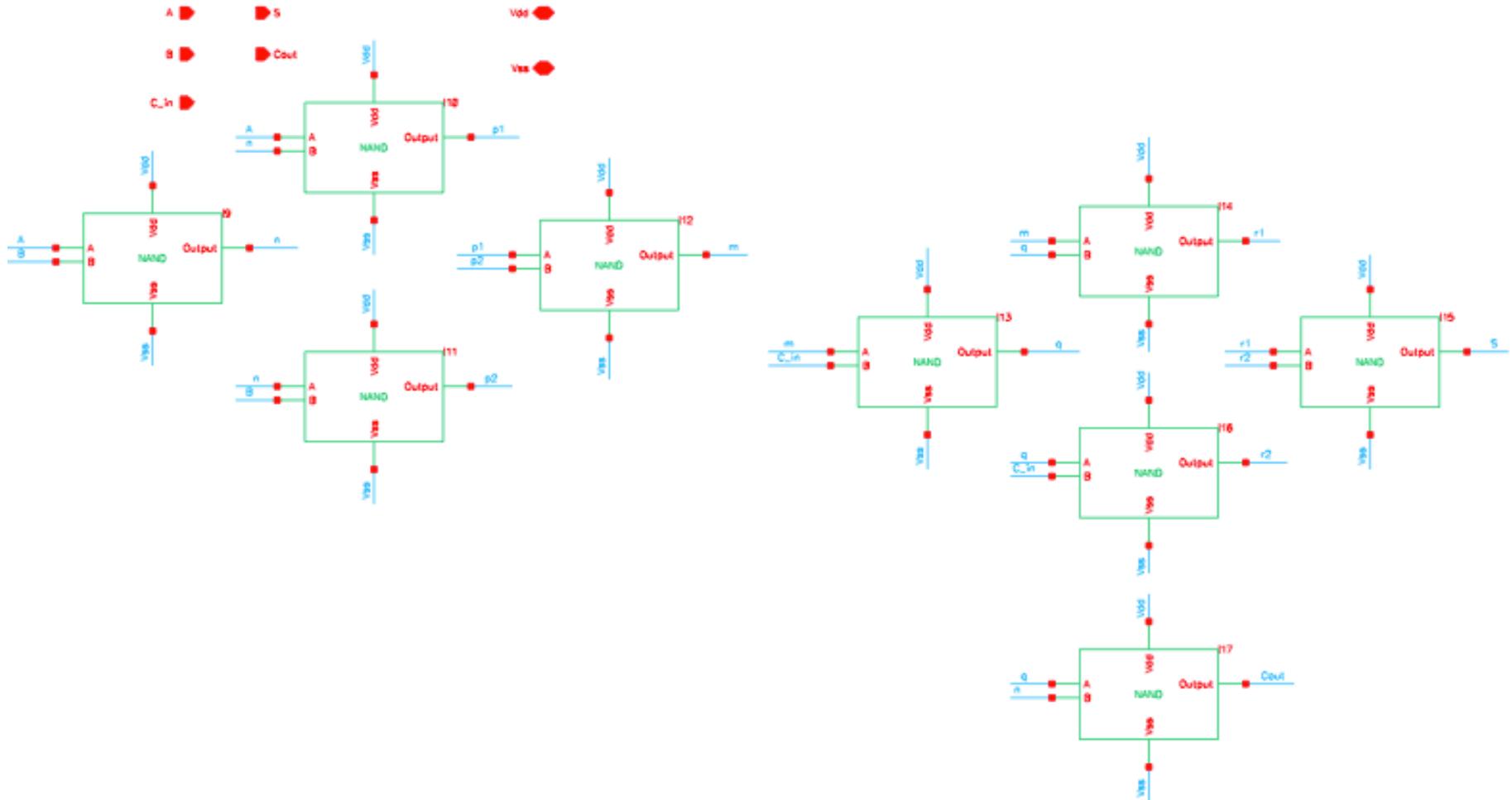




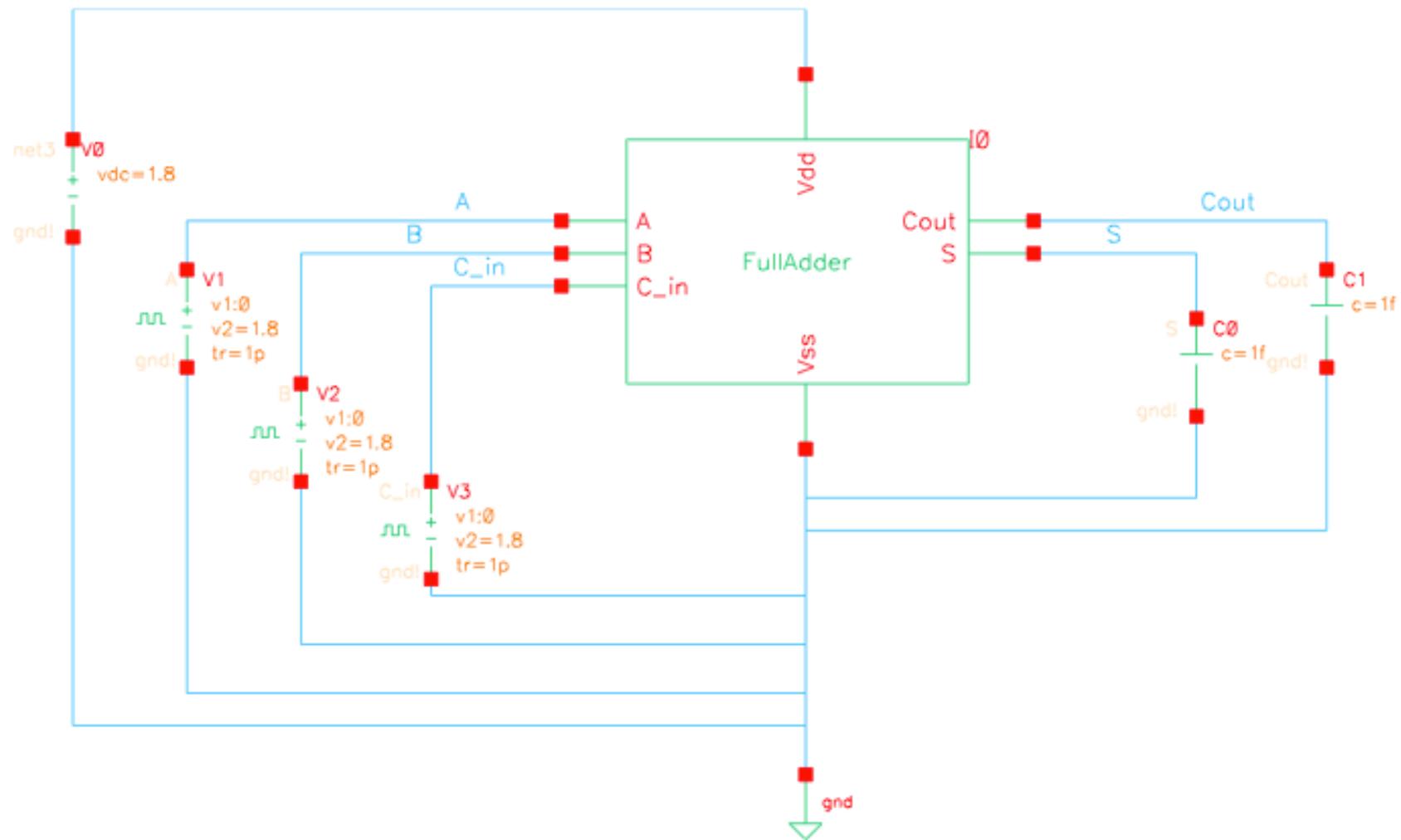
Full Adder

Contains NAND Gate

Full Adder Schematic



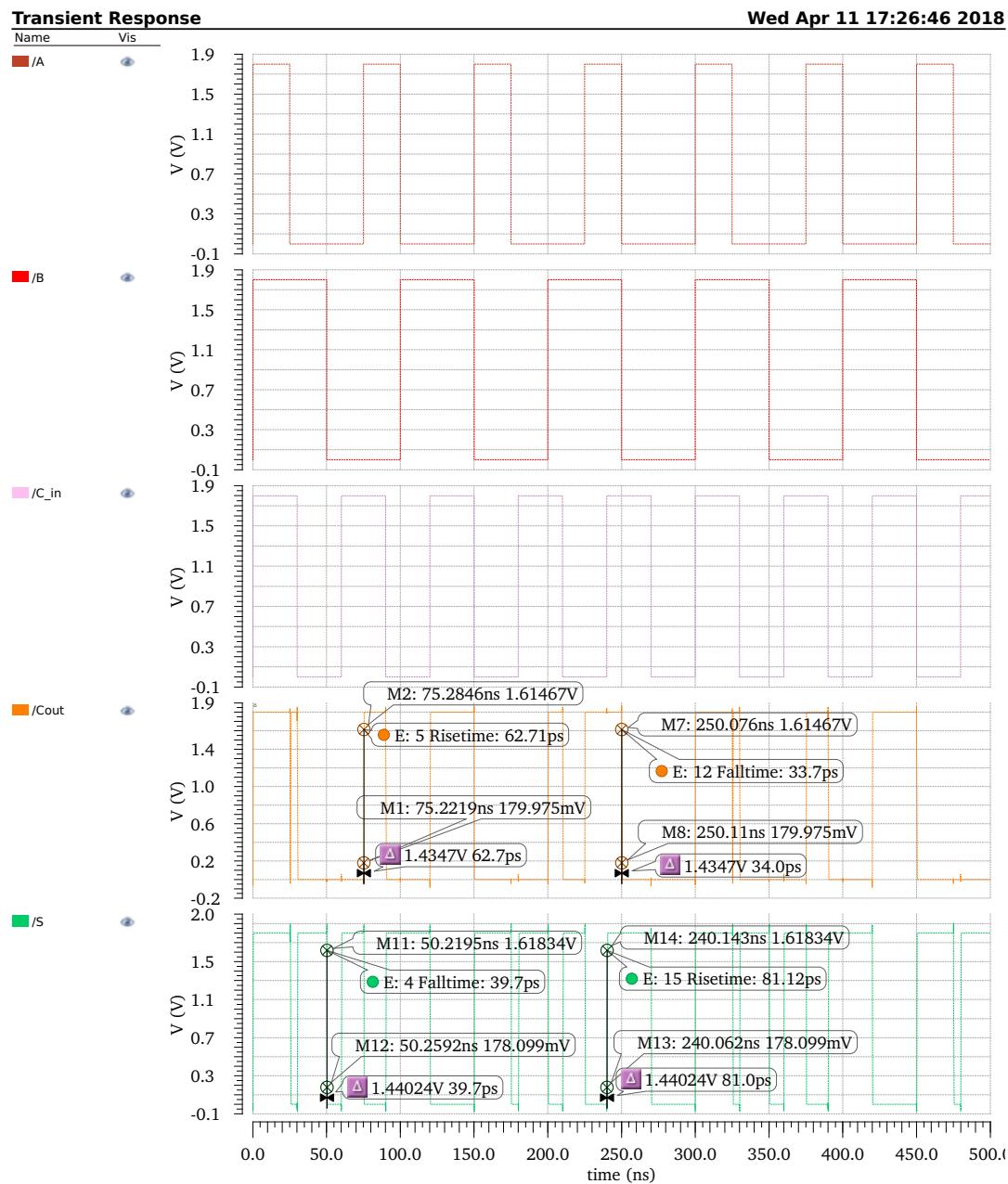
Full Adder Testbench



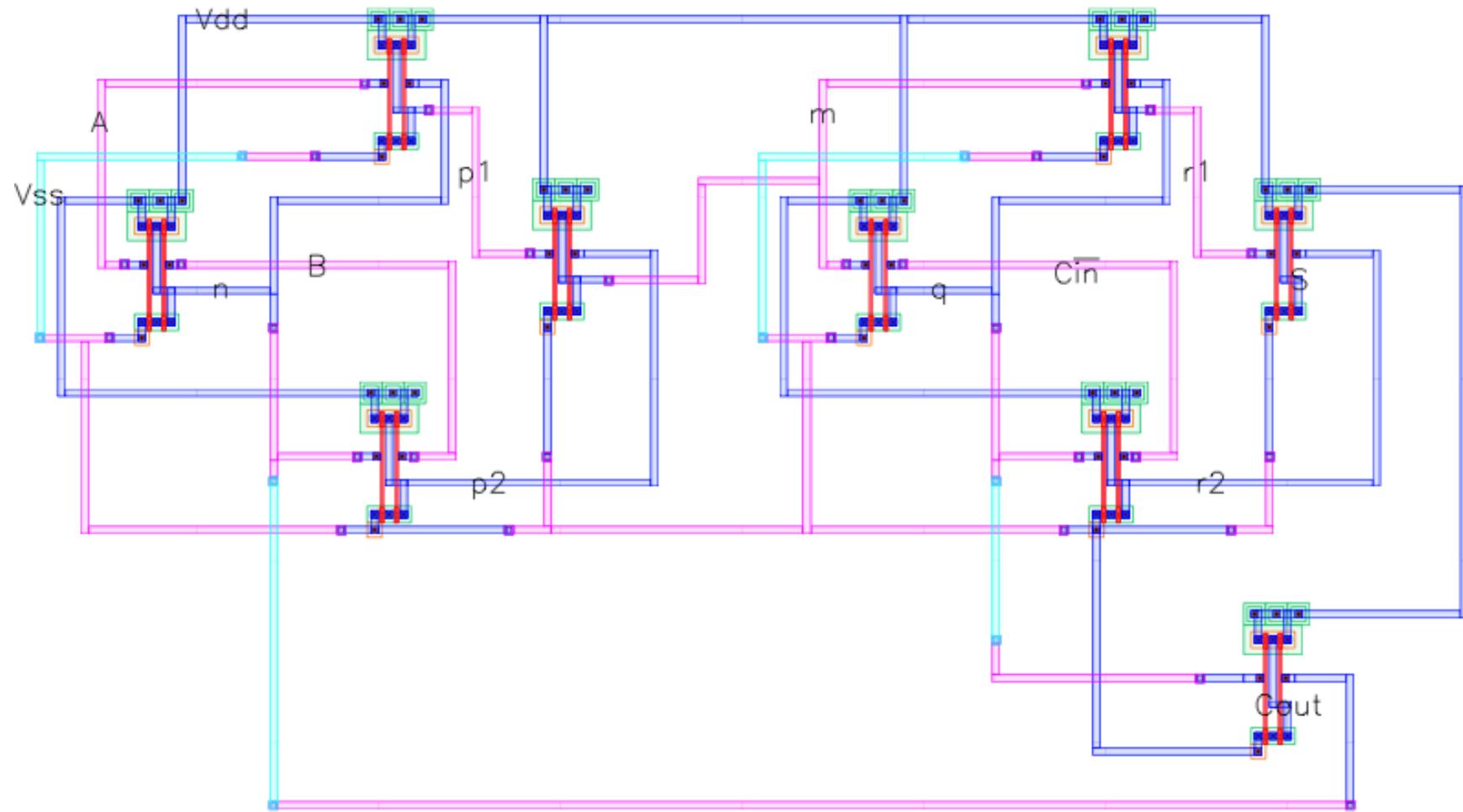
Full Adder Testbench Waveform

project2:fullAdder_tb:1 : project2 fullAdder_tb schematic

17:31:52 Wed Apr 11 2018



Full Adder Layout



Full Adder DRC

DRC started at Sun May 6 22:17:45 2018

```
Validating hierarchy instantiation for:  
library: project2  
cell: fullAdder_layout  
view: layout  
Rules come from library NCSU_TechLib_tsmc02d.  
Rules path is divaDRC.rul.  
Inclusion limit is set to 1000.  
Running layout DRC analysis  
Flat mode  
Full checking.  
DRC started.....Sun May 6 22:17:45 2018  
completed ....Sun May 6 22:17:45 2018  
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "fullAdder_layout layout" *****  
Total errors found: 0
```

Full Adder LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
23	nets
0	terminals
18	pmos
18	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
23	nets
7	terminals
18	pmos
18	nmos

Devices in the netlist but not in the rules:

pcapacitor

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	36	36
total	36	36

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	23	23
total	23	23

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	7

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

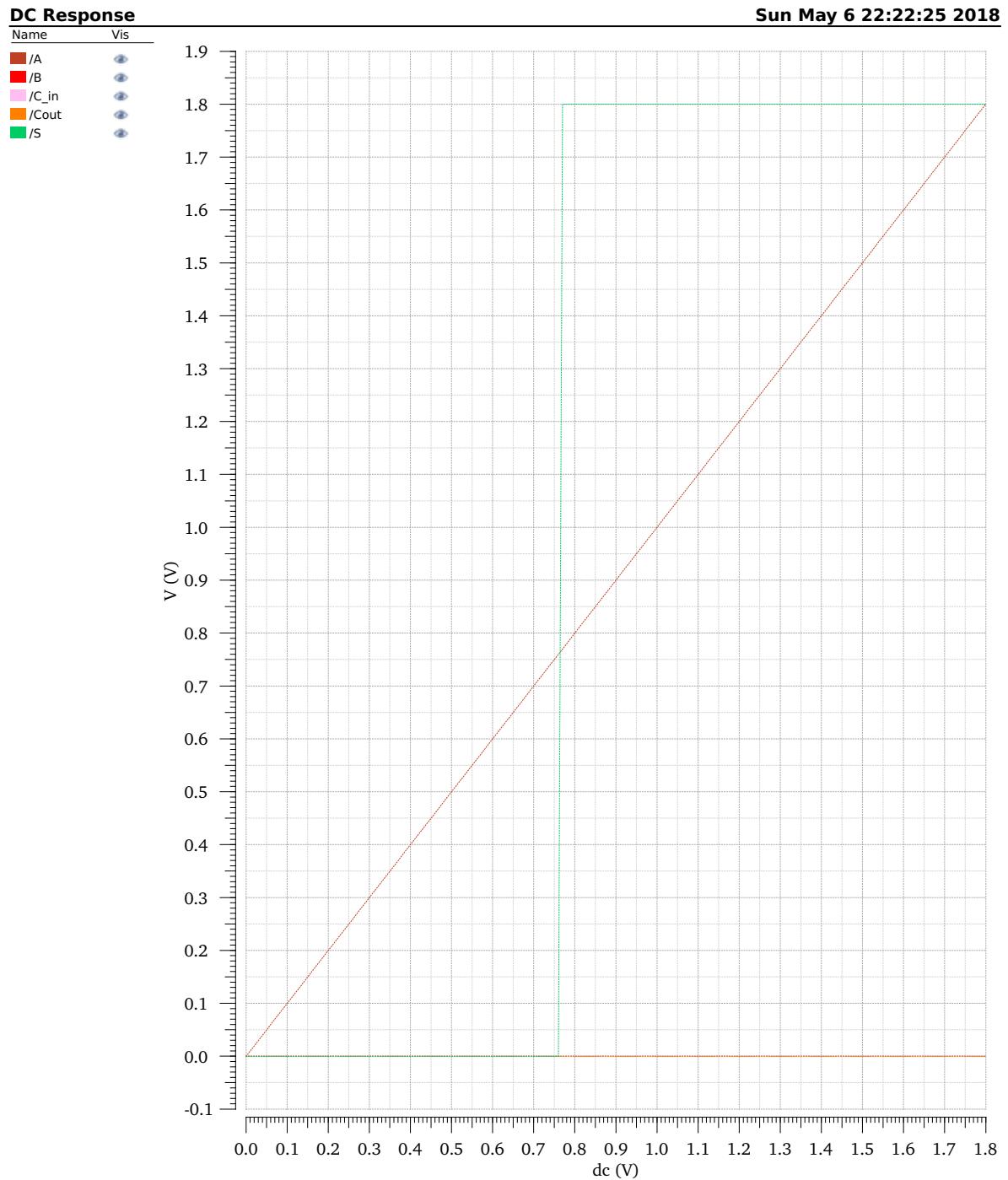
audit.out:

Full Adder Post-Layout

project2:fullAdder_tb:1 : project2 fullAdder_tb schematic

22:22:57 Sun May 6 2018



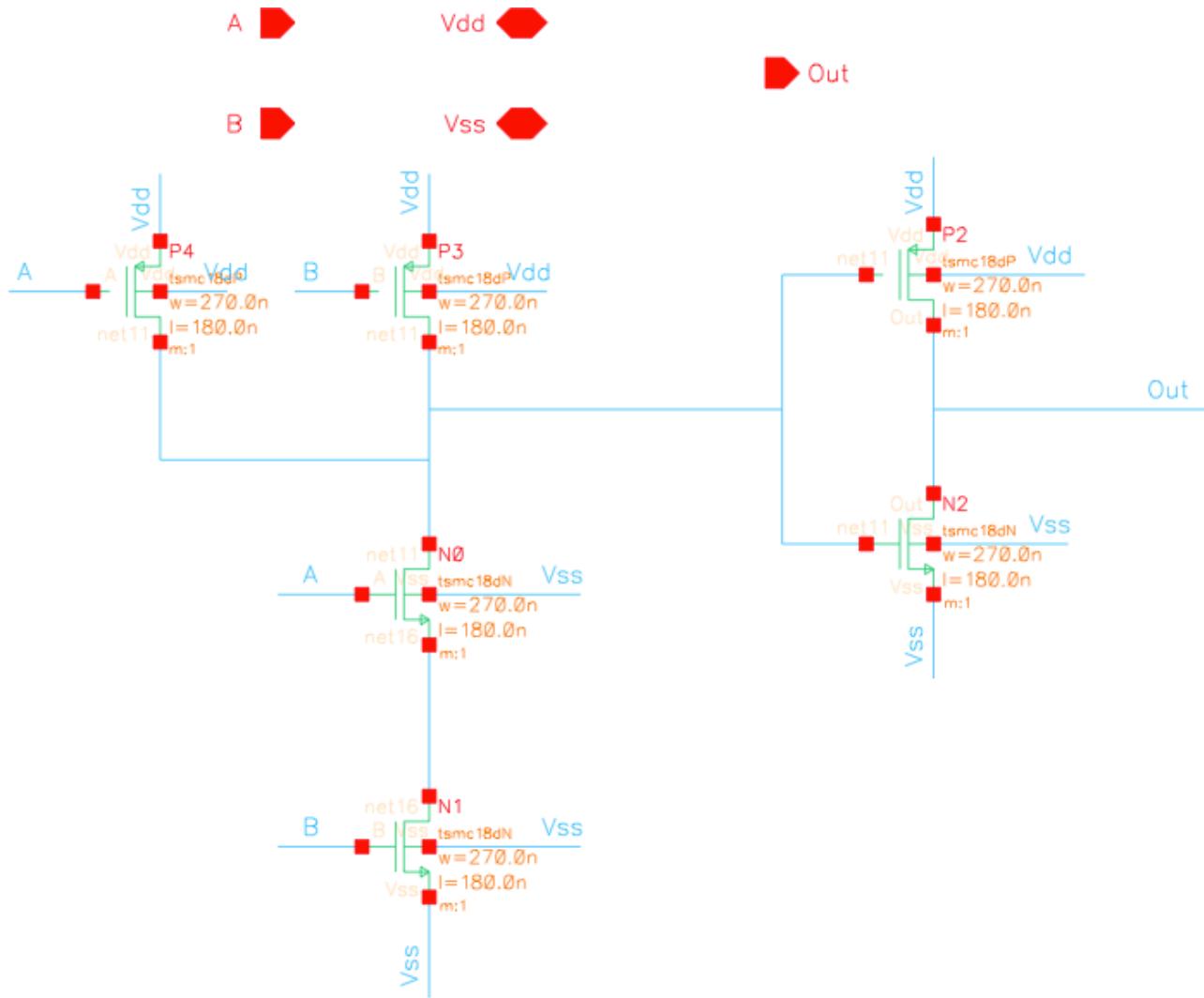


2-Input AND Gate

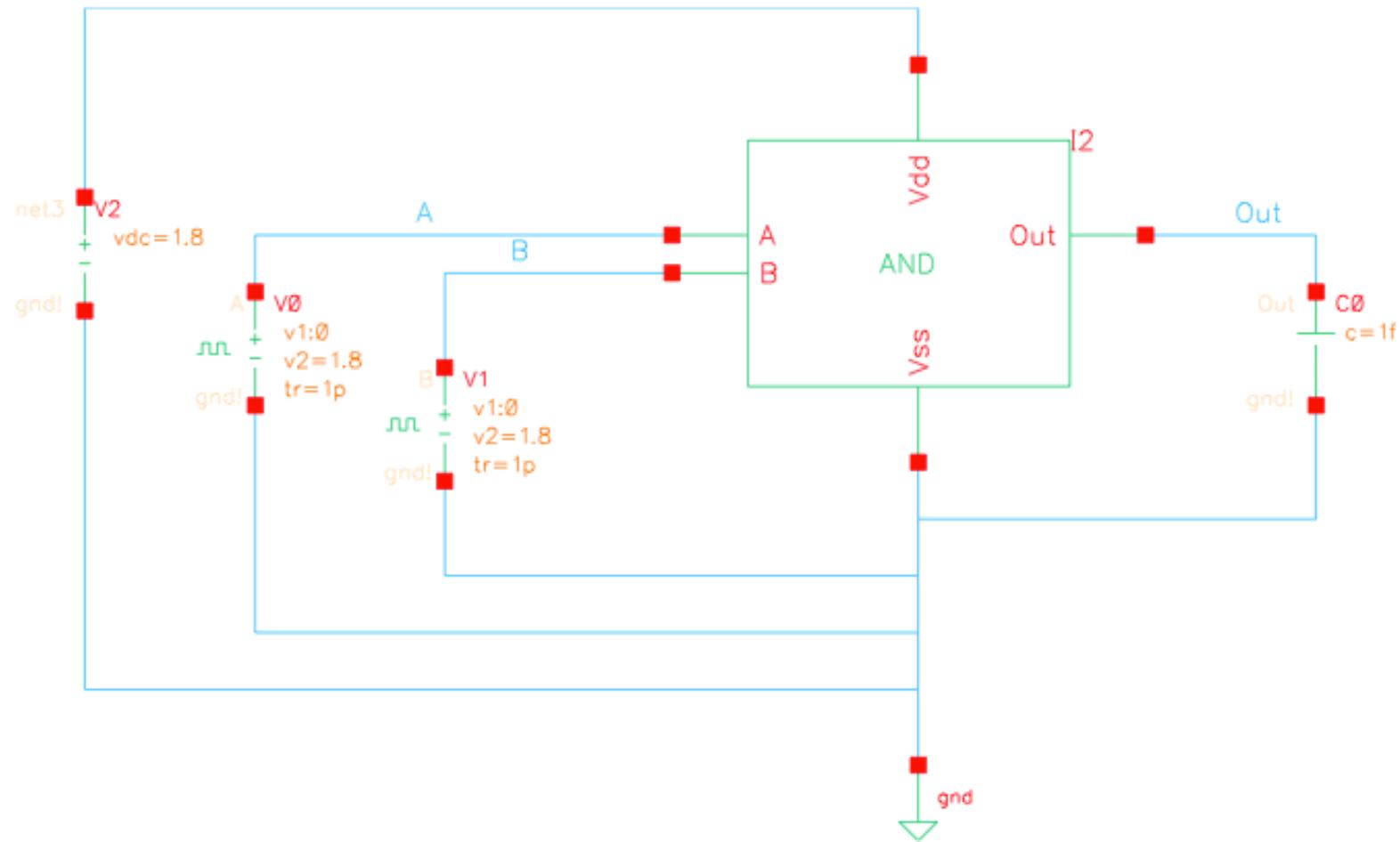
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

2-Input AND Gate Schematic



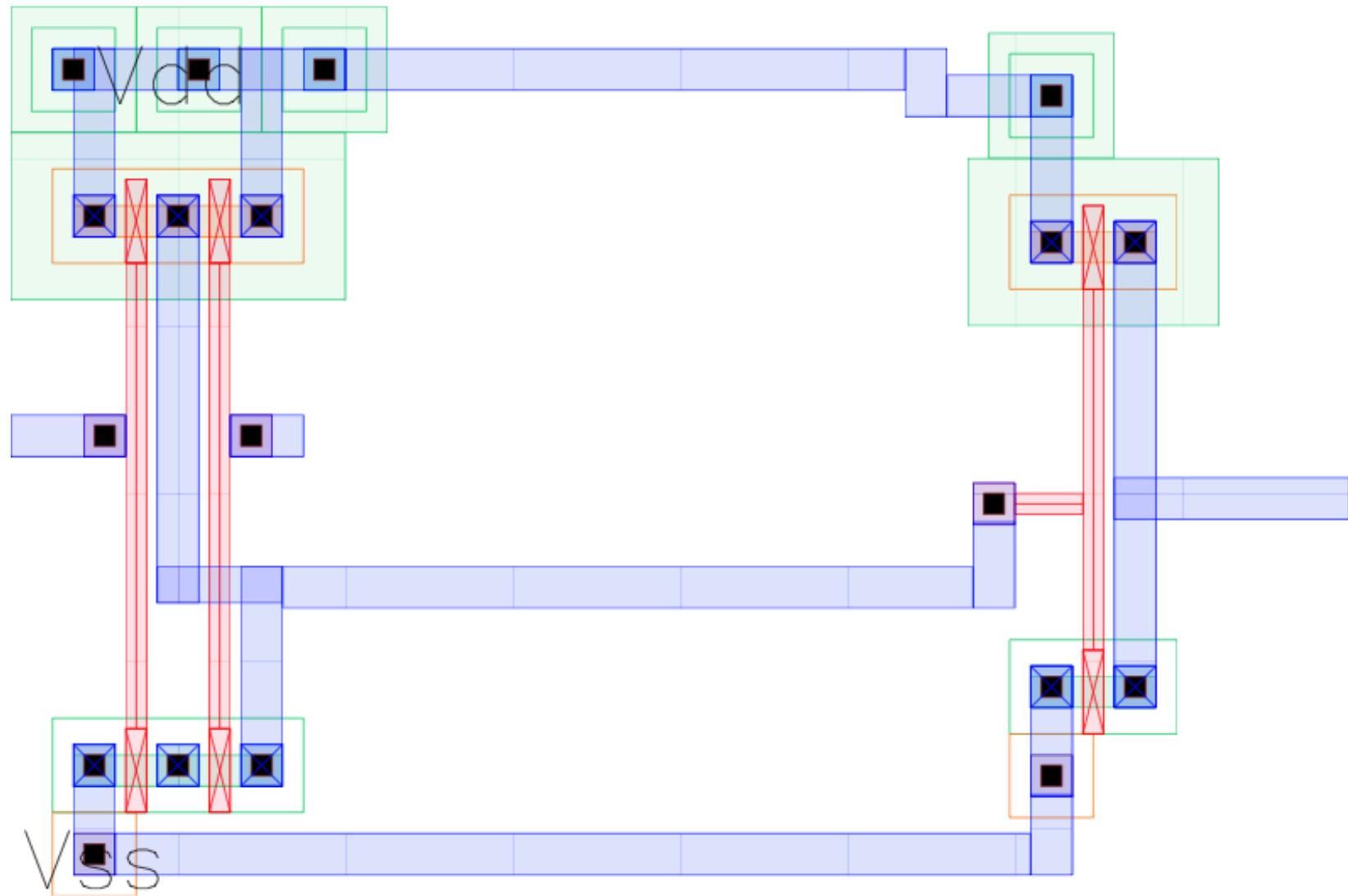
2-Input AND Gate Testbench



2-Input AND Gate Testbench Waveform



2-Input AND Gate Layout



2-Input AND Gate DRC

```
Validating hierarchy instantiation for:  
library: project2  
cell:    2AND_REAL_LAYOUT  
view:    layout  
Rules come from library NCSU_TechLib_tsmc02d.  
Rules path is divaDRC.rul.  
Inclusion limit is set to 1000.  
Running layout DRC analysis  
Flat mode  
Full checking.  
DRC started.....Fri May  4 17:43:36 2018  
completed ....Fri May  4 17:43:36 2018  
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "2AND_REAL_LAYOUT layout" *****  
Total errors found: 0
```

2-Input AND Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count

7	nets
0	terminals
3	pmos
3	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count

7	nets
5	terminals
3	pmos
3	nmos

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7

total	7	7
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

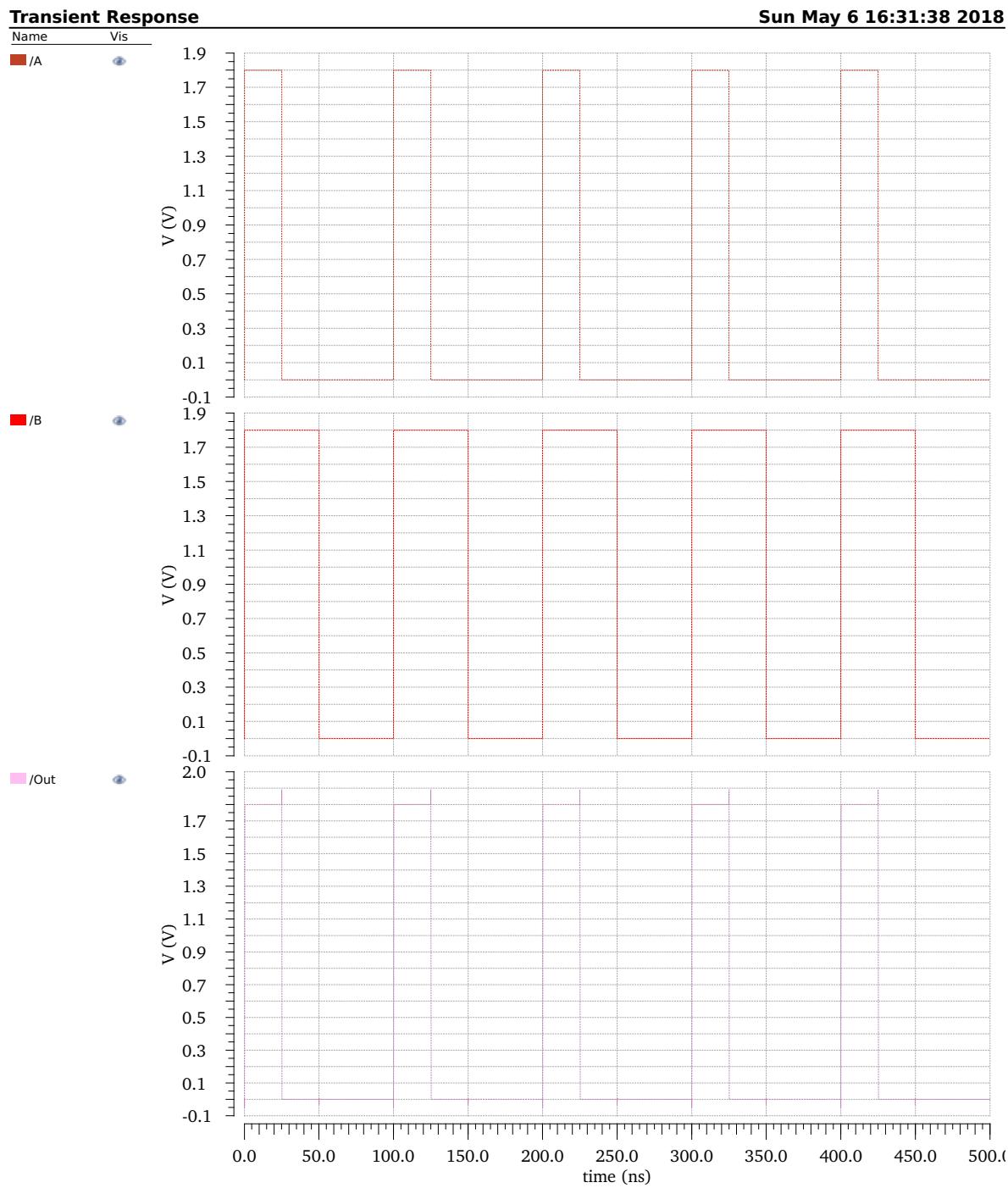
prunedev.out:

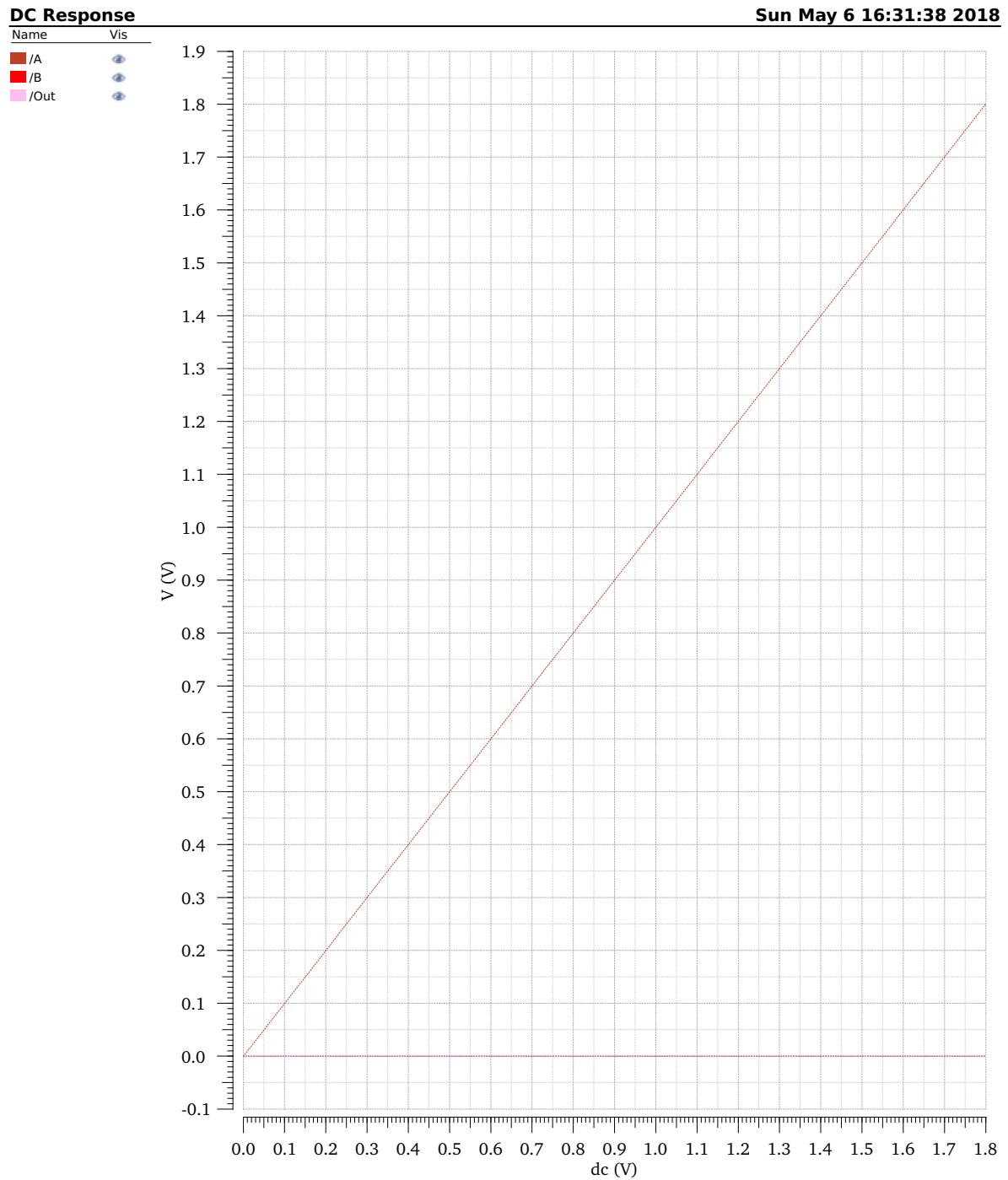
audit.out:

2-Input AND Gate Post Layout

project2:2AND_REAL_tb:1 : project2 2AND_REAL_tb schematic

16:32:26 Sun May 6 2018

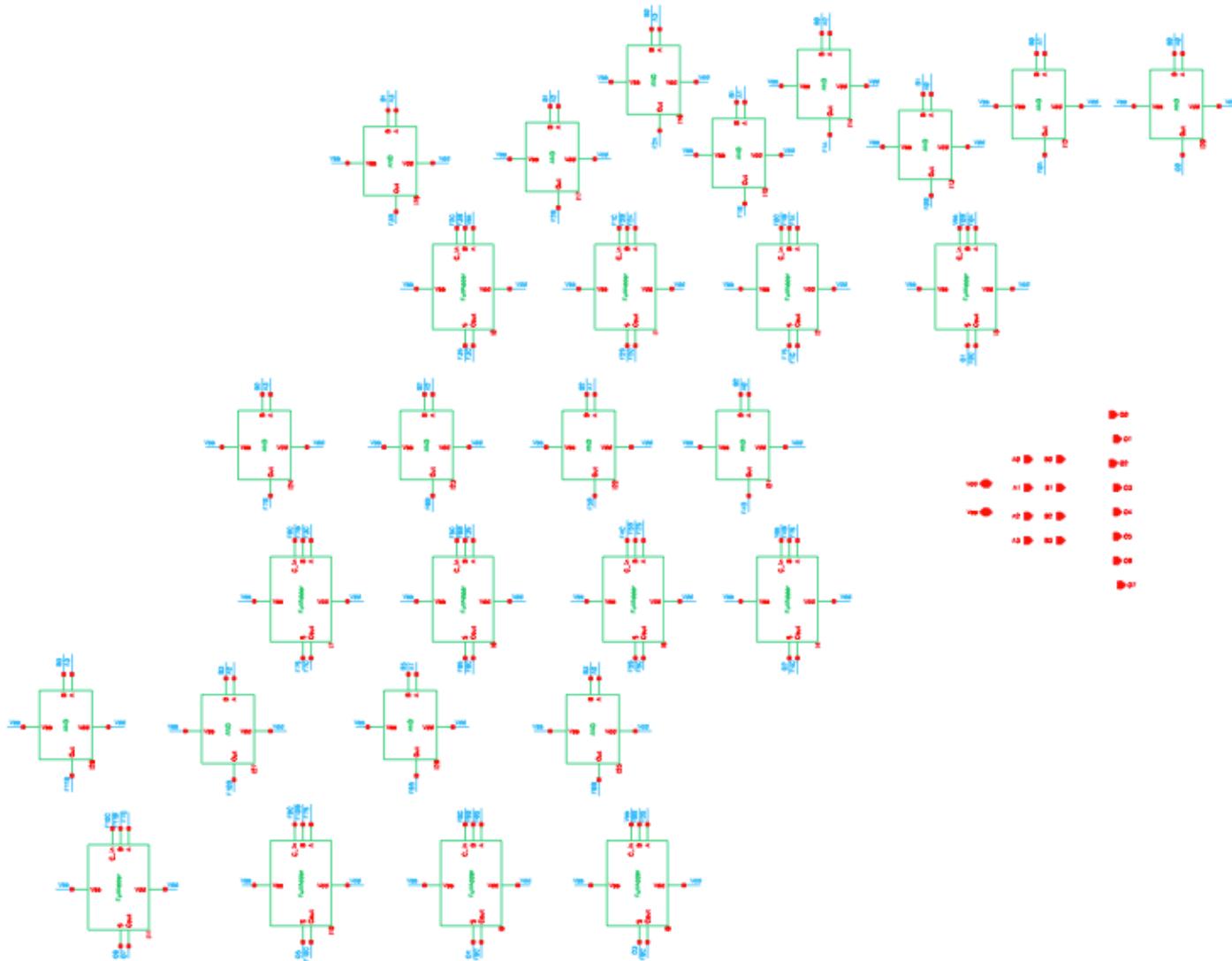




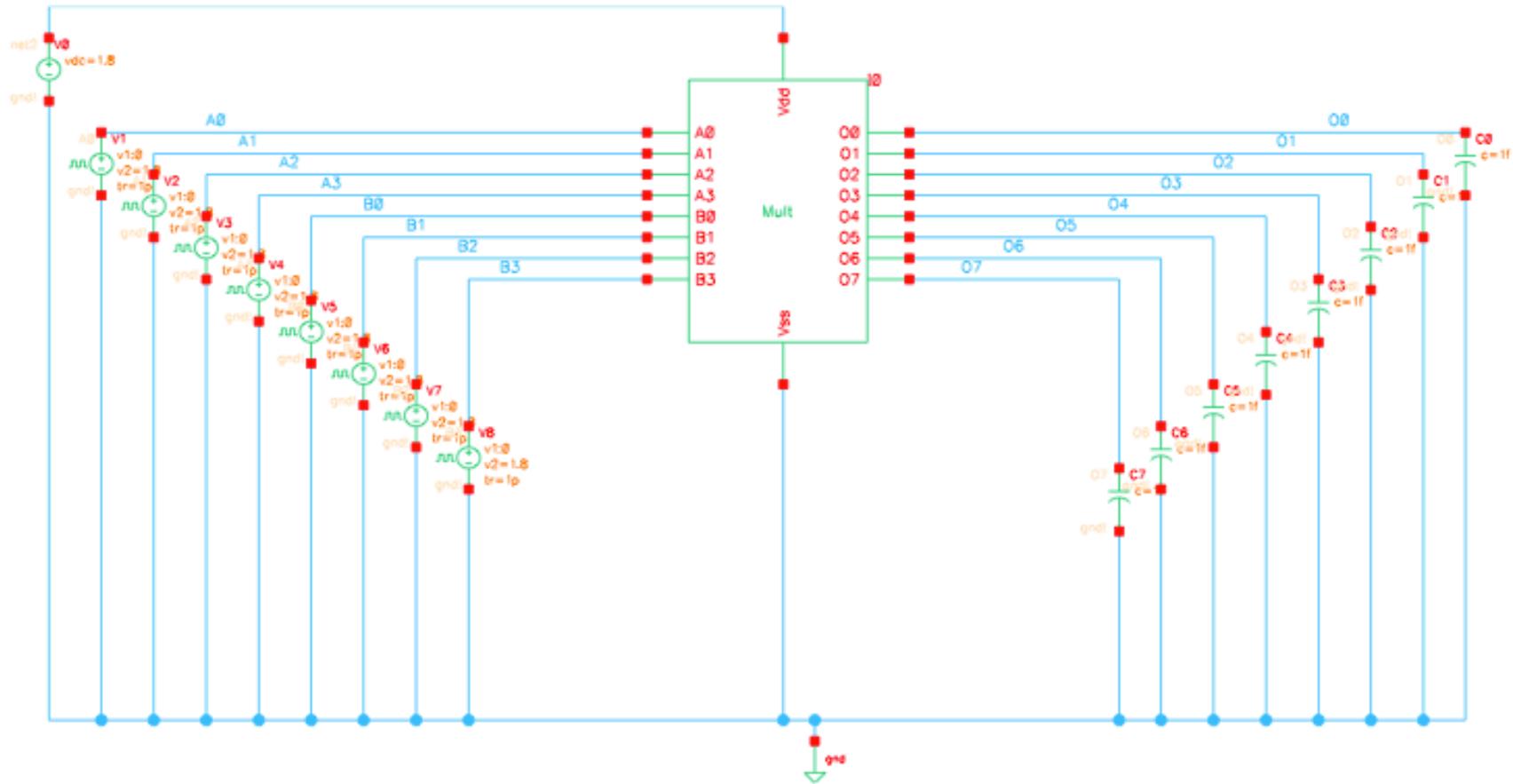
Multiplier

Contains AND Gate and Full Adder

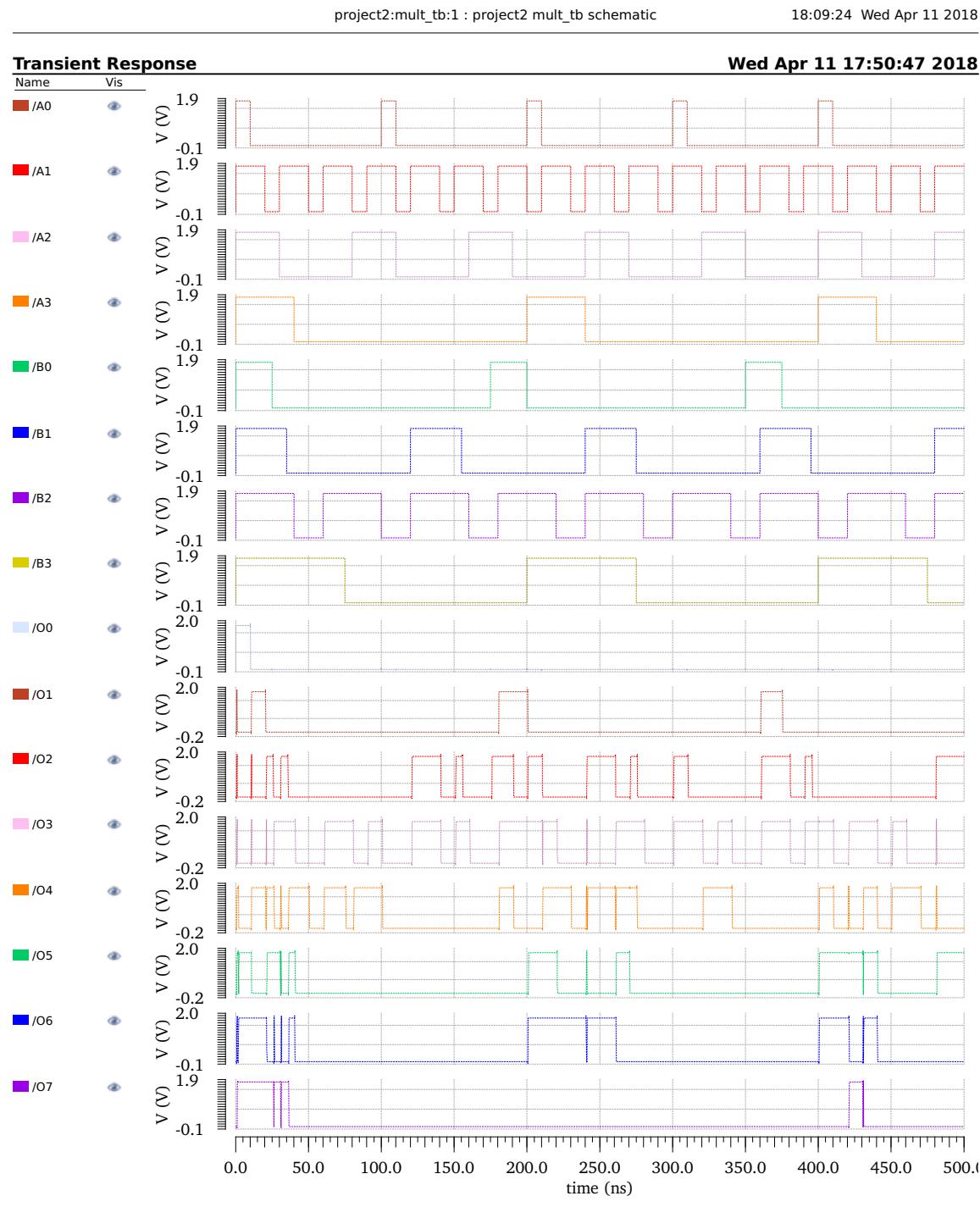
Multiplier Schematic



Multiplier Testbench



Multiplier Testbench Waveform



Multiplier Layout

Multiplier DRC

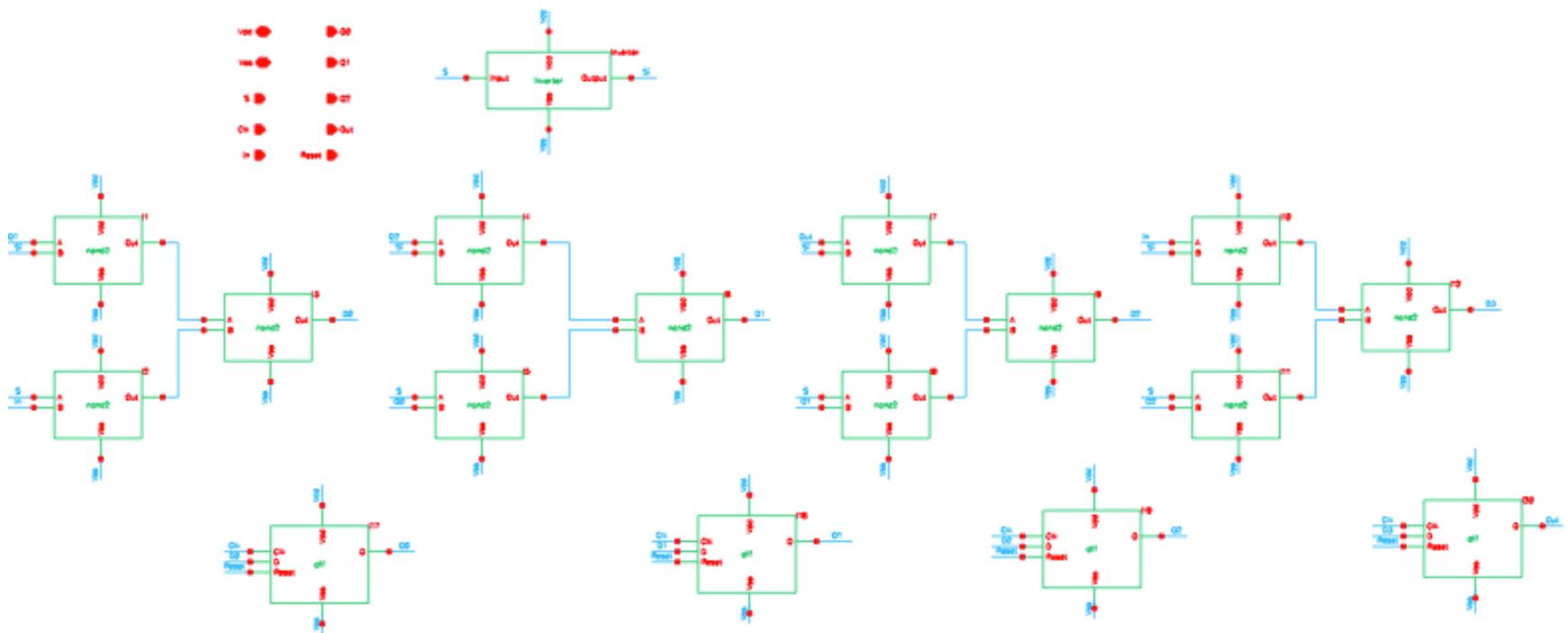
Multiplier LVS

Multiplier Post-Layout

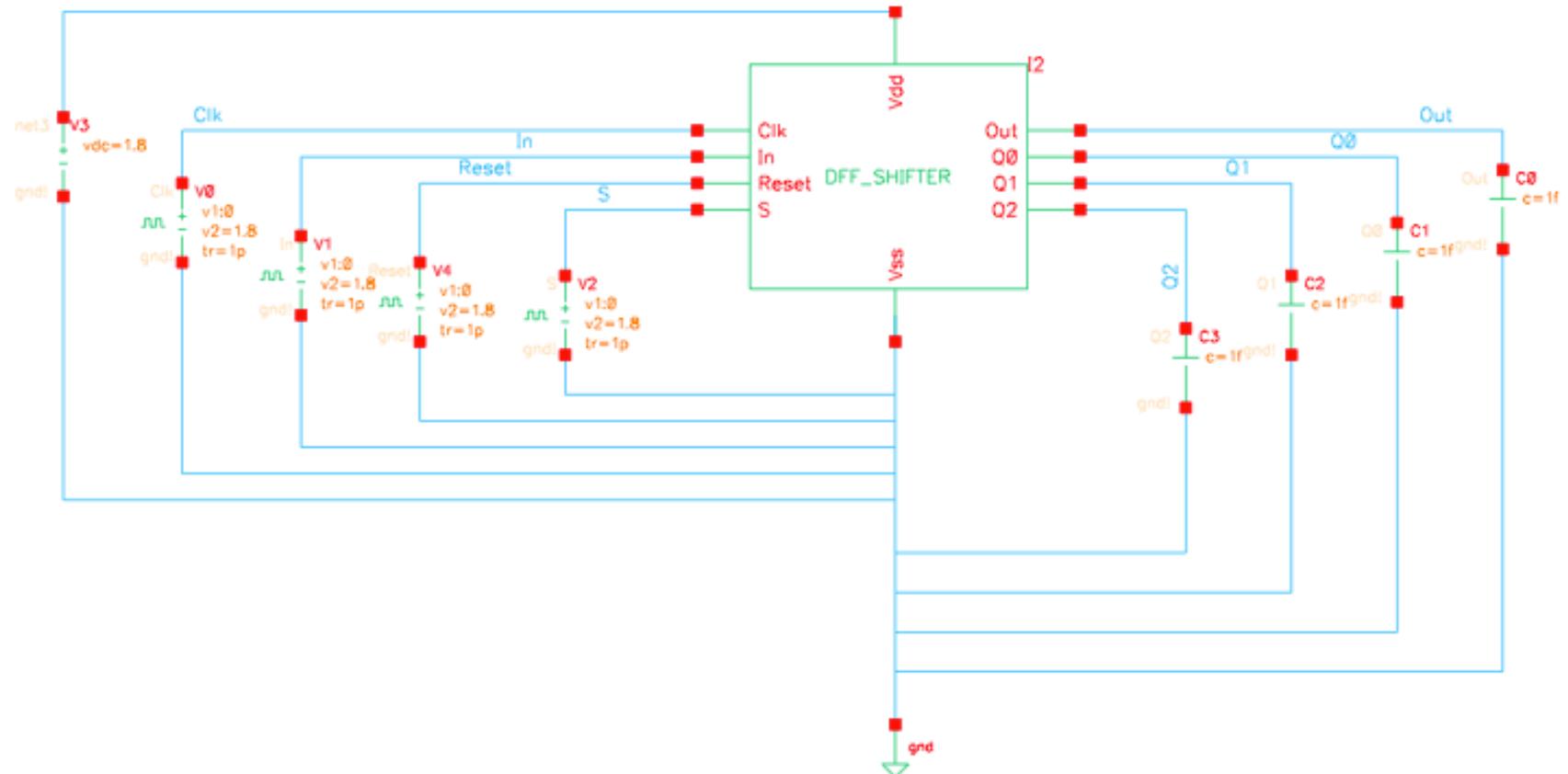
Bi-Directional Shifter

2-Input NAND, Inverter, D-Flip Flop

Bi-Directional Shifter Schematic



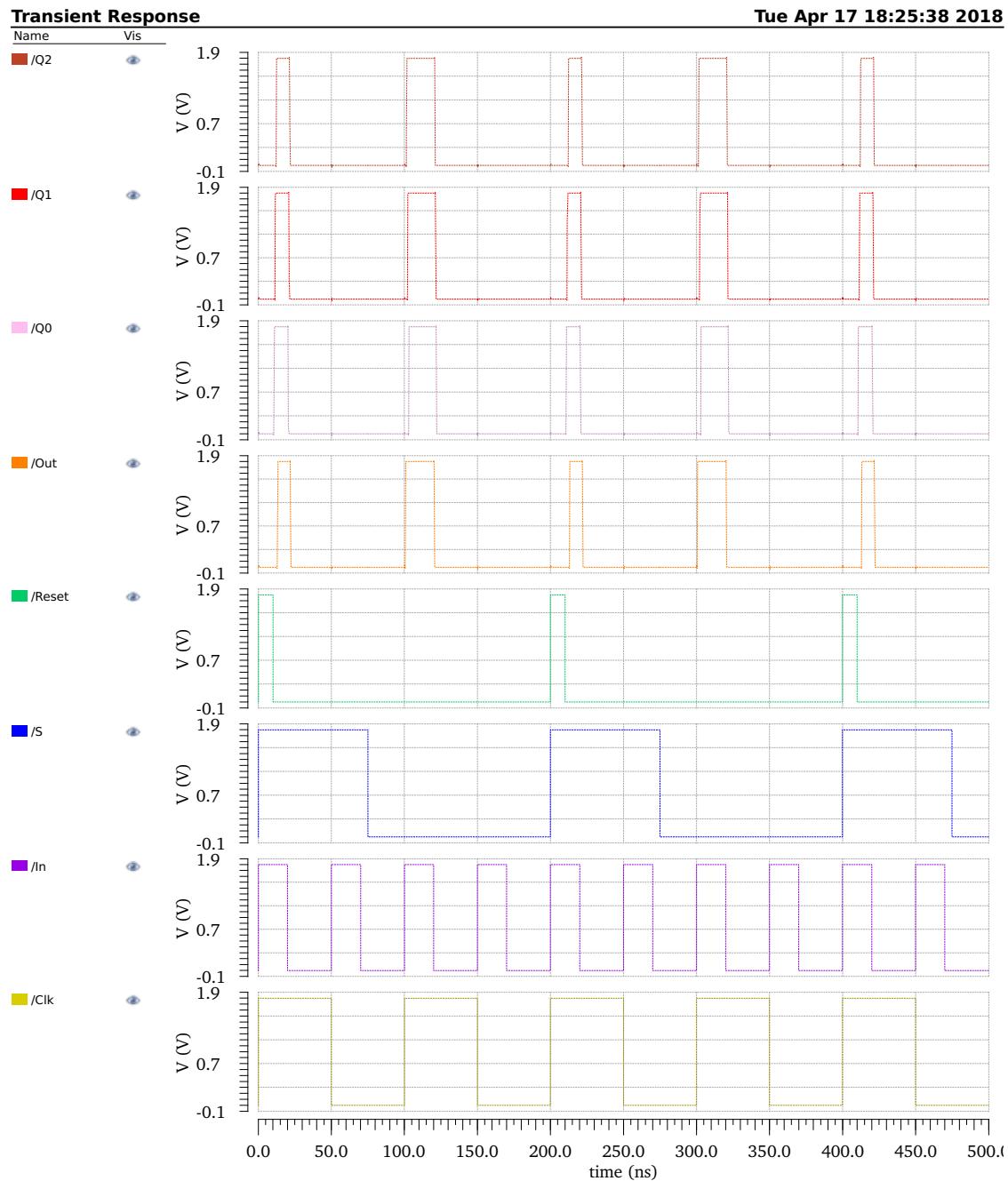
Bi-Directional Shifter Testbench



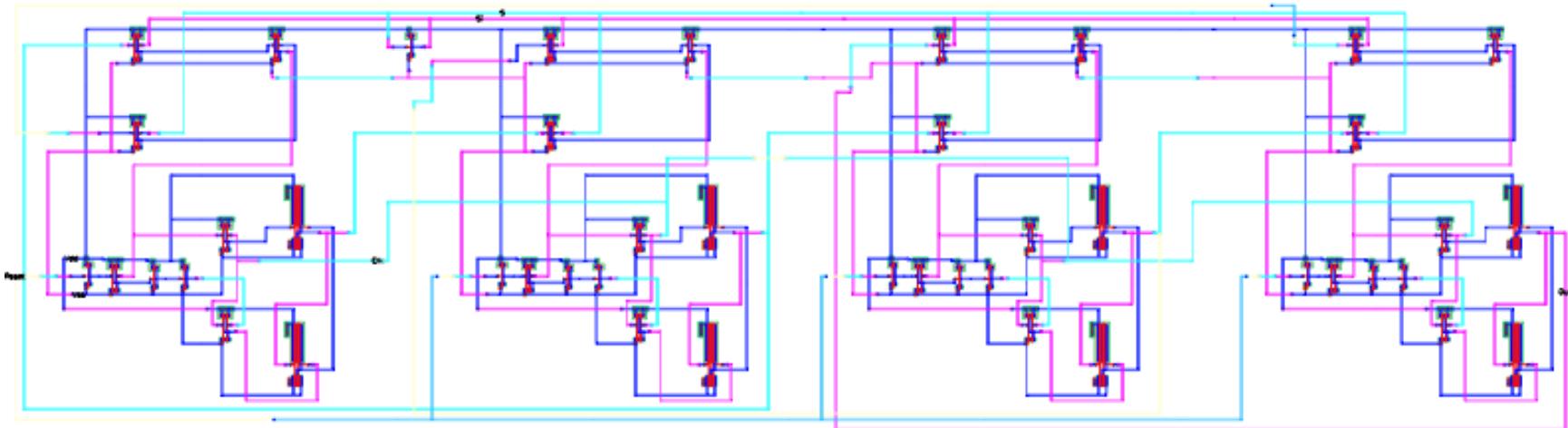
Bi-Directional Shifter Testbench Waveform

project2:shifter_tb:1 : project2 shifter_tb schematic

18:26:57 Tue Apr 17 2018



Bi-Directional Shifter Layout



Bi-Directional Shifter DRC

```
DRC started at Sun May  6 21:08:44 2018

Validating hierarchy instantiation for:
library: project2
cell:    shifter_tb
view:   layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Sun May  6 21:08:44 2018
completed ....Sun May  6 21:08:44 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*****      Summary of rule violations for cell "shifter_tb layout"      *****
Total errors found: 0
```

Bi-Directional Shifter LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
83	nets
0	terminals
77	pmos
77	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
83	nets
10	terminals
77	pmos
77	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	154	154
total	154	154

	nets	
un-matched	0	0
merged	0	0

pruned	0	0
active	83	83
total	83	83

terminals		
un-matched	0	0
matched but		
different type	0	0
total	0	10

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

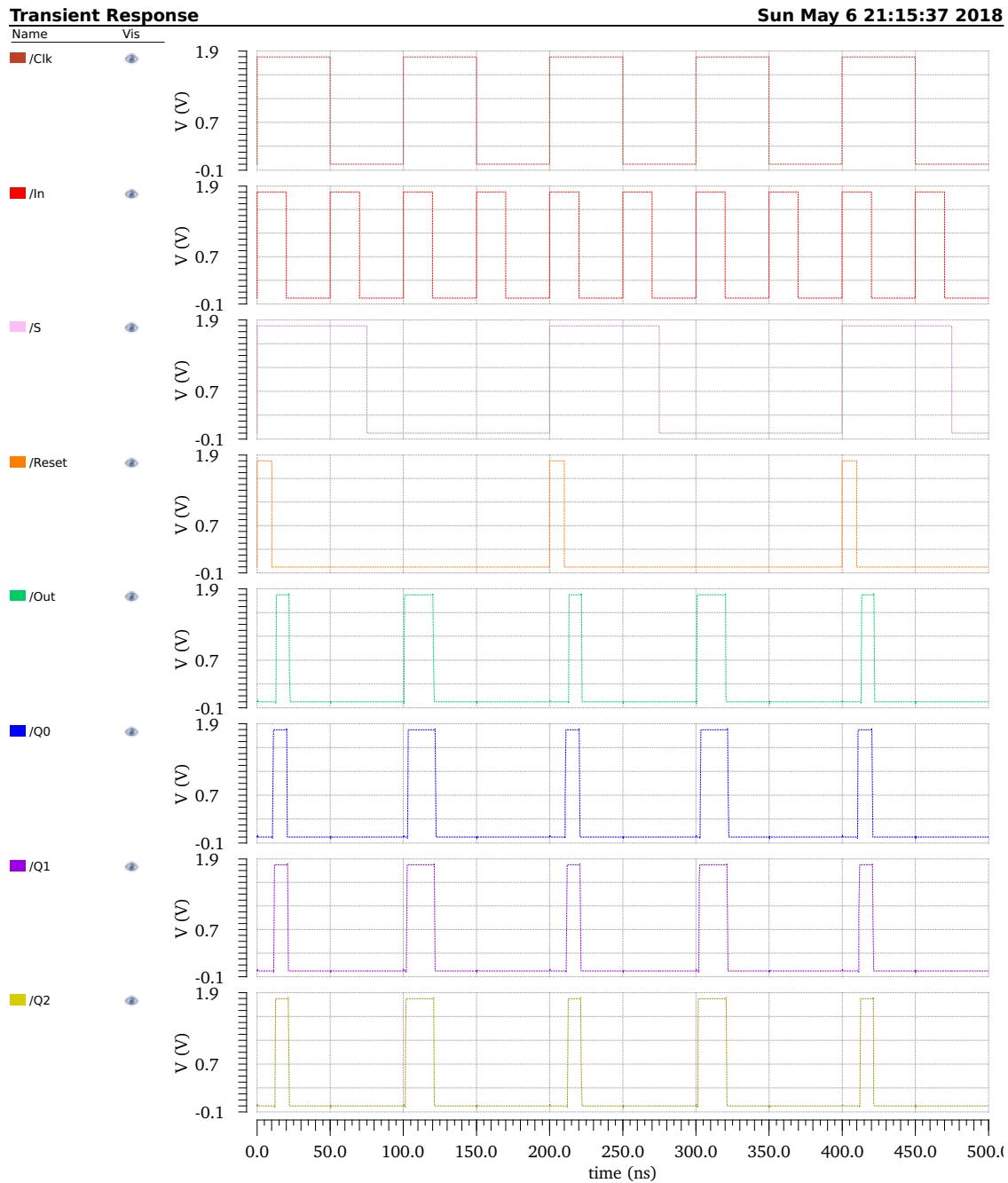
prunedev.out:

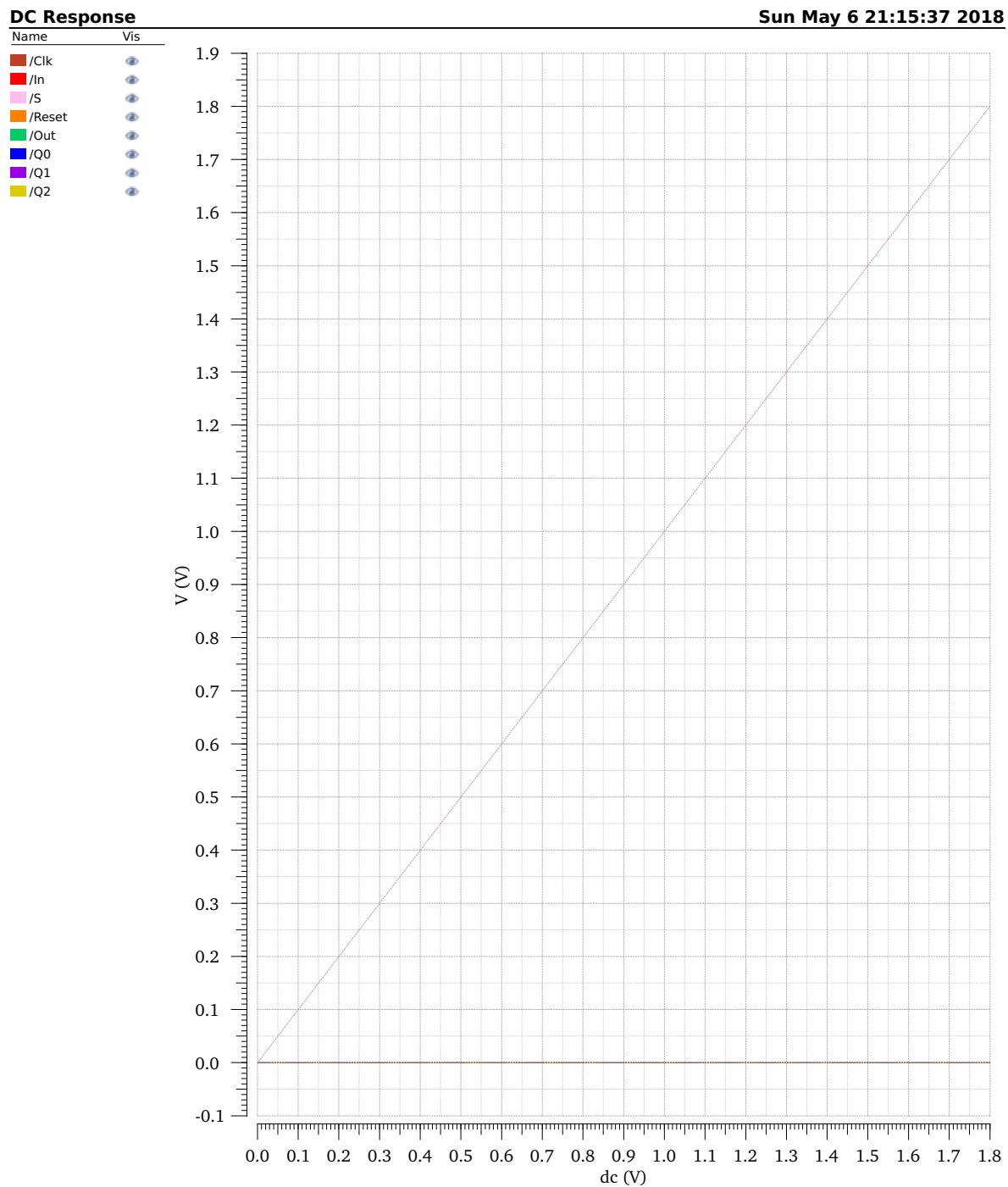
audit.out:

Bi-Directional Shifter Post-Layout

project2:shifter_tb:1 : project2 shifter_tb schematic

21:16:00 Sun May 6 2018



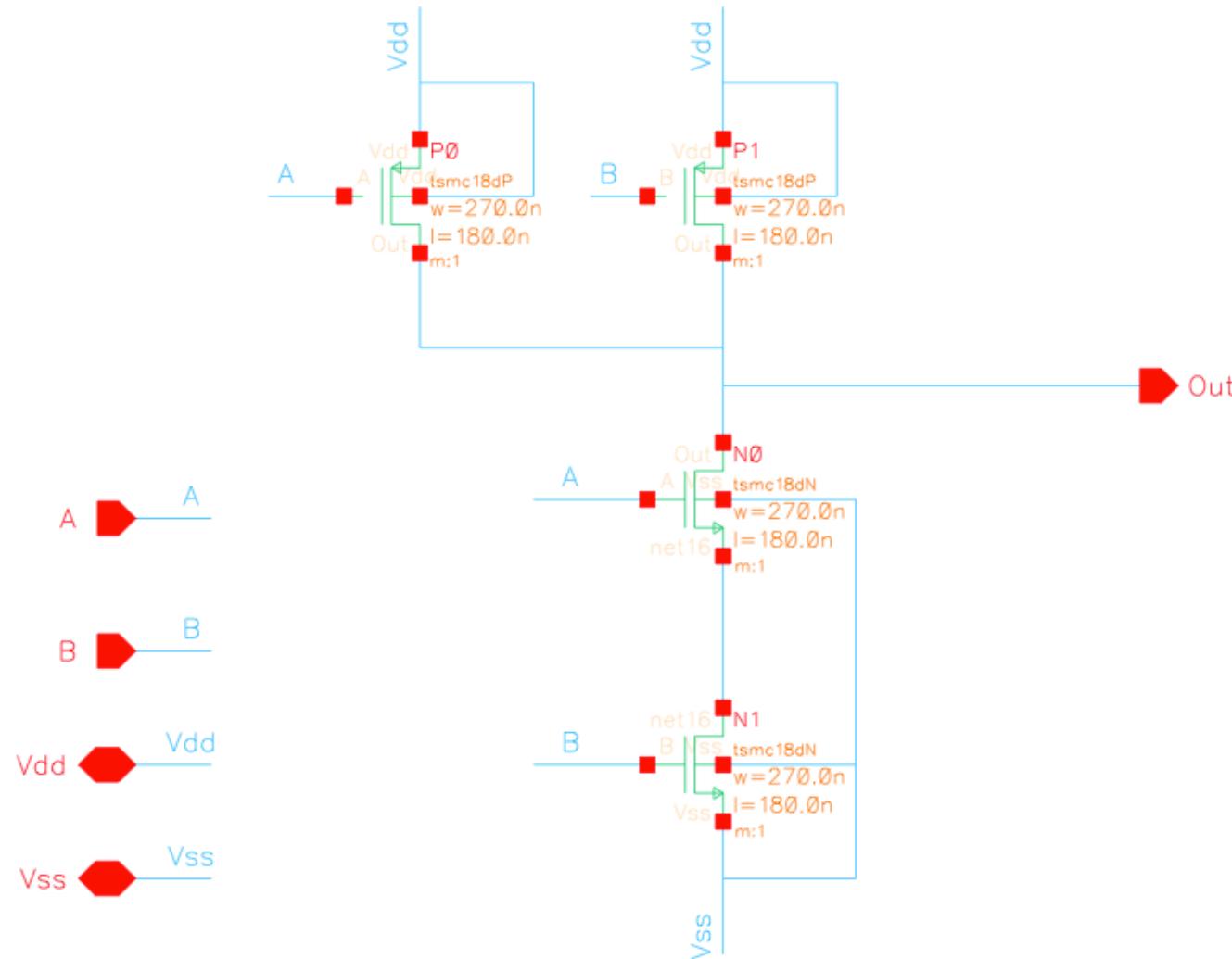


2-Input NAND Gate

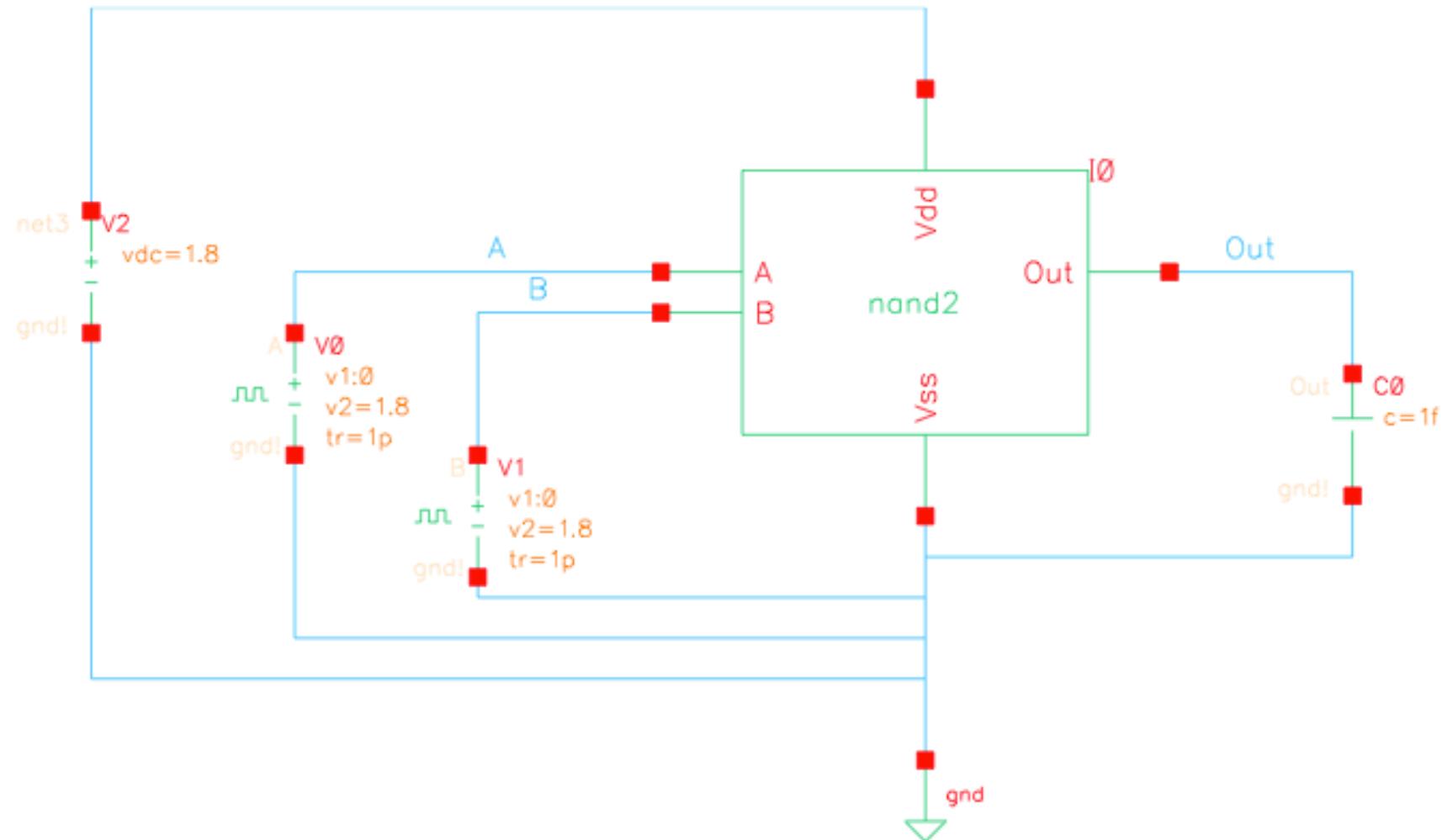
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

2-Input NAND Gate Schematic



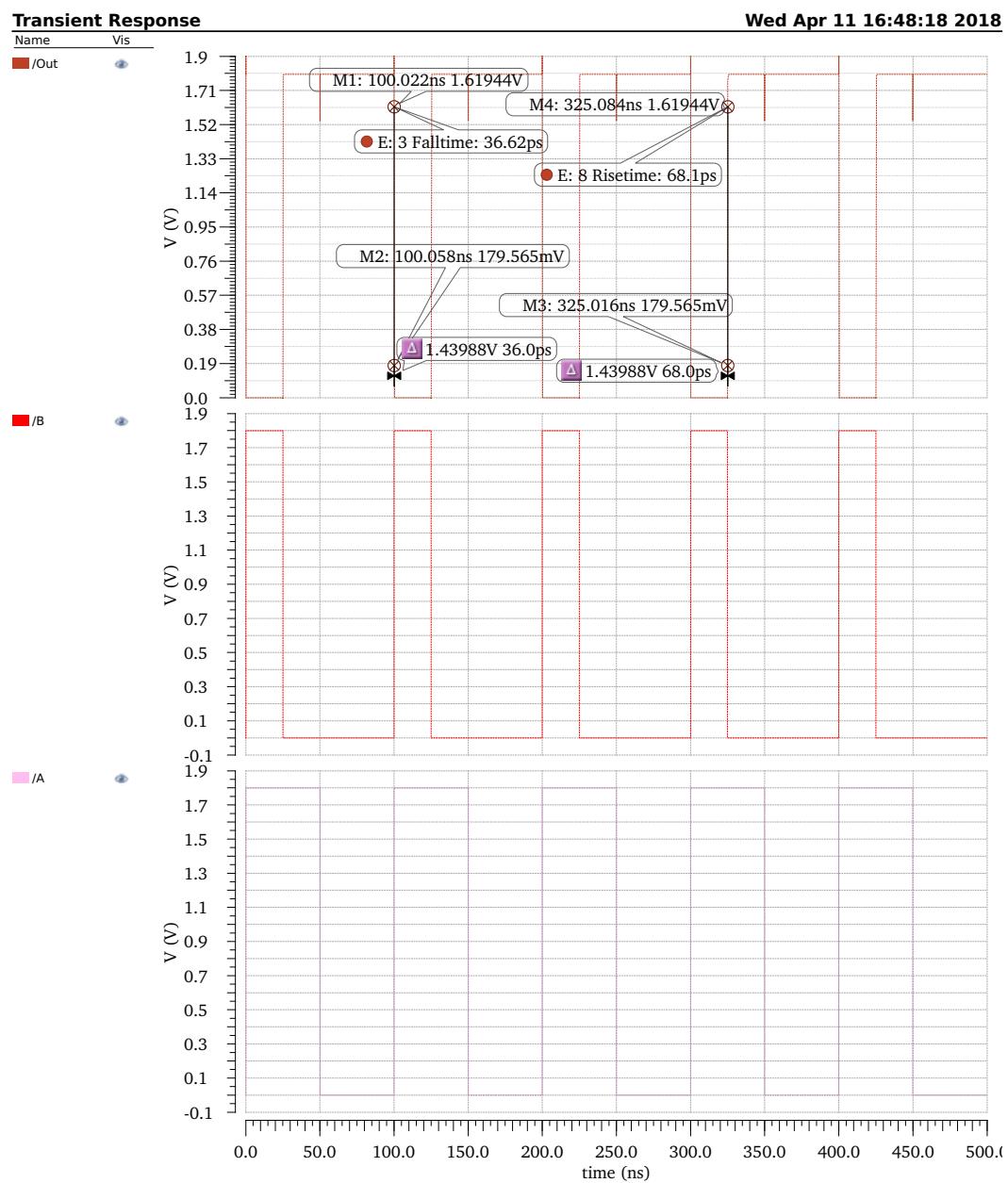
2-Input NAND Gate Testbench



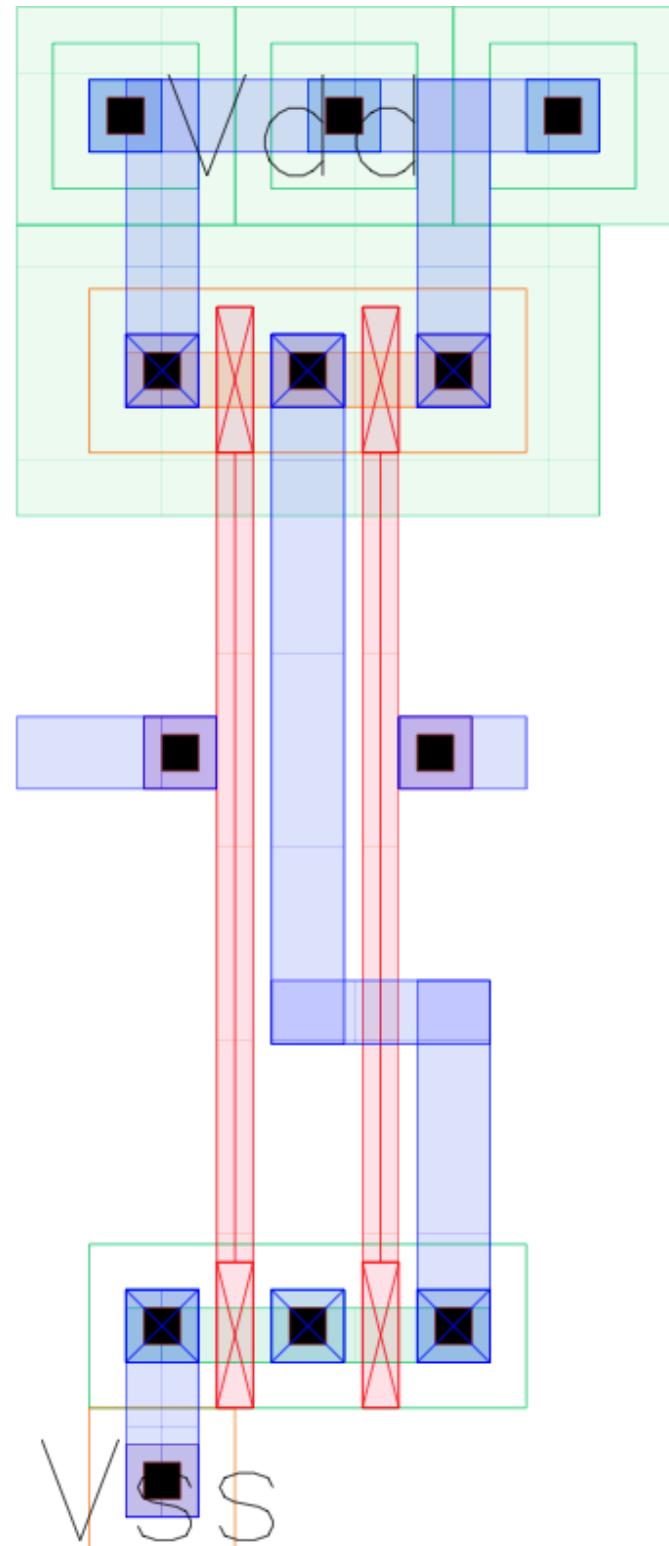
2-Input NAND Gate Testbench Waveform

project2:nand2_tb:1 : project2 nand2_tb schematic

16:52:05 Wed Apr 11 2018



2-Input NAND Gate Layout



2-Input NAND Gate DRC

```
Getting layout property bag
DRC started at Fri May  4 17:27:41 2018

Validating hierarchy instantiation for:
library: project2
cell:    nand2_layout
view:   layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Fri May  4 17:27:41 2018
completed ....Fri May  4 17:27:41 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*****      Summary of rule violations for cell "nand2_layout layout"      *****
Total errors found: 0
```

2-Input NAND Gate LVS

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout /gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
6	nets
0	terminals
2	pmos
2	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

layout	schematic
instances	
un-matched	0 0
rewired	0 0
size errors	0 0
pruned	0 0
active	4 4
total	4 4

nets	
un-matched	0 0

```
merged          0  0
pruned          0  0
active          6  6
total           6  6
```

```
terminals
un-matched      0  0
matched but
different type   0  0
total            0  5
```

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

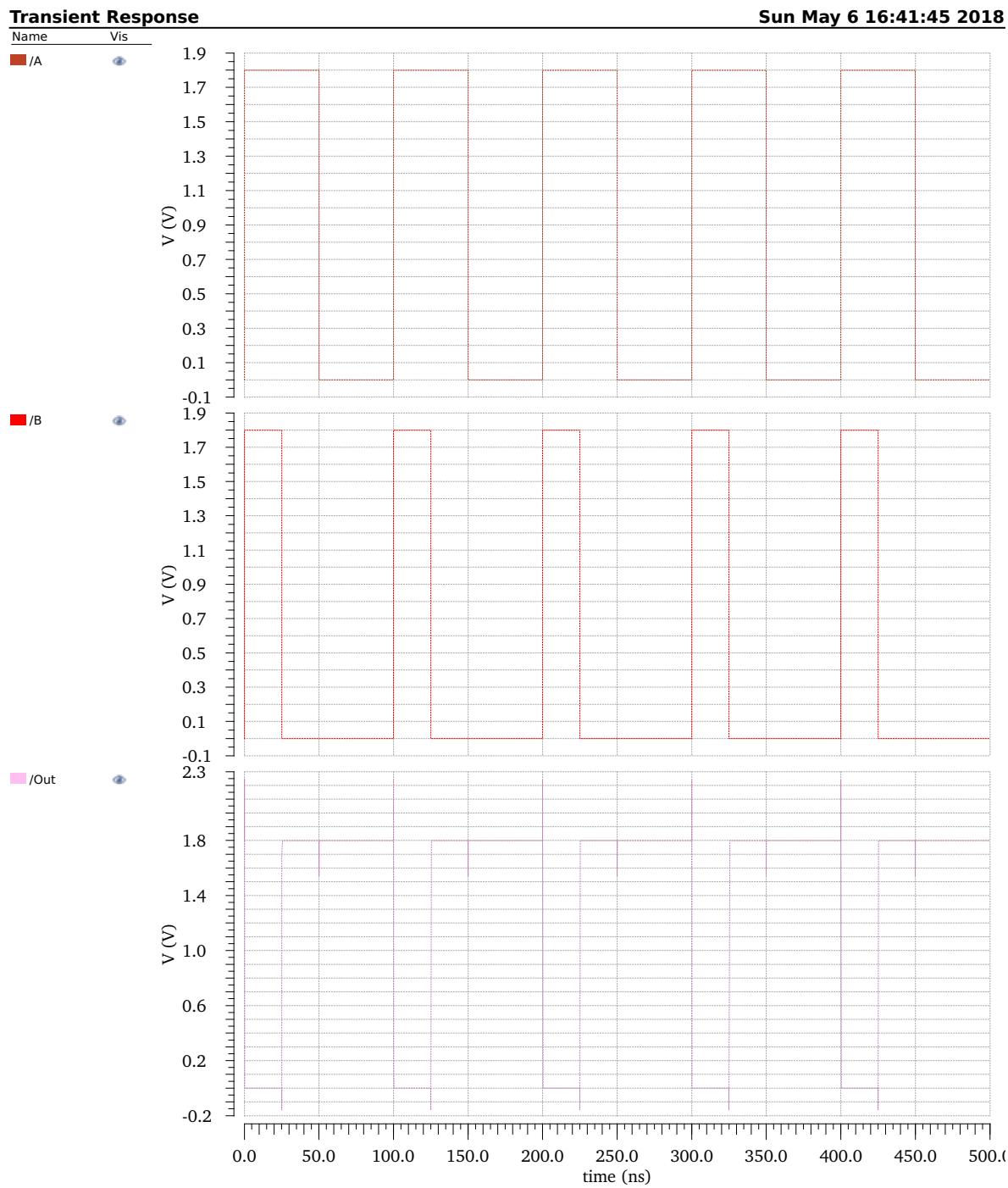
prunedev.out:

audit.out:

2-Input NAND Gate Post-Layout

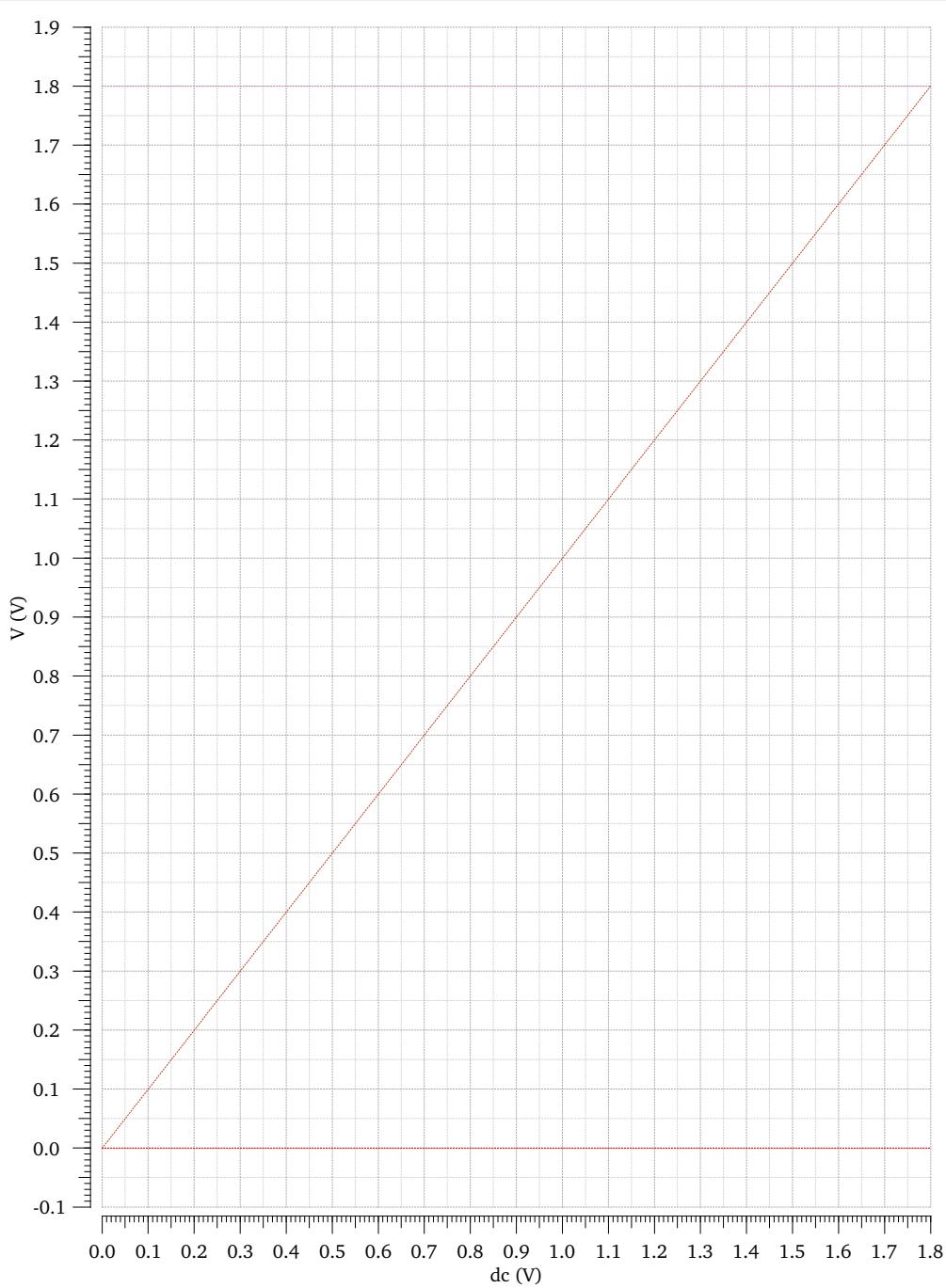
project2:nand2_tb:1 : project2 nand2_tb schematic

16:42:17 Sun May 6 2018



DC Response**Sun May 6 16:41:45 2018**

Name	Vis
/A	●
/B	●
/Out	●

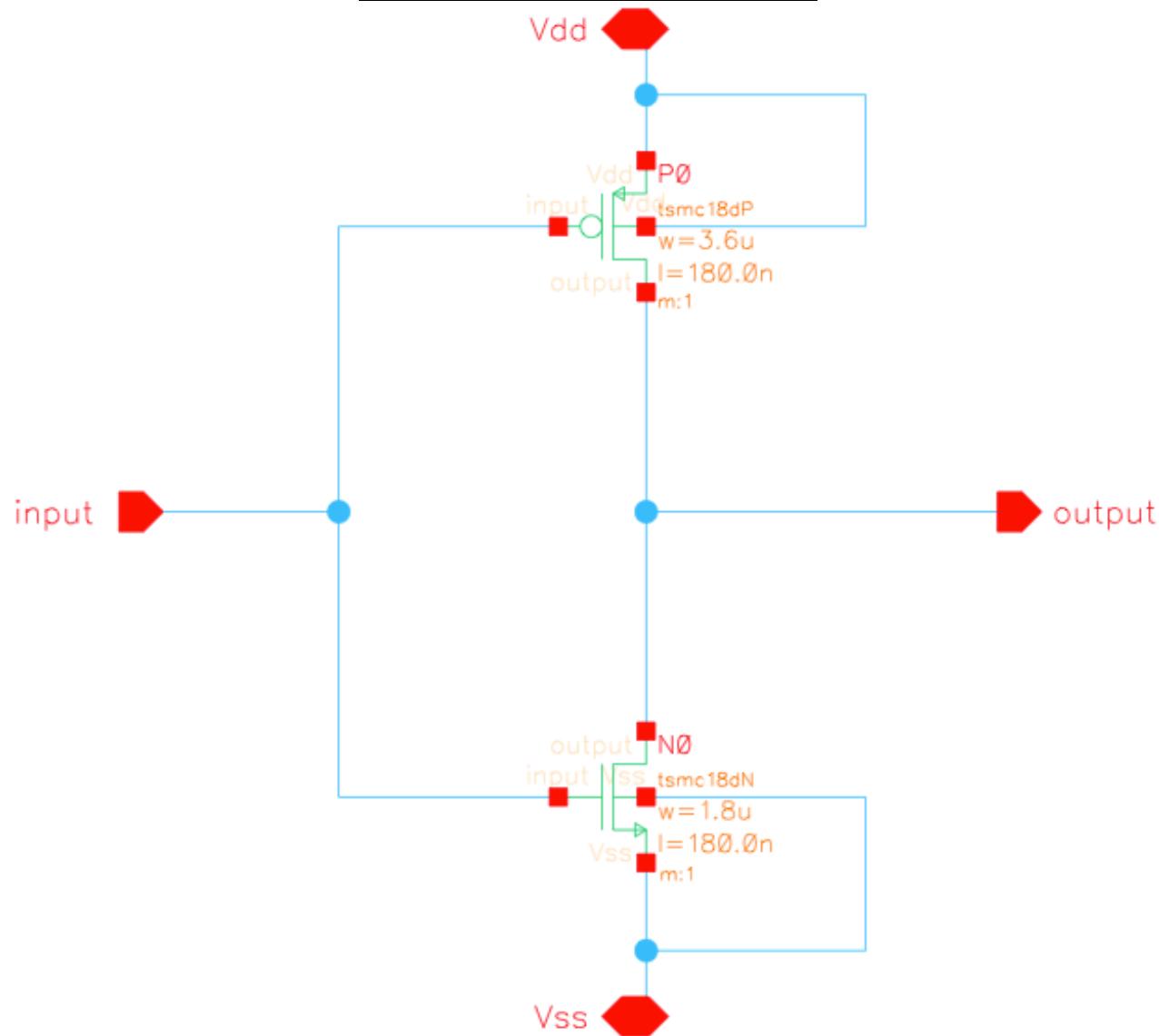


Inverter

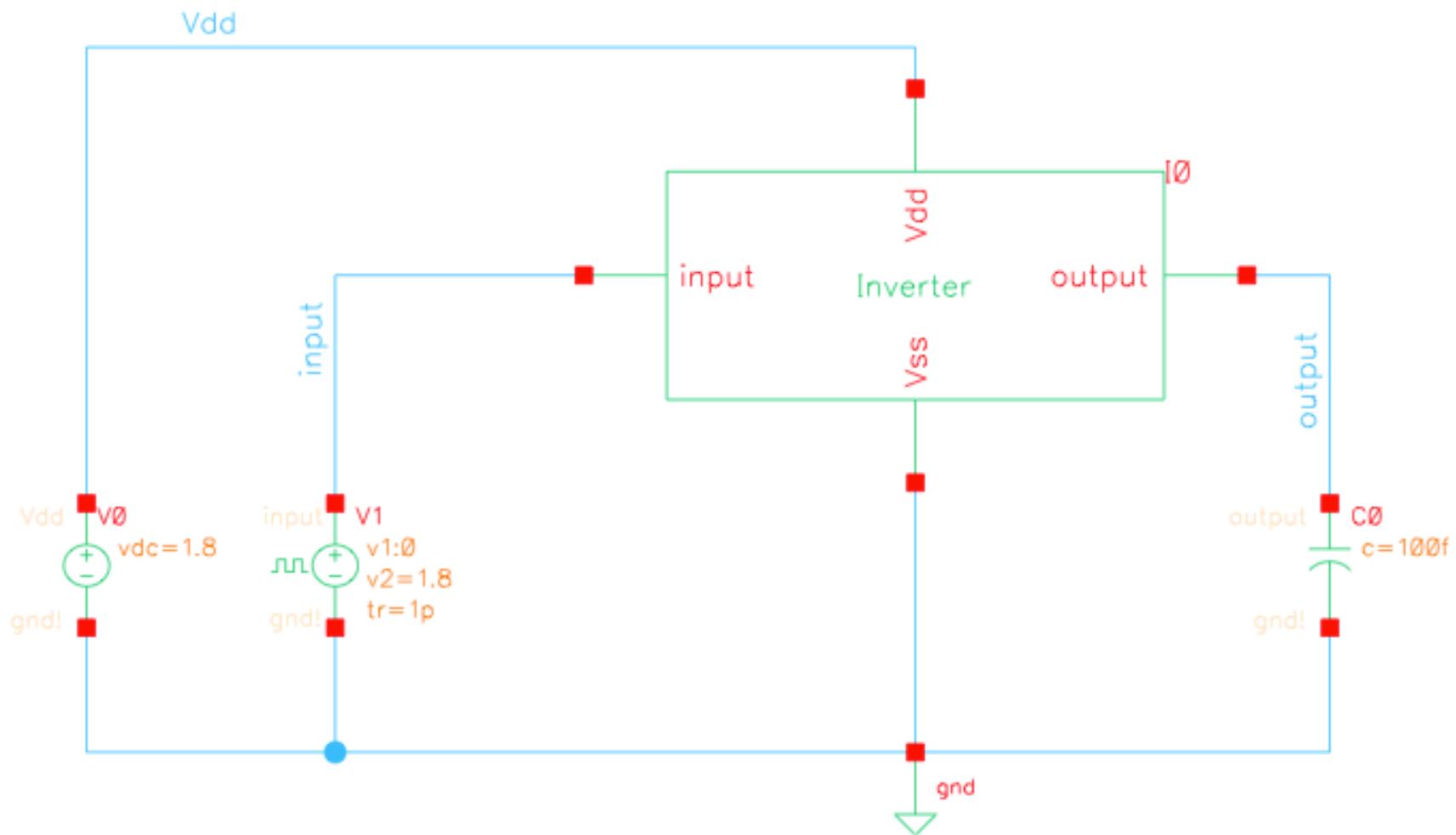
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 3.6/0.18$$

Inverter Schematic



Inverter Testbench



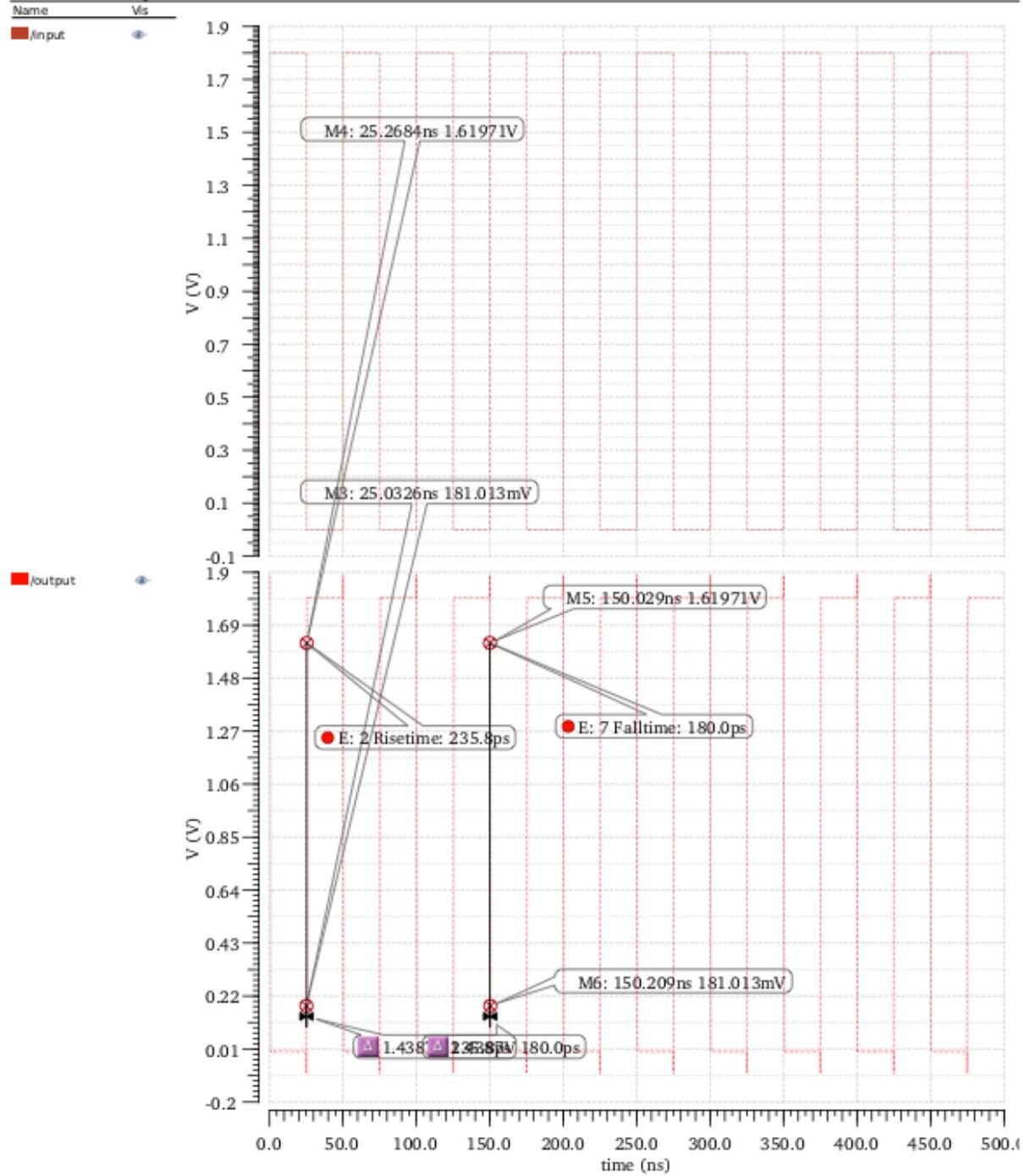
Inverter Testbench Waveform

Project1:Inverter_testbench:1 : Project1_Inverter_testbench schematic

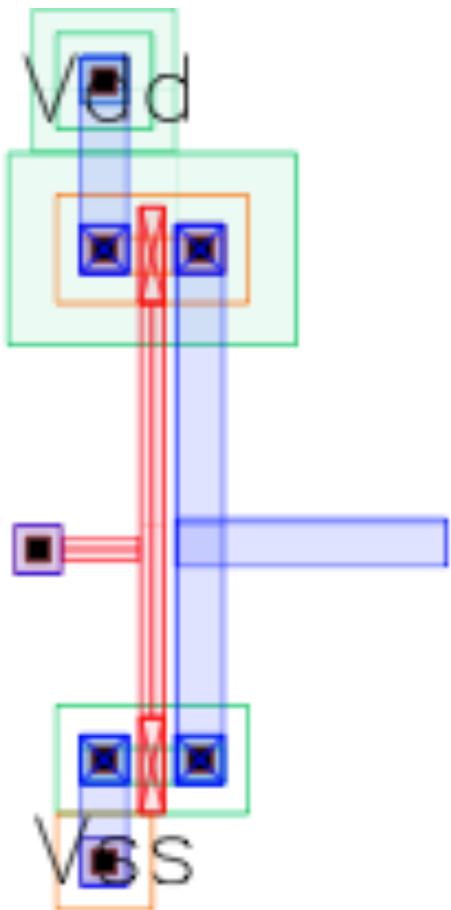
19:20:40 Wed Feb 28 2018

Transient Response

Wed Feb 28 19:14:42 2018



Inverter Layout



Inverter DRC

```
DRC started at Fri May  4 17:02:54 2018

Validating hierarchy instantiation for:
library: project2
cell:    inverter_layout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.

DRC started.....Fri May  4 17:02:54 2018
completed ....Fri May  4 17:02:54 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "inverter_layout layout" *****
Total errors found: 0
```

Inverter LVS

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout
/gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count

4	nets
0	terminals
1	pmos
1	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count

4	nets
4	terminals
1	pmos
1	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

	nets	
un-matched	0	0
merged	0	0

```
pruned      0  0
active      4  4
total       4  4
```

```
          terminals
un-matched   0  0
matched but
different type 0  0
total        0  4
```

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

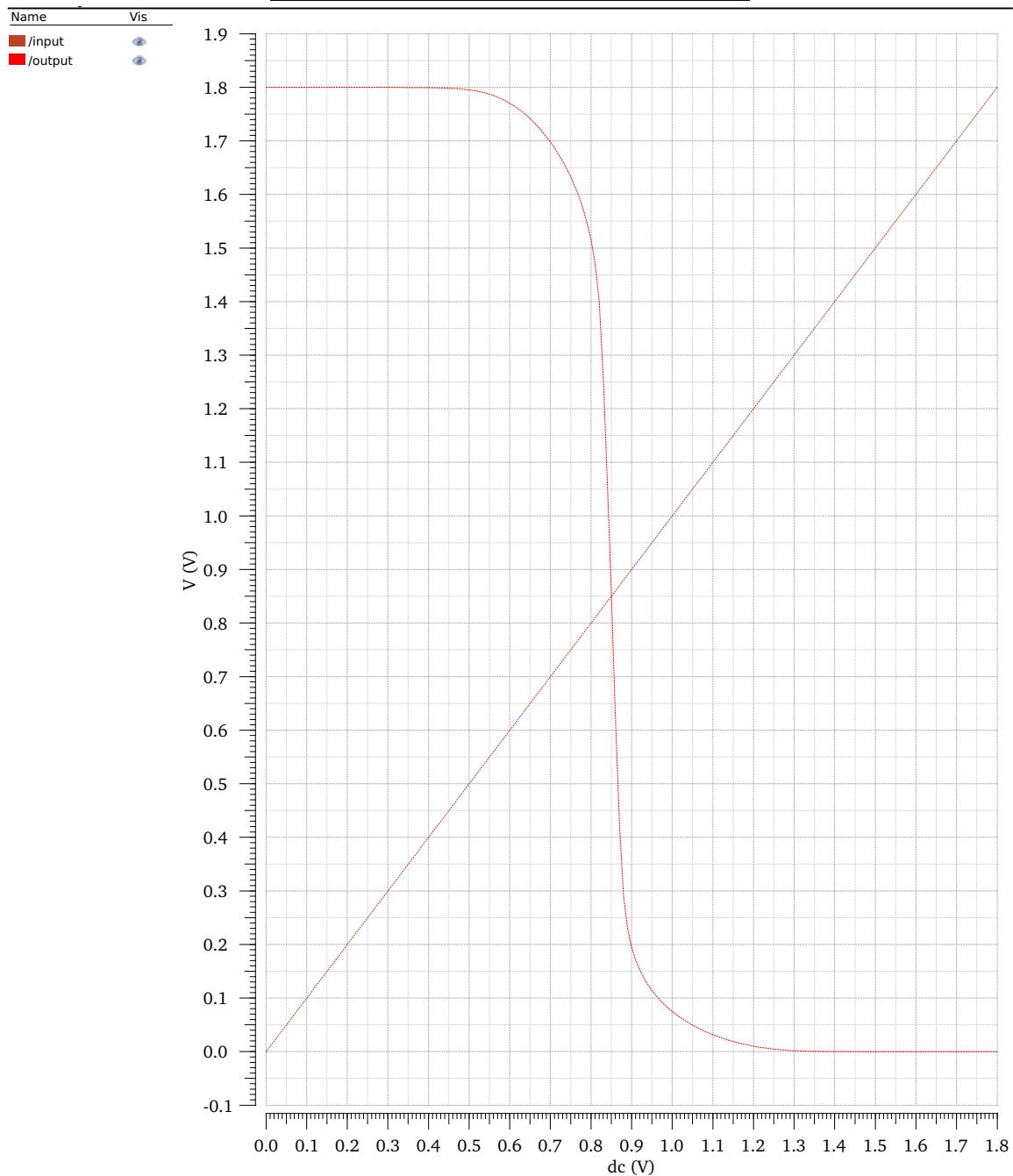
termbad.out:

prunenet.out:

prunedev.out:

audit.out:

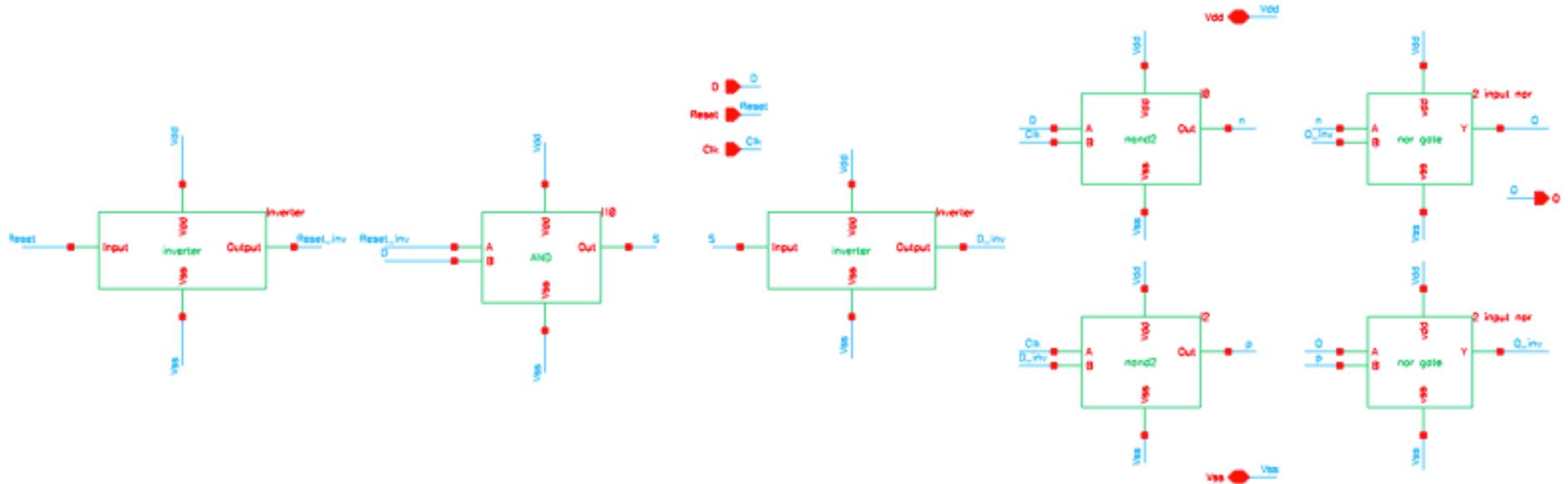
Inverter Post-Layout



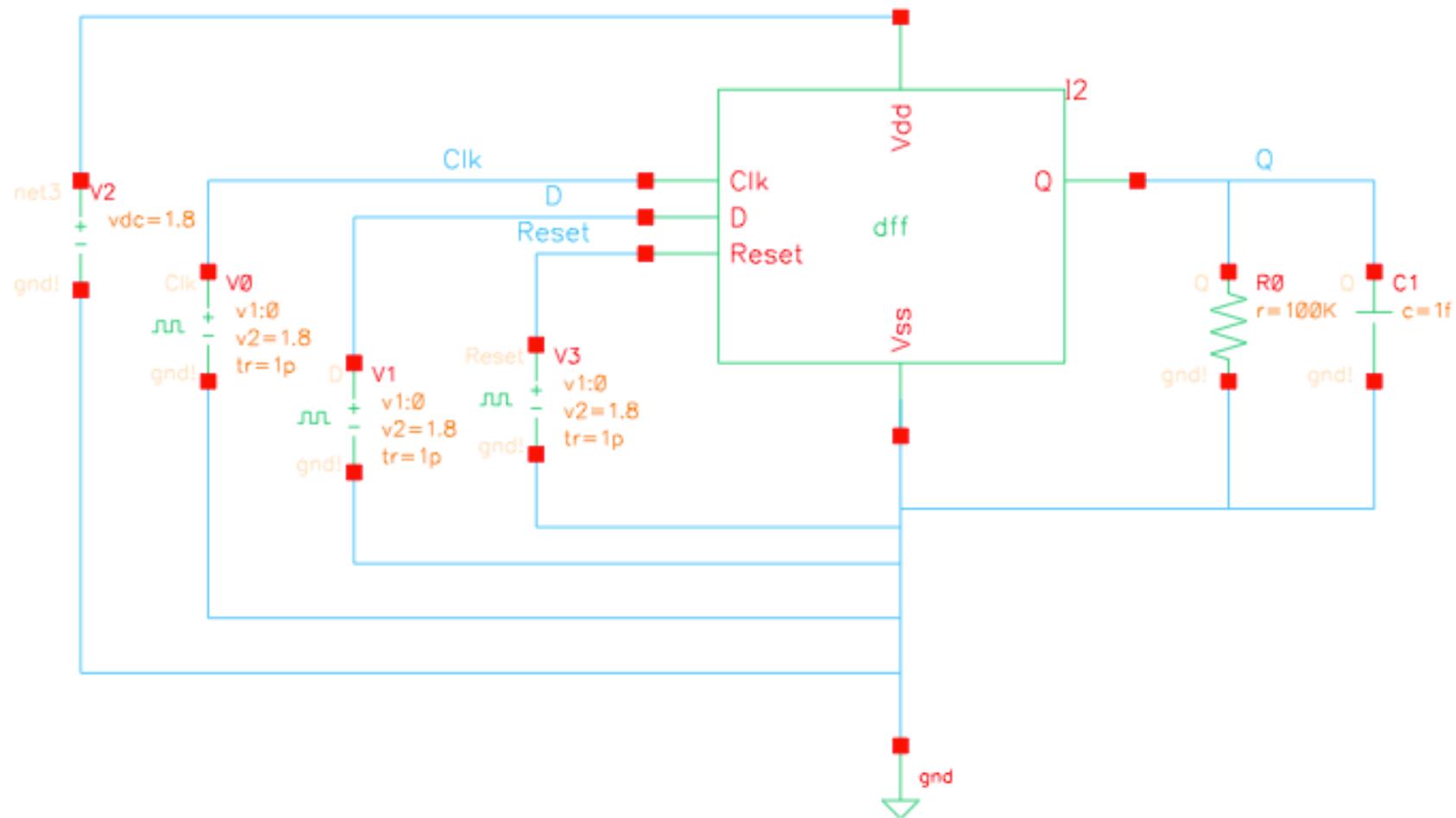
D-Type Flip Flop

Positive Clock Edge,
Synchronous Reset

D-Type Flip Flop Schematic



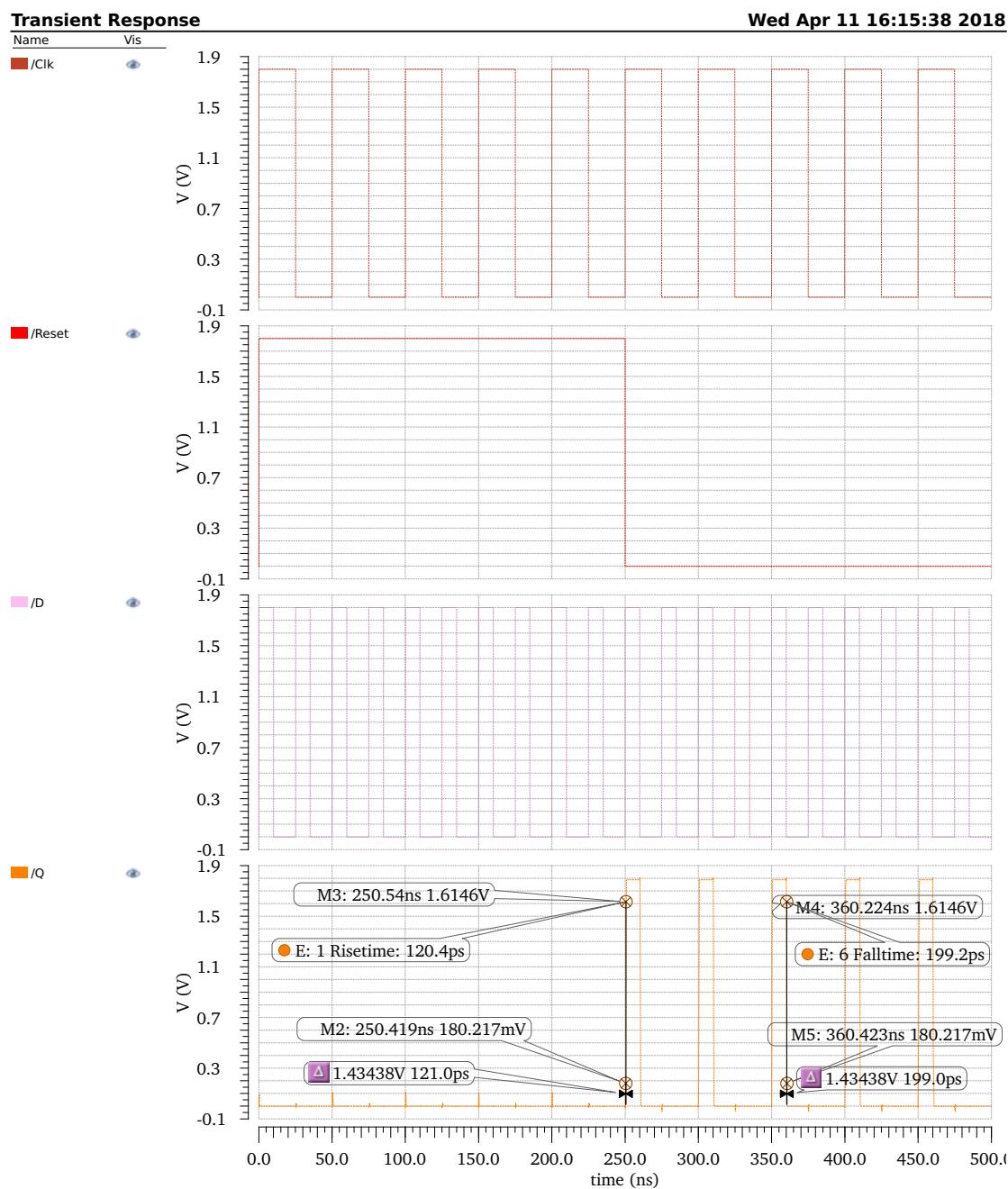
D-Type Flip Flop Testbench



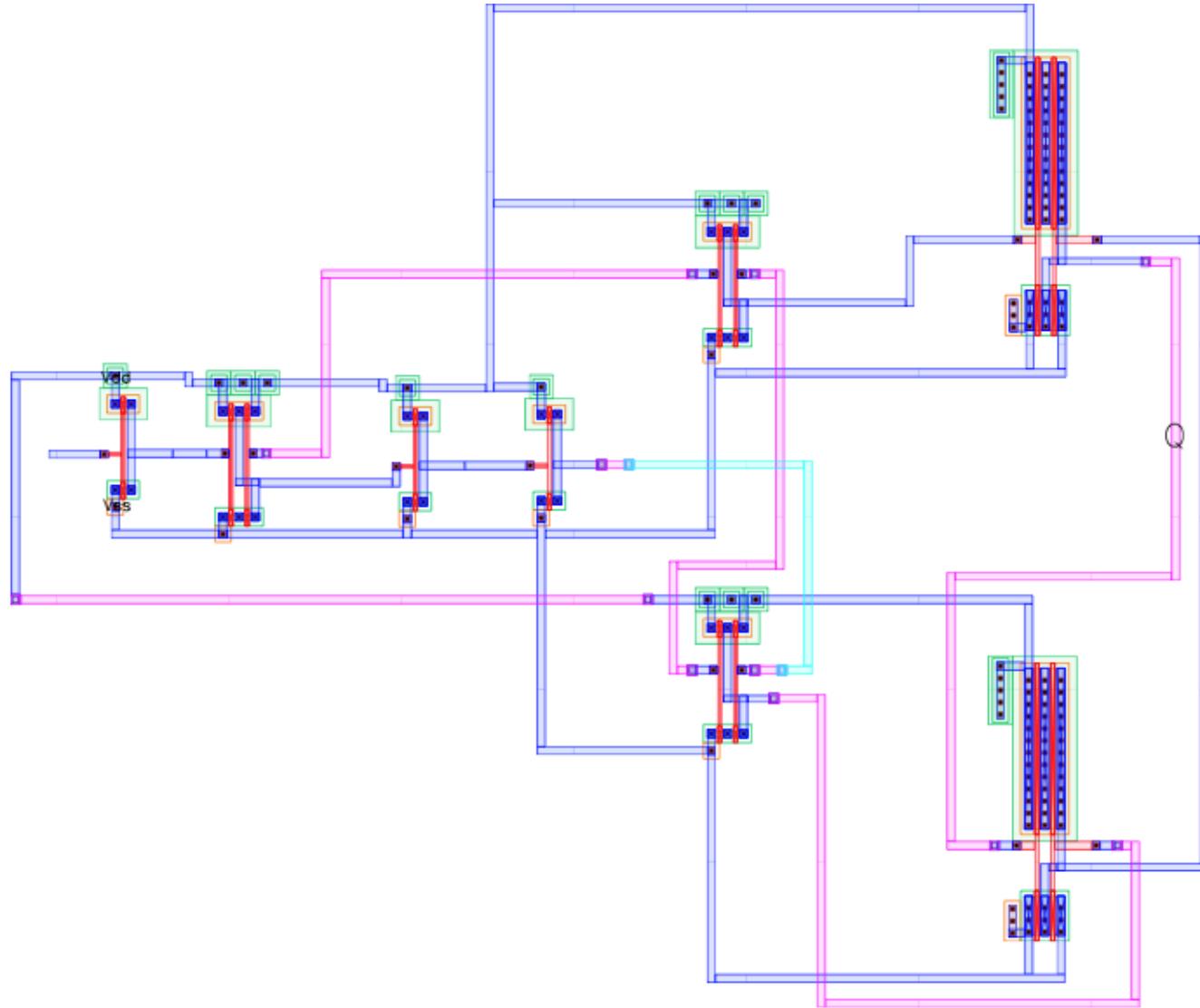
D-Type Flip Flop Testbench Waveform

project2:dff_tb:1 : project2 dff_tb schematic

16:22:25 Wed Apr 11 2018



D-Type Flip Flop Layout



D-Type Flip Flop DRC

```
Validating hierarchy instantiation for:  
library: project2  
cell:    dff_layout  
view:    layout  
Rules come from library NCSU_TechLib_tsmc02d.  
Rules path is divaDRC.rul.  
Inclusion limit is set to 1000.  
Running layout DRC analysis  
Flat mode  
Full checking.  
DRC started.....Fri May  4 19:44:51 2018  
      completed ....Fri May  4 19:44:51 2018  
      CPU TIME = 00:00:00  TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "dff_layout layout" *****  
Total errors found: 0
```

D-Type Flip Flop LVS

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/class/student/ /CPE151/LVS/layout
/gaia/class/student/ /CPE151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/ /CPE151/LVS/layout/netlist

count	
18	nets
0	terminals
13	pmos
13	nmos

Net-list summary for /gaia/class/student/ /CPE151/LVS/schematic/netlist

count	
18	nets
6	terminals
13	pmos
13	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26

	nets	
un-matched	0	0
merged	0	0

pruned	0	0
active	18	18
total	18	18

terminals		
un-matched	0	0
matched but		
different type	0	0
total	0	6

Probe files from /gaia/class/student/ /CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/ /CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

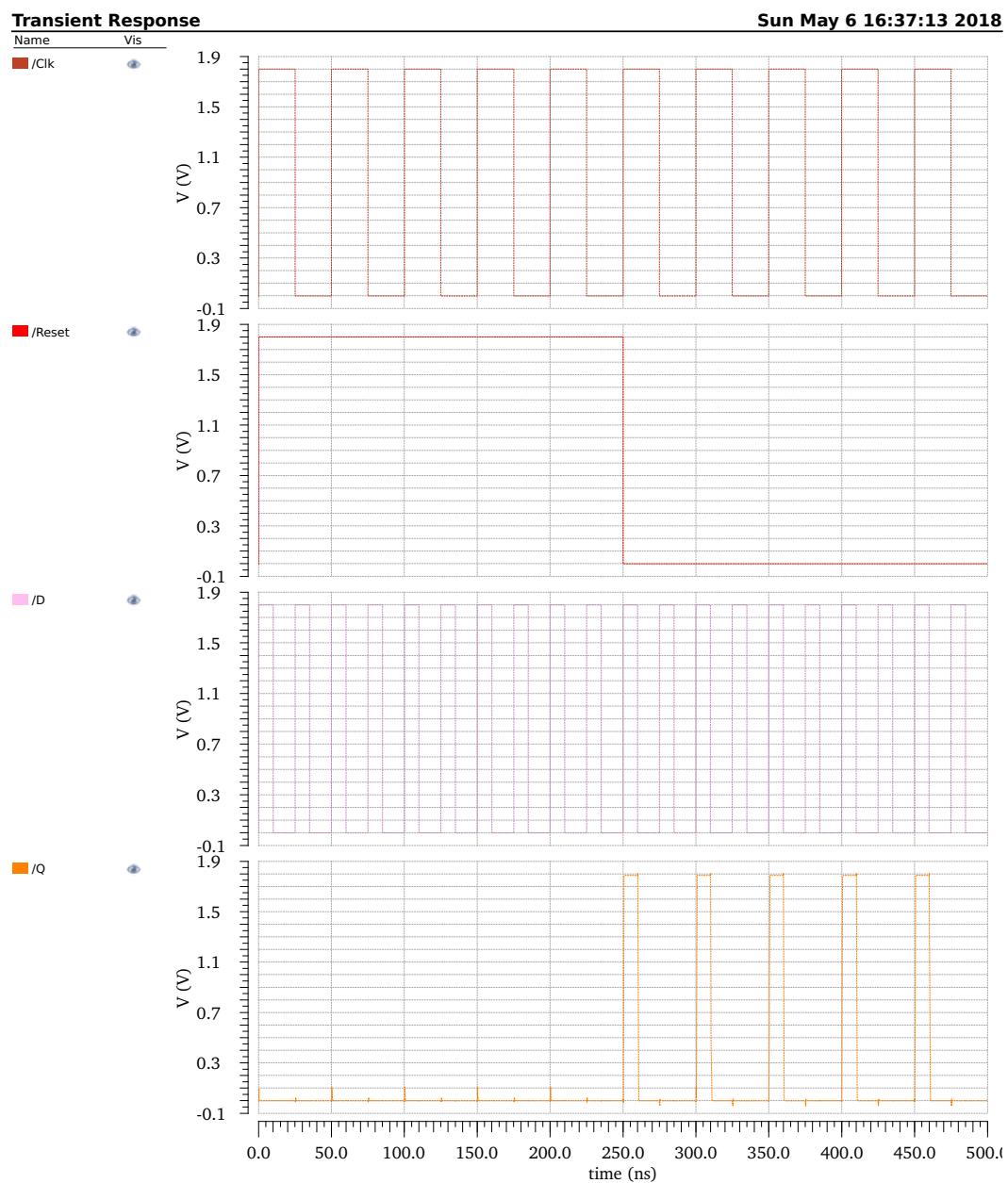
prunedev.out:

audit.out:

D-Type Flip Flop Post-Layout

project2:dff_tb:1 : project2 dff_tb schematic

16:37:32 Sun May 6 2018



DC Response**Sun May 6 16:37:13 2018**

Name Vis

/Clk

④

/Reset

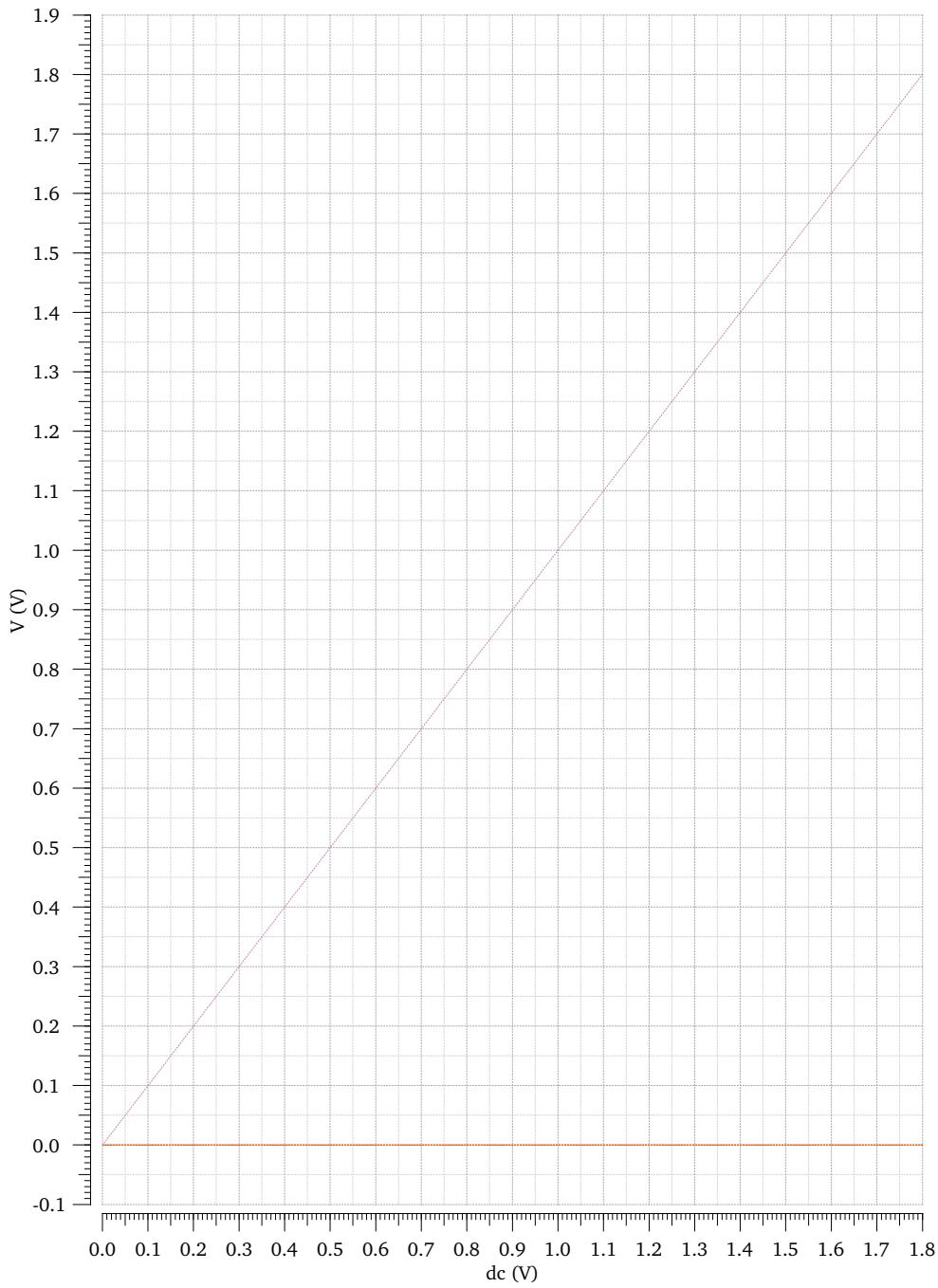
④

/D

④

/Q

④



Conclusion

S. No.	Description	Rise Time (μs)	Fall Time (μs)	Delay Time (μs)
1	Inverter	0.000236	0.00018	-0.000056
2	2-Input NAND Gate	0.0000681	0.00003662	-0.00003148
3	2-Input NOR Gate	0.002172	0.000838	-0.001334
4	2-Input AND	0.00004912	0.00002901	-0.00002011
5	D-Flip Flop	0.0001204	0.0001992	0.0000788
6	Full Adder	0.00008112	0.0000397	-0.00004142
7	Bi-Directional Shifter	0.0001178	0.0002017	0.0000839