Міністерство освіти і науки України

Національний університет „Львівська політехніка”

Кафедра ЕОМ



**Звіт**

З лабораторної роботи № 2

З дисципліни “Моделювання комп’ютерних систем”

На тему: “Структурний опис цифрового автомата. Перевірка роботи автомата за допомогою стенда”

**Варіант - 2**

**Виконав:**

ст.гр. КІ-202

Бажулін С.В.

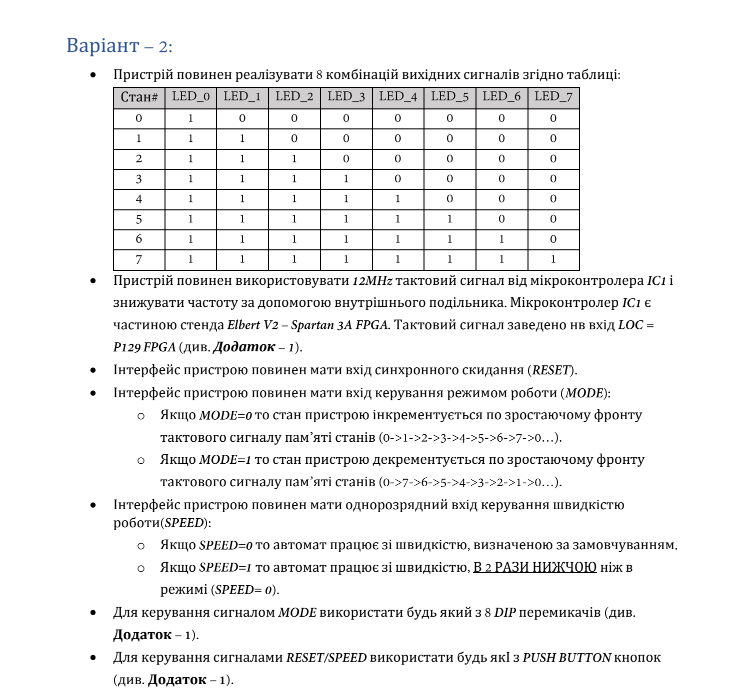
Перевірив:

Козак Н.Б.

**Львів 2023**

**Мета роботи :** На базі стенда Elbert V2 – Spartan 3A FPGA, реалізувати цифровий автомат світлових ефектів.

**Завдання**



**Виконання роботи:**

**Файл OutputLogic:**

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-- Company:

-- Engineer:

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-- Create Date: 11:41:55 04/08/2023

-- Design Name:

-- Module Name: out\_logic\_intf - out\_logic\_arch

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity out\_logic\_intf is

Port ( IN\_BUS : in std\_logic\_vector(2 downto 0);

OUT\_BUS : out std\_logic\_vector(7 downto 0)

);

end out\_logic\_intf;

architecture out\_logic\_arch of out\_logic\_intf is

begin

OUT\_BUS(0) <= ((not(IN\_BUS(2)) and not(IN\_BUS(1)) and not(IN\_BUS(0))) or(not(IN\_BUS(2)) and not(IN\_BUS(1)) and IN\_BUS(0)) or (not(IN\_BUS(2)) and IN\_BUS(1) and not(IN\_BUS(0))) or (not(IN\_BUS(2)) and IN\_BUS(1) and IN\_BUS(0)) or (IN\_BUS(2) and not(IN\_BUS(1)) and not(IN\_BUS(0))) or (IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0)) or (IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(1) <= ((not(IN\_BUS(2)) and not(IN\_BUS(1)) and IN\_BUS(0)) or (not(IN\_BUS(2)) and IN\_BUS(1) and not(IN\_BUS(0))) or (not(IN\_BUS(2)) and IN\_BUS(1) and IN\_BUS(0)) or (IN\_BUS(2) and not(IN\_BUS(1)) and not(IN\_BUS(0))) or (IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0)) or (IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(2) <= ((not(IN\_BUS(2)) and IN\_BUS(1) and not(IN\_BUS(0))) or (not(IN\_BUS(2)) and IN\_BUS(1) and IN\_BUS(0)) or (IN\_BUS(2) and not(IN\_BUS(1)) and not(IN\_BUS(0))) or (IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0)) or (IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(3) <= (((not(IN\_BUS(2)) and IN\_BUS(1) and IN\_BUS(0))) or ((IN\_BUS(2) and not(IN\_BUS(1)) and not(IN\_BUS(0)))) or ((IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0))) or ((IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0)))) or ((IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0))));

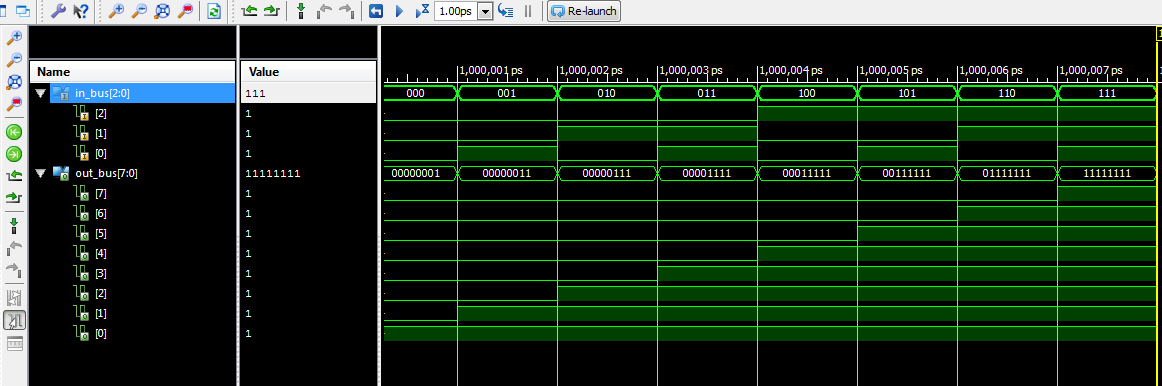
OUT\_BUS(4) <= ((IN\_BUS(2) and not(IN\_BUS(1)) and not(IN\_BUS(0))) or (IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0)) or (IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(5) <= ((IN\_BUS(2) and not (IN\_BUS(1)) and IN\_BUS(0)) or ((IN\_BUS(2)) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(6) <= ((IN\_BUS(2) and IN\_BUS(1) and not(IN\_BUS(0))) or (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0)));

OUT\_BUS(7) <= (IN\_BUS(2) and IN\_BUS(1) and IN\_BUS(0));

end out\_logic\_arch;



*Рис. 1 Діаграма проведеної симуляції для OutputLogic*

**Файл TransitionLogic:**

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-- Company:

-- Engineer:

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-- Create Date: 16:13:21 02/23/2020

-- Design Name:

-- Module Name: transition\_logic\_intf - transition\_logic\_arch

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity transition\_logic\_intf is

Port ( CUR\_STATE : in std\_logic\_vector(2 downto 0);

MODE : in std\_logic;

NEXT\_STATE : out std\_logic\_vector(2 downto 0);

RESET : in std\_logic

);

end transition\_logic\_intf;

architecture transition\_logic\_arch of transition\_logic\_intf is

begin

NEXT\_STATE(0) <= (not(RESET) and not(MODE) and not(CUR\_STATE(2)) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 000 -> 001

(not(RESET) and not(MODE) and not(CUR\_STATE(2)) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 010 -> 011

(not(RESET) and not(MODE) and CUR\_STATE(2) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 100 -> 101

(not(RESET) and not(MODE) and CUR\_STATE(2) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 110 -> 111

(not(RESET) and MODE and not(CUR\_STATE(2)) and (CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 001 <- 010

(not(RESET) and MODE and (CUR\_STATE(2)) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 011 <- 100

(not(RESET) and MODE and CUR\_STATE(2) and (CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 101 <- 110

(not(RESET) and MODE and not(CUR\_STATE(2)) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))); -- 111 <- 000

NEXT\_STATE(1) <= (not(RESET) and not(MODE) and not(CUR\_STATE(2)) and not(CUR\_STATE(1)) and CUR\_STATE(0)) or -- 001 -> 010

(not(RESET) and not(MODE) and not(CUR\_STATE(2)) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 010 -> 011

(not(RESET) and not(MODE) and CUR\_STATE(2) and not(CUR\_STATE(1)) and CUR\_STATE(0)) or -- 101 -> 110

(not(RESET) and not(MODE) and CUR\_STATE(2) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 110 -> 111

(not(RESET) and MODE and not(CUR\_STATE(2)) and (CUR\_STATE(1)) and (CUR\_STATE(0))) or -- 010 <- 011

(not(RESET) and MODE and CUR\_STATE(2) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 011 <- 100

(not(RESET) and MODE and CUR\_STATE(2) and CUR\_STATE(1) and CUR\_STATE(0)) or -- 110 <- 111

(not(RESET) and MODE and not(CUR\_STATE(2)) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))); -- 111 <- 000

NEXT\_STATE(2) <= (not(RESET) and not(MODE) and not(CUR\_STATE(2)) and CUR\_STATE(1) and CUR\_STATE(0)) or -- 011 -> 100

(not(RESET) and not(MODE) and CUR\_STATE(2) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))) or -- 100 -> 101

(not(RESET) and not(MODE) and CUR\_STATE(2) and not(CUR\_STATE(1)) and CUR\_STATE(0)) or -- 101 -> 110

(not(RESET) and not(MODE) and CUR\_STATE(2) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 110 -> 111

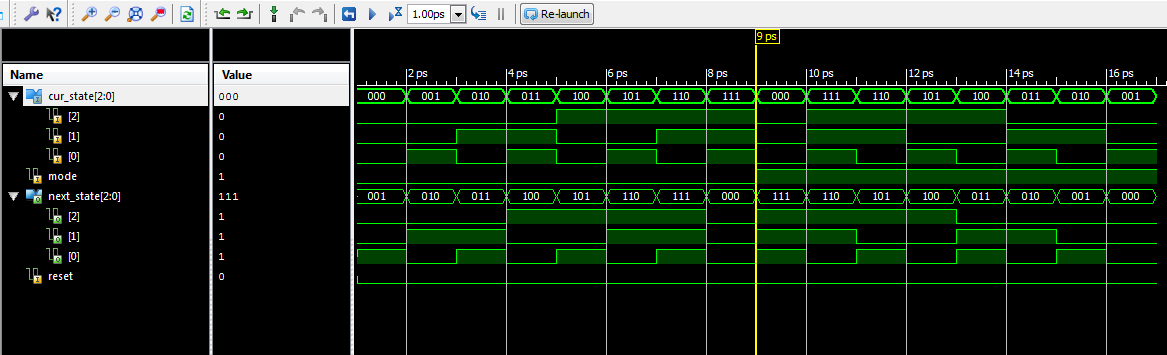
(not(RESET) and MODE and CUR\_STATE(2) and not(CUR\_STATE(1)) and CUR\_STATE(0)) or -- 100 <- 101

(not(RESET) and MODE and CUR\_STATE(2) and CUR\_STATE(1) and not(CUR\_STATE(0))) or -- 101 <- 110

(not(RESET) and MODE and CUR\_STATE(2) and CUR\_STATE(1) and CUR\_STATE(0)) or -- 110 <- 111

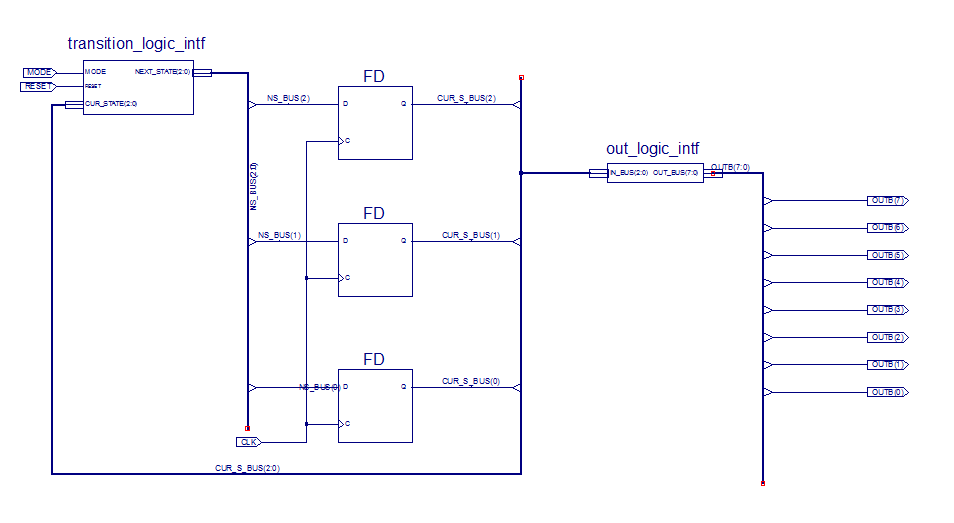
(not(RESET) and MODE and not(CUR\_STATE(2)) and not(CUR\_STATE(1)) and not(CUR\_STATE(0))); -- 111 <- 000

end transition\_logic\_arch;

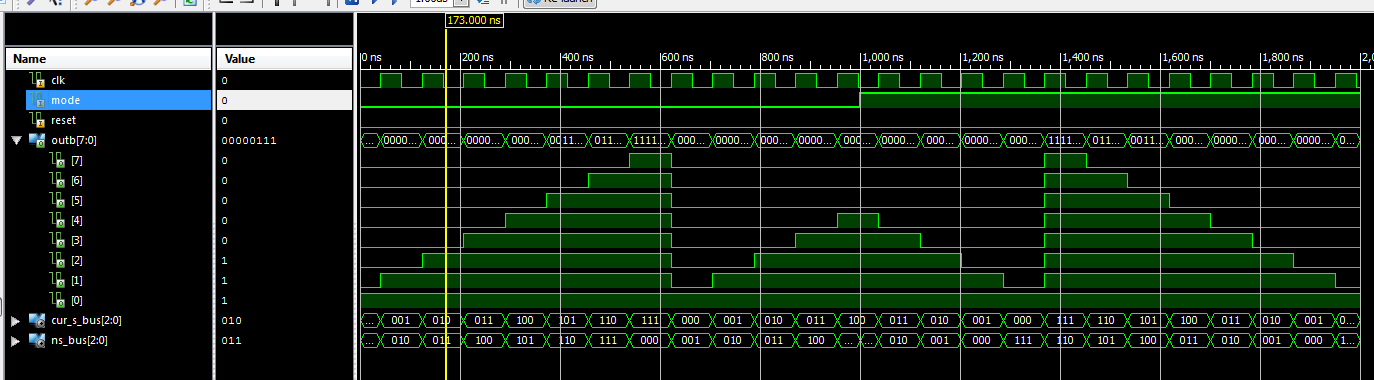


*Рис. 2 Діаграма проведеної симуляції для TransitionLogic*

**Схема для Light controller**



*Рис. 3 Схема LightController*

* Рис. 4 Діаграма проведеної симуляції для LightController*

**Файл TestBench:**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.numeric\_std.ALL;

LIBRARY UNISIM;

USE UNISIM.Vcomponents.ALL;

ENTITY TopLevel\_TopLevel\_sch\_tb IS

END TopLevel\_TopLevel\_sch\_tb;

ARCHITECTURE behavioral OF TopLevel\_TopLevel\_sch\_tb IS

COMPONENT TopLevel

PORT( SPEED : IN STD\_LOGIC;

RESET : IN STD\_LOGIC;

MODE : IN STD\_LOGIC;

OUT\_BUS : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

CLOCK : IN STD\_LOGIC);

END COMPONENT;

SIGNAL SPEED : STD\_LOGIC;

SIGNAL RESET : STD\_LOGIC;

SIGNAL MODE : STD\_LOGIC;

SIGNAL OUT\_BUS : STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SIGNAL CLOCK : STD\_LOGIC := '0';

BEGIN

UUT: TopLevel PORT MAP(

SPEED => SPEED,

RESET => RESET,

MODE => MODE,

OUT\_BUS => OUT\_BUS,

CLOCK => CLOCK

);

-- \*\*\* Test Bench - User Defined Section \*\*\*

tb : PROCESS

BEGIN

RESET <= '0';

MODE <= '1';

SPEED <= '0';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '0';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '0';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '0';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '0';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '1';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '1';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '1';

wait for 10 ms;

RESET <= '0';

MODE <= '1';

SPEED <= '1';

wait for 10 ms;

WAIT; -- will wait forever

END PROCESS;

-- \*\*\* End Test Bench - User Defined Section \*\*\*

tb\_clk: PROCESS

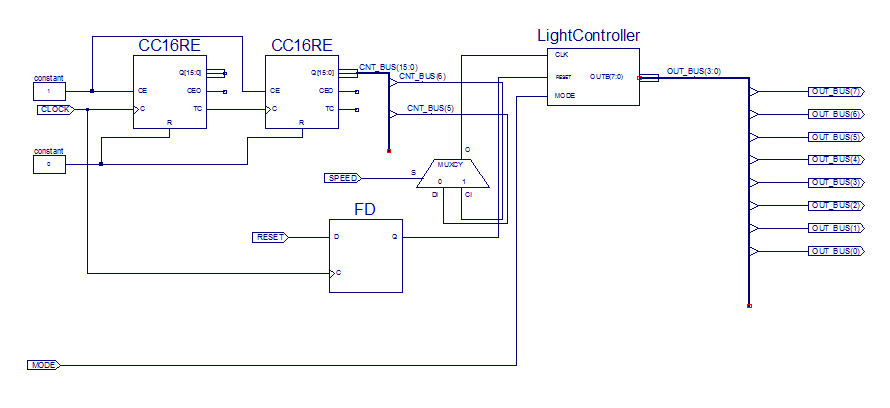
BEGIN

CLOCK <= not CLOCK;

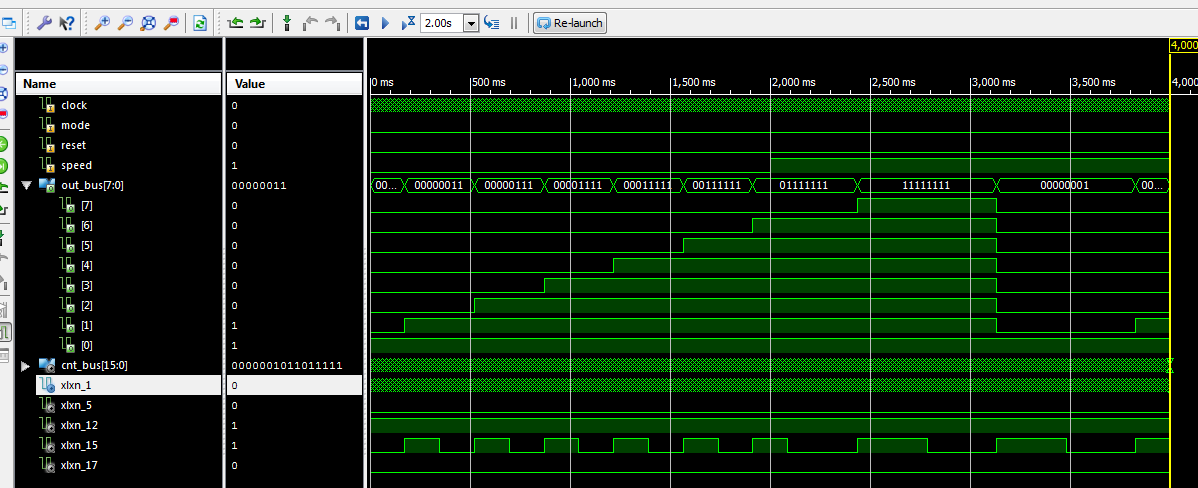
wait for 0.83 ns;

END PROCESS;

END;

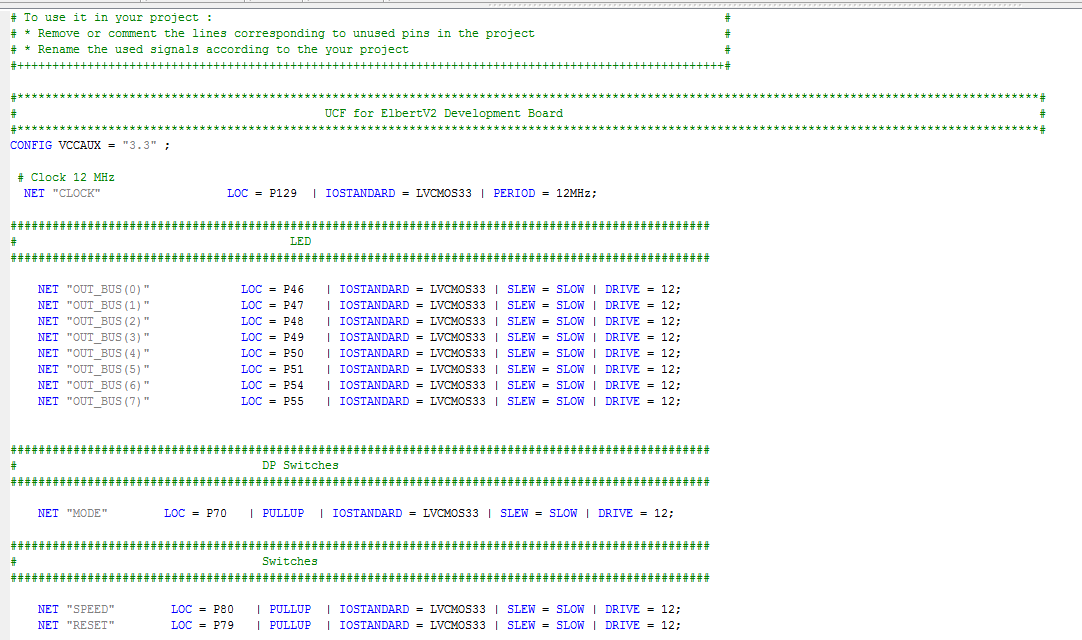
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*Рис. 5 Схема TopLevel*

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*Рис. 6 Діаграма проведеної симуляції для TopLevel*

**Створення Constant файлу:**

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**Висновок:** на цій лабораторній роботі, я на базі стенда Elbert V2 – Spartan 3A FPGA, реалізував цифровий автомат світлових ефектів.