Sergio Vinagrero Gutierrez

servinagrero@gmail.com +33634584101 Grenoble, France B Driving license

servinagrero servinagrero 0000-0001-7460-3187

Professional Experience

Postdoctoral Researcher, *CNRS / Institut des Nanotechnologies de Lyon* — 09/2024 – present, France
Development of authentication protocols restistant to Machine Learning attacks based on Photonic-based Physical Unclonable Functions

Ph.D. Researcher, *TIMA Laboratory* — 10/2022 – 09/2024, Grenoble, France
Ph.D. on Methodologies for the Design, the Modeling, and the Quality Assessment of Physical Unclonable Functions (PUFs)

Assistant Professor for Practical Sessions, *University Grenoble Alpes* — 2022 – 2023, Grenoble, France
Taught VHDL to Master students in multiple practical sessions as an assistant professor.

Research Internship, *TIMA Laboratory* — 02/2021 – 08/2021, Grenoble, France
Evaluated the potential of 0xRAM technologies as a candidate for Physical Unclonable Functions in Cadence, SPICE and Python.
Analysed the metrics and data in Python and R.

Research Labwork, *TIMA Laboratory* — 09/2020 – 01/2021, Grenoble, France
Implemented an SRAM-based Physical Unclonable Function and communication protocol in C for STM32 devices.
Developed a platform in for acquisition of SRAM data in Python, PostgreSQL and RabbitMQ.

Bachelor Thesis, *University Charles III* — 2020 – 2020, Madrid, Spain
Implemented an SRAM-based Physical Unclonable Function in C on STM32 Micro-Controllers.
Evaluated the data and metrics in Python and R.

Information Technology Teacher, *Vox Institute* — 03/2020 – 08/2020, Madrid, Spain
Taught apprentice students computer skills, most specifically the Microsoft Office Suite

Education

Ph.D. Researcher, *TIMA Laboratory* — 2021 – 09/2024, Grenoble, France
Research on Methodologies for the Design, the Modeling, and the Quality Assessment of Physical Unclonable Functions (PUFs)

Master in Wireless Integrated Communicated Systems, — 2020 – 2021, Grenoble, France
University Grenoble Alpes and Grenoble INP Phelma
First student in rank with average of 15.97/20

Bachelor degree on Electrical, Electronics and Communications Engineering, *University Carlos III de Madrid* — 2017 – 2020, Madrid, Spain

Baccalaureate in Engineering Sciences, *School Rafaela Ibarra* — 2014 – 2016, Madrid, Spain
Average of 9.3/10

Skills

Developement
R, Python, Julia, C, C++, Rust, Lua, SQL, Linux, STM32

Software
Git, Docker, PostgreSQL

Electronic Design
Cadence, Spectre, ADS, VHDL, Verilog, Verilog-A, SPICE

Graphic Design
LaTeX, Inkscape, GIMP, Blender, Processing

Awards

Ph.D. Forum Contest Award,
IEEE European Test Symposium
2022

During the European Test Symposium 2022 conference, I was awarded the Ph.D. Forum Contest Award on my work on Memristor-based security primitives

2nd Best Student Paper, *IEEE NEWCAS*
2021

During the IEEE NEWCAS 2021 conference I had the opportunity to present the SRAM Platform project that I had been working at TIMA Laboratory during the first semester of my master degree.

First Class Honors as Bachelors Degree Project, *University Charles III*
2020

I was awarded the first class honours for my work on the characterisation of SRAM-Based PUFs on Micro-Controllers.

Languages

Spanish — Native

English — Cambridge C1 Certificate

French — B1

German — Beginner

Organizations

TIMA Laboratory, *Representative of non-permanent doctoral students and researchers*
2022 – Present | Grenoble, France

University Charles III,
Leader of students' representative council
10/2018 – 10/2019 | Madrid, Spain

Took part of this role to continue my job at the student's representative council.
Helped with the coordination of other representatives and mediate problems with students

Publications

On-line reliability estimation of ring oscillator PUF, 2022
2022 IEEE European Test Symposium (ETS)
On-line test methodology for RO-PUF reliability which enables high accuracy in the results since it is not based on predictive simplified models of the device variability and noise, but on actual technological electrical models extracted from a single technology.

Memristor-based security primitives, 2022
2022 IEEE European Test Symposium (ETS)
With the rapid growth of IoT and embedded devices, the development of low power, high density, high performance SoCs has pushed the embedded memories to their limits and opened the field to the development of emerging memory technologies. The Resistive Random Access Memory (ReRAM) has emerged as a promising choice for embedded memories due to its reduced read/write latency and high CMOS integration capability. Intrinsic properties of ReRAMs make them suitable for the implementation of basic security primitives such as Physically Unclonable Functions (PUFs) and True Random Number Generators (TRNGs).

SRAM-PUF: Platform for Acquisition of Sram-Based Pufs from Micro-Controllers, *University Booth-IEEE Design Automation and Test Conference in Europe (DATE 2021)* 2021
Versatile platform for the acquisition of the content of SRAM memories embedded in microcontrollers at power-up. The platform is able to power-off and -on hundreds of microcontrollers and to retrieve the content of their SRAMs thanks to a scan chain connecting all boards. The data collected is then stored in a database to enable reliability analysis.

Python Framework for Modular and Parametric SPICE Netlists Generation,
MDPI Electronics
This article proposed a generic, open-source Python framework tackling rapid design exploration for the generation of modular and parametric electronic designs that is able to work on any major simulator.

Open automation framework for complex parametric electrical simulations, *2023 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*
This article proposes a generic, open-source framework to generate complex stimuli and parameters for electrical simulations, together with a programmable Spice- and Verilog-A-based module capable of observing and logging internal states of the circuit to facilitate further result analysis.

On-line method to limit unreliability and bit-aliasing in ro-puf, *2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS)*
Analysis of Ring Oscillator based Physical Unclonable Functions (PUF) to propose a methodology for the analytical estimation of it's Bitaliasing and Reliability, based on the variability profile of the underling technology.