CA-IS371x/2x High-Speed Single/Dual Channel Digital Isolators

1. Product Features

• Signaling rate: DC to 150Mbps • Wide supply voltage range: 2.5V to 5.5V • Wide temperature range: -40°C to 125°C • No startup initialization required • Default output high and low options • Excellent electromagnetic immunity • High CMTI: ±100kV/μs (typical) • Low power consumption, (typical): ÿ Current is 1.5mA/channel (5V power supply at 1Mbps) ÿ Current is 6.6mA/channel (5V power supply at 100Mbps)

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Precision Timing (Typical) 8ns

- Propagation Delay
- 1ns Pulse Width Distortion
- 2ns Propagation Delay
- Skew 5ns Minimum Pulse

Width • Up to 5KVRMS Isolation Voltage • Isolation Barrier Life: >40 Years • Schmitt Trigger Inputs • Narrow Body SOIC8(S), Wide Body SOIC8(G) and Wide Body SOIC16-WB(W) package, RoHS compliant

2. Application

• Industrial Automation • Motor Control • Medical Electronics • Isolated Switching Power Supplies • Solar Inverters • Isolated ADC, DAC

3. Overview

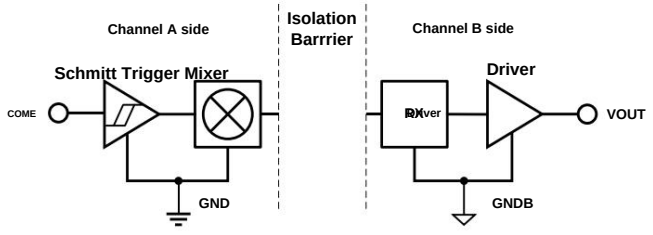
The CA-IS371x/2x is a high performance 1/2 channel digital isolator with precise timing characteristics and low power consumption. The CA-IS371x/2x devices provide high electromagnetic immunity and low emissions when isolating CMOS digital I/O. All device versions feature Schmitt trigger inputs for high Noise immunity. The logic input and output buffers of each isolation channel are separated by a silicon dioxide (SiO2) insulation barrier. The CA-IS3710 device is a single channel, the CA-IS3720 device has two forward dual channels, the CA-IS3721 has one forward and one reverse dual channels, and the CA-IS3722 and CA-IS3721 have the opposite channels, with one reverse and one forward dual channels. All devices have a fail-safe mode option. If input power or signal is lost, the default output is low for devices with a suffix of L and high for devices with a suffix of H.

The CA-IS371x/2x devices feature high isolation capabilities, helping prevent noise and surges on data buses or other circuits from entering the local ground, interfering with or damaging sensitive circuits. High CMTI capabilities are expected to ensure proper transmission of digital signals. The CA-IS371x/2x devices are available in 8-pin SOIC and 16-pin wide-body SOIC packages. All products have an isolation rating of 3.75kVrms, and the wide-body package products support insulation withstand voltages up to 5kVrms.

Device Information

Part Number	Package Package size (nominal value)	
CA-IS3710, CA-IS3720, CA-IS3721, CA-IS3722	SOIC8 (S)	4.90 mm × 3.90 mm
	SOIC8-WB(G) 5.85 mm ×7.50 mm	
	SOIC16-WB(W) 10.30mm ×7.50 mm	

Simplified channel structure diagram



Channels A and B are separated by an isolation capacitor.

GNDA and GNDB are connected to the A-side signal and B-side power isolation grounds respectively.

4. Ordering Guide

Table **4-1** Valid ordering part numbers

model	Number of input channels A side	Number of input channels B side	Fail-safe output state	Rated withstand voltage (kV)	Output Enable	Encapsulation
CA-IS3710LS	1	0	Low	3.75	No	SOIC-8
CA-IS3710LW	1	0	Low	5.0	No	WB SOIC-16
CA-IS3710HS	1	0	High	3.75	No	SOIC-8
CA-IS3710HW	1	0	High	5.0	No	WB SOIC-16
CA-IS3720LS	2	0	Low	3.75	No	SOIC-8
CA-IS3720LG	2	0	Low	5.0	No	WB SOIC-8
CA-IS3720LW	2	0	Low	5.0	No	WB SOIC-16
CA-IS3720HS	2	0	High	3.75	No	SOIC-8
CA-IS3720HG	2	0	High	5.0	No	WB SOIC-8
CA-IS3720HW	2	0	High	5.0	No	WB SOIC-16
CA-IS3721LS	1	1	Low	3.75	No	SOIC-8
CA-IS3721LG	1	1	Low	5.0	No	WB SOIC-8
CA-IS3721LW	1	1	Low	5.0	No	WB SOIC-16
CA-IS3721HS	1	1	High	3.75	No	SOIC-8
CA-IS3721HG	1	1	High	5.0	No	WB SOIC-8
CA-IS3721HW	1	1	High	5.0	No	WB SOIC-16
CA-IS3722LS	1	1	Low	3.75	No	SOIC-8
CA-IS3722LG	1	1	Low	5.0	No	WB SOIC-8
CA-IS3722LW	1	1	Low	5.0	No	WB SOIC-16
CA-IS3722HS	1	1	High	3.75	No	SOIC-8
CA-IS3722HG	1	1	High	5.0	No	WB SOIC-8
CA-IS3722HW	1	1	High	5.0	No	WB SOIC-16

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5. Revision History

Revision **0:** Initial version.

Revision **0** to Revision **A**

• Update 3 Overview

• Updated Table 4-1

ÿModify rated withstand voltage

• Updated Figure 6-1

ÿChange pin name

• Updated Table 6-1

ÿChange pin name

• Updated Figure 6-2

ÿChange pin name

• Updated Table 6-2

ÿChange pin name

• Updated 7.6 Insulation specifications

• Updated 11.1 SOIC 16 wide body package size

Revision A to Revision B

• Updated product features

Revision B to Revision C

• Added 8-pin wide-body package option

6. Pin function description

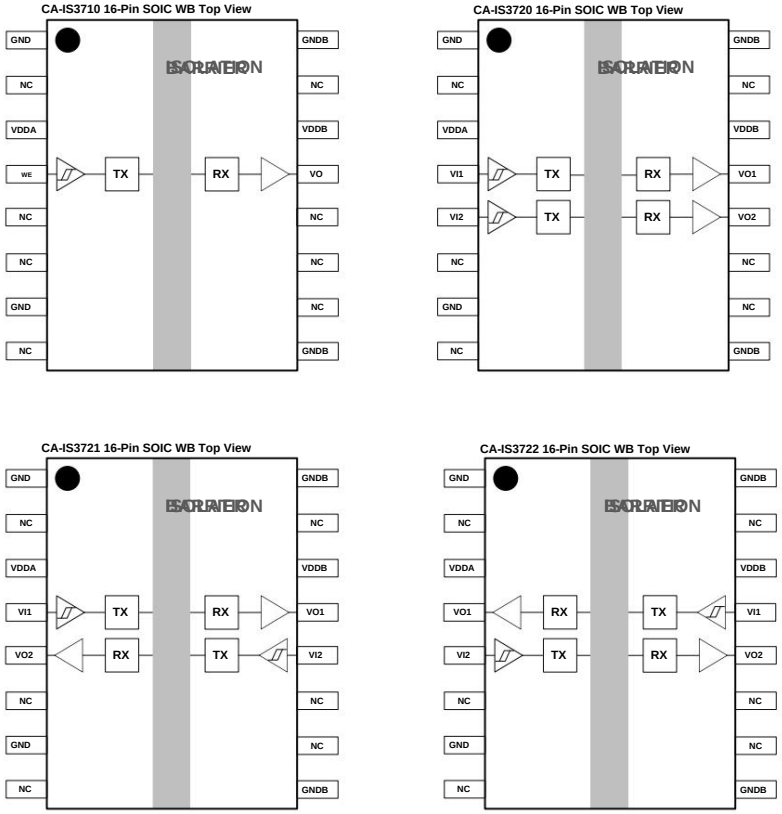


Figure 6-1 **CA-IS371x/2x SOIC16-WB** wide body top view

Table **6-1 CA-IS371x/2x SOIC16-WB** wide body pin function description

Pin Name	SOIC16 Pin Number	type	describe
GND	1	land	A-side ground reference point
NC	2	NC	No internal connections
VDDA	3	Power	A side power supply voltage
VI1/VO1	4	supply Logic input/output	CA-IS3710/20/21 A-side logic input / CA-IS3722 A-side logic output
VI2/VO2/NC1	5	Logic input/output	CA-IS3720/22 A-side logic input/ CA-IS3721 A-side logic output/ CA-IS3710 No internal connection
NC	6	NC	No internal connections
GND	7	land	A side ground reference point
NC	8	NC	No internal connections
GNDB	9	land	B side ground reference point
NC	10	NC	No internal connections
NC	11	NC	No internal connections
VI2/VO2	12	Logic Input/Output Logic	CA-IS3721 B-side logic input/CA-IS3720/22/ B-side logic output/ CA-IS3710 No internal connection
VI1/VO1	13	Input/Output Power Supply	CA-IS3722 B-side logic input / CA-IS3710/20/21 B-side logic output
VDDB	14		B-side power supply voltage
NC	15	NC	No internal connections
GNDB	16	land	B side ground reference point

Remark:

1, No Connection. These pins have no internal connection. They can be left floating, tied to VDD or tied to GND.

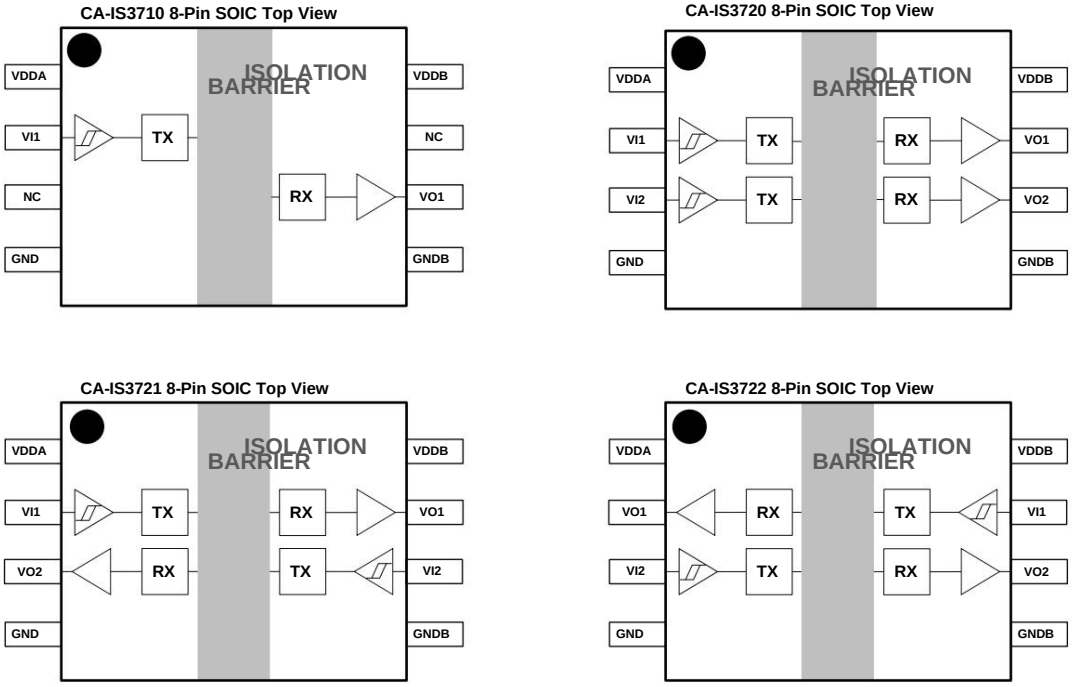


Figure 6-2 Top view of CA-IS371x/2x SOIC 8-pin narrow body and SOIC 8-pin wide body packages

Table **6-2 CA-IS371x/2x SOIC8** pin function description

Pin Name	SOIC8 Pin Number	type	describe
VDDA	1	Power	A side power supply voltage
VI1/VO1	2	Logic Input/Output Logic	CA-IS3710/20/21 A-side logic input / CA-IS3722 A-side logic output
VI2/VO2/NC1	3	Input/Output Ground	CA-IS3720/22 A-side logic input / CA-IS3721 A-side logic output / CA-IS3710 No internal connection
GND	4		A side ground reference point
GNDB	5		B side ground reference point
VI2/VO1/VO2	6	Ground Logic Input/	CA-IS3721 B-side logic input/CA-IS3710/20/22. B-side logic output
VI1/VO1/NC	7	Output Logic Input/Output	CA-IS3722 A-side logic input / CA-IS3720/21 A-side logic input / CA-IS3710 No internal connection
VDDB	8	Power	B-side power supply voltage
Remark: 1. No Connection. These pins have no internal connection. They can be left floating, tied to VDD, or tied to GND.			

7.1. Absolute Maximum Ratings **1**

parameter		Minimum Maximum Unit		
VDDA, VDDB	Supply voltage 2	-0.5	6.0	In
Come	Input Voltage t Ax, Bx, ENx Output	-0.5	VDDA+0.53	In
IT	Current Junction	-20	20	m.a.
TJ			150	°C
TSTG	Temperature Storage Temperature Range	-65	150	°C

Notes:

1. Equal to or exceeding the absolute maximum ratings may cause permanent damage to the product. This is only a maximum rating and cannot be exceeded at these or any other conditions beyond those specified in this technical specification.

Operational operation of the product is inferred within the specified conditions shown in the Operation section. Exposure to conditions exceeding the maximum ratings for extended periods may affect product reliability.

2. All voltage values, except differential I/O bus voltages, are relative to the local ground terminal (GNDA or GNDB) and are peak voltage values.

3. The maximum voltage shall not exceed 6 V.

7.2. ESD Rating

		Numerical **Unit**	
VESD Electrostatic Discharge	Human Body Model (HBM), according to ANSI/ESDA/JEDEC JS-001, all pins 1 Charged Device	±4000	In
	Model (CDM), according to JEDEC specification JESD22-C101, all pins 2	±1000	

Remark:

1. JEDEC document JEP155 stipulates that 500V HBM can be safely manufactured through standard ESD control processes.

2. JEDEC document JEP157 specifies that 250V CDM allows safe manufacturing using standard ESD control processes.

7.3. Recommended working conditions

parameter			Minimum Typical Value		Maximum value unit	
VDDA, VDDB supply voltage			2.375	3.3	5.5	In
VDDÿUVLO+ÿ	Undervoltage threshold when VDD supply voltage rises		1.95	2.24	2.375	In
VDDÿUVLO-ÿ	Undervoltage threshold when VDD supply voltage drops		1.88	2.10	2.325	In
VHYSÿUVLOÿ	VDD Hysteresis Undervoltage Threshold		70	140	250	mV
John	High level output current	VDDO1 = 5V	-4			m.a.
		VDDO = 3.3V	-2			
		VDDO = 2.5V	-1			
IOL	Low level output current	VDDO = 5V			4	m.a.
		VDDO = 3.3V			2	
		VDDO = 2.5V			1	
HIV	Input Threshold Logic High Input		2.0			In
WILL	Threshold Logic Low Signaling Rate				0.8	In
DR	Ambient Temperature		0		150	Mbps
FACING			-40	27	125	°C

Remark:

1. VDDO = output side VDD

7.4. Thermal Information

Heat meter		CA-IS371x2x			
		S (SOIC)	G(SOIC)	W (SOIC) Unit	
		8 Pins	8 Pins	16 Pins	
RÿJA	Thermal resistance from IC junction to ambient	137.7	110.1	86.5	°C/W
RÿJC(top)	IC junction to case (top) thermal resistance	54.9	51.7	49.6	°C/W
RÿJB	IC Junction-to-Board Thermal Resistance	71.7	66.4	49.7	°C/W
ÿJT	IC Junction to Top Characterization Parameters	7.1	16.0	32.3	°C/W
ÿJB	IC Junction-to-Board Characterization Parameters	70.7	64.5	49.2	°C/W
RÿJC(bottom)	IC junction to case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

7.5. Rated power

parameter		Test conditions	Min Typ Max Unit	
CA-IS3710				
PD maximum power consumption		VDDA = VDDB = 5.5 V, CL = 15 pF,	90	mW
PDA	Maximum power consumption on side A	TJ = 150°C, Input 75MHz 50% Duty Cycle	12	mW
PDB	Maximum power consumption on side B	Wave	78	mW
CA-IS3720				
PD	Maximum power consumption	VDDA = VDDB = 5.5 V, CL = 15 pF,	120 mW	
PDA	Maximum power consumption on side A	TJ = 150°C, Input 75MHz 50% Duty Cycle	20	mW
PDB	Maximum power consumption on side B	Wave	100 mW	
CA-IS3721				
PD maximum power consumption		VDDA = VDDB = 5.5 V, CL = 15 pF,	120 mW	
PDA	Maximum power consumption on side A	TJ = 150°C, Input 75MHz 50% Duty Cycle	60	mW
PDB	Maximum power consumption on side B	Wave	60	mW
CA-IS3722				
PD maximum power consumption		VDDA = VDDB = 5.5 V, CL = 15 pF,	120 mW	
PDA	Maximum power consumption on side A	TJ = 150°C, Input 75MHz 50% Duty Cycle	60	mW
PDB	Maximum power consumption on side B	Wave	60	mW

C 7.6. Isolation Features

parameter	Test conditions	Numeric		unit
		W/G	S	
CLR External Air Gap (Clearance) 1	Measure the shortest distance between input and output through	8	4	mm
CPG External creepage distance 1	air Measure the shortest distance between input and output along the	8	4	mm
DTI Isolation Distance	shell Minimum internal clearance (internal distance)	14	14	ÿm
CTI Comparative Tracking Index Material	DIN EN 60112 (VDE 0303-11); IEC 60112 According to IEC	>600 >600		In
Group	60664-1 Rated mains	.	.	
IEC 60664-1 Overvoltage Category	voltage ÿ 300 VRMS Rated mains voltage	I-IV	I-III	
	ÿ 400 VRMS Rated mains voltage ÿ 600	I-IV	I-III	
	VRMS	I-III	n/a	
DIN V VDE V 0884-11:2017-012				
VIORM Maximum Repetitive Peak Isolation Voltage	AC Voltage (Bipolar) AC	1414	637	VPC
VIOWM maximum operating isolation voltage	Voltage; Time Dependent Dielectric Breakdown (TDDB) Test DC Voltage	1000	450	VRMS
		1414	637	VDC
VIOTM Maximum transient isolation voltage	VTEST = VIOTM, t = 60 s (certification); VTEST = 1.2 × VIOTM, t = 1 s (100% production test)	7070 5300		VPC
VIOSM Maximum Surge Isolation Voltage 3	Test method according to IEC 60065, 1.2/50 ÿs waveform, VTEST = 1.6 × VIOSM (production test)	6250 5000		VPC
QPD characterization of charge 4	Method a, input to output test subclass 2/3, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIORM, tm = 10 s	ÿ5	ÿ5	pC
	Method a, input to output test subclass 1, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.6 × VIORM, tm = 10 s	ÿ5	ÿ5	
	Method b1, routine testing (100% production testing) and pre-treatment (Sampling test) Vini = 1.2 × VIOTM, tini = 1 s; Vpd(m) = 1.875 × VIORM, tm = 1 s	ÿ5	ÿ5	
CIO Gate capacitance, input to output5	VIO = 0.4 × sin (2ÿft), f = 1 MHz VIO = 500 V, TA	~0.5	~0.5	pF
RIO Insulation Resistance 5	= 25°C VIO = 500 V, 100°C ÿ TA	>1012	>1012	Oh
	ÿ 125°C VIO = 500 V at TS = 150°C	>1011	>1011	
		>109	>109	
Pollution		2	2	
UL 1577				
VISO maximum isolation voltage	VTEST = FACE . t = 60 s (certification), VTEST = 1.2 × FACE . t = 1 s (100% production tested)	5000 3750		VRMS

Remark:

1. Apply creepage and clearance requirements based on the specific equipment isolation standard for the application. Take care to maintain creepage and clearance distances in the board design to ensure isolation on the printed circuit board.
   The distance is not shortened by the mounting pads of the resistor. In some cases, creepage and clearance distances on the PCB become equal. Techniques such as inserting grooves in the PCB
   Used to help increase these specifications.
2. This standard applies only to safe electrical insulation within the safety level. Compliance with the safety level should be ensured by appropriate protection circuits.
3. Testing is performed in air or oil to determine the inherent surge immunity of the isolation barrier.
4. Characteristic charge is the discharge charge caused by partial discharge (pd).
5. All pins on both sides of the gate are connected together to form a two-terminal device

7.7. Security-related certification

VDE (pending)	CSA (pending)	UL(pending)	CQC (pending)	TUV (pending)
according to DIN V VDE V 0884-11:2017-01 Certification	according to IEC60950-1, IEC 62368-1 and IEC 60601-1 Certification	UL1577 Device Recognition Program Can	certified according to GB4943.1-2011 certificate	According to EN61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013 certified

Electrical Characteristics

7.8.1. VDDA = VDDB = 5 V ± 10%, TA = -40 to 125°C

parameter	Test conditions	Min Typ Max Unit			
VOH output voltage logic high level	IOH = -4mA; Figure 8-1	VDDO1 -0.4 4.8			In
VOL output voltage logic low level	IOL = 4mA; Figure 8-1		0.2	0.4	In
VIT+(IN) positive input threshold		1.4	1.67	1.9	In
VIT-(IN) negative input threshold		1.0	1.23	1.4	In
VI(HYS) Input threshold hysteresis Input		0.30	0.44	0.50	In
IIH high level leakage current	VIH = VDDA at Ax or Bx or ENx			4	µA
IIL Input low level leakage current Output impedance	VIL = 0 V at Ax or Bx	-4			µA
LIKE THIS 2			50		Oh
CMTI Common Mode Transient Immunity	VI = VDDI1 or 0 V, VCM = 1200 V; Figure 8-3	75	100		kV/µS
THERE Input Capacitor 3	VI = VDD/ 2 + 0.4×sin(2ÿft), f = 1 MHz, VDD = 5 V		2		pF
Remark: 1. VDDI = input side VDD, VDDO = output side VDD 2. The output impedance of a normal isolator channel is about 50ÿ±40%. 3. Measured from pin to ground.					

7.8.2. VDDA = VDDB = 3.3 V ± 10%, TA = -40 to 125°C

parameter	Test conditions	Min. Typ. Max. Unit VDDO1 -0.4 3.1			
VOH output voltage logic high level	IOH = -4mA; Figure 8-1				In
VOL output voltage logic low level	IOL = 4mA; Figure 8-1		0.2	0.4	In
VIT+(IN) positive input threshold		1.4	1.67	1.9	In
VIT-(IN) negative input threshold		1.0	1.23	1.4	In
VI(HYS) Input threshold hysteresis Input		0.30	0.44	0.50	In
IIH high level leakage current	VIH = VDDA at Ax or Bx or ENx			4	µA
IIL Input low level leakage current	VIL = 0 V at Ax or Bx	-4			µA
LIKE THIS output impedance 2			50		Oh
CMTI Common Mode Transient Immunity	VI = VDDI1 or 0 V, VCM = 1200 V; Figure 8-3	75	100		kV/µs
THERE Input Capacitor 3	VI = VDD/ 2 + 0.4×sin(2ÿft), f = 1 MHz, VDD = 3.3 V		2		pF
Remark: 1. VDDI = input side VDD, VDDO = output side VDD 2. The output impedance of a normal isolator channel is approximately 50ÿ±40%. 3. Measured from pin to ground.					

7.8.3. VDDA = VDDB = 2.5 V ± 5%, TA = -40 to 125°C

parameter	Test conditions	Min. Typ. Max. Unit VDDO1 -0.4 2.3			
VOH output voltage logic high level	IOH = -4mA; Figure 8-1				In
VOL output voltage logic low level	IOL = 4mA; Figure 8-1		0.2	0.4	In
VIT+(IN) positive input threshold		1.4	1.67	1.9	In
VIT-(IN) negative input threshold		1.0	1.23	1.4	In
VI(HYS) Input threshold hysteresis Input high level leakage		0.30	0.44	0.50	In
IIH current Input low level leakage current	VIH = VDDA at Ax or Bx or ENx			4	µA
IIL Output impedance 2	VIL = 0 V at Ax or Bx	-4			µA
LIKE THIS			50		Oh
CMTI Common Mode Transient Immunity	VI = VDDI1 or 0 V, VCM = 1200 V; Figure 8-3	75	100		kV/µS
THERE Input Capacitor 3	VI = VDD/ 2 + 0.4×sin(2ÿft), f = 1 MHz, VDD = 2.5 V		2		pF
Remark:					

VDDI = input side VDD, VDDO = output side VDD

2. The output impedance of a normal isolator channel is about 50ÿ±40%.

3. Measured from pin to ground.

7.9.Power supply current characteristics

7.9.1. VDDA = VDDB = 5 V ± 10%, TA = -40 to 125°C

Parameter test conditions			Supply Current	Min	Typ	Max	Unit
CA-IS3710							
Supply Current – DC Signal	VIN = 0V (CA-IS3710L); VIN = VDDA (CA-IS3710H)		IDDA		0.7	1.0	m.a.
			IDDB		0.9	1.4	
	VIN = VDDA (CA-IS3710L); VIN = 0V(CA-IS3710H)		IDDA		1.4	2.1	
			IDDB		0.9	1.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.0	1.5	
			IDDB		1.0	1.5	
		10Mbps (5MHz)	IDDA		1.0	1.5	
			IDDB		1.5	2.2	
		100Mbps (50MHz)	IDDA		1.0	1.5	
			IDDB		6.2	9.3	
CA-IS3720							
Supply Current – DC Signal	VIN = 0V (CA-IS3720L); VIN = VDDI [1] (CA-IS3720H)		IDDA		0.8	1.2	m.a.
			IDDB		1.6	2.3	
	VIN = VDDI (CA-IS3720L); VIN = 0V(CA-IS3720H)		IDDA		2.3	3.5	
			IDDB		1.6	2.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.6	2.3	
			IDDB		1.7	2.6	
		10Mbps (5MHz)	IDDA		1.6	2.3	
			IDDB		2.7	4.0	
		100Mbps (50MHz)	IDDA		1.6	2.3	
			IDDB		12.2	18.2	
CA-IS3721							
Supply Current – DC Signal	VIN = 0V (CA-IS3721L); VIN = VDDI (CA-IS3721H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3721L); VIN = 0V(CA-IS3721H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.2	3.3	
			IDDB		2.2	3.3	
		100Mbps (50MHz)	IDDA		7.0	10.5	
			IDDB		7.0	10.5	
CA-IS3722							
Supply Current – DC Signal	VIN = 0V (CA-IS3722L); VIN = VDDI (CA-IS3722H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3722L); VIN = 0V(CA-IS3722H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.2	3.3	
			IDDB		2.2	3.3	
		100Mbps (50MHz)	IDDA		7.0	10.5	
			IDDB		7.0	10.5	

Remark:

1. VDDI = input side VDD

C 7.9.2. VDDA = VDDB = 3.3 V ± 10%, TA = -40 to 125°C

parameter	Test conditions		Supply Current	Min	Typ	Max	Unit
CA-IS3710							
Supply Current – DC Signal	VIN = 0V (CA-IS3710L); VIN = VDDA (CA-IS3710H)		IDDA		0.7	1.0	m.a.
			IDDB		0.9	1.4	
	VIN = VDDA (CA-IS3710L); VIN = 0V(CA-IS3710H)		IDDA		1.4	2.1	
			IDDB		0.9	1.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.0	1.5	
			IDDB		1.0	1.5	
		10Mbps (5MHz)	IDDA		1.0	1.5	
			IDDB		1.3	2.0	
		100Mbps (50MHz)	IDDA		1.0	1.5	
			IDDB		4.7	7.1	
CA-IS3720							
Supply Current – DC Signal	VIN = 0V (CA-IS3720L); VIN = VDDI [1] (CA-IS3720H)		IDDA		0.8	1.2	m.a.
			IDDB		1.6	2.3	
	VIN = VDDI (CA-IS3720L); VIN = 0V(CA-IS3720H)		IDDA		2.3	3.5	
			IDDB		1.6	2.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.6	2.3	
			IDDB		1.7	2.6	
		10Mbps (5MHz)	IDDA		1.6	2.3	
			IDDB		2.4	3.6	
		100Mbps (50MHz)	IDDA		1.6	2.3	
			IDDB		9.2	13.7	
CA-IS3721							
Supply Current – DC Signal	VIN = 0V (CA-IS3721L); VIN = VDDI (CA-IS3721H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3721L); VIN = 0V(CA-IS3721H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.1	3.2	
			IDDB		2.1	3.2	
		100Mbps (50MHz)	IDDA		5.5	8.2	
			IDDB		5.5	8.2	
CA-IS3722							
Supply Current – DC Signal	VIN = 0V (CA-IS3722L); VIN = VDDI (CA-IS3722H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3722L); VIN = 0V(CA-IS3722H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.1	3.2	
			IDDB		2.1	3.2	
		100Mbps (50MHz)	IDDA		5.5	8.2	
			IDDB		5.5	8.2	

Remark:

1. VDDI = input side VDD

7.9.3. VDDA = VDDB = 2.5 V ± 5%, TA = -40 to 125°C

Parameter test conditions			Supply Current	Min	Typ	Max	Unit
CA-IS3710							
Supply Current – DC Signal	VIN = 0V (CA-IS3710L); VIN = VDDA (CA-IS3710H)		IDDA		0.7	1.0	m.a.
			IDDB		0.9	1.4	
	VIN = VDDA (CA-IS3710L); VIN = 0V(CA-IS3710H)		IDDA		1.4	2.1	
			IDDB		0.9	1.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.0	1.5	
			IDDB		1.0	1.5	
		10Mbps (5MHz)	IDDA		1.0	1.5	
			IDDB		1.2	1.8	
		100Mbps (50MHz)	IDDA		1.0	1.5	
			IDDB		3.7	5.6	
CA-IS3720							
Supply Current – DC Signal	VIN = 0V (CA-IS3720L); VIN = VDDI [1] (CA-IS3720H)		IDDA		0.8	1.2	m.a.
			IDDB		1.6	2.3	
	VIN = VDDI (CA-IS3720L); VIN = 0V(CA-IS3720H)		IDDA		2.3	3.5	
			IDDB		1.6	2.4	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.6	2.3	
			IDDB		1.7	2.6	
		10Mbps (5MHz)	IDDA		1.6	2.3	
			IDDB		2.2	3.3	
		100Mbps (50MHz)	IDDA		1.6	2.3	
			IDDB		7.2	10.7	
CA-IS3721							
Supply Current – DC Signal	VIN = 0V (CA-IS3721L); VIN = VDDI (CA-IS3721H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3721L); VIN = 0V(CA-IS3721H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.0	3.0	
			IDDB		2.0	3.0	
		100Mbps (50MHz)	IDDA		4.5	6.7	
			IDDB		4.5	6.7	
CA-IS3722							
Supply Current – DC Signal	VIN = 0V (CA-IS3722L); VIN = VDDI (CA-IS3722H)		IDDA		1.3	2.0	m.a.
			IDDB		1.3	2.0	
	VIN = VDDI (CA-IS3722L); VIN = 0V(CA-IS3722H)		IDDA		2.1	3.1	
			IDDB		2.1	3.1	
Supply Current – AC Signal	All channels input 50% duty cycle, amplitude is 5V square wave; CL = 15 pF per channel	1Mbps (500kHz)	IDDA		1.8	2.6	
			IDDB		1.8	2.6	
		10Mbps (5MHz)	IDDA		2.0	3.0	
			IDDB		2.0	3.0	
		100Mbps (50MHz)	IDDA		4.5	6.7	
			IDDB		4.5	6.7	

Remark:

1. VDDI = input side VDD

Timing Characteristics

7.10.1. VDDA = VDDB = 5 V ± 10%, TA = -40 to 125°C

parameter	Test Description	Min	Typ	Max	Unit
DR Data Rate			0	150	Mbps
PWmin minimum pulse width				5.0	ns
tPLH, tPHL propagation delay	Figure 8-1		5.0 8.0	13.0	ns
PWD Pulse Width Distortion |tPLH - tPHL| tsk(o)			0.2	4.5	ns
Channel-to-channel output skew time1	Same direction channel		0.4	2.5	ns
tsk(pp) Part-to-part Skew Time2			2.0	4.5	ns
tr output rise time	Figure 8-1		2.5	4.0	ns
tf Output Fall Time	Figure 8-1		2.5	4.0	ns
tDO default output delay time from input power loss	Figure 8-2		8	12	ns
tSU startup time notes:			15	40	µs

1. tsk(o) is the deviation between the output of a single device with all driving inputs connected together and the output switching in the same direction when driving the same load.

2. tsk(pp) is the difference in propagation delay time between any terminals of different devices switching in the same direction under the same supply voltage, temperature, input signal and load.

7.10.2. VDDA = VDDB = 3.3 V ± 10%, TA = -40 to 125°C

parameter	Test Description	Min	Typ	Max	Unit
DR Data Rate			0	150	Mbps
PWmin minimum pulse width				5.0	ns
tPLH, tPHL propagation delay	Figure 8-1	1.0	8.0	13.0	ns
PWD Pulse Width Distortion |tPLH - tPHL| tsk(o)			0.2	4.5	ns
Channel-to-channel output skew time1	Same direction channel		0.4	2.5	ns
tsk(pp) Part-to-part Skew Time2			2.0	4.5	ns
tr output rise time	Figure 8-1		2.5	4.0	ns
tf Output Fall Time	Figure 8-1		2.5	4.0	ns
tDO default output delay time from input power loss	Figure 8-2		8	12	ns
tSU Startup time			15 40		µs

Remark:

1. tsk(o) is the deviation between the output of a single device with all driving inputs connected together and the output switching in the same direction when driving the same load.

2. tsk(pp) is the difference in propagation delay time between any terminals of different devices switching in the same direction under the same supply voltage, temperature, input signal and load.

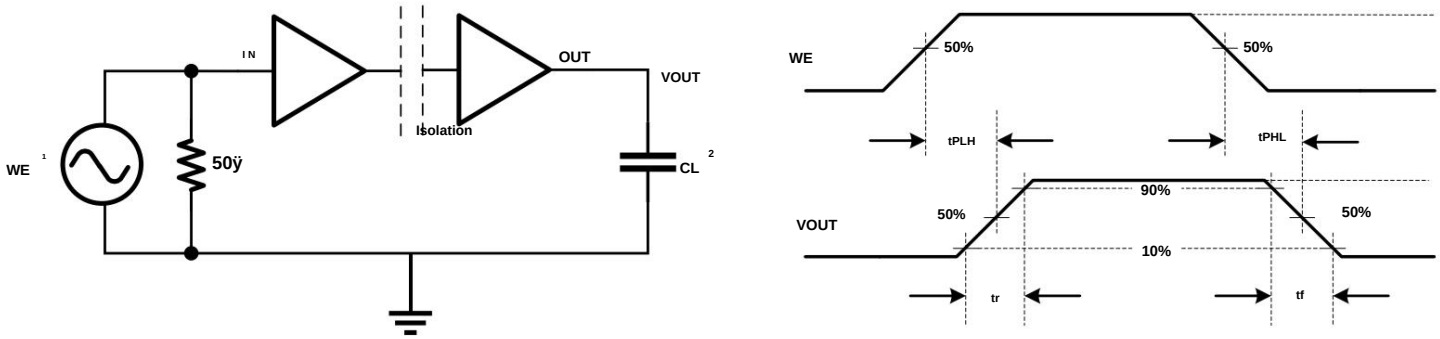
7.10.3. VDDA = VDDB = 2.5 V ± 5%, TA = -40 to 125°C

parameter	Test Description	Min	Typ	Max	Unit
DR Data Rate			0	150	Mbps
PWmin minimum pulse width				5.0	ns
tPLH, tPHL propagation delay	Figure 8-1	5.0	8.0	13.0	ns
PWD Pulse Width Distortion |tPLH - tPHL| tsk(o)			0.2	5.0	ns
Channel-to-channel output skew time1	Same direction channel		0.4	2.5	ns
tsk(pp) Part-to-part Skew Time2			2.0	5.0	ns
tr output rise time	Figure 8-1		2.5	4.0	ns
tf Output Fall Time	Figure 8-1		2.5	4.0	ns
tDO default output delay time from input power loss	Figure 8-2		8	12	ns
tSU startup time notes:			15	40	µs

1. tsk(o) is the deviation between the output of a single device with all driving inputs connected together and the output switching in the same direction when driving the same load.

2. tsk(pp) is the difference in propagation delay time between any terminals of different devices switching in the same direction under the same supply voltage, temperature, input signal and load.

8. Parameter measurement information



Remark:

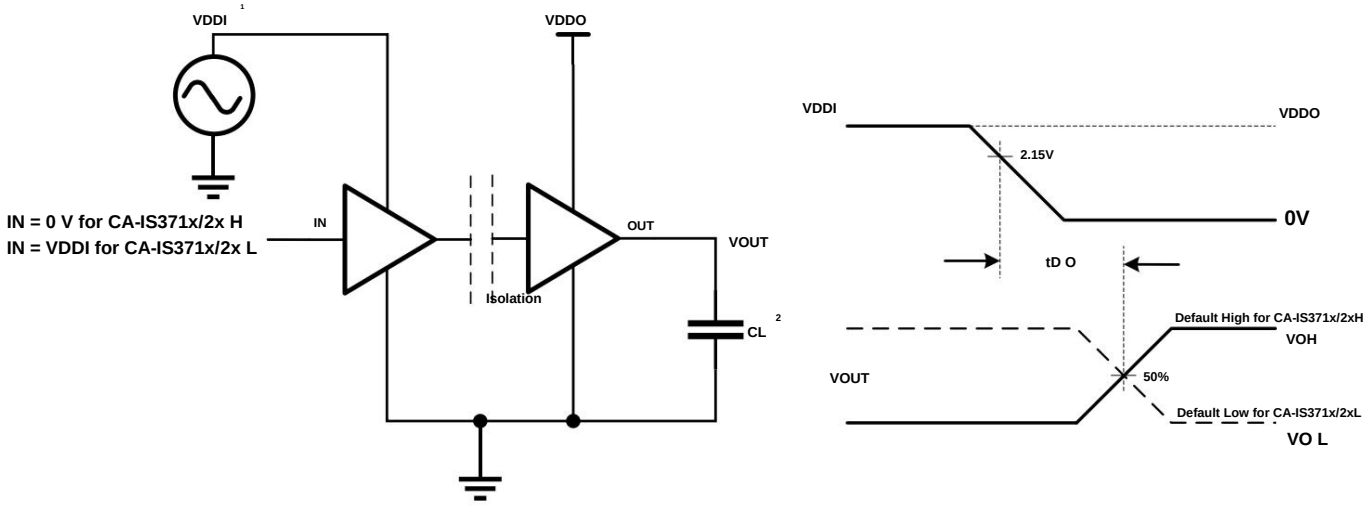
1. The signal generator generates the input signal VIN with the following constraints: waveform frequency ÿ 100kHz, duty cycle 50%, tr ÿ 3ns, tf ÿ 3ns.

   The output impedance Zout = 50ÿ, the 50ÿ resistor in the figure is used for matching. It is not necessary in practical applications.

2. CL is the load capacitance of approximately 15pF and the instrument capacitance. Since the load capacitance affects the output rise time, it is a key factor in timing characteristics measurement.

   white.

Figure 8-1 Timing characteristics test circuit and voltage waveform



Remark:

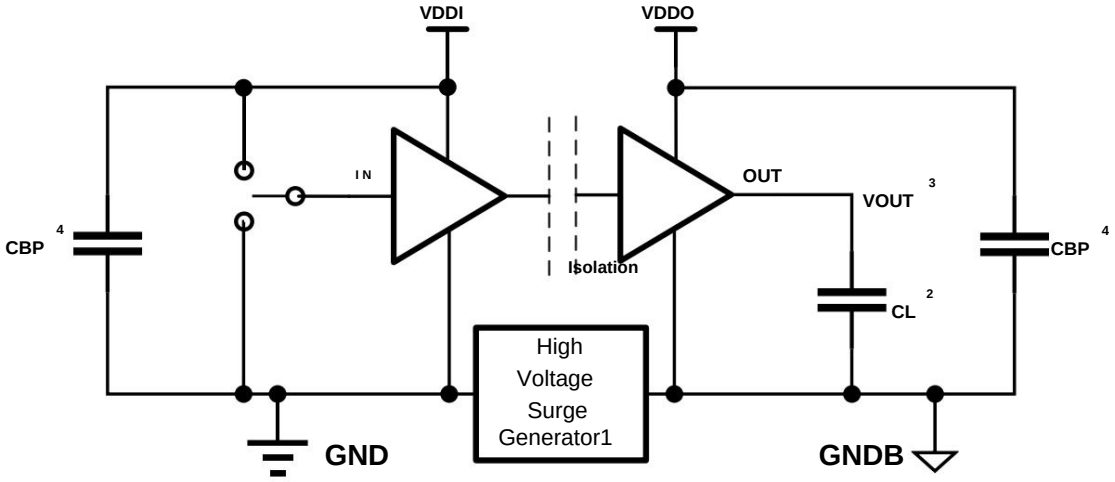
1. The signal generator generates the input signal VIN with the following constraints: waveform frequency ÿ 100kHz, duty cycle 50%, tr ÿ 3ns, tf ÿ 3ns.

   The output impedance Zout = 50ÿ, the 50ÿ resistor in the figure is used for matching. It is not necessary in practical applications.

2. CL is the load capacitance of approximately 15pF and the instrument capacitance. Since the load capacitance affects the output rise time, it is a key factor in timing characteristics measurement.

   white.

Figure 8-2 Default output delay time test circuit and voltage waveform



Remark:

1. The high voltage surge pulse generator generates repetitive high voltage pulses with amplitude > 1kV, rise/fall time <10ns, and common mode transient noise slew rate > 100kV/ÿs.
   rush.
2. CL is the load capacitance of approximately 15pF plus the instrument capacitance.
3. Pass-Fail Criteria: The output must remain stable whenever a high voltage surge occurs.
4. CBP is a bypass capacitor of 0.1~1uF.

Figure 8-3 Common mode transient immunity test circuit

Detailed description

9.1. Working Principle

The CA-IS371x/2x family of devices uses a simple on-off keying (OOK) modulation scheme to transmit signals between SiO2 isolation capacitors that are connected between two

The transmitter (TX) modulates the input signal onto the carriers.

In frequency, that is, TX passes a high frequency signal across the isolation barrier in one input state, but does not pass any signal across the isolation barrier in the other input state.

The receiver then reconstructs the incoming signal based on the detected in-band energy. This simple architecture provides a reliable isolated data path that does not require

Special consideration should be given to initialization. The capacitor-based signal path is fully differential to maximize noise immunity, also known as common-mode transient immunity.

The use of advanced circuit technology can suppress the EMI introduced by the carrier signal and IO switch. Compared with the inductive coupling structure, the capacitive coupling structure has higher

The OOK modulation scheme eliminates the pulse leakage error that occurs in the pulse modulation method. Figure 9-1 and Figure 9-2 are simplified functional block diagrams and

Concept operation waveform.

9.2. Functional block diagram

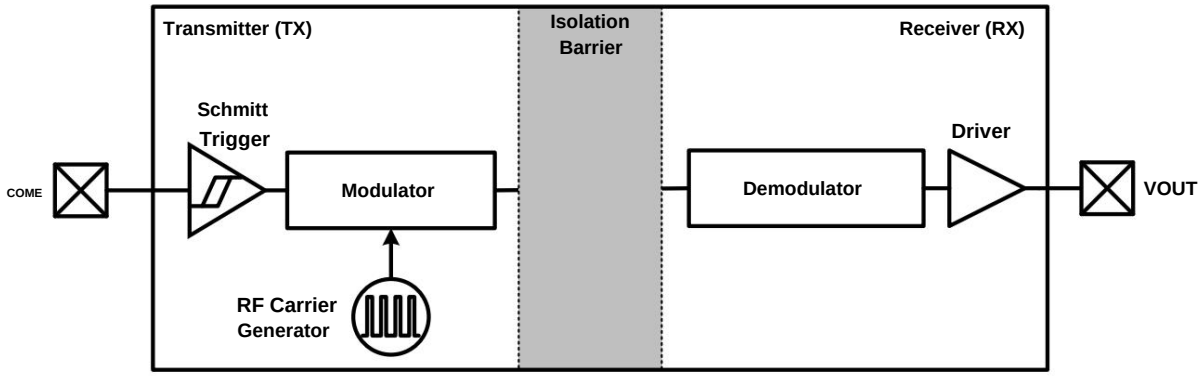


Figure **9-1** Single channel functional block diagram

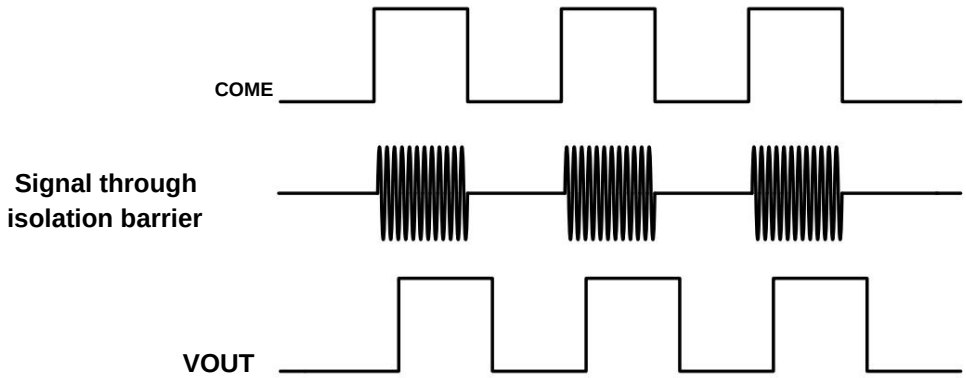


Figure **9-2** Single channel conceptual waveform

Table 9-1 CA-IS371x/2x device truth table.

Table **9-1** Truth Table **1**

VDDI	VDDO	Input (Ax/Bx) 2	Output Enable (ENx) 3, 4	Output (Ax/Bx)	
COULD	COULD	H	H		Normal operation mode: The output of the channel follows the channel input state
		L	L		
		Open	Default		Default output fail-safe mode: If the input of a channel remains disconnected, its output will go to the default value (low for CA-IS371x/2xL and high for IS371x/2xH). THAT-
PD	COULD	X	Default		Default output fail-safe mode: If the input side VDD is not powered, the output enters the default output fail-safe mode (CA-IS371x/2xL is low power). level, CA-IS371x/2xH is high level).
X	PD	X	Undetermined	If the output side VDD is not powered, the output state is undetermined. 3	

Remark:

1. VDDI = input side VDD; VDDO = output side VDD; PU = power on (VCC ÿ 2.375 V); PD = power off (VCC ÿ 2.25 V); X = don't care; H = high level; L = low level.

2. A strongly driven input signal can weakly drive the floating VDD through the internal protection diode, resulting in an uncertain output.

3. When 2.25V < VDDI, VDDO < 2.375 V, the output is in an uncertain state.

10. Application Circuit

Unlike optocouplers that require external components to provide bias or current limiting performance, the CA-IS371x/2x series of CMOS digital isolators require only two external VDD

The TTL-compatible inputs draw only microamps of leakage current and can be driven without external buffer circuits.

The characteristic impedance of the output is 50ÿ (rail-to-rail swing), and forward and reverse channel configurations are available. Figure 10-1 shows a typical application of the CA-IS3721 device.

The circuit of 10-2 is a typical application circuit of CA-IS37xx series products and is as easy to use as a standard logic gate.

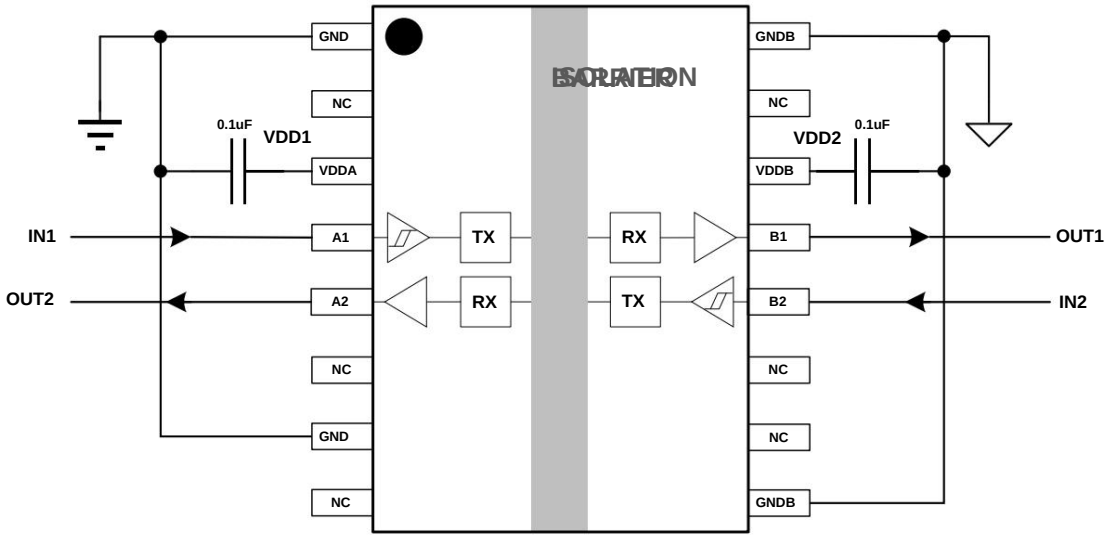


Figure 10-1 Typical application circuit of **SOIC-16 CA-IS3721**

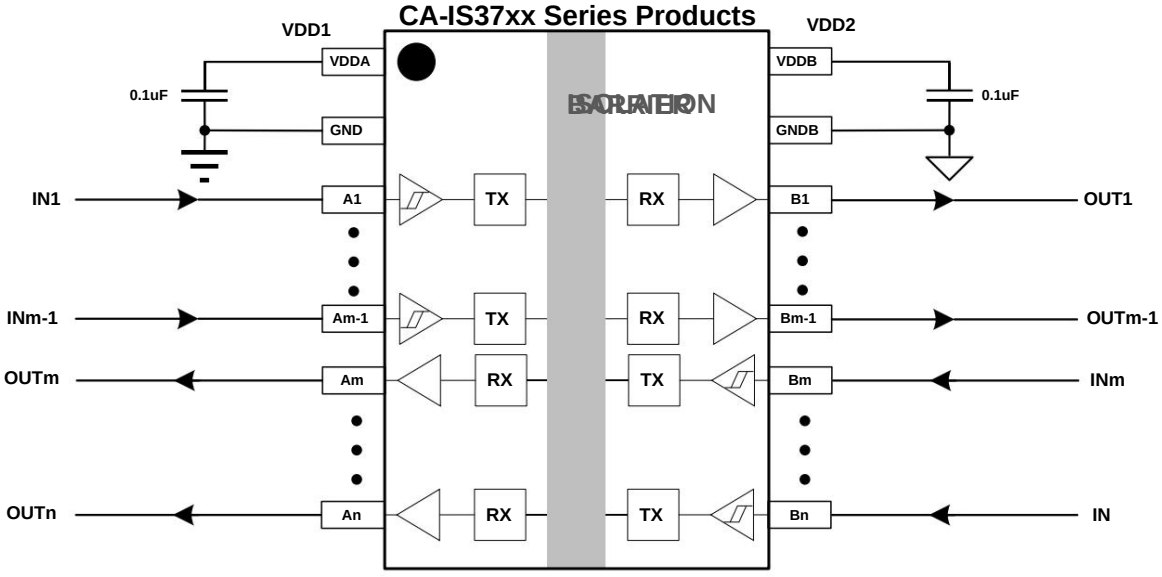


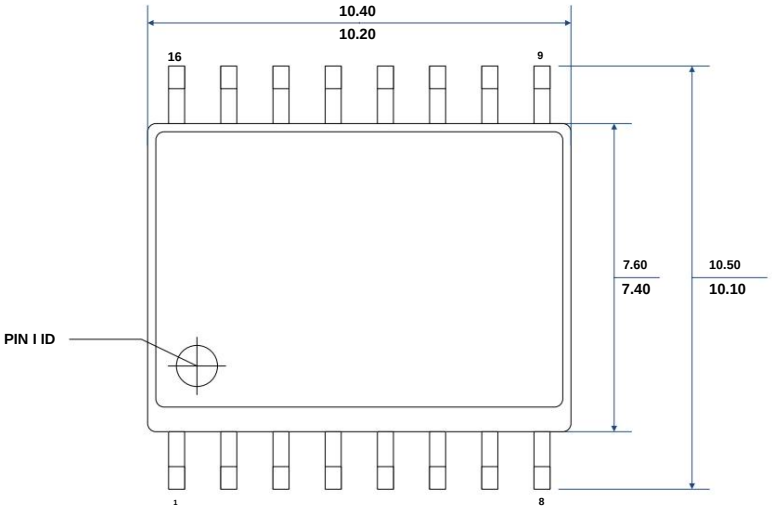
Figure **10-2 CA-IS37xx** series digital isolator application schematic

Packaging Information

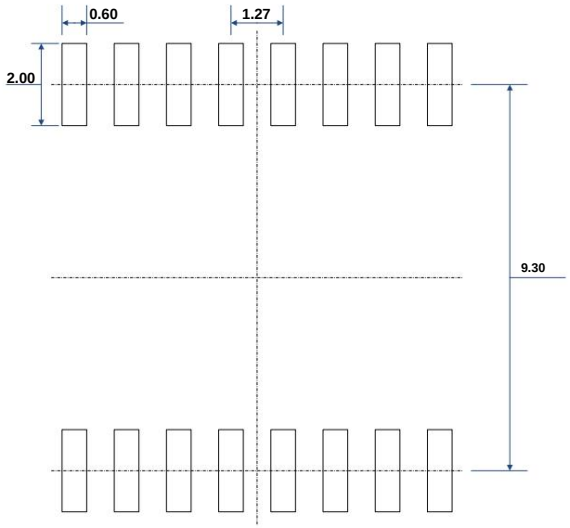
11.1. SOIC-16WB Wide Body Dimensions

The following figure shows the dimensions and recommended pad dimensions of the CA-IS371x/2x series digital isolators in the SOIC-16WB wide-body package. Dimensions are in millimeters.

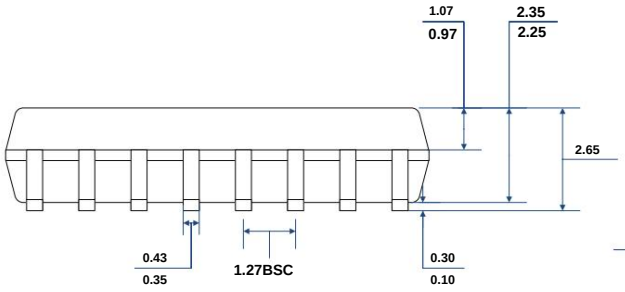
unit



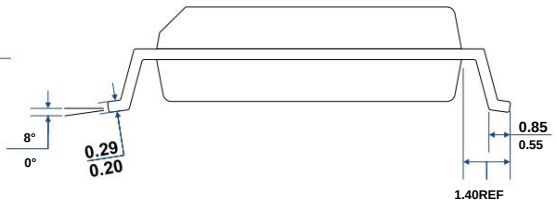
TOP VIEW



RECOMMENDED LAND PATTERN



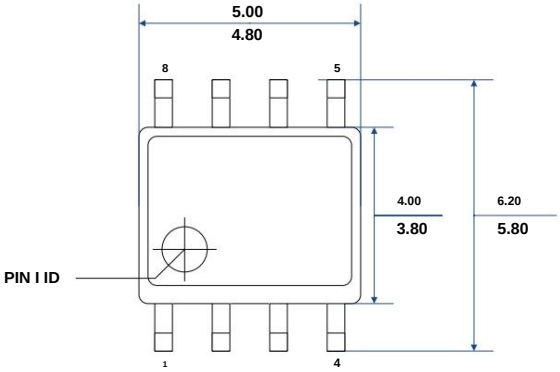
FRONT VIEW



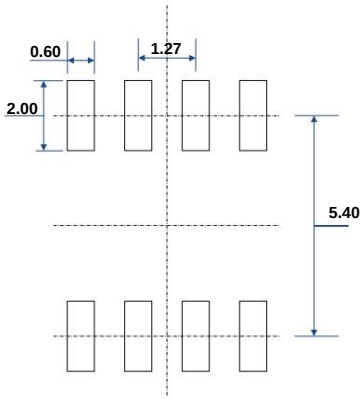
LEFT-SIDE VIEW

11.2. SOIC8 Narrow Body Dimensions

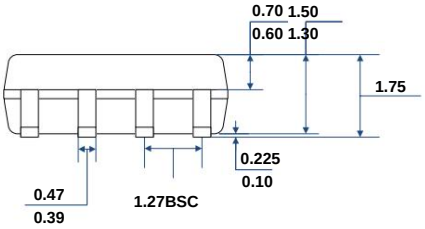
The following figure illustrates the dimensions and recommended pad dimensions of the CA-IS371x/2x series digital isolators in a SOIC-8 narrow package. Dimensions are in millimeters.



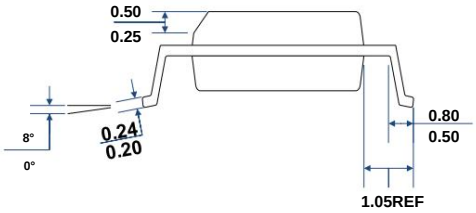
TOP VIEW



RECOMMENDED LAND PATTERN



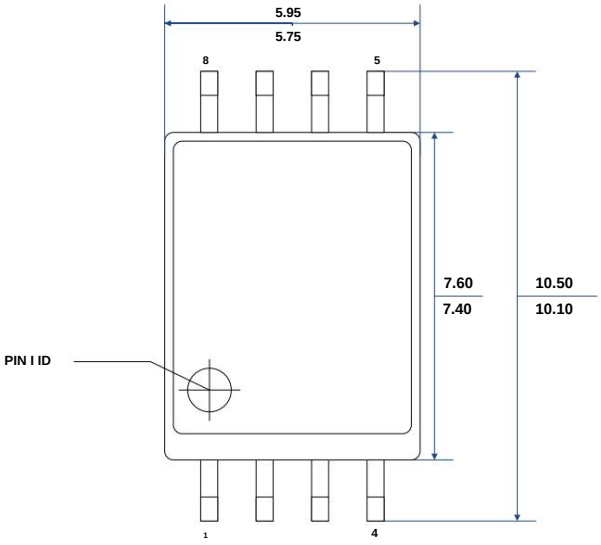
FRONT VIEW



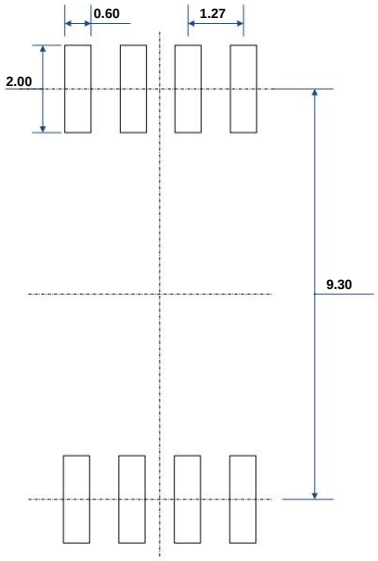
LEFT-SIDE VIEW

SOIC8 Wide Body Dimensions

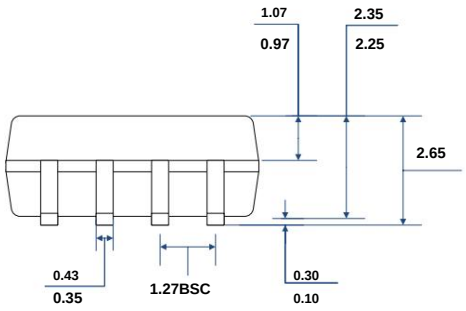
The following figure illustrates the dimensions and recommended pad dimensions of the CA-IS371x/2x series digital isolators in SOIC-8 wide-body package. Dimensions are in millimeters.



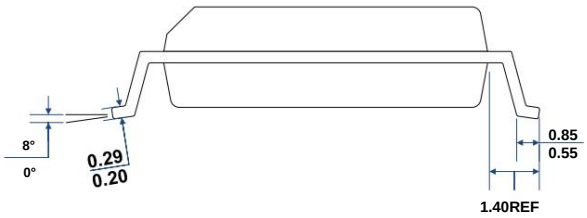
TOP VIEW



RECOMMENDED LAND PATTERN



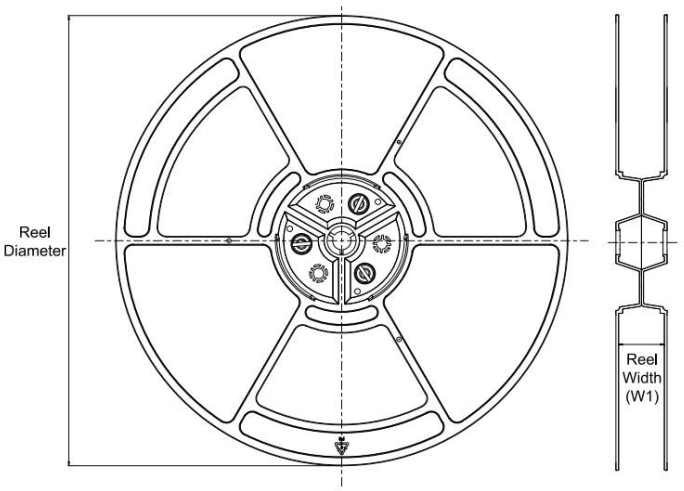
FRONT VIEW



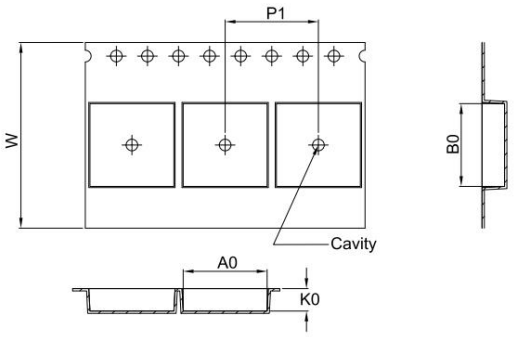
LEFT-SIDE VIEW

TAPE AND REEL INFORMATION

REEL DIMENSIONS

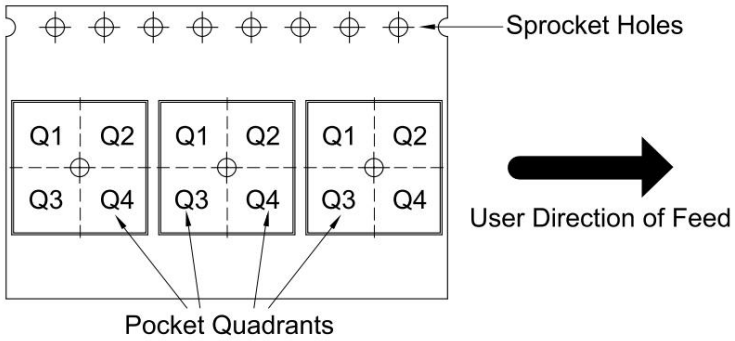


TAPE DIMENSIONS



A0 Dimension designed to accommodate the component width
B0 Dimension designed to accommodate the component length
K0 Dimension designed to accommodate the component thickness
W Overall width of the carrier tape
P1 Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	IN (mm)	Pin1 Quadrant
CA-IS3710LSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3710LWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3710HSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3710HWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3720LSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3720LGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1
CA-IS3720LWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3720HSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3720HGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1
CA-IS3720HWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3721LSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3721LGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1
CA-IS3721LWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3721HSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3721HGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1
CA-IS3721HWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3722LSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3722LGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1

CA-IS3722LWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3722HSR	SOIC	S	8	5000	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3722HGR	SOIC	G	8	5000	330	16.4	6.5	10.7	2.9	12.0	24.0	Q1
CA-IS3722HWR	SOIC W 16			1200	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

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