11Clock Management Unit (CMU)

11.1 Overview

The chip contains a 32.768KHz low-frequency crystal oscillator circuit (XTLF), a 4~32MHz high-frequency crystal oscillator, and a maximum high-frequency RC oscillator (RCHF), 32KHz low power internal loop (LPOSC), 4MHz low power loop, and a phase-locked loop (PLL).

The clock generation module inside the chip combines these clock sources to generate the clock required for each module to work.

Features:

ÿ The system main clock can select multiple clock sources

ÿ The clock can be switched in real time during system operation

ÿ Low frequency crystal oscillator equipped with stop detection circuit

ÿ Some peripheral modules have independent working clocks (decoupled from CPU and line clocks)

ÿ CPU and line maximum frequency 64MHz

11.2 Clock Architecture

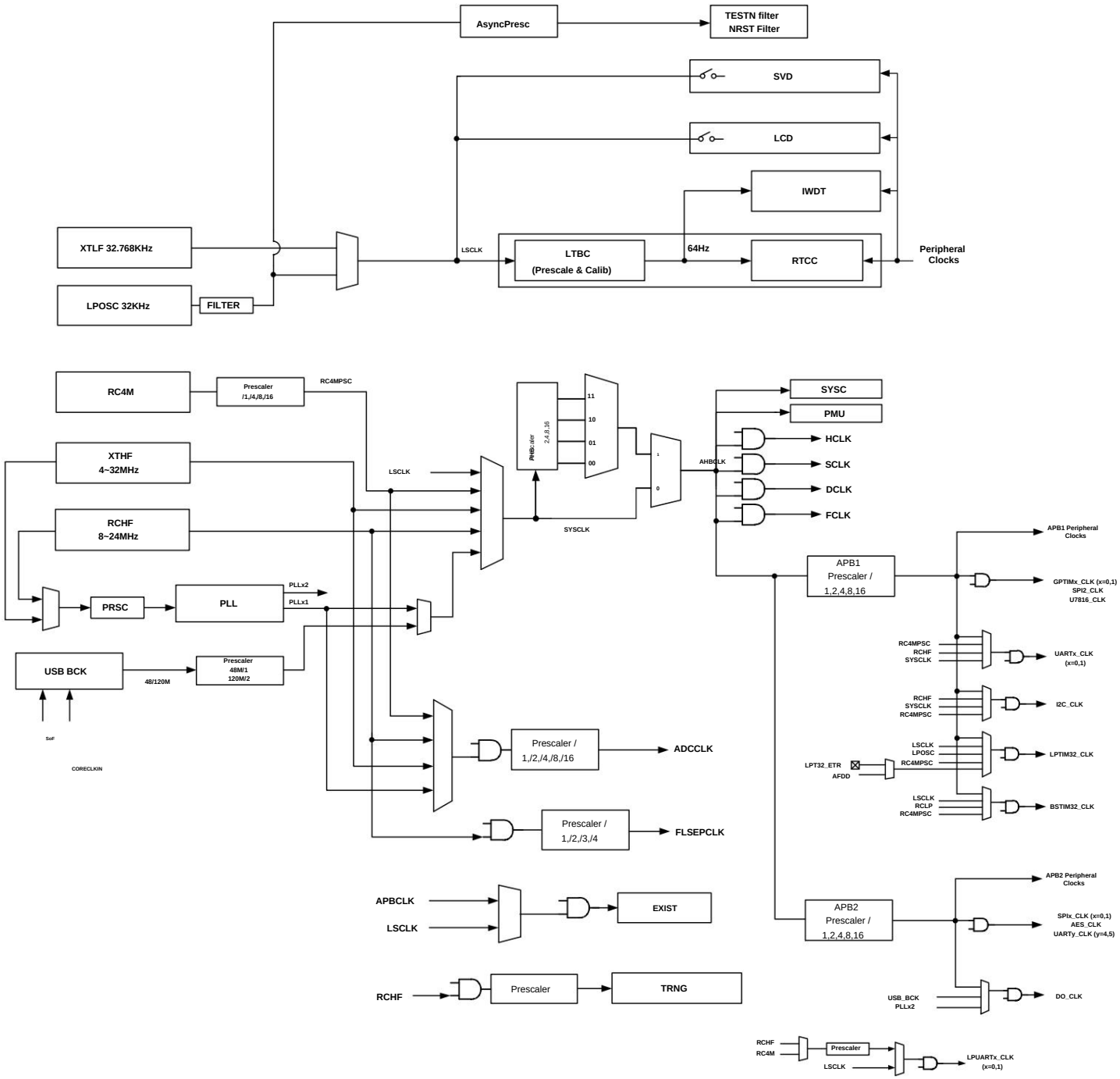

Figure **11-1** Chip clock block diagram

The system main clock (SYSCLK) can be generated by XTLF, RCHF, LPOSC, PLL, XTHF, RCMF and their divided clocks.

The default 8MHz RCHF clock is used as the main system clock when powered on, and the clocks of each peripheral module can be controlled independently.

When the chip is working, only the module clock that needs to work can be turned on, and the clocks of other modules can be turned off to save power.

APBCLK can be a divided-frequency clock of AHBCLK, which is used to drive low-speed peripherals on the APB line.

11.2.1 SYSCLK Switching Instructions

SYSCLK is the main system clock. From SYSCLK, you can get line clocks such as AHBCLK and APBCLK, as well as the clocks required for CPU operation. clock.

When SYSCLK selects any clock source, the hardware will check whether the corresponding clock source is enabled. If the clock source is not enabled, In software switching, the SYSCLKSEL register will not be written and clock switching will not occur.

Target clock	Switching Condition
RCHF	RCHF Enable
RCMF	RCMF Enable
XTHF	XTHF is enabled and not stopped
PLL	The PLL is enabled and: 1. If the PLL reference clock is XTHF, then XTHF must be enabled and not stopped. 2. If the PLL reference clock is RCHF, then RCHF Must be enabled
XTLF	XTLF is enabled and not stopped
USB BCK	USB BCK module enable (USB series models only)

Table **11-1** System clock switching conditions

11.2.2 Main clock description

clock	source	illustrate
LSCLK	XTLF, LPOSC	32KHz low frequency system clock, can be switched when crystal stops To LPOSC Mainly used for RTC, IWDT, foot filter, SVD, LCD
SYSCLK	RCHF, PLL,LSCLK, XTHF, RCMF, USB_BCK	32K~64MHz, after frequency division to AHBCLK
HCLK(AHBCLK) SYSCLK		AHB line clock, used to drive CPU, RAM, Flash and high-speed peripherals
SCLK	SYSCLK	CPU core system clock
DCLK	SYSCLK	CPU core debug clock (the emulator is connected to this The clock must be active)
FCLK	SYSCLK	Free-Running clock, supplying CPU core WIC Modules, and APB bridges
APBCLK	AHBCLK	APB line clock, used to drive low-speed peripherals

Table **11-2** Description of main system clocks

11.2.3 Bus Clock and Working Clock of Peripheral Modules

The line clock and working clock of some peripheral modules are independent of each other.

The line clock is used for AHBAPB line access. When the software accesses the function register of the peripheral, it must first pass the peripheral line clock. Clock register to enable the corresponding line clock.

The working clock of the peripheral is the clock used by the peripheral to actually work. This clock may be different from APBCLKAHBCLK.

Before the block works, it is necessary to select the required clock source through the peripheral working clock register and open the clock gate.

For peripheral modules with unified working clock and line clock, you only need to enable the line clock to work normally.

Modules	Line clock	Working clock
independent working clock peripheral		
UARTx (x=0,1)	APB1CLK	APBCLK
		RCHF
		SYSCLK
		RCMF
LPUART0	APB1CLK	LSCLK
		RCHF
		RCMF
LPUART1	APB2CLK	LSCLK
		RCHF
		RCMF
I2C	APB1CLK	APBCLK
		RCHF
		SYSCLK
		RCMF
ATIM	APB2CLK	APBCLK
		USB_BCK
		PLLx2_CLK
LPTIM32	APB1CLK	APBCLK
		LSCLK
		LPOSC
		LPTIN
BSTIM32	APB2CLK	APBCLK
		LSCLK
		LPOSC
		RCMF_PSC
ADC	APB2CLK	RCMF
		XTHF
		RCHF
		PLL
NVMIF (Flash erase/program)	AHBCLK	RCHF
EXIT (PADCFG)	AHBCLK	AHBCLK
		LSCLK
TRNG	APB2CLK	RCHF
IWDT	APB1CLK	LSCLK
LCD	APB1CLK	LSCLK
RTC	APB1CLK	LSCLK
Non-independent clock peripherals		
PMU	AHBCLK	
DMA	AHBCLK	
GPTIMx	APB1CLK	
UARTy (y=4.5)	APB2CLK	

Modules	Line clock	Working clock
SPI2	APB1CLK	
SPI1	APB2CLK	
7816	APB1CLK	
AES	APB2CLK	
CRC	APB2CLK	
WWDT	APB1CLK	
OPAx	APB2CLK	
COMPx	APB2CLK	

Table **11-3** Bus clock and peripheral working clock

11.2.4 Peripheral clocks in sleep mode

In Sleep/DeepSleep mode, SYSCLK is turned off, so AHBCLK and APBCLK do not work in sleep mode.

All peripherals based on AHBCLKAPBCLK stop working. However, peripherals using independent line clocks can continue to work.

operations, such as UART0/1, LPUARTx, I2C, ATIM, LPTIM32, BSTIM32.

In order for the above peripherals to continue to work in sleep mode, the software needs to ensure that the above peripherals use SYSCLK and line clock before sleep.

Other clocks work.

11.2.5LSCLK Switching Logic

LSCLK is a low-speed clock used by RTC, IWDT, SVD and LCD driver, with a typical frequency of about 32K. The source of LSCLK is

XTLF or LPOSC, the chip switches automatically or automatically by software.

The automatic switching function of LSCLK is configured by the LSACTS register and is only available when XTLF is enabled.

The main clock, LPOSC is the backup clock, which is only used to prevent XTLF from stopping abnormally. LSCATS starts only when XTLF is enabled.

If XTLF stops externally, the stop signal output by FDET will automatically switch LSCLK to LPOSC.

When LSCLK automatic switching is disabled, the software can implement dynamic switching of LSCLK through the LSCLKSEL register.

After the chip is powered on and reset, XTLFEN=0, LFDET output is continuous, LSCLKSEL selects LPOSC by default, and XTLF output;

Therefore, after power-on, LSCLK defaults to LPOSC.

After that, if the software wants to use XTLF, it should enable XTLF and poll the LFDET output until XTLF is confirmed to be on.

LSCATS is set, while LSCLKSEL is cleared.

When LSCLK is used as the system clock (SYSCLK), it is recommended to enable or disable the automatic switching function in software.

11.3 USB PHY BCK

The built-in clock source of USB PHY can use the internal reference clock of the line SoF chip to do clock self-calibration to obtain accurate

48/96/120M output.

When PHY uses the chip's internal clock as the reference clock, the CMU module is required to output the reference clock, whose frequency can be 12M or 32768Hz. Its clock source can come from the internal loop of the crystal, as shown in the following figure:

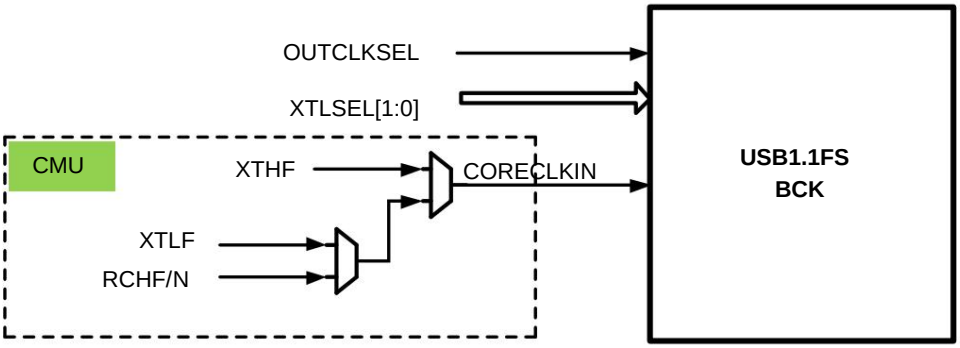

Figure **11-2 USB PHY** reference clock source selection

11.4 High Frequency **RC Oscillator (RCHF)**

11.4.1 Overview

The typical oscillation frequency of the high-frequency RC oscillator is 8/16/24MHz, which can be used as the system main clock. When the MCU works at this frequency, it can achieve

To meet the requirements of different applications for MCU speed, the output frequency of the high-frequency RC oscillator is adjustable, with a maximum

The RCHF output frequency can be adjusted to within +/-1% of the target frequency before leaving the factory.

The frequency variation in the temperature range (-40~+85°C) is less than +/-1%, and the frequency variation in the full temperature range (-40~+85°C) of 16MHz output is less than +/-2%.

11.4.2 Software Instructions

After the chip is powered on, it uses the RCHF 8MHz clock by default. The hardware circuit will automatically read the 8MHz calibration value from the Flash to ensure the 8MHz

The frequency error is less than +/-0.5%.

If the software needs to use another frequency, follow the steps below:

ÿ Write RCHF_CR.FSEL

ÿ Read the frequency adjustment value from Flash (0x1FFF_FB40, 0x1FFF_FB3C, 0x1FFF_FB38) (corresponding to

8/16/24MHzÿ

ÿ Write the frequency adjustment value into the RCHF_TR register to get a clock with a target frequency error less than +/-1%

The RCHF calibration parameters in Flash are as follows:

AHB Address	bit[31:16]	bit[15:0]	illustrate
0x1FFF_FB38	{9'b0000_0000_0, ~RCHF24M_TRIM}	{9'b1111_1111_1, RCHF24M_TRIM}	RCHF 24Mhz Tuning Value (Software Loading)
0x1FFF_FB3C	{9'b0000_0000_0, ~RCHF16M_TRIM}	{9'b1111_1111_1, RCHF16M_TRIM}	RCHF 16Mhz Tuning Value (Software Loading)
0x1FFF_FB40	{9'b0000_0000_0, ~RCHF8M_TRIM}	{9'b1111_1111_1, RCHF8M_TRIM}	RCHF 8Mhz Tuning Value (automatically loaded after power on) load)

Table **11-4 RCHF** calibration data

The RCHF calibration value is 7 bits. The upper 16 bits and lower 16 bits of the above flash address store the calibration value and the inverse code check word respectively.

If the forward and reverse code verification fails, the calibration value should be discarded.

11.5 Intermediate Frequency **RC Oscillator (RCMF)**

11.5.1 Overview

RCMF is a low-power intermediate frequency loop with a typical frequency of 4MHz and a typical power consumption of only about 20uA. It is used for low-power and low-speed operation of the CPU.

RCMF is tested and calibrated before leaving the factory. Before using the software, the calibration value can be read from the address 0x1FFF_FB44 and written into the RCMFTR register.

By using the memory, a 4M clock with an error less than +/-1% at room temperature can be obtained.

The RCMF calibration parameters in Flash are as follows:

AHB Address	**bit[31:16]**	**bit[15:0]**	illustrate
0x1FFF_FB44	{9'b0000_0000_0, ~RCMF_TRIM}	{9'b1111_1111_1, RCMF_TRIM}	RCMF adjustment value

Table **11-5 RCMF** calibration data

The RCMF calibration value is 7 bits. The upper 16 bits and lower 16 bits of the above flash address store the calibration value and the inverse code check word respectively.

If the forward and reverse code verification fails, the calibration value should be discarded.

11.6 High Precision Low Power **RC Oscillator (LPOSC)**

11.6.1 Overview

LPOSC has extremely low power consumption, only a few hundred nA, and can be used as a backup clock for XTLF or used alone.

It is enabled by default in ACTIVE and LPRUN modes and cannot be disabled.

If the function of automatically switching to the backup clock when XTLF stops is enabled, LPOSC will be turned on when XTLF stops.

When the software turns off XTLF, LFDET will not output a stop signal. If the software also turns off LPOSC at this time, IWDT and RTC
If the software wants to keep LPOSC running in sleep mode, it needs to ensure that LPOSC is enabled before sleep mode.

Power consumption mode	Description	
Active/LPRun	Keep open and cannot be closed	
Sleep/DeepSleep	You can enable or disable the RCC.LPM_LPOSC_OFF register setting. Set to keep LPOSC enabler closed If LPOSC is off, XTLF stops when Register configuration determines whether to automatically start LPOSC and Output 32KHz	
Sleep/DeepSleep wake-up automatically turns on		LPOSC is automatically started when waking up

Table **11-6 LPOSC** control status

LPOSC is tested and calibrated before leaving the factory. Before using the software, the calibration value can be read from the address 0x1FFF_FB20 and written into LPOSCTR
Register to obtain a calibrated low-frequency clock.

The LPOSC calibration parameters in Flash are as follows:

AHB Address	bit[31:16]	bit[15:0]	illustrate
0x1FFF_FB20	{8'b0000_0000, ~LPOSC_TRIM}	{8'b1111_1111, LPOSC_TRIM}	LPOSC calibration value

Table **11-7 LPOSC** calibration data

The LPOSC calibration value is 8 bits. The upper 16 bits and lower 16 bits of the above flash address store the calibration value and the inverse code check word respectively.

If the forward and reverse code verification fails, the calibration value should be discarded.

11.7 Low Frequency Crystal Oscillator Circuit (XTLF)

11.7.1 Overview

The low-frequency crystal oscillator circuit uses an external 32768Hz crystal to provide a stable oscillator source with extremely low power consumption. It is mainly used to power the real-time clock (RTC)

The module provides input clock. The swing degree of XTLF is adjustable, and the user can select the swing degree according to the needs to achieve the best swing capacity and power consumption.

Balance. The feedback resistor of XTLF is integrated inside the chip, and it is necessary to add a load capacitor to the swing pin.

The chip has a stop detection circuit inside to detect whether the XTLF is stopped. Once the XTLF is detected to be stopped, the XTLF

During the stop, notify the CPU to handle it in time.

Software can enable XTLF to be turned off. To improve the performance, a 4-bit XTLFEN bit is used, and the 4-bit reset value is 0101.

Must be written as 1010 to disable XTLF, anything else will keep XTLF enabled.

11.7.2 Working method

After XTLF is powered on, it is turned off by default. When the software is started, it uses medium power by default to shorten the startup time, and the corresponding swing power consumption is also larger.

The typical startup time is less than 1s. After the oscillator is fully started, the software can reduce the oscillator power consumption by configuring the registers.

11.7.3 Vibration stop detection

The FM33LC0XX has an on-chip low-frequency crystal stall detection circuit, see the FDET section for details.

11.8 High-frequency crystal oscillator circuit (XTHF)

11.8.1 Overview

Through an external high-frequency crystal, XTHF can provide a high-precision high-frequency clock source for the MCU. The static and load capacitors should be as close as possible.

The XTHF pin is arranged so that the load capacitor size should be chosen appropriately to suit the selected crystal type.

XTHF can adapt to 4~32MHz crystal. Software can enable or disable XTHF clock through XTHFEN register.

11.8.2 Working method

XTHF is turned off by default after power-on. After power-on reset, the software can turn on XTHF as needed.

Before software enables XTHF, it is necessary to configure the PC2 and PC3 pins as analog functions.

11.8.3 Vibration stop detection

The FM33LC0XX has an on-chip high frequency crystal stall detection circuit, see the FDET section for details.

11.9 Phase-Locked Loop (PLL)

11.9.1 Overview

The reference clock input to the phase-locked loop can be divided by RCHFXTHF, and the maximum output frequency can reach 64MHz and its 2 times.

Before using PLL as the system clock, you need to configure the input reference clock and frequency multiplication system.

11.9.2 Software Application Guide

For reliability reasons, the software needs to pay attention to the following points:

ÿ When selecting PLL input by software, ensure that RCHFXTHF is enabled.

ÿ PLL cannot be turned off when PLL output is selected as SYSCLK

ÿ Software should wait until the PLL is locked before configuring SYSCLK as PLL output

Configure the PLL to output 64MHz and make the system run at 64MHz:

ÿ Configure the PLLCON register to select the input clock source and output clock frequency

ÿ Set Flash wait cycle to 2

ÿ Enable Flash prefetch (optional)

ÿ Select AHB clock as PLL output

11.10 Clock Sources in Low Power Mode

In low power mode, some clock sources are shut down by hardware, while other clock sources can still work.

Below table:

Clock Source	**LPRUN/Sleep/DeepSleep**	illustrate
RCHF	X	Hardware shutdown
PLL	X	
XTHF	X	
USB_BCK	X	
RCMF	THE	Software configuration enable shutdown
LPOSC	THE	
XTLF	THE	

Table **11-8** Clock sources in low power consumption

11.11 Clock Processing for Sleep and Wake-up

When the chip wakes up from Sleep/DeepSleep mode, the hardware automatically turns on RCHF and restores the frequency output before sleep. The SYSCLKSEL register is reset to 00, the system clock is selected as RCHF, and the AHBPRES register is not reset, keeping the sleep state. Therefore, after the chip wakes up, it will use RCHF or its divided clock by default.

11.12 Registers

offset address	name	symbol
RCC (module start address: 0x40000200)		
0x00000000	LOCKUP reset register ÿLockup reset Control Registerÿ Software	RCC_LKPCR
0x00000004	reset register ÿSoftware Reset Registerÿ Reset	RCC_SOFTRST
0x00000008	register ÿReset Flag Registerÿ	RCC_RSTFR
0x0000000C	System clock register ÿSystem Clock Control Registerÿ	RCC_SYSCLKCR
0x00000010	RCHF register ÿRCHF Control Registerÿ	RCC_RCHFCR
0x00000014	RCHF Trim Register ÿRCHF Trim Registerÿ	RCC_RCHFTR
0x00000018	PLL Control Register ÿPLL Control Registerÿ	RCC_PLLCR
0x0000001C	LPOSC Control Register ÿLPOSC Control Registerÿ	RCC_LPOSCCR
0x00000020	LPOSC Tuning Register ÿLPOSC Trim Registerÿ	RCC_LPOSCTR
0x00000024	XTLF control register (XTLF Control Register)	RCC_XTLFCR
0x00000028	Peripheral Line Clock Control Register 1 (Peripheral bus Clock Control Register1) Peripheral	RCC_PCLKCR1
0x0000002C	bus clock control register 2 (Peripheral bus Clock Control Register2) Peripheral	RCC_PCLKCR2
0x00000030	bus clock control register 3 (Peripheral bus Clock Control Register3) Peripheral	RCC_PCLKCR3
0x00000034	bus clock control register 4 ÿPeripheral bus Clock Control Register4ÿ	RCC_PCLKCR4
0x00000038	LSCLK Select Register ÿLSCLK Select Registerÿ	RCC_LSCLKSEL
.	.	.
.	.	.
0x00000044	AHB Master Registers ÿAHB Master Control Registerÿ	RCC_AHBMCR
.	.	.
0x00000050	Peripheral reset enable register ÿPeripheral Reset Enable Registerÿ	RCC_RING
0x00000054	AHB Peripheral Reset Register ÿAHB Peripherals Reset Control Registerÿ	RCC_AHBRSTCR
0x00000058	APB Peripheral Reset Register 1 ÿAPB Peripherals Reset Control Register1ÿ	RCC_APBRSTCR1
0x0000005C	APB Peripheral Reset Register 2 ÿAPB Peripherals Reset Control Register2ÿ	RCC_APBRSTCR2
0x00000060	XTHF control register ÿXTHF Control Registerÿ	RCC_XTHFCR

offset address	name	symbol
RCC (module start address: 0x40000200)		
0x00000064	RCMF control register ÿRCMF Control Registerÿ	RCC_RCMFCR
0x00000068	RCMF Trim Register (RCMF Trim Register)	RCC_RCMFTR
0x0000006C	Peripheral working clock register 1 (Peripheral Operation Clock Control Register1) Peripheral	RCC_OPCCR1
0x00000070	Operation Clock Control Register 2 ÿPeripheral Operation Clock Control Register2ÿ	RCC_OPCCR2
0x00000074	PHY Control Registers ÿPHY Control Registerÿ	RCC_PHYCR
0x00000078	PHY BCK Control Register ÿPHY BCK Control Registerÿ	RCC_PHYBCKCR

11.12.1 LOCKUP reset control register (RCC_LKPCR)

name	RCC_LKPCR						
Offset	0x00000000						
Bit31 Bit name bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
	.						
	U-0						
permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name	.						
bit	U-0						
permission Bit15 Bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
name	.						
bit	U-0						
permission Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	.					LKUPRST_IN	.
Bit permissions	U-0					R/W-0	U-0

Position No.	Mnemonics	Functional Description
31:2	-	RFU: Unimplemented, read as 0
1	**LKUPRST_EN**	LOCKUP Reset Enable 1: Enable SC000 LOCKUP reset 0: Disable SC000 LOCKUP reset
0	-	RFU: Unimplemented, read as 0

11.12.2 Software Reset Register (RCC_SOFTRST)

name	RCC_SOFTRST						
Offset	0x00000004						
Bit31 Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
	SOFTRST[31:24]						
	W-0000 0000						
Permission bit Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16

Bit	SOFTRST[23:16]							
name, bit	W-0000 0000							
permission, bit 15, bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
name,	SOFTRST[15:8]							
bit	W-0000 0000							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	SOFTRST[7:0]							
permission, bit name, bit permission	W-0000 0000							

Position No.	Mnemonics	Functional Description
31:0	**SOFTRST**	Software writes 0x5C5C_AABB to trigger global reset (software reset, write only)

11.12.3 Reset Flag Register (RCC_RSTFR)

name	RCC_RSTFR							
Offset	0x00000008							
bit Bit31 Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
bit								
	U-0							
permission bit Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
Bit								
name	U-0							
bit permission bit Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Position Name			MDFN_FLAG	NRSTN_FLAG	TEXT_FLAG	PORN_FLAG	PDRN_FLAT	
Permission	U-0		R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name			SOFTN_FLAG	IWDTN_FLAG		WWDTN_FLAG	LKUPN_FLAG	NVICN_FLAG
Bit permissions	U-0		R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31:12	-	RFU: Unimplemented, read as 0
12	**MDFN_FLAG**	MDFN reset Flag, write 1 to clear, hardware position, software write 1 to clear
11	**NRSTN_FLAG**	NRST pin reset flag, high, software write 1 to clear (NRST reset Flag, write 1 to clear)
10	**TESTN_FLAG**	TESTN pin reset flag, high, software write 1 to clear (TESTN reset Flag, write 1 to clear)
9	**PORN_FLAG**	Power-up-reset Flag, write 1 to clear
8	**PDRN_FLAG**	Power-down-reset Flag, write 1 to clear
7:6	-	RFU: Unimplemented, read as 0
5	**SOFTN_FLAG**	Software reset flag, high, software write 1 to clear (Software reset flag, write 1 to clear)
4	**IWDTN_FLAG**	IWDT reset flag, high, software write 1 to clear (IWDT reset flag, write 1 to clear)

Position No.	Mnemonics	Functional Description
3	-	RFU: Unimplemented, read as 0
2	**WWDTN_FLAG**	WWDT reset flag, high, software write 1 to clear (WWDT reset flag, write 1 to clear, write 1 to clear)
1	**LKUPN_FLAG**	LOOKUP reset flag, high, software writes 1 to clear (Lockup reset flag, write 1 to clear)
0	**NVICN_FLAG**	NVIC reset flag, high, software writes 1 to clear (NVIC reset flag, write 1 to clear)

11.12.4 System Clock Control Register (RCC_SYSCLKCR)

name	RCC_SYSCLKCR							
Offset	0x0000000C							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Position Name					LSCATS	-	SLP_EN EXIST	-
Bit	U-0				R/W-1	U-0	R/W-1	U-0
permission bit Bit23		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Bit	-		APBPRES2			APBPRES1		
name bit	U-0		R/W-000			R/W-000		
permission bit Bit15		Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit	-					AHBPRES		
name bit	U-0					R/W-000		
permission bit Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	RFU		-		BCKOSEL	SYSCLKSEL		
Bit permissions	R/W-00		U-0		R/W-0	R/W-000		

Position No.	Mnemonics	Functional Description
31:28	-	RFU: Unimplemented, read as 0
27	LSCATS	LSCLK automatic switch Enable 0: When abnormal stop of XTLF is detected, LSCLK will not be automatically switched to LPOSC, the software can switch to LPOSC by writing the LSCLKSEL register 1: When abnormal stop of XTLF is detected, LPOSC is automatically enabled and LSCLK is Switch to LPOSC
26	-	RFU: Unimplemented, read as 0
25	SLP_ENEXTI	Sleep/DeepSleep mode EXTI sampling settings (EXTI under Sleep mode Enable) 1: Enable external pin sampling in Sleep/DeepSleep mode (sampling clock for LSCLK) 0: Disable external pin sampling in Sleep/DeepSleep mode (set the (Exti)
24:22	-	RFU: Unimplemented, read as 0
21:19	APBPRES2	APB2 bus clock prescaler 0xx: No frequency division 100: 2 frequency division 101: 4-way 110: 8 frequency division 111:16 frequency division Note: This register is located in the PD Domain

Position No.	Mnemonics	Functional Description
18:16	APBPRES1	APB1 clock prescaler selection (APB1bus clock Prescaler) 000/001/010/011: No frequency division 100: 2 frequency division 101: 4-way 110: 8 frequency division 111:16 frequency division
15:11	·	RFU: Unimplemented, read as 0
10:8	AHBPRES	AHB bus clock prescaler 000/001/010/011: No frequency division 100: 2 frequency division 101: 4-way 110: 8 frequency division 111:16 frequency division
7:6	RFU	Dummy Registers
5:4	·	RFU: Unimplemented, read as 0
3	BCKOSEL	USB PHY BCK output clock selection signal (USB clock select) 0: Select 48M BCK output as the system clock source 1: Select the 120M BCK output divided by two as the system clock source
2:0	SYSCLKSEL	System clock select 000ýRCHF 001ýXTHF 010ýPLL 011ýRCHF 100ýRCMFPSC 101ýLSCLK 110ýLPOSC 111ýUSBBCK

11.12.5 RCHF Control Register (RCC_RCHFCR)

name	RCC_RCHFCR							
Offset	0x00000010							
Bit31 Bit name bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	·							
	U-0							
permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
name	·			FSEL				
bit	U-0			R/W-0000				
permission Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Bit	·							
name	U-0							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	·							IN
permission	Bit name bit permission			U-0				R/W-1

Position No.	Mnemonics	Functional Description
31:20	·	RFU: Unimplemented, read as 0
19:16	FSEL	RCHF frequency selection register (RCHF 187lock187ncy Select)

Position No.	Mnemonics	Functional Description
		0000ÿ8MHz 0001ÿ16MHz 0010ÿ24MHz Others: RFU
15:1		RFU: Unimplemented, read as 0
0	IN	RCHF Enable Register (RCHF Enable) 1: Enable RCHF 0: Disable RCHF

11.12.6 RCHF Calibration Register (RCC_RCHFTR)

name	RCC_RCHFTR							
offest	0x00000014							
bit 31 bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	U-0							
permission bit 23 bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
name								
	U-0							
permission bit 15 bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
name								
	U-0							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		TRIM						
permission bit name permission U-0	R/W-100 0000							

Position No.	Mnemonics	Functional Description
31:7		RFU: Unimplemented, read as 0
6:0	TRIM	RCHF frequency adjustment register, 7'h00 indicates the lowest frequency, 7'h7F indicates the highest frequency Highest, the adjustment range is mid-frequency +/-30%, the adjustment step is mid-frequency 0.5% After power-on, the chip automatically reads the 8MHz calibration value from NVR1 and writes it into this register. When the software uses other frequencies, it can read the calibration information from the NVR1 address. and write to this register to ensure the output frequency is accurate. (RCHF Trim)

11.12.7 PLL Control Register (RCC_PLLCR)

name	RCC_PLLCR							
Offset	0x00000018							
Bit31 Bit Name Bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	U-0							
Permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
Name	DB							
Bit Permission U-0	R/W-010 1111							
Bit15 Bit Name	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	

Bit	U-0							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Permissions Bit Name	REFPRSC				OSEL	·	ISLAND	IN
LOCKED Bit Permissions	R-0	R/W-000			R/W-0	U-0	R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31:23	·	RFU: Unimplemented, read as 0
22:16	DB	PLL Divide Boost 0011111: Output 32 times 0101111: Output 48 times
15:8	·	RFU: Unimplemented, read as 0
7	LOCKED	PLL lock flag. The software can query this register to confirm that the PLL is locked. Condition (PLL is Locked) 1: PLL is locked 0: PLL is not locked
6:4	REFPRSC	PLL reference clock pre-scaling (the goal is to generate a 1MHz reference clock for the PLL) (PLL reference clock prescaler) 000: No frequency division 001: 2-way 010: 4-way 011: 8-way 100: 12 frequency division 101:16 frequency division 110:24 frequency division 111:32 frequency division
3	OSEL	PLL output select register 0: Select PLL double output as PLL clock in word circuit 1: Select PLL double output as PLL clock in word circuit
2	·	RFU: Unimplemented, read as 0
1	ISLAND	PLL input select register (PLL reference input select) 0ÿRCHF 1ÿXTHF
0	IN	PLL enable register (PLL enable) 1: Enable PLL 0: Disable PLL

11.12.8 LPOSC Control Register (RCC_LPOSCCR)

name	**RCC_LPOSCCR**							
Offset	0x0000001C							
Bit31 Bit Name Bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	·							
	U-0							
Permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
Name	·							
Bit	U-0							
Permission Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Bit Name	·							

Permission	U-0							
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name						LPO_CHOPEN	LPO_ENB	LPM_LPO_OFF
Bit permissions	U-0					R/W-0	R-0	R/W-0

Position No.	Mnemonics	Functional Description
31:3		RFU: Unimplemented, read as 0
2	LPO_CHOP_EN	LPOSC Chopper enable register (LPOSC chopper enable)
1	LPO_ENB	LPOSC enable signal, read-only, for software to query LPOSC enable status (LPOSC Enable Bar,read only) 0: LPOSC is in the open state 1: LPOSC is in the off state
0	LPM_LPO_OFF	LPOSC Off in Sleep Mode LowPowerMode Enable) 1: LPOSC is turned off in sleep mode 0: LPOSC is on in sleep mode ÿNote 1ÿ This register is only available in the chip sleep mode. LPOSC is kept enabled in Sleep/Deepsleep mode ÿNote 2ÿWhen XTLF stops abnormally, the root LSCATS register configuration determines whether Automatically enable LPOSC

11.12.9 LPOSC Calibration Register (RCC_LPOSCTR)

name	**RCC_LPOSCTR**							
Offset	0x00000020							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit								
	U-0							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name								
bit	U-0							
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit								
name	U-0							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	LPOTRIM							
permission	Bit name bit permission	R/W-1000 1101						

Position No.	Mnemonics	Functional Description
31:8		RFU: Unimplemented, read as 0
7:0	LPOTRIM	LPOSC trimming register 0000 0000: lowest frequency 1111 1111: highest frequency

11.12.10 XTLF Control Register (RCC_XTLFCR)

name	RCC_XTLFCR
Offset	0x00000024

Bit31 Bit name bit		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
	U-0							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name								
bit	U-0							
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit					IN			
name	U-0				R/W-xxxx			
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						IPW		
permission	Bit name bit permission	U-0				R/W-000		

Position No.	Mnemonics	Functional Description
31:12		RFU: Unimplemented, read as 0
11:8	IN	XTLF enable register, XTLF is disabled by default on power-on (Enable) 1010: Disable XTLF and FDET 0101: Enable XTLF and FDET Others: RFU When XTLF is working, the software must write 1010 to turn it off. When not working, the software must be written to 0101 to start
7:3		RFU: Unimplemented, read as 0
2:0	IPW	XTLF working current selection, the larger the current, the higher the swing. Use 000 gear and above, 100 011 gear is recommended for normal operation. The measured negative resistance of the adaptor crystal is used to select the appropriate current size (XTLF current select) 000: 450 nA 001: 400 nA 010: 350 nA 011: 300 nA 100: 250 nA 101: 200 nA 110: 150 nA 111: 100 nA

11.12.11 Peripheral Bus Clock Control Register **1 (RCC_PCLKCR1)**

name	RCC_PCLKCR1							
Offset	0x00000028							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Position Name	DCU_PC AND							
Bit Permission	R/W-1	U-0						
Bit 23 Bit Name Bit		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
	U-0							
Permission	Bit 15 Bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Name								

Permission	U-0							
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	PAD_PC AND	ANAC_P THIS	IWDT_P THIS	SCU_PC AND	PMU_PC AND	RTC_PC AND	USB_PC AND	LPT_PCE
Bit Permission R/W-0		R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31	DCU_PCE	DCU line clock enable, high enable (Debug Control Unit APB bus clock enable)
30:8		RFU: Unimplemented, read as 0
7	PAD_PCE	PADCFG line clock enable, high enable (GPIO controller APB bus clock enable)
6	ANAC_PCE	ANAC line clock enable, high enable (Analog controller APB bus clock enable)
5	IWDT_PCE	IWDT line clock enable, high enable (IWDT APB bus clock enable)
4	SCU_PCE	SCU line clock enable, high enable (System controller APB bus clock enable)
3	PMU_PCE	PMU line clock enable, high enable (PMU APB bus clock enable)
2	RTC_PCE	RTC line clock enable, high enable (RTC APB bus clock enable)
1	USB_PCE	USB line clock enable, high enable (USB device APB bus clock enable)
0	LPT_PCE	LPTIM32 line clock enable, high enable (LPTIM APB bus clock enable)

11.12.12 Peripheral Bus Clock Control Register **2 (RCC_PCLKCR2)**

name	RCC_PCLKCR2							
Offset	0x0000002C							
Bit31 Bit name bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	U-0							
permission bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
name								
bit	U-0							
permission bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Position Name						HDIV_P THIS	ADC_PC AND	
Permission	U-0					R/W-0	R/W-0	
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	WWDT_P THIS	RAMBIST _PCE	FLASH_P THIS	DMA_PC AND	LCD_PC AND	AES_PC AND	TRNG_P THIS	CRC_PC AND
Bit Permission R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31:10		RFU: Unimplemented, read as 0
9	HDIV_PCE	Hardware Divider APB bus clock enable, high enable
8	ADC_PCE	ADC line clock enable, high enable (ADC controller APB bus clock enable)
7	WWDT_PCE WWDT line clock enable, high enable (WWDT APB bus clock enable)	
6	RAMBIST_PCE RAMBIST line clock enable, high enable (RAMBIST APB bus clock	

Position No.	Mnemonics	Functional Description
		enable)
5	FLASH_PCE	Flash writer line clock enable, high enable (Flash interface APB bus clock enable)
4	DMA_PCE	DMA line clock enable, high enable (DMA APB bus clock enable)
3	LCD_PCE	LCD line clock enable, high enable (LCD APB bus clock enable)
2	AES_PCE	AES line clock enable, high enable (AES APB bus clock enable)
	RNG_PCE	RNG line clock enable, high enable (RNG APB bus clock enable)
1 0	CRC_PCE	CRC line clock enable, high enable (CRC APB bus clock enable)

11.12.13 Peripheral Bus Clock Control Register **3 (RCC_PCLKCR3)**

name	RCC_PCLKCR3							
Offset	0x00000030							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Position Name								I2C_PC AND
	U-0							R/W-0
Permission bit Bit 23		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Position Name						LPUART 1_PCE		U7816_ PCE
	U-0					R/W-0	U-0	R/W-0
Permission bit Bit15		Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Position Name	LPUART 0_PCE	UCIR_P THIS	UART5_ PCE	UART4_ PCE			UART1_ PCE	UART0_ PCE
Bit Permission R/W-0		R/W-0	R/W-0	R/W-0	U-0		R/W-0	R/W-0
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name							SPI2_PC AND	SPI1_PC AND
Bit permissions	U-0						R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31:25		RFU: Unimplemented, read as 0
24	I2C_PCE	I2C line clock enable, high (I2C APB bus clock enable)
23:19		RFU: Unimplemented, read as 0
18	LPUART1_PCE	LPUART1 line clock enable, high (LPUART1 APB bus clock enable)
17		RFU: Unimplemented, read as 0
16	U7816_PCE	7816 line clock enable, high (U7816 APB bus clock enable)
15	LPUART0_PCE	LPUART line clock enable, high is (LPUART0 APB bus clock enable)
14	UCIR_PCE	UART infrared modulation working clock enable, high is (UART infra-red APB bus clock enable)
13	UART5_PCE	UART5 line clock enable, high is (UART5 APB bus clock enable)
12	UART4_PCE	UART4 line clock enable, high (UART4 APB bus clock enable)
11:10		RFU: Unimplemented, read as 0
9	UART1_PCE	UART1 line clock enable, high (UART1 APB bus clock enable)
8	UART0_PCE	UART0 line clock enable, high (UART0 APB bus clock enable)
7:2		RFU: Unimplemented, read as 0
1	SPI2_PCE	SPI2 line clock enable, high (SPI2 APB bus clock enable)

Position No.	Mnemonics	Functional Description
0	SPI1_PCE	SPI1 line clock enable, high (SPI1 APB bus clock enable)

11.12.14 Peripheral Bus Clock Control Register **4 (RCC_PCLKCR4)**

name	RCC_PCLKCR4						
Offset	0x00000034						
bit Bit31 Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit							
	U-0						
permission bit Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name							
bit	U-0						
permission bit Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit							
name bit	U-0						
permission bit Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name			AT_PCE	GT1_PC AND	GT0_PC AND		BT_PCE
Bit permissions	U-0		R/W-0	R/W-0	R/W-0	U-0	R/W-0

Position No.	Mnemonics	Functional Description
31:5 4		RFU: Unimplemented, read as 0
	AT_PCE	Advanced timer line clock enable, high (ATIM APB bus clock enable)
3	GT1_PCE	General timer 1 line clock enable, high (GPTIM1 APB bus clock enable)
2	GT0_PCE	General timer 0 line clock enable, high (GPTIM0 APB bus clock enable)
1		RFU: Unimplemented, read as 0
0	BT_PCE	Basic timer 0 line clock enable, high (BSTIM APB bus clock enable)

11.12.15 LSCLK Selection Register (RCC_LSCLKSEL)

name	**RCC_LSCLKSEL**						
Offset	0x00000038						
bit Bit31 Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit							
	U-0						
permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name							
bit	U-0						
permission Bit15 Bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
name							
bit	U-0						
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	CELL						
permission Bit name bit permission	R/W-0000 0001						

Position No.	Mnemonics	Functional Description
31:8		RFU: Unimplemented, read as 0
7:0	CELL	When LSCLK is XTLF, software writes 0x55 to this address, which will set the LSCLK source Head cut to LPOSC When LSCLK is LPOSC, software writes 0xAA to this address, which will Source switched to XTLF Write any other value, and the previous LSCLK will not change; this register is only used when LSCATS is 0 hours

11.12.16 AHB Master Control Register (RCC_AHBMCR)

name	RCC_AHBMCR							
Offset	0x00000044							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit								
	U-0							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name								
bit	U-0							
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit								
name	U-0							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								MPRIL
permission	Bit name bit permission			U-0				R/W-0

Position No.	Mnemonics	Functional Description
31:1		RFU: Unimplemented, read as 0
0	MPRIL	AHB Master Priority Configuration Register (Priority Config) 0: DMA priority 1: CPU priority

11.12.17 Peripheral Reset Enable Register (RCC_PRSTEN)

name	RCC_RING							
Offset	0x00000050							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit	PERHRSTEN[31:24]							
	W-0000 0000							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name	PERHRSTEN[23:16]							
bit	W-0000 0000							
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit	PERHRSTEN[15:8]							
name	W-0000 0000							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	PERHRSTEN[7:0]							
permission	Bit name bit permission			W-0000 0000				

Position No.	Mnemonics	Functional Description
31:0	PERHRSTEN	Peripheral module reset enable, 32-bit virtual register, write only (Peripheral Reset Enable,write only) The software writes 0x1357_9BDF to this address to enable the peripheral reset function. Reset each module through the peripheral module reset register If the software writes anything else to this address, the peripheral reset function will be disabled.

11.12.18 AHB Peripheral Reset Register (RCC_AHBRSTCR)

name	RCC_AHBRSTCR							
Offset	0x00000054							
Bit31 Bit name bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
	U-0							
permission Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
name								
bit	U-0							
permission Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Bit								
name	U-0							
bit permission Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Position Name						USBRST	DMARST	
Bit permissions	U-0					R/W-0	R/W-0	

Position No.	Mnemonics	Functional Description
31:2		RFU: Unimplemented, read as 0
1	USBRST	USB module reset, software write 1 to reset, write 0 to reset (USB reset Enable) 0: Do not reset 1: Reset
0	DMARST	DMA module reset, software writes 1 to reset, writes 0 to reset (DMA reset Enable) 0: Do not reset 1: Reset

11.12.19 APB Peripheral Reset Register 1 (RCC_APBRSTCR1)

name	RCC_APBRSTCR1							
Offset	0x00000058							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Position Name	UART5RST	UART4RST					GPT1RST	GPT0RST
Bit Permission R/W-0	R/W-0	U-0					R/W-0	R/W-0
Bit 23 Bit Name Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
								LCDRST
	U-0							R/W-0
Permission Bit 15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	

Position Name	·	U7816RST	·	SPI2RST	·
Bit permission U-0 bit		R/W-0	U-0	R/W-0	U-0

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	·	LPUART0RST	·		I2C1RST	·		LPT32RST
Bit Permission U-0		R/W-0	U-0		R/W-0	U-0		R/W-0

Position No.	Mnemonics	Functional Description
31	UART5RST	UART5 module reset, software write 1 to reset, write 0 to reset (UART5 reset Enable) 0: Do not reset 1: Reset
30	UART4RST	UART4 module reset, software write 1 to reset, write 0 to reset (UART4 reset Enable) 0: Do not reset 1: Reset
29:26	·	RFU: Unimplemented, read as 0
25	GPT1RST	GPTIM1 module reset, software write 1 reset, write 0 pin reset (GPTIM1 reset Enable) 0: Do not reset 1: Reset
24	GPT0RST	GPTIM0 module reset, software write 1 to reset, write 0 to reset (GPTIM0 reset Enable) 0: Do not reset 1: Reset
23:17	·	RFU: Unimplemented, read as 0
16	LCDRST	LCD module reset, software write 1 reset, write 0 pin reset (LCD reset Enable) 0: Do not reset 1: Reset
15	·	RFU: Unimplemented, read as 0
14	U7816RST	U7816 module reset, software write 1 reset, write 0 pin reset (U7816 reset Enable) 0: Do not reset 1: Reset
13:11	·	RFU: Unimplemented, read as 0
10	SPI2RST	SPI2 module reset, software writes 1 to reset, writes 0 to reset (SPI2 reset) 0: Do not reset 1: Reset
9:7	·	RFU: Unimplemented, read as 0
6	LPUART0RST	EUART0 module reset, software writes 1 to reset, writes 0 to reset the pin (LPUART0 reset Enable) 0: Do not reset 1: Reset
5:4	·	RFU: Unimplemented, read as 0
3	I2C1RST	I2C1 module reset, software write 1 reset, write 0 pin reset (I2C1 reset Enable) 0: Do not reset 1: Reset
2:1	·	RFU: Unimplemented, read as 0
0	LPT32RST	LPTIM32 module reset, software write 1 to reset, write 0 to reset (LPTIM

Position No.	Mnemonics	Functional Description
		resetEnable) 0: Do not reset 1: Reset

11.12.20 **APB** Peripheral Reset Register **2 (RCC_APBRSTCR2)**

name	RCC_APBRSTCR2							
Offset	0x0000005C							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Bit Name	ATRST			BT32RST				ADCCRST
Bit permission	R/W-0	U-0		R/W-0	U-0			R/W-0
Bit 23		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Bit Name	ADCRST	OPARST			HDVRST	AESRST	CRCRST	RNGRST
Bit permission	R/W-0	R/W-0	U-0		R/W-0	R/W-0	R/W-0	R/W-0
Bit 15		Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Position Name				UART1RST	UART0RST		SPI1RST	UCIRRST
Permission	U-0			R/W-0	R/W-0	U-0	R/W-0	R/W-0
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	LPUART1RST							
bit permission	R/W-0	U-0						

Position No.	Mnemonics	Functional Description
31	FIND	ATIM module reset, software writes 1 to reset, writes 0 to reset (ATIM reset Enable) 0: Do not reset 1: Reset
30:29		RFU: Unimplemented, read as 0
28	BTRST	BSTIM32 module reset, software writes 1 to reset, writes 0 to reset (BSTIM32 reset Enable) 0: Do not reset 1: Reset
27:25		RFU: Unimplemented, read as 0
24	ADCCRST	ADC controller reset, software writes 1 to reset, writes 0 to reset (ADC controller reset Enable) 0: Do not reset 1: Reset
23	ADCRST	ADC module reset, software write 1 to reset, write 0 to reset (ADC reset Enable) 0: Do not reset 1: Reset
22	OPARST	Operation module reset, software writes 1 to reset, writes 0 to reset (OPA reset Enable) 0: Do not reset 1: Reset
21:20		RFU: Unimplemented, read as 0
19	HDVRST	Hardware divider reset, software write 1 reset, write 0 pin reset (Hardware Divider Reset Enable)

Position No.	Mnemonics	Functional Description
		0: Do not reset 1: Reset
18	AESRST	AES module reset, software write 1 to reset, write 0 to reset (AES reset Enable) 0: Do not reset 1: Reset
17	CRCRST	CRC module reset, software writes 1 to reset, writes 0 to reset (CRC reset Enable) 0: Do not reset 1: Reset
16	RNGRST	RNG module reset, software write 1 to reset, write 0 to reset (RNG reset Enable) 0: Do not reset 1: Reset
15:13	·	RFU: Unimplemented, read as 0
12	UART1RST	UART1 module reset, software write 1 reset, write 0 pin reset (UART1 reset Enable) 0: Do not reset 1: Reset
11	UART0RST	UART0 module reset, software write 1 to reset, write 0 to reset (UART0 reset Enable) 0: Do not reset 1: Reset
10	·	RFU: Unimplemented, read as 0
9	SPI1RST	SPI1 module reset, software writes 1 to reset, writes 0 to reset (SPI1reset Enable) 0: Do not reset 1: Reset
8	UCIRRST	Infrared modulation module reset, software write 1 reset, write 0 pin reset (UCIR reset Enable) 0: Do not reset 1: Reset
7	LPUART1RST	LPUART1 module reset, software writes 1 to reset, writes 0 to reset the pin (LPUART1 reset Enable) 0: Do not reset 1: Reset
6:0	·	RFU: Unimplemented, read as 0

11.12.21 XTHF Control Register (RCC_XTHFCR)

name	RCC_XTHFCR							
Offset	0x00000060							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit	·							
	U-0							
permission	bit Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Bit	·							
name	U-0							
bit permission	bit Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

Bit name						CFG		
Bit permission	U-0					R/W-000		
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
name								IN
Bit permission	U-0							R/W-0

Position No.	Mnemonics	Functional Description
31:11		RFU: Unimplemented, read as 0
10:8	CFG	XTHF oscillation strength config 000: Most 111: Most
7:1		RFU: Unimplemented, read as 0
0	IN	XTHF enable register (XTHF enable) 0: Disable XTHF 1: Enable XTHF

11.12.22 RCMF Control Register (RCC_RCMFCR)

name	RCC_RCMFCR							
Offset	0x00000064							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit								
	U-0							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name							PSC	
bit	U-0						R/W-00	
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit								
name	U-0							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								IN
permission	Bit name bit permission			U-0				R/W-0

Position No.	Mnemonics	Functional Description
31:18		RFU: Unimplemented, read as 0
17:16	PSC	RCMF output prescaler 00: No frequency division 01: 4-way 10:8 frequency division 11:16 frequency division
15:1		RFU: Unimplemented, read as 0
0	IN	RCMF Enable Register (RCMFEnable) 0: Disable RCMF 1: Open RCMF

11.12.23 RCMF Calibration Register (RCC_RCMFTR)

name	**RCC_RCMFTR**

Offset	0x00000068							
bit Bit31	Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit	·							
	U-0							
permission	Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name	·							
bit	U-0							
permission	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit	·							
name	U-0							
bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	·	TRIM						
permission	Bit name bit permission U-0	R/W-100 0000						

Position No.	Mnemonics	Functional Description
31:7	·	RFU: Unimplemented, read as 0
6:0	TRIM	RCMF frequency adjustment register, 7'h00 indicates the lowest frequency, 7'h7F indicates the highest frequency Highest, the adjustment range is mid-frequency +/-30%, and the adjustment step is mid-frequency 1% (RCMF trimming)

11.12.24 Peripheral Operation Clock Control Register **1 (RCC_OPCCR1)**

name	RCC_OPCCR1							
Offset	0x0000006C							
Bit31		Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Position Name	EXTICK AND	EXTICK S	LPUART 1CKE	LPUART 0CKE	LPUART1CKS		LPUART0CKS	
Bit Permission R/W-0		R/W-0	R/W-0	R/W-0	R/W-00		R/W-00	
Bit 23 Bit Name Bit		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
	·			I2CCKE	·		I2CCKS	
	U-0			R/W-0	U-0		R/W-00	
Permission Bit 15		Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NameATCKE		·					UART1C KE	UART0C KE
Bit Permission R/W-0		U-0					R/W-0	R/W-0
Bit	Bit7 Bit	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
name	ATCKS		·		UART1CKS		UART0CKS	
Bit permission	R/W-00		U-0		R/W-00		R/W-00	

Position No.	Mnemonics	Functional Description
31	EXTICKE	EXTI operation clock enable, high (External interrupt operation clock Enable)
30	EXTICKS	EXTI sampling clock selection (External interrupt sampling clock select) 1: Use LSCLK sampling in external pin 0: Use HCLK sampling in external pin *It is recommended to set it with EXTI turned off, and then enable it after setting it EXIT
29	LPUART1CKE LPUART1 operation clock enable, high is	

Position No.	Mnemonics	Functional Description
		enable)
28	LPUART0CKE	LPUART0 operation clock enable, high is (LPUART0 operation clock enable)
27:26	LPUART1CKS	LPUART1 operation clock select 00ÿLSCLK 01: RCHF frequency division 10: RCMF frequency division 11ÿRFU
25:24	LPUART0CKS	LPUART0 operation clock select 00ÿLSCLK 01: RCHF frequency division 10: RCMF frequency division 11ÿRFU
23:21	·	RFU: Unimplemented, read as 0
20	I2CCKE	I2C working clock enable
19:18	·	RFU: Unimplemented, read as 0
17:16	I2CCKS	I2C host operation clock select (I2C operation clock select) 00ÿAPBCLK 01ÿRCHF 10ÿSYSCLK 11ÿRCMF_PSC
15	ATCKE	ATIM operation clock enable register, high is (ATIM operation clock Enable)
14:10	·	RFU: Unimplemented, read as 0
9	UART1CKE	UART1 operation clock enable, high is (UART1 operation clock enable)
8	UART0CKE	UART0 operation clock enable, high is (UART0 operation clock enable)
7:6	ATCKS	ATIM operation clock select register 00ÿAPBCLK2 01ÿUSB PHY BCK 120M 10ÿAPBCLK2 11: PLL double frequency
5:4	·	RFU: Unimplemented, read as 0
3:2	UART1CKS	UART1 operation clock select 00ÿAPBCLK 01ÿRCHF 10ÿSYSCLK 11ÿRCMF_PSC
1:0	UART0CKS	UART0 operation clock select 00ÿAPBCLK 01ÿRCHF 10ÿSYSCLK 11ÿRCMF_PSC

11.12.25 Peripheral Operation Clock Control Register **2 (RCC_OPCCR2)**

name	RCC_OPCCR2						
Offset	0x00000070						
Bit31 Bit Name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
·	RNGPRSC			·	ADCPRSC		

Bit permission U-0 Bit		R/W-000			U-0	R/W-000		
23		Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Position Name	USBREFCKE	FLASHCKE	RNGCKAND	ADCCKAND	USBREFCKS		ADCCKS	
Bit Permission R/W-0		R/W-0	R/W-0	R/W-0	R/W-00		R/W-00	
Bit15 Bit Name Bit		Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	·			LPTCKE	·		LPTCKS	
	U-0			R/W-0	U-0		R/W-00	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	·			BTCKE	·		BTCKS	
Permission Bit Name Bit Permission	U-0			R/W-0	U-0		R/W-00	

Position No.	Mnemonics	Functional Description
31	·	RFU: Unimplemented, read as 0
30:28	RNGPRSC	RNG operation clock prescaler 000: No frequency division 001: 2-way 010: 4-way 011: 8-way 100:16 frequency division 101:32 frequency division 110, 111ÿRFU
27	·	RFU: Unimplemented, read as 0
26:24	ADCPRSC	ADC operation clock prescaler 000: No frequency division 001: 2-way 010: 4-way 011: 8-way 100:16 frequency division 101:32 frequency division 110/111ÿRFU
23	USBREFCKE	USB reference clock enable 0: Disable USB reference clock output 1: Enable USB reference clock output
22	FLASHCKE	Flash write clock enable, high (Flash erase/program clock enable)
21	RNGCKE	Random generator working clock enable, high (RNG operation clock enable)
20	ADCCKE	ADC operation clock enable, high (ADC operation clock enable)
19:18	USBREFCKS	USB reference clock select 00/11ÿXTLFÿ32768Hzÿ 01ÿXTHFÿ12MHzÿ 10: RCHF frequency division
17:16	ADCCKS	ADC operation clock select 00ÿRCMF_PSC 01ÿRCHF 10ÿXTHF 11ÿPLL
15:13	·	RFU: Unimplemented, read as 0
12	LPTCKE	LPTIM operation clock enable, high is (LPTIM operation clock enable)

Position No.	Mnemonics	Functional Description
11:10	-	RFU: Unimplemented, read as 0
9:8	LPTCKS	LPTIM operation clock select 00ÿAPBCLK1 01ÿLSCLK 10ÿLPOSC 11ÿRCMF_PSC
7:5	-	RFU: Unimplemented, read as 0
4	BTCKE	BSTIM operation clock enable, high is (BSTIM operation clock enable)
3:2	-	RFU: Unimplemented, read as 0
1:0	BTCKS	BSTIM operation clock select 00ÿAPBCLK2 01ÿLSCLK 10ÿLPOSC 11ÿRCMF_PSC

11.12.26 PHY Control Register (RCC_PHYCR)

name	RCC_PHYCR							
offset	0x00000074							
bit Bit31 bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
bit	-							
	U-0							
permission bit Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
bit	-							
name	U-0							
bit permission bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Bit15	-							
bit name	U-0							
bit permission bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	-			PHY_PO NRST_B	PD	PLVREA DY_33V	BCKPD	NONCR Y_RSTB
Bit permissions	U-0			R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

Position No.	Mnemonics	Functional Description
31:5	-	RFU: Unimplemented, read as 0
4	**PHY_PONRST_B**	USB PHY reset, low is true; the default is 0 when powered on, and the software writes 1 to reset the pin (PHY Power-On_Reset Bar Enable) 0: Reset USB PHY 1: Pin resets USB PHY Note: When the system clock comes from **PHY ,** this register cannot be written as 0; In the *FM33LC0xx* series, before using the clock for communication, you must first set this *USB BCK* register to reset the pin. *USB PHY*
3	**PD**	PHY transceiver power down ÿÿÿ (PHY Power Down Enable) 1: PHY transmitter is in machine mode 0: PHY transmitter is in working mode

Position No.	Mnemonics	Functional Description
2	**PLVREADY_33V**	VDD15D power supply establishment mark, before using USB PHY, the software needs to set this Register Set (Power Low Voltage Ready Enable) 1: VDD15D power supply has been established 0: VDD15D power supply is not established
1	**BCKPD**	BCK module of PHY is enabled (Built-in-Clock Power Down Enable) 1: BCK is disabled and no clock is output 0: BCK enabled, output clock Note: When the system clock comes from **PHY ,** this register cannot be written as 1.
0	**NONCRY_RSTB**	Reset signal of BCK module (Non-Crystal Reset Bar Enable) 1: BCK reset release 0: BCK reset is enabled Note: When the system clock comes from **PHY ,** this register cannot be written as 0;

11.12.27 PHY BCK Control Register (RCC_PHYBCKCR)

name	**RCC_PHYBCKCR**							
Offset	0x00000078							
bit Bit31 Bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	
bit								
	U-0							
permission bit Bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
name								
bit	U-0							
permission bit Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Position Name							CK48M_ IN	
Permission	U-0						R/W-0	
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name	CLK_RD Y							OUTCLK CELL
bit permission R	U-0							R/W-0

Position No.	Mnemonics	Functional Description
31:9	-	RFU: Unimplemented, read as 0
8	**CK48M_EN**	48M clock output enable (Clock 48Mhz Enable) 1: Allow PHY to output 48M clock, must be set before USB communication 0: Disable PHY output 48M clock
7	**CLK_RDY**	Clock Ready Flag (read only) 1: Indicates that the clock tracking is completed 0: Clock tracking is not yet complete Note: *OUTCLKSEL=1* In this case, this register is kept as *0*
6:1	-	RFU: Unimplemented, read as 0
0	**OUTCLKSEL**	Output Clock Select 1: Use CORECLKIN reference clock as clock tracking source 0: Use the SOF sent by USB line for clock tracking