

# 6 CPU

## 6.1 Overview

The CPU core used by FM33LC0XX is Cortex-M0, which complies with the ARMv6-M architecture and programming model; for more information, please refer to ARM official website [www.arm.com](http://www.arm.com)

Its basic characteristics are as follows:

- User/Privileged Mode
- VTOR (Interrupt Vector Table Redirection)
- NVIC supports 32 external interrupts
- Data monitoring points: 1
- Hardware breakpoints: 4
- Single-cycle 32-bit hardware multiplier
- SWD debug interface

### 6.1.1 Processor Configuration

Feature	Options	FM33LC0XX Config
Interrupts	1~32	32
Data endianness	little/big	little
SysTick Timer	Present or absent	Present
watchpoints	0,1,2	1
breakpoints	0,1,2,3,4	4
halting debug support multiplier	Present or absent	Present
	Fast or Small	Fast
Single-Cycle IO wake-up interrupt controller(WIC)	Present or absent	Absent
	Present or absent	Present
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
JTAGnSW	JTAG or SWD for DAP	SWD
Memory Protection Unit	Present or absent	Absent

Table 6-1FM33LC0xx CPU configuration table

## 6.2 Registers

List of main core registers

name	describe
R0-R12	General registers
MSP (R13)	Stack pointer; MSP (Main Stack Pointer) is used in Handler mode, Thread Mode through the CONTROL register to select MSP or PSP (Process Stack Pointer)
PSP (R13)	
LR (R14)	Link register, saves the return information of sub-function/function call/exception handling
PC (R15)	Program Pointer
PSR	Contains application program status (APSR), interrupt program status (IPSR), and program execution Status (EPSR)
PRIMASK	PRIMASK is used to mask all interrupt responses of the specified priority level and below
CONTROL	Set the stack pointer used in Thread mode

Table 6-2 Cortex-M0 core register summary

For detailed register definitions, see the ARMv6-M Architecture Reference Manual.

6.3 Exceptions and Interrupts

The kernel's exception and interrupt management is done through the NVIC. The NVIC's programmable management registers are located in the SCS space of the PPB bus.

The NVIC has the following features:

- Support 32 external interrupts and 5 internal exceptions
- 1 NMI interrupt
- Support interrupt nesting
- Vectorized exception entry
- Interrupt mask

After the processor core accepts an exception request, it first pushes the core registers R0–R3, R12, R14, PC, and xPSR into the stack.

The link register LR (R14) is updated with a special value (EXC\_RETURN) used when an exception is returned, and then the exception vector is

The table locates the exception handler and starts executing. Note that the registers that are not automatically pushed onto the stack during exception handling must be saved by software. and recovery.

6.3.1 Interrupt Vector Table

Position	Priority	Priority type	Acronym	Description	Address
0	-	-	MSP initial value	main stack pointer initialization address	0x0000_0000
1	-3	fixed	Reset	Reset vector	0x0000_0004
2	-2	fixed	NMI	WKUPx Interrupt Low power mode error interrupt	0x0000_0008
3	-1	fixed	HardFault	HardFault interrupt vector	0x0000_000C
4-10	-	-	-	Reserved	0x0000_0010–0x0000_002B
11	3	settable	SVC	SVC system service request	0x0000_002C
12-13	-	-	-	Reserved	0x0000_0030–0x0000_0037
14	5	Settable	PendSV	PendSV can suspend system service request	0x0000_0038
15	6	settable	Systick	Systick internal timer interrupt vector	0x0000_003C
16	7	settable	WWDG	WWDG window watchdog interrupt	0x0000_0040
17	8	settable	SVD	SVD power monitoring alarm interrupt	0x0000_0044
18	9	settable	RTC	RTC real-time clock interrupt	0x0000_0048
19	10	settable	FLASH	FLASH NVMIIF interrupt	0x0000_004C
20	11	settable	LFDET	XTLF or XTHF vibration stop detection Interrupt	0x0000_0050
21	12	settable	ADC	ADC conversion completed interrupt	0x0000_0054
22	13	settable	IWDT	IWDT interrupt	0x0000_0058
23	14	SPI1	-	SPI Interrupt	0x0000_005C
24	15	settable	SPI2	-	0x0000_0060
25	16	settable	LCD	LCD display module interrupt	0x0000_0064

Position	Priority	Priority type	Acronym	Description	Address
26	17	settable UART0		UART Interrupts	0x0000_0068
27	18	settable UART1	settable		0x0000_006C
28	19	UART4			0x0000_0070
29	20	settable UART5	0x0000_0074		
30	21	settable HFDET	High frequency crystal stop detection interrupt	0x0000_0078	
31	22	settable U7816		U7816 Interrupt	0x0000_007C
32	23	settable LPUART1	LPUART1 interrupt	0x0000_0080	
33	24	settable I2C		I2C Interrupt	0x0000_0084
34	25	settable USB	0x0000_0088	USB device yy	
35	26	interrupt settable AES	0x0000_008C		
36	27	settable LPTIM	low power timer interrupt	0x0000_0090	
37	28	interrupt settable DMA	0x0000_0094		
38	29	settable WKUP	WKUP pin interrupt	0x0000_0098	
39	30	interrupt settable OPAX	0x0000_009C		
40	31	settable BSTIM	basic timer interrupt	0x0000_00A0	
41	32	settable COMPx	COMPx interrupt	0x0000_00A4	
42	33	settable GPTIM0	general timer 1 interrupt	0x0000_00A8	
43	34	settable GPTIM1	general timer 2 interrupt	0x0000_00AC	
44	35	settable ATIM	Advanced Timer Interrupt	0x0000_00B0	
45	36	settable VREF		1.2V internal reference voltage is being established Break	0x0000_00B4
46	37	settable GPIO	external pin interrupt	settable LPUART0	0x0000_00B8
47	38	LPUART0 interrupt			0x0000_00BC

Table 6-3FM33LC0xx interrupt vector table

The WKUP interrupt can be connected to NMI or 38# entry. The interrupt entry address is selected through the WKSEL register of the PMU module.

When configured as entry 38#, the WKUPx interrupt can be masked through PRIMASK, and the CPU does not enter the interrupt service routine after wake-up.

Instead, execution continues from the sleep instruction downward.

6.3.2 Interrupt Priority

The processor supports 3 fixed highest priority levels and 4 programmable priority levels.

Exceptions with lower numbers are always executed first.

6.3.3 Error Handling

The processor supports only one hardware error handling mode: HardFault exception. HardFault priority -1, only NMI can preempt it.

The triggering reasons of HardFault include the following situations:

Error Type	Error conditions
Memory related	Bus Error. A bus error occurs when an illegal address is used in a bus transaction.
	An attempt was made to execute a program in the XN region.
Program Error	Execution of undefined instruction
	Trying to switch to ARM state

	<div>An attempt was made to perform an unaligned memory access.</div> <div>An SVC instruction was executed during a higher priority exception handler. An illegal value for EXC_RETURN was obtained when executing an exception return. An attempt was made to execute a BKPT instruction when debugging was not enabled.</div>
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Table 6-4 Hardfault triggering reasons list

The HardFault triggering cause of FM33LC0XX can be queried through registers to help software developers locate the cause of the error.

### 6.3.4 Lockup

When another HardFault occurs during the processor HardFault processing, or when an NMI occurs during the NMI processing

If HardFault occurs, the processor will enter a locked state (stop execution) and output a LOCKUP signal. At this time, the chip will automatically reset.

processor core instead of waiting for the watchdog timer to overflow.

## 6.4 Debugging Features

The processor supports the following debug features

- Pause, resume and single-step execution of the program
- Access to core registers and special registers
- Hardware breakpoints (4)
- Software breakpoints (unlimited number of BKPT instructions)
- Data monitoring point (1 point)
- Dynamic non-intrusive memory access (without stopping the processor)
- SWD interface

The debugging features of Cortex-M0 are based on the ARM CoreSight debugging architecture. For details, please refer to CoreSight Technology Architecture.

System Design Guide—ARM Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

### 6.4.1 Debug Function Pin

FM33LC0XX uses SWD debug interface, and only 4 wires (NRST, GND, SWIO, SWCLK) are required in user mode.

Debugging function can be realized. The 2-wire debug pin can be multiplexed as GPIO, and its function is selected and configured by software.

The NRST pin is used to reset the chip. Through the cooperation of NRST and SWD, the chip can be Halted at the first instruction after reset.

For the description of debugging pin multiplexing, refer to the I/O Control chapter.

### 6.4.2 Watchdog control in debug state

The watchdog can be enabled or disabled in debug mode. Software or debugger can configure the watchdog through the MCUDBGCR register.

The watchdog is turned on or off.

### 6.4.3 DEBUG reset

The DEBUG part of the kernel is only affected by power-on and power-off resets. Other system reset sources such as watchdog, pin reset, software reset, etc. are not affected.

The DAP circuit will not be reset. This allows the CPU core to be in reset state through a pin reset after the chip is powered on, but the debugger

It is still possible to establish communications with the DAP and set breakpoints normally, and the CPU can be put into debug mode immediately after reset is released.

It is recommended that the debugger connect to the kernel at system reset (set a breakpoint at the reset vector).

# 6.5 Registers

offset address	name	symbol
DBG (module start address: 0x40000000)		
0x00000004	DEBUG Configuration Register ÿDebug Configuration Registerÿ	DBG_CR
0x00000008	HardFault Query Register ÿHardFault Flag Registerÿ	DBG_HDFR

## 6.5.1 DEBUG Configuration Register (DBG\_CR)

FM33LC0XX extends the MCUIDBGCR register to configure the watchdog and timer in Debug state.

The registers can be rewritten via the SWD interface or software.

name	DBG_CR							
offset	0x00000004							
Bit31 Bit	name bit	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
	U-0							
permission	bit23 Bit	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
name	U-0							
bit	U-0							
permission	bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Position Name			AT_STO P	LPT_ST ON	GT2_STO P	GT1_STO P		BT1_STO P
Permission	U-0		R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1
bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Position Name							WWDT_S TOP	IWDT_ST ON
Bit permissions	U-0						R/W-1	R/W-1

Position No.	Mnemonics	Functional Description
31:14		RFU: Unimplemented, read as 0
13	AT_STOP	ATIM enable control bit in debug state (Stop ATIM under Debug Enable) 1: Turn off ATIM during debugging 0: Keep the original state of ATIM during debugging
12	LPT_STOP	LPTIM32 enable control bit in debug state (Stop LPTIM32 under Debug Enable) 1: Turn off LPTIM32 during debugging 0: Keep the original state of LPTIM32 during debugging
11	GT1_STOP	GPTIM1 enable control bit in debug state (Stop GPTIM1 under Debug Enable) 1: Turn off GPTIM1 during debugging 0: Keep GPTIM1 in its original state during debugging
10	GT0_STOP	GPTIM0 enable control bit in debug state (Stop GPTIM0 under Debug Enable) 1: Disable GPTIM0 during debugging 0: Keep GPTIM0 in its original state during debugging

Position No.	Mnemonics	Functional Description
9		RFU: Unimplemented, read as 0
8	BT_STOP	BSTIM32 enable control bit in Debug state (Stop BSTIM under Debug Enable) 1: Turn off BSTIM32 during debugging 0: Keep the original state of BSTIM32 during debugging
7:2		RFU: Unimplemented, read as 0
1	WWDT_STOP	WWDT enable control bit in Debug state (Stop WWDT under Debug Enable) 1: Turn off WWDT during debugging 0: Keep the original WWDT status during debugging
0	IWDT_STOP	IWDT enable control bit in debug state (Stop IWDT under Debug Enable) 1: Turn off IWDT during debugging 0: Keep IWDT enabled during debugging

### 6.5.2 HardFault Query Register (DBG\_HDFR)

name	DBG_HDFR							
offset	0x00000008							
bit Bit31	bit name	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
bit	U-0							
permission bit Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	
bit	U-0							
name	U-0							
bit permission bit	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Bit15	U-0							
bit name	U-0							
bit permission Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Position Name	DABORTE_ADDR_FLAG	DABORTE_RESP_FLAG	SVCUNDEF_FLAG	BKPT_FLAG	TBIT_FLAG	SPECIAL_OP_FLAG	HDF_REQUEST_FLAG	
Bit Permission	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Position No.	Mnemonics	Functional Description
31:7		RFU: Unimplemented, read as 0
6	DABORT_ADDR_FLAG	Address misaligned access error flag, write 1 to clear (Debug Abort Flag for misaligned Address)  1: Address misalignment access error 0: No unaligned address access is performed
5	DABORT_RESP_FLAG	Illegal address access error flag, write 1 to clear (Debug Abort Flag for HRESP)  1: An illegal address is accessed during bus transmission, causing HRESP to be high and generating an error 0: No illegal address is accessed
4	SVCUNDEF_FLAG	SVC instructions undefined flag, write 1 to clear (SVC undefined instruction Flag)  if the SVCcall priority is lower than the currently activelevel, or if HardFault or NMI is active, or PRIMASK is set,

Position No.	Mnemonics	Functional Description
		the core should treat SVC instructions as though theywere UNDEFINED
3	BKPT_FLAG	Execute the BKPT instruction flag, write 1 to clear it (Break point instruction Flag) 1: BKPT instruction executed 0: BKPT instruction is not executed
2	TBIT_FLAG	Thumb-State Flag, write 1 to clear (Thumb state Flag) 1: Switch to ARM state 0: In Thumb-State
1	SPECIAL_OP_FLAG	Special instruction flag, write 1 to clear (Special OP code Flag) 1: A special instruction code is executed, such as attempting to fetch an instruction in the XN area. 0: No special instruction code is executed
0	HDF_REQUEST_FLAG	Hardfault flag. Any type of hardfault will cause this bit to be set. 1 Clear (Hardfault Request Flag) 1: hardfault request 0: No hardfault request