ISE 5264

Modelling and Analysis of Semiconductor Manufacturing

PROJECT PHASE II REPORT

TEAM MEMBERS

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On My honor, as a hokie, I have neither given nor received unauthorized aid on this work

OBJECTIVE

To apply the basics of AutoMod simulation software learned in Assignment 2 to a real life like wafer fabrication facility.

PROBLEM DESCRIPTION

The Department of Electrical and Computer Engineering (ECE) at Department at Virginia Tech has recently built a research and development fab, the Whittemore Fab. It is built to pilot test the state-of-the-art Automated Material Handling System (AMHS) manufactured by PRI Automation. The process areas and AMHS layout are shown in Figure 1. Note that the stockers and bays are located symmetrically. Inside each process bay, the tools are located in such a way that they are equidistant among each other. In addition, the tools are arranged in alphabetical order along the loop of the process bay.

The AMHS includes one inter-bay (the central loop) and four intra-bays (the smaller loops), namely, CMP, Diffusion, Etch and Lithography. There are 37 tools in this fab, 10 tools in the CMP Bay, 8 tools in the DIFF Bay, 11 tools in the ETCH Bay, and 8 tools in the LITHO Bay. The tool names and processing times are listed in Table 1. The AMHS related data are included in Table 2.

The followings are the assumptions you can make for this project.
• Each vehicle is capable of carrying one lot at a time.
• All lots are ready at the beginning and have the same priority.
• At the beginning, all lots are stored in the stocker S-CMP and all AGVs are parked at the stockers. After finishing all the tasks, all AGVs return to their original places.
• Each stocker has unlimited capacity.

Processing times are constant with no variability involved. Also, the setup time at each tool is negligible.
• On the intra-bay transport systems, empty vehicles move continuously until reaching a point where a FOUP is ready to be transferred onto a vehicle.
• For each move, the path between the origin and destination is known. Thus, there are no alternative routings.
• Pickup/unload time at the stocker or at the tool is negligible. We also assume that the AGVs move at a constant speed.
• An AGV performs tasks only in its own bay.
• Vehicles and stockers do not fail and do not need preventive maintenance.
• The fail-related data for the tools are listed in Table 1

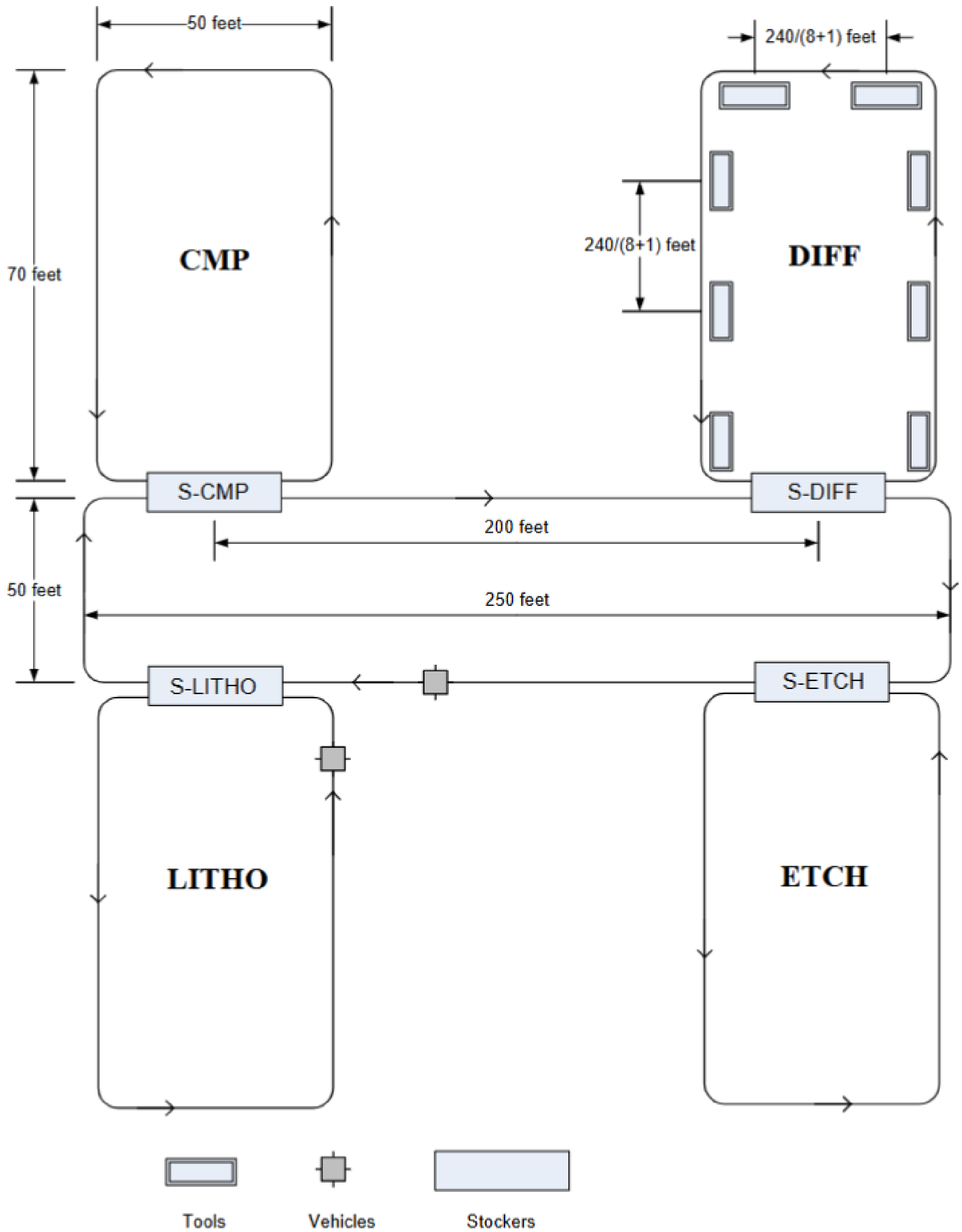


Figure 1 The process areas and the AMHS layout*

Figure 1: AMHS Layout

Workstation No	Automod Tool Name	Process Type	Process Bay	No. of machines	Mean Processing Time	MTTF	MTTR
1	TOOLS1	Al Clean and Deposition	CMP	1	1	98.22	8.71
2	TOOLS2	Al Sinter	CMP	1	0.5	60.43	5.28
3	TOOLS3	Alignment Check	CMP	1	0.2	22.37	2.83
4	TOOLS4	Bonding	CMP	1	0.5	58.47	3.12
5	TOOLS5	Bond-pad Opening	CMP	1	0.4	33.31	1.69
6	TOOLS6	Cleaning	CMP	1	0.4	41.41	3.23
7	TOOLS19	Dicing	ETCH	1	0.5	51.51	1.27
8	TOOLS20	Dry Etch	ETCH	1	2.2	117.22	9.31
9	TOOLS21	Dry Release Etch	ETCH	1	2	114.33	8.12
10	TOOLS22	Dry Resist Strip	ETCH	1	0.5	49.36	2.21
11	TOOLS30	Hard Brake	LITHO	1	0.5	49.49	3.82
12	TOOLS31	Inspection	LITHO	8	0.2	21.11	1.78
13	TOOLS32	Mask Exposure	LITHO	1	1	104.34	9.25
14	TOOLS33	Measurement	LITHO	5	0.2	22.53	1.66
15	TOOLS34	Mount Wafer	LITHO	1	0.2	19.61	2.12
16	TOOLS11	Organic Resist Strip	DIFF	1	0.5	55.21	3.22
17	TOOLS12	Oxide Deposition	DIFF	1	1	121.78	8.91
18	TOOLS13	Pre Furnace Clean	DWF	1	0.2	33.12	2.29
19	TOOLS14	Pre Fire Glass Frit	DIFF		3	312.12	21.11
20	TOOLS15	Record Test Data	DIFF	1	0.1	11.17	1.46
21	TOOLS16	Remove Bond-pad Strip	DIFF	1	0.5	61.13	4.99

22	TOOLS35	Resist Coat	LITHO	1	1	106.55	10.23
23	TOOLS36	Resist Develop	LITHO	1	1	107.7	11.13
24	TOOLS37	Screen Printing	LITHO	1	1	107.45	10.94
25	TOOLS23	Silicon Trench Etch	ETCH	1	1	115.34	9.76
26	TOOLS24	Sorting	ETCH	1	0.2	19.97	1.32
27	TOOLS25	Spin Rinse Dry	ETCH	1	0.5	21.39	2.31
28	TOOLS26	Tape and Label	ETCH	1	0.3	44.11	2.4
29	TOOLS17	Tape Curing	DIFF	1	0.1	19.17	1.34
30	TOOLS18	Thermal Oxide	DIFF	1	1	121.56	7.42
31	TOOLS7	Wafer Alignment	CMP	1	0.3	51.01	2.77
32	TOOLS8	Wafer Probe	CMP	1	0.5	54.02	3.81
33	TOOLS9	Wafer Scribe	CMP	1	0.1	29.31	1.94
34	TOOLS10	Wafer Scribe Clean	CMP	1	0.4	31.4	1.08
35	TOOLS27	Wet Etch	ETCH	1	0.2	23.5	1.06
36	TOOLS28	Wet Oxidation	ETCH	1	1	121.9	8.76
37	TOOLS29	Wet Resist Strip	ETCH	1	0.5	61.77	4.63

Table 1: Segregated Tool names according to the Bays with process flow

Table 2 AMHS data

Number of vehicles	Inter-bay	12
	CMP Bay	5
	DIFF Bay	6
	ETCH Bay	8
	LITHO Bay	3
Vehicle travel speed (loaded)(feet/sec)		1.0
Vehicle travel speed (empty) (feet/sec)		1.5
Inter-bay loop	Length (feet)	250 (horizontal).
	Width (feet)	50
Intra-bay loop	Length (feet)	70 (vertical)
	Width (feet)	50
Stocker capacity (lots)	200	
Tool buffer capacity (lots)	2	

Figure 2: AMHS Data

Question: Given the information above, build the AutoMod model for the front-end process only. Which rules achieve the best performance in terms of cycle time? Also, investigate use of the CONWIP-based job loading policy and BMI-based job dispatching policy.

Operations in the front end process are as follows:

Step No.	Name of the Step
1	Lot Start
2	Wafer Scribe
3	Wafer Scribe Clean
4	Spin Rinse Dry
5	Resist Coat
6	Mask Exposure
7	Resist Develop
8	Inspection
9	Dry Oxide Etch
10	Wet Resist Strip
11	Spin Rinse Dry
12	Inspection
13	Oxide Deposition
14	Measurement
15	Resist Coat
16	Mask Exposure
17	Resist Develop
18	Inspection
19	Dry Oxide Etch
20	Wet Resist Strip
21	Spin Rinse Dry
22	Inspection

23	Wet Etch
24	Spin Rinse Dry
25	Silicon Trench Etch
26	Inspection
27	Wet Etch
28	Spin Rinse Dry
29	Inspection
30	Oxide Deposition
31	Measurement
32	Dry Oxide Etch
33	Measurement
34	Dry Release Etch
35	Measurement
36	Wet Etch
37	Spin Rinse Dry
38	Measurement
39	Pre Furnace Clean
40	Inspection
41	Wet Etch
42	Spin Rinse Dry
43	Wet Oxidation
44	Measurement
45	Pre Furnace Clean
46	Spin Rinse Dry
47	Inspection
48	Oxide Deposition
49	Measurement
50	Inspection
51	Oxide Deposition
52	Measurement
53	Resist Coat
54	Mask Exposure
55	Resist Develop
56	Inspection
57	Dry Oxide Etch
58	Wet Resist Strip
59	Spin Rinse Dry
60	Inspection
61	Al Clean and Deposition
62	Resist Coat
63	Mask Exposure
64	Resist Develop
65	Inspection
66	Measurement

67	Wet Etch
68	Spin Rinse Dry
69	Inspection
70	Dry Resist Strip
71	Organic Resist Strip
72	Spin Rinse Dry
73	Al Sinter
74	Inspection
75	Oxide Deposition
76	Measurement
77	Resist Coat
78	Mask Exposure
79	Resist Develop
80	Inspection
81	Measurement
82	Wet Etch
83	Spin Rinse Dry
84	Inspection
85	Dry Resist Strip
86	Organic Resist Strip
87	Spin Rinse Dry
88	Inspection
89	Oxide Deposition
90	Measurement
91	Resist Coat
92	Mask Exposure
93	Resist Develop
94	Inspection
95	Dry Oxide Etch
96	Measurement
97	Dry Resist Strip
98	Organic Resist Strip
99	Spin Rinse Dry
100	Inspection
101	Wet Etch
102	Spin Rinse Dry
103	Silicon Trench Etch
104	Inspection
105	Wet Etch
106	Spin Rinse Dry
107	Record Test Data
108	Hold

Table 2: Process Flow

FAB MODEL

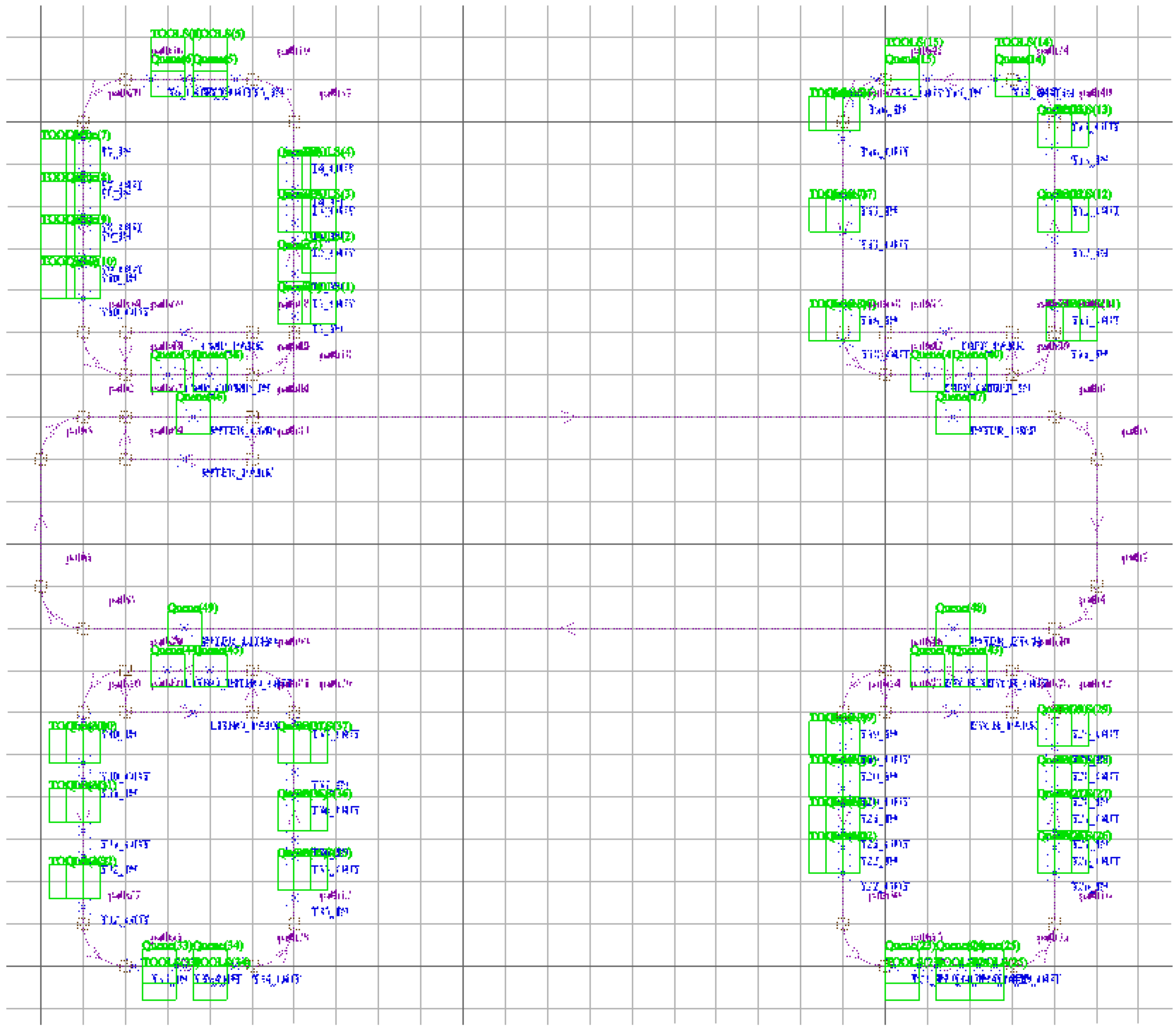


Figure 3: Fab model of 37 tools with single vehicle.

We modeled the layout with 37 tools but we cant able to assign the multiple vehicles to the respective bays due to limit of instances for student version in the Automod. So for Front end manufacturing process it requires only 21 tools. So we eliminated the 15 tools to get some space to add park list to the multiple vehicles. The model with reduction of the tools can be seen in the next page.

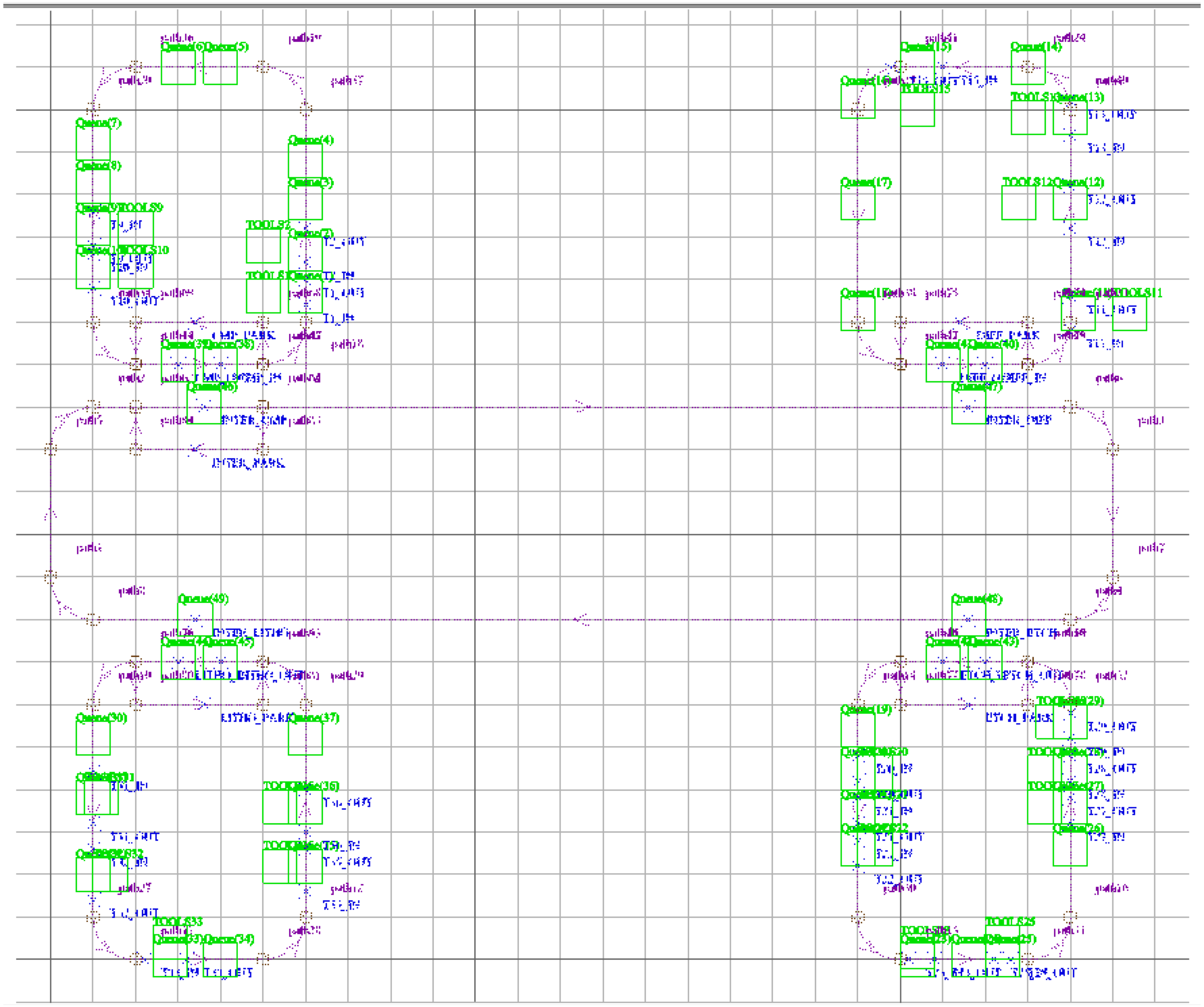


Figure 4: Fab model after reducing the tools and control points

METHODOLOGY

1. **Fab Layout:** In the layout there are five bays, 4 of them are Intra bays and 1 is an Inter bay. Resources, control points, queue points, Loads were added to the layout. The syntax of the control point is mentioned below :
2. **Control points :** In project Phase 2, we denoted control point as the below mentioned
   For tools Syntax:
   [Tool Name]_in/out
   Example: For tool number 1 : T1_in and T1_out

   For Entry and Exit of the Intra Bay Station Syntax:
   [StationName]_in/out
   Example: for diffusion : DIFF_in and DIFF_out

   For Entry and Exit of the Inter-Bay system Syntax:

   INTER_IN and INTER_OUT

3. **Queue Points:** In the above project, we described queue points in the below mentioned format, we used only single queue for the tools rather than two ques

   For Tools : Syntax: Queue_in/out(ToolNumber)
   Example: at Tool 1 -> Queue(1) and Queue(2)

   For Entry and Exit of the Intra bay station and Inter bay station

   Syntax: Queue_entry_in/out(number)

4. **Resources :** Resources at each station is represented by Tools(number)
   Example: In CMP station there are 10 tools and it is represented as Tools(1), Tools(2), …..Tools(10)

5. **Source_File:** The sequence of the 108 processing steps of the front end manufacturing process along with the processing times are written in the code and attached in the source file section.

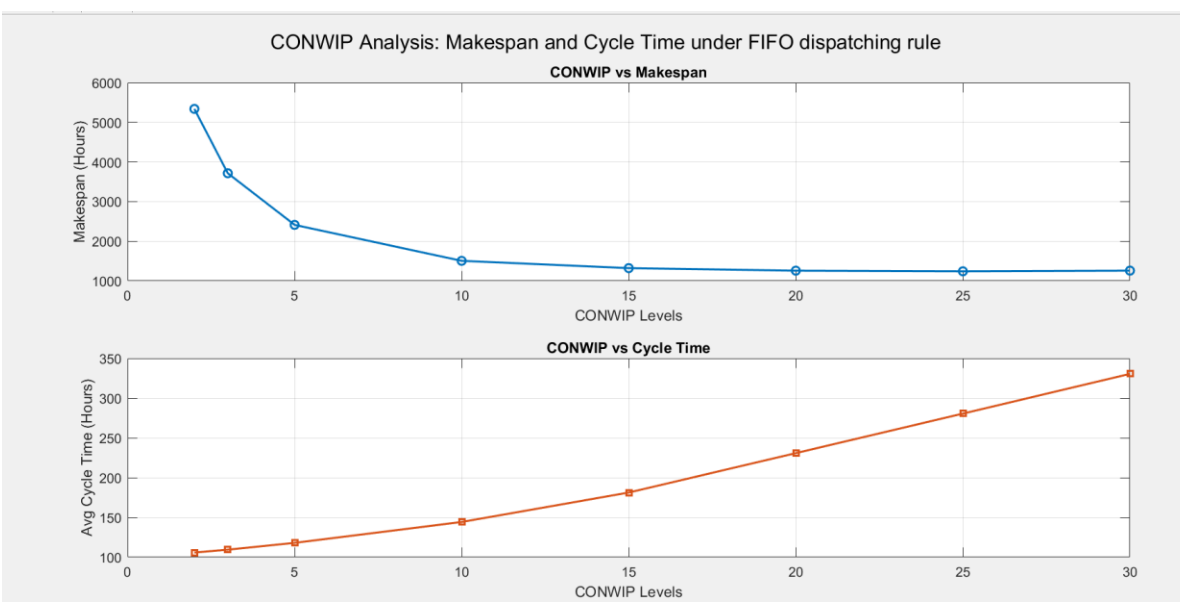
6. **Simulation:** The final model was simulated with all possible combinations of load sequences to achieve results of cycle time and makespan. Please find the onedrive link of the fab model in the final section of the report.

RESULTS AND DISCUSSIONS

- **Dispatching rule : FIFO**

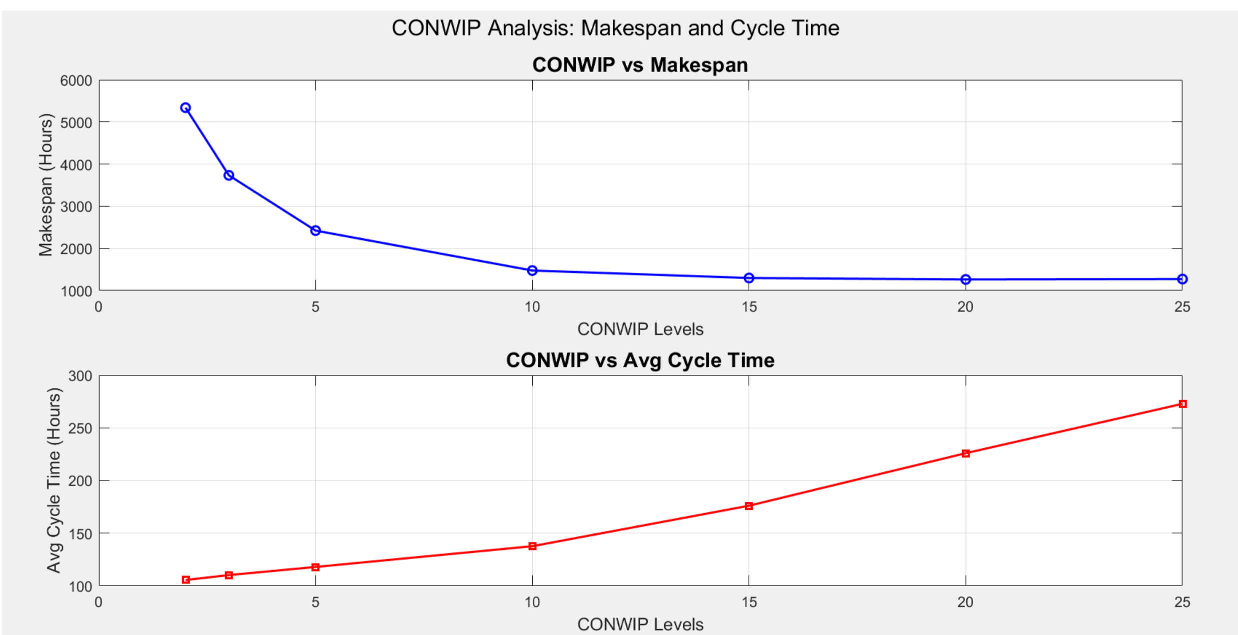
We simulated the model with lot size of 5 with different CONWIP level with different load activation time and we check the effect of cycle time and makespan with FIFO (First in First out) dispatching rule.

Lot size = 5			
CONWIP	**Load - 100 wafers activation time**	**Makespan (Hrs)**	**Avg Cycle Time (hrs)**
2	1 lot/15 hours	5338.392642	105.885425
3	1 lot/15 hours	3715.001	109.43
5	1 lot/15 hours	2412.48	118.01
10	1 lot / 15 hours	1505.015	144.28
15	1 lot / 15 hours	1320.6	181.28
20	1 lot / 15 hours	1256.99	230.84
25	1 lot/ 15 hours	1240.6	280.54
30	1 lot/15 hours	1257.47	330.51



- When we increased the load activation time 1/ 15 hours to 1 lot/ 30 hours and check the effect of job releasing into the system on makespan and cycletime. We observe that makespan doesn't have much effect but cycletime is low when we increased the job releasing time into the system.

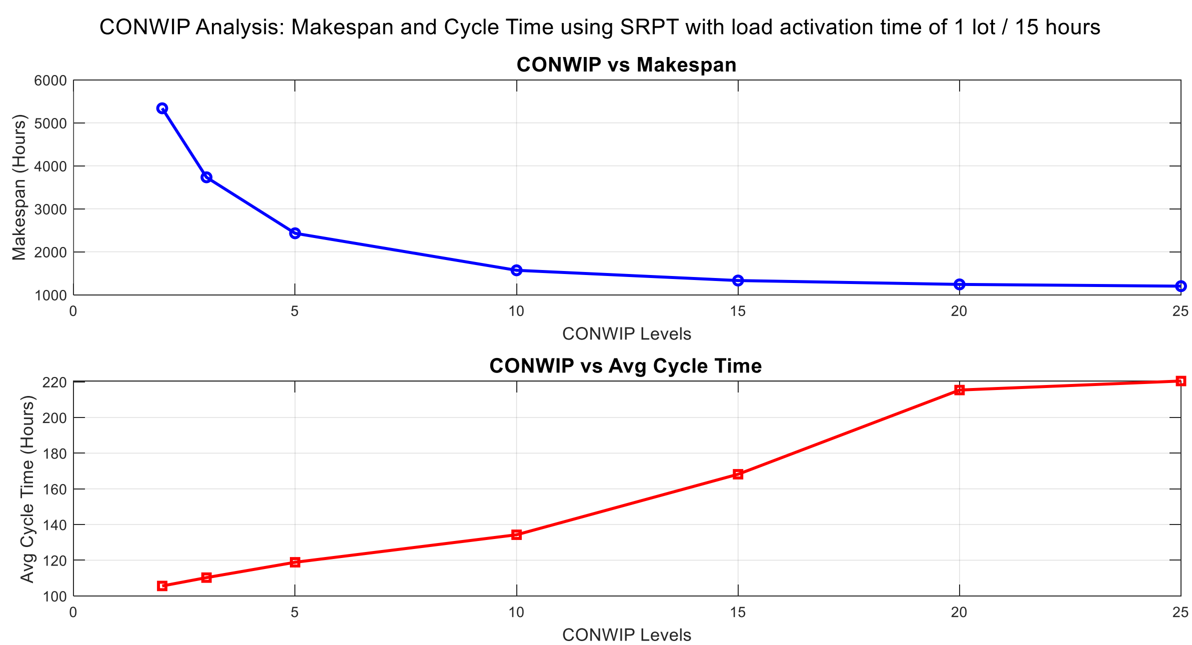
Lot size= 5			
CONWIP	**Load 100 wafers activation time**	**Makespan (hrs)**	**Avg Cycle Time (hrs)**
2	1 lot/30 hours	5338.39	105.58
3	1 lot/30 hours	3732.69	110.25
5	1 lot/30 hours	2422.206	117.97
10	1 lot/30 hours	1474.76	137.66
15	1 lot/30 hours	1297.26	176.09
20	1 lot/30 hours	1263.15	225.93
25	1 lot/30 hours	1272.57	272.78



Effect of Makespan and Cycle Time under FIFO dispatching rule with varying CONWIP and load activation time is 1 lot / 15 hours

Dispatching rule : SRPT

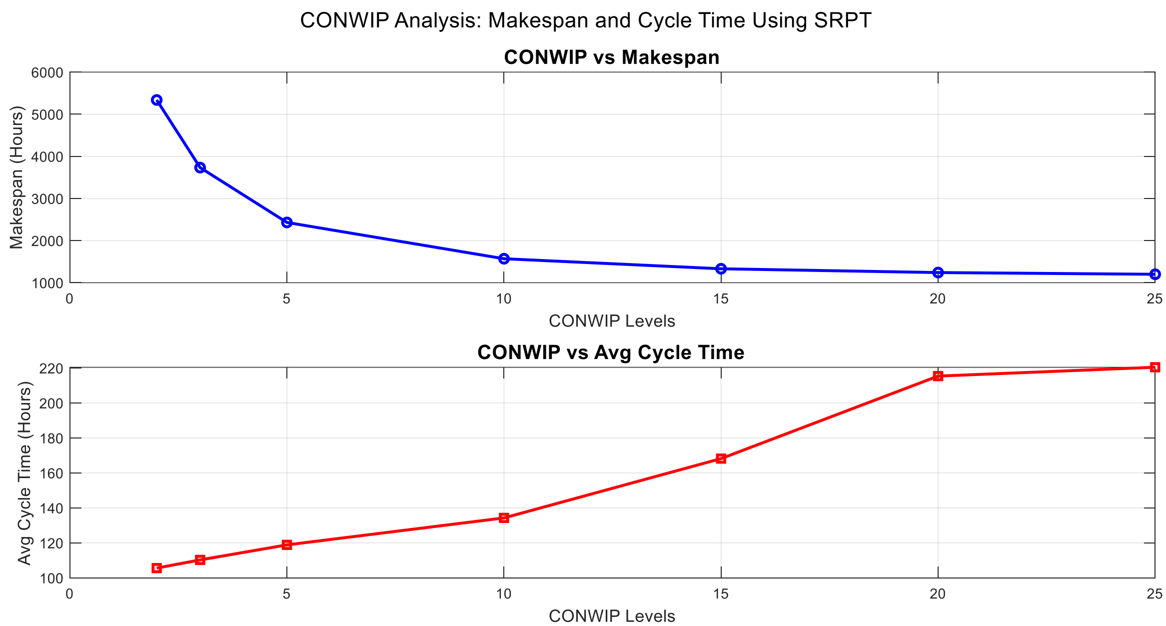
CONWIP	Load 100 wafers activation time	Makespan (hrs)	Cycle Time (hrs)
5	1 lot/15 hours	2447.60	120.17
10	1 lot/15 hours	1567.58	135.08
15	1 lot/15 hours	1328	168.97
20	1 lot/15 hours	1253.81	229.84
25	1 lot/15 hours	1209.59	260.78



CONWIP	Load 100 wafers activation time	Makespan (hrs)	Avg Cycle Time (hrs)
2	1 lot/30 hours	5338.39	105.58
3	1 lot/30 hours	3732.6	110.25

5	1 lot/30 hours	2430.45	118.85
10	1 lot/30 hours	1568.9	134.27
15	1 lot/30 hours	1330.58	168.176
20	1 lot/30 hours	1240.6	215.37
25	1 lot/30 hours	1200	220.432

With load activation time of 1 lot / 30 hours



CONCLUSION:-

From the above fab model we can see that the CT for both SRPT and FIFO varies with respect to conwip level and the load activation time. We didn't see much difference in the makespan with change in the load activation time. But we can see small change in the decrease of the cycletime when we increase in the load activation time. And in both FIFO and SPRT we can see a small change in the cycle time. SRPT has low cycle times for some of the cases when compared to FIFO.

AUTOMOD MODEL:
[Semiconductor_ phase 2_zip_Final.zip]