ISE 5264
Modelling and Analysis of Semiconductor Manufacturing

ASSIGNMENT II

TEAM MEMBERS

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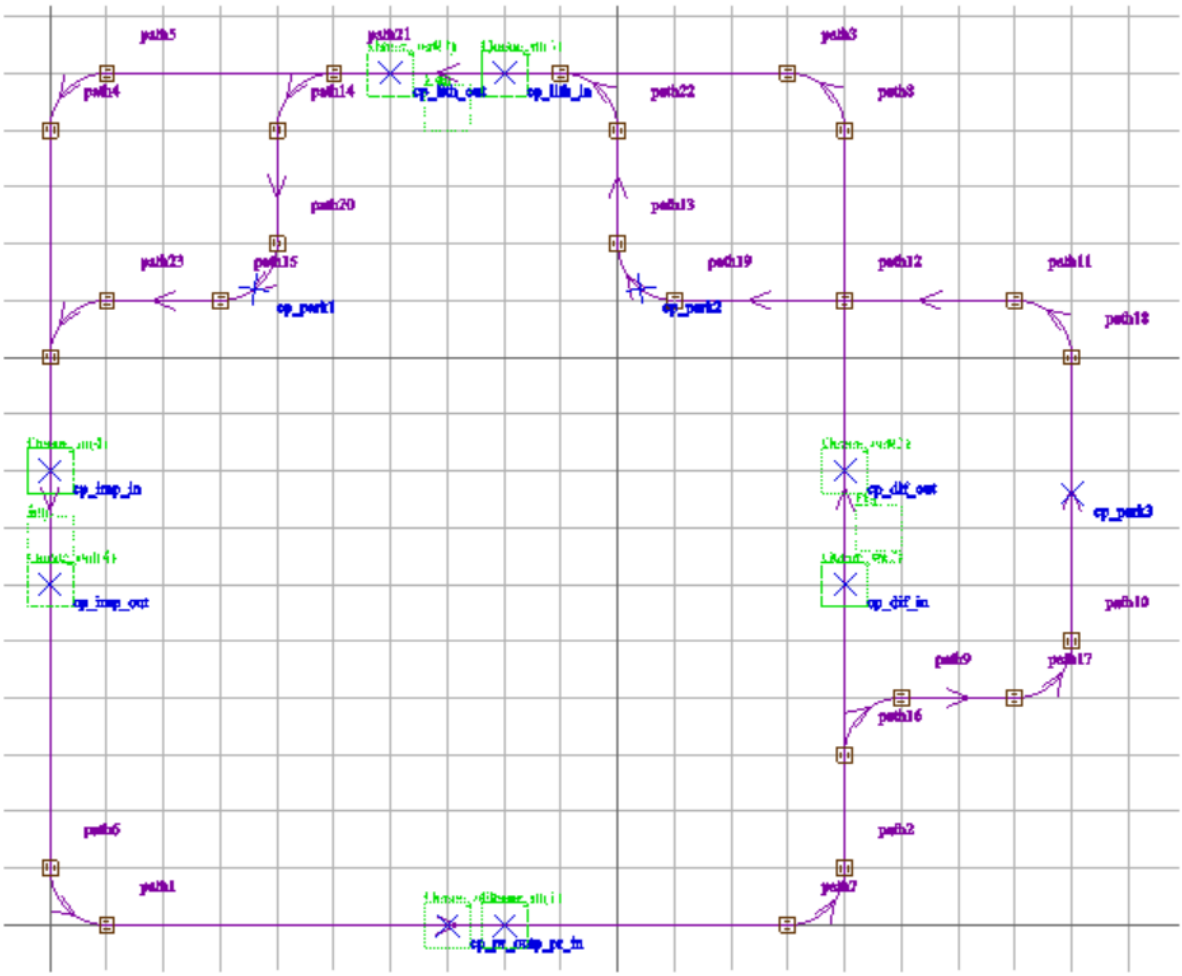
On My honor, as a hokie, I have neither given nor received unauthorized aid on this work.

FAB LAYOUT


path5
path21
path3
path4
path14
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cp_litk_in
path22
path8
path20
path13
path23
path15
path19
path12
path11
cp_park1
cp_park2
path18
cp_imap_in
cp_diff_out
cp_park3
cp_imap_out
cp_diff_in
path10
path9
path17
path16
path6
path2
path1
path7
cp_pr_comp_pr_in

JOB LOADING AND SEQUENCING

In this section we Assigned the priority to jobs at stations based on FIFO (First In, First Out) and SRPT (Shortest Remaining Processing Time) methods and also Implementing job loading strategies like CONWIP (Constant Work In Process) and lot dispatch.

Q1: Using FIFO on every machine, determine the makespan, cycle time and throughput when the wafers are uniformly released into the fab at the frequency of:

Answer 1:

Frequency	Makespan (Min)	Cycle Time(Min)
1 Wafer/4.5 hour	270640.053	639.42
1 Wafer/5 hour	300640.053	639.42
1 Wafer/6 hour	360638.433	669.97
1 Wafer/8 hour	480638.087	637.86
1 Wafer/10 hour	600638.087	637.86
1 Wafer/12 hour	720638.087	637.86

Q2: Using SRPT on every machine, determine the makespan, cycle time and throughput when the wafers are uniformly released into the fab at the frequency of:

Answer 2:

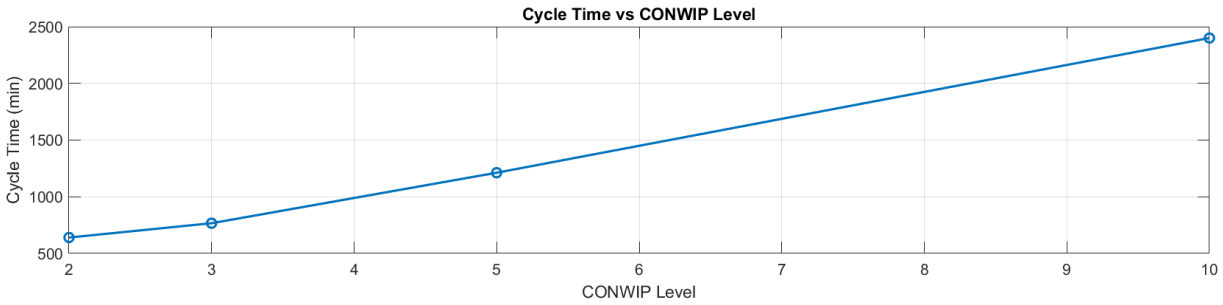
Frequency	Makespan (Min)	Cycle Time (Min)
1 Wafer/10 hour	600863.326	638.086
1 Wafer/12 hour	720638.087	638.086

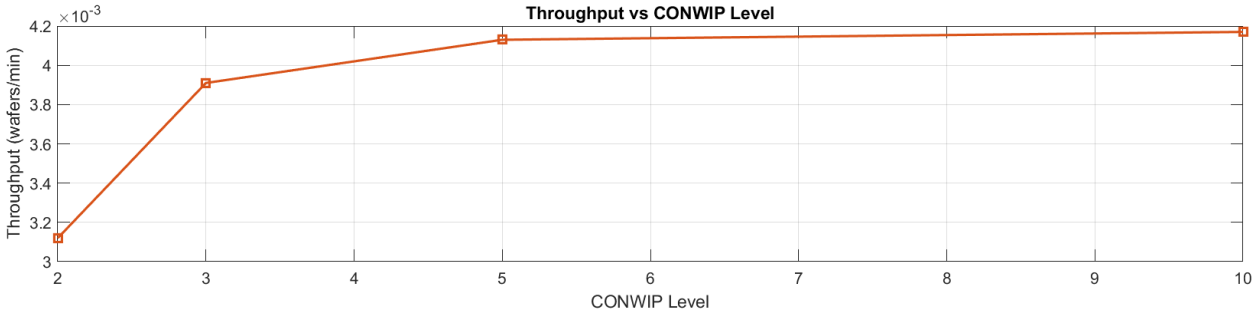
Q3: Using FIFO on every machine, determine the makespan , cycle time and throughput under the CONWIP job release policy when:

Answer 3:

CONWIP	Makespan (Min)	Cycle Time (Min)	Throughput (wafers/min
2	320323.281	640.414	0.00312
3	251524.199	766.759	0.00391
5	240113.972	1212.072	0.00413
10	240164.627	2400	0.00417

Please find the graphs of the Cycle Time and Throughput vs CONWIP Level under FIFO job release policy.



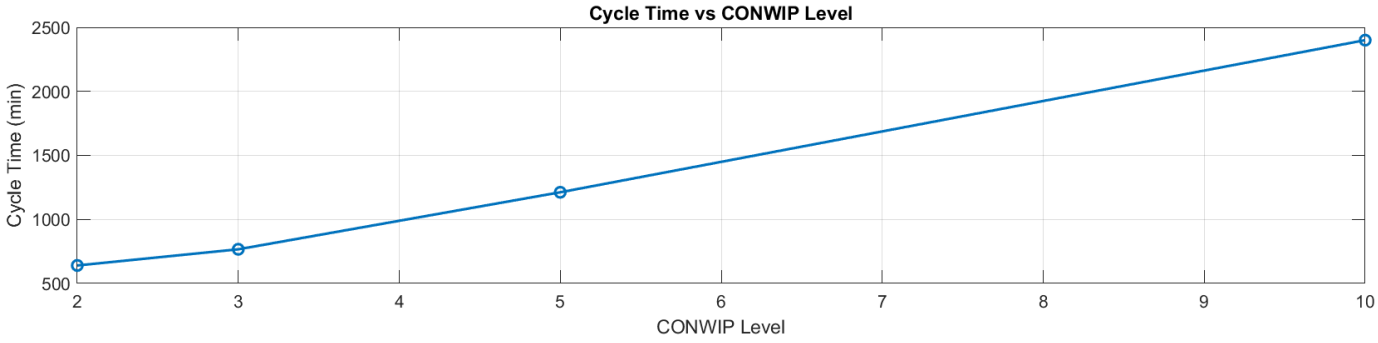


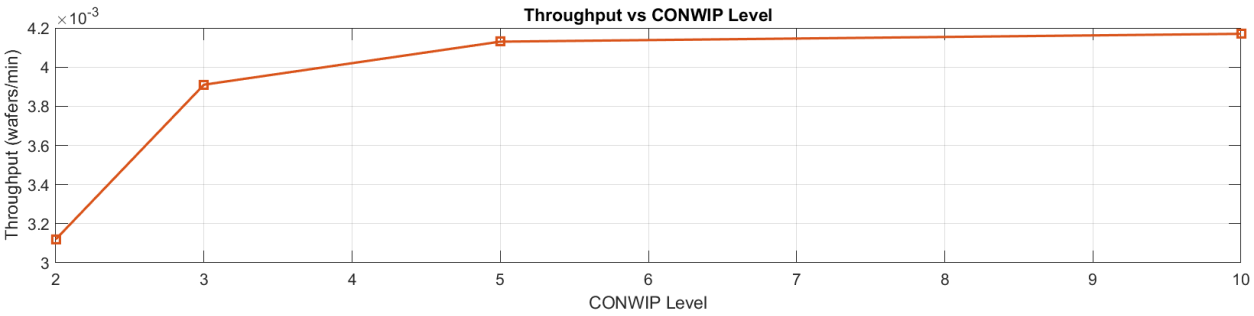
Q4: Using SRPT on every machine, determine the makespan, cycle time and throughput under the CONWIP job release policy when:

Answer 4:

CONWIP	Makespan (Min)	Cycle Time(Min)	Throughput (wafers/min)
2	425828.96	635.631	0.00314
3	252159.712	745.95	0.00402
5	240385.485	1199.157	0.00416
10	240278.032	2392.45	0.00417

graphs of the Cycle Time and Throughput vs CONWIP Level under SRPT job release policy.





Q5: Instead of loading one wafer at-a-time, now consider their release into the fab in lots. Using FIFO on every machine and lot loading policy with lot size = 5, determine the makespan , throughput and cycle time for the following loading rates.

Answer 5:

Loading Rates	Makespan (Min)	Cycle Time (Min)
1 lot/15 hrs	240946.899	4389.933
1 lot/20 hrs	241454.627	1454.626

Q6:Consider the same situation as in 5 above except that, now, the lots are processed using SRPT on every machine and lot size = 6. Determine the makespan , throughput and cycle time for the following loading rate

Answer 6:

Loading Rates	Makespan (Min)	Cycle Time (Min)
1 lot/15 hrs	240718.972	5541.416

Q7: Determine the makepan when a wafer is released into the fab once a wafer is completed at the BN station. Initially, 2 wafers are released into the system.

Answer 7 : 240085.498 minutes

Q8: The same situation as in 7 above except that now a wafer is released into the fab once a wafer is completed at the Litho station. Initially, 2 wafers are released into the system

Answer 8: 240117.979 minutes

MULTI – PRODUCTS

Managing multiple types of wafers in a system involves optimizing workflows to handle varying sizes, priorities, and processing requirements efficiently. Job releasing or dispatching help allocate resources and sequence tasks effectively. Combining both ensures streamlined operations, improved throughput, and reduced cycle times in wafer manufacturing systems.

Q9: Consider two types of wafers, namely, A and B. The processing/usage requirements for these wafers are given below:

The values given in the tables are mean processing time values.

• For Cases 1-5, the processing times are deterministic.

• Cases 6 and 7, include variable processing times.

The LV and HV mentioned at the top of some columns indicate high and low variability, where for high variability std =1.5*mean, and for low variability: std =0.5*mean.

Consider that a CONWIP of 4 wafers is maintained and a total of 1000 wafers A and 1000 wafers B are to be processed. Find the cycle times for the processing sequence given below, for all the seven cases:

All the units of makespan and cycletime are minutes and the processing times is considered in hours

CASE 1:

	WS1	WS2	WS3	WS4
A	3	6	3	3
B	3	3	3	9

Sequence	Makespan (Min)	Cycle time A Constant (Min)
AA..BB..	766930.175	1534.236
BB..AA..	767823.39	1535.042
ABAB	720613.96	1439.786
BABA	720608.634	1440.134

- **ABAB is the best job loading scenario for Case 1 which is giving lowest cycle time**

CASE 2:

	WS1	WS2	WS3	WS4
A	6	10	6	12
B	12	10	6	6

Sequence	Makespan	Cycle time
AA..BB..	1233334.03	2465.370
BB..AA..	1232324.82	2465.44
ABAB	1204371.54	2407.177
BABA	1205275.88	2409.652

- **ABAB is the best job loading scenario for Case 2 which is giving lowest cycle time**

Case 3

	WS1	WS2	WS3	WS4
A	6	10	6	12
B	4	6	6	12

Sequence	Makespan	Cycle time
AA..BB..	14439446.5	2880.405
BB..AA..	14439446	2879.688
ABAB	1441033.53	2879.725
BABA	14410282.8	2879.714

- **BBBBB…AAAAA is the best job loading policy for case 3**

Case 4: (6 Processing Steps)

	WS1	WS2	WS3	WS4	WS1	WS4
A	3	6	3	3	4	2
B	3	3	3	9	6	6

Sequence	Makespan	Cycle Time
AA..BB..	1340365.4	2678.951
BB..AA..	1354090.88	2707.482
ABAB	1235398.75	2470.048
BABA	1240194.08	2479.791

- **ABAB is the best job loading scenario for Case 4 which is giving lowest cycle time**

Case 5

	WS1	WS2	WS3	WS4	WS1	WS4
A	3	6	3	3	9	6
B	3	3	3	9	6	6

Sequence	Makespan	Cycle Time
AA..BB..	1893553.08	3785.780
BB..AA..	1801452.2	3106.438
ABAB	1537889.19	3074.686
BABA	1808343.32	3613.791

- **ABAB is the best job loading scenario for Case 5 which is giving lowest cycle time**

Case 6

	WS1	WS2 (LV)	WS3	WS4 (HV)
A	3	6	3	3
B	3	3	3	9

Sequence	Makespan	Cycle Time
AA..BB..	1078536.99	2158.064
BB..AA..	1055069.17	2109.322
ABAB	1076928.01	1914.278
BABA	1076934.68	1966.247

Case 7:

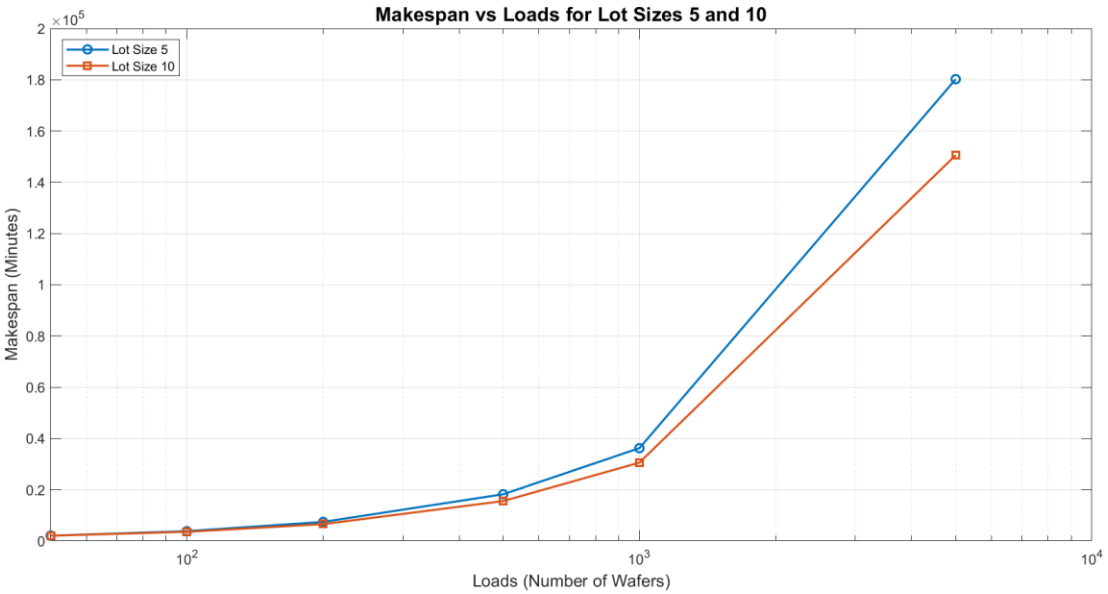
	WS1	WS2 (HV)	WS3	WS4 (LV)
A	3	6	3	3
B	3	3	3	9

Sequence	Makespan	Cycle Time
AA..BB..	929928.863	1860.866
BB..AA..	938515.799	1876.756
ABAB	930781.672	1537.579
BABA	930278.13	1562.127

Q10: For lot sizes of 5, 10, 50 (all stations process in lots) determine the makespan, time spent for each load in the system, and CT, and plot their values for the following loads:

Answer 10:

Loads	Lot Size	Makespan	Cycle Time
50	5	2062.7695	206.27695
	10	2046.6895	409.3379
	50	2067.6168	2067.6168
100	5	3817.2421	190.8621
	10	3567.6168	356.7616
	50	3597.6168	1798.8084
200	5	7432.5738	185.8143
	10	6567.6168	328.3808
	50	6597.6168	1649.4042
500	5	18222.5023	182.2250
	10	15567.6168	311.3523
	50	15597.6168	1559.761683
1000	5	36215.0608	181.0753
	10	30567.6168	305.6761
	50	30597.6168	1529.8808
5000	5	180211.5933	180.2115
	10	150567.6168	301.1352
	50	150597.6168	1505.9761



AUTOMOD MODEL

Please find the automod model in the below link

Assignment 2_final.zip