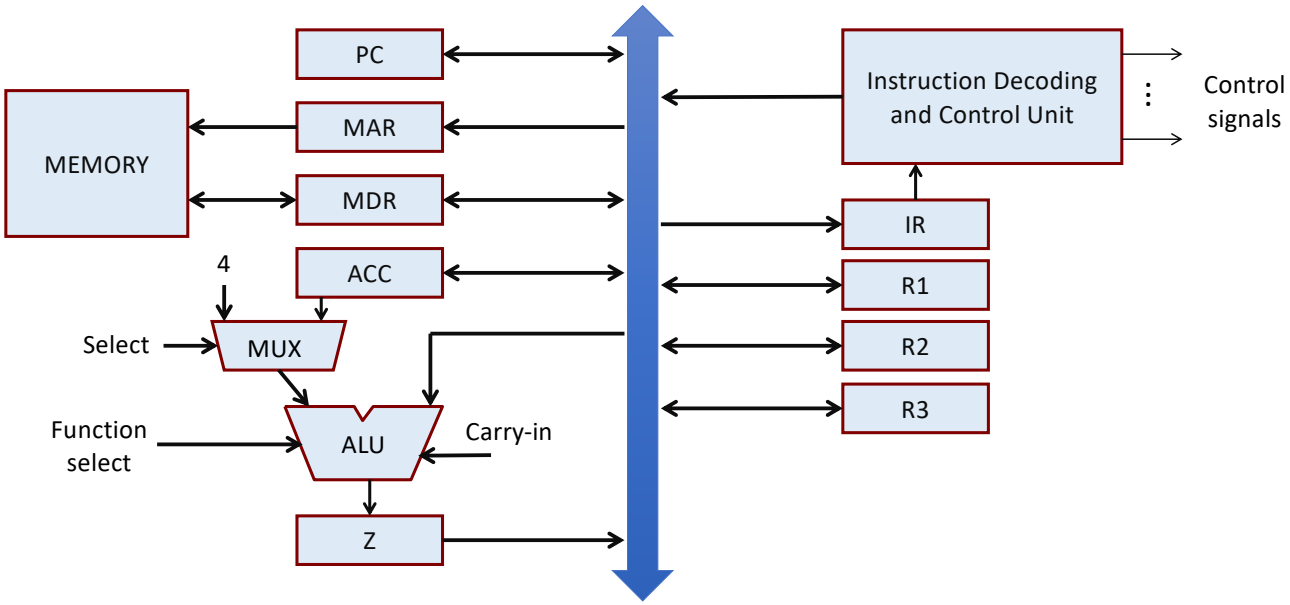
Department of Computer Science and Engineering
Indian Institute of Technology Kharagpur

Computer Organization and Architecture (CS31001)
Class Test 1

Date: August 22, 2024 **Time: 60 minutes** **Full Marks: 50**

Answer all the questions

Consider the following data-path for a single-bus accumulator-based processor. There is a special-purpose register called *Accumulator* (ACC) that serves as one of the source operands and also the destination operand for instructions. R1, R2, R3 are general-purpose registers, and Z is a temporary register. Assume that the memory is byte-oriented and all instructions and registers are of size 32 bits.



a) List all the control signals corresponding to the data-path diagram shown above. **[10 marks]**

PC_{in}, PC_{out},

MAR_{in}, MDR_{in}, MDR_{out}, READ, WRITE, WMFC,

ACC_{in}, ACC_{out}, Select4, $Select_{ACC}$, Z_{in}, Z_{out}, IR_{in}, IR_{out}, ADD, SUB

$R1_{in}$, $R1_{out}$, $R2_{in}$, $R2_{out}$, $R3_{in}$, $R3_{out}$,

END

b) Write down the control signals along with the time steps for executing the following instructions: **[25 marks]**

```
i)    LOAD  60(R2)        // ACC = Mem[R2+60]
ii)   STOR  50(R3)        // Mem[R3+50] = ACC
iii)  ADD   (R1)          // ACC = ACC + Mem[R1]
iv)   SUB   Label         // ACC = ACC - Mem[Label]
v)    BZ    Loop          // If Z == 1, PC = PC + Loop
```

Common for all instructions

T1: PC_{out}, MAR_{in}, Select4, Z_{in}, READ, ADD
T2: Z_{out}, PC_{in}, WMFC
T3: MDR_{out}, IR_{in}

Instruction I1

T4: $R2_{out}$, ACC_{in}, $Select_{ACC}$
T5: IR_imm_{out}, ADD, Z_{in}
T6: Z_{out}, MAR_{in}, READ
T7: WMFC
T8: MDR_{out}, ACC_{in}, END

Instruction I2

T4: $R3_{out}$, ACC_{in}, $Select_{ACC}$
T5: IR_imm_{out}, ADD, Z_{in}
T6: Z_{out}, MAR_{in}
T7: ACC_{out}, MDR_{in}, WRITE
T8: WMFC, END

Instruction I3

T4: MAR_{in}, $R1_{out}$, READ
T5: $Select_{ACC}$, MDR_{out}, WMFC, ADD, Z_{in}
T6: Z_{out}, ACC_{in}, END

Instruction I4

T4: MAR_{in}, IR_imm_{out}, READ
T5: $Select_{ACC}$, MDR_{out}, WMFC, SUB, Z_{in}
T6: Z_{out}, ACC_{in}, END

Instruction I5

T4: if (Z == 0) then END
T5: PC_{out}, ACC_{in}
T6: $Select_{ACC}$, IR_imm_{out}, ADD, Z_{in}
T7: Z_{out}, PC_{in}, END

c) Show the design of a hardwired control unit for the above five instructions. Draw the overall schematic diagram, and show the logic expressions to generate the control signals. **[15 marks]**

BLOCK DIAGRAM HERE (5 marks)

PC_{out} = T1 + T5.I5

PC_{in} = T2 + T7.I5

Z_{in} = T1 + T5.(I1 + I2 + I3 + I4) + T6.I5

Z_{out} = T2 + T6.(I1 + I2 + I3 + I4) + T7.I5

ACC_{in} = T4.(I1 + I2) + T6.(I3 + I4) + T8.I1

MAR_{in} = T1 + T4.(I3 + I4) + T6.(I1 + I2)

MDR_{out} = T3 + T5.(I3 + I4) + T8.I1

Select4 = T1

$Select_{ACC}$ = T4.(I1 + I2) + T5.(I3 + I4) + T6.I5

and others … (10 marks)

ROUGH WORK