PCB

Board size: 63.0x35.6 mm (2.48x1.4 inches)

- This is the size of the rectangle that contains the board
- Thickness: 1.6 mm (63 mils)
- Material: FR4
- Finish: HAL
- Layers: 4
- Copper thickness: 35 µm

Solder mask: TOP / BOTTOM

- Color: Green

Silk screen: TOP / BOTTOM

- Color: White

Important sizes

Clearance: 0.15 mm (6 mils)

Track width: 0.38 mm (15 mils)

- By design rules: 0.15 mm (6 mils)

Drill: 0.5 mm (20 mils)

- Vias: 0.5 mm (20 mils) [Design: 0.4 mm (16 mils)]
- Pads: 1.05 mm (41 mils)
- The above values are real drill sizes, they add 0.1 mm (4 mils) to plated holes (PTH)

Via: 0.8/0.4 mm (31/16 mils)

- By design rules: 0.4/0.3 mm (16/12 mils)
- Micro via: yes [0.2/0.1 mm (8/4 mils)]
- Buried/blind via: yes
- Total: 40 (thru: 40 buried/blind: 0 micro: 0)

Outer Annular Ring: 0.15 mm (6 mils)

- By design rules: 0.28 mm (11 mils)

Eurocircuits class: 6B - Using min drill 0.5 mm for an OAR of 0.15 mm

General stats

Components count: (SMD/THT)

- Top: 25/5 (SMD + THT)

- Bottom: 0/0 (NONE)

Defined tracks:

- 0.15 mm (6 mils)
- 0.2 mm (8 mils)
- 0.25 mm (10 mils)
- 0.38 mm (15 mils)
- 0.51 mm (20 mils)
- 0.76 mm (30 mils)

Used tracks:

- 0.38 mm (15 mils) (78) defined: yes
- 0.51 mm (20 mils) (212) defined: yes

Defined vias:

Used vias:

- 0.8/0.4 mm (31/16 mils) (Count: 40, Aspect: 2.0 A) defined: no

Holes (excluding vias):

- 0.95 mm (37 mils) (4)
- 1.0 mm (39 mils) (21)
- 2.0 mm (79 mils) (1)
- 2.3 mm (91 mils) (2)
- 2.7 mm (106 mils) (4)

Oval holes:

- 1.5x2.0 mm (59x79 mils) (1)

Drill tools (including vias and computing adjusts and rounding):

- 0.5 mm (20 mils) (40)
- 1.05 mm (41 mils) (4)
- 1.1 mm (43 mils) (21)
- 1.5 mm (59 mils) (1)
- 2.0 mm (79 mils) (1)
- 2.4 mm (94 mils) (2)
- 2.7 mm (106 mils) (4)

Solder paste stats:

Using a paste with 87.75 % alloy, that has an specific gravity for the alloy of 7.4 g/cm^3 and 1.0 g/cm^3 for the flux. This paste has an specific gravity of 4.15 g/cm^3.

The stencil thickness is 0.12 mm.

Side	Pads with paste	Area [mm²]	Paste [g]
Total	82	138.11	0.69

Note: this is just an approximation to the theoretical value. Margins of the solder mask and waste aren't computed.

Schematic

Schematic in SVG format

PCB Layers

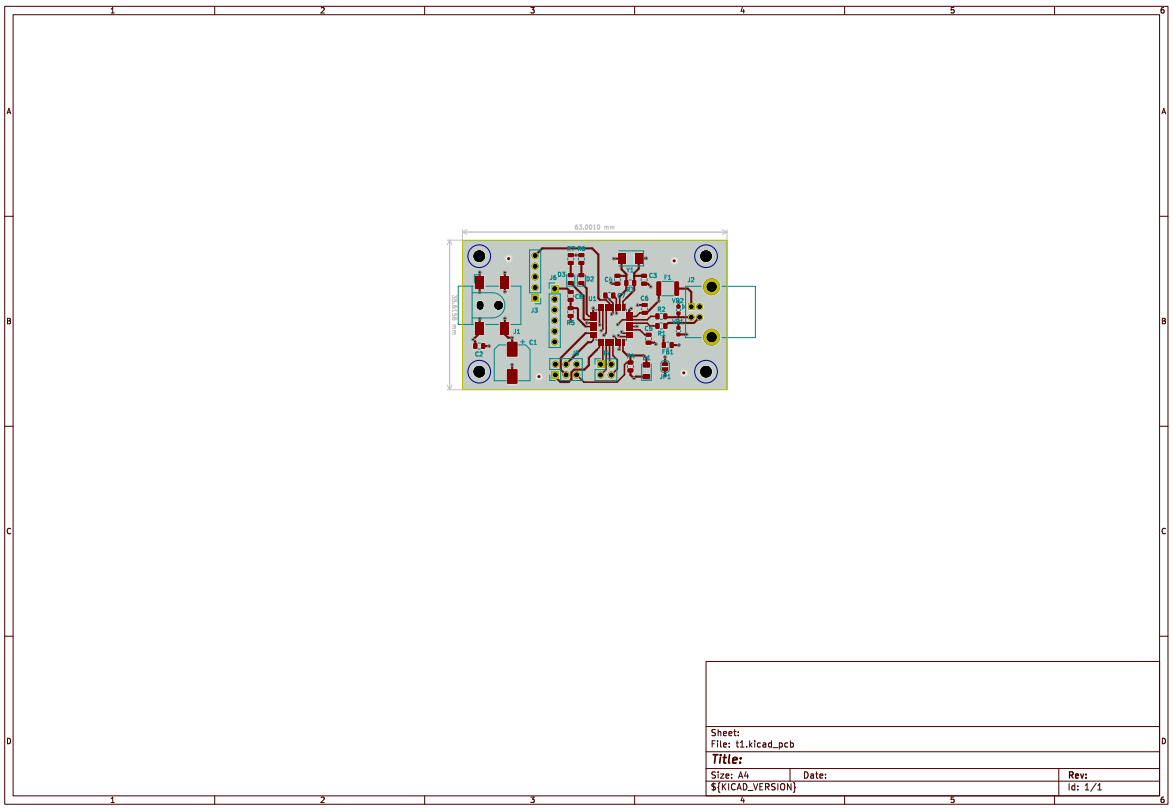

Figure 1: PCB Front copper

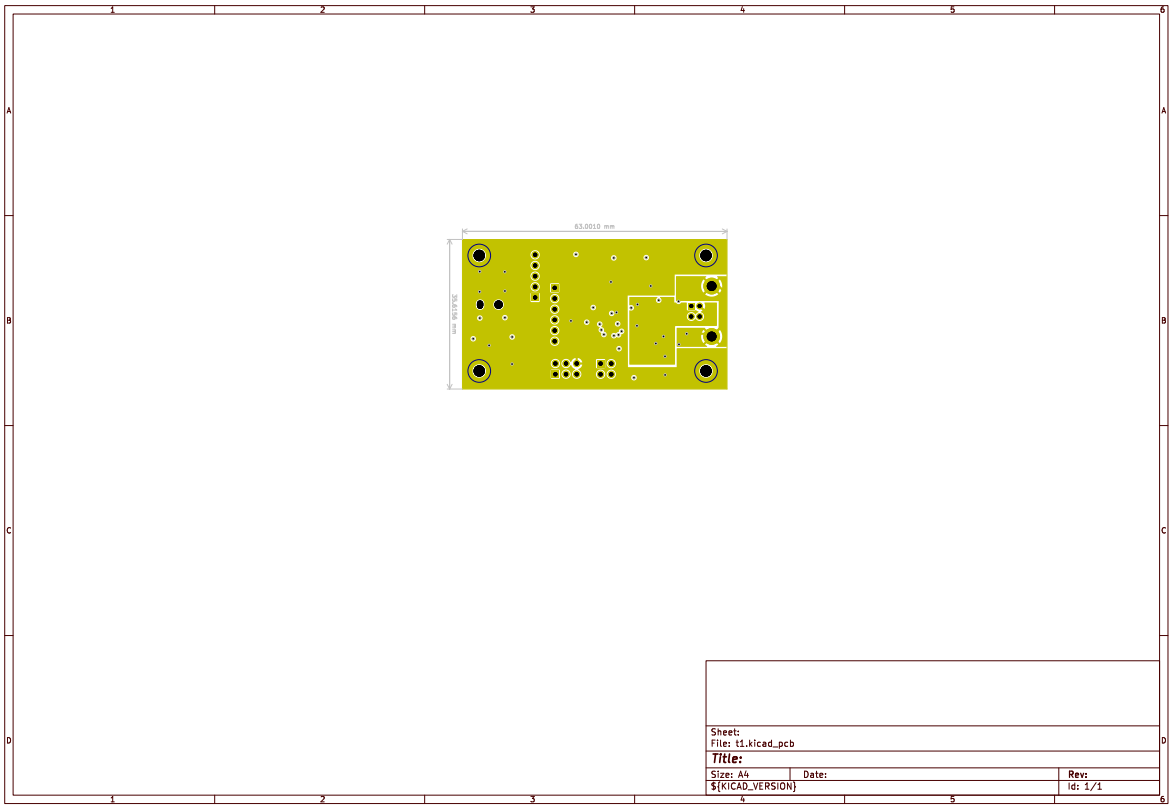

Figure 2: PCB No description

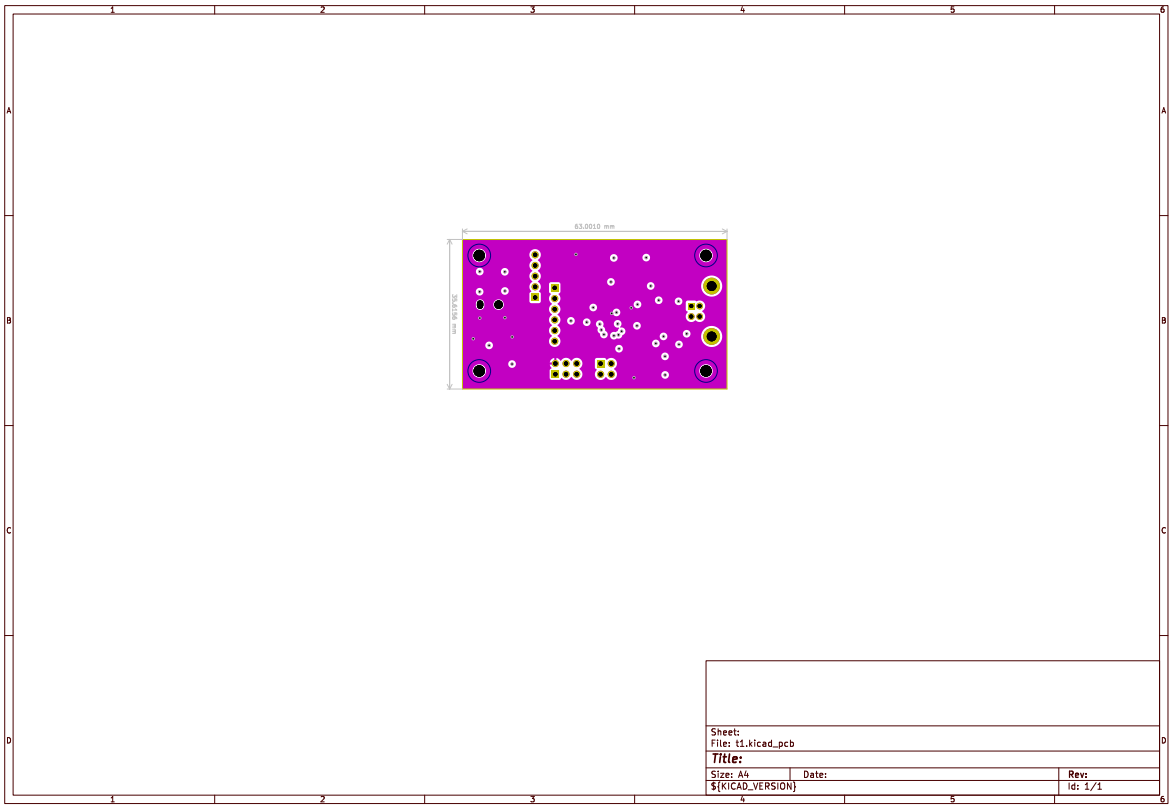

Figure 3: PCB No description

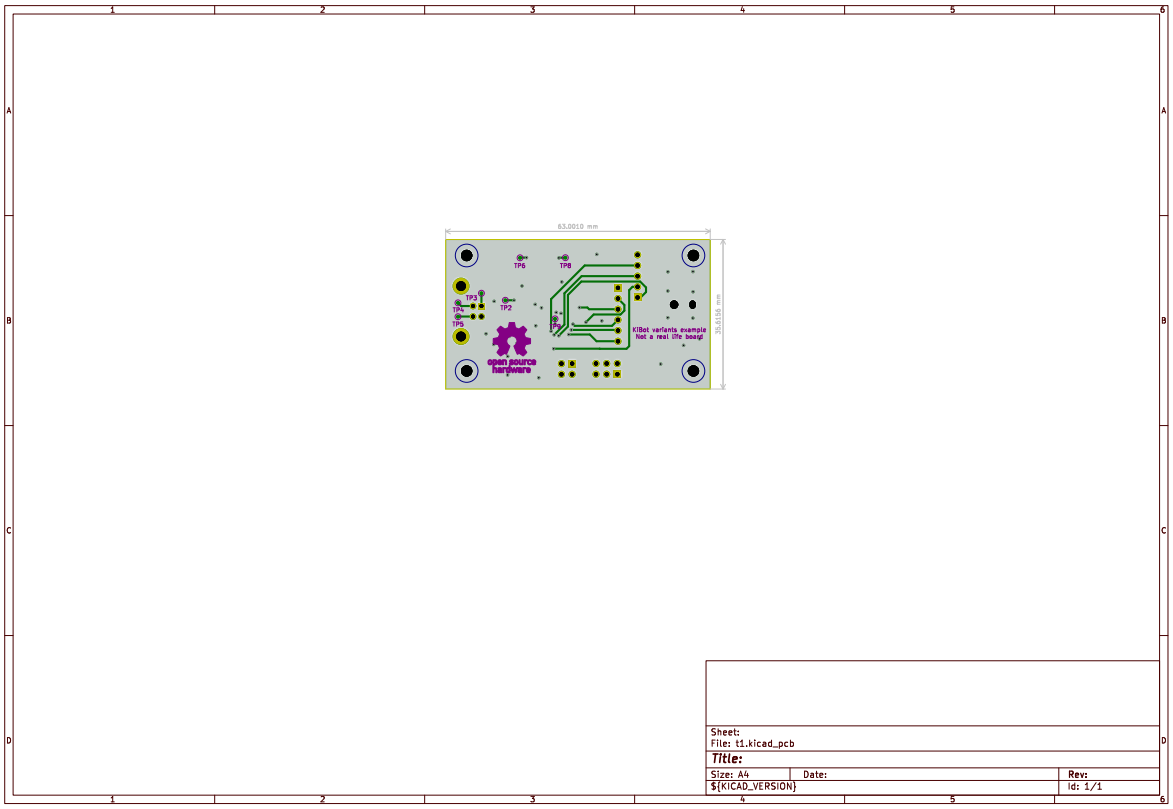

Figure 4: PCB Bottom copper

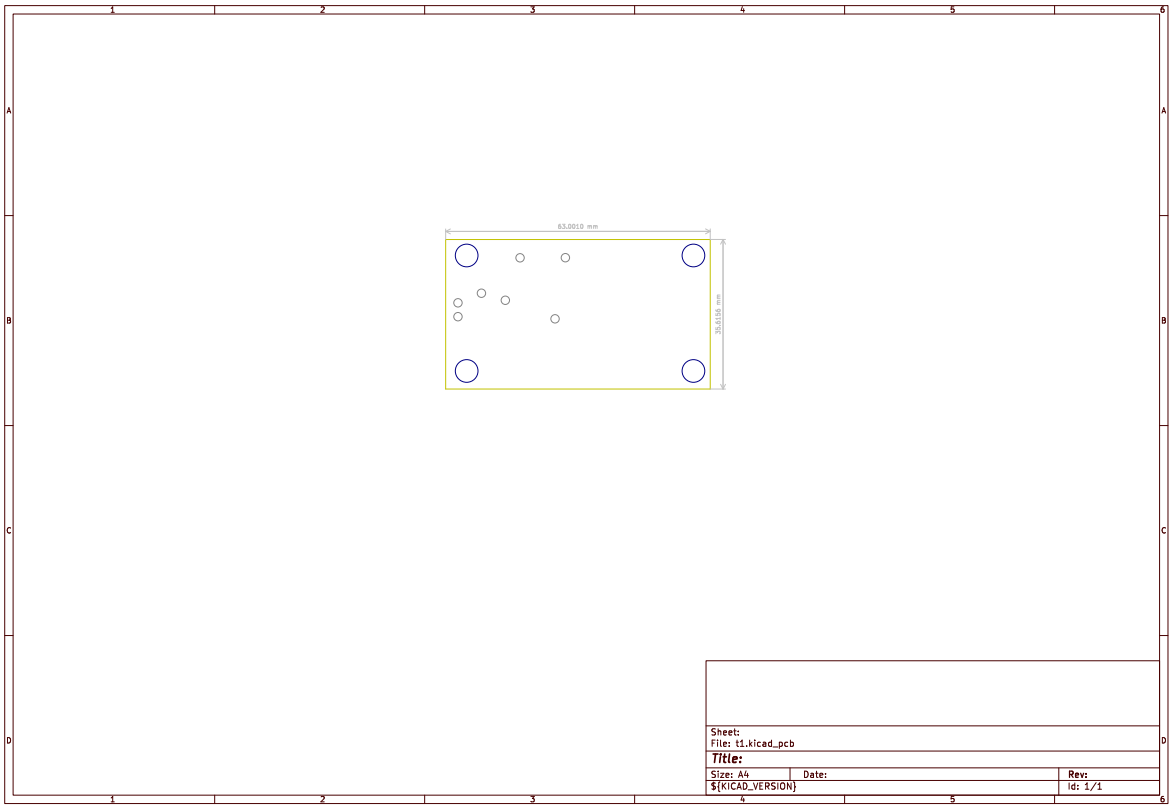

Figure 5: PCB Bottom courtyard area

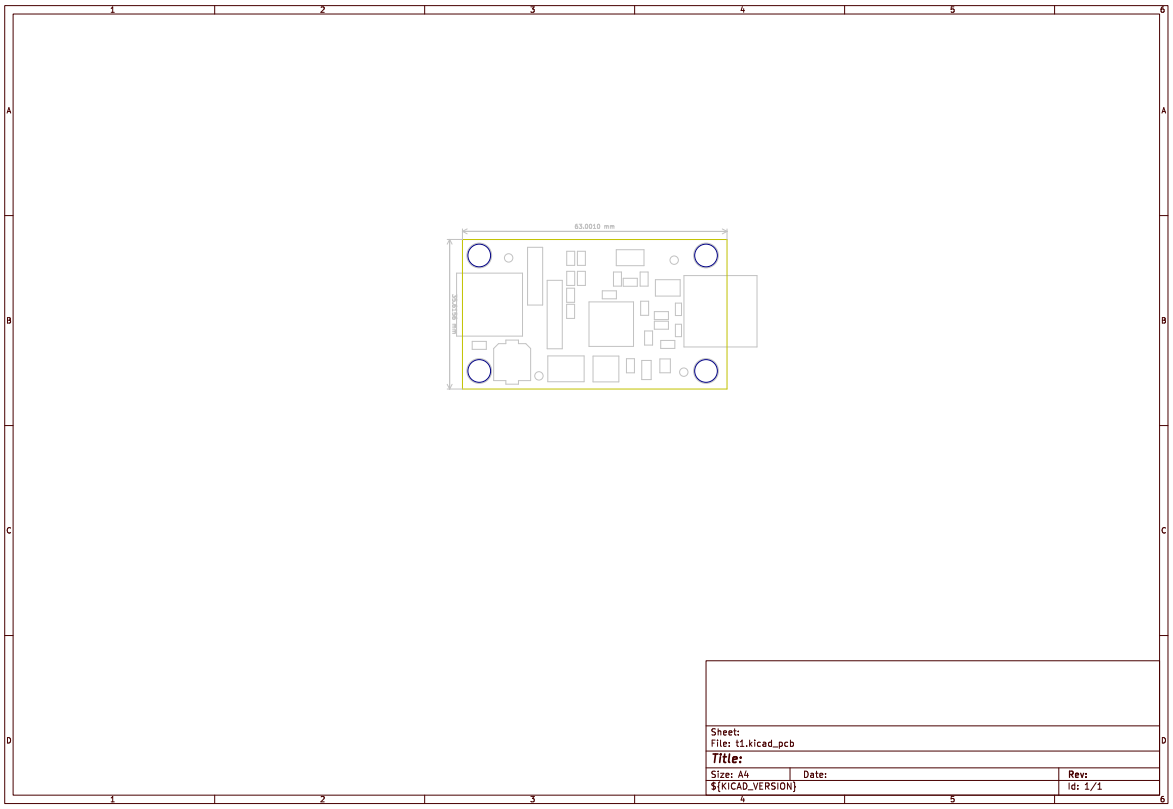

Figure 6: PCB Front courtyard area

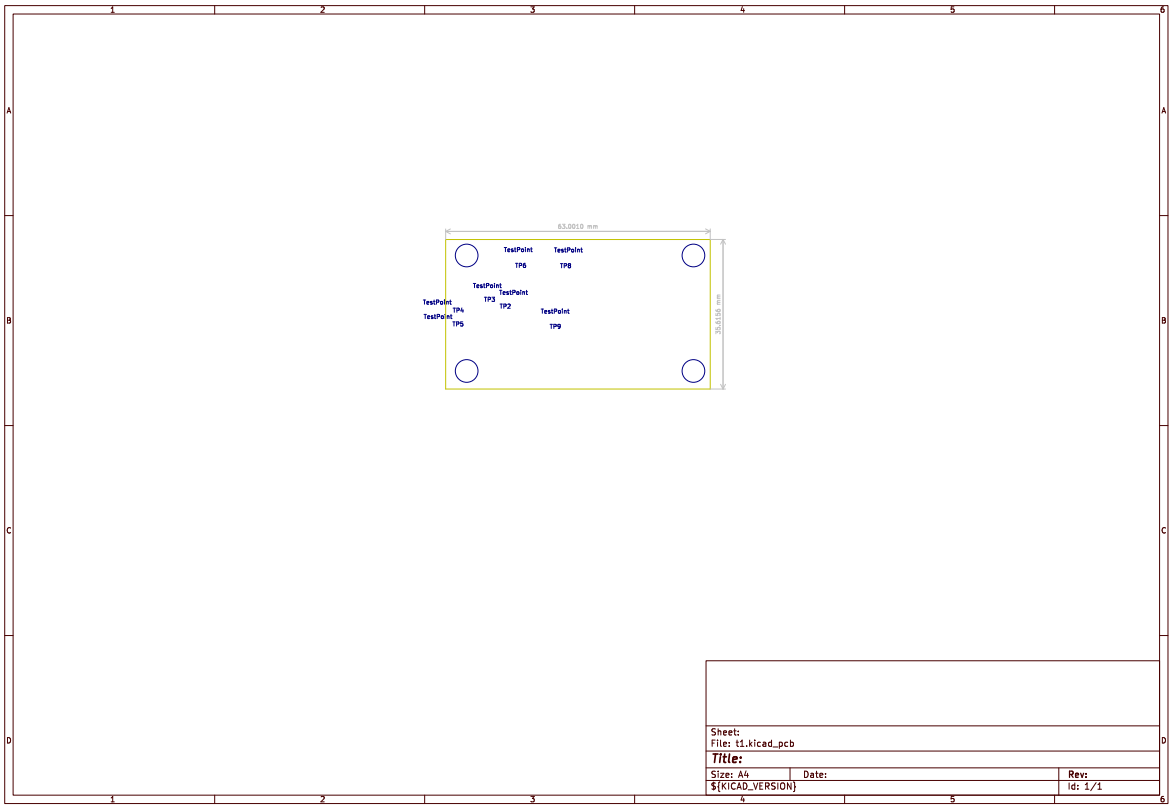

Figure 7: PCB Bottom documentation

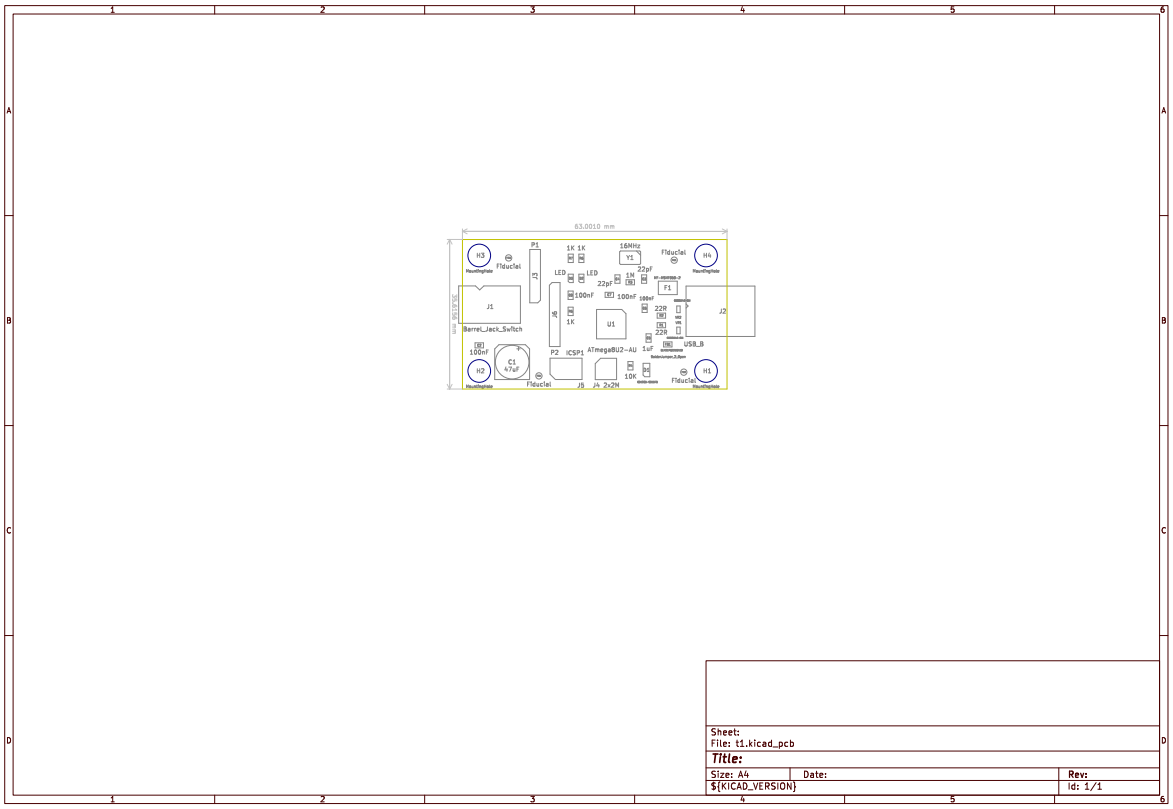

Figure 8: PCB Front documentation