

Test KDT example Fabrication Document

Layer Stack Legend

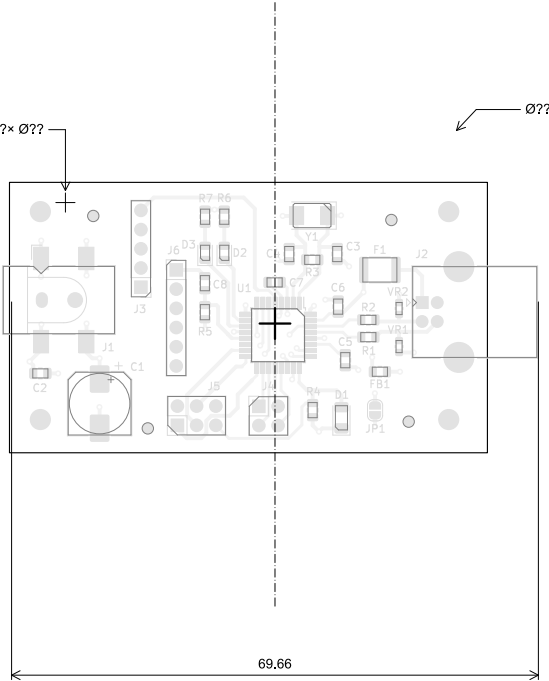
	Material	Layer	Thickness	Dielectric	Type	Gerber
	F,Paste				Paste Mask	
	F,Silkscreen				Legend	GBR
	F,Mask		0,02mm	Solder Resist	Solder Mask	GBR
	Copper	L1 (Sig, PWR)	0,07mm (2,00oz)		Signal	GBR
	Prepreg		0,18mm	FR4_7628	Dielectric	
	Copper	L2 (GND)	0,035mm (1,00oz)		Plane	GBR
	Core		0,4mm	FR4	Dielectric	
	Copper	L3 (Sig, PWR)	0,035mm (1,00oz)		Signal	GBR
	Prepreg		0,18mm	FR4_7628	Dielectric	
	Copper	L4 (Sig, PWR)	0,035mm (1,00oz)		Signal	GBR
	Core		0,4mm	FR4	Dielectric	
	Copper	L5 (GND)	0,035mm (1,00oz)		Plane	GBR
	Prepreg		0,18mm	FR4_7628	Dielectric	
	Copper	L6 (Sig, PWR)	0,07mm (2,00oz)		Signal	GBR
	B,Mask		0,02mm	Solder Resist	Solder Mask	GBR
	B,Silkscreen				Legend	GBR
	B,Paste				Paste Mask	

Total thickness: 1,66mm
Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0,2032	0,28	L2

Top Fabrication (Scale 1:1)



FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 4) SURFACE FINISH: IMMERSION GOLD
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR BLACK.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING YELLOW NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:

A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.

B. Tg 170 C OR EQUIVALENT.

C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY INTI.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE63.200 × 35.760 mm

BOARD THICKNESS1.660 mm

TRACE WIDTH0.381 mm

TRACE TO TRACE0.200 mm

MIN. HOLE (PTH)0.400 mm

MIN. HOLE (NPTH)1.500 mm

ANNULAR RING0.200 mm

COPPER TO HOLE0.254 mm

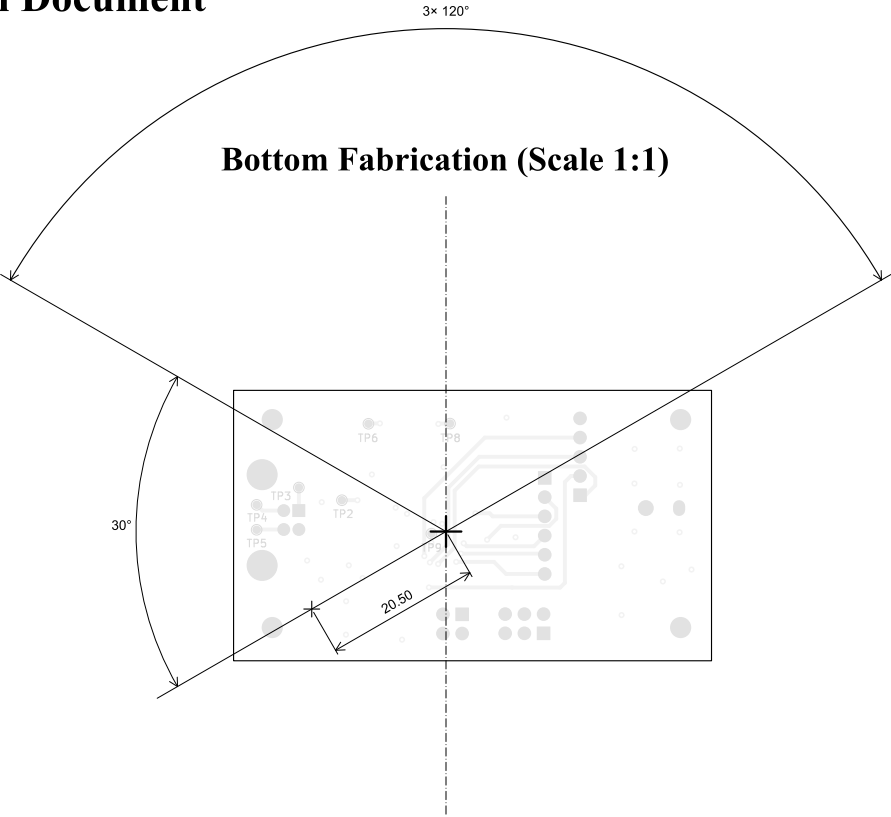
COPPER TO EDGE0.250 mm

HOLE TO HOLE0.254 mm
- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

All dimensions are in millimeters unless otherwise specified.

	Comments:	Company: INTI	Variant: RELEASED	Git Hash: df07eff
		Board Name: Test KDT example	Project Name: Test KDT	
	Sheet Title: Top Fabrication (Scale 1:1)	File Name: KDT_Hierarchical_KiBot.kicad_pcb	Designer: SET	Date: 2024-04-13
	Sheet Path:	Reviewer:	Size: A4	Revision: 0.1.5
			Sheet: 1 of 12	

Test KDT example Fabrication Document



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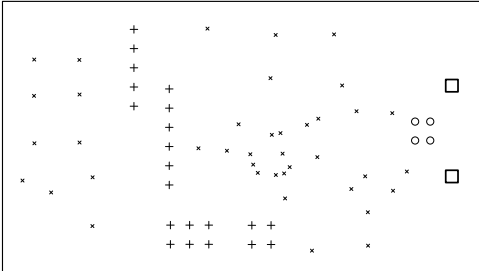
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	Sheet Title: Bottom Fabrication (Scale 1:1)	File Name: KDT_Hierarchical_KiBot.kicad_pcb	Designer: SET	Date: 2024-04-13	Revision: 0.1.5
	Sheet Path:		Reviewer:	Size: A4	Sheet: 2 of 12

Test KDT example Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	40	0,40mm (15,75mils)	PTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Via
○	4	0,95mm (37,40mils)	PTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Pad
+	21	1,00mm (39,37mils)	PTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Pad
□	2	2,30mm (90,55mils)	PTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Pad
Total 67						

Drill Drawing L1 - L6 (Scale 1:1)



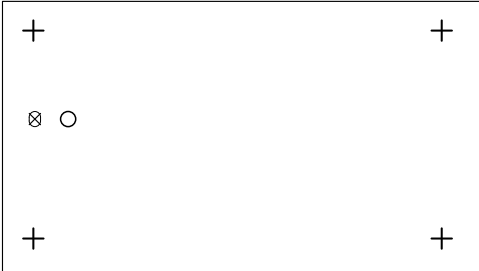
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	Sheet Path:		Reviewer:	Size: A4	Sheet: 3 of 12

Test KDT example Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
X	1	1,50mm (59,06mils)	NPTH	Slot	L1 (Slg, PWR) - L6 (Slg, PWR)	Mechanical
O	1	2,00mm (78,74mils)	NPTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Mechanical
+	4	2,70mm (106,30mils)	NPTH	Round	L1 (Slg, PWR) - L6 (Slg, PWR)	Mechanical
	Total 6					

Drill Drawing L1 - L6 (Scale 1:1)



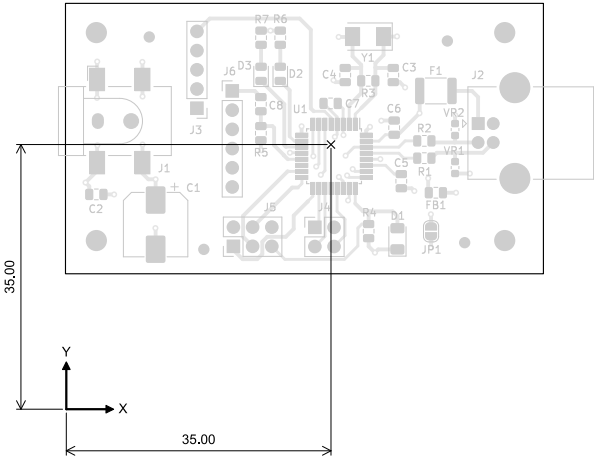
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		File Name: KDT_Hierarchical_KiBot.kicad_pcb	Designer: SET	Date: 2024-04-13	Revision: 0.1.5
	Sheet Path:		Reviewer:	Size: A4	Sheet: 4 of 12

Test KDT example Fabrication Document

Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
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Ref.	Net	X [mm]	Y [mm]
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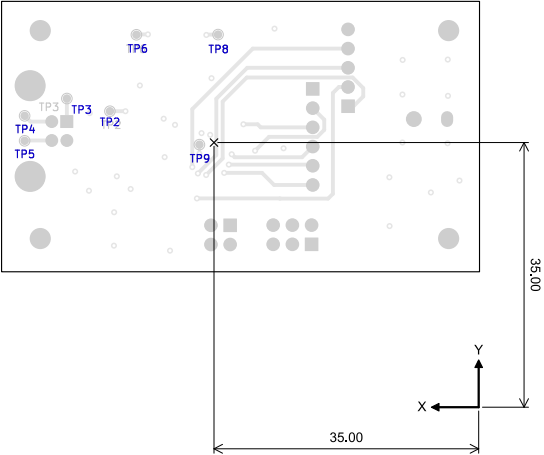
All dimensions are in millimeters unless otherwise specified.

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	Sheet Path:		Reviewer:	Size: A4	Sheet: 5 of 12

Test KDT example Fabrication Document

Bottom Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
TP2	VBUS	98.27	20.14
TP3	Net-(J2-VBUS)	103.96	21.82
TP4	Earth	109.54	19.53
TP5	Net-(J2-D+)	109.54	16.23
TP6	Net-(U1-XTAL1)	94.76	30.25
TP8	Net-(U1-PC0/XTAL2)	83.97	30.28
TP9	Net-(U1-D-)	86.43	15.72

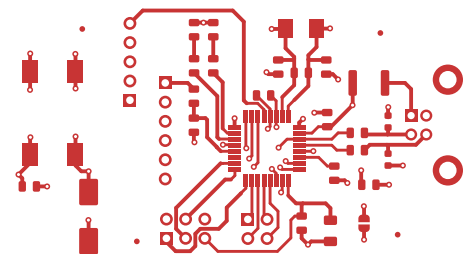


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	Sheet Path:		Reviewer:	Size: A4	Sheet: 6 of 12

Test KDT example Fabrication Document

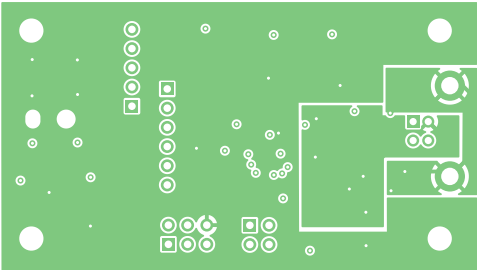
L1 (Sig, PWR) (Scale 1:1)



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	L1 (Sig, PWR) (Scale 1:1)	File Name:	Designer:	Date:	Revision:
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	Sheet Path:		Reviewer:	Size:	Sheet:
				A4	7 of 12

Test KDT example Fabrication Document

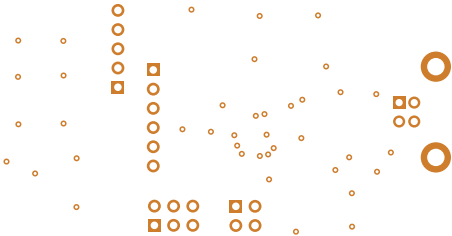
L2 (GND) (Scale 1:1)



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				A4	8 of 12

Test KDT example Fabrication Document

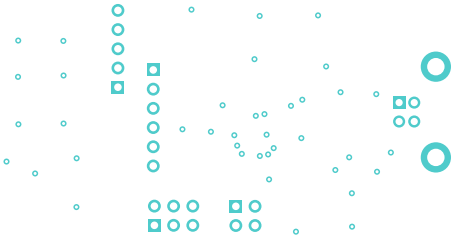
L3 (Sig, PWR) (Scale 1:1)



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	L3 (Sig, PWR) (Scale 1:1)	File Name:	Designer:	Date:	Revision:
	Sheet Path:	Reviewer:	Size:	Sheet:	
				A4	9 of 12

Test KDT example Fabrication Document

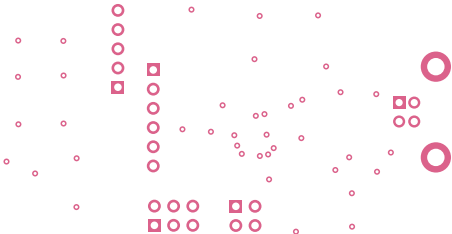
L4 (Sig, PWR) (Scale 1:1)



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				A4	10 of 12

Test KDT example Fabrication Document

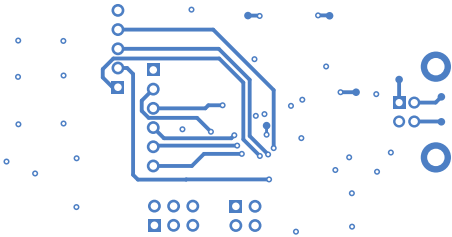
L5 (GND) (Scale 1:1)



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	L5 (GND) (Scale 1:1)	File Name:	Designer:	Date:	Revision:
	Sheet Path:	Reviewer:	Size:	Sheet:	
			A4	11 of 12	

Test KDT example Fabrication Document

L6 (Sig, PWR) (Scale 1:1)



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		Board Name: Test KDT example		Project Name: Test KDT	
	Sheet Title: L6 (Sig, PWR) (Scale 1:1)	File Name: KDT_Hierarchical_KiBot.kicad_pcb	Designer: SET	Date: 2024-04-13	Revision: 0.1.5
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