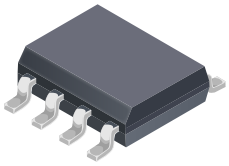
ACS711

Hall-Effect Linear Current Sensor with Overcurrent Fault Output for <100 V Isolation Applications

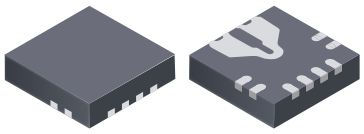
FEATURES AND BENEFITS

- No external sense resistor required; single package solution
- Reduced power loss:
  - □ 0.6 mΩ internal conductor resistance on EX package
  - □ 1.2 mΩ internal conductor resistance on LC package
- Economical low- and high-side current sensing
- Output voltage proportional to AC or DC currents
- ±12.5 A and ±25 A full-scale sensing ranges on LC package
- ±15.5 A and ±31 A full-scale sensing ranges on EX package
- Overcurrent $\overline{\text{FAULT}}$ trips and latches at 100% of full-scale current
- Low-noise analog signal path
- 100 kHz bandwidth
- Small footprint, low-profile SOIC8 and QFN packages
- 3 to 5.5 V single supply operation
- Integrated electrostatic shield for output stability
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Zero magnetic hysteresis
- Ratiometric output from supply voltage

PACKAGES:



8-pin SOICN
with internally fused path
(LC package)



12-contact QFN
3 mm × 3 mm × 0.75 mm
(EX package)

Not to scale

DESCRIPTION

The Allegro™ ACS711 provides economical and precise solutions for AC or DC current sensing in <100 V audio, communications systems, and white goods. The device package allows for easy implementation by the customer. Typical applications include circuit protection, current monitoring, and motor and inverter control.

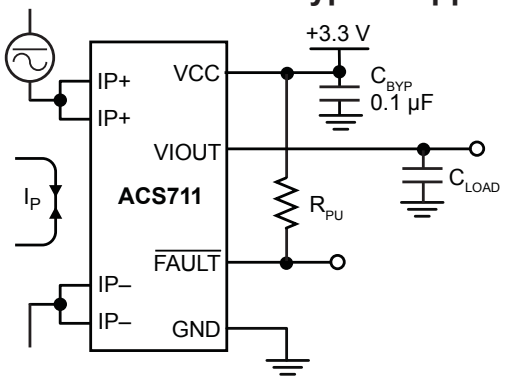
The device consists of a linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer.

The output of the device has a positive slope proportional to the current flow from IP+ to IP– (pins 1 and 2, to pins 3 and 4). The internal resistance of this conductive path is 0.6 mΩ for the EX package, and 1.2 mΩ for the LC package, providing a non-intrusive measurement interface that saves power in applications that require energy efficiency.

The ACS711 is optimized for low-side current sensing applications, although the terminals of the conductive path are electrically isolated from the sensor IC leads, providing sufficient internal creepage and clearance dimensions for a low AC or DC working voltage applications. The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions.

The ACS711 is provided in small, surface-mount packages: SOIC8 and QFN12. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Typical Application

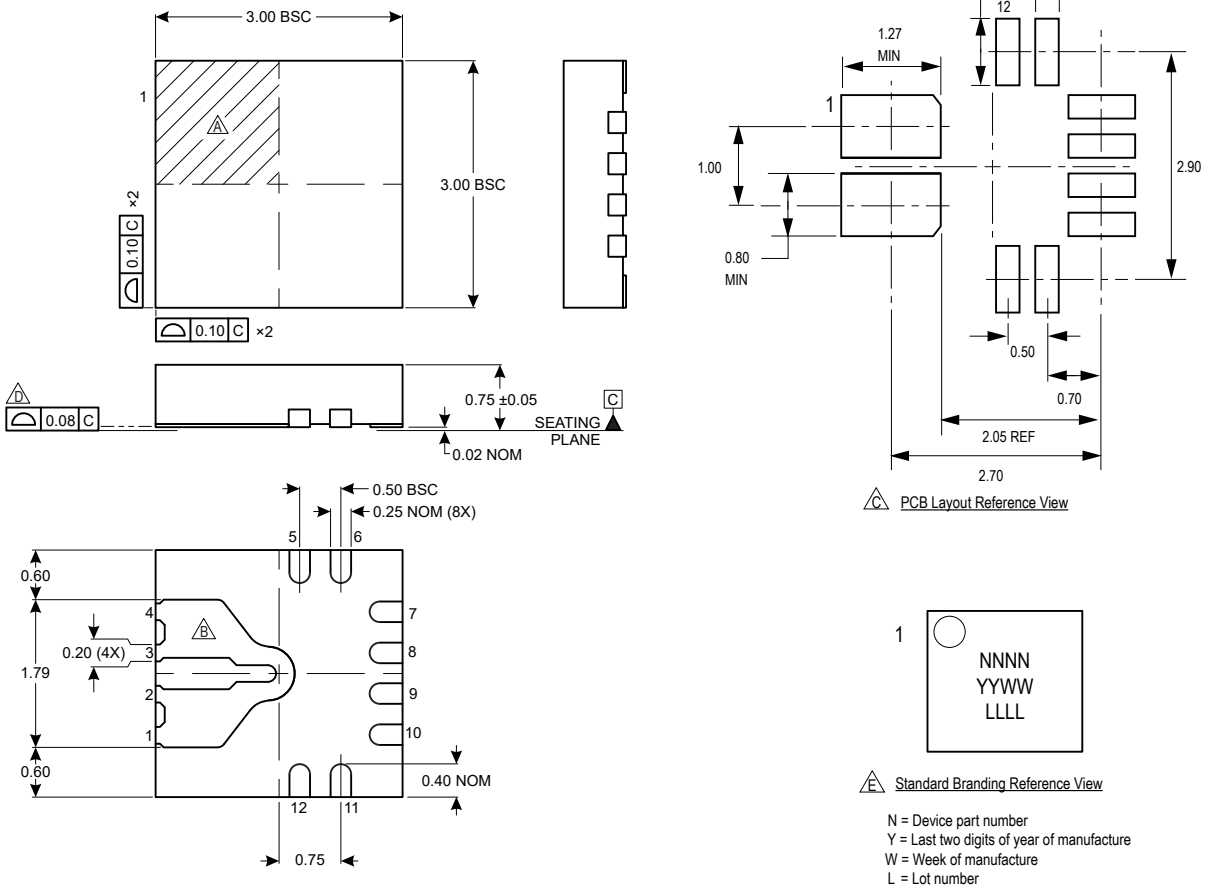


Application 1. The ACS711 outputs an analog signal, V_{IOUT}, that varies linearly with the bi-directional AC or DC primary current, I_P, within the range specified. The $\overline{\text{FAULT}}$ pin trips when I_P reaches ±100% of its full-scale current.

Package EX, 12-Contact QFN
With Fused Sensed Current Loop

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000382, Rev. 2)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

A Terminal #1 mark area

B Fused sensed current path

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed current path and terminals

E Branding scale and appearance at supplier discretion

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