# Lab 1: Quartus Prime Tutorial

# ECE – 380


## University of Alabama

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## Introduction

The Purpose of the laboratory was to become familiar with Quartus Prime. Students created three different design entries using Schematic capture, VHDL, and Schematic entry at the top level.

## Procedure

a) We went through tutorials about quartus prime to make ourselves familiar with the software before getting into the lab.
b) We followed the lab #1 instruction manual using debugging techniques as posted by the Professor.
c) After each successful build we started compilation and showed the demo to the TA

## Results

The first two test cases showed similar wavelengths, However the third one revealed a different wavelength.

Image 1:- example_schematic.bdf

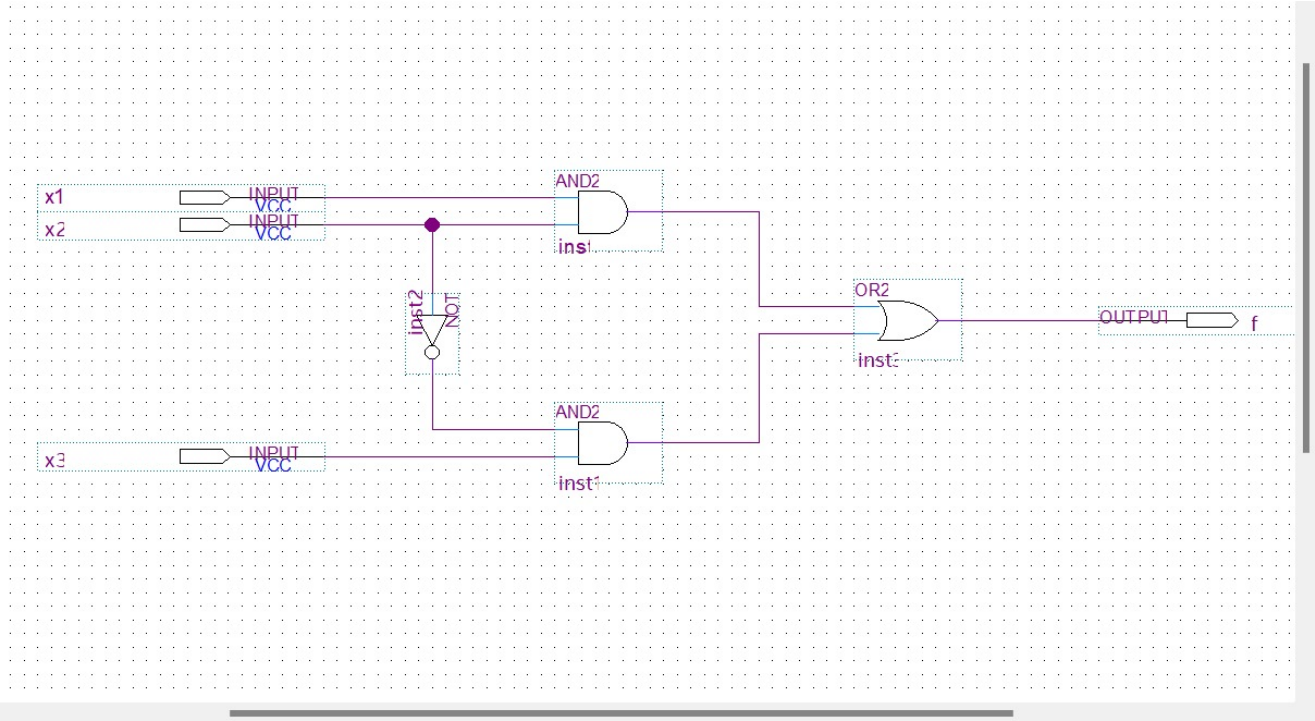



Image 2:- example_schematic.vwf

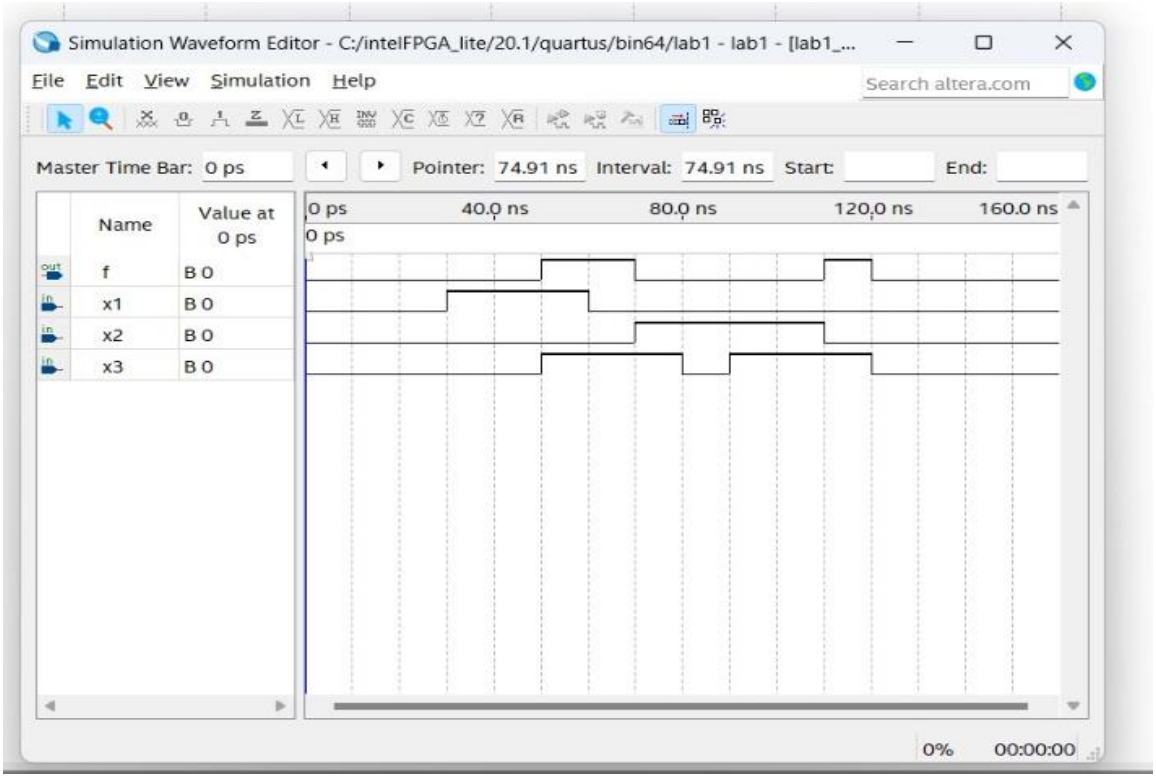


Image 3:- example_vhdl.vhd

part2_lab1.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY part2_lab1 IS
4     PORT ( x1, x2, x3 : IN  STD_LOGIC;
5            f          : OUT STD_LOGIC);
6  END part2_lab1;
7
8  ARCHITECTURE Behavior OF part2_lab1 IS
9  BEGIN
10    f <= (x1 AND x2) OR (NOT x2 and X3);
11 END Behavior;
```

Image 4:- example_vhdl.vwf

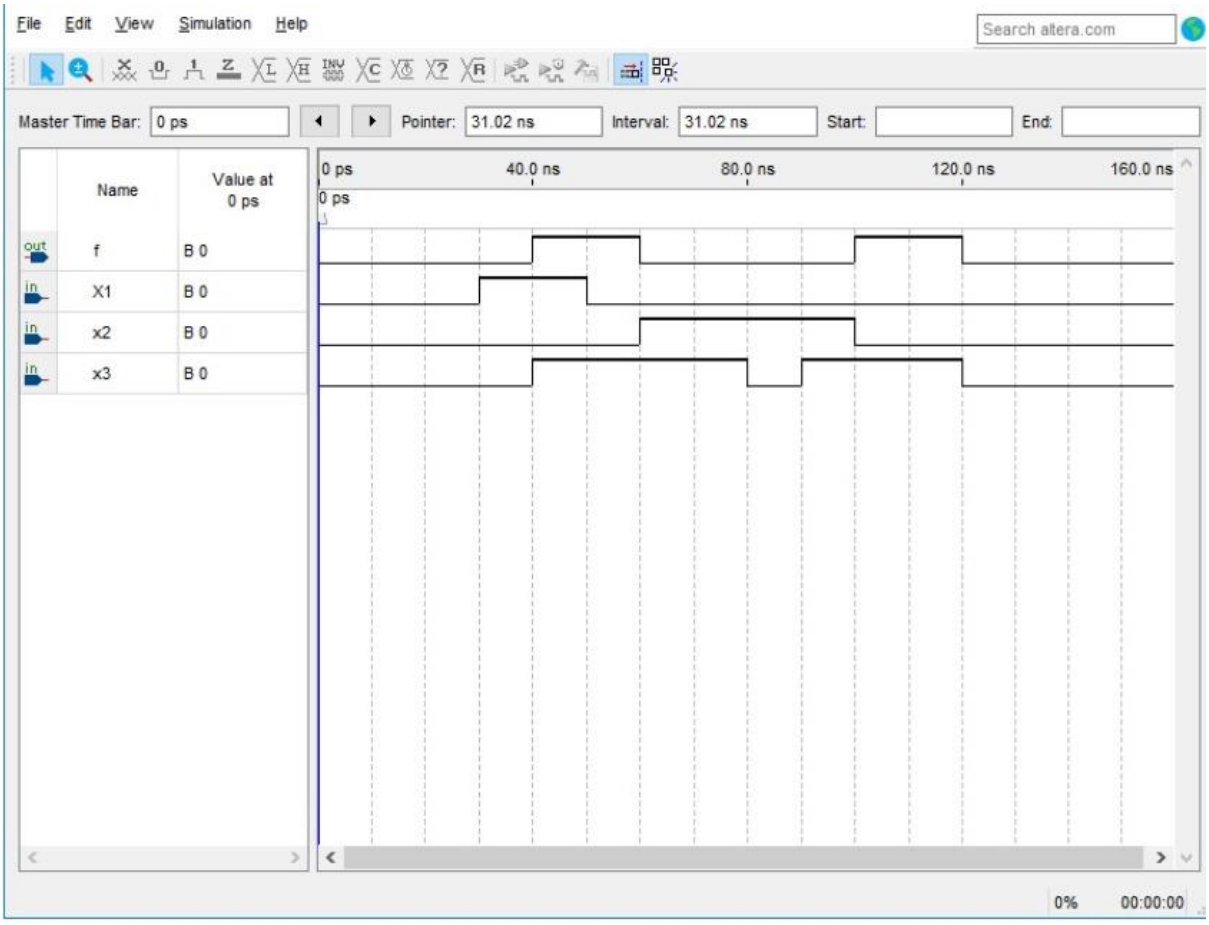


Image 5:- vhdlfunctions.vhd

```
1  ENTITY vhdlfunctions IS
2     PORT ( w1, w2, w3, w4 : IN BIT;
3            g, h           : OUT BIT);
4  END vhdlfunctions;
5
6  ARCHITECTURE LogicFunc OF vhdlfunctions IS
7  BEGIN
8     g<= (w1 AND w2) OR (w3 AND w4);
9     h<= (w1 AND w3) OR (w2 AND w4);
10  END LogicFunc;
```

Image 6:- example_mixed1.bdf

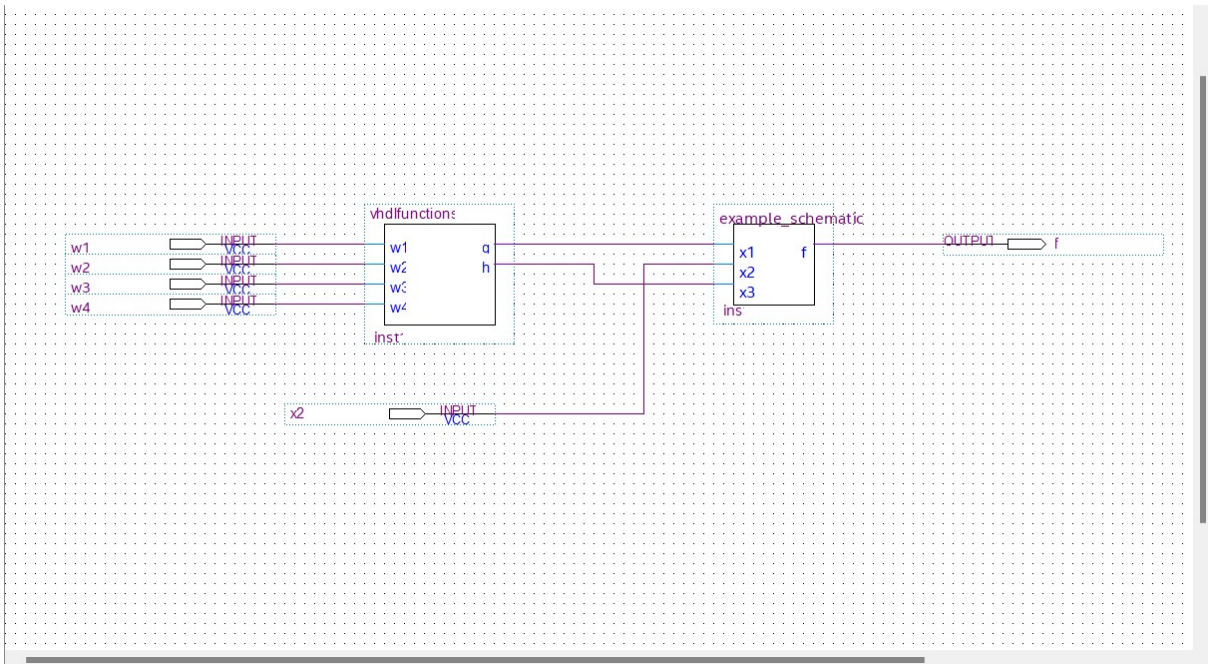


Image 7:- example_mixed1.vwf

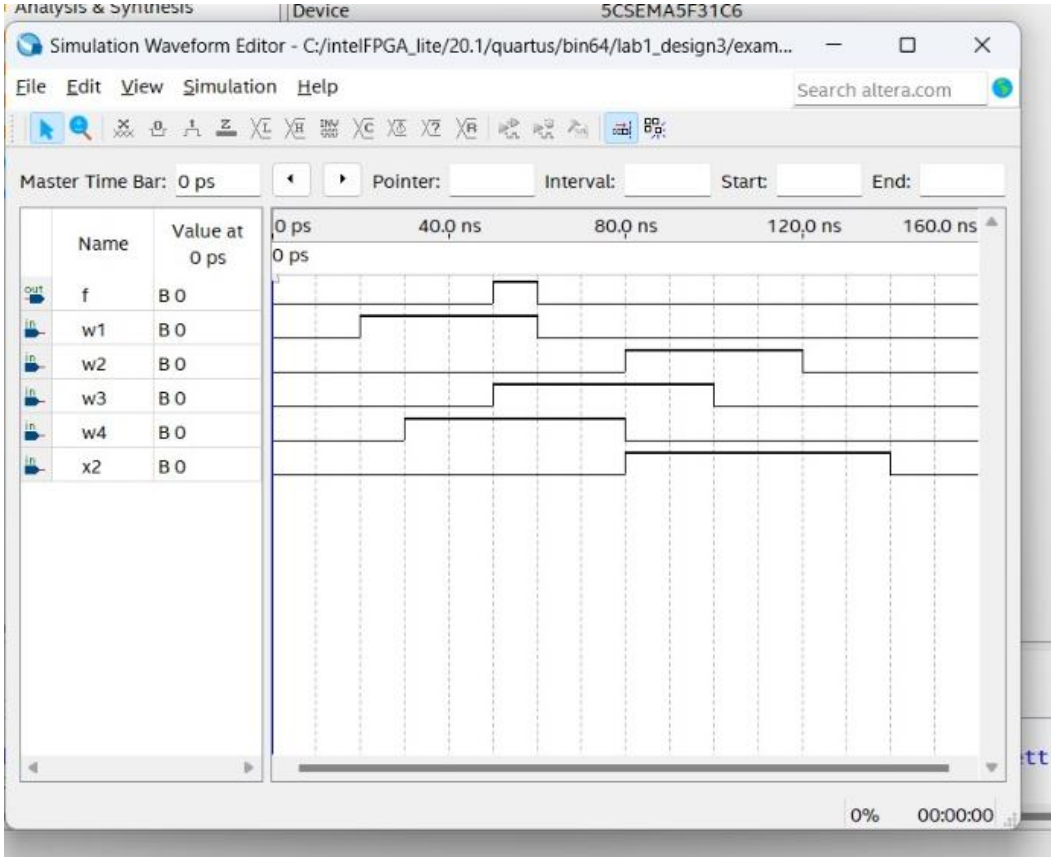
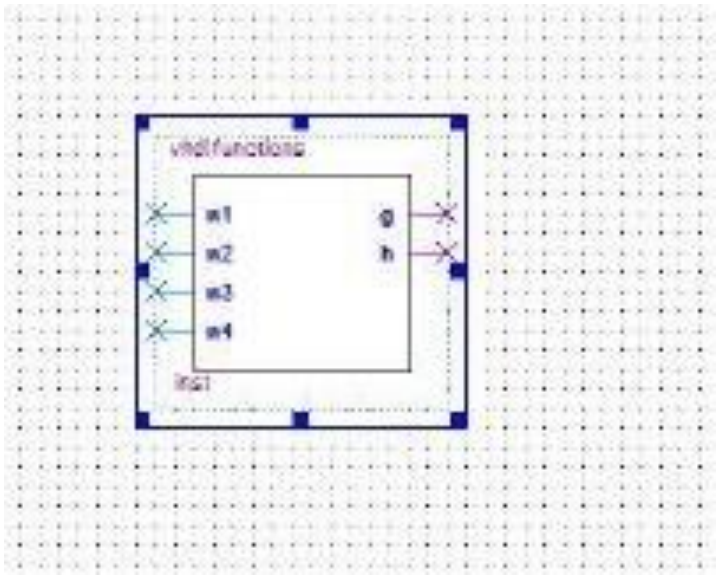



Image 8:- vhdlfunctions.bsf



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**Lab scoring sheet**

| | Score | TA Comments |
|---|---|---|
| Design 1: Schematics | 10 | Schematic/WF. |
| Design 2: VHDL | 20 | WF/ code. |
| Design 3: Schematics | 20 | Schematic/WF |
| | | |
| **Report (50 pts)** | | |
| | | |
| **Lab 1 Total Grade (100 pts)** | | |
| | | |
| **Extra 20 pts: Quartus Prime Installation (deadline: Feb 2).** | 20 | Pics |
| | | |