ECE 380 Lab 3 Report with pictures

Digital Logic (University of Alabama)

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Lab 03
ECE 380
University of Alabama

9/16/2019

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Introduction

The objective of this lab was to create a NAND circuit from a multi-functional logic diagram. The NAND circuit was implemented in VHDL code as well as a block schematic. These two circuits were then used to control an led on the Alterra DE1 circuit board. When the correct buttons were pushed on the board, the led would flash whenever the output of the circuit was one.

Procedure

a) Pre-laboratory

For the pre-lab, we used the information in figure 1 to draw a 4 variable truth table. In this truth table, the outputs of A and B depend on the inputs of C1 and C0. Once we completed the truth table, we then used a Karnaugh Map to generate the simplest SOP function. That information was then used to create NAND only circuits using the VHDL and block diagram methods.

C_1C_0	F
00	$\overline{A + B}$
01	$A \cdot B$
10	$\overline{A \oplus B}$
11	$A \oplus B$

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Figure 1

b) Setup and Data Collection

After each circuit was created, we tested it in the waveform simulator. Since there were four variables, the end time for each variable was set to 20, 40, 80, and 160 respectively. After the waveform data was determined to be correct, we then uploaded the code onto the Alterra DE1 boards and tested both circuits individually. To set up the circuits to work on the DE1 board, we utilized the pin planner and assigned each pin to its correct I.D. This information was gathered in the lab manual.

Results

For the VHDL and block diagram circuits, our waveform outputs matched the truth table exactly. When we tested the circuits on the DE1 board, the led also matched the truth table exactly.

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```
1  ENTITY Lab3Design IS
2      PORT(A, B, c1, c0: IN BIT;
3           f    : OUT BIT);
4  END Lab3Design;
5
6  ARCHITECTURE Behavior OF Lab3Design IS
7  BEGIN
8      f <= NOT( NOT (NOT c0 AND NOT A AND NOT B) AND NOT(c1 AND c0 AND NOT A AND B) AND NOT(NOT c1 AND c0 AND A AND B) AND NOT ( c1 AND NOT c0 AND A AND B)
9      END Behavior;
```

Figure 2 Screen Shot of VHDL code of NAND gate

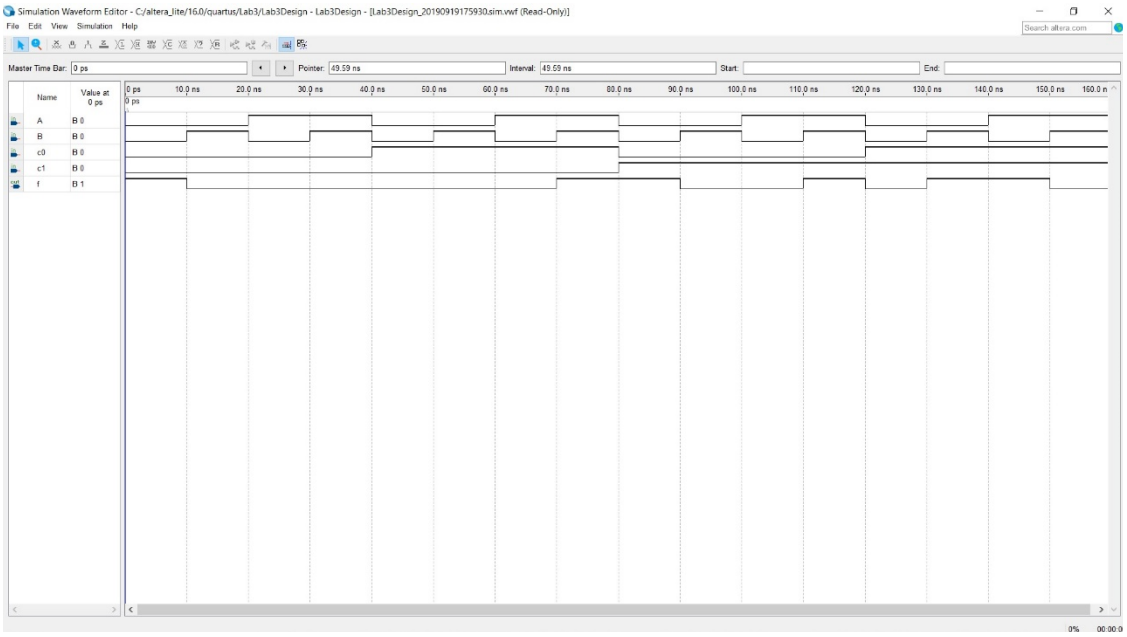

Figure 3 Waveform of VHDL NAND gate circuit

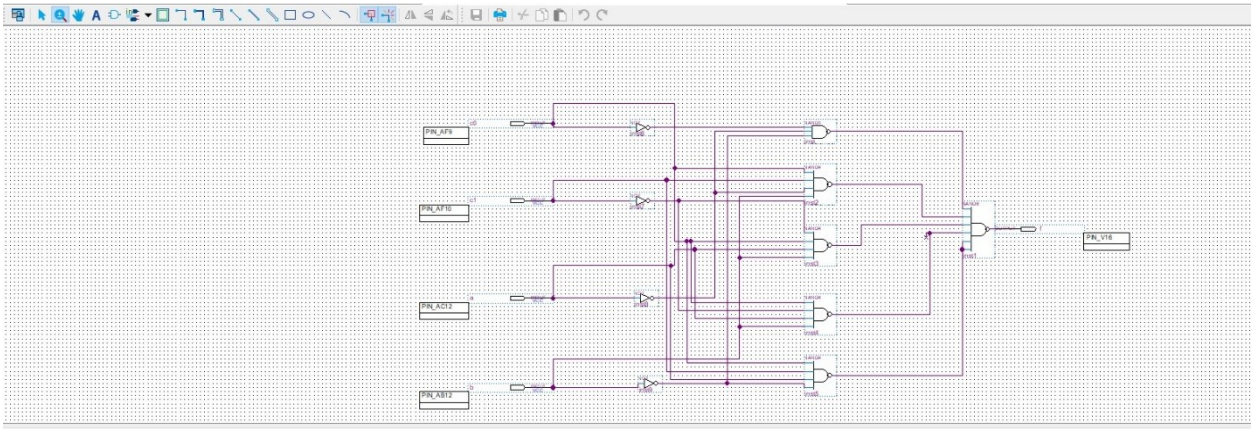

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Figure 4 Screenshot of block schematic NAND gate

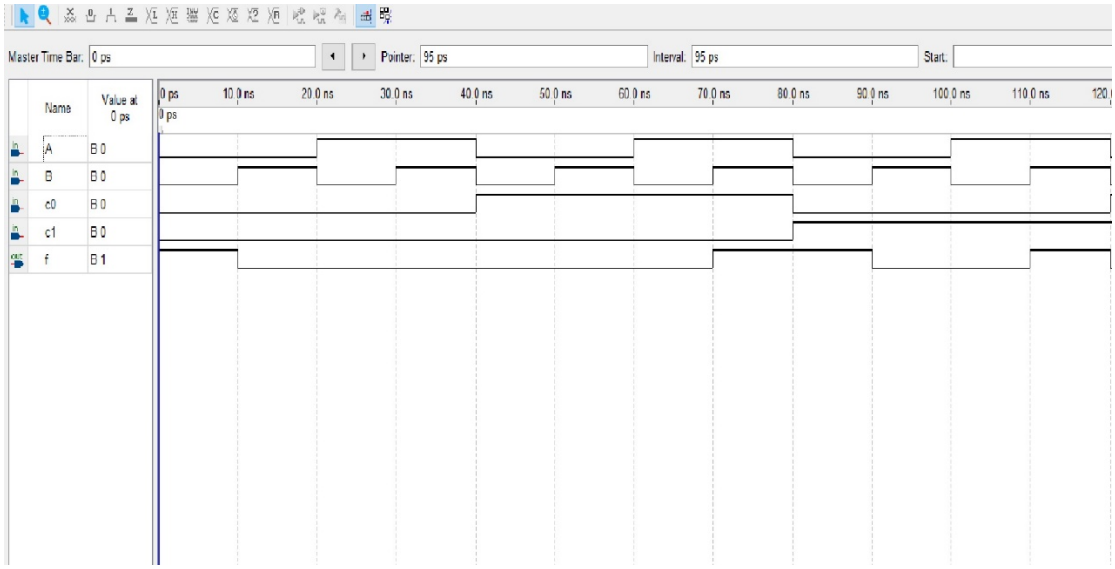

Figure 5 Screenshot of block diagram NAND gate waveform output

Conclusion

By creating the circuits and following the resources provided in the lab manual, we were able to create a multifunctional logic circuit that could produce multiple logic functions from a single output. This was demonstrated by observing the led when a single input was given.

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