Lab 04

ECE 380

The University of Alabama

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Introduction

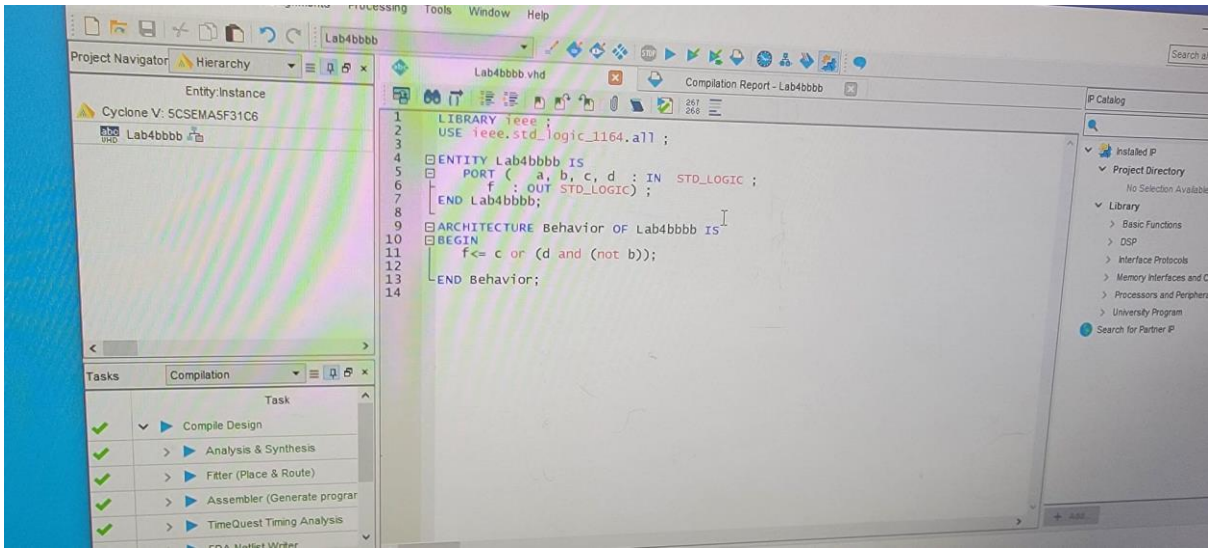
The objective of this lab was to practice optimization via Karnaugh maps and implementation via NAND-only and NOR-only gates through different tools, Quartus software, DE1 boards, and breadboards.

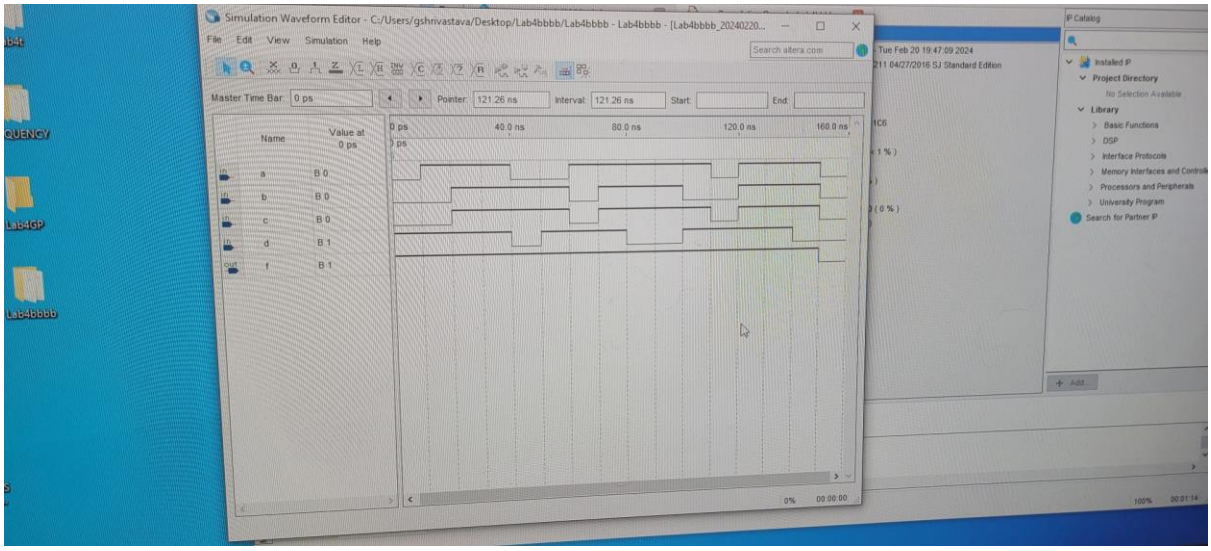
Procedure

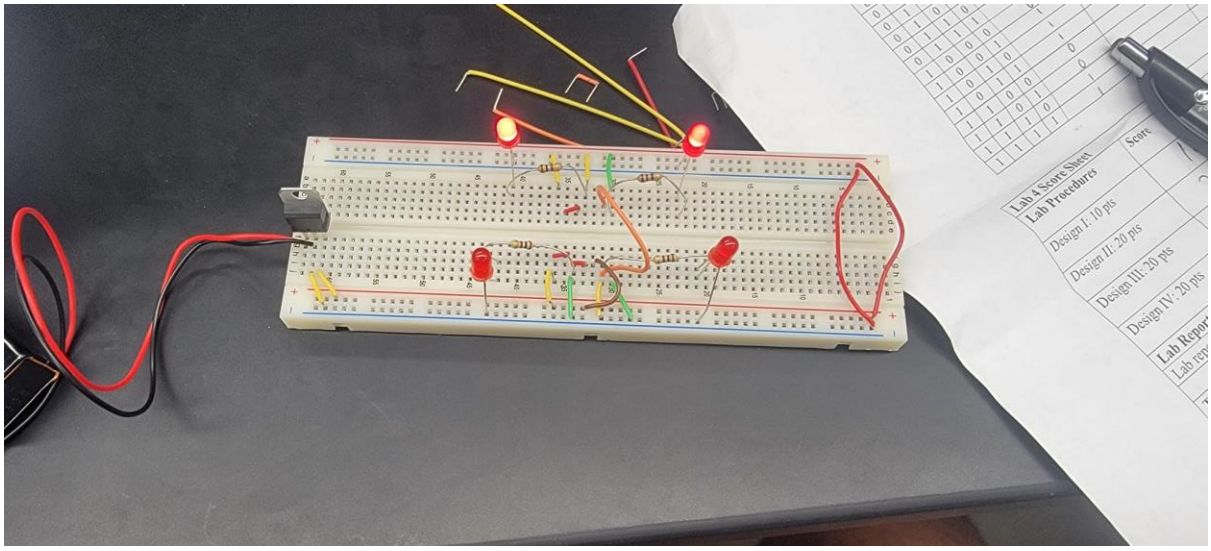
We followed the laboratory manual to practice building NAND-only and NOR-only gates. First with a VHDL implementation on Quartus Prime Software and then breadboard implementations for the same.

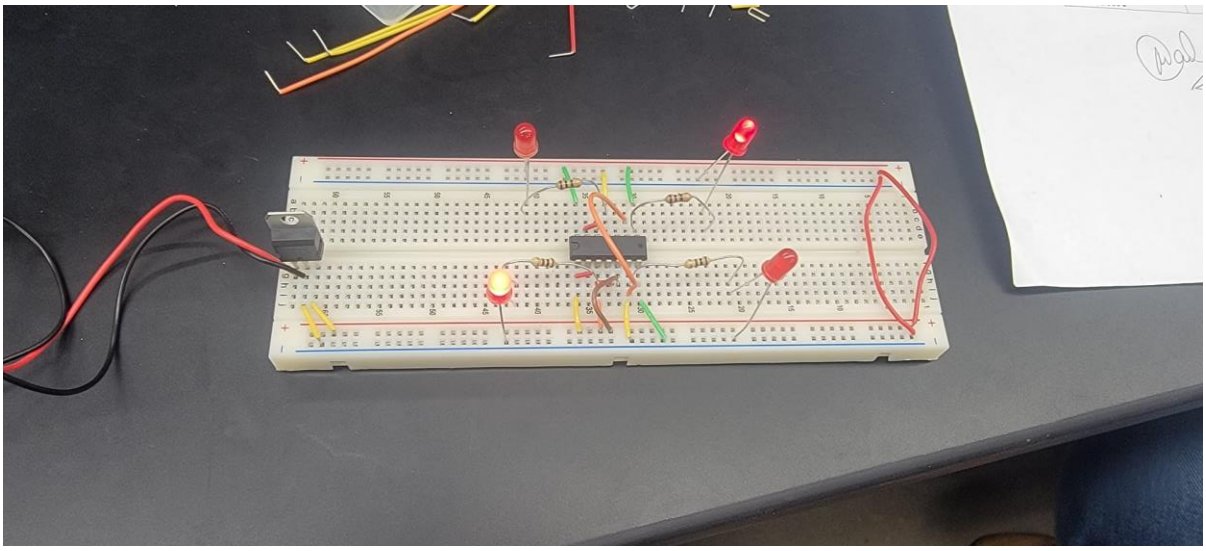
We used Karnaugh Maps to find out their logic functions and then further schematics.

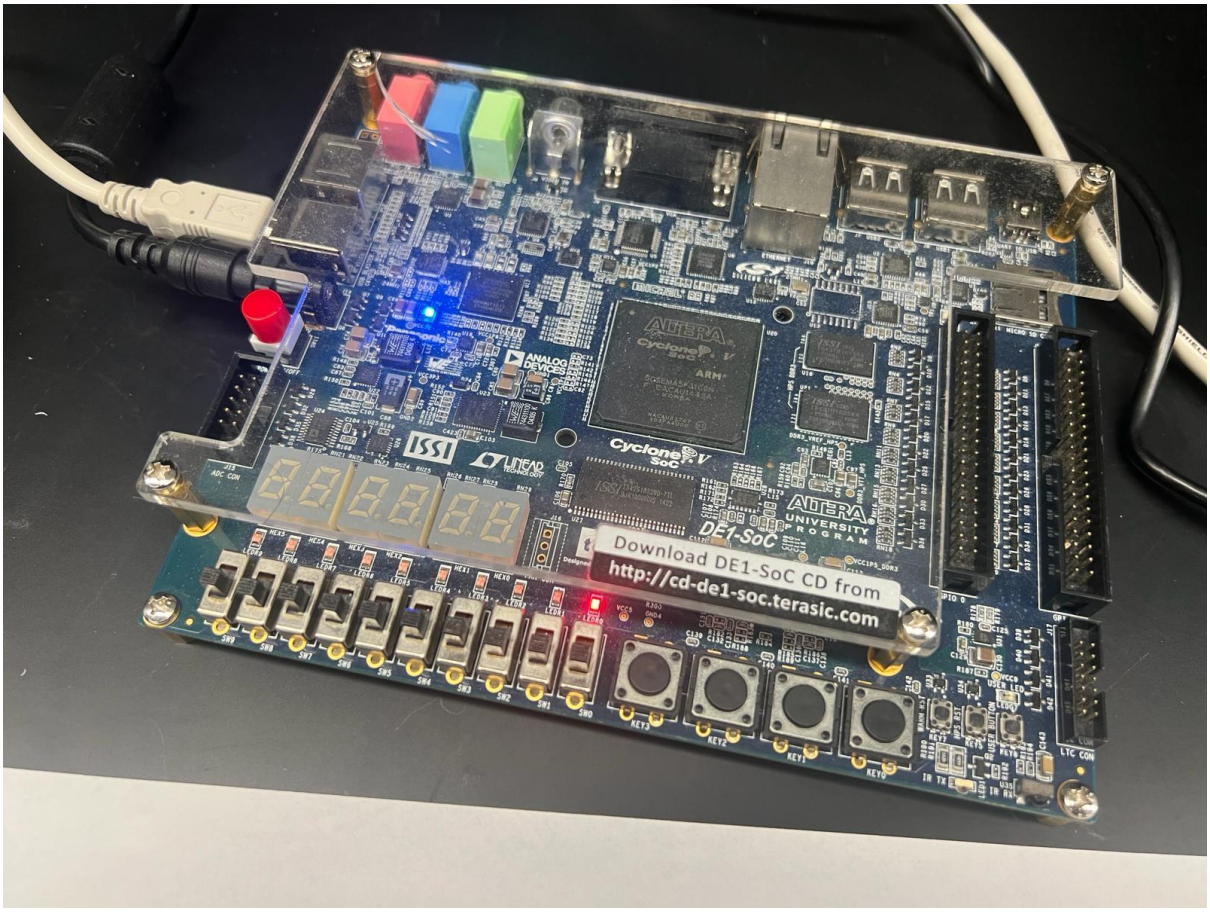
Then we followed the manual to build a flashing light pattern on the altera board.






Lab 4 Score Sheet
Score
Lab Procedures
Design I: 10 pts
Design II: 20 pts
Design III: 20 pts
Design IV: 20 pts
Lab Report




Download DE1-SoC CD from
http://cd-de1-soc.terasic.com
DE1-SoC

a	b	c	d	*Design I f(waveform)*	*Design II f(NAND-BB)*	*Design III f(NOR-BB)*
0	0	0	0	0		0
0	0	0	1	1		1
0	0	1	0	1		1
0	0	1	1	1		1
0	1	0	0	0		0
0	1	0	1	0		0
0	1	1	0	1		1
0	1	1	1	1		1
1	0	0	0	0		0
1	0	0	1	1		1
1	0	1	0	1		1
1	0	1	1	1		1
1	1	0	0	0		0
1	1	0	1	0		0
1	1	1	0	1		1
1	1	1	1	1		1

Lab 4 Score Sheet		
Lab Procedures	**Score**	**Lab TA comments/Initials**
Design I: 10 pts	10	Checked WF
Design II: 20 pts	20	Checked BB
Design III: 20 pts	20	Checked BB
Design IV: 20 pts	20	Checked BB
Lab Report		
Lab report: 30 pts		
Total Score