

**The University of Alabama
ECE 380
Lab 7**

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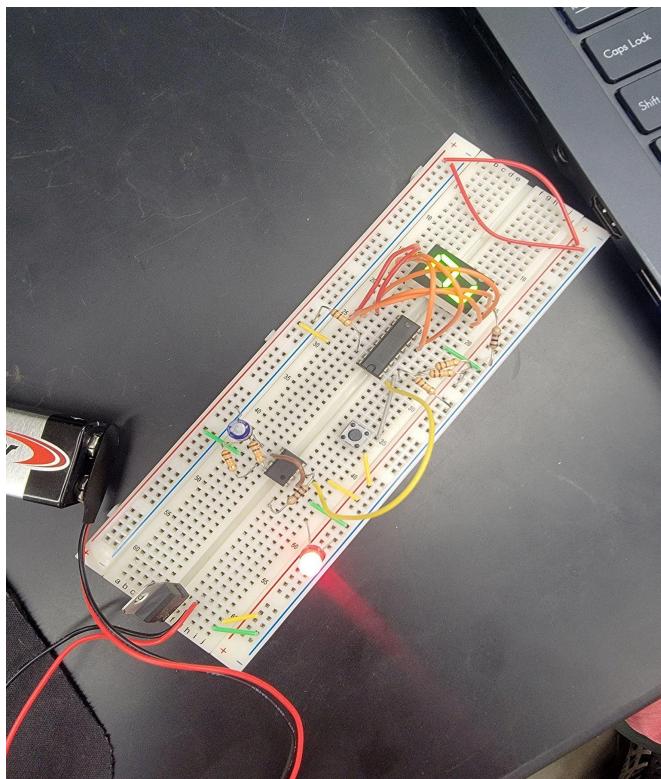
Introduction

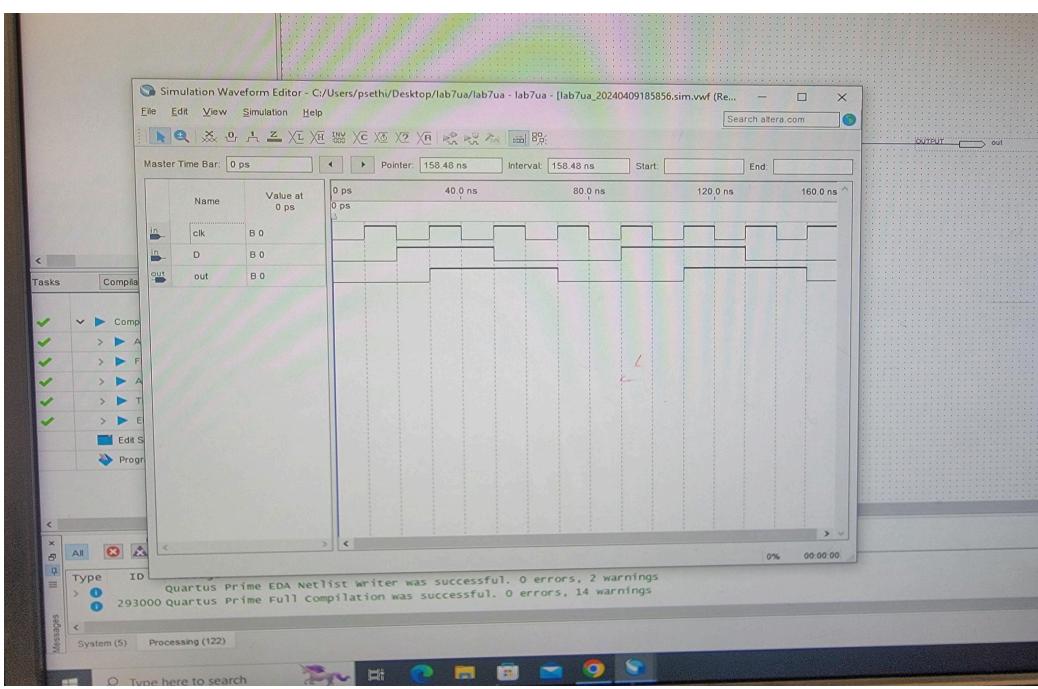
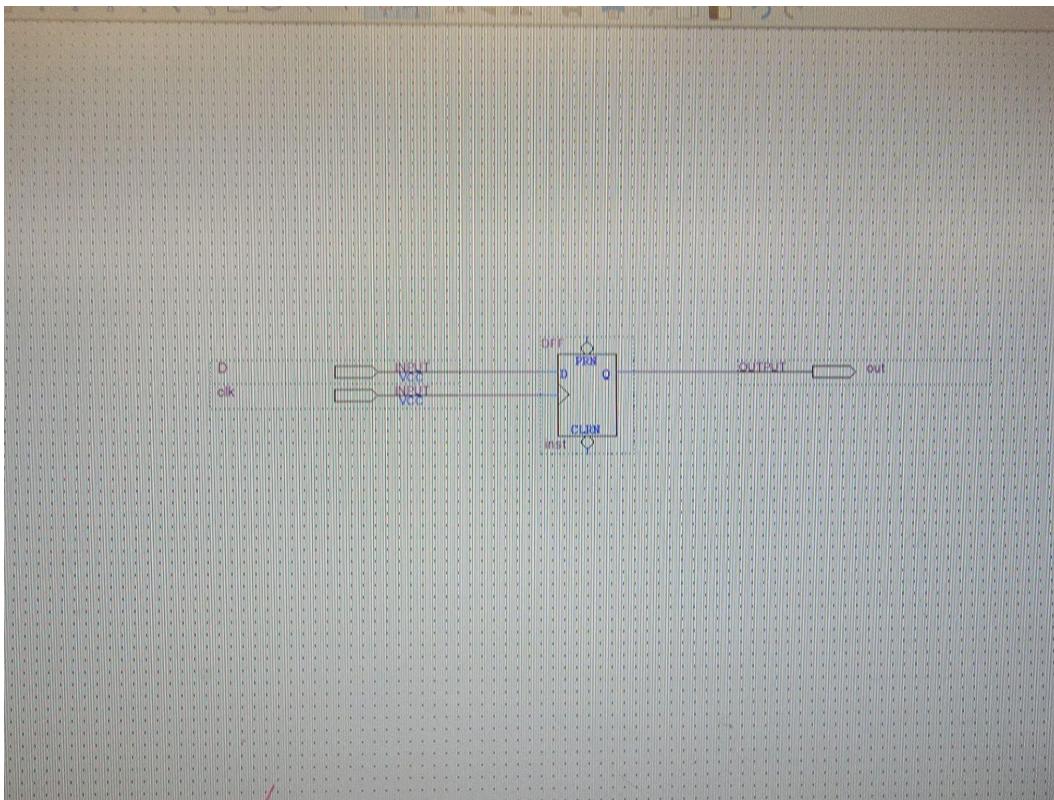
In this lab, we use two tools to implement multiple sequential devices using Quartus software and a breadboard. The devices include D flip-flops, counters, and a sequence detector.

Procedure

- 1)- We designed and edge triggered D flip-flop in a .bdf file followed by implementation of the same using VHDL.
- 2)- Then, we used VHDL code to create a BCD counter to count upward. We further used the provided circuit kit to implement this counter on a breadboard.
- 3)- For our last design, We used behavioral VHDL to design a Moore Type finite state machine that detects the input sequence of 100.

Images





Standard Edition - C:/Users/psethi/Desktop/lab7ua/lab7ua - lab7ua

Project Assignments Processing Tools Window Help

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Hierarchy Entity:Instance EMA5F31C6

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 ENTITY flipflop IS
4 PORT ( D, Clock : IN STD_LOGIC ;
5 Q : OUT STD_LOGIC );
6 END flipflop;
7 ARCHITECTURE Behavior OF flipflop IS
8 BEGIN
9 PROCESS ( clock )
10 BEGIN
11 IF Clock'EVENT AND clock = '1' THEN
12 Q <= D ;
13 END IF ;
14 END PROCESS ;
15 END Behavior ;
```

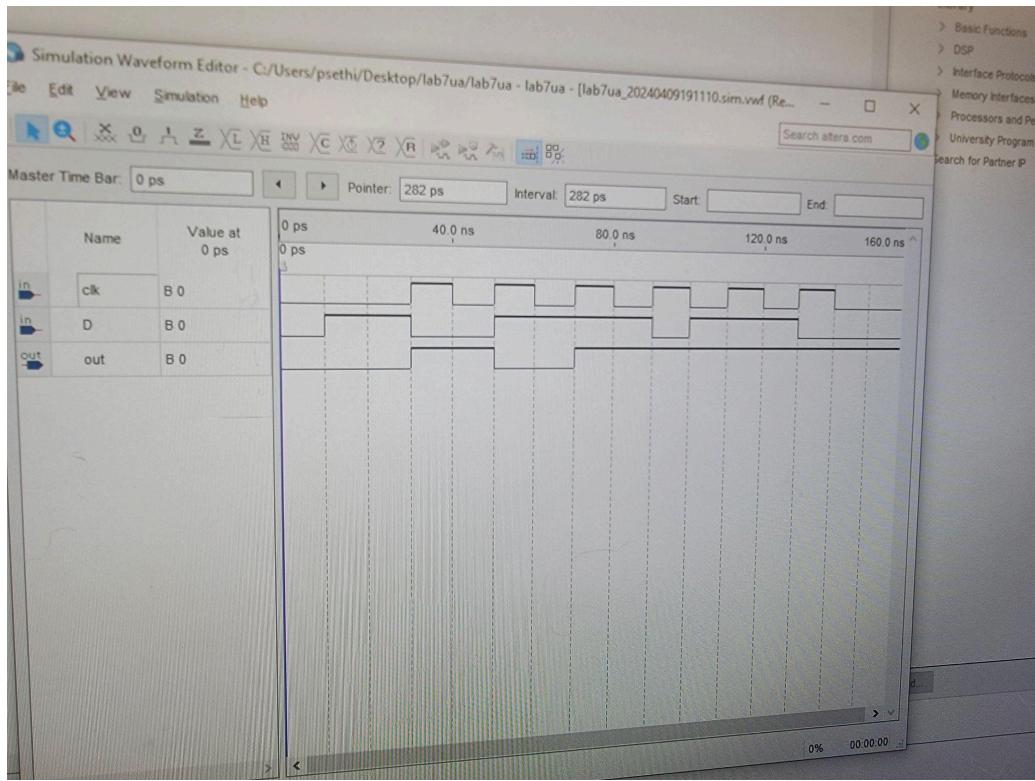
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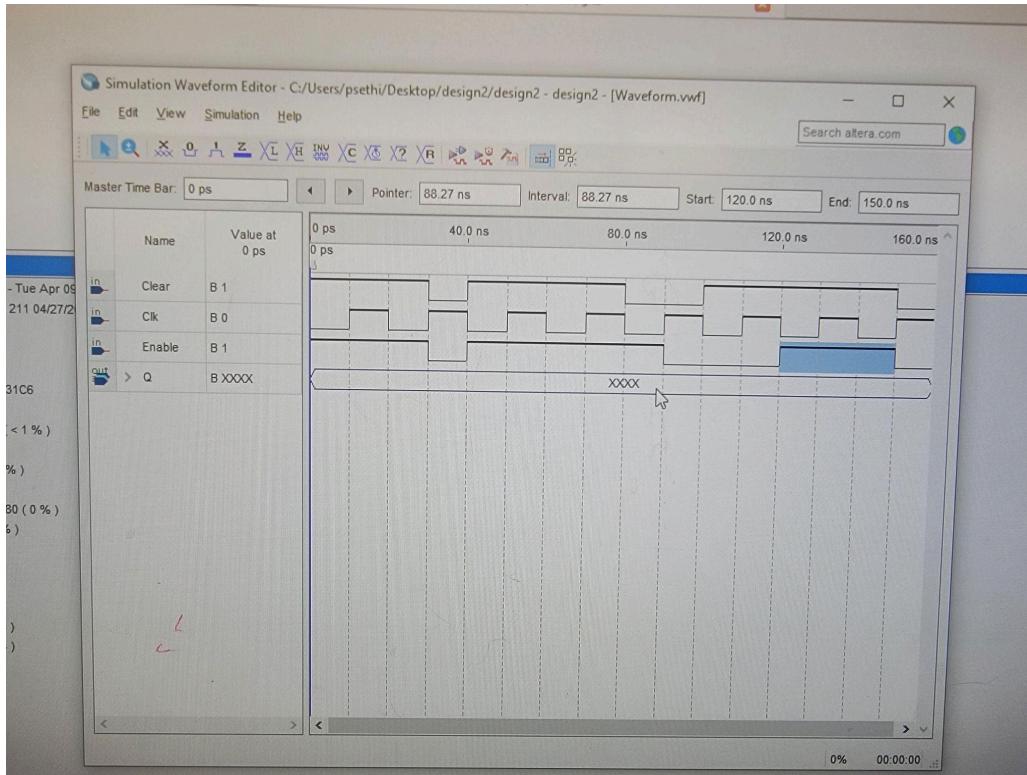
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Vhd3.vhd

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 USE ieee.std_logic_arith.all;
4 USE ieee.std_logic_unsigned.all;
5 ENTITY counter10 is
6 PORT (Clk: in std_logic; Clear: in std_logic;Enable : in std_logic;
7 Q : out std_logic_vector(3 downto 0));
8 END counter10;
9 ARCHITECTURE RTL of counter10 is
10 signal Count: std_logic_vector(3 downto 0);
11 BEGIN
12 counter10: PROCESS (Clk, clear)
13 BEGIN
14 IF (clear = '0') THEN
15 Count <= (others => '0');
16 ELSIF (Clk'event and Clk = '1') THEN
17 IF (Enable = "1") THEN
18 IF (Count = "1001") THEN
19 Count <= (others => '0');
20 ELSE
21 Count <= Count + 1;
22 END IF;
23 END IF;
24 END IF;
25 END PROCESS counter10;
26 Q <= Count;
27 END RTL;
```





The screenshot shows the Quartus II software interface with the file `design2.vhd` open. The code is as follows:

```

1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 USE ieee.std_logic_arith.all;
4 USE ieee.std_logic_unsigned.all;
5 ENTITY design2 IS
6 PORT (Clk: in std_logic; clear: in std_logic; Enable : in std_logic;
7       Q : out std_logic_vector(3 downto 0));
8 END design2;
9 ARCHITECTURE RTL OF design2 IS
10 SIGNAL Count: std_logic_vector(3 downto 0);
11 BEGIN
12 design2: PROCESS (clk, clear)
13 BEGIN
14 IF (Clear = '0') THEN
15 Count <= (others =>'0');
16 ELSIF (clk'event and clk = '1') THEN
17 IF (Enable = '1') THEN
18 IF (Count = "1001") THEN
19 Count <= (others => '0');
20 ELSE
21 Count <= Count + 1;
22 END IF;
23 END IF;
24 END IF;
25 END PROCESS design2;
26 Q <= Count;
27 END RTL;

```

Lab Score Sheet

Lab Procedures	Score	Lab TA comments/Initials
Design A (A-1 and A-2): 10 pts	10	llas
Design B: 20 pts	20	llas
Design C: 20 pts	20	llas
Design D: 20	20	llas
Design E: Bonus 10 pts.		
Lab Report		
Lab report: 30 pts	Impostar	
Total Score		

