Combinepdf - DEEZ

Digital Logic (University of Alabama)

Lab 4

ECE 380

University of Alabama

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Introduction

The purpose of the laboratory was to use k maps to find the simplest logic to both an Sum of Product function and Product of Sum function. Drawings, Schematics and VDHL were created to reflect their logic.

Procedure

a) Prelaboratory

Kmaps were created from the given function. The SOP K map looked as such.

CD \ AB	00	01	11	10
00	1	1		1
01	1	1		
11		1	1	
10	1	1		1

$$\bar{A}\bar{C} + \bar{A}\bar{D} + \bar{B}\bar{D} + BCD$$

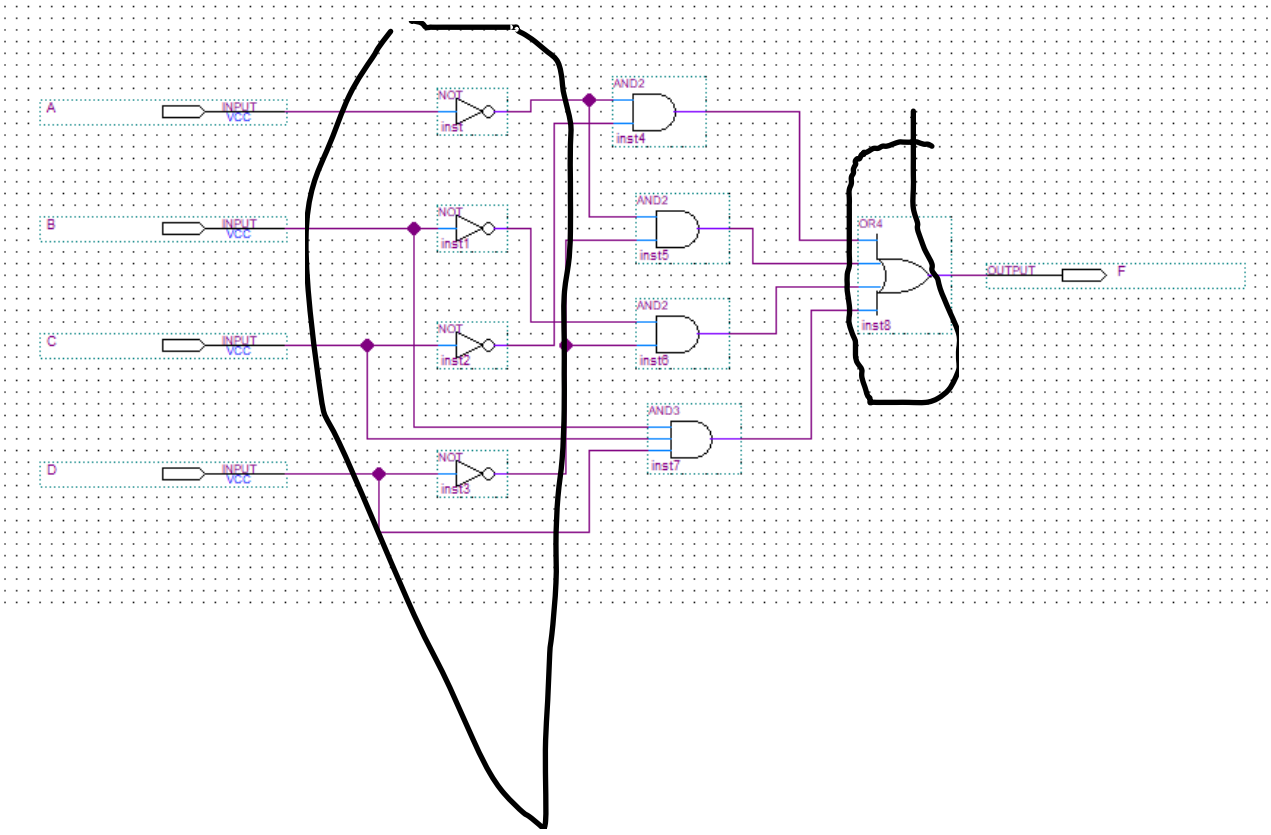
The given POS function created a kmap as such.

CD \ AB	00	01	11	10
00			0	
01			0	0
11	0			0
10			0	

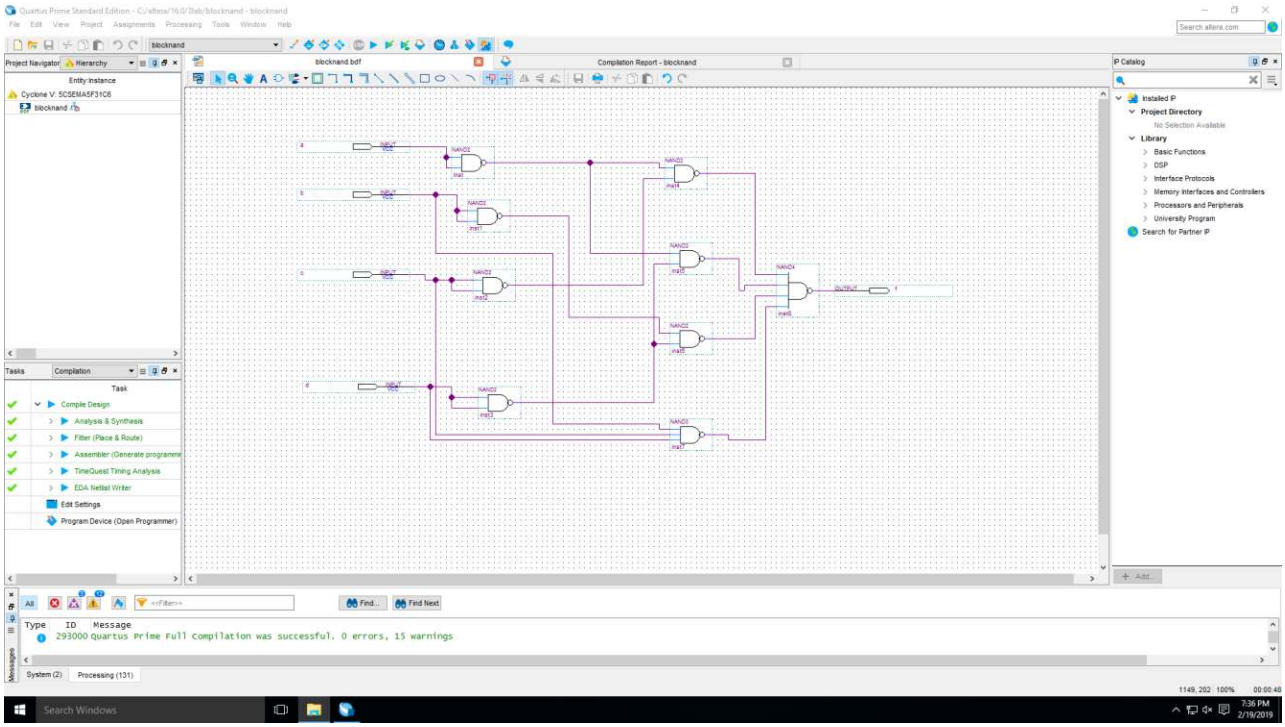
$$(B + \bar{C} + \bar{D})(\bar{A} + C + \bar{D})(\bar{A} + \bar{B} + D)$$

b) Setup and Data Collection

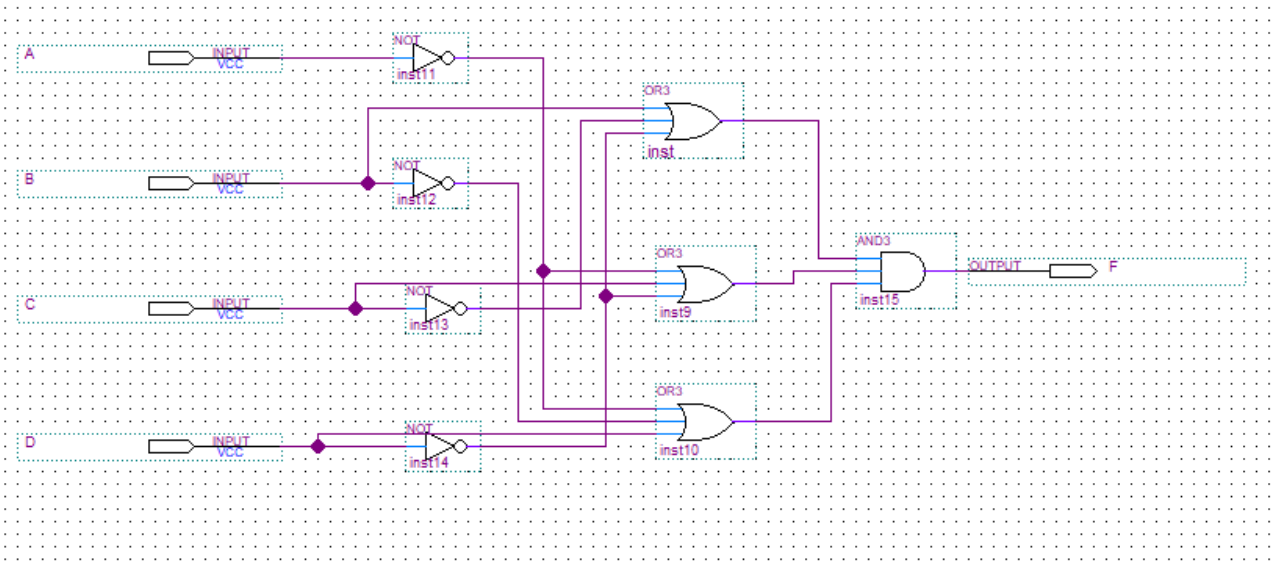
1. Next, A drawing of the SOP logic was created using And, Or, and Not Gates.



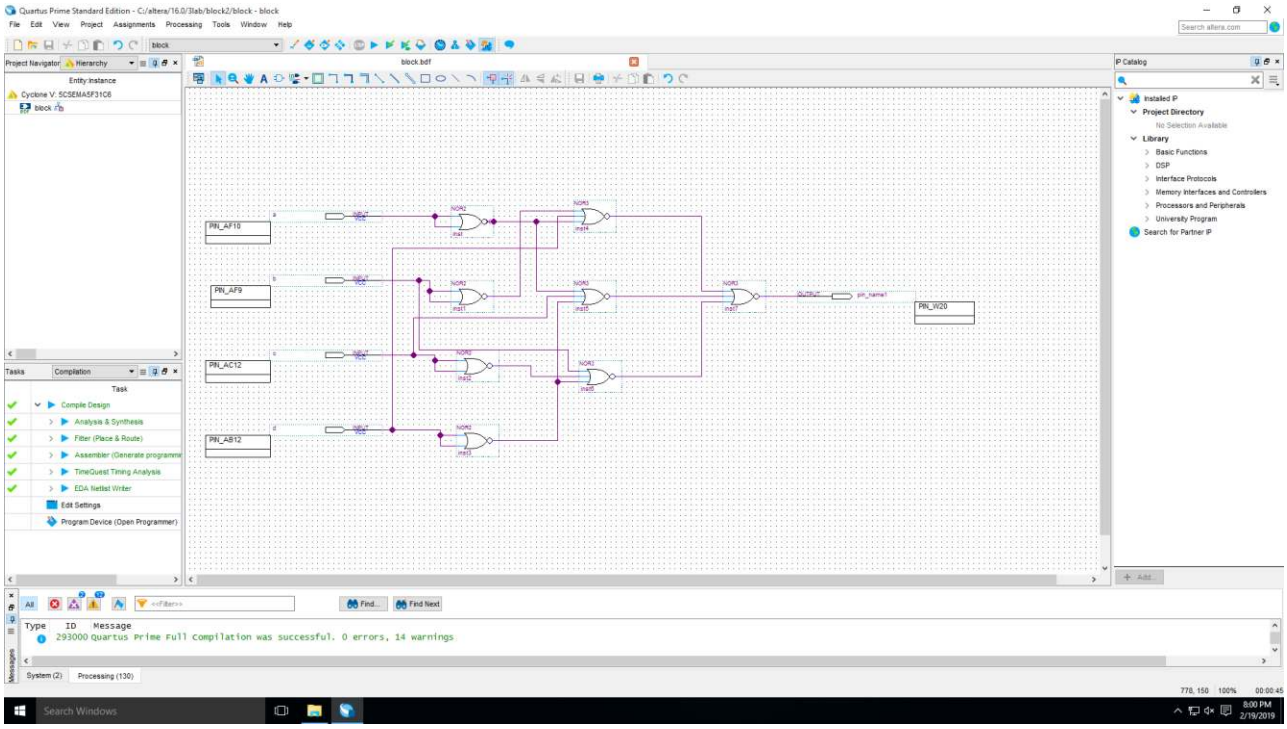
2. A NAND only drawing was created to represent the SOP logic.



3. Using the POS kmap, a drawing of the simplified logic was created using And, Not, and Or Gates.



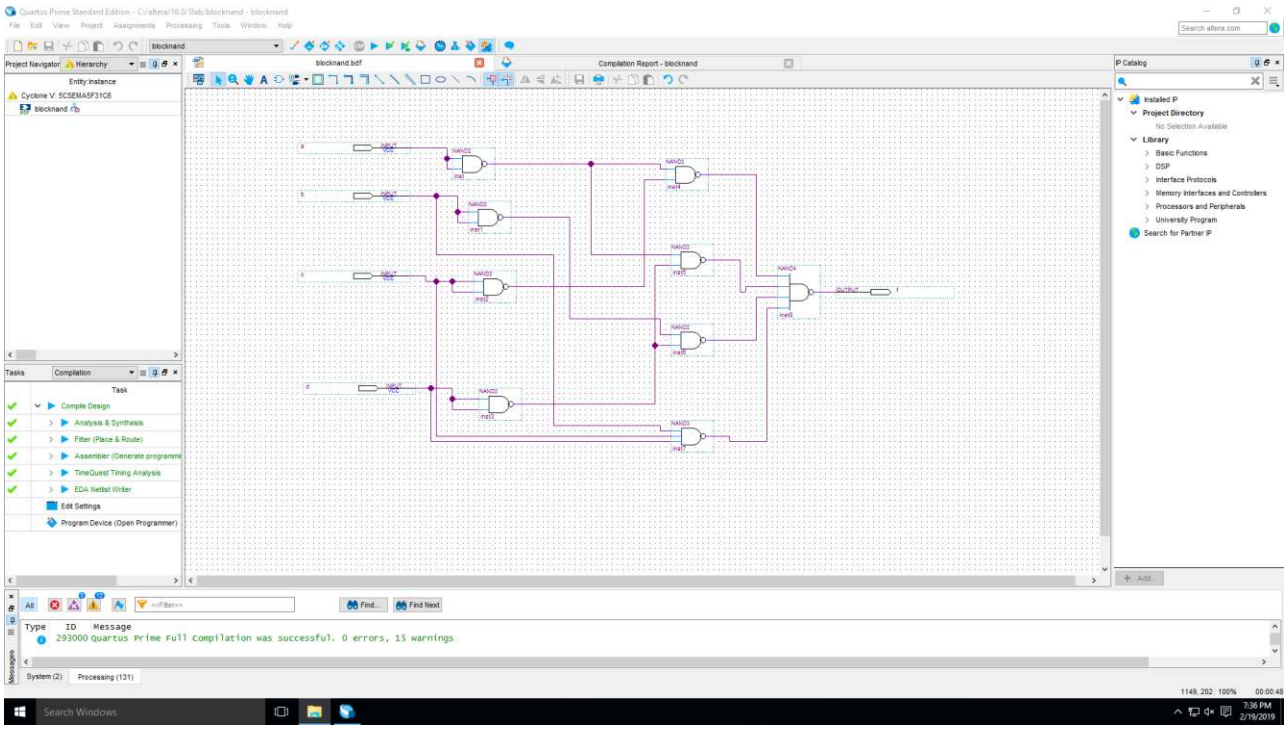
2. A NOR only Gate was created.



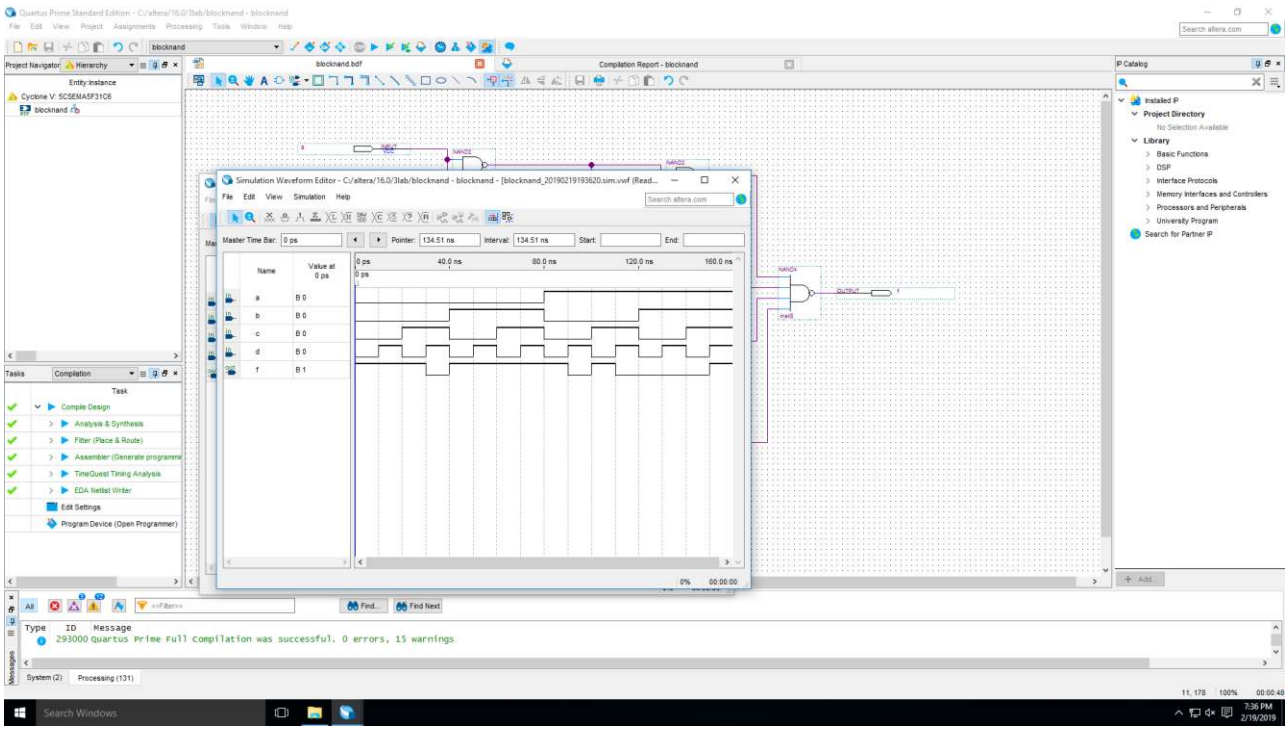
Results

In lab, we designed four circuits, two different ways. The 1st was created using the SOP only NAND gates in a schematic and then typing a VDHL for it. The 2nd was created using the POS only NOR gates in schematic and VHDL coding.

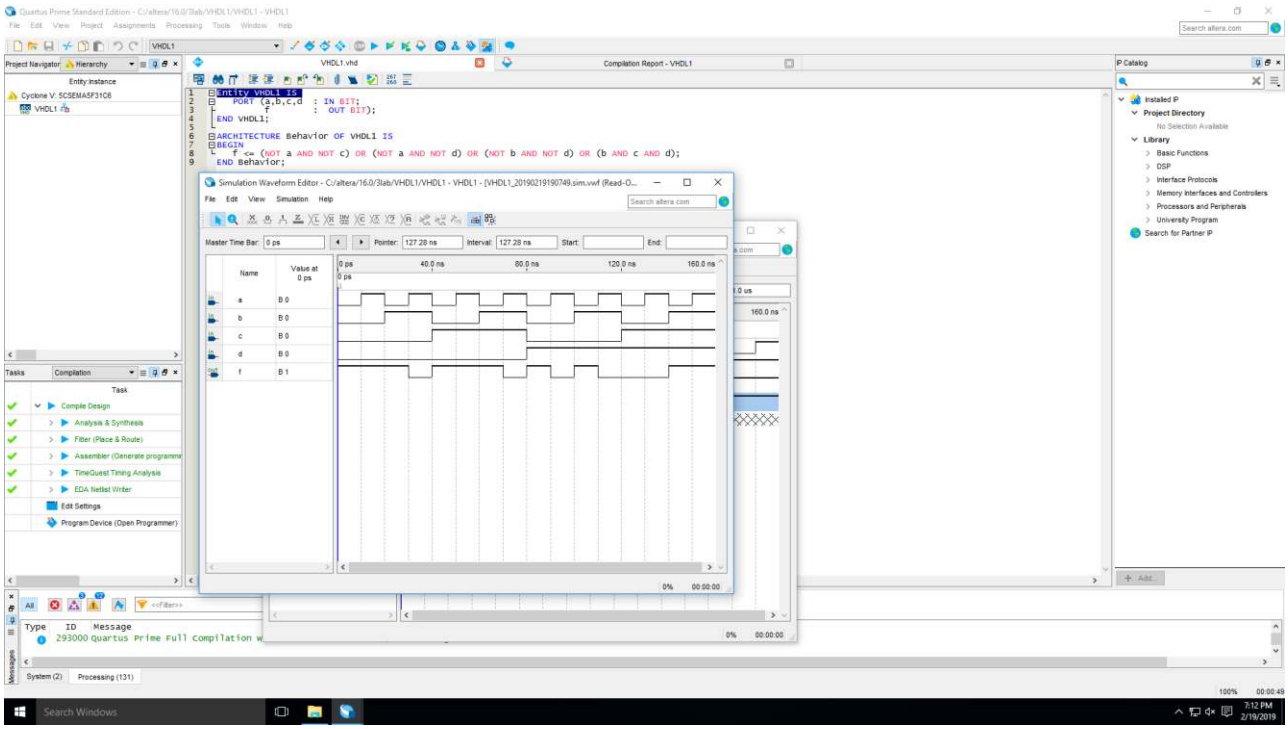
SOP NAND ONLY GATE SCHEMATIC



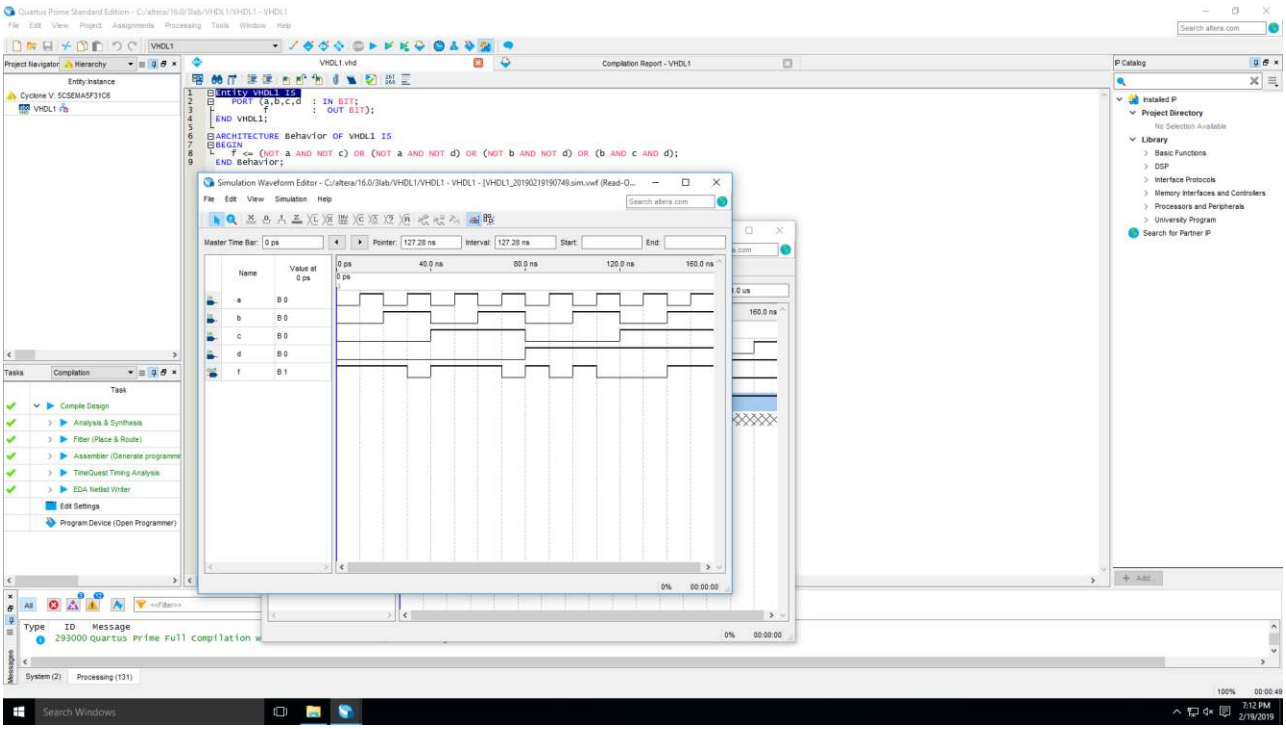
SOP NAND ONLY GATE WAVEFORM



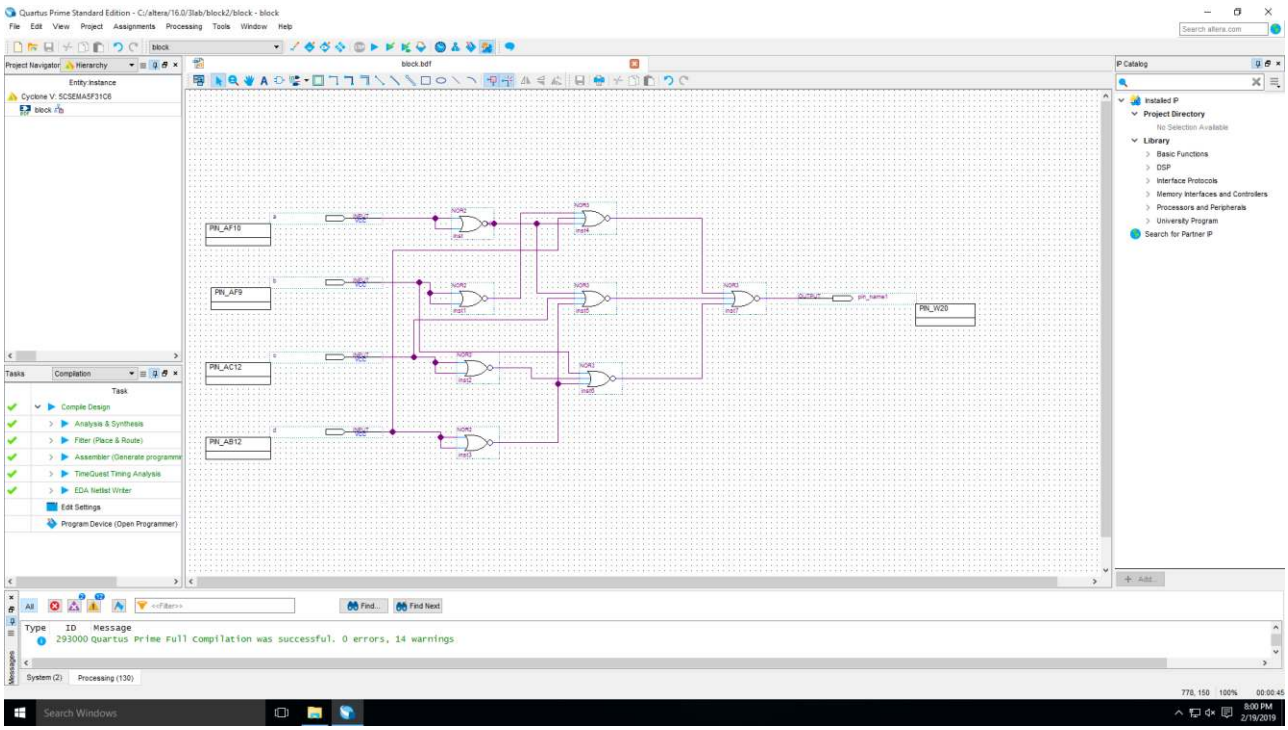
SOP VHDL



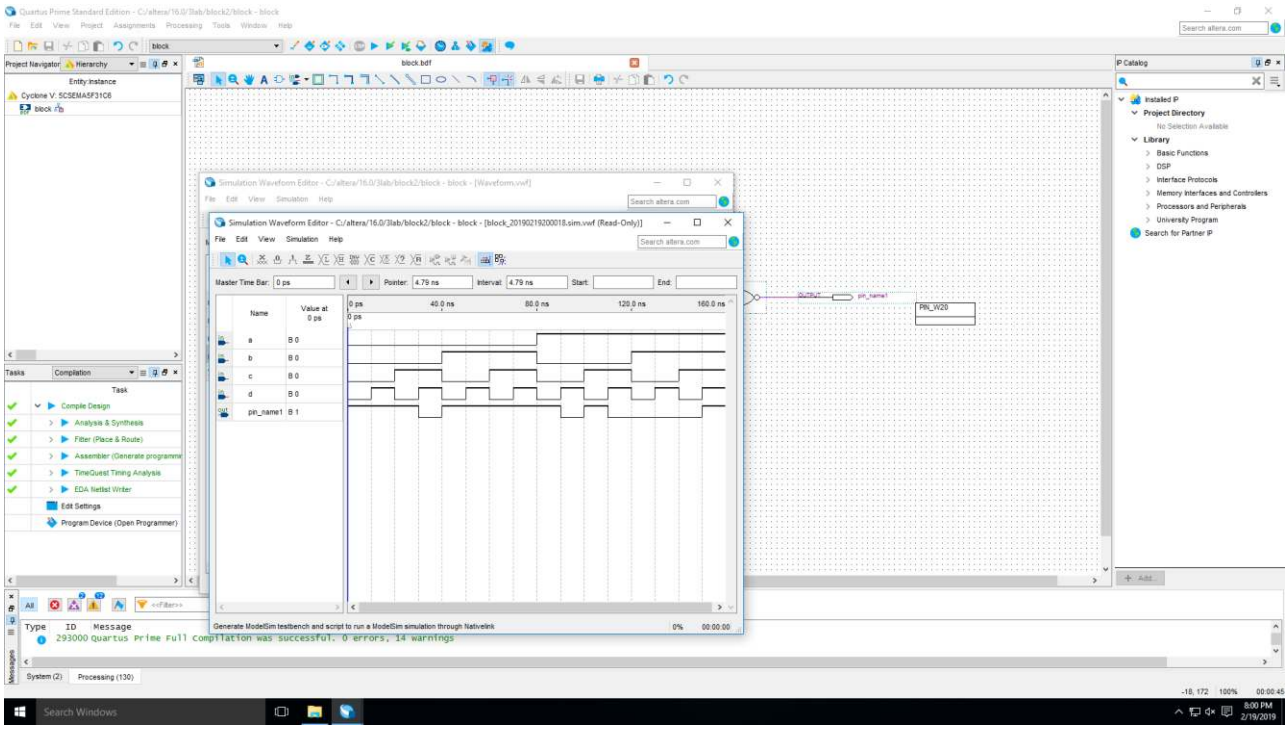
SOP VHDL WAVEFORM



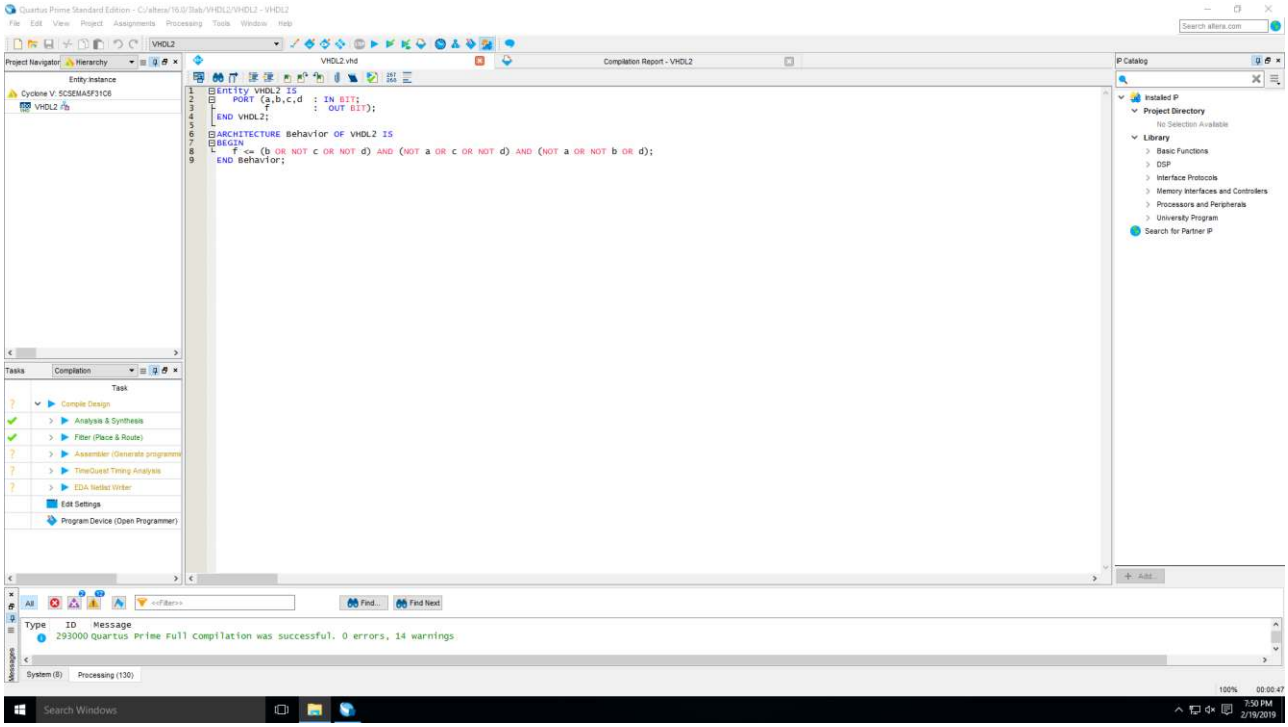
POS SCHEMATIC



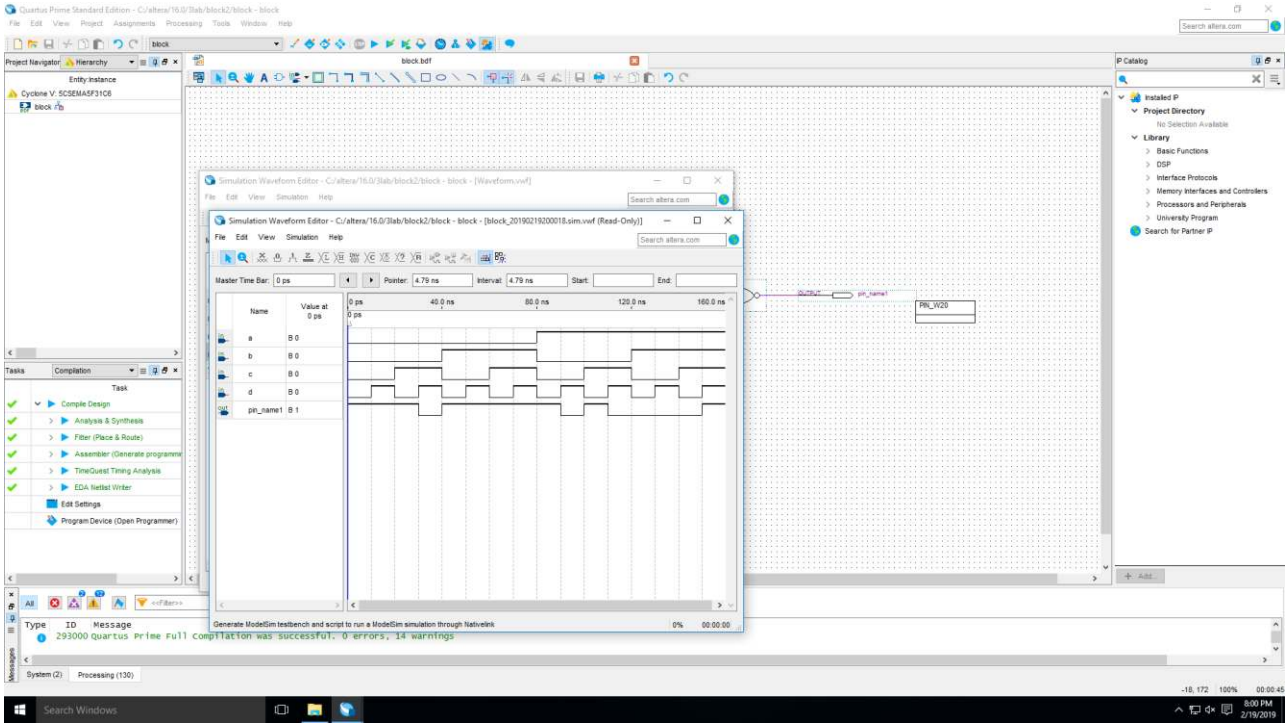
POS SCHEMATIC WAVEFORM



POS VHDL



POS VHDL WAVEFORM



The following table was updated with the information.

INPUTS				OUTPUTS				
A	B	C	D	f	f min SOP	f NAND	g min POS	g NAND
0	0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1
0	0	1	1	0	0	0	0	0
0	1	0	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1
1	0	0	1	0	0	0	0	0
1	0	1	0	1	1	1	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1

Conclusion

In summary, if all designs were done correctly, the outputs for each should have been the same as originally calculated in the prelab.