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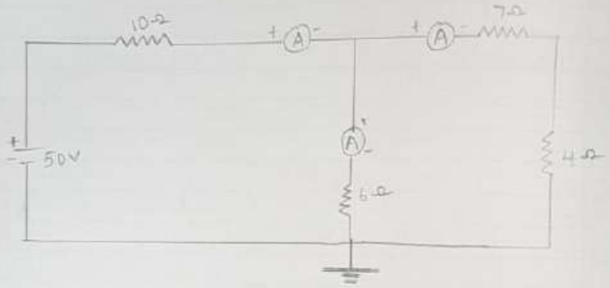
CIRCUIT DIAGRAM: KCL :-



TABULATION:-

KCL	Ia(A)	Ib(B)	Ic(A)	Ib+Ic (A)
THEORITICAL	3.601	2.33	1.271	3.601
PRACTICAL	3.602	2.33	1.271	3.602

Expt. No. 1

VERIFICATION OF KIRCHHOFF'S LAW

AIM:-

To verify Kirchhoff current law and kirchhoff's voltage law of circuit.

SOFTWARE REQUIRED:-

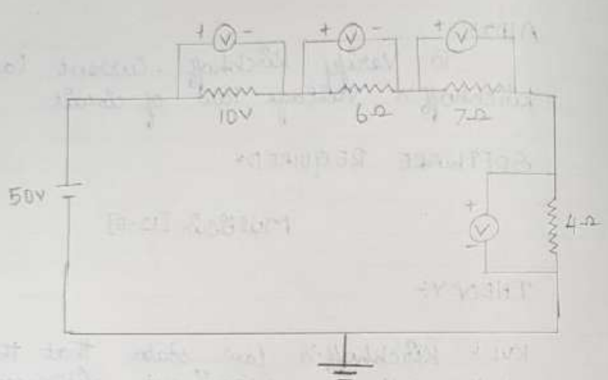
Multisim [12.0]

THEORY:-

KVL:- Kirchhoff's law states that the sum of the voltage experiment differences around any closed loop in a circuit must be zero. A loop in a circuit is any path which ends at the end at the same point at which it starts.

KCL:- Kirchhoff's current law states that the algebricl sum of the current entering and leaving a node is equal to zero. by convention. currents entering the node are positive and those leaving a node are negative.

CIRCUIT DIAGRAM:-



TABULATION:-

KVL	SOURCE (V)	$V_{10\Omega}$ (V)	$V_{6\Omega}$ (V)	$V_{7\Omega}$ (V)	$V_{4\Omega}$ (V)
THEORITICAL	50	36.01	13.98	0	0
PRACTICAL	50	18.519	11.111	7.407	12.968

kvgejdwksldffdfghj

KCL:-

To prove,

At Node A,

$I_a = I_b + I_c$

$I_b = 2.33A$

$I_c = 1.271A$

$I_a = 3.601A$

$\therefore I_a = I_b + I_c$

$3.601A = 2.33A$

KVL:-

LOOP 1:-

$50 = V_{10\Omega} + V_{6\Omega}$

$V_{10\Omega} = I_{10\Omega} \times 10$

$V_{6\Omega} = 6(I_1 - I_2)$

$50 = 10I_1 + 6(I_1 - I_2)$

$50 = 16I_1 - 6I_1 \Rightarrow (1)$

LOOP 2:-

$0 = 7I_2 + 4I_2 + 6(I_2 - I_1)$

$= 11I_2 + 6(I_2 - I_1)$

$= 17I_2 - 6I_1 \Rightarrow (2)$

$$\begin{bmatrix} 16 & -6 \\ -6 & 17 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 50 \\ 0 \end{bmatrix}$$

Expt. No.

$$I_1 = 3.6014\,A$$
$$I_2 = 1.2714\,A$$

$V_{10\Omega} = I_{10\Omega} \times 10 = 3.6014 \times 10 = 36.01V.$

$V_{6\Omega} = I_{6\Omega} \times 6 = (I_1 - I_2) \times 6.$
$= (3.601 - 1.271) \times 6.$
$V_{6\Omega} = 13.98V$

To prove :- $50 = V_{10\Omega} + V_{6\Omega}$
$= 36.01 + 13.98.$
$= 49.99V$

10

RESULT:-

Thus, The Kirchhoff's current law and Kirchhoff's Voltage law were Verified successfully.

OPEN CIRCUIT AND LOAD CHARACTERISTICS OF DC SHUNT GENERATOR.

AIM:-

To draw the open circuit and load characteristics of DC Shunt generator.

APPARATUS REQUIRED:-

Laptop with internet connection.

THEORY:-

DC generator converts mechanical energy into electrical energy.

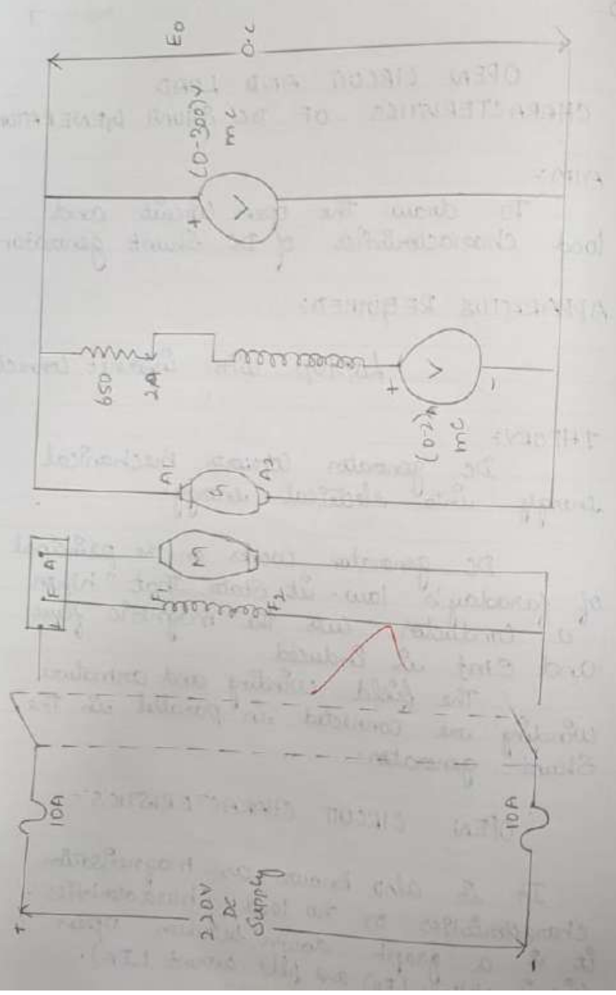
DC generator works on the principal of faraday's law. it states that "when a conductor cuts the magnetic flux and emf is induced.

The field winding and armature winding are connected in parallel in the shunt generator.

OPEN CIRCUIT CHARACTERISTICS:-

It is also known as magnetisation characteristics or no load characteristics. it is a graph drawn between open circuit voltage (E_0) and field current (I_F).

OPEN CIRCUIT CHARACTERISTICS:-



Expt. No.

LOAD CIRCUIT CHARACTERISTICS:-

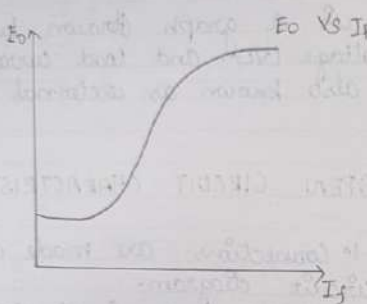
It is a graph drawn between load voltage (VL)V. and load current (IL). It is also known as external Characteristics.

OPEN CIRCUIT CHARACTRISTICS:-

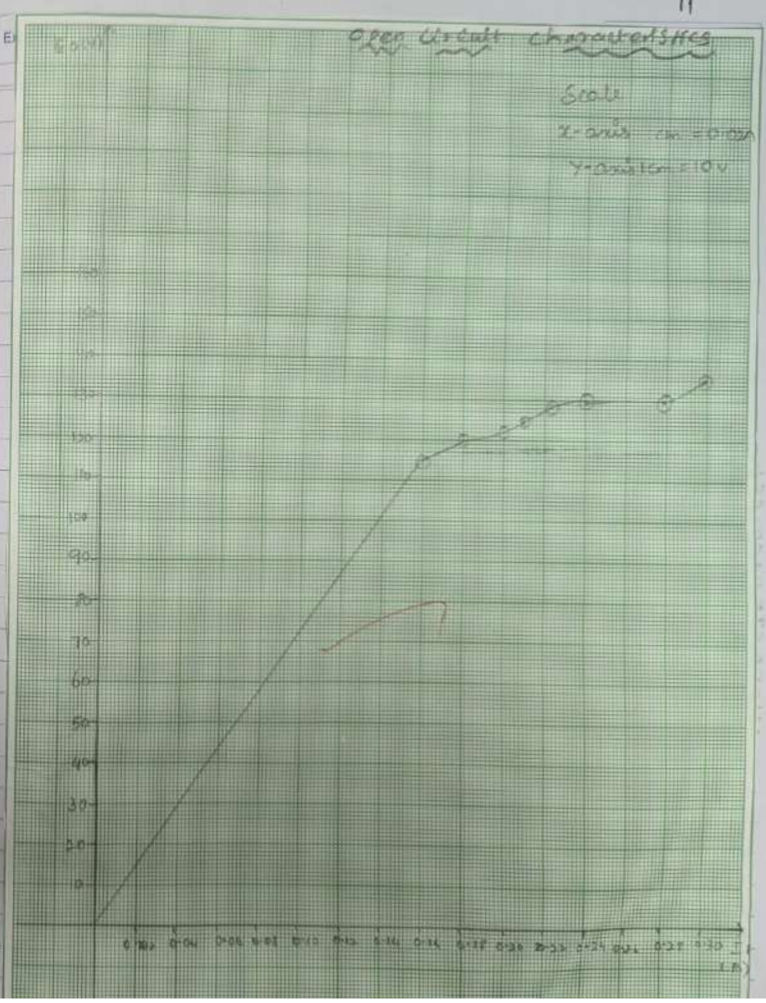
1. Connections are made as per the circuit diagram.
2. Switch on the supply and note drawn the reading (Voltage and current).
3. By varying the field rheostat different values of open circuit voltage are field current are noted.
4. Plot the graph b/w open circuit voltage and field current.

MODEL GRAPH.

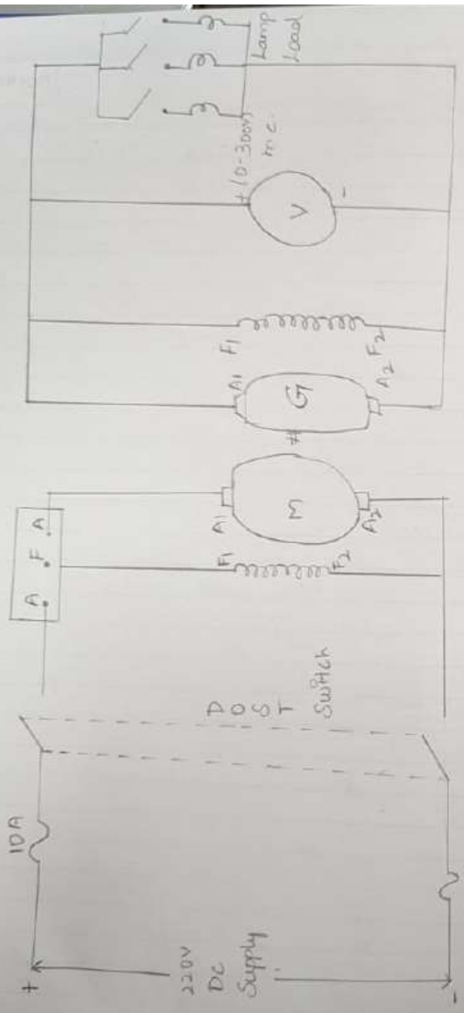
OPEN CIRCUIT CHARACTERISTICS :-



S.NO	VOLTAGE	CURRENT (A)
1	115	0.16
2	120	0.18
3	126	0.20
4	129	0.21
5	133	0.23
6	135	0.24
7	138	0.28
8	142	0.30



LOAD CIRCUIT CHARACTERISTICS:-



LOAD CHARACTERISTICS:-

1. Connections are made as per the circuit diagram.

2. Switch on the supply and note the no load voltage and current.

3. By connection different nodes, different values of load voltage and note current are noted.

4. plot the graph between load voltage are load current.

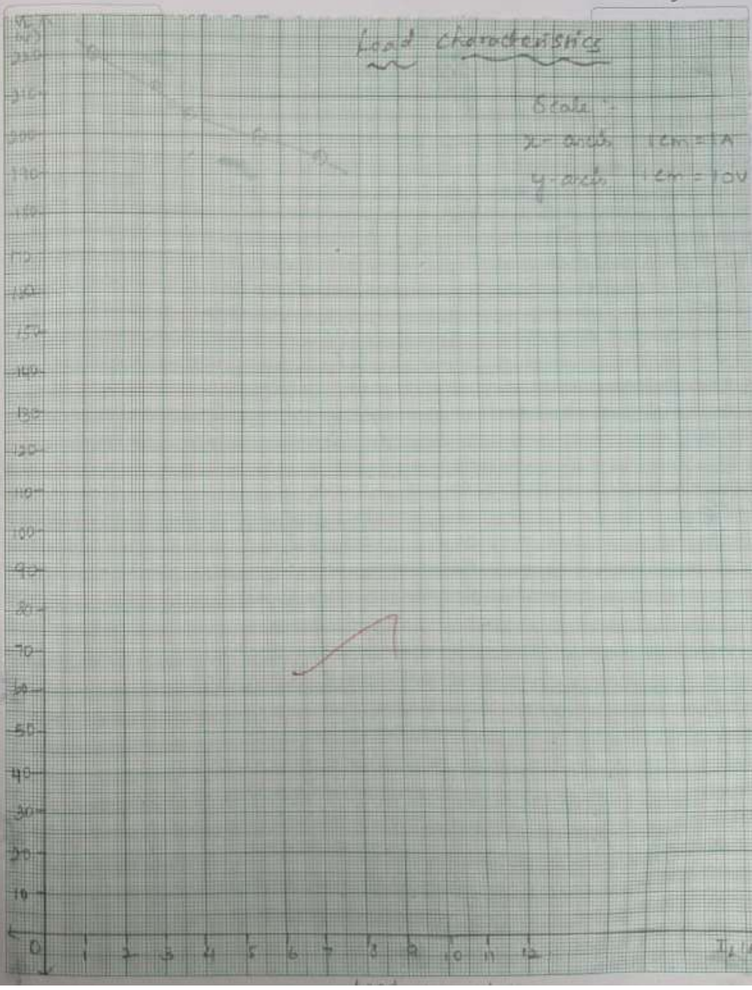
LOAD CHARACTERISTICS

1. Connections are made as per the circuit diagram.

2. Switch on the supply and note the no load voltage and current.

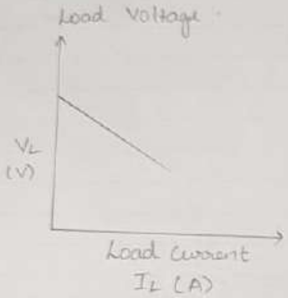
3. By connecting different loads, different values of load voltage and load current are noted.

4. plot the graph between load voltage and load current.



MODEL GRAPH.

Load Characteristics



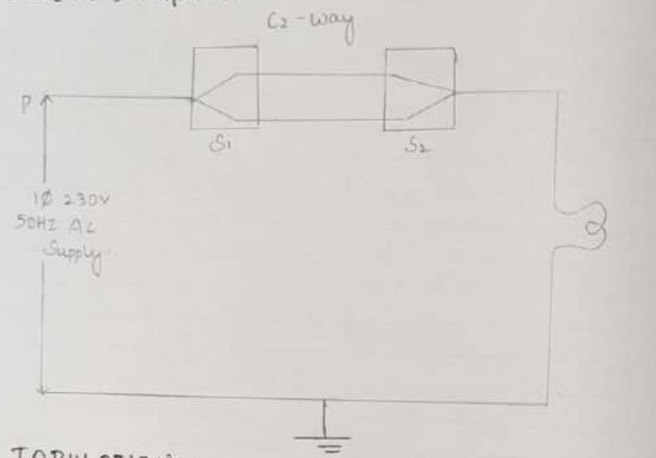
S.No	Current (A)	Voltage(V)
1	1.2	220
2	2.8	212
3	3.2	208
4	3.6	205
5	5.5	200
6	7	195.

10

RESULT:-

Thus the open circuit and load characteristics of DC shunt generator were verified successfully.

CIRCUIT DIAGRAM:-



TABULATION:-

Mode	S_1	S_2	Lamp.
1	OFF	OFF	ON
2	OFF	ON	OFF
3	ON	OFF	OFF
4	ON	ON	ON

STAIRCASE WIRING

AIM:

Draw the staircase wiring diagram and develop it in proteus.

APPARATUS REQUIRED:-

Laptop with proteus.

THEORY:-

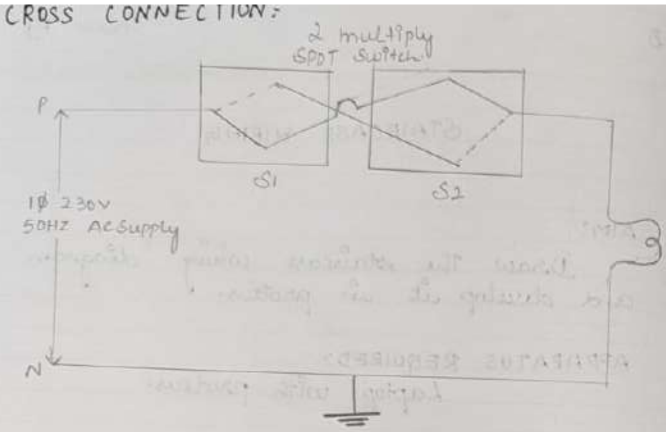
Staircase wiring is a common multiply way switching or two way switching connection. It involves wiring for one light with two switches in this setup a single lamp is controlled by two switches located at different position is allows the user to operate the load from separate position above or below the staircase from inside or outside of room or two way bed switch.

PROCEDURE:-

1) Drag the required components from the proteus library.

2) Connect the components as per circuit diagram.

CROSS CONNECTION:-



TABULATION:-

Mode	S_1	S_2	Lamp
1	OFF	OFF	OFF
2	OFF	ON	ON
3	ON	OFF	ON
4	ON	ON	OFF

Components	Proteus	Specification
AC Supply	Vsine	Amplitude = 230V Frequency = 50HZ
2 way S/w	SPDT	
LAMP	Lamp (Animated)	230V

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3) Run the simulation and check the lamp for different switch condition.

10

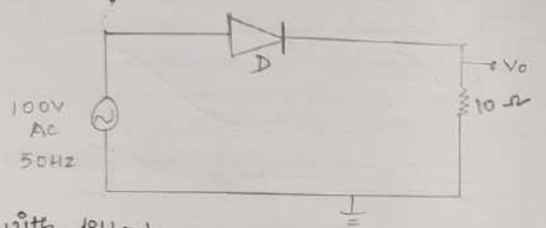
RESULT:-

Thus the staircase wiring connection are developed in proteus and tested.

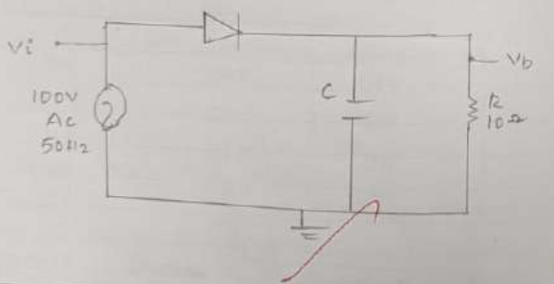
HALF WAVE RECTIFIER:-

Circuit Diagram:-

Without filter:-



with filter:-



Input Voltage		Output Voltage			
		Without filter		With filter.	
Vm(V)	t(ms)	Vm(V)	t(ms)	Vm(V)	t(ms)
100V	20ms	100V	10ms	100V, 85V	5ms, 15ms.

Expt. No. 4

HALF WAVE AND FULL WAVE

AIM:-

TO Stimulate the following circuits proteus (i) Half wave rectifier
(ii) Full wave rectifier.

APPARATUS REQUIRED:-

Laptop with Proteus Software.

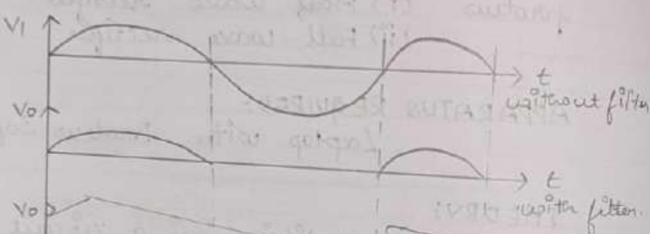
THEORY:-

A rectifier is a circuit that converts alternating current (AC) into Direct current (DC).

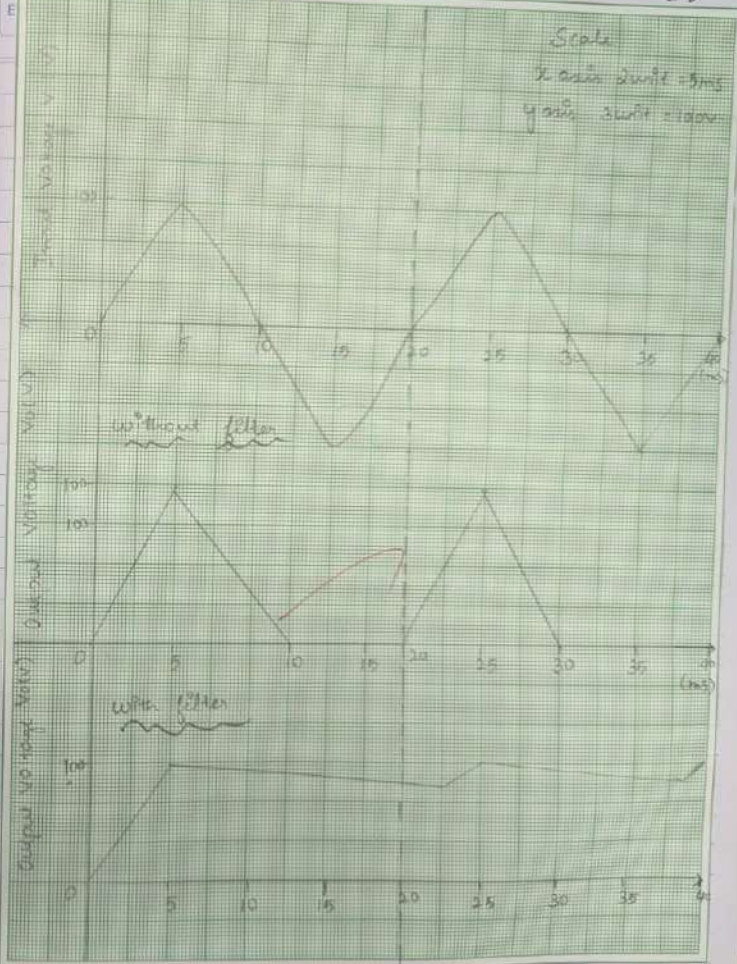
HALF wave rectifier:-

Half wave rectifier conductor only during positive half cycle. During positive half cycle, the diode current and the Output voltage is equal to the Voltage. During negative half cycle, the diode does not conduct and the output Voltage is equal to zero.

MODEL GRAPH:-



Vi
t
without filter
Vo
t
with filter.
Vo
t

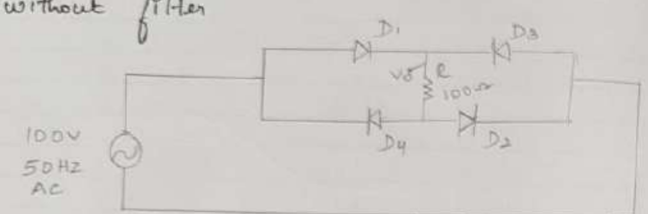


Scale
x axis 2unit = 5ms
y axis 2unit = 100v
Input Voltage V (V)
without filter
Output Voltage Vo (V)
with filter
0
5
10
15
20
25
30
35
40
(ms)
100

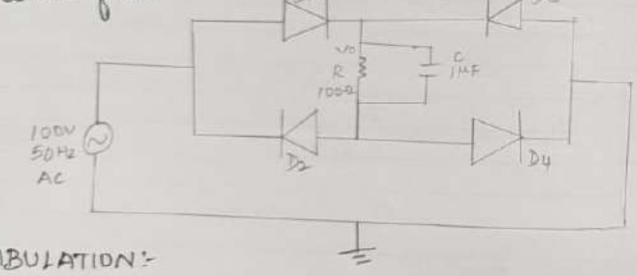
FULL WAVE RECTIFIER:-

Circuit diagram:-

without filter



with filter



TABULATION:-

Input Voltage		Output Voltage			
		without filter.		with filter	
Vm (V)	t(ms)	V(ms)	t(ms)	Vm(V)	t(ms)
50V	20ms	50V	5ms	50V, 46V	5ms, 11ms

Expt. No.

FULL wave rectifier:-

Full wave rectifier conducts during both +ve and -ve half cycles. During +ve half cycle, the output voltage is equal to input voltage. During negative half cycle, the output voltage is equal to negative of the input voltage.

The output of the rectifier circuit is impure DC. In order to get, Pure DC the output is filtered by a capacitor filter.

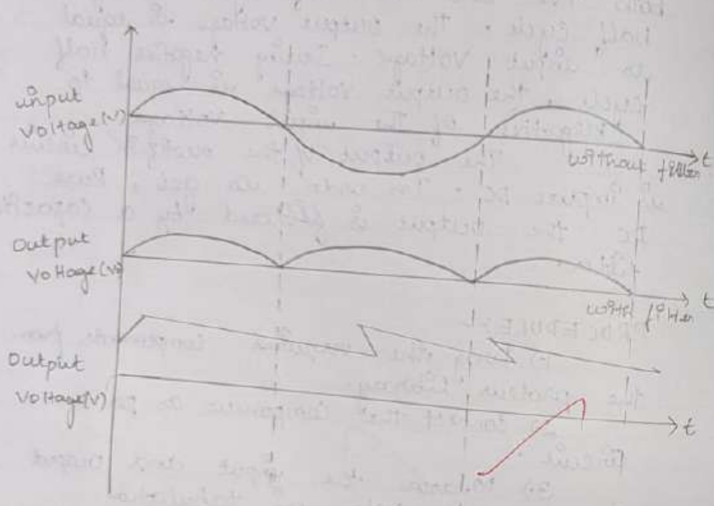
PROCEDURE:-

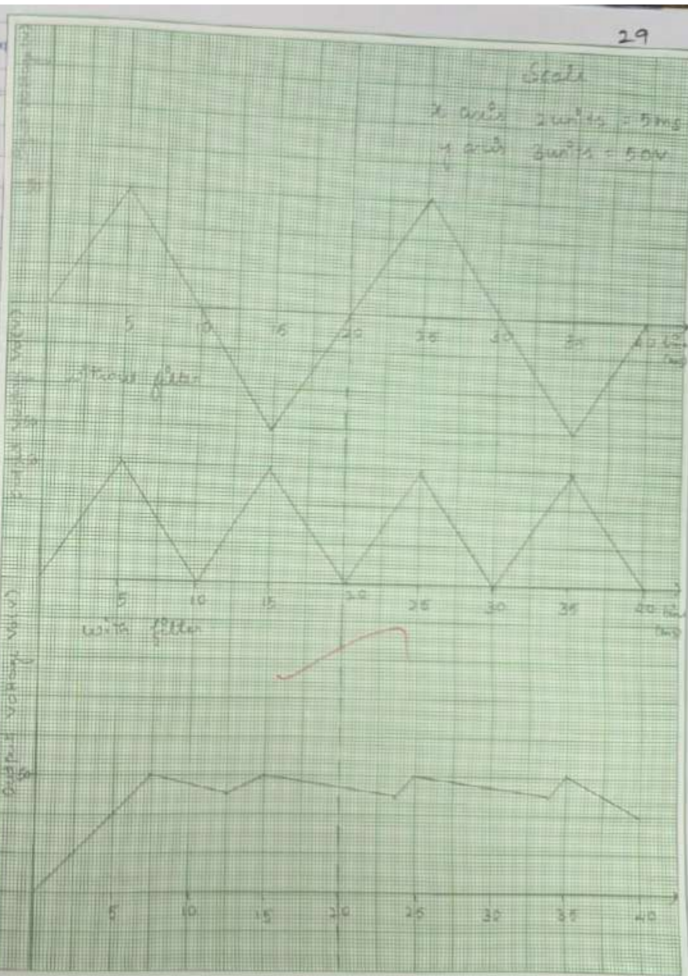
1) Drag the required components from the proteus library.

2) Connect the components as per the circuit.

3) Measure the input and output voltage and note in tabulation.

MODEL GRAPH :-


input Voltage(V)
without filter
t
Output Voltage(V)
with filter
t
Output Voltage(V)
t


Scale
x axis 2 units = 5ms
y axis 2units = 5.0V
without filter
with filter
5
10
15
20
25
30
35
40

COMPONENTS REQUIRED:-

S.No	Components	Proteus	Specification
1.	AC Supply	VSine	amplitude=100v Frequency=50Hz
2.	Diode	Generic diode	
3.	Resistor	Analog resistor primitive	100kΩ
4.	Capacitor	Generic Non-electrolytic Capacitor	1 microF.
5.	Ground	From terminal mode	
6.	Probe	From Probe mode - Voltage.	
7.	Graph	From Graph mode Analogue.	

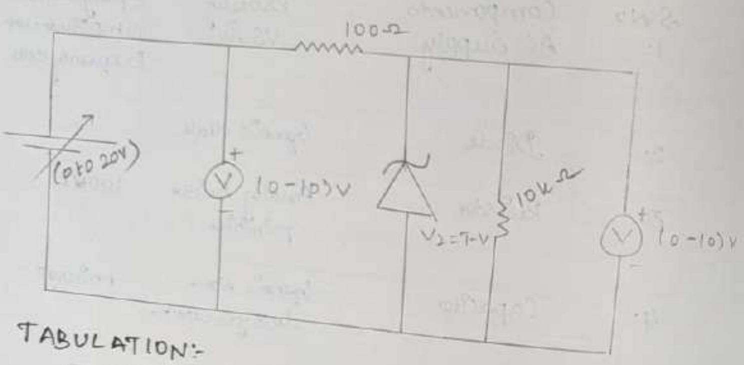
10
8

RESULT:-

Stimulation of both half-wave and full-wave rectifiers was successfull.

LINE REGULATION:-

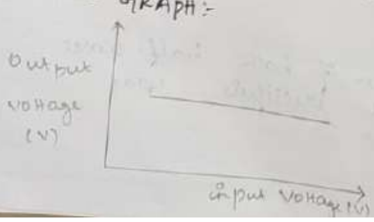
CIRCUIT DIAGRAM:-



TABULATION:-

S.NO	Input Voltage Vi(V)	Output Voltage Vo(V)
1	+12.0	+5.4
2	+13.0	+5.16
3	+14.0	+5.17
4	+15.0	+5.17
5	+16.0	+5.18
6	+17.0	+5.19

MODEL GRAPH:-



Expt. No. 5

ZENER DIODE AS VOLTAGE REGULATOR.

AIM:-

To Stimulate that line and load regulation operation zener diode.

APPARATUS REQUIRED:-

Laptop with proteus Software.

THEORY:-

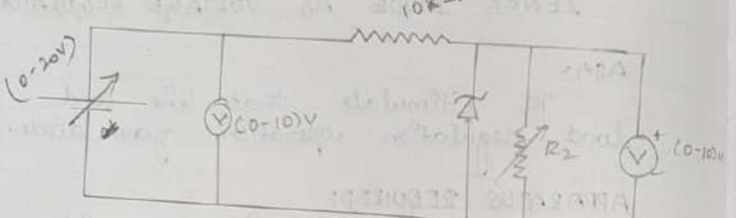
A Heavily dopped PN Junction diode is called Zener diode. Due to heavily dopped nature Zener diode works under forward bias and reverse bias Conditions.

Zener diode under reverse bias Condition is used as a voltage regulator. If the input voltage changes the output is Constant. This is Called line regulation.

The load resistance Changes the output voltage is Constant this is called load regulation.

LOAD REGULATION:-

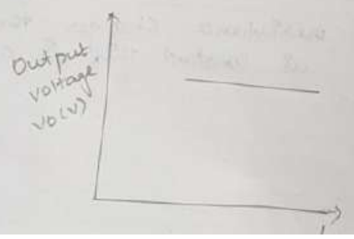
CIRCUIT DIAGRAM:-



TABULATION:-

S.No	Load Resistance $R_2(\Omega)$	Output Voltage Vo(V)
1	+17.0 (100Ω)	+5.19
2	+17.0 (200Ω)	+5.20
3	+17.0 (300Ω)	+5.20
4	+17.0 (400Ω)	+5.20
5	+17.0 (500Ω)	+5.20
6	+17.0 (600Ω)	+5.21

MODEL GRAPH:-



Expt. No.

PROCEDURE:-

1.) Drag the required components from the proteus library.

2.) Connect the components (required) as per circuit diagram.

3.) For line regulation vary the input voltage and note the output voltages in tabulations. Draw the graph between input and output voltages.

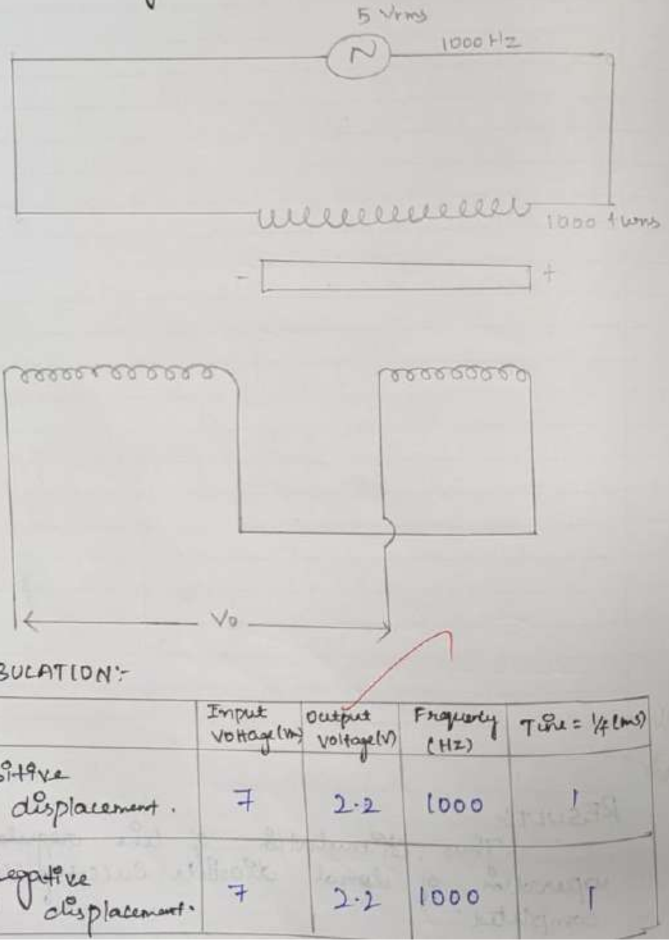
4.) For load regulations vary the load resistance and note the output voltage in tabulation. Draw the graph between Load resistance and voltage.

10

RESULT:-

Thus Stimulation of line regulation operation of zonal diode successfully completed.

Circuit Diagram :-



TABULATION:-

	Input Voltage (Vm)	Output Voltage (V)	Frequency (Hz)	Time = 1/f (ms)
Positive displacement.	7	2.2	1000	1
Negative displacement.	7	2.2	1000	1

CHARACTERISTIC OF LVDT
[LINEAR VARIABLE DIFFRENTIAL TRANSFORMER]

AIM:-
TO understand and stimulate the reaction between core displacement and output voltage

APPARATUS REQUIRED:-
Laptop with internet connection.

THEORY:-
LVDT is an inductive transducer that converts linear displacement into a electrical signal. It consist of a transformer having primary winding and two secondary windings wound on a core. As the primary is connected to an AC source. The AC current and the voltage are produced in the secondary of the LVDT.

When the core is at the center, the flux linking with both the secondary winding are equal. So, the emf induced in both the windings are equal this mean there is no displacement.

CALCULATION:-

$$V_m = V_{rms} \times \sqrt{2} = 5\sqrt{2} = 7V.$$

$$4SD = 7V.$$

$$1SD = 7/4 \ V.$$

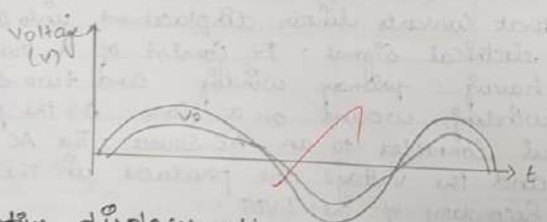
$$1.2\ SSD = 7/4 \times 1.25 = 2.2V.$$

$$f = 1000\ Hz.$$

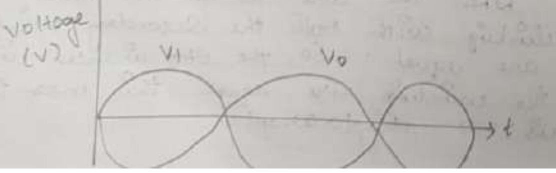
$$T = 1/f = 1/1000 = 1ms$$

MODEL GRAPH:-

Positive displacement:-



Negative displacement:-



When the core is at the right, the flux linkage with the secondary winding S_1, is more so, the emf induced in S_1, is more than S_2. So the emf is positive.

When the core is at the left, the flux linkage and the emf in S_2 is more than S_1. So the net emf is negative.

PROCEDURE:-

1) Connections are made as per the circuit diagram.

2) Set the number of turns, supplied voltage

3) Configure the parameters.

4) Move the core to positive side and the negative side and observe the input voltage and output voltage waveforms.

5) Plot the graph between input and output voltage.

When the core is at the right, the flux linkage with the secondary winding S_1 is more so the emf induced in S_1 is more than S_2 so the emf is positive.

When the core is at the left, the flux linkage with the emf in S_2 is more than S_1 so the net emf is negative.

PROCEDURE:

1) Connection are made as per the circuit diagram.

2) Set the switch of [illegible] supplied voltage.

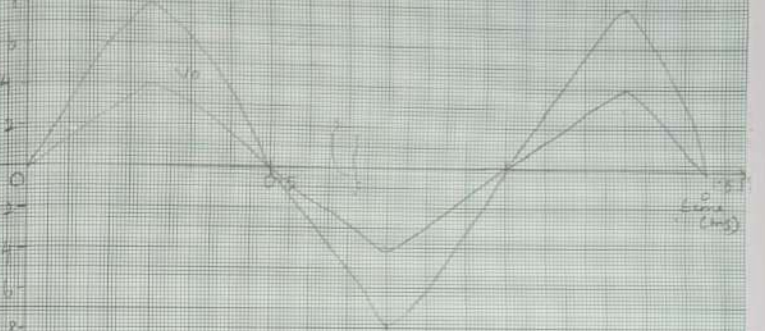
3) Configure the parameters.

4) Move the core to positive side and the negative side and note the input voltage and output voltage [illegible].

5) Plot the graph between input and output voltage.

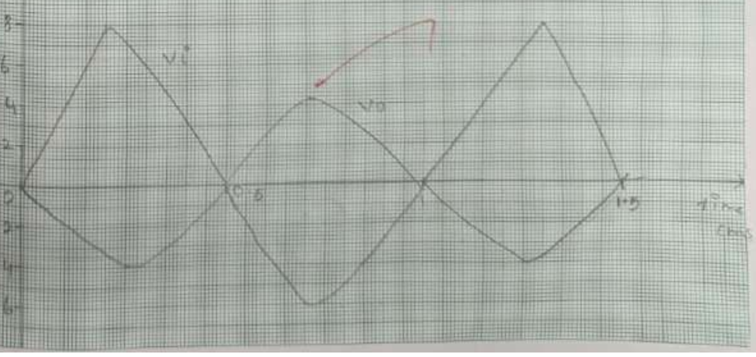
Positive displacement

Scale
On x-axis 5cm = 0.5ms
On y-axis 1cm = 2V



Negative displacement

Scale
x axis 5cm = 0.5ms
on y-axis 1cm = 2V



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RESULT:-

The relation between core displacement and output voltage is simulated successfully.