SETHUPATHI BALAKRISHNAN b.sethupathi@gmail.com | 7845844568

An experienced professional seasoned in Physical Design and STA looking for a full time position at a leading Semiconductor organisation.

EDUCATION

- 2015-2017 | M.Tech (VLSI Design) | VIT University | GPA : 8.23/10.
- 2010-2014 | B.Eng (Electrical & Electronics) | Anna Univ. | GPA : 7.54/10

WORK EXPERIENCE

- **QUALCOMM - ENGINEER I (GPU IMPLEMENTATION) (CONTRACT)** **March '19 - Present**
  Was responsible for the floor planning, placement of the GPU design blocks for area and congestion reduction. Major challenges include - Floor-planning for maximising effective standard cell placement area, and optimising the wire length. Fixing critical DRC's like overlaps, pin violations (both block pins and macro pins), checking un-connected instances, adding manual routes, creating placement blockages over the macros, checking power hookups of macros, placement of the macros for proper power switch insertion, macro alignment, fixing the exact power boundary, creating custom scripts for automating the runs, Block Area Reduction, fixing power switch coverage violation, querying the dB using dbTCL, creating various runs to arrive on the optimal utilisation, enabling local skew for CTS optimisation, allowing setup to degrade to fix hold, path grouping, changing cell list for CTS, ESD Cell Insertion, Congestion Removal, ECO Fixes, Timing closure and MSCTS. Design specs — 11nm design; 3 power domains, 134 Hard Macros, 1GHz Freq, 2.2 sq. mm area, 2.2 Mn instance count and 74.8% utilisation.
- **Si2CHIP TECHNOLOGIES - DESIGN ENGINEER (DMA_MAC IMPLEMENTATION)** **May '18 - March '19**
  Was responsible for the implementation of DMA_MAC block from floor-planning, placement, clock tree synthesis, routing and Timing Closure. Major challenges include Power Planning the design and Timing Closure. Design Specs — 45nm design, 7 hard macros, 500MHz Freq, 37K instance count.
- **DXCORR HARDWARE TECHNOLOGIES - VLSI ENGINEER (SILICON DEBUG)** **June '17 - May '18.**
  Major responsibilities include Silicon debugging of memory IPs using test codes developed on an FPGA.

RESEARCH/ ACADEMIC PROJECTS

- **LAYOUT GENERATION ENGINE —** A tool to generate layouts for std cells and then for analog IP's.
- **BITMAPPER INT. TECHNOLOGIES - HARDWARE INTERN** **Aug '16- June '17**
  Design of a Partial Discharge Detector using Xilinx FPGAs. Client - **TENEGA NATIONAL, MALAYSIA.**
- **ALGORITHM IMPLEMENTATION AND CASE STUDY**
  Study of common algorithms in Physical Design (Pin Placement, Maze Routing, Track Assignment) and implementation of Path Finding Algorithm and Tower of Hanoi Problem.
- **ADVANCED STA**
  Detailed analysis of each and every case in STA and Debug on Innovus. (gen_clk, mcp's, crpr, interpolation techniques, crosstalk analysis, constraints development, OCV's etc.)

COMPUTER SKILLS

DESIGN TOOLS - INNOVUS & ICC2.
PROGRAMMING/SCRIPTING - CPP, dbTCL & TCL.
TIMING ANALYSIS - ADVANCED LEVEL PROFICIENCY.

ACHIEVEMENTS

- Published articles on "Preparation Strategy for VLSI-CAD and STA jobs" on careerhigh.in. A research proposal on writing/building a "STA Engine" was accepted by a professor from IIT-Madras.
- Rank-3000. CodeZen Programming Platform & qualified IIIT-Hyderabad PGEE.

EXTRA-CURRICULAR ACTIVITIES

- Design Review Project. [Teacher Transfer Portal, BCG & Govt. of Odisha] & design of Pitch Video for launch of in-house startup at VIT (Social Networking Site for VITians).