SETHUPATHI BALAKRISHNAN b.sethupathi@gmail.com | 7845844568

An experienced professional seasoned in Physical Design and STA & interested in VLSI CAD Research looking for a full time position at a leading Semiconductor organisation.

EDUCATION

- 2015-2017 | M.Tech (VLSI Design) | VIT University | GPA : 8.23/10.
- 2010-2014 | B.Eng (Electrical & Electronics) | Anna Univ. | GPA : 7.54/10

WORK EXPERIENCE

- **NTU-TAIWAN - EDA RESEARCHER** **Jan '21 - Present**
  Major responsibilities include research and implementation of Novel Routing/Placement Algorithms for performance and area optimisation.
- **QUALCOMM - ENGINEER I (GPU IMPLEMENTATION) (CONTRACT)** **March '19 - Sept '20**
  Was responsible for the floor planning, placement of the GPU design blocks for area and congestion reduction. Design specs — 11nm design; 3 power domains, 134 Hard Macros, 1GHz Freq, 2.2 sq. mm area, 2.2 Mn instance count and 74.8% utilisation.
- **Si2CHIP TECHNOLOGIES - DESIGN ENGINEER** **May '18 - March '19**
  Was responsible for the implementation of DMA_MAC block from floor-planning, placement, clock tree synthesis, routing and Timing Closure. Major challenges include Power Planning the design and Timing Closure. Design Specs — 45nm design, 7 hard macros, 500MHz Freq, 37K instance count.
- **DXCORR HARDWARE TECHNOLOGIES - VLSI ENGINEER (SILICON DEBUG)** **June '17 - May '18.**
  Major responsibilities include Silicon debugging of memory IPs using test codes developed on an FPGA.
- **BITMAPPER INT. TECHNOLOGIES - HARDWARE INTERN** **Aug '16- June '17**
  Design of a Partial Discharge Detector using Xilinx FPGAs. Client - **TENEGA NATIONAL, MALAYSIA.**

RESEARCH PROJECTS

- **LAYOUT GENERATION ENGINE (EDA)—** An attempt to generate layouts for std cells and then for analog IP's . GitHub Link — **https://github.com/sethupathib/vsdGraphExtractor**
- **ALGORITHM IMPLEMENTATION AND CASE STUDY**
  Study of common algorithms in Physical Design (Pin Placement, Maze Routing, Track Assignment) and implementation of Path Finding Algorithm.
- **ADVANCED STA**
  Detailed analysis of each and every case in STA and Debug on Innovus. (gen_clk, mcp's, crpr, interpolation techniques, crosstalk analysis, constraints development, OCV's etc.)

COMPUTER SKILLS

DESIGN TOOLS - INNOVUS & ICC2.
PROGRAMMING/SCRIPTING - CPP, dbTCL & TCL.
TIMING ANALYSIS - ADVANCED LEVEL PROFICIENCY.

ACHIEVEMENTS

- My Git Repo (https://github.com/sethupathib/Answers) has been picked up as a data point by researchers from ETH Zurich.
- Recorded and Published tutorials on the usage of ALIGN (Analog Layouts Intelligently Generated from Netlists). (ALIGN is an Open Source Analog Layout Generation Engine).(https://rb.gy/f8gcri).
- Published articles on "Preparation Strategy for VLSI-CAD and STA jobs" on careerhigh.in. (https://rb.gy/zjqems)
- A research proposal on writing/building a "STA Engine" was accepted by a professor from IIT-Madras. I am working towards this.
- Rank-3000. CodeZen Programming Platform.
- Qualified IIIT-Hyderabad PGEE.
- Secured an 'A' in my final thesis project during Master's Program. (Awarded only to a few candidates for outstanding performance in the Internship/Project).
- Runners-Up - Logo Quiz (VIT MCQC Club)

EXTRA-CURRICULAR ACTIVITIES

- Design Review Project. [Teacher Transfer Portal, BCG & Govt. of Odisha] .
- Design of Pitch Video for launch of in-house startup at VIT (Social Networking Site for VITians).
- Written several technical & non-technical articles on medium.com (https://medium.com/@sethupathibalakrishnan) and on Quora (131K views).
- All articles can be found here —> (https://github.com/sethupathib/Answers)
- Reading & Reviewing Books —> (https://rb.gy/nawkce).
- Designing Anything and Everything —> (https://www.behance.net/bsethupathi/projects)
- Career Guidance/Mentorship to Juniors. (https://rb.gy/ta2mqz).
- Represented AECS,KK in district level Badminton Championships (Twice) & in Inter-AECS Volleyball Championships.
- My career goal is to become a EDA Researcher. I want to solve hard, open ended problems.