TurboConcept story
&
my experience as CTO

David Gnaedig

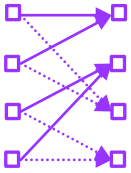
david.gnaedig@turboconcept.com

TurboConcept at a glance

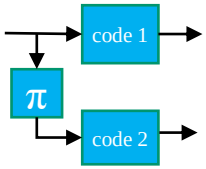
Founded in 1999 and backend by the inventors of turbo codes

A company selling IP cores for Forward Error Correction (FEC) technologies

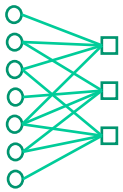
FEC technologies



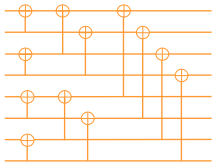
Convolutional code



Turbo codes

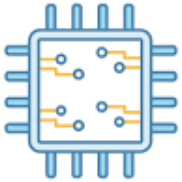


LDPC codes



Polar codes

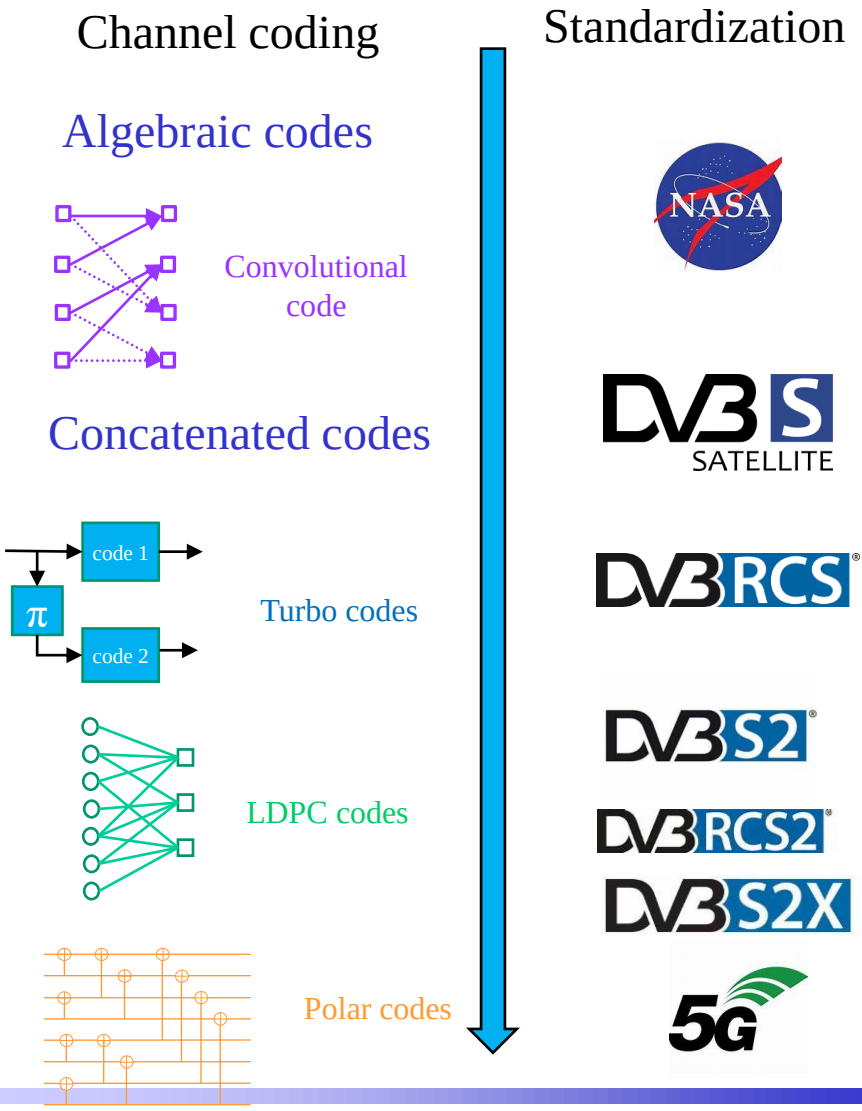
IP cores



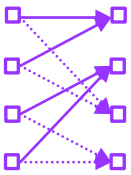
algorithm → silicon *(FPGA or ASIC)*
Hardware Description language
Software implementation

Outline

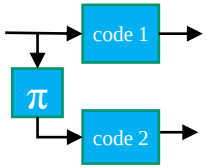
- Channel coding & FEC technologies
- IP cores
- TurboConcept creation & evolution
  - Creation & first success
  - Experimentation phase
  - Growth phase
- TurboConcept today



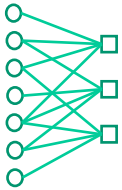
FEC technologies



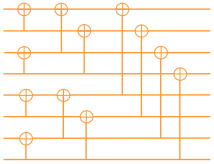
Convolutional code



Turbo codes

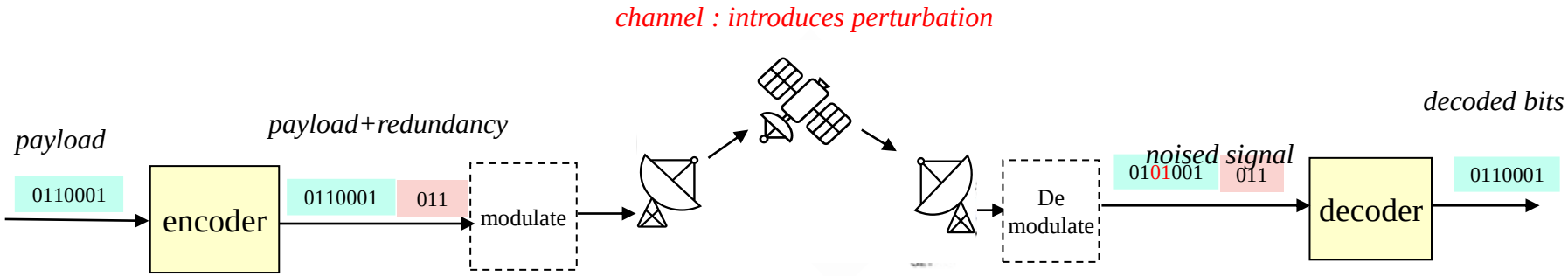


LDPC codes

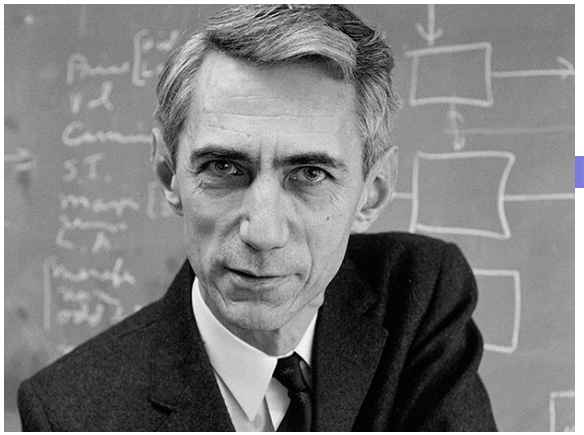


Polar codes

Channel coding

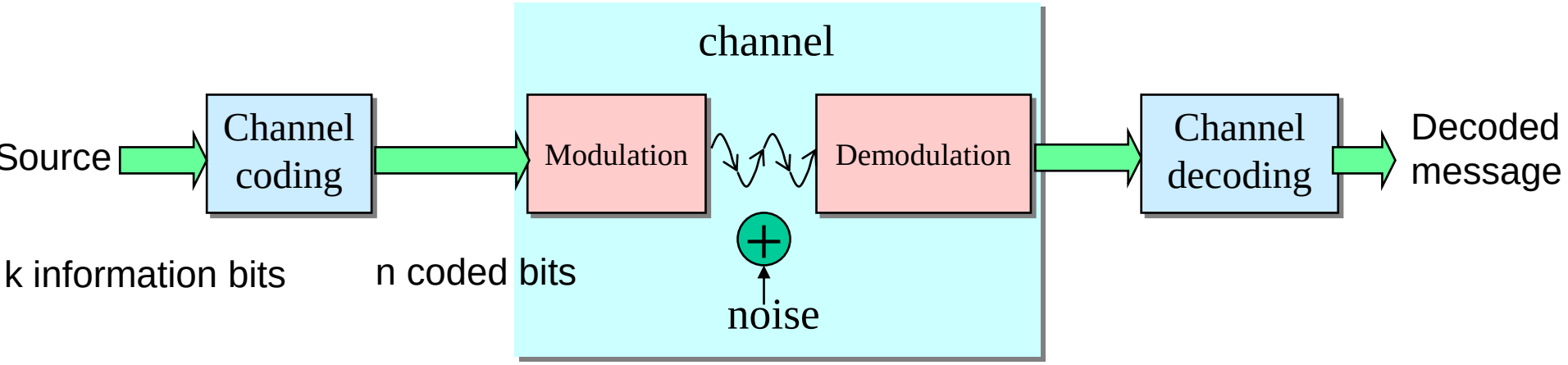


Many technologies use channel coding:



Shannon channel coding model

The father of information theory



Code rate R = k / n

Shannon coding theorem - 1948

The Noisy Channel Coding Theorem (1948)

Theorem 11. Let a discrete channel have the capacity C and a discrete source the entropy per second H. If $H \leq C$ there exists a coding system such that the output of the source can be transmitted over the channel with an arbitrarily small frequency of errors (or an arbitrarily small equivocation). If $H > C$ it is possible to encode the source so that the equivocation is less than $H - C + \epsilon$ where ϵ is arbitrarily small. There is no method of encoding which gives an equivocation less than $H - C$.

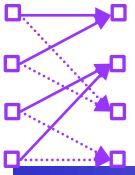
- There exists a limit to the quantifity of information that can be transmitted over a channel : the channel capacity C
- There exists channel codes that can reach asymptotically this limit with probability of error arbitrarily small

$$\exists\, C \; such \; that \; for \; R \leq C, P_e \underset{n\to\infty}{\longrightarrow} 0$$

- The proof of existence is based on random codes
- No pratical way to design such a code achieving the Shannon capacity and that can be efficiently decoded and encoded

Codes for pratical applications

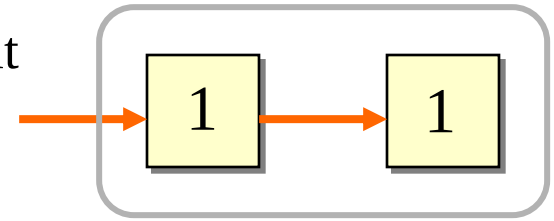
- Algebraic codes using complex mathematical modelisation
  - Hamming codes
  - BCH codes (1959- 1960) by Bose, Ray-Chaudhuri, and Hocquenghem
    - Used in DVB-S2 (satellite standard defined in 2002)
  - Reed-Muller code
    - Use in Spatial application (NASA)
    - Used in LTE & 5G specifications for short control messages
  - RS codes (1960) by Irving S. Reed and Gustave Solomon
    - A classe of BCH codes
    - Used in storage application such as CD, Blue-ray discs, …
    - Used in 2-d bar codes
    - Used in satellite application by the NASA (Voyager)
- Convolutional codes
  - Simple construction and decoding



Convolutional codes

- Invented by Peter Elias in 1955

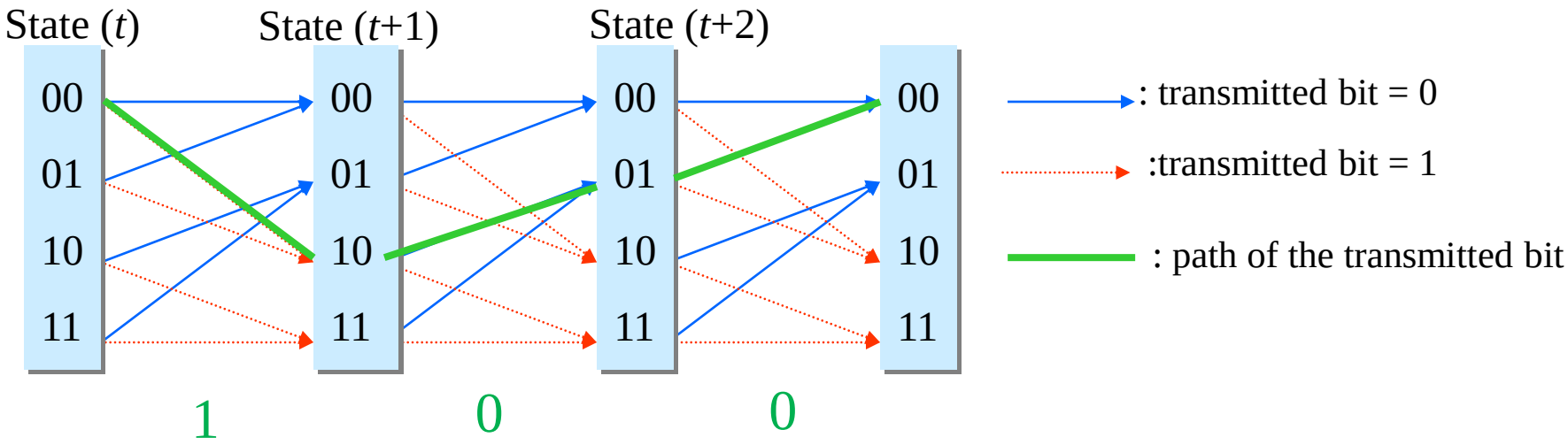
Transmitted bit



State at time *t*

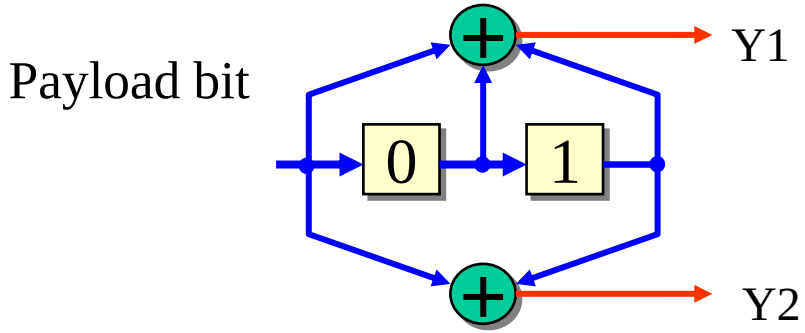
Constraint length K=3
(1 bit à transmettre + 2 bits d'état)

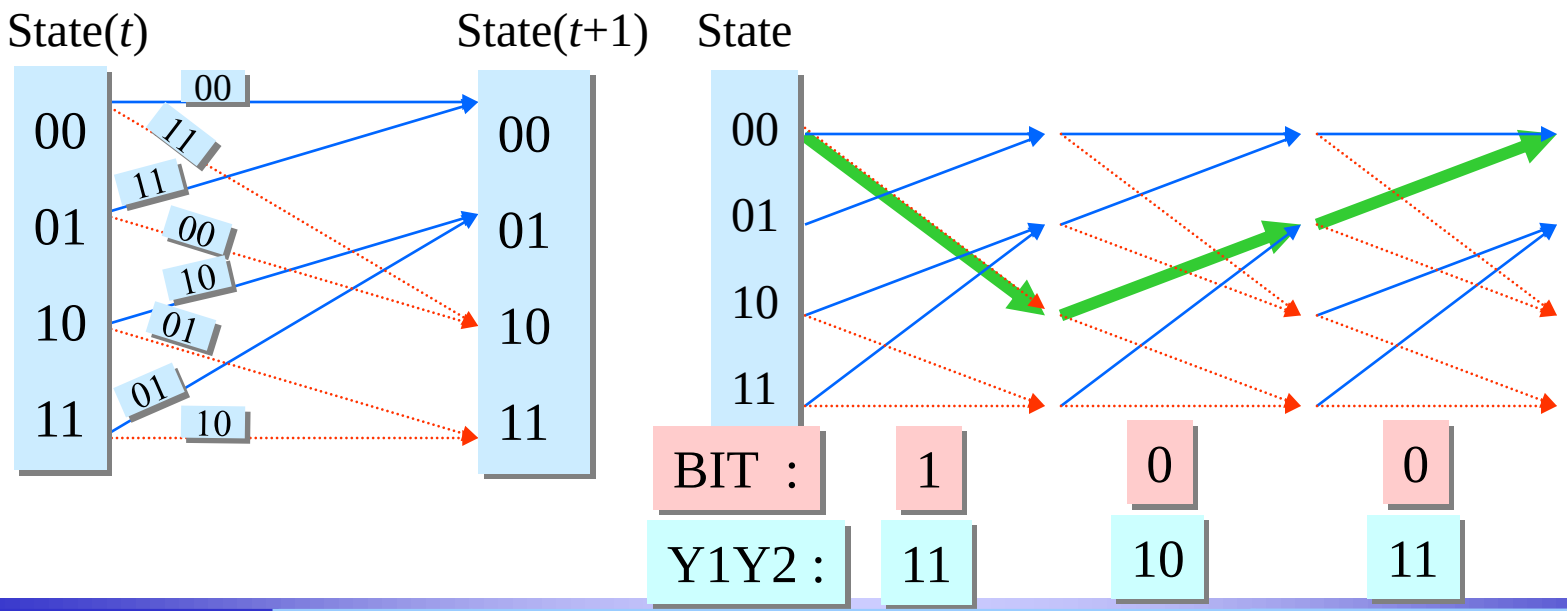
Evolution of the encoder state is represented by a trellis :



Convolutional codes

Signature of the encoder evolution:



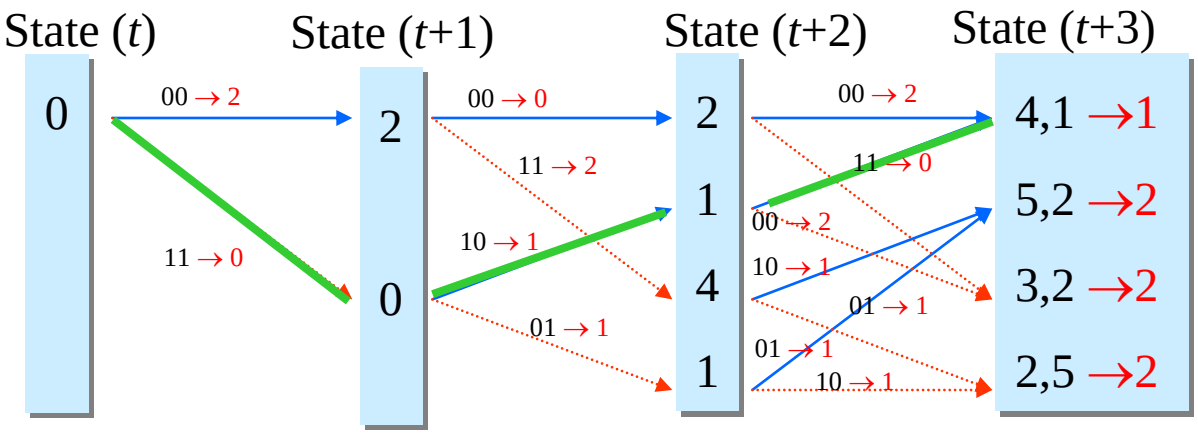


Decoding convolutional codes

- The Viterbi Algorithm (1967) :
  - ML decoding with reasonable complexity
  - Find the most likely path of the encoder in the trellis based on the channel obervations

111011→ 110011

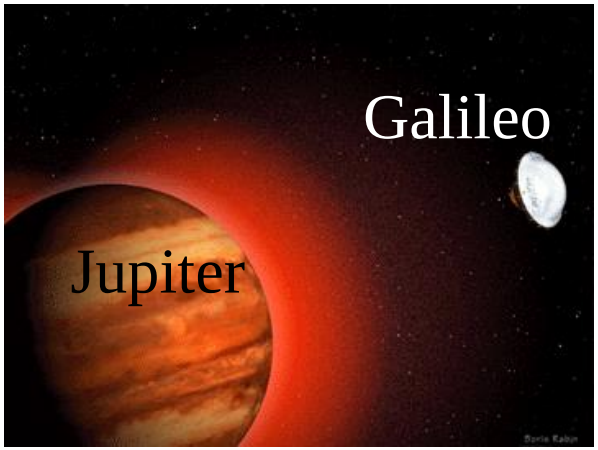
Y1Y2 :	11	00	11



Channel codes used by NASA missions

Channel coding schemes used by NASA missions[9]

Years	Code	Mission(s)
1958–present	Uncoded	Explorer, Mariner, many others
1968–1978	convolutional codes (CC) (25, 1/2)	Pioneer, Venus
1969–1975	Reed-Muller code (32, 6)	Mariner, Viking
1977–present	Binary Golay code	Voyager
1977–present	RS(255, 223) + CC(7, 1/2)	Voyager, Galileo, many others
1989–2003	RS(255, 223) + CC(7, 1/3)	Voyager
1989–2003	RS(255, 223) + CC(14, 1/4)	Galileo
1996–present	RS + CC (15, 1/6)	Cassini, Mars Pathfinder, others

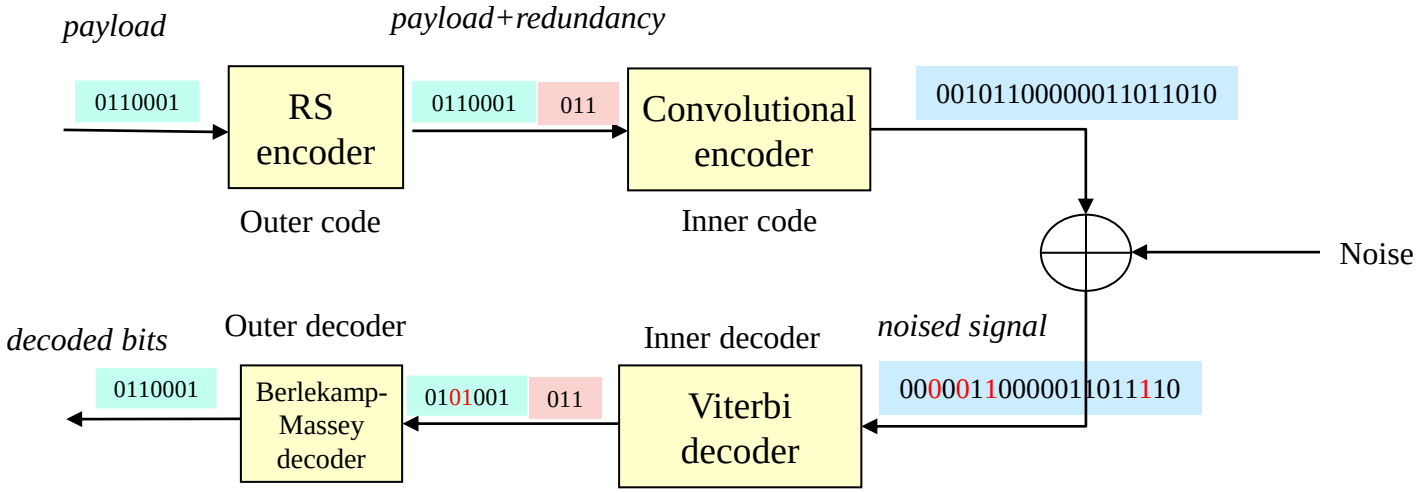


When Galileo spacecraft was launched, the decoder complexity was too high to be practically implemented

9. ^ [a] [b] Andrews, K.S.; Divsalar, D.; Dolinar, S.; Hamkins, J.; Jones, C.R.; Pollara, F. (2007). "The development of turbo and LDPC codes for deep-space applications" (PDF). *Proceedings of the IEEE*. **95** (11): 2142–56. doi:10.1109/JPROC.2007.905132. S2CID 9289140.

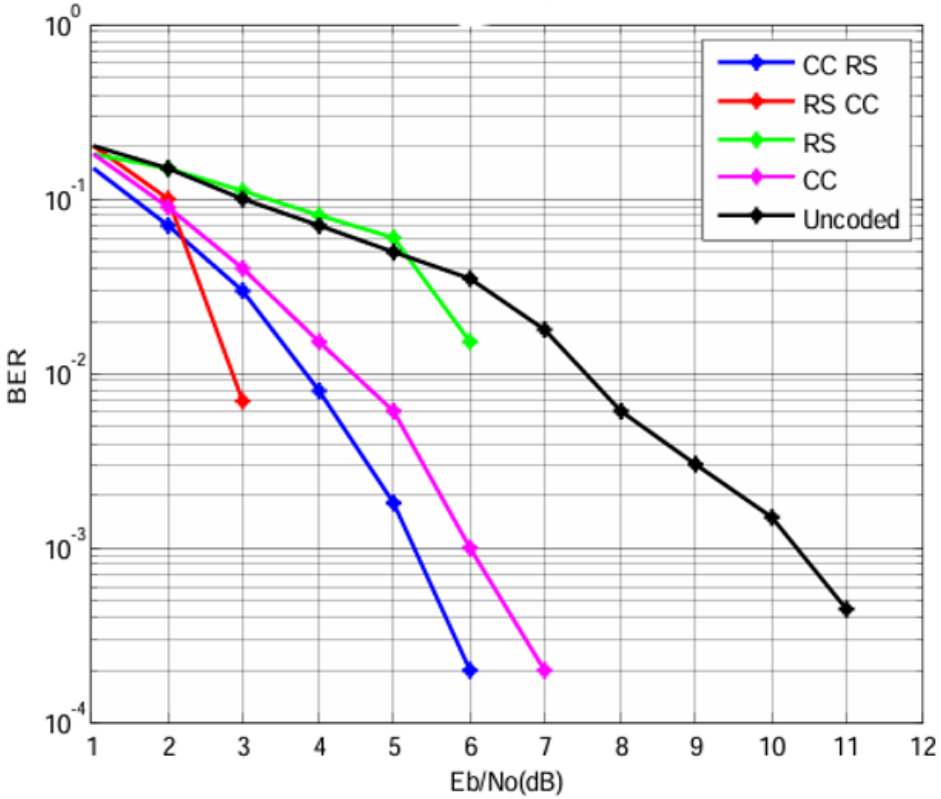
Concatenated codes (Forney 1965)

- Concatenation of two-or more simpler codes in order to achieve a powerfull composite code
  - good performance with reasonable complexity
- Concatenation of Reed-Solomon code with convolutional code
  - Errors in Viterbi decoder occurs in burst
  - RS code is very efficient to correct errors that occurs in burst
- decoding
  - Simple sequential decoding
  - but do not exploit full available information

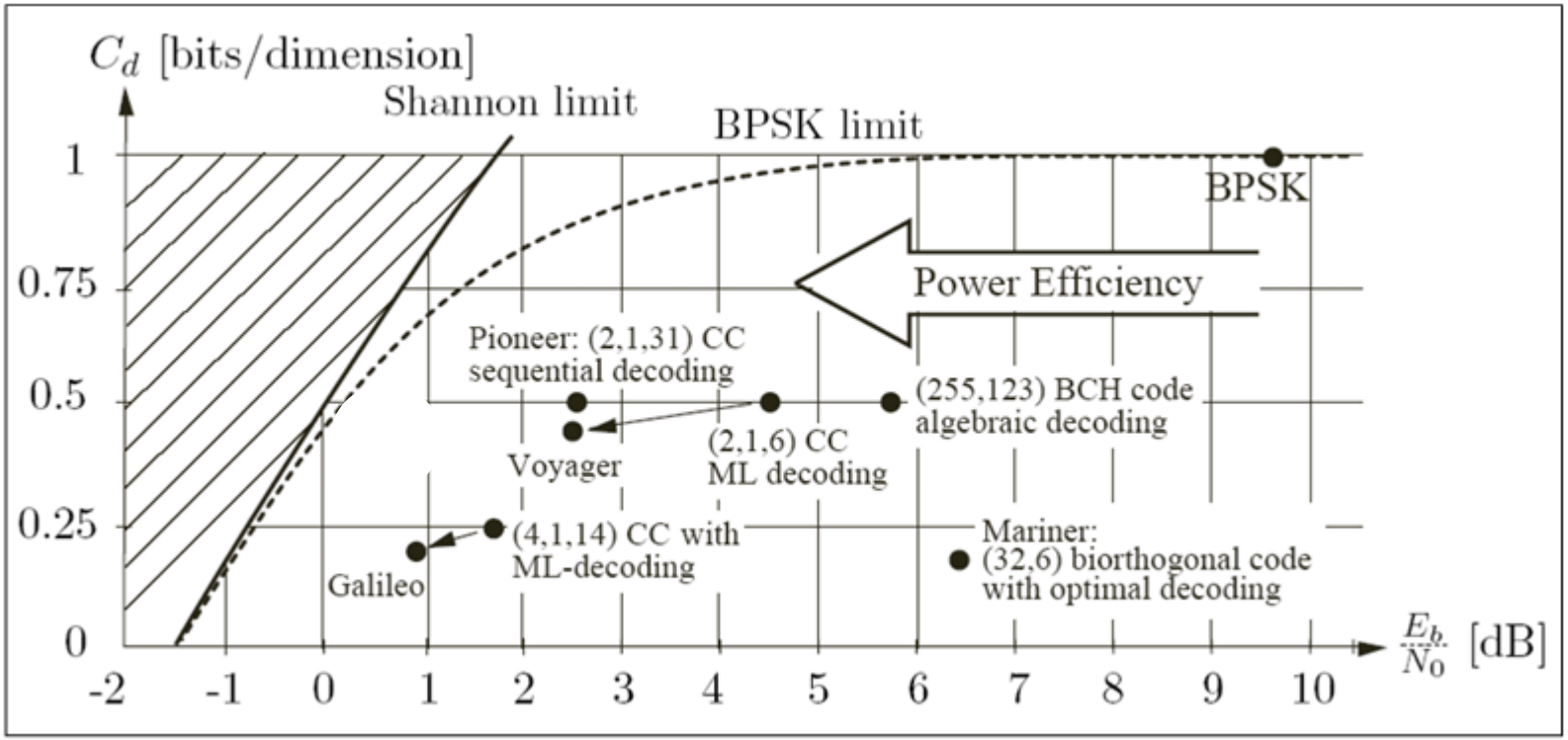


Performance of concatenated codes

- The NASA standard concatenated code
  - 64-state convolutional code
  - RS Code (256,239)
  - coding gain of more than 7 dB
- But still several dBs from the Shannnnon limit (several dBs)

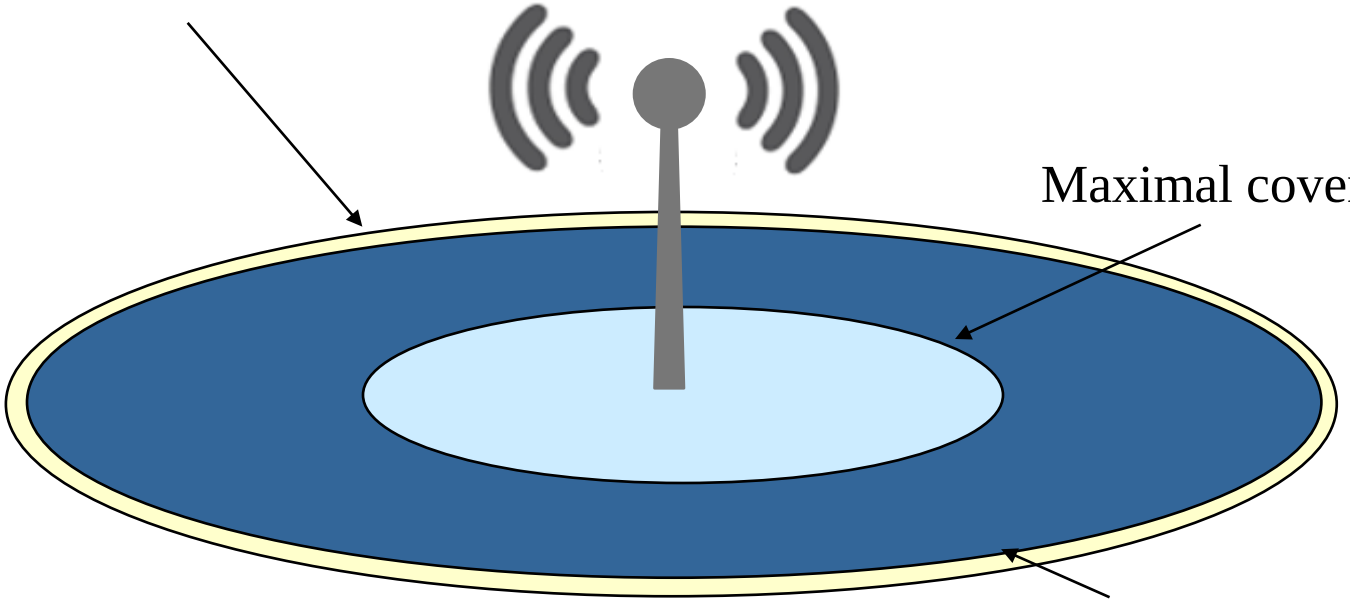


Distance to Shannon limit



Impact of channel coding on coverage

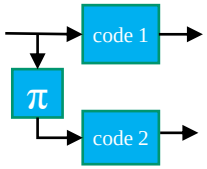
Shannon prediction (1948)
Potential coverage area



Maximal coverage in 1990

Discovery of Turbo-codes
1991-93 (Berrou Glavieux)

Starting point for the design of the capacity achieving codes

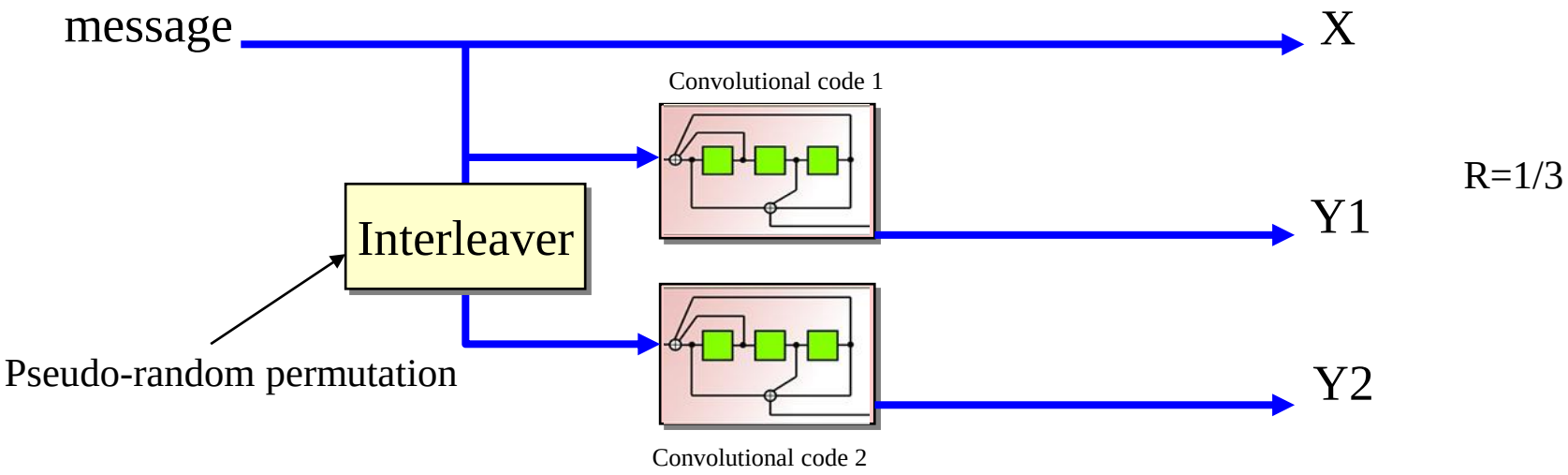


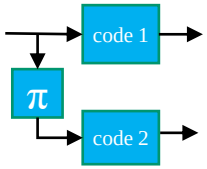
Turbo-codes

- Invented by C. Berrou and A. Glavieux in 1991 (published in 1993)
- Parallel concatenation of two convolutional codes separated by an interleaver:
  - ⊕ randomnes property of the code
  - ⊖ main constraint for the implementation
- Capacity achieving code : less than 1 dB from the channel capacity

Claude Berrou

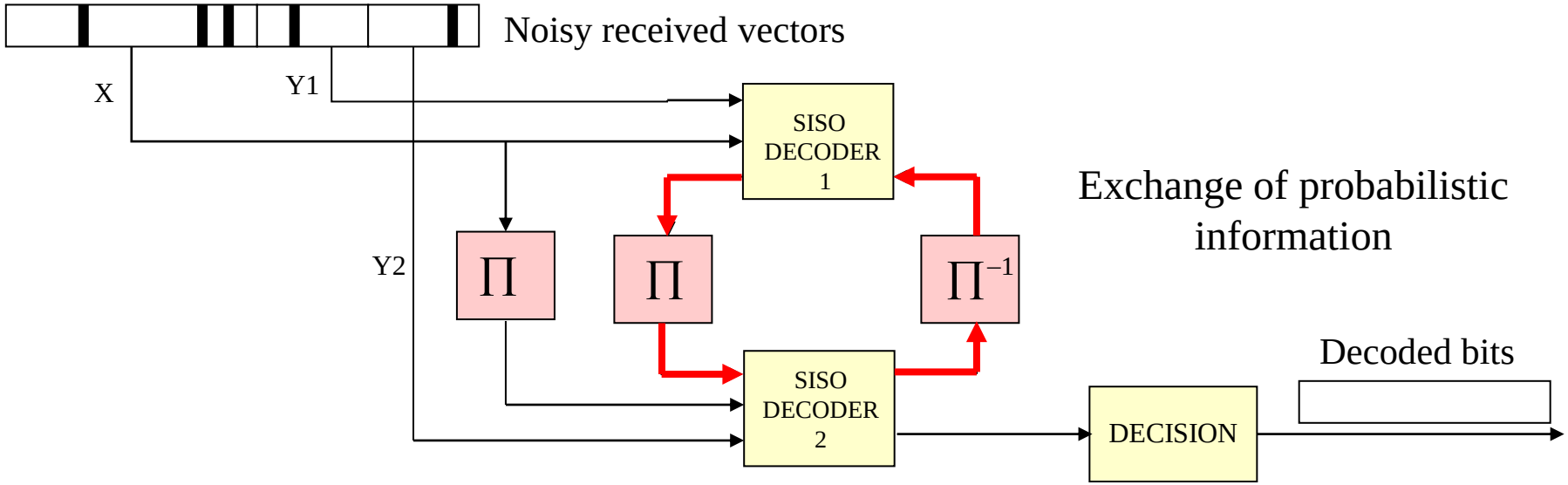
Alain Glavieux



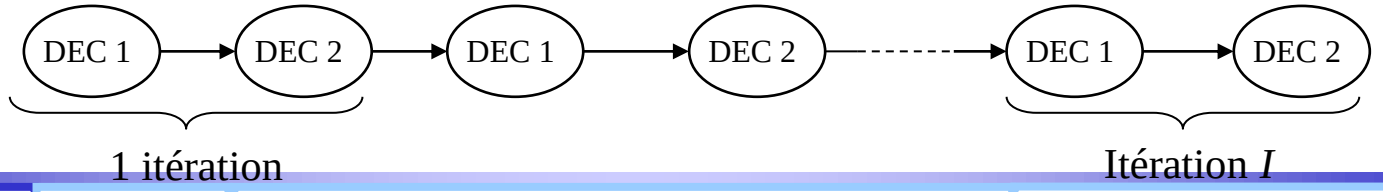


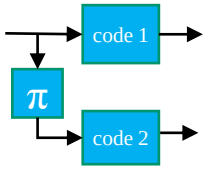
Turbo-decoding

- Iterative decoding (sub-optimal) with exchange of soft information (extrinsic)
- soft-input soft-output component decoder

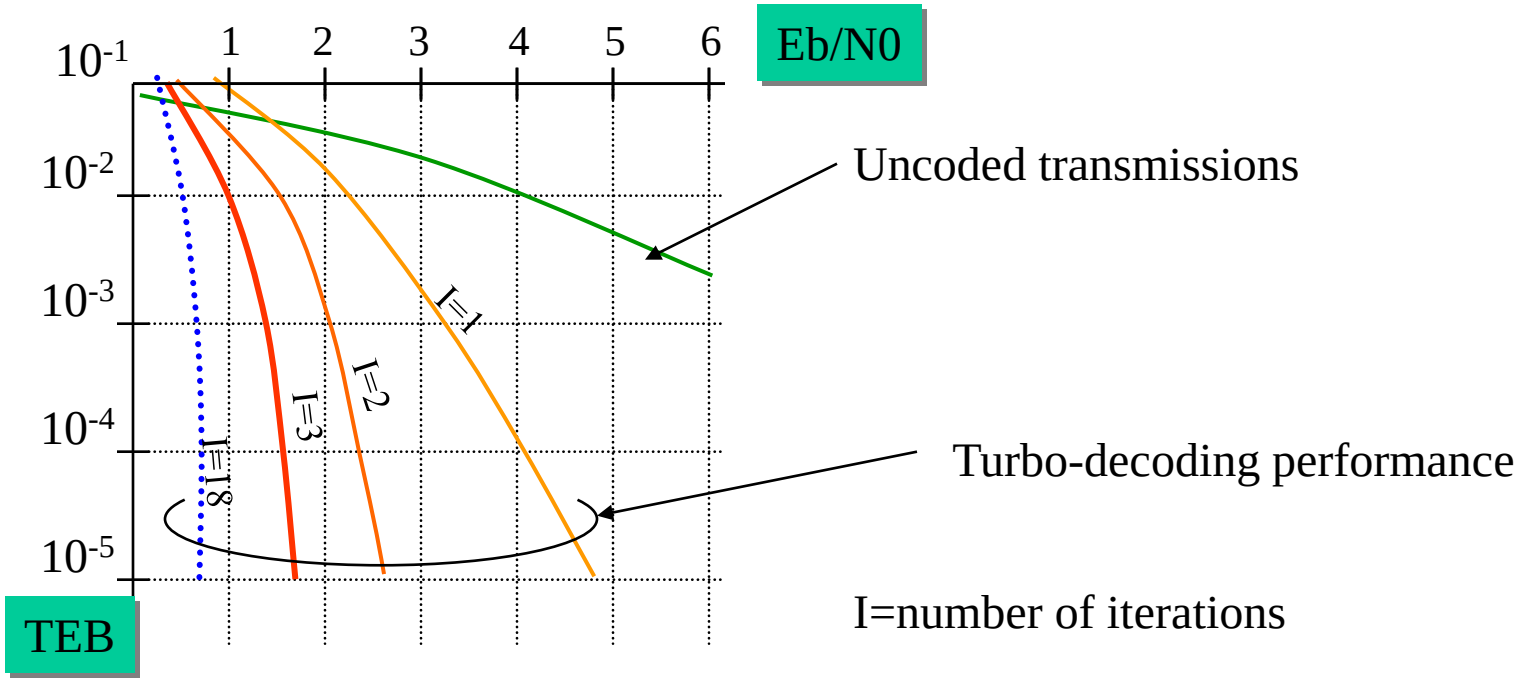


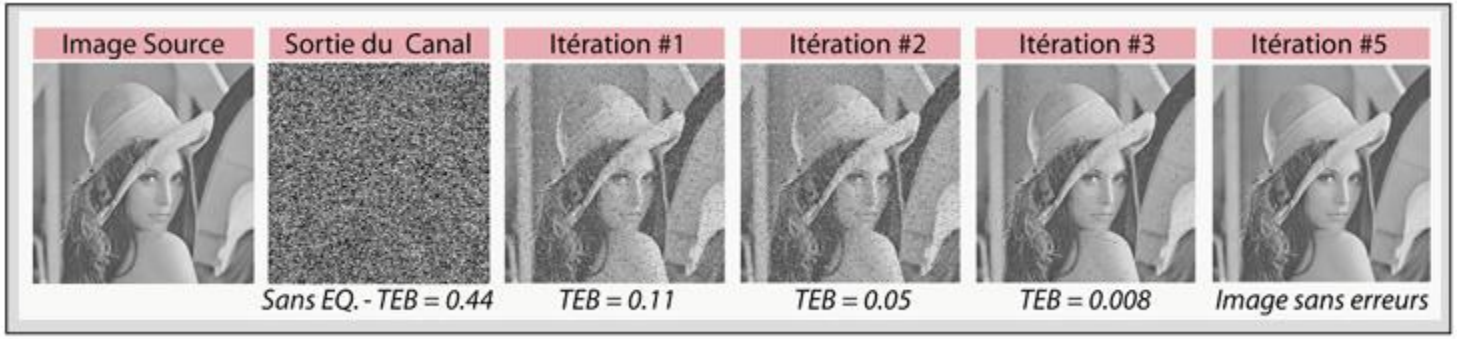
- Sequential decoding:

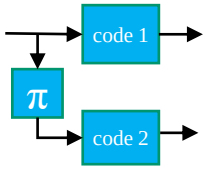




Performance of turbo codes

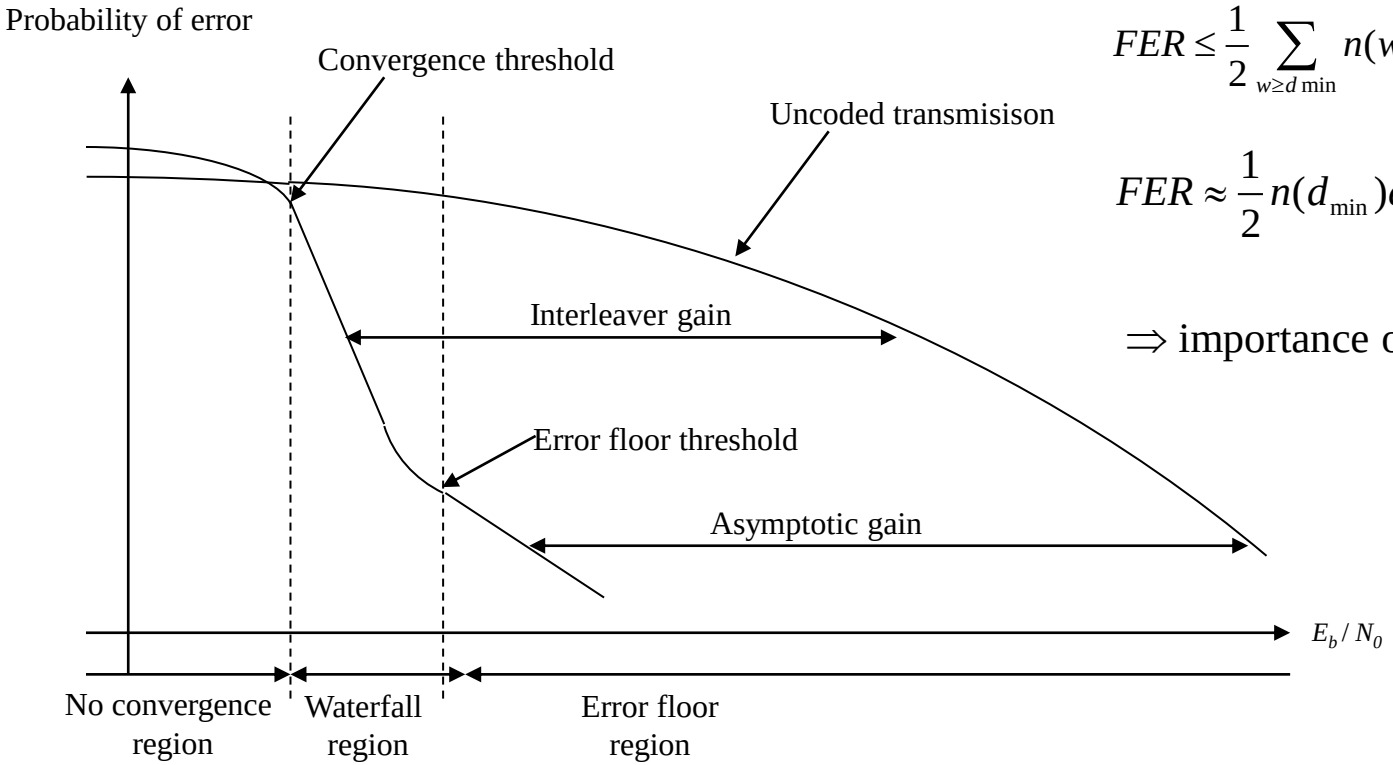






Analysis of turbo code performance

- Key component = the interleaver
  - Influence on the convergence through correlation properties between the two dimensions [Hokfelt et al.-99]
  - Influence on the asymptotic gain through the distribution of low weight codewords [Benedetto et al.-96a]

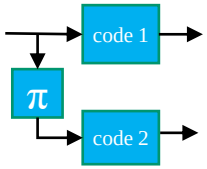


$$FER \le \frac{1}{2} \sum_{w \ge d\,\min} n(w) erfc\left(\sqrt{w \cdot R \cdot \frac{E_b}{N_0}}\right)$$

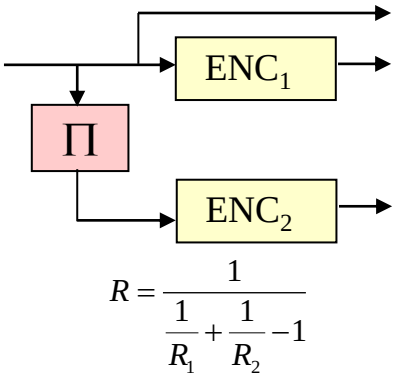
$$FER \approx \frac{1}{2} n(d_{\min}) erfc\left(\sqrt{d_{\min} \cdot R \cdot \frac{E_b}{N_0}}\right)$$

$\Rightarrow$ importance of the minimum distance

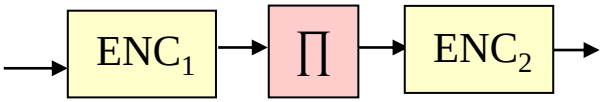
[Hokfelt et al.-99] : J. Hokfelt, O.Edfors and T. Maseng, "Interleaver Design for Turbo Codes Based on the Performance of Iterative Decoding," in Proceeding of the IEEE International Conference on Communications, ICC'99, Vancouver, Canada, Vol. 1, pp.93-97, 1999



Classes of turbo codes



$$R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} - 1}$$



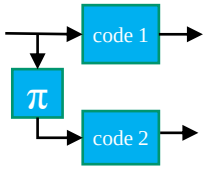
$$R = R_1 \cdot R_2$$

- Flexible : block size, code rate
- Best convergence performance at low SNRs
- Error-floor for low FERs

- Flexible : block size, code rate
- Converge at higher SNRs
- No error-floor for low FERs

- Not flexible : code rate, block size
- Low complexity decoding
- Good performance for high code rates

[Berrou et al.-96] : C. Berrou and A. Glavieux, "Near Optimum Error Correcting Coding and Decoding: Turbo Codes," IEEE Transaction on Communications, Vol. 44, No.10, pp. 1261-1271, October 1996.
[Benedetto et al.-96a] : S. Benedetto and G. Montorsi, "Unveiling turbo-codes: some results on parallel concatenated coding schemes,'' IEEE Transactions on information Theory, Vol. 42, No. 2, pp. 409--429, March 1996.
[Benedetto et al.-96b] : S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, "Serial Concatenation of Interleaved Codes: Performance Analysis, Design and Iterative Decoding," IEEE Trans. on Information Theory, Vol. 44, No. 3, pp. 909-926, May 1998

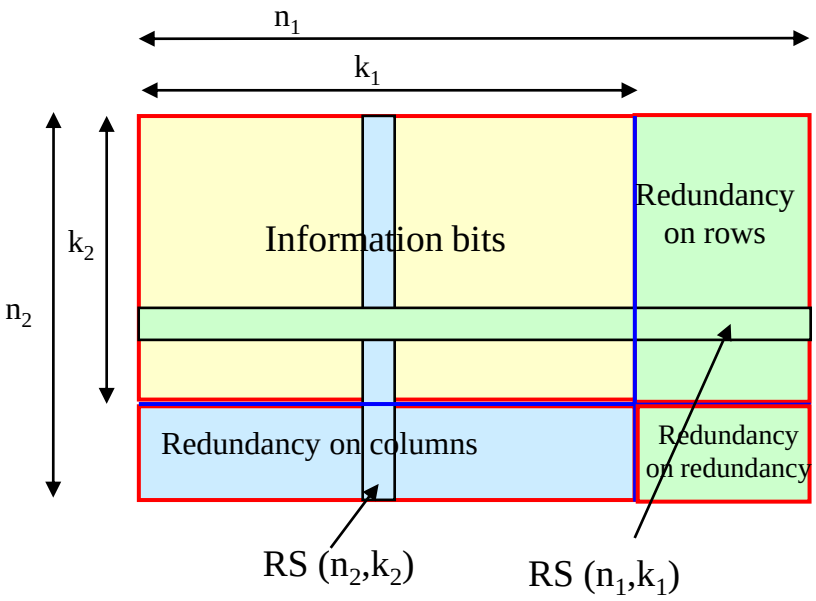


Turbo-product codes (Pyndiah, 94)

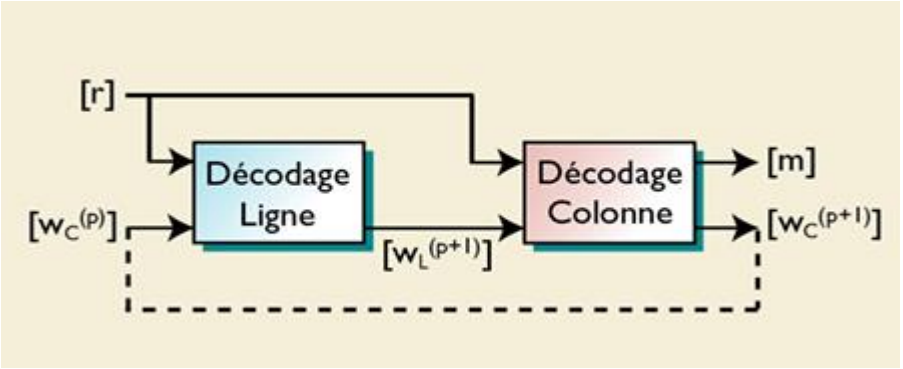
- Concatenated block code invented by P. Elias (1955)
  - serial concatenation of 2 linear code (RS) separated by a row-column interleaver

- Iterative decoding based on row-decoding followed by column decoding using a soft-in soft out algorithm (Chase Pyndiah algorithm)

Product code structure



Iterative decoding structure



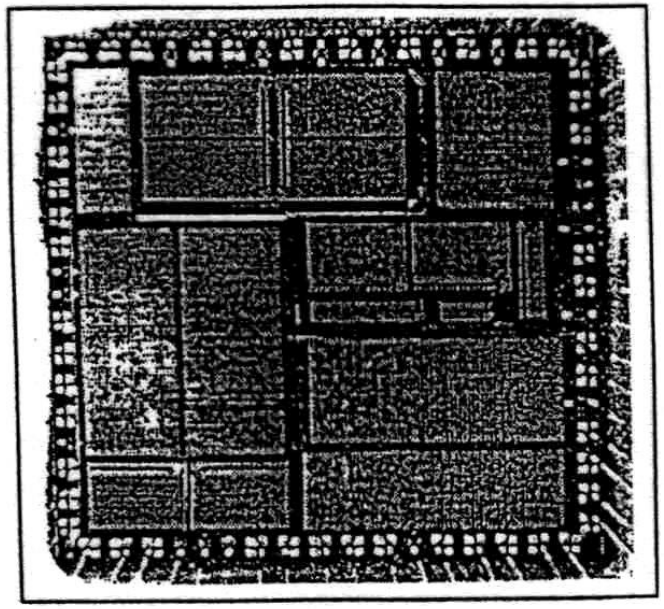
[Pyndiah et al.-94] : R. Pyndiah, A. Glavieux, A. Picart and S. Jacq, "Near optimum decoding of product codes," in Proceedings of the Global Telecommunication Conference, GLOBECOM'94, San Francisco, USA, Nov. 1994.

Valorisation of the turbo-code technology

- Intellectual property
  - Several patents owned by France Telecom (Orange)
- Hardware implementation of turbo-code / turbo-decodeur to proove that it can be actually implemented in real commercial products with reasonable complexity
  - Circuit COMATLAS CAS 5093
- Proposition of turbo-codes to standardization comittees
  - …

Turbo-code ASIC implementation (1995)

Circuit COMATLAS CAS 5093



- Turbo code avec K=4 (8-state
- Entrelacement non uniforme 32x32
- Iterative decoding using 2,5 itérations (4 SOVA + 1 Viterbi 8 state)
- 40Mbits/s
- 60000 gates+ 48K dual-port memory
- 63mm2 (techno 0,8µ)

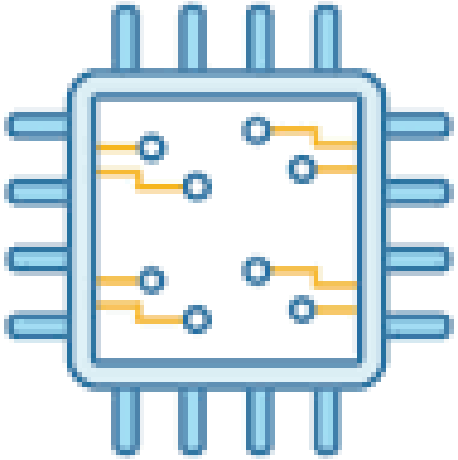
Complexity comparison:
1 circuit RS dans GF(256) ~ 50Kportes
1 circuit Viterbi 64 états ~ 50Kportes ~ 8 viterbi 8 states~ 4 SOVA 8states

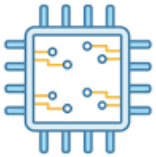
[CAS-95] : CAS 5093 40 Mb/s Turbo Code Decoder. December Rev 4.1. Comatlas. May 1995.

Valorisation of the turbo-code technology

- Intellectual property
  - Several patents owned by France Telecom (Orange)
- Hardware implementation of turbo-code / turbo-decodeur
  - Circuit COMATLAS CAS 5093
- Proposition of turbo-codes to standardization comittees
  - …
- Creation of TurboConcept …

IP cores





IPs : definition

- Intellectual Property (IP) block or IP cores:
  - is a pre-designed function to be implemented in one or more semiconductor devices such as
    - application-specific integrated circuits (ASICs),
    - application-specific standard products (ASSPs) or
    - programmable logic devices (PLDs).
- Reused over different projects
  - Inside a single development team
  - Inside a single company
  - From an external IP provider

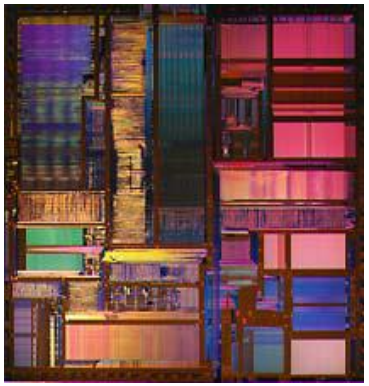
IPs : examples

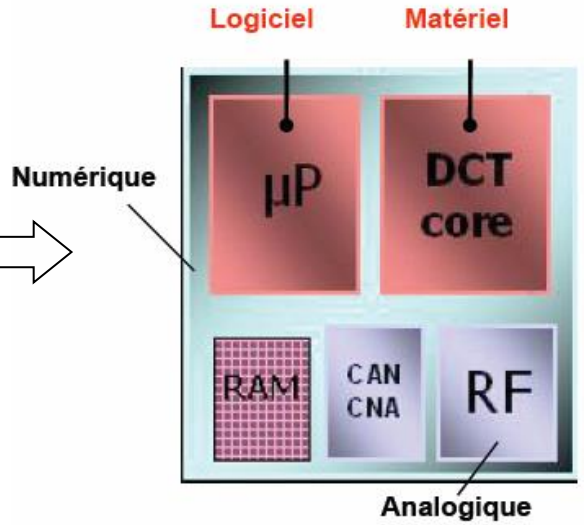
- Examples:
  - Memory : single port RAMs, dual port RAMs, SDRAM controller, …
  - Processor : RISC cores, DSP cores, …
  - Communication : PCI-Express, USB, Ethernet controller, Bluetooth, …
  - Digital Signal Processing blocks (DSP) : FFT, Viterbi decoder, Turbo Code decoder, …
  - Imaging and video : DCT, MPEG4, JPEG, …
  - Cryptography : AES, RSA, …
  - Analog : PLL, A/D converters, …

Why silicon IP's ?

- Context : SoC design
- Historial drivers
  - Technology scaling
  - Economic
- Problems with SoC design
  - Productivity
  - Product lifecycle
- Solutions for SoC design

Context : System on Chip (SoC)





SoC (system on (a) chip) :

Circuit combining several functional blocs (processor, memory, peripherals, …)
with software (SW) and hardware (HW)

SW : OS, algorithms

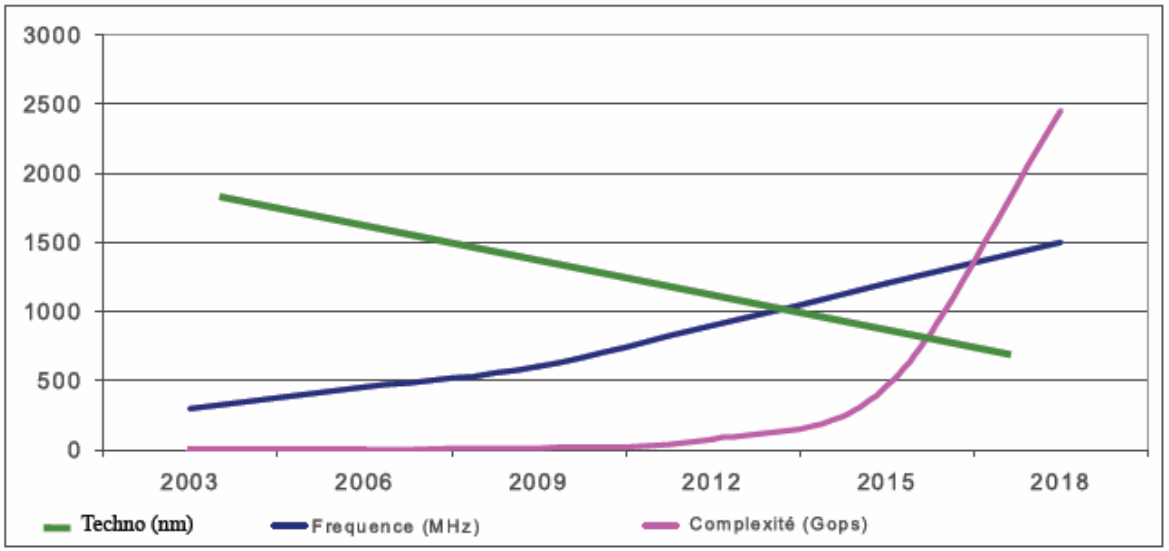
HW :

- analog (CAN,CNA, PLL, RF)
- Digital (procesor, memory, interfaces, …)

⇒ complex circuit

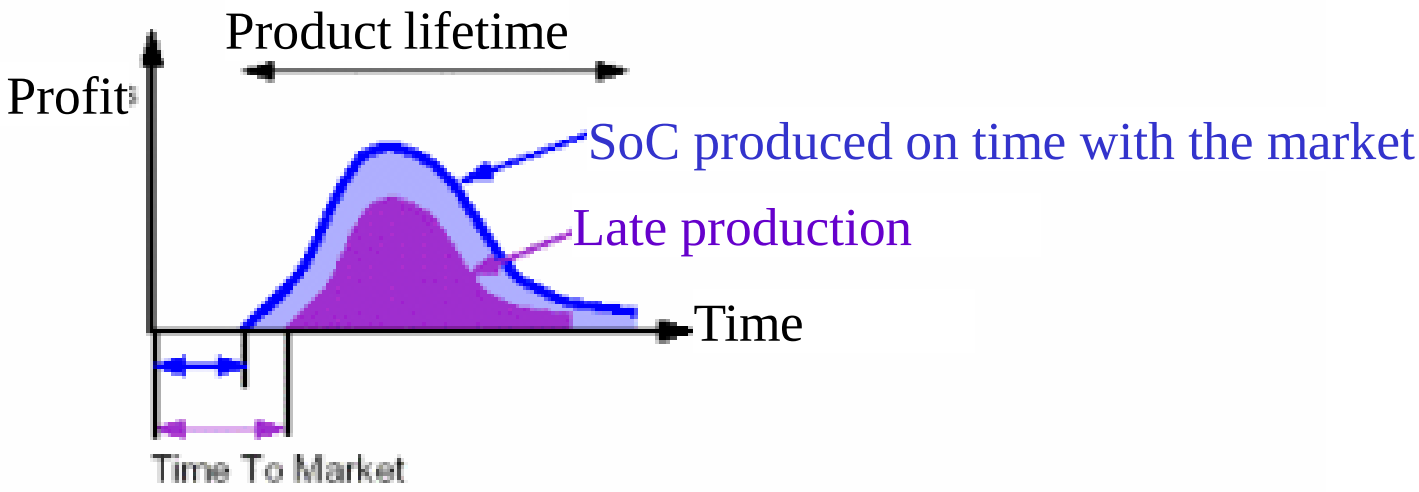
Historical drivers

- Technology : scaling
  - Moore's law : doubling of number of transistors every 2 years
    - reduction of transistors size
    - more transistors on a chip, increase of complexity
  - Reduction of transistor cost $ $0{,}05.10^{-6}$ (production)
  - Increase of clock frequency: increase performance



Historical drivers

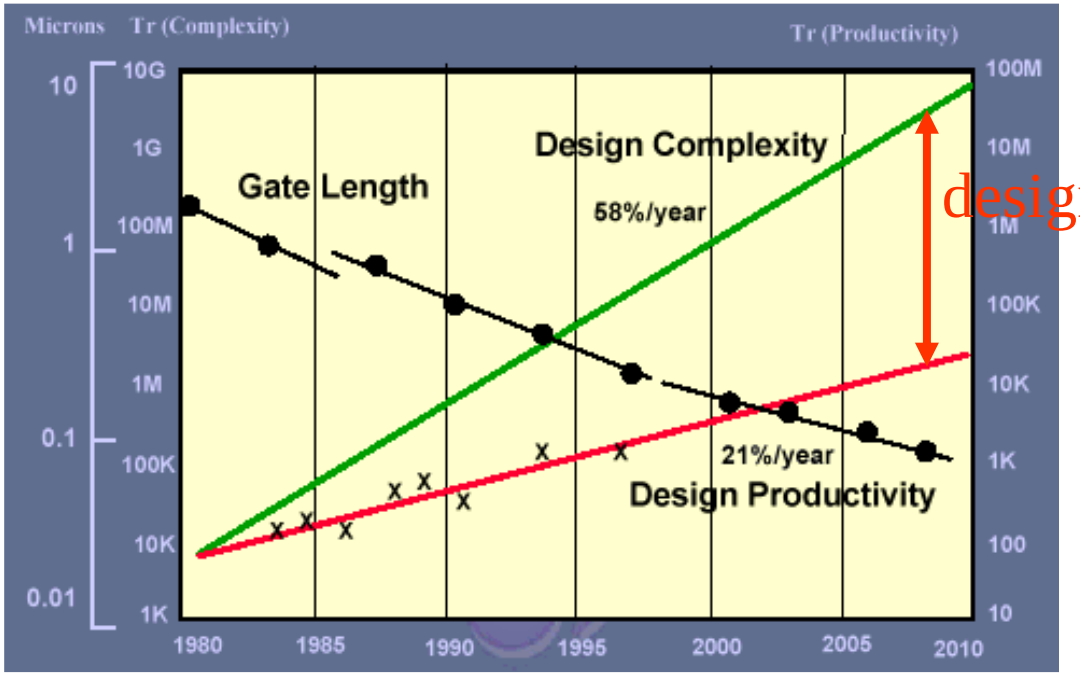
- Economic :
  - High pressure on price for products for the consumer market
  - Time-To-Market
  - Fondamental law : cost - volume



Problems with SoC design

- Productivity
  - 6000 transistors / engineer / month

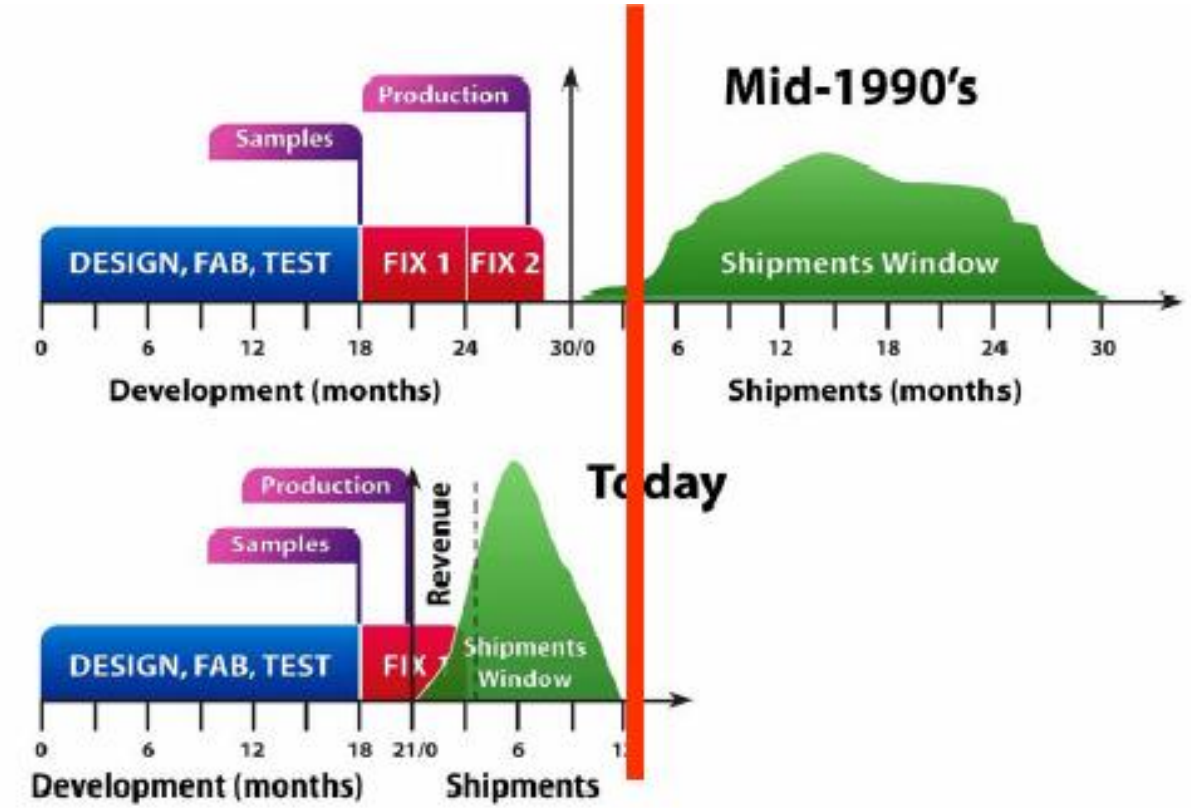
=> 140 engineer during one year for 10M gates circuit



design gap

Problems with SoC design

- Short product development cycle and product life time



SoC, solutions

- Increase abstraction level and productivity
  - High level synthesis (HLS)
  - hardware / software partitionning
  - System-level design
- "Divide an conquer"
  - Separate a complex system in smaller independent parts
  - Reuse of blocks
    - Developped internally in other projects
    - Developped by a third party provider

⇒ usage of Intellectual Property blocks (IPs)

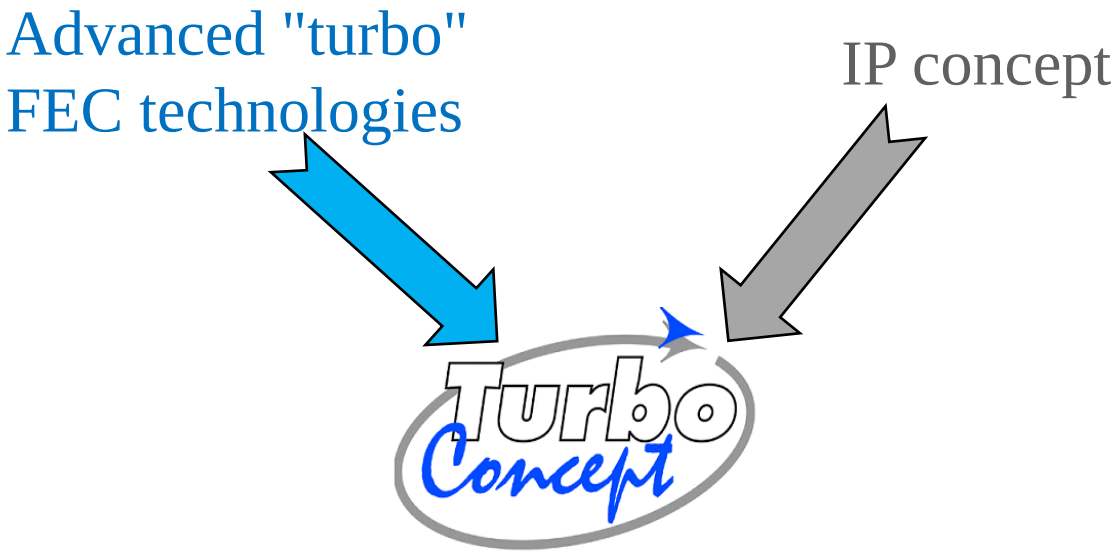
IP market

- Historical facts:
  - 1990 : first "IP" µprocessor sold : HDL System proposed a synthesizable processor : MIPS 3000 (source code VHDL-Verilog + scripts) : 256 k$
  - 1990 : Rambus developps a bus specification in order to improve the connection DRAM↔µprocesseur
  - 1991 : ARM proposes a license of the ARM6
- Today the IP market is widely developped
  - but in late 90's, it was not necessarilly the case but rather an emerging market

TurboConcept

COMPANY CREATION

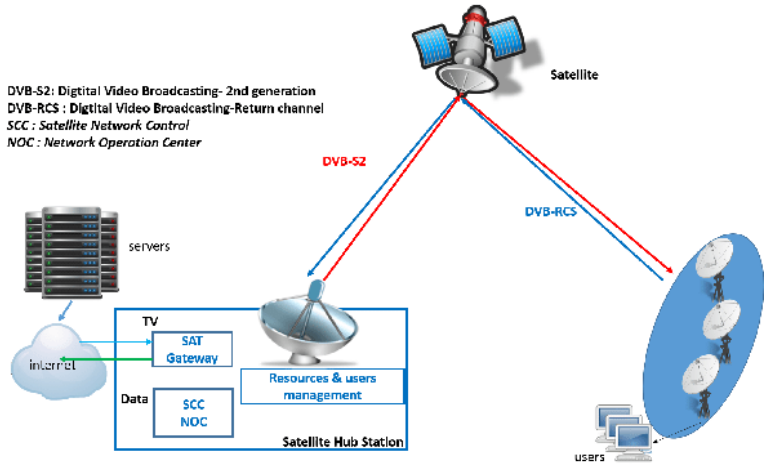
Creation of TurboConcept in 1999



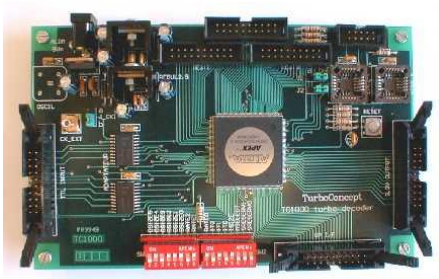
- Funded by J. Tousch and N. Brengarth as a spin-off from French University « IMT-Atlantique »
- backed by Claude Berrou, inventor of turbo-codes and professors from IMT Atlantique
- First project : FPGA demonstrator for DVB-RCS standardization commitee

DVB-RCS standardization

- Standard for Return link via satellite
  - A FPGA prototype was developed in 1999 for a demonstration to DVB members.
  - The DVB committee adopted the proposed solution, over competitor proposals
  - Competition with AHA : proposed a TPC (with ASIC implementation)
  - Double-binary turbo codes were selected by the consortium



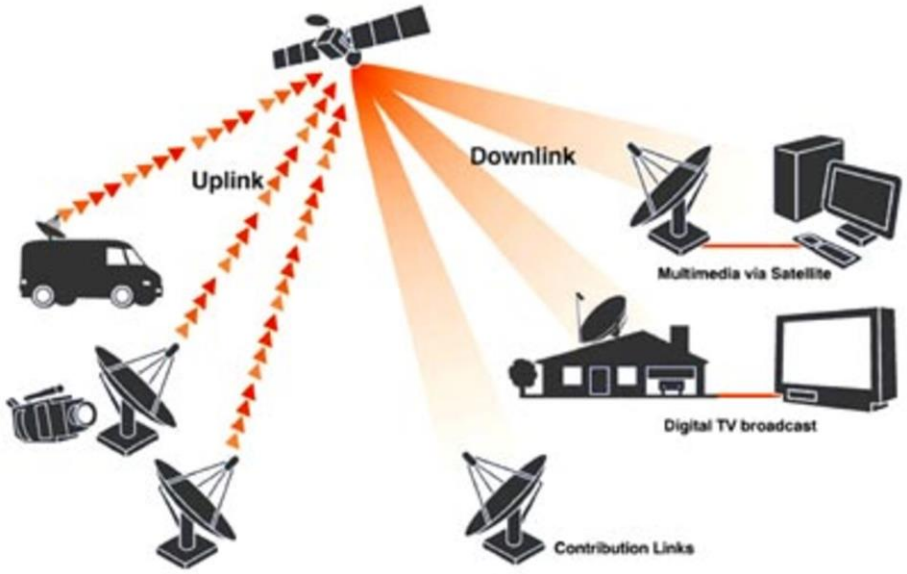
- First commercial success
  - First DVB-RCS players in the market used TurboConcept's turbo decoder



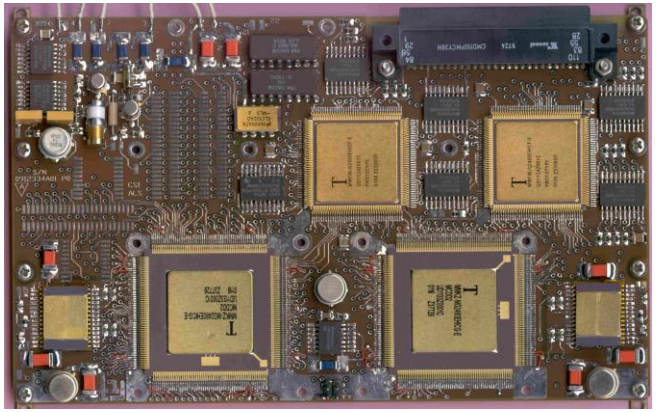
Gilat · Newtec (SHAPING THE FUTURE OF SATELLITE COMMUNICATIONS) · EMS TECHNOLOGIES · ViaSat · eutelsat COMMUNICATIONS · iDIRECT

Skyplex

- In 2000, TurboConcept designed a turbo decoder function for the Skyplex system.
  - satellite on-board DVB multiplexing system operated by Eutelsat and manufactured by Alenia Aerospazio
  - The technology is a TEMIC Gate Array ASIC.

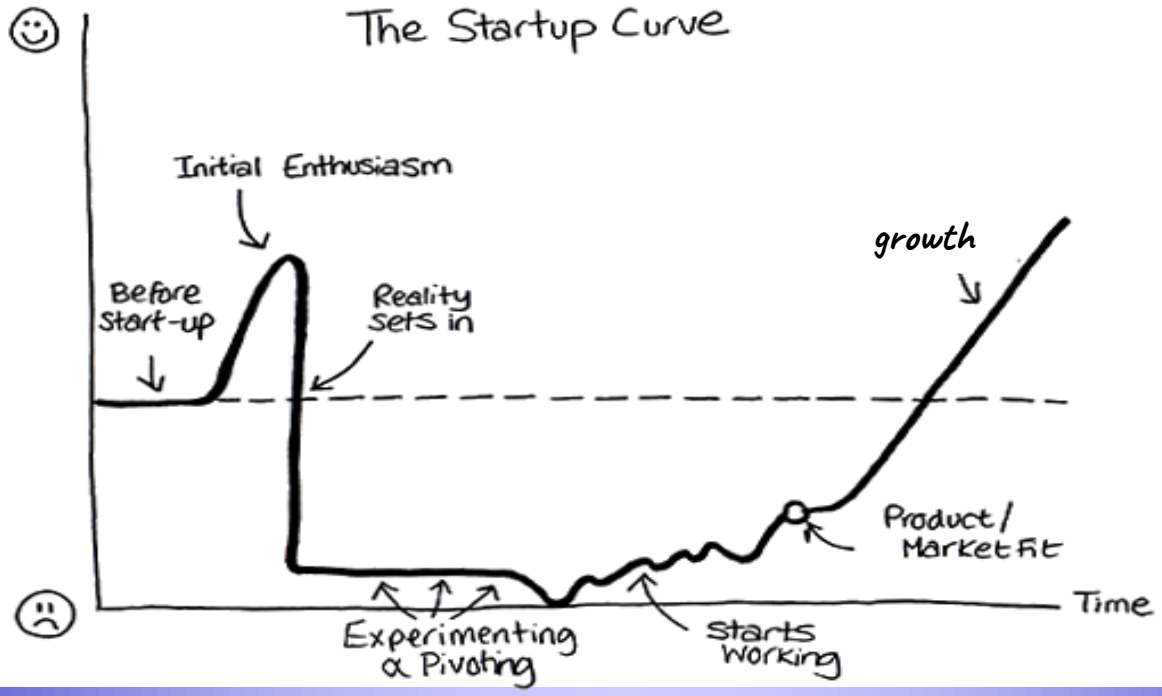


- Applications:
  - digital TV program broadcasting
  - digital radio broadcasting,
  - interactive multimedia services
  - Internet connectivity



Is TurboConcept a startup Company ?

- Startup definition:
  - A young company founded to develop a unique product or service and bring it to market.
  - Typically in the early stages of development
  - Often started by 1-3 founders who focus on capitalizing upon a perceived market demand.
  - May seek outside investment from sources like angel investors, venture capitalists, or crowdfunding.
- definitely YES

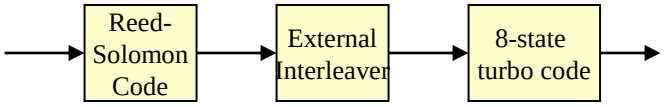


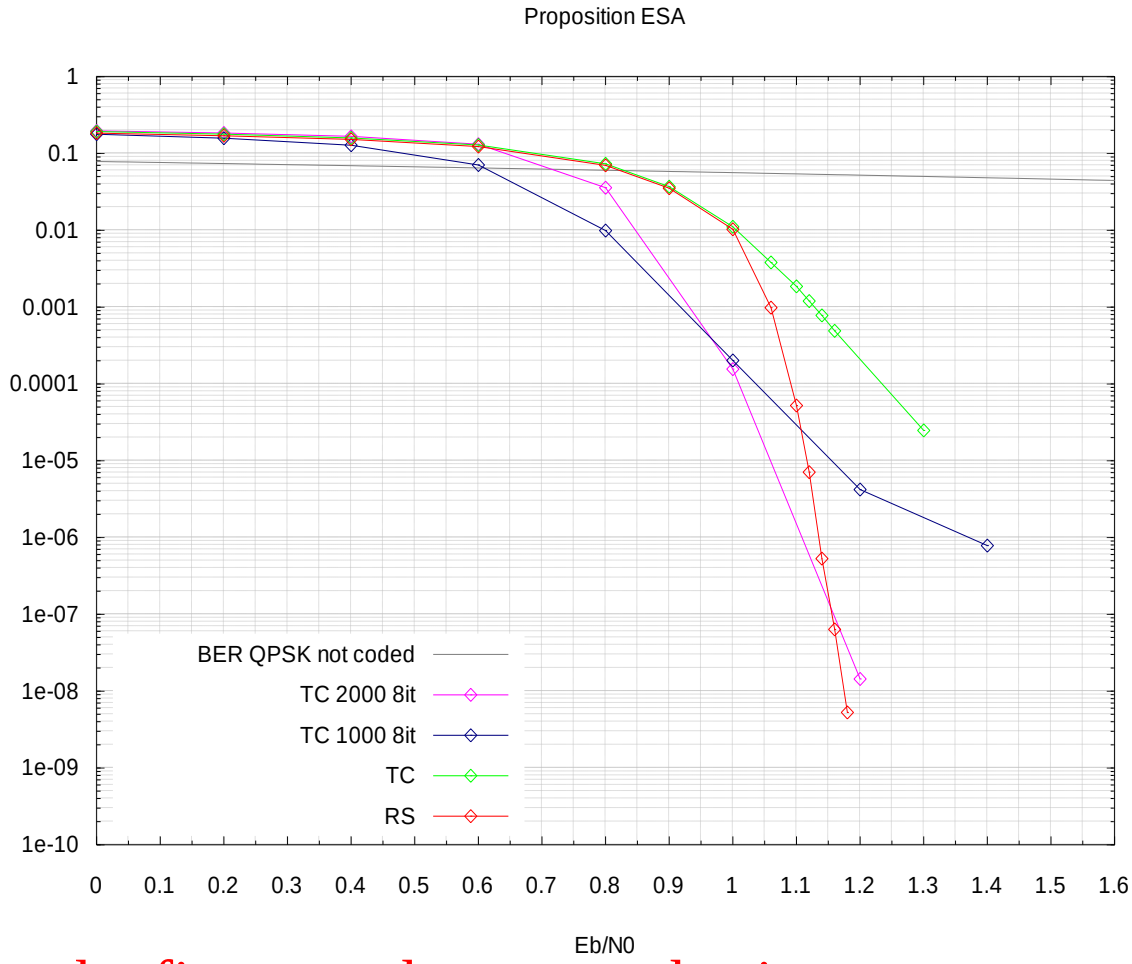
David Gnaedig - resume

- 2000 : internship at STMicro-electronics in San Diego
  - Discovering of turbo-codes and decoding through reverse engineering of
- 2001 :
  - Graduated with MSc from Telecom Paris
    - Project on Viterbi decoder
    - Specialization : micro-electronics, digital communication
  - DEA (Research master) in Communication Systems
  - Internship with UBS & TurboConcept on DVB-RCS turbo-decoder implementation (SW and HW)
- 2002 -2005 : Phd with TurboConcept to work on turbo-code design and high-speed implementation
- Since 2010 : acting as Chief Technology Officer (CTO)

DVB-S2 standardization

- In 2002, TurboConcept contributed to standardization of the DVB-S2 standard
  - Proposition of turbo-code concatenated with Reed-Solomon
- High throughput application





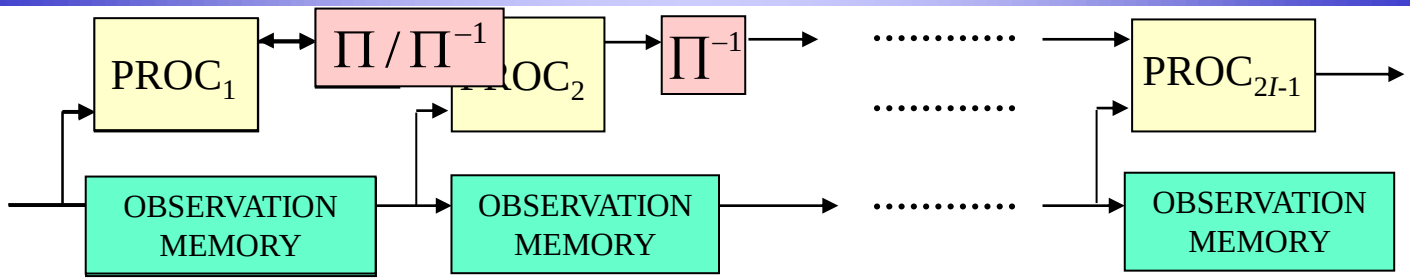
Turbo code designed during the first months on my thesis

Parallel implementation of turbo-codes

Increase processing power

Serial architecture

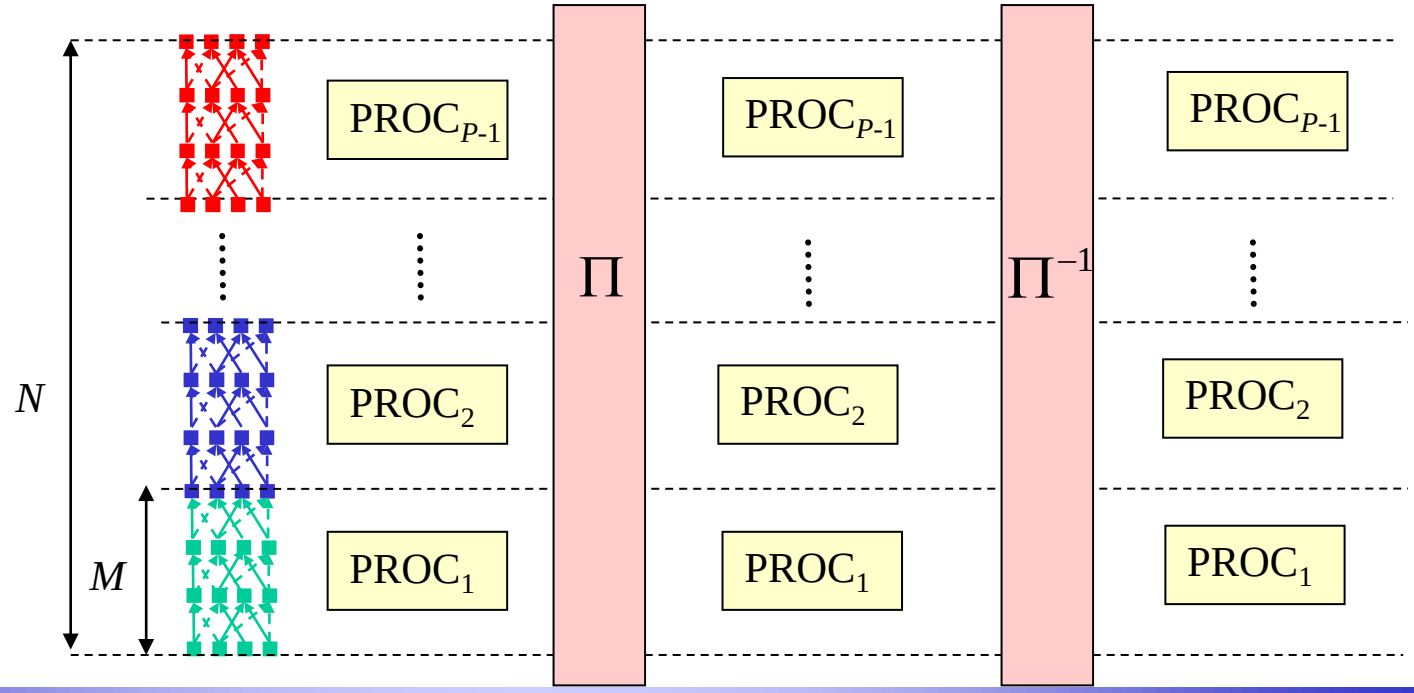
- memory duplication



Parallel architecture

- memory reduction
- latency reduction

$N = P \cdot M$

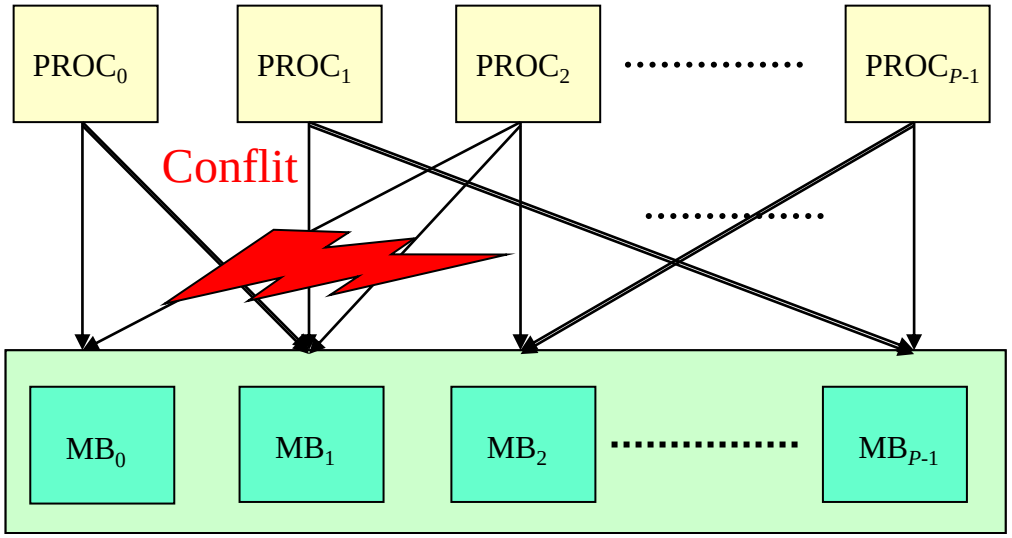


Parallel architecture

Parallel architecture

Natural order

Interleaved order



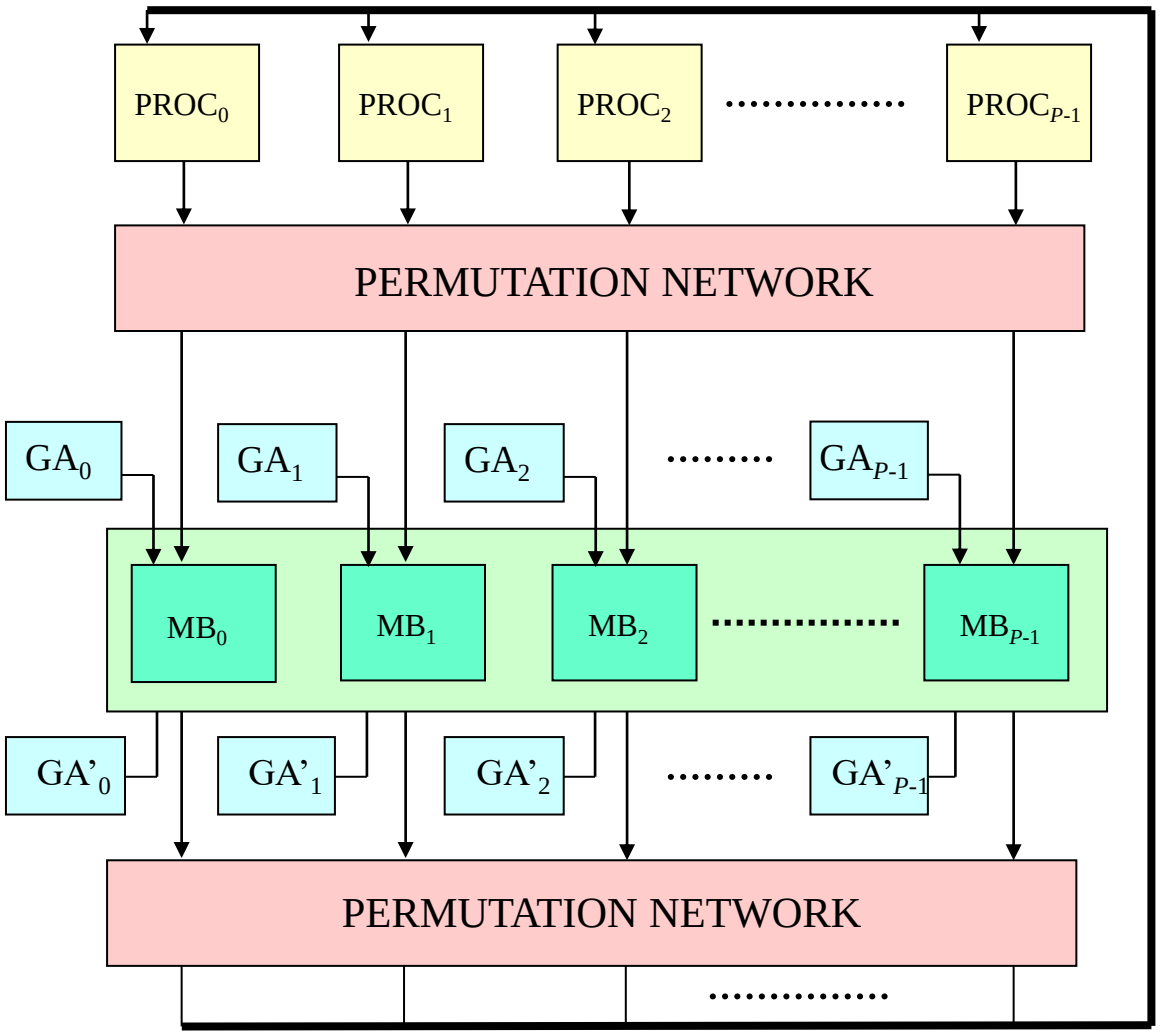
- Memory organization
- Permutation means

Parallel architecture: memory access conflicts resolution

Parallel architecture

Parallel access conflicts

- Execution
- Compilation
- Design



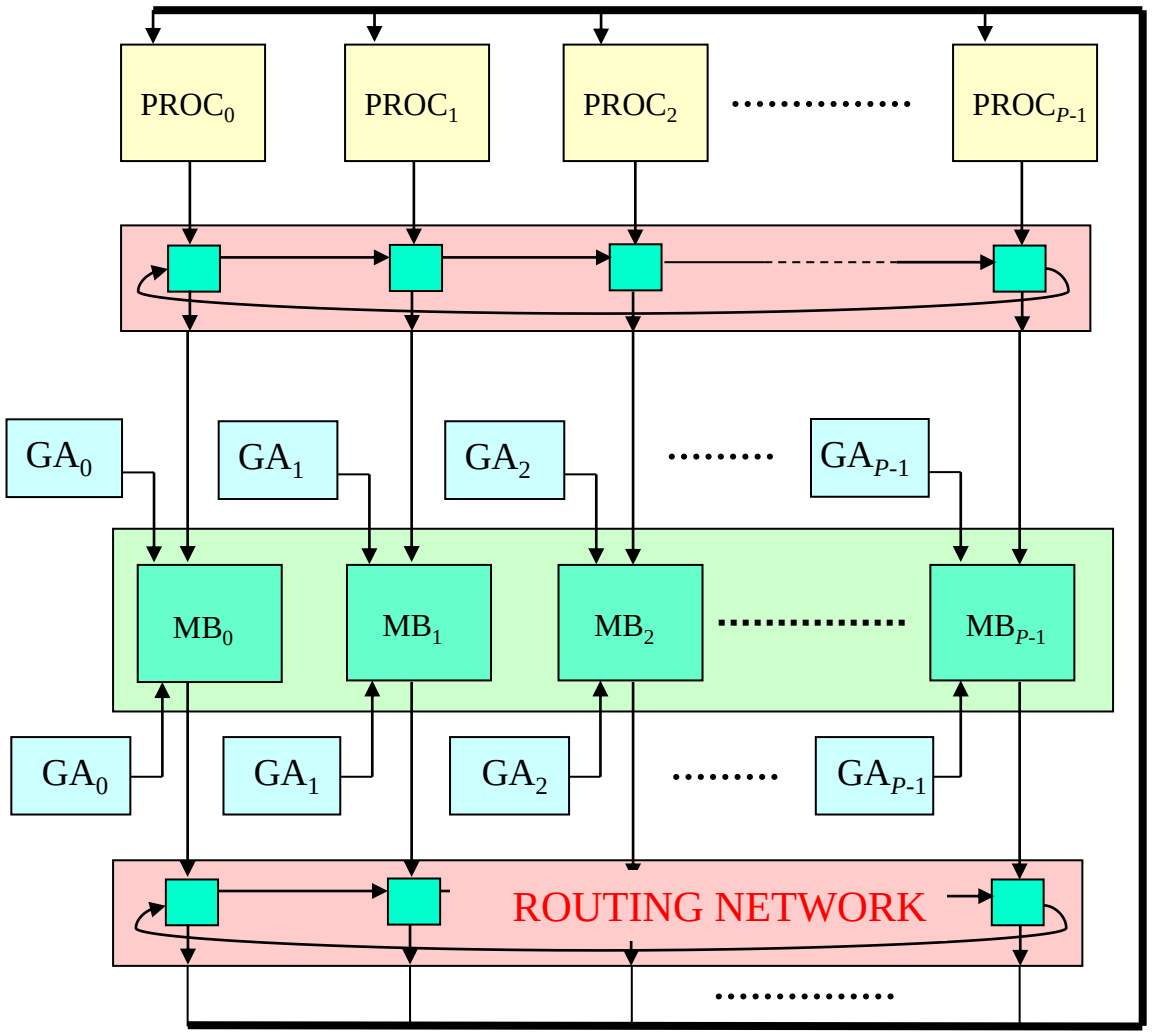
Parallel architecute: memory access conflicts resolution

Parallel architecture

Parallel access conflicts

Execution [Thül *et al.*, 2002]

High complexity:
- memory
- interconnections



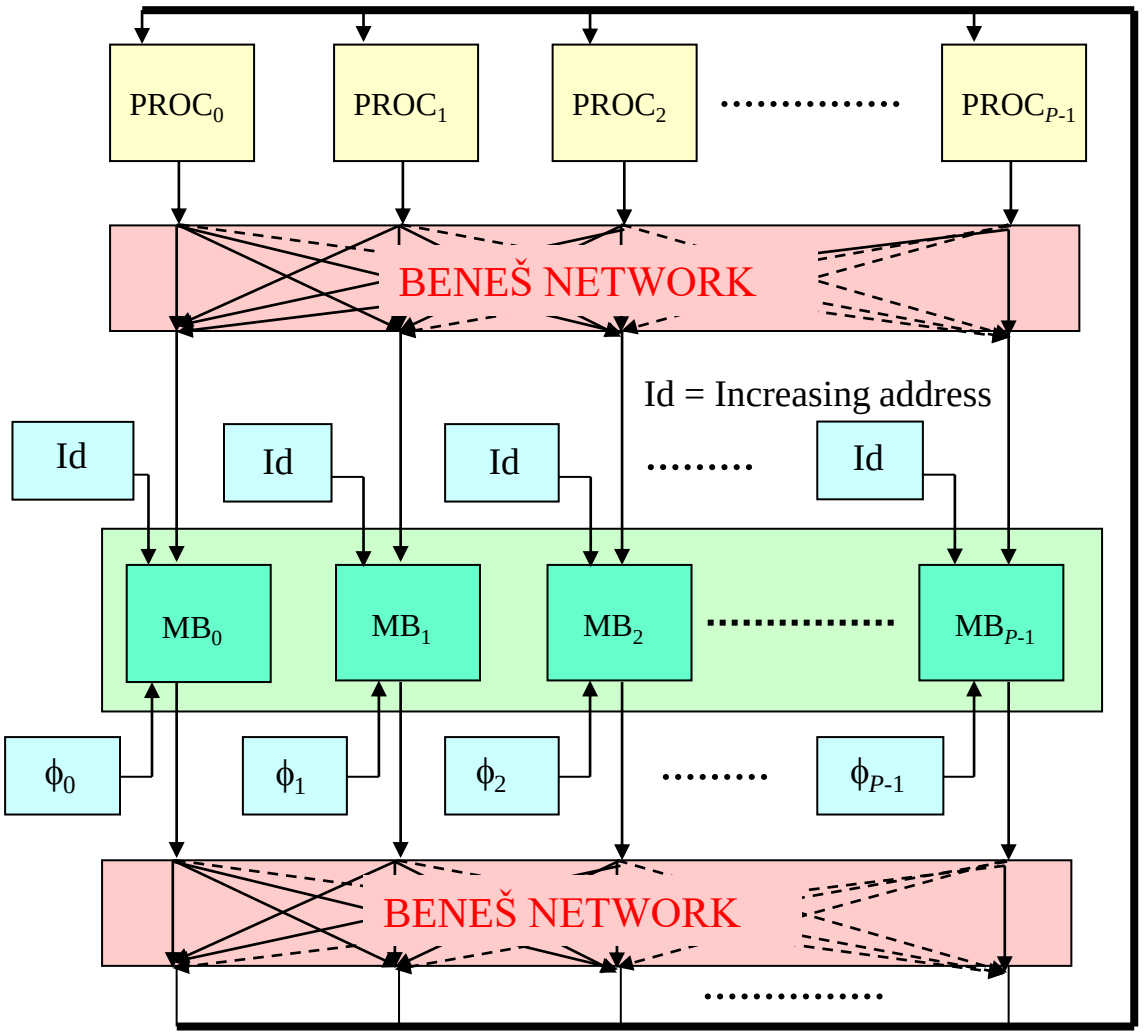
Parallel architecute: memory access conflicts resolution

Parallel architecture

Parallel access conflicts

Execution [Thül *et al.*, 2002]
- memory
- interconnections

Compilation [Tarable *et al.*, 2003]
- memory



Memory mapping adapted to the interleaver

Parallel architecute: memory access conflicts resolution

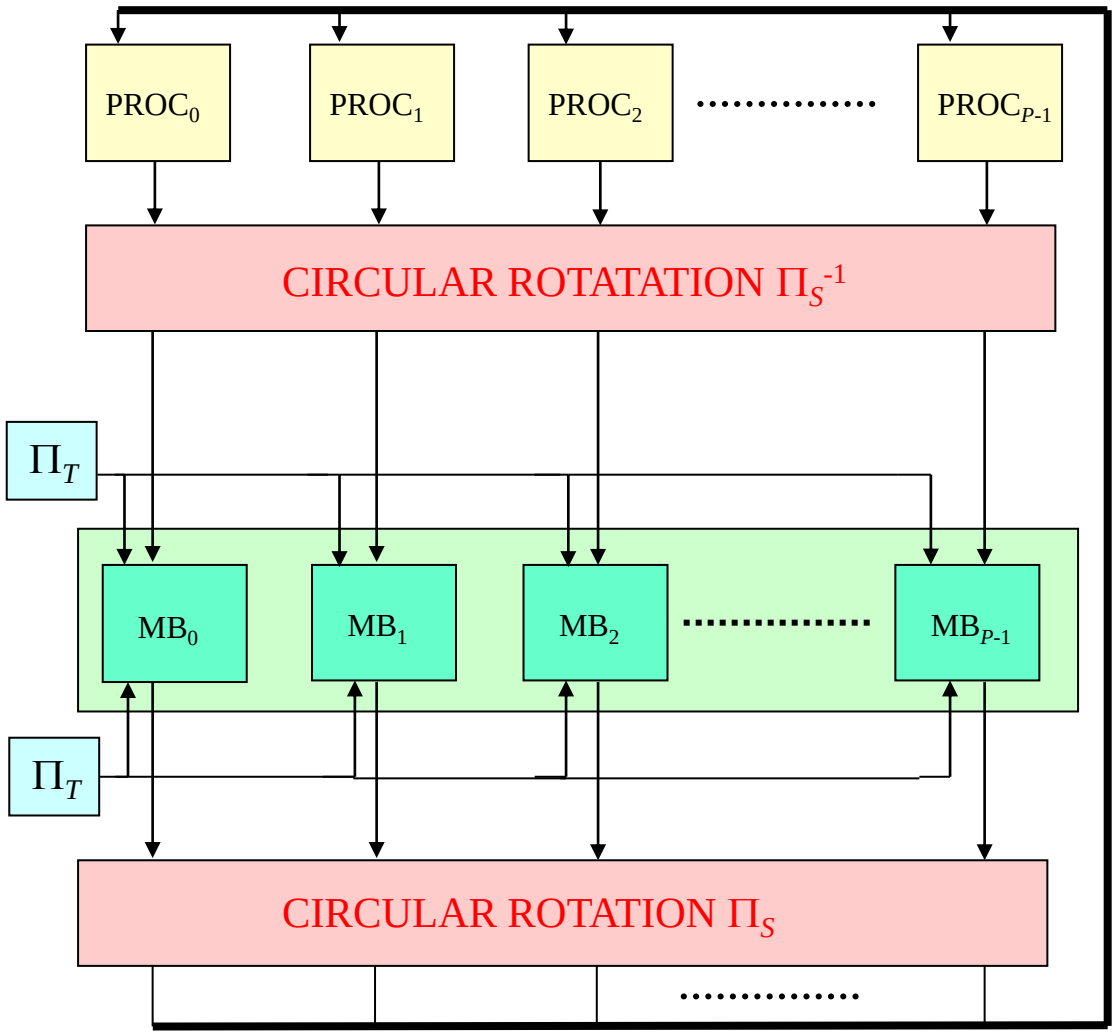
Parallel architecture

Parallel access conflicts

Execution [Thül *et al.*, 2002]
- memory
- interconnections

Compilation [Tarable *et al.*, 2003]
- memory

Conception [Boutillon *et al.*, 2002] [Gnaedig *et al.*, 2003]
- address generation through combinational logic
- constrained spatial permutation =>complexity divided by 2



DVB-S2 standardization (2)

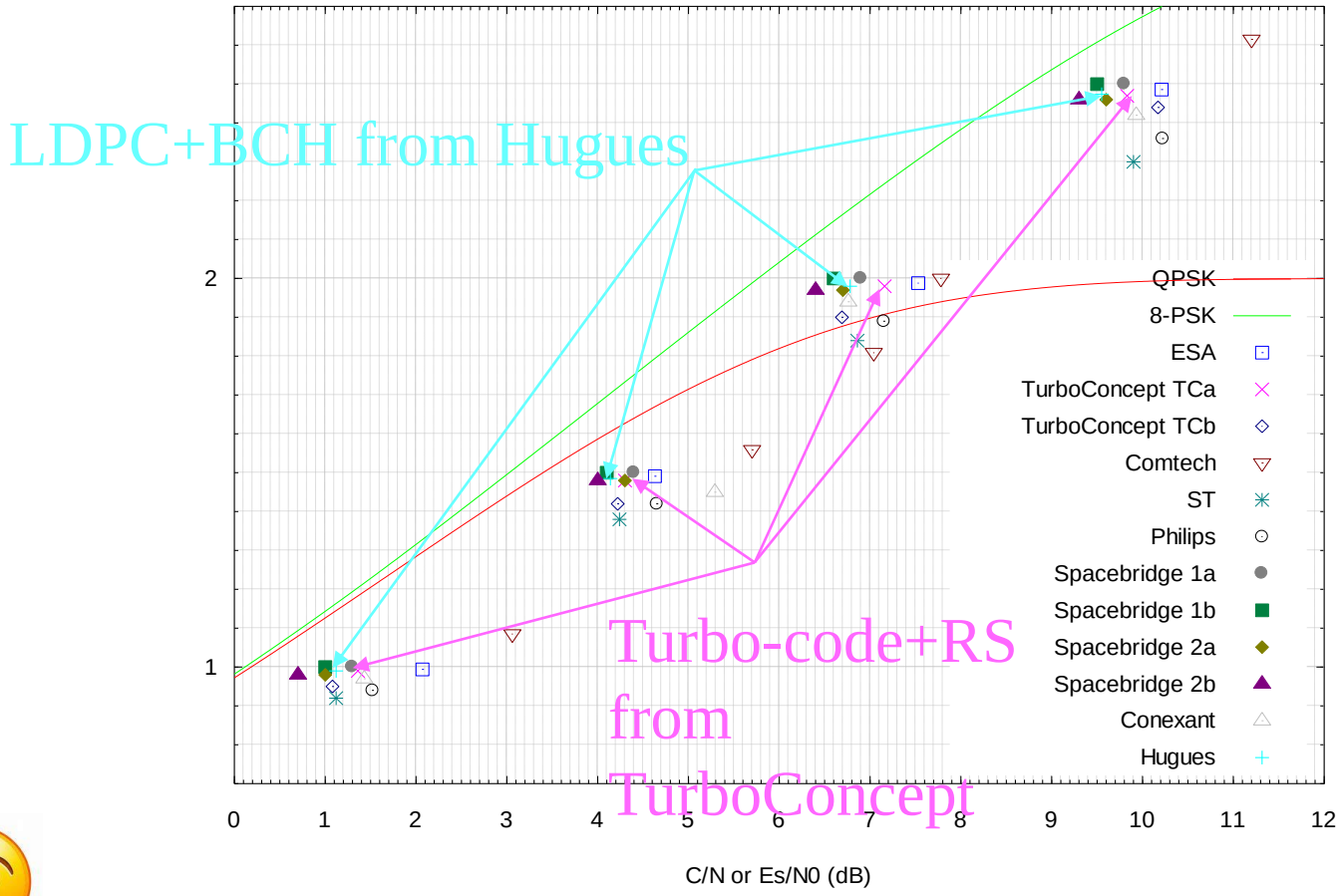
- Endless discussion on complexity:
  - The committee decided to estimate turbo decoder complexity a much less efficient serial architecture rather a parallel decoder architecture

  ⇒ reduction of maximal block size supported by turbo-codes solutions

		3rd Round formula	4th Round formula
SISOs	Traceback memory bits	3840	3840
	Area(Traceback memory)	0,02	0,02
	Number of Max*	79	76
	Area Max*	0,28	0,27
	Area 1 SISO(incl. traceback)	*0,30*	*0,29*
	Number of SISOs	10	5
	Area all SISOs	**3,01**	**1,45**
Input samples	bits	273600	273600
	Area 1 memory	*0,82*	*0,82*
	Number of memories	5	2
	Area	**4,11**	**1,65**
Extrinsic	bits	182400	296400
	Area 1 memory	*0,57*	*0,88*
	Number of memories	10	1
	Area	**5,73**	**0,88**
	External interleaver bits	136800	136800
	Area external interleaver	**0,45**	**0,45**
	RS Area	**0,5**	**0,5**
	Total	**13,80**	**4,93**

DVB-S2 standardization (3)

- Comparison of solutions: @ PER 10^{-7}



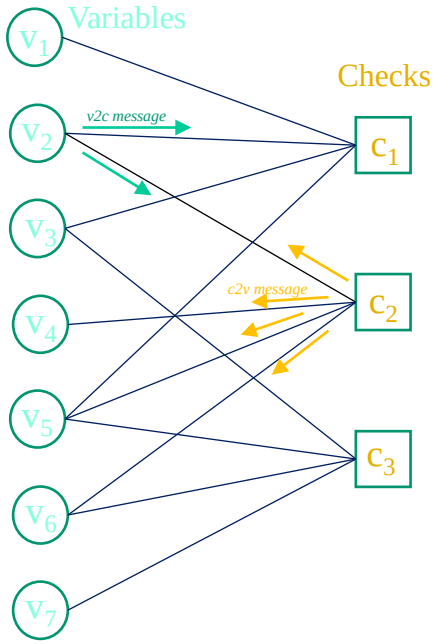
LDPC codes were selected as the FEC solution for DVB-S2

LDPC codes

- Originally proposed by Gallager in 1960
- Re-discovered in 1996 by D. MacKay

Variables / *Checks*

$$H = \begin{array}{c} \begin{matrix} v_1 & v_2 & \dots & & v_5 & v_6 & v_7 \end{matrix} \\ \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix} \end{array} \begin{matrix} \\ c_1 \\ c_2 \\ c_3 \end{matrix}$$



code structure

- a set of parity check equations
- arranged in a matrix : Parity Check Matrix H
  - rows = checks
  - columns = coded bits (or variables)
- Low Density
  - low number of '1' in H (typical ~1^E-4)
  - breaks correlation (avoids short cycles in the decoding graph)

decoding algorithm

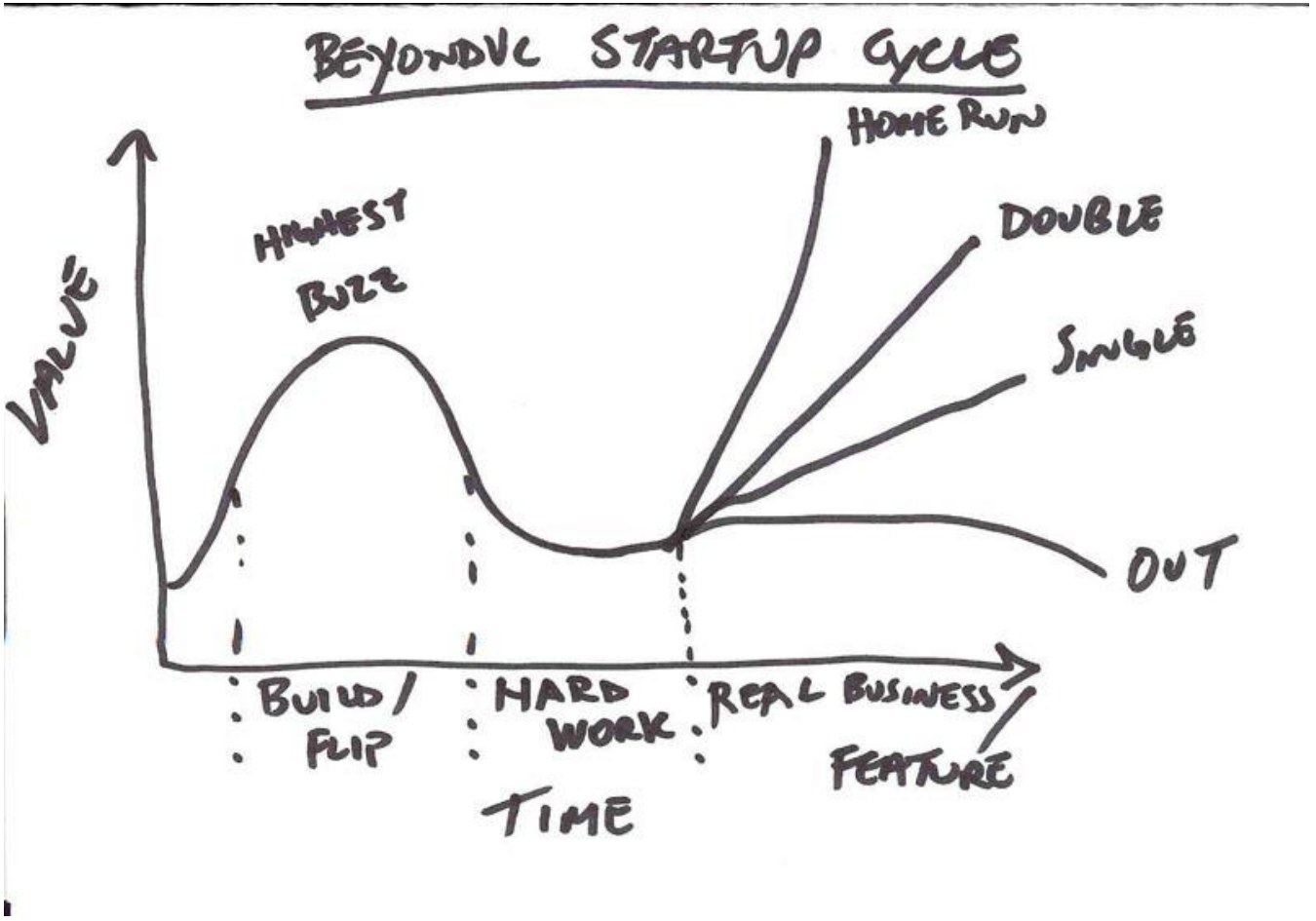
"Belief Propagation" or "Message-Passing"

- Check Node Unit (CNU) and Variable Node (VNU) computation
  - manipulates probabilities on bits, or Log-Likelihood ratios (LLR)
- Iterative processing
  - Exchange of messages between CNUs and VNUs
- typical 20 iterations

Gallager, R.G. (January 1962). "Low density parity check codes". IRE Trans. Inf. Theory. 8 (1): 21-28.

David J.C. MacKay and Radford M. Neal, "Near Shannon Limit Performance of Low Density Parity Check Codes," Electronics Letters, July 1996

TurboConcept evolution as a startup company



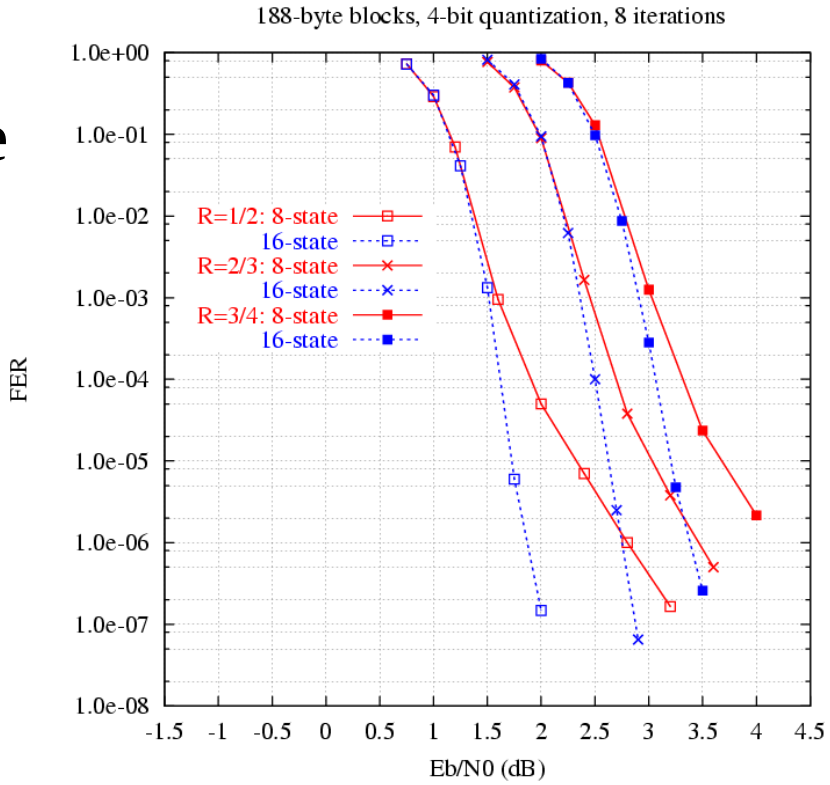
Implementation of LDPC codes for DVB-S2

- TurboConcept rapidly implemented LDPC codes & BCH code for DVB-S2
  - with the support of Universities (E. Boutillon from UBS)
- Patent on layered decoding architecture
- Commercial product in Dec 2003 (less than 12 months after standardization)
- SkyPlug: partnership with CommSonic a UK IP company providing the demodulator

- Commercial success with several customers among ground equipment satellite providers.

DVB-RCS2 standardization

- Several ESA projects to define a new code without the error floor issue of 8-state turbo code
  - 2003 : MoHOMs
  - 2008 : ADMOST
- Extend to 16-state turbo code
- Solution selected by DVB-RCS2 standardization committee



WiMAX turbo-code

- 1999-2004 : TurboConcept is focused on the satellite market exclusively
  - Standard : DVB-RCS, DVB-S2, DVB-RCS2
  - Custum solutions
  - Mainly on FPGA
- 2001 : Creation of the WiMAX forum to define a standard for broadband wireless access
- 2004 : completion of the specification IEEE 802.16-2004 using turbo-code similar to DVB-RCS
- 2005 :TurboConcept developped IP cores
  - One for ASIC design (UE)
  - One for BaseStation (FPGA)
- Commercial success with many start-ups designing chips for the WiMAX market

SEQUANS COMMUNICATIONS

altair semiconductor

DesignArt Networks

ApaceWave TECHNOLOGIES

Acquisition by Newtec

- 2007 : acquisition by Newtec
  - Ground equipment equipment provider for satellite communications
  - One of TurboConcept's first customer on the satellite market (DVB-RCS, DVB-S2)
  - Interest for joint demodulation / channel decoding
- TurboConcept evolution:
  - FEC technologies design & development for satellite market for Newtec
  - continue its IP core business of IP development and commercialization for other markets
    - Wireless (3G & 4G)
    - Broadcast (DVB-T2, CMMB)
    - Domestic networking (Homeplug AV, WiFi, …)
- In 2017, Newtec was acquired by its competitor iDirect, part of ST Engineering (Singapour based company)

4G LTE turbo code

- 2000: 3G specifications
  - 8-state turbo code
- 2007-2008 : 4G LTE standardization by the 3GPP consortium
  - a competing solution to WiMAX 802.16
- Dec 2008 : finalization of the 4G LTE specification
- 2007 :Availability of IP cores for LTE specification (FPGA & ASIC)
- 2008: Availability of dual-mode WiMAX / LTE IP cores (FPGA & ASIC)
- Same UE customers than for WiMAX cores

SEQUANS COMMUNICATIONS

altair semiconductor

DesignArt Networks

- Base station customers:

Wavesat

MINDSPEED BUILD IT FIRST

NORTEL

DVB-S2X standardization

- 2011 : definition of Newtec proprietary S2 evolution
- 2013 : eXtension of DVB-S2
  - TurboConcept proposed new LDPC codes and new modulations
  - Selected to be incorporated in DVB-S2X specification

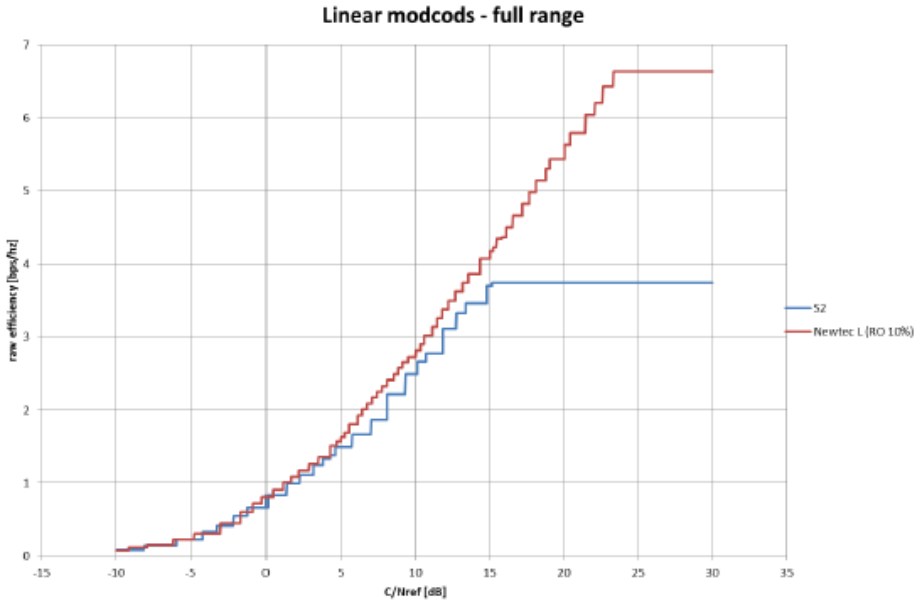
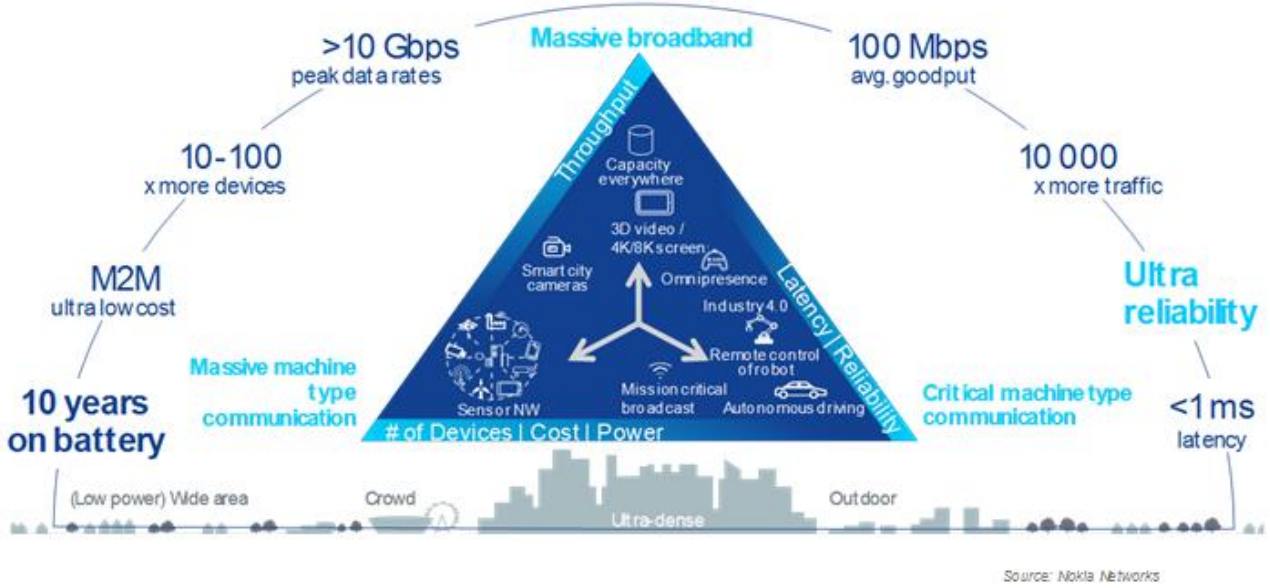


Figure 12: Efficiency of proposed linear modcods compared to DVB-S2.

5G standardisation

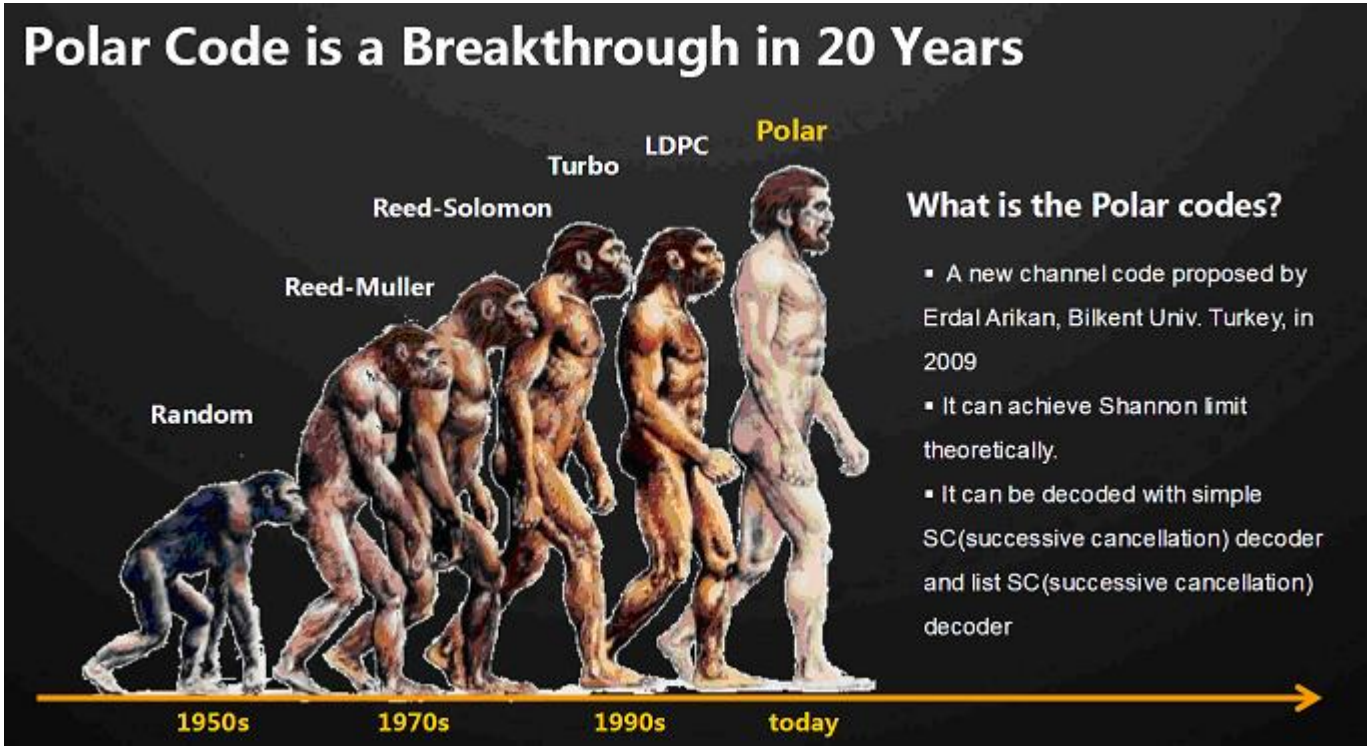
- Evolution of 4G networks with new applications
- 3 main applications
  - Wireless broadband: video, data transfers, internet access
  - Machine Type Communication (M2M): IoT, sensor networks, …
  - Critical communication: autonomous driving, control of robot



Source: Nokia Networks

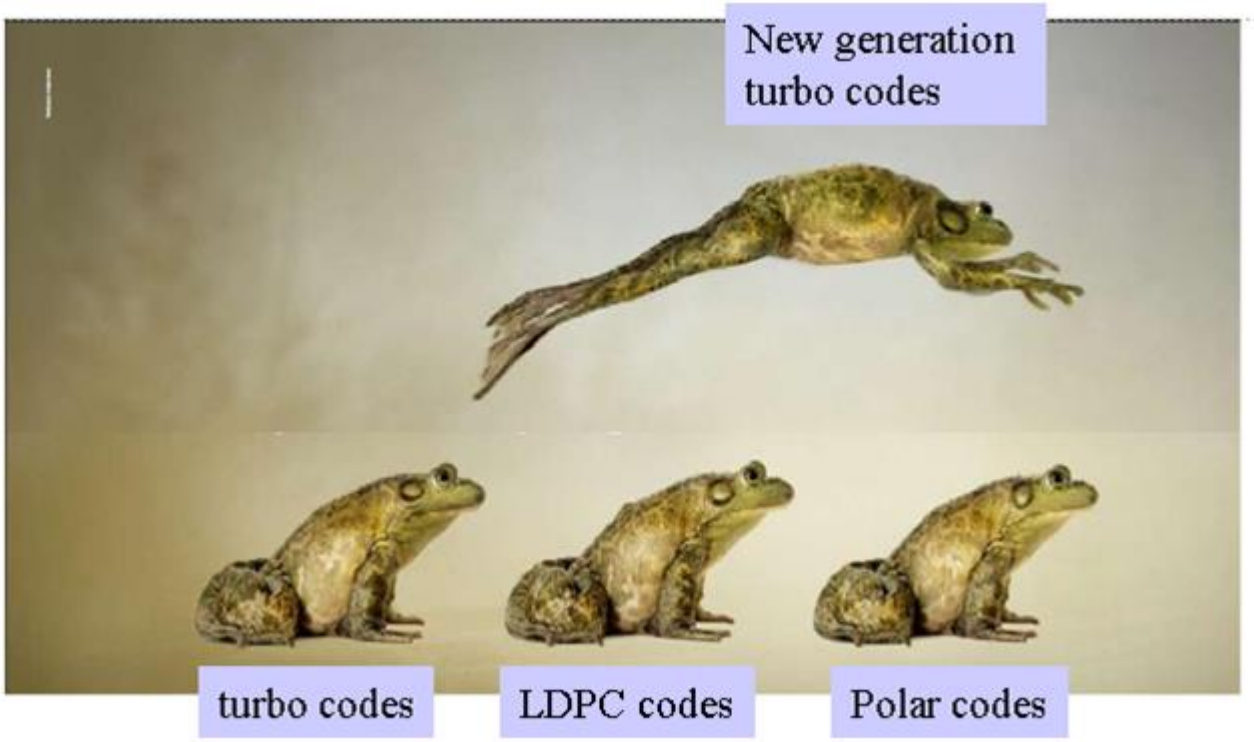
Polar codes

- Pushed by Huawei at 5G standardization



New turbo codes

- Pushed by IMTA&Orange at 5G standardization



5G standardization

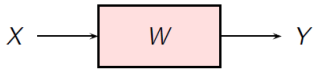
- Nov 2016: 5G specification by 3GPP
  - Data channels : use LDPC codes
  - Control channels : use polar codes
    - Were not selected only for technical reasons
    - but also for political reasons
      - Fight between US (Qualcomm) / China (Huawei)
- Sept. 2017 :
  - Availability of IP Cores for 5G LDPC
- Dec 2017:
  - Availability of IP Core for 5G polar
- IP cores licensed to
  - major providers of chips for Base Station
  - UE chips providers
    - wireless broadband applications
    - IoT
    - autonomous driving

	Uplink	Downlink
Transport channels (traffic)	UL-SCH LDPC	DL-SCH PCH LDPC
Transport channels (control)		BCH Polar code
Control information	UCI Block code Polar code	DCI Polar code

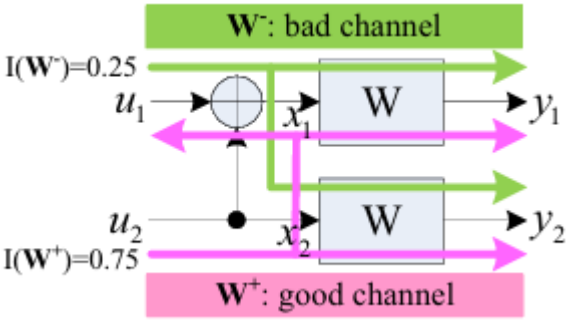
Polar codes (Arikan, 2009)

- Provably achieves capacity
- Channel polarization

Capacity I(W) = 0.5



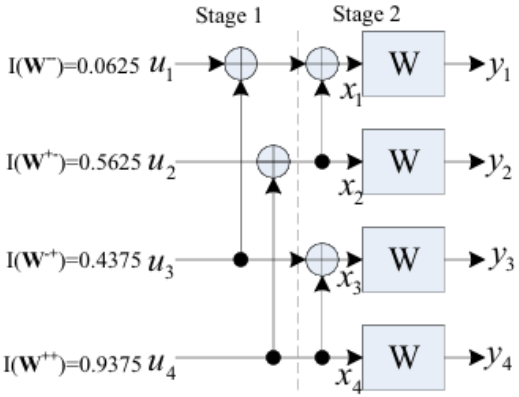
Combination of 2 channels

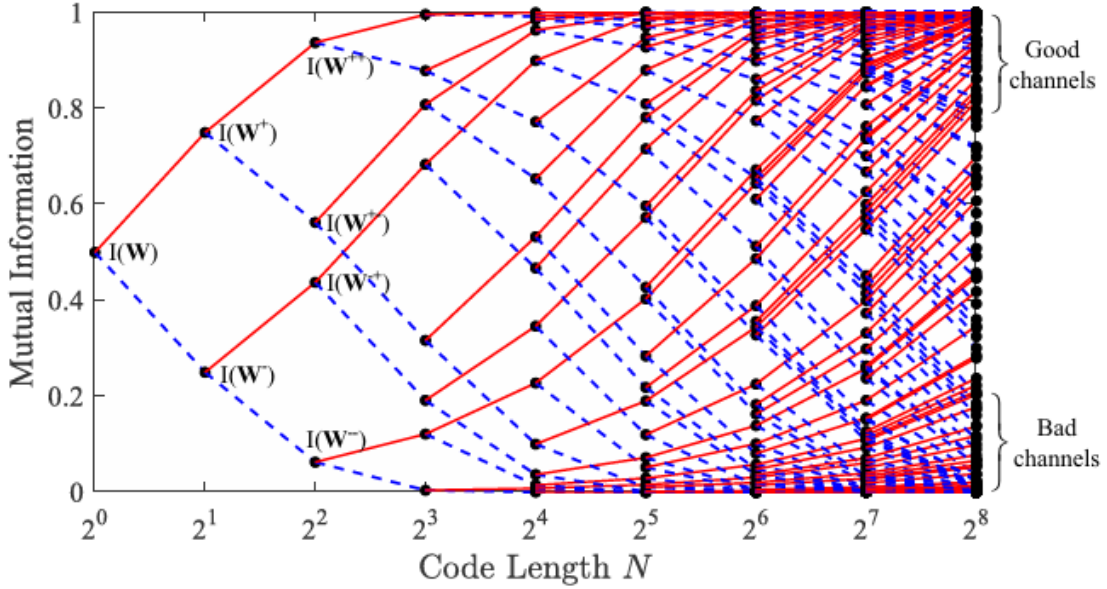


$$I(W^-) + I(W^+) = 2I(W)$$

$$I(W^-) \le I(W) \le I(W^+)$$

Combination of 4 channels

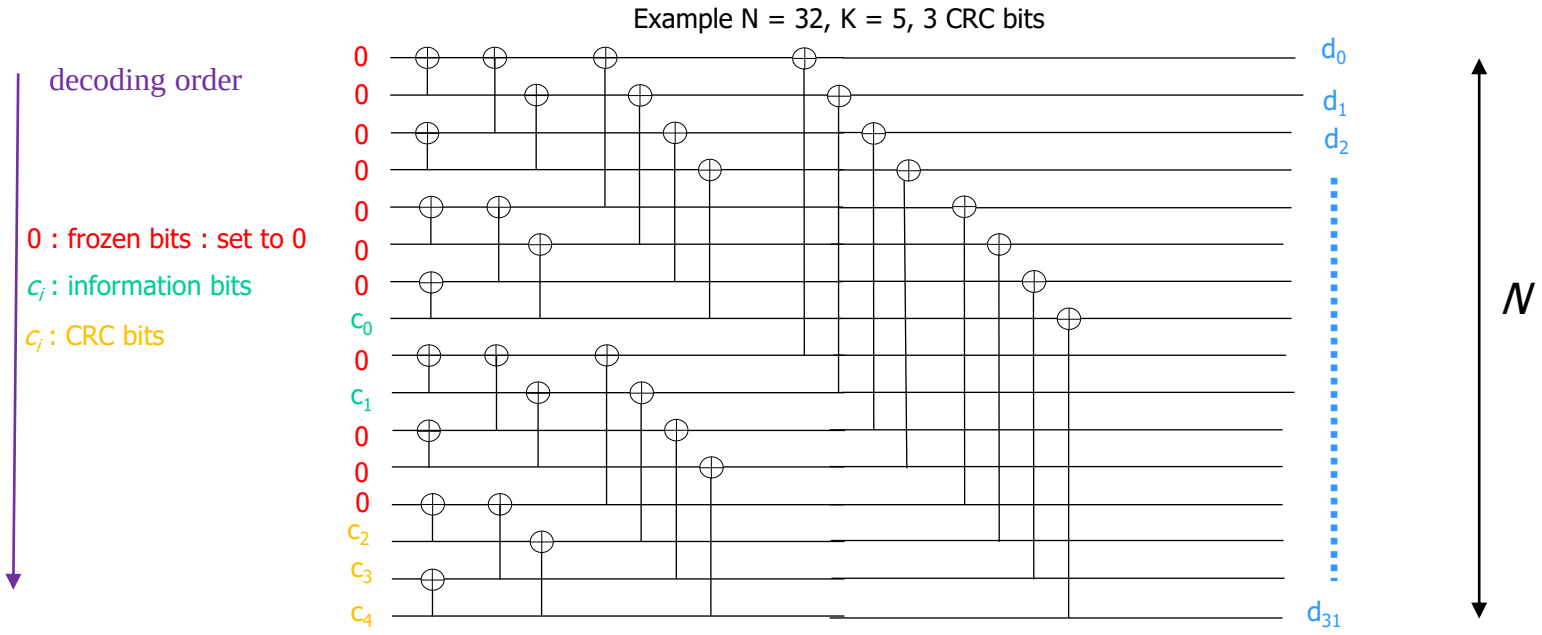




(d) Evolution of channel polarization.

Polar codes (Arikan, 2009

Information bits are placed on best protected positions of the polar coding scheme
Frozen bits are placed on bits that are least protected positions



Polar decoding

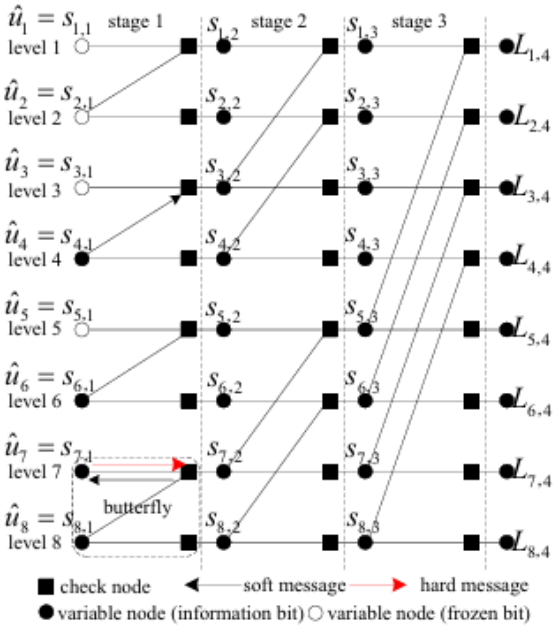
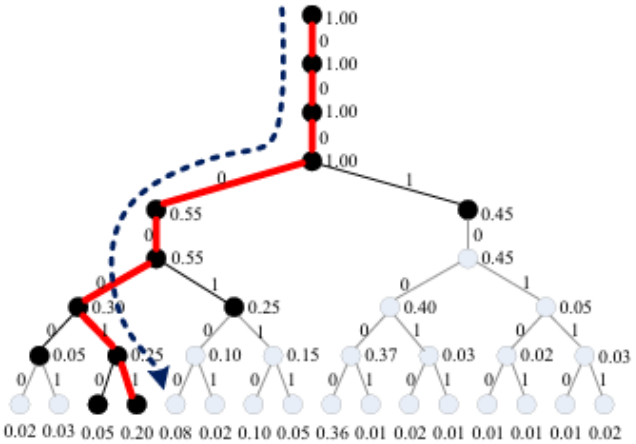
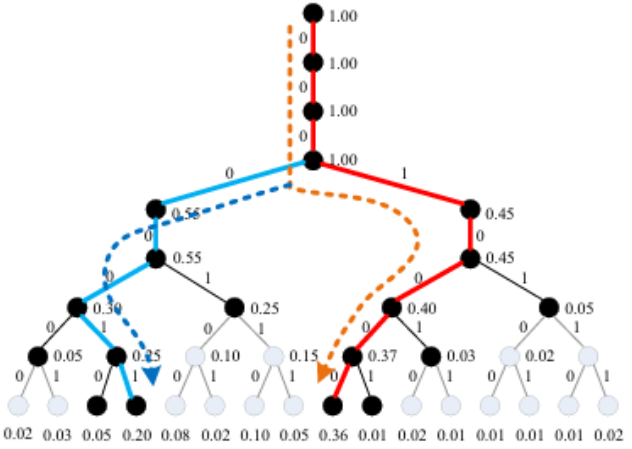


Figure 4. *Trellis of the* $(8, 4)$ *polar code.*

Successive Cancellation (SC)



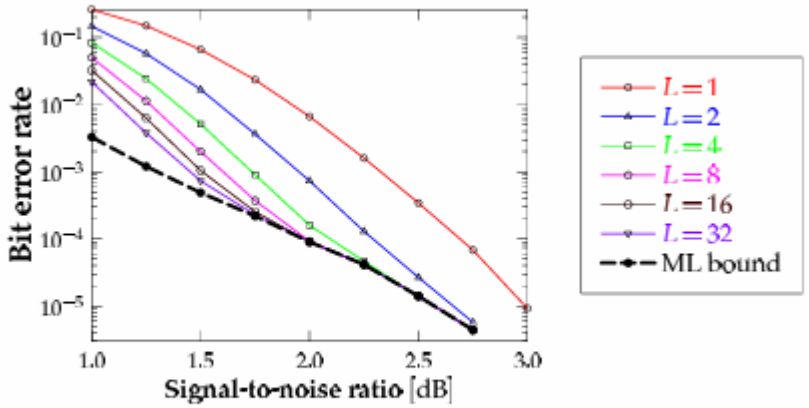
Successive Cancellation List (SCL) – L = 2



A Golden Decade of Polar Codes: From Basic Principle to 5G Applications Kai Niu1,3,*, Ping Zhang2, Jincheng Dai1, Zhongwei Si1, Chao Dong1

Performance of polar codes

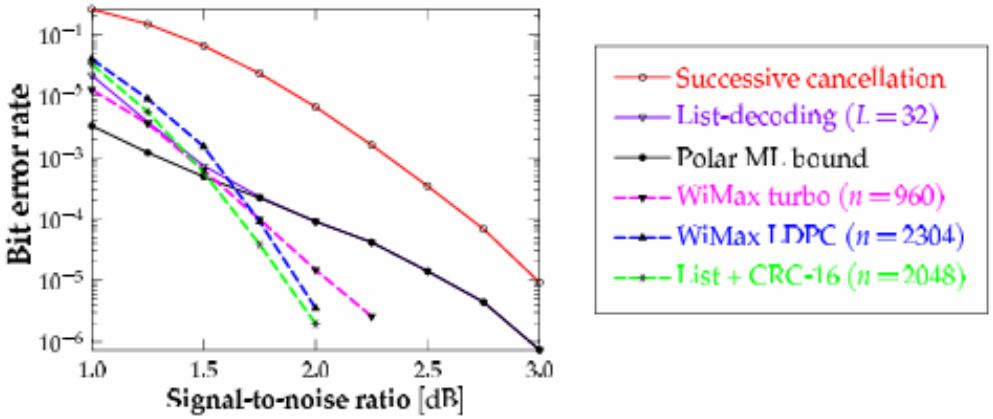
Length $n = 2048$, rate $R = 0.5$, BPSK-AWGN channel, list-size L.



List-of-L performance quickly approaches ML performance!

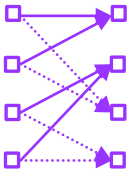
Add CRC code

Length $n = 2048$, rate $R = 0.5$, BPSK-AWGN channel, list-size L.

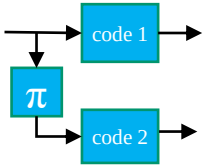


Polar codes (+CRC) achieve state-of-the-art performance!

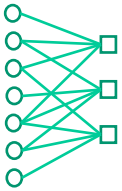
today



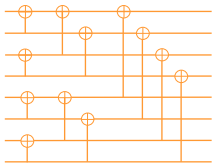
Convolutional code



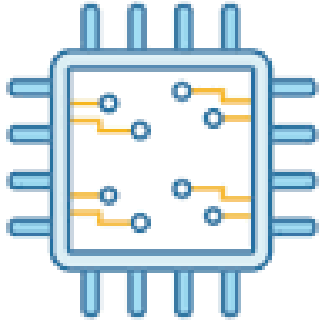
Turbo codes

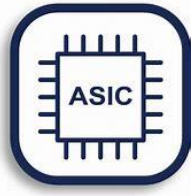


LDPC codes



Polar codes





TurboConcept's team

- 6-engineers team

- Roles *(from left-to-right)*
  - Jacky Tousch (Co-founder) : Sales & Management
  - David Gnaedig : CTO
  - Omid Zia Chahabi : IP Core design
  - Patricia Ruiz : Polar expert
  - Nathalie Brengarth (co-founder): Admin & HR
  - Pierre Wadier: LDPC expert

- Homogen & overlapping skills
- very good team-spirit
- low turnover

IP core licensing to 3rd party

portfolio of IP Cores

- Mostly open standard - based solutions (3GPP, IEEE, DVB, CCSDS)
  - *cover all 4G/5G FEC technologies*
- But also proprietary / custom solutions
- Several profiles available *(eg. throughput/area tradeoff)*
- Continuous maintenance and improvement effort
- FGPA & ASIC cores

license structure

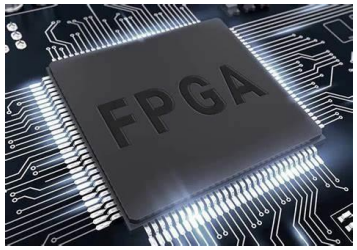
- project-based *(one project = one ASIC or one FPGA)*
- entrance fee
- reuse fee for each new ASIC (70%)
- maintenance fee (10-15%, optional)
- (no volume-royalties)

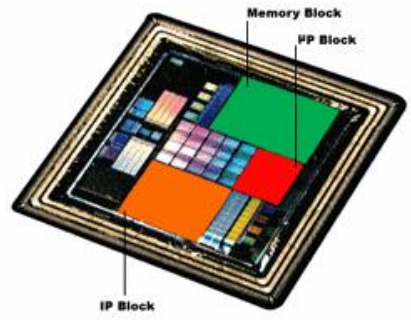
Selling of IP cores

- At the beginning of the value chain

IP décodeur FEC hardware

Vendeur d'IP hardware
Ex: TurboConcept, ARM, …





Chipset providers
ex: Intel, Sequans, Sony, Qualcomm, Samsung, …

Cell phone equiment manufacturers
ex: Apple, Samsung, Xiaomi,…

Telecommunication equipment manufacturers
ex: Nokia, Alcatel Lucent, Huawei, Ericsson …

Satellite equipment manufacturers:
ex: iDirect, Viasat, SpaceX

FEC families and applications

Advanced

- Turbo Codes
  - DVB-RCS (1 and 2)
  - 3GPP-LTE
  - CCSDS
  - Homeplug AV
- LDPC codes
  - DVB-S2
  - WiFi
  - CCSDS
  - 5G-NR
  - PON
- Polar codes
  - 5G-NR

Classical

- Convolutional Code
  - 3GPP-LTE (control channels)
- BCH codes
  - used as outer code in DVB-S2
- Reed Solomon
  - used in optical links, HDD
- Reed Muller
  - LTE
  - 5G

IP Core design : key challenges

High throughput

- several SISO or CNUs processors
- practical issues to solve
  - avoid conflict on shared memory access (extrinsics/messages)
  - scheduling ; routing large bus

Tradeoffs

metrics :

- SNRperf ; QoS ; Throughput ; Latency ; Area ;
- market segments (UE/BS , customization,...)

knobs:

- algorithmic variants (approximations) ;
- fixed point & quantization ;
- architecture (e.g. pipeline for better clock frequency)
- profiling (dedicated implementation for each market segment)

Flexibility

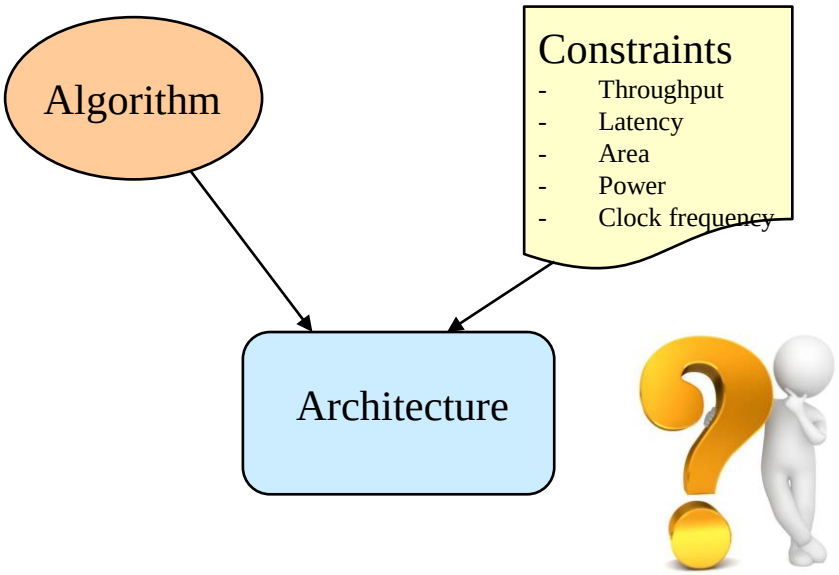
- block size ; code rate , ... can change over time
- IP Core needs to dynamically adapt

Validation

Requirement : first-time-right ASIC

- in-house validation framework ;
- continuous effort to maintain/improve

Algorithm Architecture Adequacy (AAA)



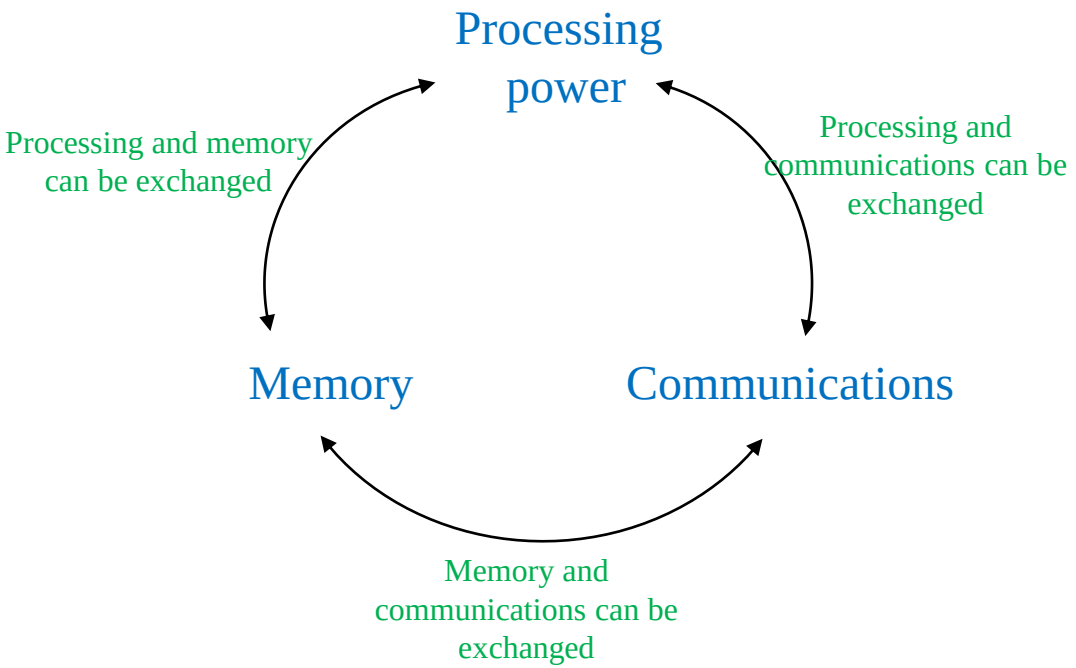
Definition:

description of a system of hardware components and their interrelationships used to execute the algorithm

Architecture definition

3 hardwares ressources:
- Processing power
- Memory (storage means)
- Communication means

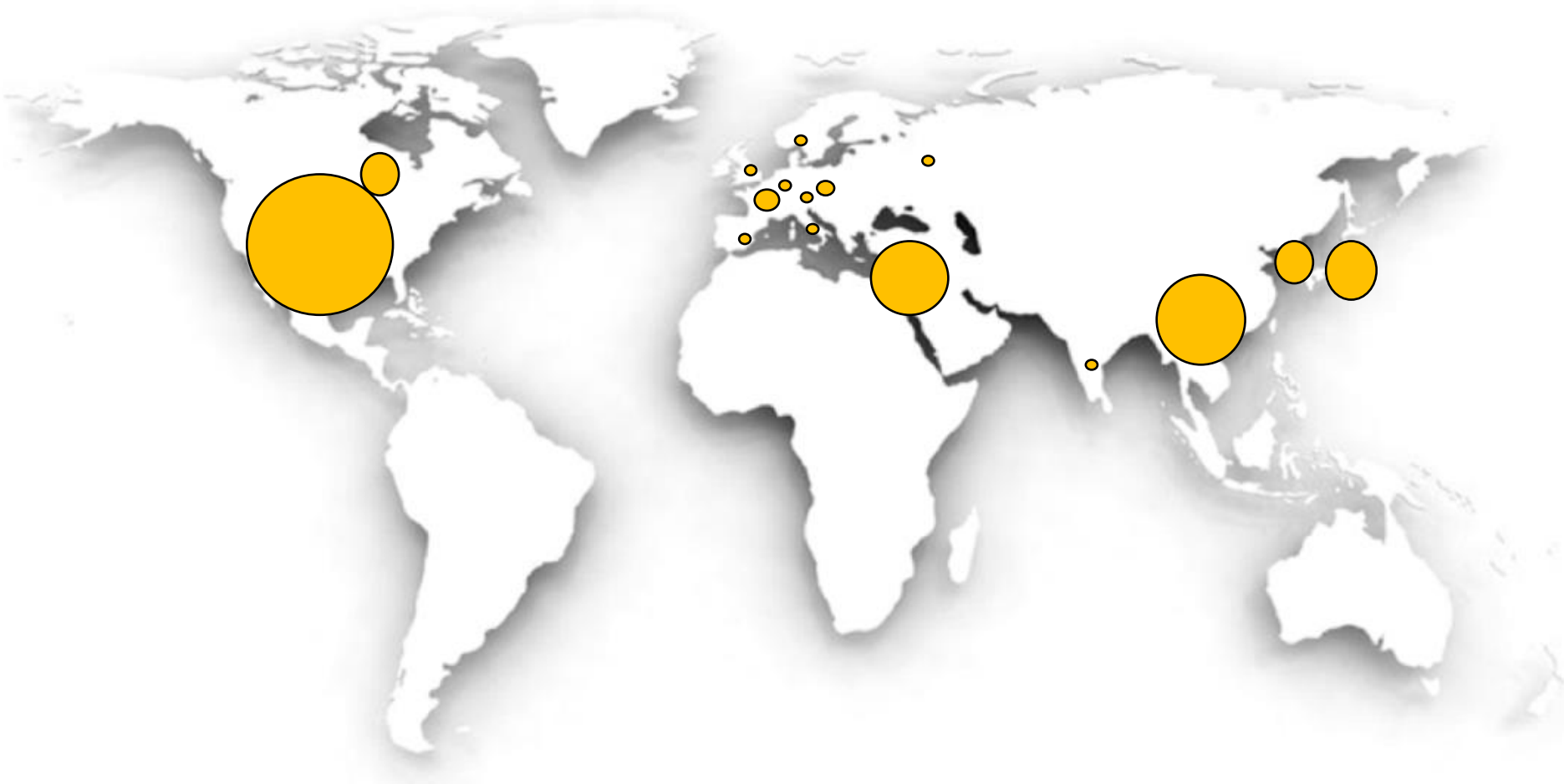
Scheduling : space and time ressource allocation



Partnership with Universities & Research centers

- IMT Atlantique
  - Previously Telecom Bretagne
  - TurboConcept is a spin-off of Telecom Bretagne
  - Many joint projects (ESA, ANR, …)
- University of South Britanny (UBS)
  - Many joint funded projects (ESA, ANR, …)
- Member of Pracom
  - Collaboration between IMTA and French companies around 4G & 5G networks
- Member of "pôle de compétitivité" Image & Réseau

Worldwide market

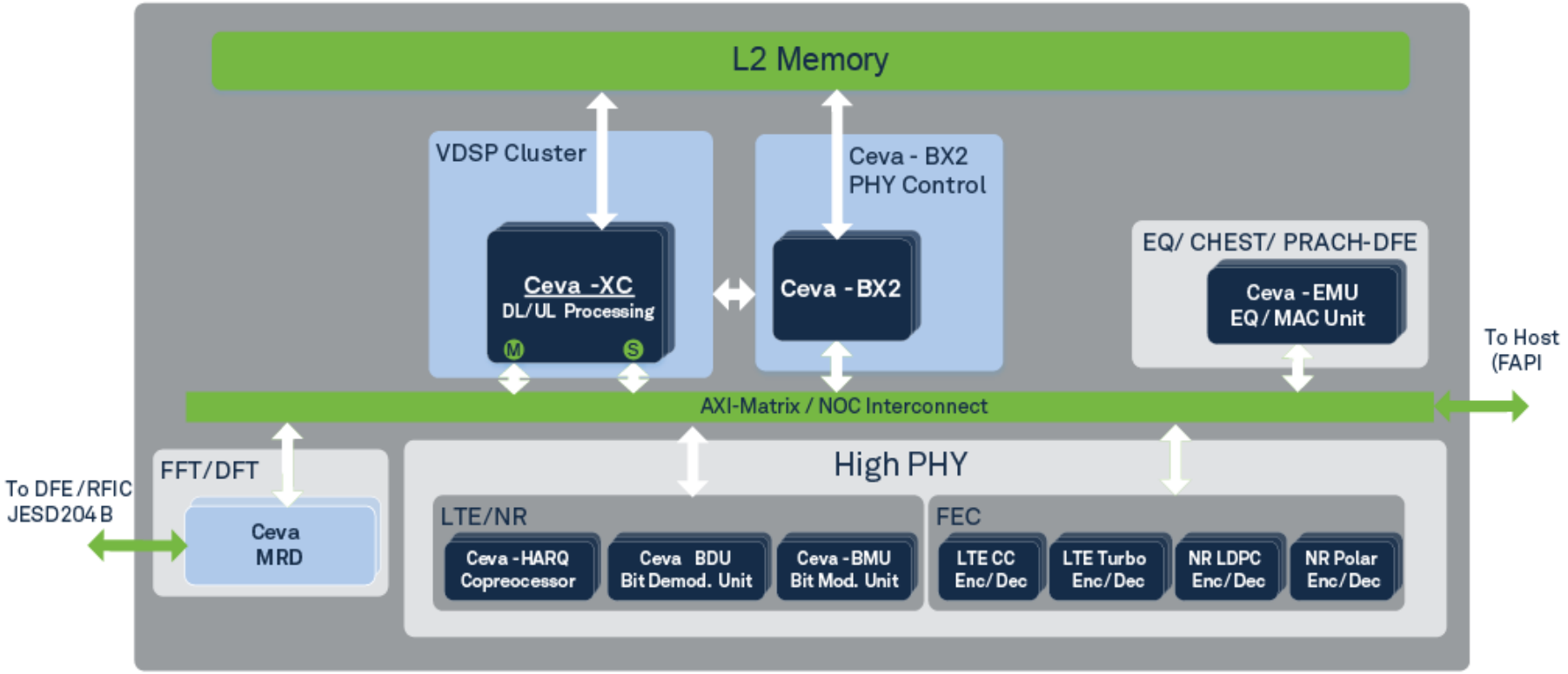


Commercial distribution

- Direct sales
  - US, Europe, Israel
- Distributors
  - 1 distributor in Japan
    - Since > 15 years
  - 1 distributor in China
    - Since 2021
  - Partnership with Ceva DSP
    - DSP IP vendor
    - sublicense contract

Ceva DSP partnership

- FEC IP core for acceleration



Customer references

- More than 200 design wins over 25 years

Customers references (2)

- Several customers in the top 10 semi-conductor vendors

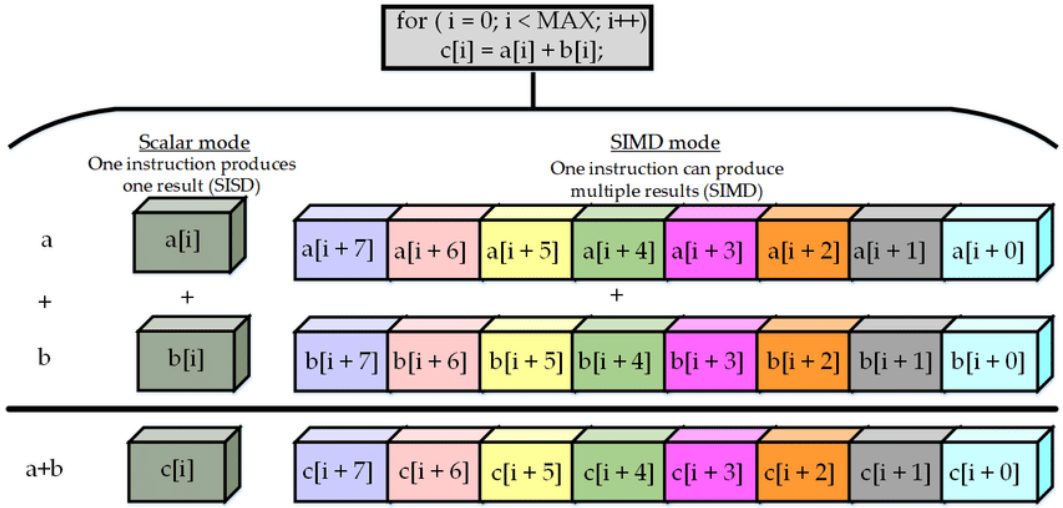
Table 1. Top 10 Semiconductor Vendors by Revenue, Worldwide, 2023 (Billions of U.S. Dollars)

2023 Rank	2022 Rank	Vendor	2023 Revenue	2023 Market Share (%)	2022 Revenue	2023-2022 Growth (%)
1	2	Intel	48.664	9.1	58.436	-16.7
2	1	Samsung Electronics	39.905	7.5	63.823	-37.5
3	3	Qualcomm	29.015	5.4	34.780	-16.6
4	6	Broadcom	25.585	4.8	23.868	7.2
5	12	NVIDIA	23.983	4.5	15.331	56.4
6	4	SK Hynix	22.756	4.3	33.505	-32.1
7	7	AMD	22.305	4.2	23.620	-5.6
8	11	STMicroelectronics	17.057	3.2	15.842	7.7
9	9	Apple	17.050	3.2	18.099	-5.8
10	8	Texas Instruments	16.537	3.1	18.844	-12.2
		Others (outside top 10)	268.853	50.7	294.729	-8.8
		Total Market	**533.025**	**100.0**	**599.562**	**-11.1**

Source: Gartner (January 2024)

What's next ?

- Market is demanding for flexible and programmable solutions on existing hardware platforms and datacenters (cloud-computing)
- New hardware platforms in addition to FPGA and ASIC
  - SW implementation on processors using SIMD instruction



What's next ? (2)

- New markets
  - Non-Terrestrial Networks (NTN) & 5G convergence

  - 6G
    - New codes for short blocks

    with near ML performance ?

Thank you for you attention !

Questions ?

david.gnaedig@turboconcept.com