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IoT chipsets and Challenges

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Guest lecturers of Professor Florian Kaltenberger as part of the Eurecom course “Radio Engineering”.

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Agenda

- Chipset Market and Challenges
- A GOOD ENOUGH product
- Production Stages of the chip
- Examples of Algos
- 4G/5G PHY recall
- DL Synchronization
- PSS detection

Players in the 5G chipsets market

- Qualcomm Technologies (USA)
- MediaTek (Taiwan)
- Huawei Technologies (China)
- Samsung (South Corea)
- Broadcom (USA)
- Sequans Communications (France)

Sequans offers a range of cellular IoT solutions optimized for non-smartphone applications:

- Massive IoT
- Broadband & Critical IoT

From a chip to a device

"Papillon"

SQN3430

GM02S

Jiobit Tracker

Research and Development in Telecom

- Research is not that close to Development as it seems to be
- Research
    - New topologies, new architectures
    - Showing what is possible in ideal conditions
    - Innovation leads to papers and patents
    - Always trying to find the BEST solution

- Development
    - Creating a product that can be sold in a real market
    - Not about making a prototype or a proof-of-concept, but a million devices
    - Innovation leads to better products
    - Solution should be GOOD ENOUGH and respect price/quality/product requirements trade-off

What does it mean to be GOOD ENOUGH?

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- **Time to market**
  - Being first to market may not lead to success, but …
  - Being too late to the market can lead to failure
  - The next generation is always not far away

- **Features**
  - What does the market actually want?
  - What is the market actually willing to pay for?

- **Power**
  - Mobile devices: Longer battery life, less battery weight
  - Fixed devices: Less power and heat handling -> lower cost

What does it mean to be GOOD ENOUGH?

- **Price**
  - Consumer market is very price sensitive, but …
  - People will spend money for what they want
    - E.g. - How much did your phone cost?

- **Reliability**
  - Consumer market is the least concerned with reliability, but …
  - As a chip vendor, your customer wants reliability
    - A failed chip at product level might mean throwing away the whole product

E.g. IoT and 5G Features and Trade-offs

4G IoT

- Price sensitive
  - Cost: few dollars
- Low power
  - Small battery, years of life
- Low throughput
  - TDD / HD-FDD
  - Single Rx / Tx
  - Low duty cycle
  - Narrow channels
- Limited band coverage
  - E.g. 600 - 950 MHz, 1.7 – 2.2 GHz

5G

- Less price sensitive
  - Cost: tens of dollars
- Less power sensitive
  - Plugged in or large battery
- High throughput
  - TDD / HD-FDD / FDD
  - Multiple Rx / Tx
  - High duty cycle
  - Wide channels
- All available bands
  - FR1: 600 MHz – 7 GHz
  - FR2: 24 – 52 GHz

Tasks of BU and product team

- What features to support? Who will pay?
  - Who are the potential investors/clients
  - Which 3GPP Release to support
  - What are mandatory features and what will be just good to have
  - Client-specific features
  - RedCaps?

Chip production stages

- Pre-study (basic architecture definition, time lines)
- Architecture spec development
- Modeling and RTL verification
- HW tape out (could be a few)
- FW spec development
- Modeling and implementation
- Chip BringUp (HW chip comes back from China)
- Testing, testing, testing
- FW Release (a few)
- Testing, testing, testing

What do we do in the Algo Team

- Internal Clients and Task Providers
  - Task Definer : Architect, Product Team
  - Main Client: HW ASIC Team, MFW team, Validation teams
- We implement a HW and SW model of BB and TD parts of the physical layer of the chip (usually Matlab or C++)
  - 3GPP compliant
  - Efficient
  - Reliable
  - Does the job (sync, metric computations, signal generation, FFT/IFFT, precoding, …) - actual ALGO in FXP
  - Undergoes Continuous Integration
  - GOOD ENOUGH ☺
  - Provides easily retrievable dumps for verifications and debug
- With every developed feature, the model is delivered to the clients that begin writing ASIC or micro code and testing for matching
  - Model is delivered as an exec or library
  - A set of specs describing the feature algo and design
  - A set of scenarios
- Every new feature has a kick off and follow up meetings

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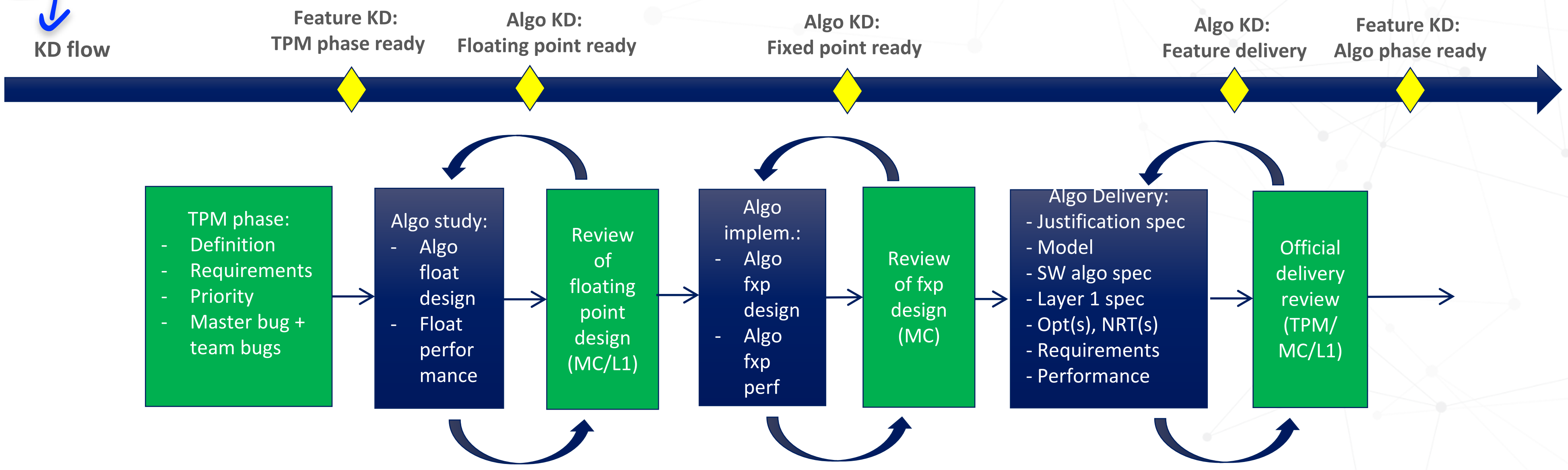
Algo design flow

Key date



Some examples of our algos (UE side)

- Interference mitigation
- Synchronization
- Measurement Reporting
- High speed enhancement
- Time/Frequency estimation
- Channel Estimation
- HW-based algos designed to optimize processing time

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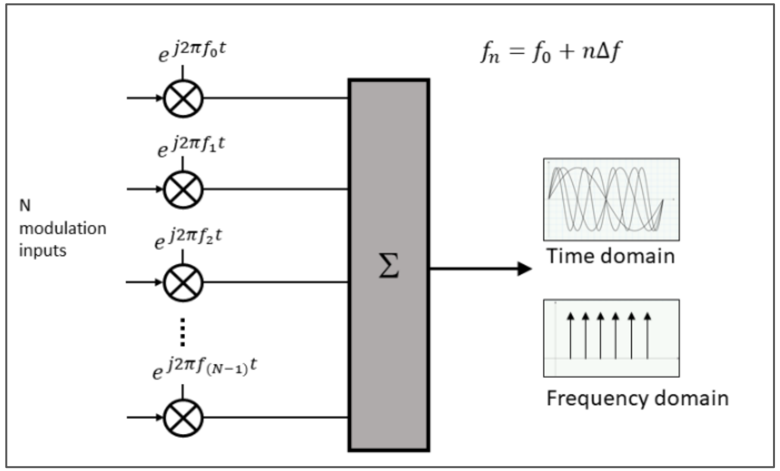
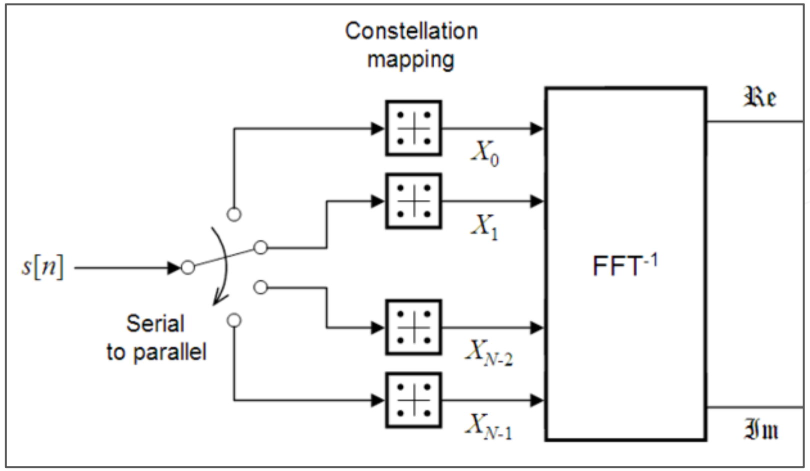
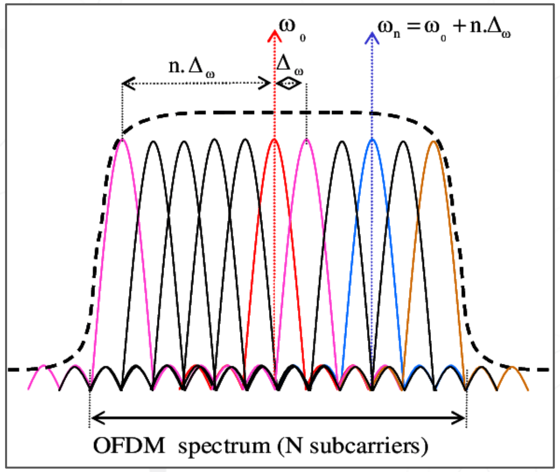
Timing synchronization in downlink LTE, RX IQ imbalance

LTE (4g/5g) PHY Overview

- Orthogonal Frequency Division Multiplexing (OFDM)
- OFDM divides the available bandwidth into orthogonal subcarriers 15kHz that are modulated by QAM symbols which carry the (coded) information bits.
- The use of Fast Fourier Transform (FFT) – no need of multiple RF modulators
- Effective against multipath fading and Inter Symbol Interference (ISI) via use of the CP.







LTE 4g vs 5g

- One of remarkable points between 4g and 5g is numerology which sets arbitrary subcarrier spacing that affects the bandwidth and performance of a 5G network: QoS, latency requirements and frequency ranges

OFDM parameters	Up to ~10 GHz	Up to ~20 GHz	Up to ~40 GHz	Above ~40 GHz
Subcarrier spacing	15 kHz	30 kHz	60 kHz	$2^L \times 60$ kHz
Symbol duration	66.77 µs	33.33 µs	16.67 µs	$16.67/2^L$ µs
CP duration	4.69 µs	2.35 µs	1.17 µs	$1.17/2^L$ µs
Clock frequency	30.72 MHz	61.44 MHz	122.88 MHz	$2^L \times 122.88$ MHz
FFT size	2048	2048	2048	2048
CP samples	144	144	144	144
CP samples (Extended)	512	512	512	512

What does it mean being sync?

- The initial process of identifying any available base station (BS) by a user equipment (UE) that wants to communicate. To ensure a reliable communication, any UE has to be synchronized with the BS both in time and frequency domains.

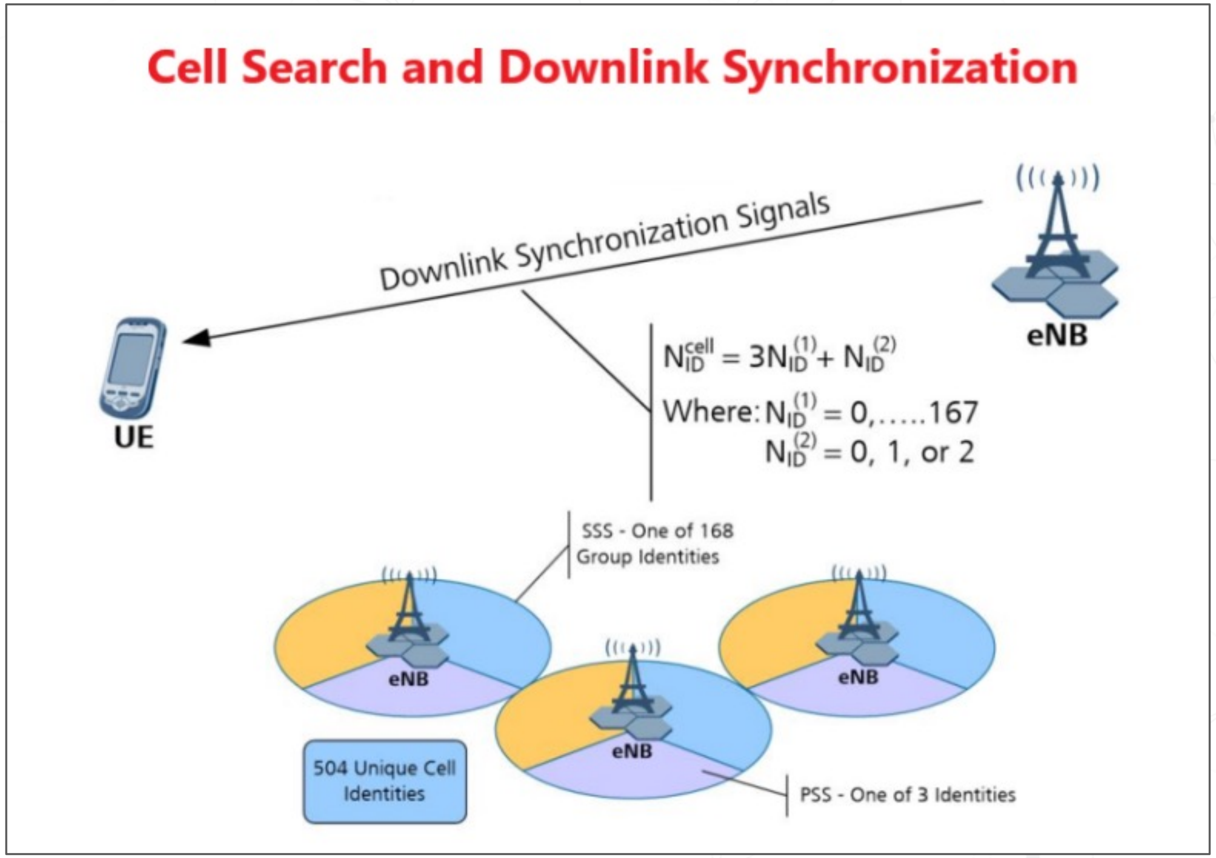
- Frequency synchronization helps in identifying the center of the channel bandwidth and compensate residual carrier frequency errors

- Timing synchronization is the process in which UE detect the radio boundary (i.e, the exact timing when a radio frame starts), OFDM symbols boundary(i.e, the exact timing when an OFDM symbol starts) and Physical Cell ID.

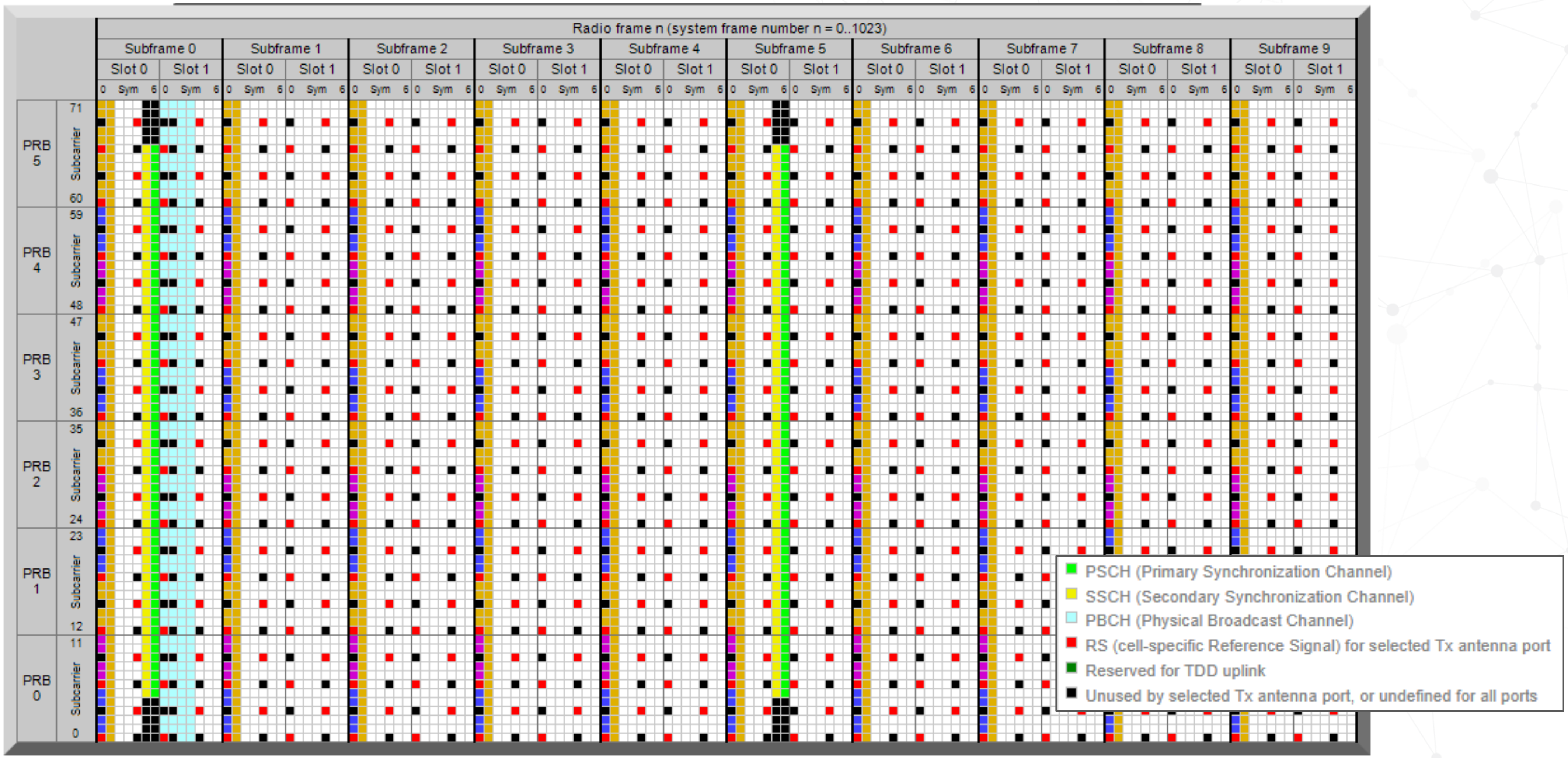
- In LTE sync signals are random sequences that also carry base station related information

UE Downlink synchronization

- Downlink synchronization is the first step that a UE needs to complete after entering a cell. Only after the downlink synchronization is complete, the UE can start to receive other channels (for example, broadcast channels) and perform other activities.
- **Primary Synchronization Sequence (PSS).** PSS helps in identifying the Root-index (1 of 3)
- **Secondary Synchronization Sequence (SSS)** SSS helps in identifying the Group Identifiers (1 of 168)



LTE resource grid



Downlink synchronization signals

- The PSS sequence $d(n)$ used for the primary synchronization signal is generated from a frequency-domain Zadoff-Chu sequence according to

$$d_u(n) = \begin{cases} e^{-j\frac{\pi u n(n+1)}{63}} & n = 0,1,\ldots,30 \\ e^{-j\frac{\pi u (n+1)(n+2)}{63}} & n = 31,32,\ldots,61 \end{cases}$$

Table 6.11.1.1-1: Root indices for the primary synchronization signal

$N_{ID}^{(2)}$	Root index u
0	25
1	29
2	34

- The SSS sequence sequence $d(0),\ldots,d(61)$ used for the second synchronization signal is an interleaved concatenation of two length-31 binary sequences.

$$d(2n) = \begin{cases} s_0^{(m_0)}(n)c_0(n) & \text{in subframes } 0,1,2,3,4 \\ s_1^{(m_1)}(n)c_0(n) & \text{in subframes } 5,6,7,8,9 \end{cases}$$

$$d(2n+1) = \begin{cases} s_1^{(m_1)}(n)c_1(n)z_1^{(m_0)}(n) & \text{in subframes } 0,1,2,3,4 \\ s_0^{(m_0)}(n)c_1(n)z_1^{(m_1)}(n) & \text{in subframes } 5,6,7,8,9 \end{cases}$$

PSS detection

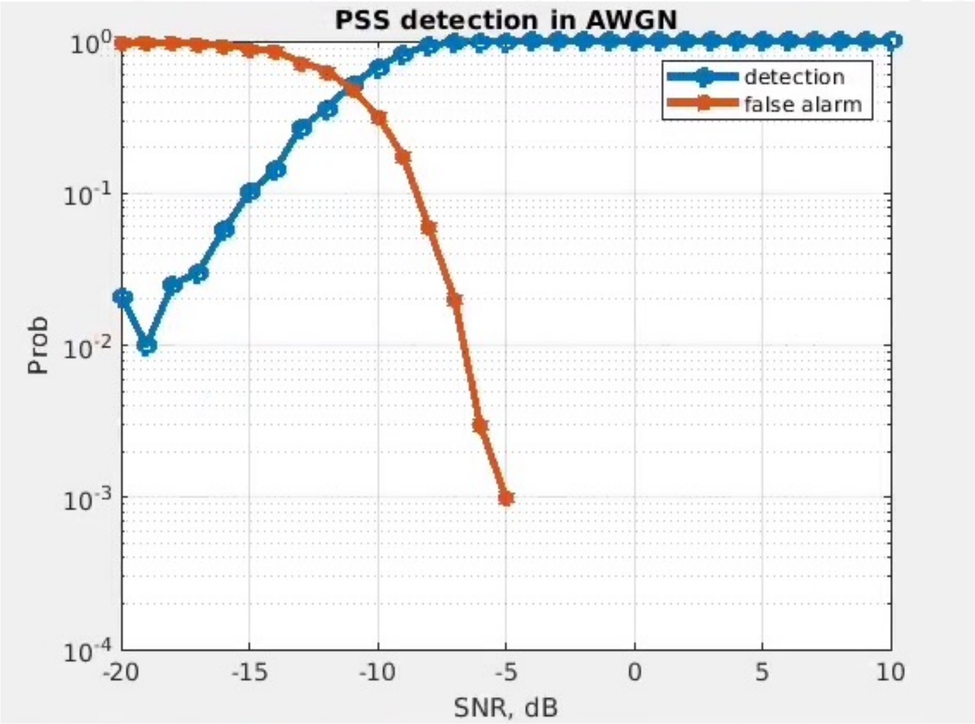
- The UE must detect the PSS without any a priori knowledge of the channel, so noncoherent is required for PSS timing detection. A maximum likelihood detector finds the timing offset $m*$, that corresponds to the maximum correlation

$$m_M^* = \operatorname{argmax}_m \left| \sum_{i=0}^{N-1} Y[i+m] S_M^*[i] \right|^2$$

Y - received samples

S – reference samples to be searched of length M-samples

(one of the 3 PSS sequences)



- **What about False Alarm Rate?**

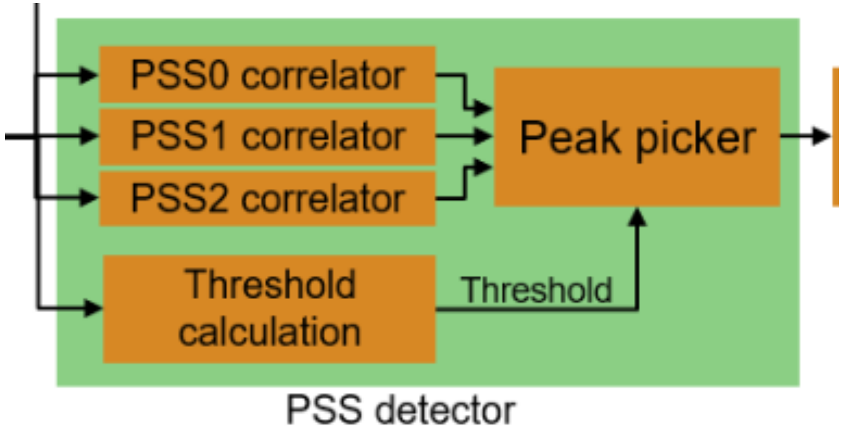
UE goal is to detect the PSS sequence at predefined FA (e.g. 1%)

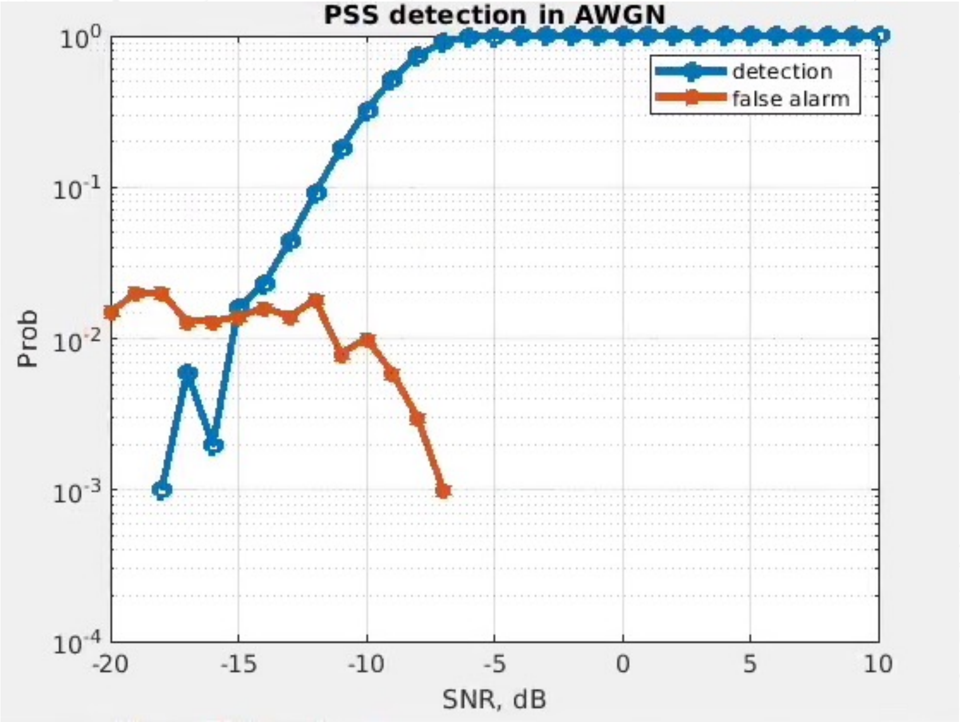
PSS detection

- **What about False Alarm Rate?**

UE goal is to detect the PSS sequence at predefined FA (e.g. 1%)

Use detector with power normalization. The signal power is measured over the correlation length and is used to calculate a threshold for the correlation output. A signal is detected when one of the correlator outputs exceeds the **FIXED** and **PREDEFINED** threshold.





PSS, path loss and AGC

IF intermediate frequency

- Zero-IF receiver architecture
- Path loss affects UE AGC behavior. When signal power is low, AGC increases gain in analog/digital domains. But sometimes maximum analog gain can't boost the incoming signal to the desired level.

Automatic gain control

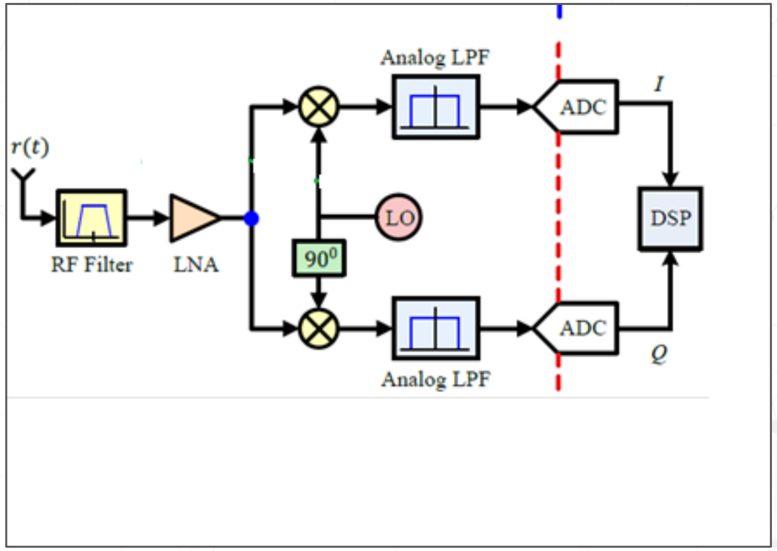
- The lower the input signal at the ADC input – the higher the quantization noise at ADC output and digital 'backoff'.

'backoff' – how much dB digital signal's power is below full scale.

Example: signed 16 bits fixed-point format

1) **0 dB** Backoff means that signal Mean abs(re/im) components are around 2^15-1
2) **12.0412** dB Backoff means that signal Mean abs(re/im) components are around 2^13
3) **84.2884** dB Backoff means that signal Mean abs(re/im) components are around 1

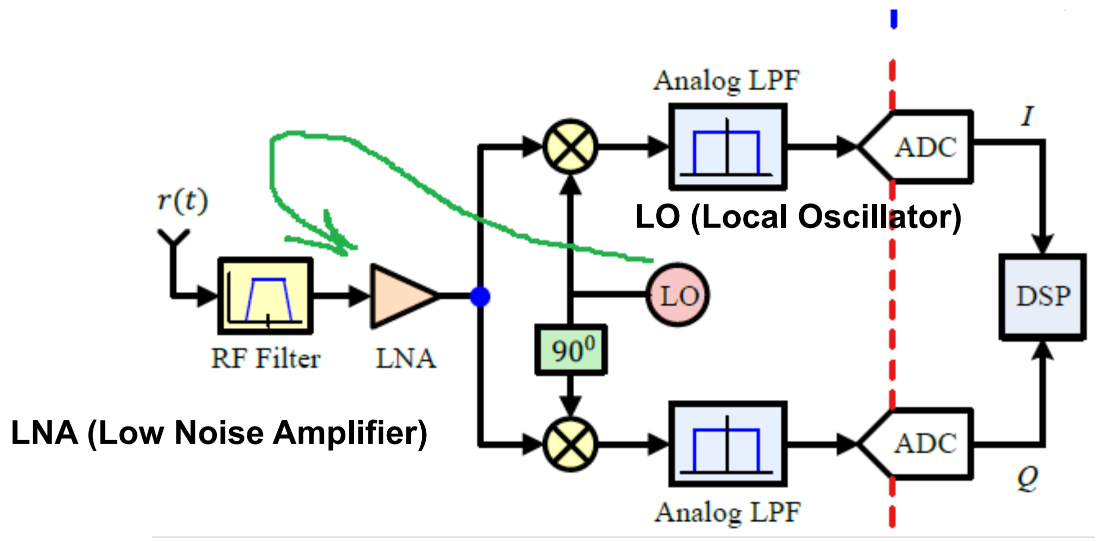
- The PSS detector with power normalization is independent from RX gain.

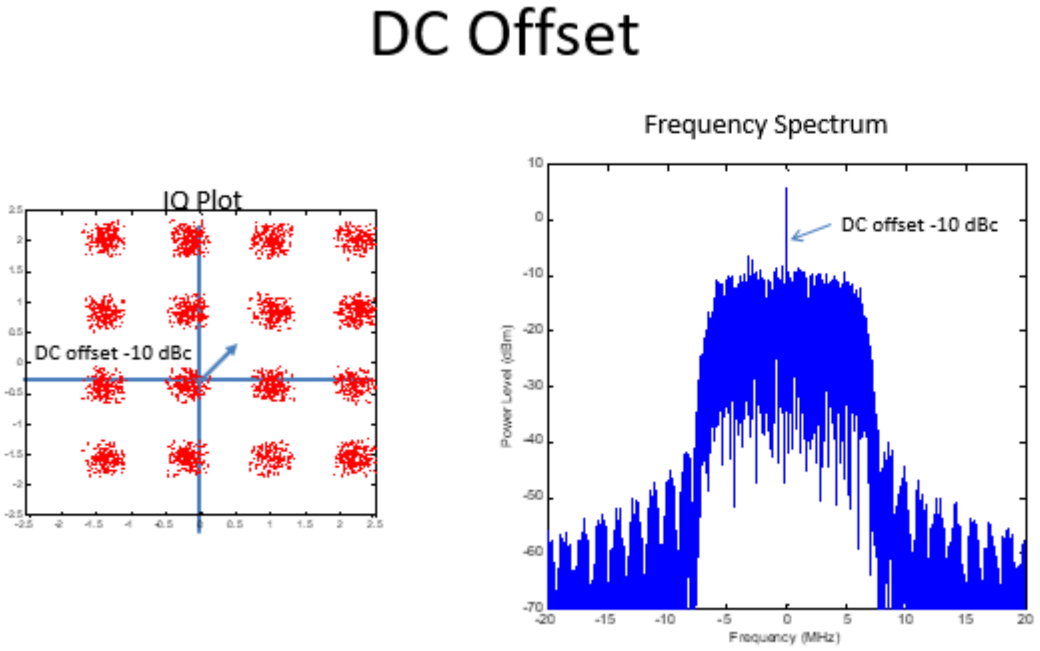


$$\begin{aligned}\mathrm{FSPL(dB)} &= 10\log_{10}\left(\left(\frac{4\pi d f}{c}\right)^2\right)\\ &= 20\log_{10}\left(\frac{4\pi d f}{c}\right)\\ &= 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}\left(\frac{4\pi}{c}\right)\\ &= 20\log_{10}(d) + 20\log_{10}(f) - 147.55,\end{aligned}$$

DC Offset

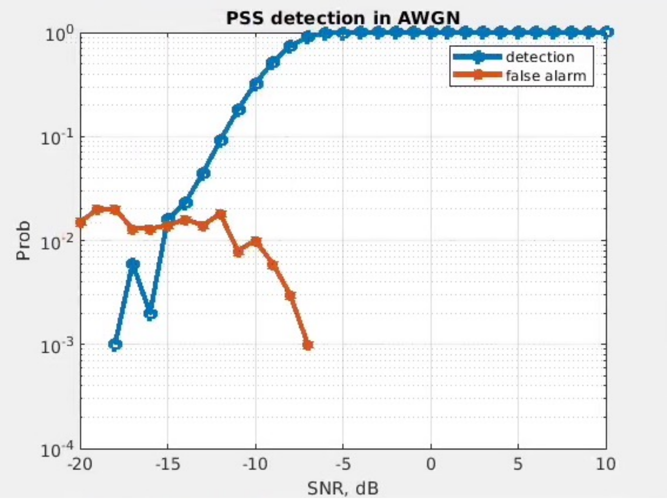
- The isolation between the mixer ports connected to the LO and the LNA output is not infinite which causes the LO sinusoid to leak through to the other input of the mixer. LO leakage.
- There are other aspects as self-mixing, interference and other factors what can cause RX DC offset problem.

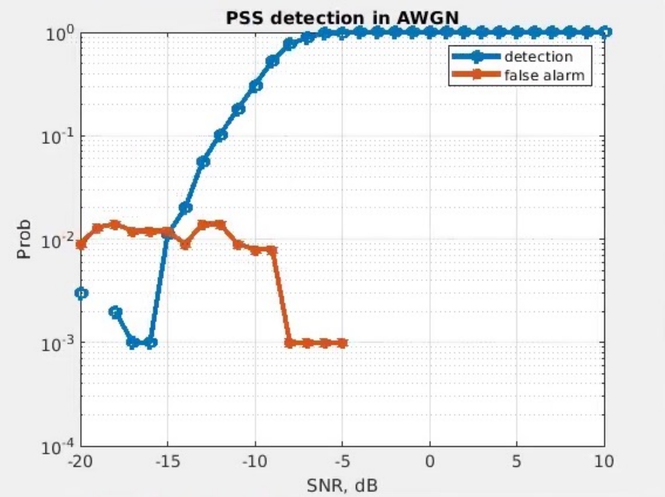




PSS detection curves

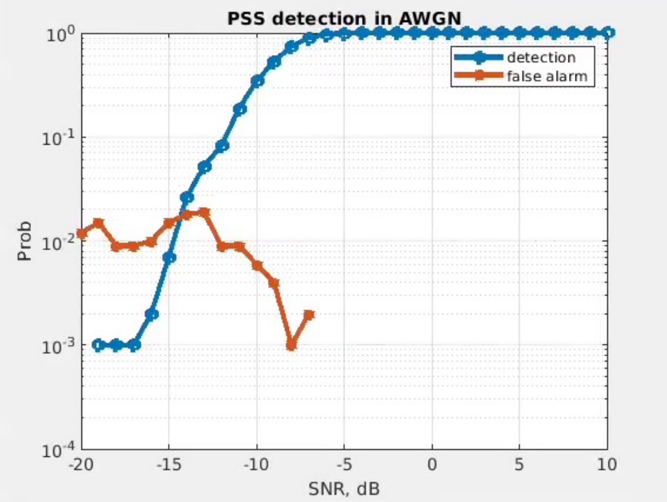
Signal backoff 0 dB
DC backoff +Inf dB

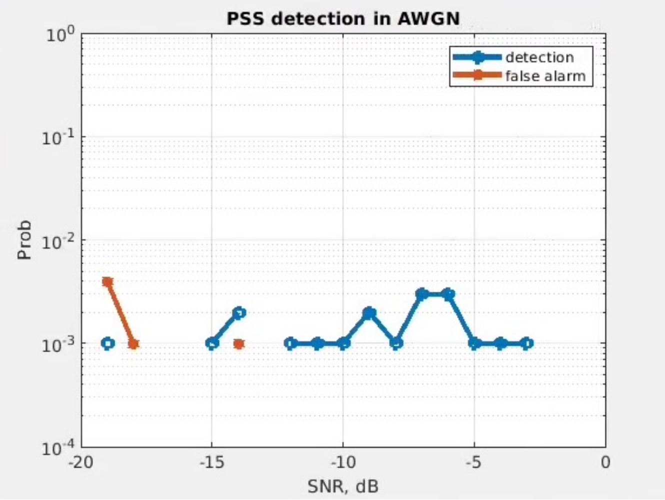




Signal backoff 80 dB
DC backoff +Inf dB

Signal backoff 0 dB
DC backoff 68 dB





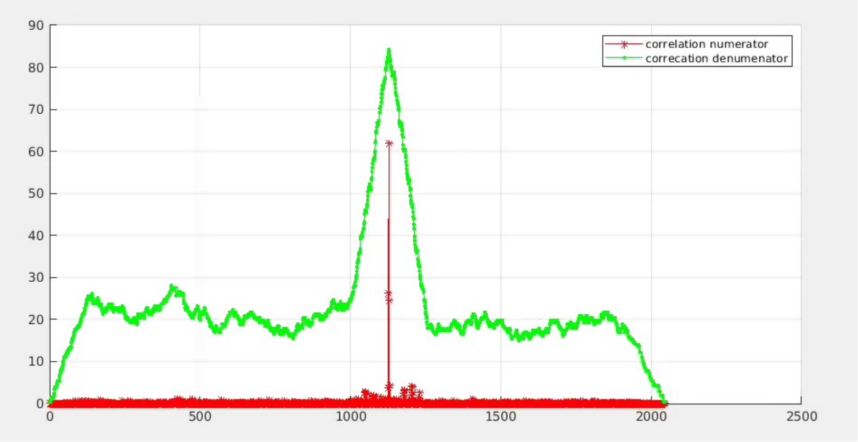
Signal backoff 80 dB
DC backoff 68dB

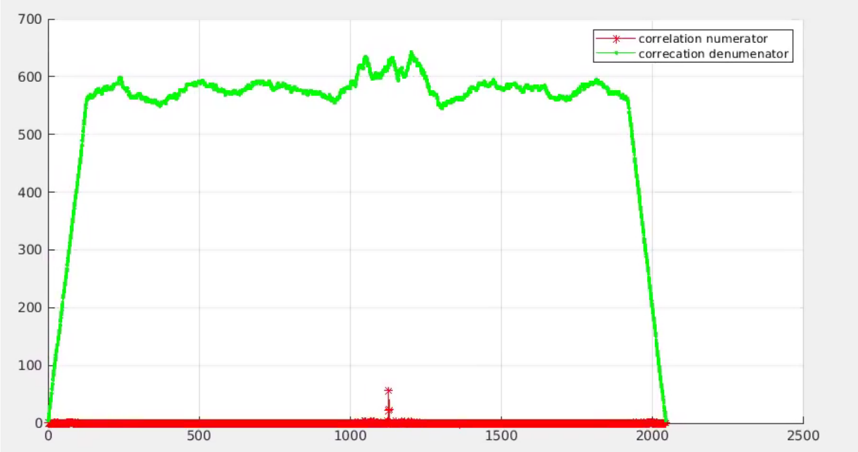
PSS detection curves

- The detection curve with DC offset appeared to be bad
- Actually, if we analyze matched filter output separately from normalization factor one will still observe

Correlation peaks.

- Matched filter decorrelates DC offset power and still provides observable correlation.
- But DC offset power contributes to normalization factor, it becomes bigger.
- So, it’s matters when DC offset power is higher that backoff power.





Q & A