Simulink Design Verifier Report

rev

SJ

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SJ

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차례

1장. Summary

Analysis Information.

Model:	rev
Mode:	Test generation
Test generation target:	Model
Status:	Completed normally
Analysis Time:	9s

Objectives Status.

Number of Objectives:	12
Objectives Satisfied:	12

2장. Analysis Information

차례

Model Information

File:	rev
Version:	1.2
Time Stamp:	Thu Jul 16 16:55:01 2020
Author:	SJ

Analysis Options

Mode:	TestGeneration
Test generation target:	Model
Test Suite Optimization:	CombinedObjectives (Nonlinear Extended)
Maximum Testcase Steps:	10000time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Save Data:	on
Save Harness:	off
Save Report:	off

3장. Test Objectives Status

차례

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Decision	ACC Classical/Switch	trigger > threshold false (output is from 3rd input port)	12	1 [6]
2	Decision	ACC Classical/Switch	trigger > threshold true (output is from 1st input port)	12	1 [6]
3	Decision	ACC Classical/Min	Logic to determine output input 1 is the minimum	12	1 [6]
4	Decision	ACC Classical/Min	Logic to determine output input 2 is the minimum	12	1 [6]
5	Decision	ACC Classical/Saturation	input > lower limit F	12	1 [6]
6	Decision	ACC Classical/Saturation	input > lower limit T	12	1 [6]
7	Decision	ACC Classical/Saturation	input >= upper limit F	12	1 [6]
8	Decision	ACC Classical/Saturation	input >= upper limit T	12	1 [6]
9	Decision	ACC Classical/Switch2	trigger > threshold false (output is from 3rd input port)	12	1 [6]
10	Decision	ACC Classical/Switch2	trigger > threshold true (output is from 1st input port)	12	1 [6]
11	Decision	ACC Classical/Switch1	trigger > threshold false (output is from 3rd input port)	12	1 [6]
12	Decision	ACC Classical/Switch1	trigger > threshold true (output is from 1st input port)	12	1 [6]

4장. Model Items

차례

This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the sldvruntest command.

ACC Classical/Switch

#:	Type	Description	Status	Test Case
1	Decision	trigger > threshold false (output is from 3rd input port)	Satisfied	1 [6]
2	Decision	trigger > threshold true (output is from 1st input port)	Satisfied	1 [6]

ACC Classical/Min

#:	Type	Description	Status	Test Case
3	Decision	Logic to determine output input 1 is the minimum	Satisfied	1 [6]
4	Decision	Logic to determine output input 2 is the minimum	Satisfied	1 [6]

ACC Classical/Saturation

#:	Type	Description	Status	Test Case
5	Decision	input > lower limit F	Satisfied	1 [6]
6	Decision	input > lower limit T	Satisfied	1 [6]

#:	Type	Description	Status	Test Case
7	Decision	input >= upper limit F	Satisfied	1 [6]
8	Decision	input >= upper limit T	Satisfied	1 [6]

ACC Classical/Switch2

#:	Type	Description	Status	Test Case
9	Decision	trigger > threshold false (output is from 3rd input port)	Satisfied	1 [6]
10	Decision	trigger > threshold true (output is from 1st input port)	Satisfied	1 [6]

ACC Classical/Switch1

#:	Type	Description	Status	Test Case
11	Decision	trigger > threshold false (output is from 3rd input port)	Satisfied	1 [6]
12	Decision	trigger > threshold true (output is from 1st input port)	Satisfied	1 [6]

5장. Test Cases

차례

This section contains detailed information about each generated test case.

Test Case 1

Summary.

Length:	0.5 second (6 sample periods)
Objectives Satisfied:	12

Objectives.

Step	Time	Model Item	Objectives
1	0	ACC Classical/Switch ACC Classical/Saturation ACC Classical/Saturation ACC Classical/Switch2 ACC Classical/Switch1	trigger > threshold true (output is from 1st input port) input >= upper limit F input > lower limit F trigger > threshold false (output is from 3rd input port) trigger > threshold false (output is from 3rd input port)
2	0.1	ACC Classical/Saturation	input > lower limit T
3	0.2	ACC Classical/Switch2 ACC Classical/Switch1	trigger > threshold true (output is from 1st input port) trigger > threshold true (output is from 1st input port)
4	0.3	ACC Classical/Saturation	input >= upper limit T
5	0.4	ACC Classical/Switch ACC Classical/Min	trigger > threshold false (output is from 3rd input port) Logic to determine output input 2 is the minimum
6	0.5	ACC Classical/Min	Logic to determine output input 1 is the minimum

Generated Input Data.

Time	0	0.1	0.2	0.3	0.4	0.5
Step	1	2	3	4	5	6
Longitudinal Velocity	5.9566	0	0	0	-66.6667	-66.6667

Time	0	0.1	0.2	0.3	0.4	0.5
Step	1	2	3	4	5	6
Relative Distance	1.9184	0	0	0	0	0
Relative Velocity	-5.4067	27.5	51.25	52.5	0	202.0833