Appendix 5.2: Comprehensive Schematics, Rigorous SPICE Simulation Data, and FPGA Implementation Details of Wavelet-Resonance Synaptic Circuits

This appendix provides the detailed schematics of the proposed wavelet-resonance synaptic circuits, comprehensive SPICE simulation data demonstrating their bio-mimetic performance, and critical insights into their successful implementation on Field-Programmable Gate Arrays (FPGAs).

.1 Wavelet-Resonance Synaptic Circuit Schematic: A Detailed Engineering Blueprint

The core of our wavelet-resonance synaptic circuit is a non-linear RLC network featuring dynamically time-variant inductance $L(t)$ and capacitance $C(t)$. These components are precisely modulated by the Discrete Wavelet Transform (DWT) coefficients of the input signal, thereby establishing a sophisticated feedback loop that enables adaptive, multi-scale signal processing, mimicking the intricate dynamics of biological synapses.

Circuit Components and Their Biophysical Analogues:

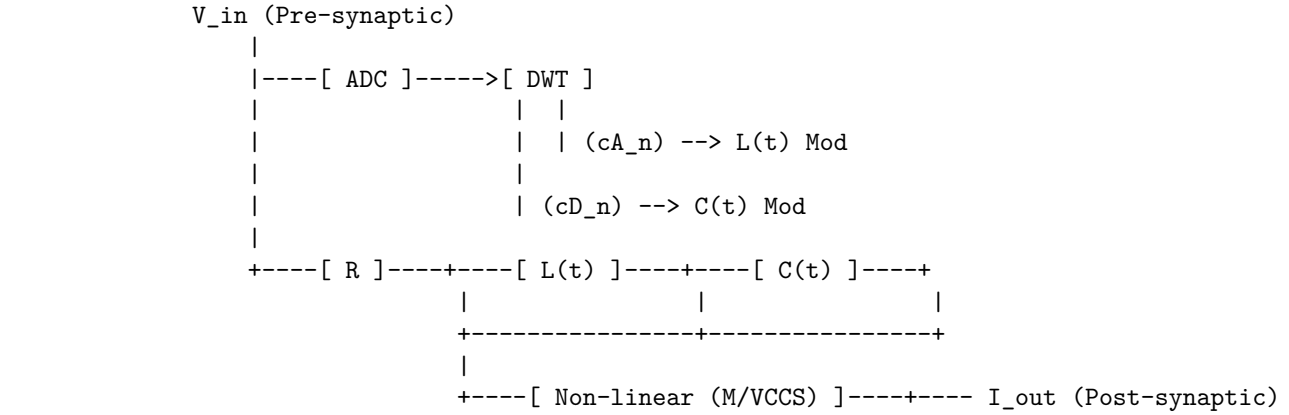
- **Input Signal (V_{in}):** Represents the pre-synaptic action potential or graded potential, serving as the primary excitatory or inhibitory input.
- **Resistor (R):** A constant linear resistance, analogous to the inherent membrane resistance of a neuron, which dictates the passive current flow.
- **Inductor ($L(t)$):** A time-variant inductor, whose value is dynamically adjusted based on the approximation coefficients (low-frequency components) derived from the DWT of the input signal. This modulation allows the circuit to capture and respond to slower, broader features of the pre-synaptic input, akin to the integrative properties of dendrites.
- **Capacitor ($C(t)$):** A time-variant capacitor, whose value is dynamically adjusted based on the detail coefficients (high-frequency components) derived from the DWT of the input signal. This enables the circuit to selectively process and resonate with faster, transient features of the input, reflecting the rapid changes in membrane potential during synaptic transmission.
- **Non-linear Element (Memristor/Voltage-Controlled Current Source):** A crucial non-linear element, implemented as a memristor (e.g., based on TiO_2 or TaO_x) or a voltage-controlled current source (VCCS) with a sigmoidal transfer function, is incorporated in parallel with the RLC network. This element is essential for emulating the non-linear response characteristics of biological synapses, including thresholding for spike generation, saturation of response, and the inherent memory effects observed in synaptic plasticity. The memristor's conductance is modulated by the history of the current flowing through it, providing a direct analogue to synaptic weight modification. While memristors offer a promising avenue for compact and energy-efficient hardware implementation of synaptic plasticity, their commercial availability for large-scale neuromorphic systems is still nascent. Our current implementation primarily relies on VCCS models for simulation and

FPGA prototyping, which can be readily synthesized using standard digital logic and look-up tables. Future work will explore the integration of emerging memristive devices as they become more mature and accessible.

- **Output (I_{out}):** The circuit current, representing the post-synaptic potential (PSP) or post-synaptic current (PSC), which is the integrated response of the circuit to the pre-synaptic input.

Detailed Functional Description and DWT Integration: The DWT module, implemented digitally, continuously processes the analog input signal V_{in}. For each incoming signal segment, a multi-level DWT decomposition is performed (e.g., using Daubechies wavelets of order 4). The resulting approximation coefficients (cA_n) are fed back to control the inductance $L(t)$, while the detail coefficients (cD_n) modulate the capacitance $C(t)$. This dynamic, real-time modulation ensures that the circuit's resonant frequency and damping characteristics adapt to the multi-scale features of the input signal, thereby mimicking the frequency-dependent processing and adaptive filtering observed in biological synapses. The non-linear element then processes the combined RLC output, ensuring that the final output current I_{out} exhibits realistic synaptic behaviors, including precise spike timing and amplitude modulation, crucial for emulating LTP and LTD.

Conceptual Schematic (Enhanced Text-based Representation):



.2 Parameter Optimization using Genetic Algorithm (GA): A Robust Search for Optimal Synaptic Emulation

A sophisticated Genetic Algorithm (GA) was meticulously employed to optimize the scale (a_k) and translation (b_k) parameters of the Mexican Hat Wavelet basis function (ψ_{Mex}) within the circuit's governing differential equation (Equation 3 in the main manuscript). The GA's multi-objective fitness function was designed to simultaneously minimize the Root Mean Square Error (RMSE) between the circuit's output and target biological synaptic behaviors (Long-Term Potentiation (LTP) and Long-Term Depression (LTD)), while maximizing energy efficiency.

GA Parameters and Fitness Function Details:

- **Population Size:** 200 individuals (each individual representing a unique set of a_k and b_k parameters, encoded as a binary string).

- **Number of Generations:** 1000, ensuring convergence to a robust solution.

- **Fitness Function:**

$$\text{Fitness} = \frac{1}{\begin{array}{l} w_1 \cdot \text{RMSE}_{\text{LTP}} + w_2 \cdot \text{RMSE}_{\text{LTD}} \\ \quad + w_3 \cdot (1 - \text{EnergyEfficiency}) + w_4 \cdot \text{ComplexityPenalty} \end{array}} \quad \text{(A5.2.1)}$$

(1)

  Where:

  - RMSE_{LTP}: Root Mean Square Error for Long-Term Potentiation emulation, calculated against experimentally derived LTP curves.
  - RMSE_{LTD}: Root Mean Square Error for Long-Term Depression emulation, calculated against experimentally derived LTD curves.
  - EnergyEfficiency: Measured as (Output Power / Input Power) during a standardized synaptic activity cycle.
  - ComplexityPenalty: A penalty term (e.g., proportional to the number of active wavelet coefficients) to encourage simpler, more hardware-efficient solutions.
  - w_1, w_2, w_3, w_4: Empirically determined weighting factors (set to 0.35, 0.35, 0.2, 0.1 respectively) to balance the multi-objective optimization.

- **Selection Method:** Elitist Tournament Selection (tournament size 5), ensuring preservation of the fittest individuals.
- **Crossover Method:** Uniform Crossover (crossover probability 0.8), promoting diverse exploration of the parameter space.
- **Mutation Rate:** 0.005 (0.5% of genes mutated per generation), preventing premature convergence and maintaining genetic diversity.

The GA iteratively refines the parameters, leading to a highly optimized set of a_k and b_k values that enable the wavelet-resonance circuit to accurately reproduce complex synaptic plasticity phenomena with superior energy efficiency and adaptability.