ADQ14 Hard X-Ray Monitor

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DMCS

Contents

1 INTRODUCTION

1.1 DOCUMENT STRUCTURE

This document describes the functionality of a firmware package developed for the ADQ14 digitizer. The solution implements a real time Pulse Height Analyzer for exponential pulses, intended for use in Hard X-Ray Monitors. The Pulse Height Analyzer firmware is built on top of the SPDevices ADQ14 DevKit. Initial chapters of this paper go over the digitizer board itself, highlighting its features and limitations. The custom firmware solution is built on top of a development kit provided by SPDevices with ADQ14.

2 ADQ14

2.1

3 SPDEVICES DEVKIT

The custom spectroscopy firmware is built on top of a development kit provided with the digitizer board. The base system is referred to as the DevKit by the manufacturer. A full documentation of the DevKit can be downloaded from the manufacturer's website. An offline copy is included with the firmware source code in the `documentation` folder.

3.1 THE CONCEPT OF USER LOGIC

The modules provided with the DevKit control the Analog Digital Converter, triggering, packeting, the DRAM data queue and the PCIe interface. The subsystems responsible for these parts of the pipeline are provided in the form of encrypted IP cores and cannot be modified. Two modifiable modules, referred to as User Logic 1 and 2, are exposed in between, enabling the use of entirely custom algorithms at two points in the data flow. User Logic 1 is placed right before the trigger control, enabling the use of detection or smoothing filters with the digitizer's level trigger feature. User Logic 2 allows for modifications being placed right before the individual consecutive samples are packed into records, assigned metadata and queued in the DRAM for transmission to the host computer. The DevKit structure, with the placement of the User Logic modules highlighted in gold, is shown in Figure 1. Both modules are described in greater detail in the next chapters.

FIGURE 1: DEVKIT OVERVIEW

3.2 SAMPLES IN THE FPGA

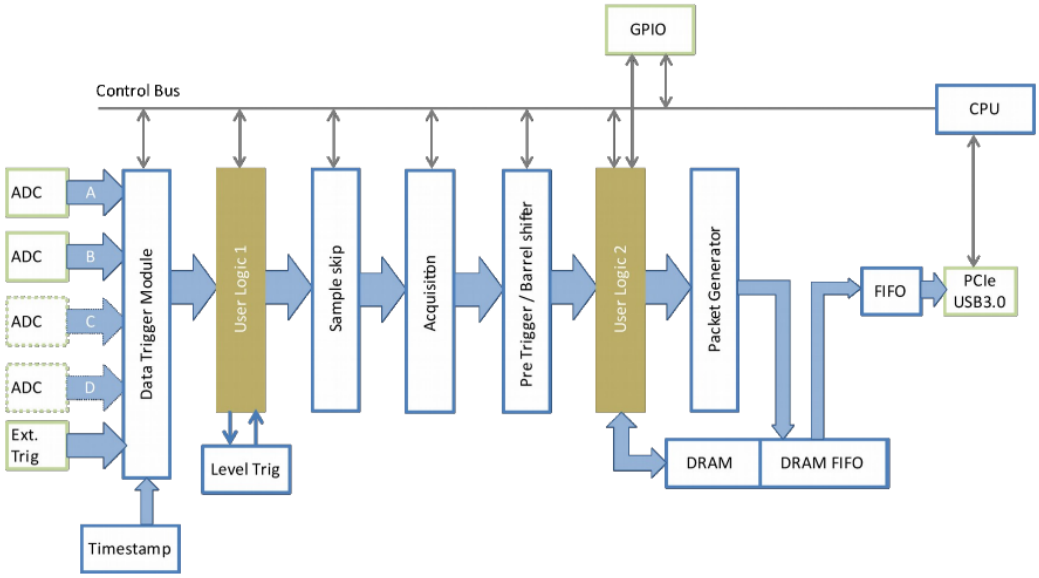

FIGURE 2: PRIMARY DATA FLOW IN THE FPGA

The digitizer's ADC is capable of sampling the signal at a rate up to 1 GS/s or 1 GHz. The FPGA is clocked at 250 MHz, resulting in a parallel design where each channel produces 4 new consecutive samples for the FPGA on each clock cycle. The ADCs produce 14-bit samples. The raw signal is however subject to a digitial gain and shift. Two additional fractional bits are appended to the 14-bit samples before calculations. Two configurations are factored in the gain and shift calculations. The board comes preconfigured with a factory calibration that is always applied. A second configuration is made available to the users and can be freely modified from base values to apply custom digital signal shift or change the gain.

3.3 DATA FLOW IN USER LOGIC 1

After the digital gain and shift, the 16-bit samples are packed into a data bus and made available at the User Logic 1 module. This component is located before the level trigger. By default the raw sample data is passed on to the triggering module unchanged. If the device trigger mode is set to the level trigger, digital filters can be implemented in User Logic 1 to modify the trigger behaviour. In initial testing a configurable moving average smoothing filter was placed in this module to reduce the influence of noise. At one point a boxcar and a trapezoidal filters were successfully implemented for pulse detection. These filtering modules were created in an abstract manner and can be combined to modify the level trigger behaviour to a desired shape and signal-to-noise ratio.

The samples that are passed to the level trigger module can differ from those that are sent further down the processing pipeline, meaning that it is possible to trigger on appropriately filtered data, while still storing unmodified samples at the host PC. The current version of the firmware

does not perform any filtering in this part of the firmware. All spectroscopy logic has been moved to User Logic 2, however the filter modules remain usable and can be reintroduced if the need appears.

3.4 DATA FLOW IN USER LOGIC 2

User Logic 2 deals with data that has passed through User Logic 1, decimation and shifting to accomodate for pretrigger (horizontal shift). User Logic 2 is responsible for tagging the start and end of a single acquisition window (record). Further DevKit modules can then then pack and queue the records for transmission. User Logic 2 also inserts header data containing the metadata. The record length is fixed by default and set

All spectroscopy logic in the current firmware revision is contained within User Logic 2. Appendix A contains a detailed description of the input and output signals available in the User Logic modules, mostly useful for firmware developers.

3.5 DATA PATHS IN THE FPGA

Records built of the 16-bit samples, together with the metadata are initially stored in the digitizer's internal DRAM. This memory forms a FIFO queue, that is periodically transferred over to the host PC. The ADQ14's RAM has a capacity of 2 GB. With two bytes per sample up to a billion samples can be queued for data transfer before overflow leads to data loss. With up to a billion samples being generated every second for every active channel, this memory must be efficiently transferred. Two data paths exist within the firmware for exchanging data with the host PC.

3.5.1 DMA

After being packed in records and queued in the digitizer's DRAM, the acquired samples are sent using Direct Memory Access. This path makes it possible to write data directly to the host PC's RAM, without the need of CPU involvment. Naturally, the host PC's RAM is not unlimited, so the data must be processed (e.g. saved to a hard drive) at a rate comparable to the DMA transfers. DMA is a one-way path, so data can be transferred from the digitizer to the host PC, but not the other way around. Any data can be inserted in place of the samples for each channel to leverage the fast data path. The custom Pulse Height Analyzer relies on this fact to periodically transfer computed spectras.

3.5.2 USER REGISTERS

A substantially slower two-way data path is available through the user registers (top data bus on Figure 2). Both User Logic modules implement a small individually addressable memory block, that can be written to or read from by both the host PC and the FPGA. The memory structure contains 32-bit integers. 2^{14} addressable words are available in User Logic 1, and 2^{19} in User Logic

2. First 4 positions in both modules are reserved for internal use by the DevKit and cannot be modified in the custom firmware. The custom PHA firmware relies on User Registers primarily for transferring configuration settings to the FPGA. The current version of the firmware also enables spectra transfer through this data path for testing purposes.

3.6 BYPASSING USER LOGIC

4 CUSTOM FIRMWARE

4.1 CORE FIRMWARE FUNCTIONALITY

The firmware spectroscopy solution consists of four primary subsystems:

- Pulse Detection Module
- Pulse Shaping Module
- Pulse Sampler
- Spectrum Storage and Transfer

4.2 PULSE DETECTION MODULE

4.3 PULSE SHAPING MODULE

4.4 PULSE SAMPLER

4.5 SPECTRUM STORAGE AND TRANSFER

5 SECOND SECTION

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5.1 FIRST SUBSECTION

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TABLE 1: SAMPLE TABLE.

Value 1	Value 2	Value 3	Value 4
odd	odd	odd	1.00
even	even	even	1.00
odd	odd	odd	1.00
even	even	even	1.00

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FRAME 1: SAMPLE FRAME

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A USER LOGIC DATA BUS

A.1 USER LOGIC 1

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A.2 USER LOGIC 2

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