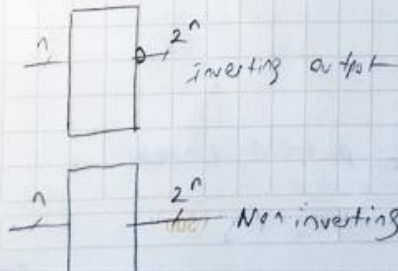


Combinational Logic Design with Decoder

Decoder



Logic function

Canonical SOP form

Canonical POS form

Logic function Canonical for the circuit

OSOW

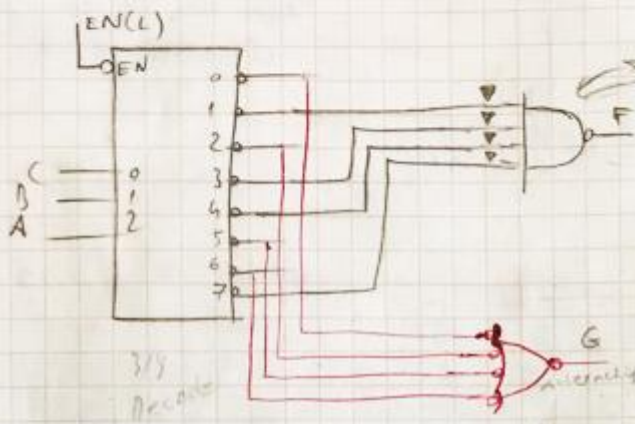
$$F(A,B,C) = \sum m(1,3,4,7)$$

$$G(A,B,C) = \prod M(0,2,5,6)$$

İki tane 3 girişli dekodör kullanılarak
bu fonksiyonlar gerçekleştirilebilir.

$$F = m_1 + m_3 + m_4 + m_7 = \overline{M_1} \cdot \overline{M_3} \cdot \overline{M_4} \cdot \overline{M_7} \text{ NAND}$$

$$\overline{M_1} = M_1$$

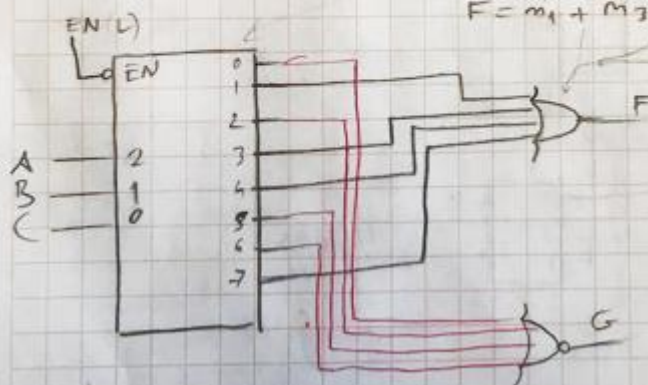


dekodörün çıkışları
eviren olarak
max term üretir

F fonksiyonunu paralelleştiririz

$$G = M_0 \cdot M_2 \cdot M_5 \cdot M_6$$

Evirenlerin sırasıyla yapılabilir



$$F = m_1 + m_3 + m_4 + m_7$$

$$G = M_0 M_2 M_5 M_6$$

$$= m_0 + m_2 + m_5 + m_6$$

Arithmetic Circuits

Half Adder

Full Adder

Full Subtractor

Multiplier

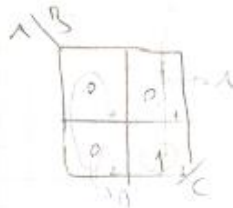
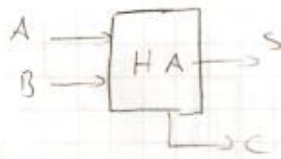
Divider

Comparator

Half Adder

a) using NAND

b) " NOR



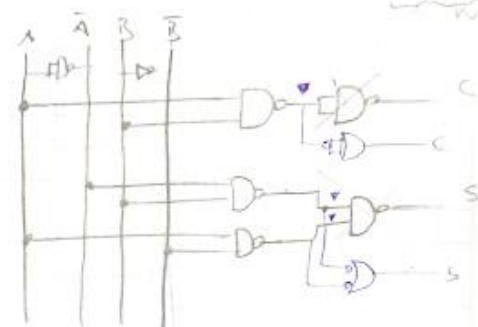
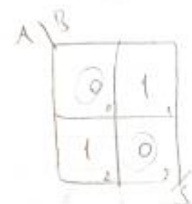
$$C = AB$$

$$S = \overline{A}B + A\overline{B}$$

$$C = \overline{A}B$$

$$S = \overline{A}B + A\overline{B} = \overline{A}B + A\overline{B}$$

Dec	A	B	C	S
0	0	0	0	0
1	0	1	0	1
2	1	0	0	1
3	1	1	1	0

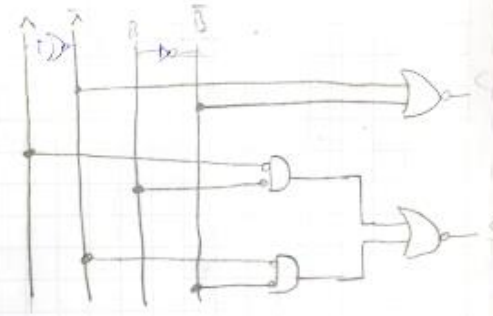


b) $C = A \cdot B$

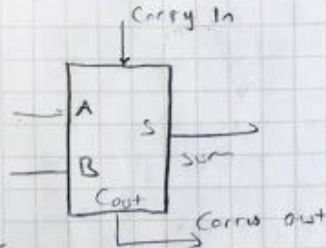
$$S = (A+B) \cdot (\overline{A} + \overline{B})$$

$$C = \overline{A} \cdot B = \overline{A} + \overline{B}$$

$$S = (A+B) \cdot (\overline{A} + \overline{B}) = \overline{A} + B + \overline{A} + B$$



Full Adder



Dec	A	B	Cin	Cout	S
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

Cin	A	B	Cout	S
-----	---	---	------	---

OSOW

$(A+B)$

A \ B	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$(A+C_i)$ $(B+C_i)$

$(A+B+C_i)$ $(A+B+C_i)$ $(A+B+C_i)$

A \ B	00	01	11	10
0	0	1	0	1
1	1	0	1	0

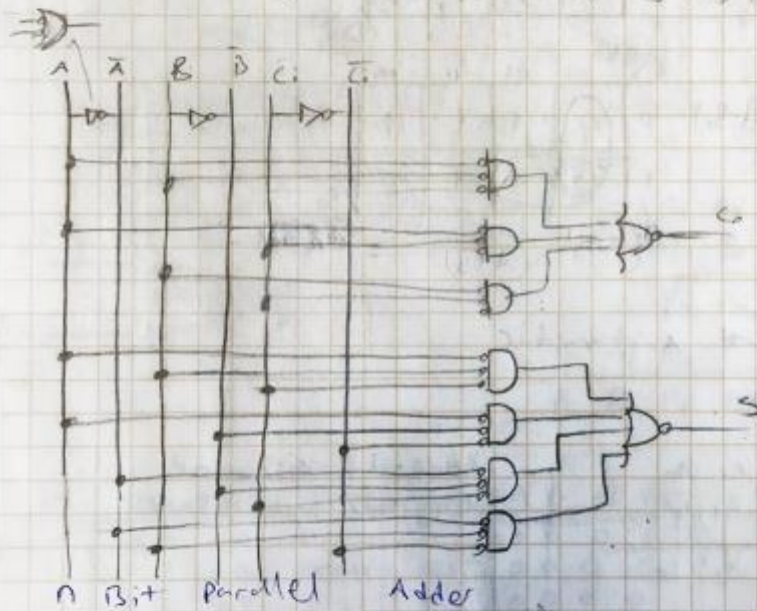
$(A+B+C_i)$ $(A+B+C_i)$ $(A+B+C_i)$

$$C_o = (A+B) \cdot (A+C_i) \cdot (B+C_i)$$

$$= (A+B) + (A+C_i) + (B+C_i)$$

$$S = (A+B+C_i) \cdot (A+B+C_i) \cdot (A+B+C_i) \cdot (A+B+C_i)$$

$$(A+B+C_i) + (A+B+C_i) + (A+B+C_i) + (A+B+C_i)$$



1 Bit Parallel Adder

