

fonksiyonun gerselleştirilme
dijital olarak

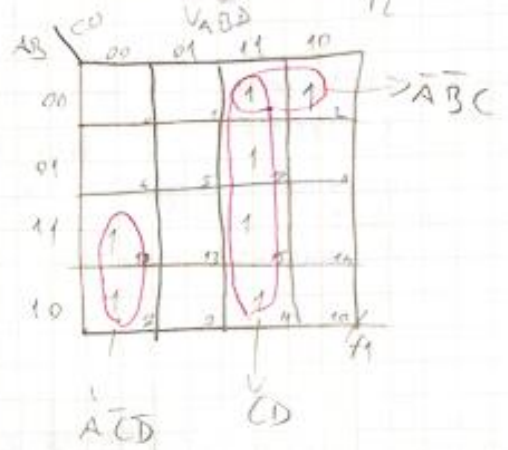
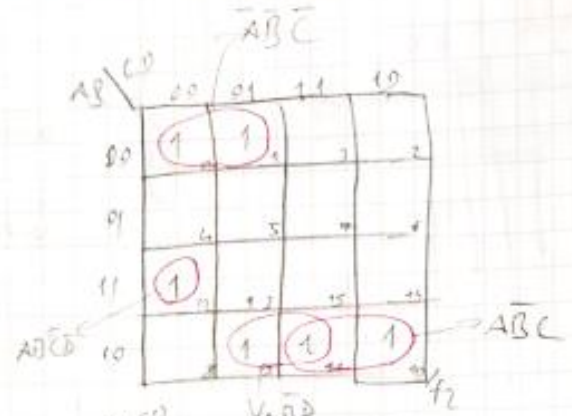
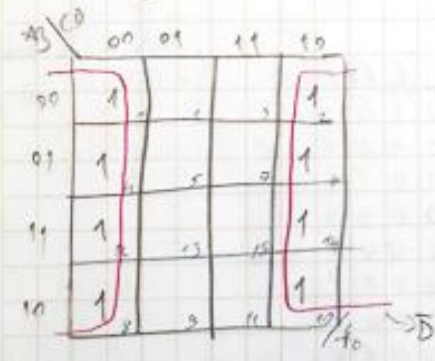
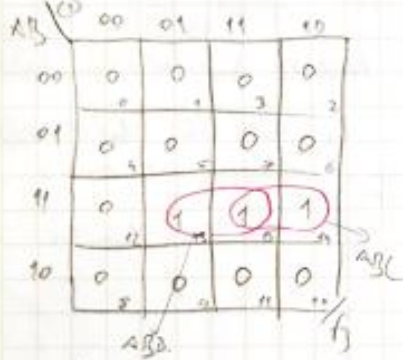
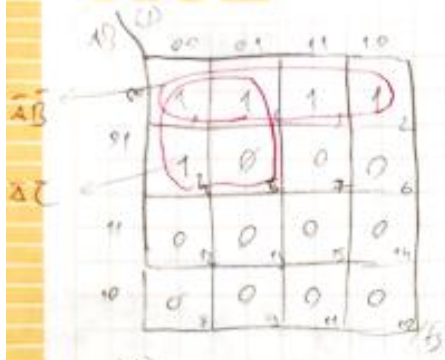
$f = x - 5$ fonksiyonunu yalnızca NAND kapılarını kullanarak
gerçekleştir, x burada 4 bitlik bir dijital
negatif değere karşılık bir lamba,
fonksiyonun mutlak değeri yeti lamba ile
tersinir edilir.

Çözüm



	A	B	C	D	$f = x - 5$	f_3	f_2	f_1	f_0
0	0	0	0	0	-5	1	0	1	0
1	0	0	0	1	-4	1	0	1	0
2	0	0	1	0	-3	1	0	0	1
3	0	0	1	1	-2	1	0	0	1
4	0	1	0	0	-1	1	0	0	0
5	0	1	0	1	0	0	0	0	0
6	0	1	1	0	1	0	0	0	0
7	0	1	1	1	2	0	0	0	0
8	1	0	0	0	3	0	0	0	0
9	1	0	0	1	4	0	0	0	0
10	1	0	1	0	5	0	0	0	0
11	1	0	1	1	6	0	0	0	0
12	1	1	0	0	7	0	0	0	0
13	1	1	0	1	8	0	0	0	0
14	1	1	1	0	9	0	0	0	0
15	1	1	1	1	10	0	0	0	0

OSOW



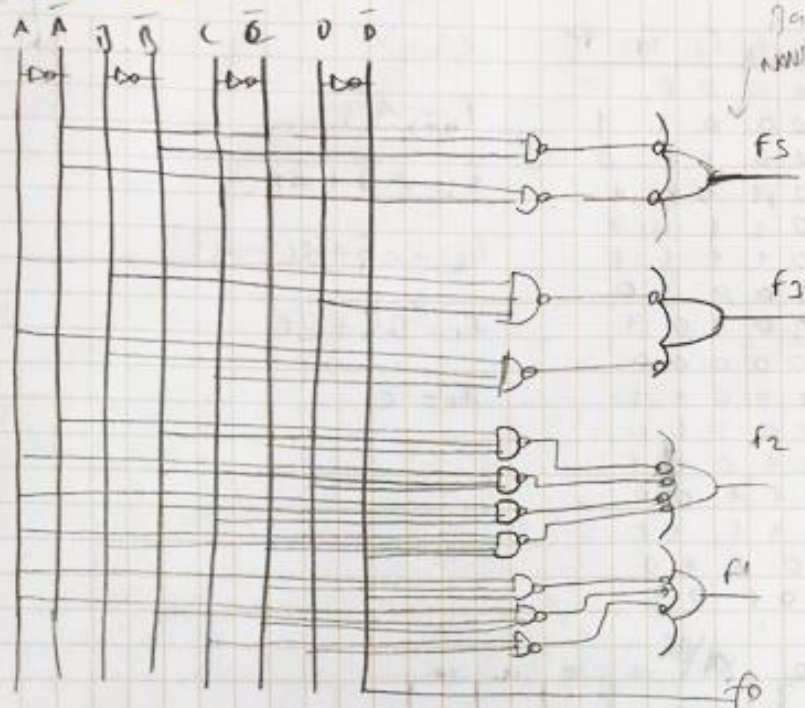
$$f_5 = \bar{A}\bar{B} + \bar{A}\bar{C} = \bar{A}\bar{B} \cdot \bar{A}\bar{C}$$

$$f_3 = \bar{A}BD + ABC =$$

$$f_2 = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}D + \bar{A}B\bar{C} + \bar{A}BC$$

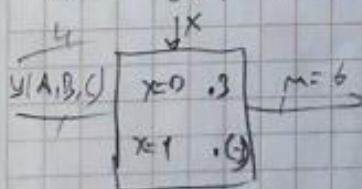
$$f_1 = \bar{A}\bar{C}D + \bar{A}BC + CD$$

$$f_0 = \bar{D} = D$$



Not: negatif girişler için
AND'ler negatifini kullanır

Bir logic devresi $y(A,B,C)$ 3 bitlik binary veri girişi X ile kontrol girişidir. $X, 0$ olduğu zaman $y, +3$ ile $X, 1$ olduğu zaman $y, -3$ ile çalışır. Böyle bir devreyi yalnızca nasıl kullandık gösterdik. Böyle bir devreyi yalnızca nasıl kullandık gösterdik. Böyle bir devreyi yalnızca nasıl kullandık gösterdik.



$3 \rightarrow 3 + 21$
 $-3 \rightarrow -21$

OSOW

Dec	X	Y	A	B	C	f	f ₅	f ₄	f ₃	f ₂	f ₁	f ₀
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	3	0	0	0	0	1	1
2	0	0	1	0	1	6	0	0	0	1	1	0
3	0	0	1	1	1	5	0	0	1	0	0	1
4	0	1	0	0	1	12	0	0	1	1	0	0
5	0	1	0	1	1	15	0	0	1	1	1	1
6	0	1	1	0	1	18	0	1	0	0	1	0
7	0	1	1	1	1	21	0	1	0	1	0	1
8	1	0	0	0	1	3	1	0	0	0	1	1
9	1	0	0	1	1	6	1	0	0	1	1	0
10	1	0	1	0	1	9	1	0	1	0	0	1
11	1	0	1	1	1	12	1	0	1	1	0	0
12	1	1	0	0	1	15	1	0	1	1	1	1
13	1	1	0	1	1	18	1	1	0	0	1	0
14	1	1	1	0	1	21	1	1	0	1	0	1

$$f_5 = X$$

$$f_4 = AB$$

$$f_3 = A\bar{B} + \bar{A}BC$$

$$f_2 = A\bar{B} + AC + \bar{A}BC$$

$$f_1 = B\bar{C} + \bar{B}C$$

$$f_0 = C$$

X \ BC	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	1
10	1	1	1	1

X \ BC	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	1	1
10	1	1	1	1

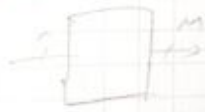
X \ BC	00	01	11	10
00	0	0	1	0
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

X \ BC	00	01	11	10
00	0	0	0	1
01	1	1	1	0
11	1	1	1	0
10	0	0	1	1

X \ BC	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

X \ BC	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

Multiple Output Minimization



or
 $f_1 = \sum m(0, 3, 4, 5, 6)$

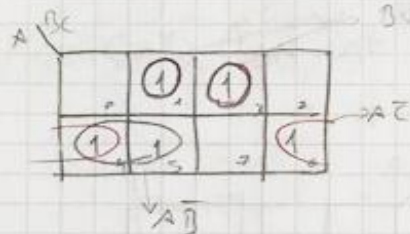
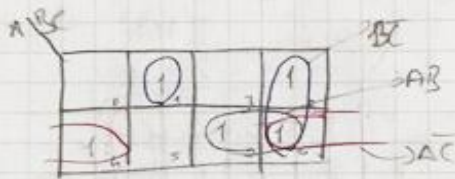
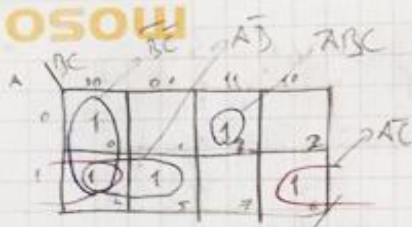
$$f_2 = \sum m(1, 2, 4, 6, 7)$$

$$f_3 = \sum m(1, 3, 4, 5, 6)$$

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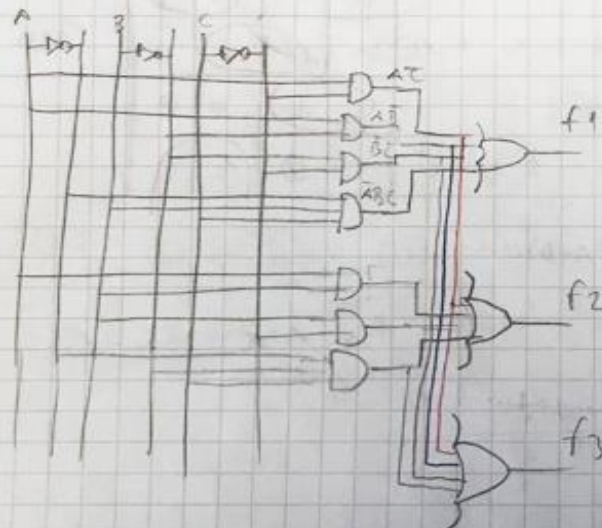
OSOW



$$f_1 = A\bar{C} + \bar{A}\bar{B} + \bar{A}BC$$

$$f_2 = A\bar{C} + AB + B\bar{C} + \bar{A}\bar{B}C$$

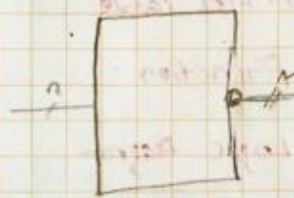
$$f_3 = A\bar{C} + \bar{A}\bar{B} + \bar{A}BC + \bar{A}\bar{B}C$$



COMBINATIONAL LOGIC DESIGN

Gate Perspective (Approach)

Modular Perspective (Approach)



The Building Blocks

- 1) Data Manipulation
- 2) Data Conversion
- 3) Data selection from various sources
- 4) Data Routing from source to various destinations
- 5) Data Error Detection
- 6) Data busing from one part of the digital system to another

Arithmetic Type Multipurpose Circuit

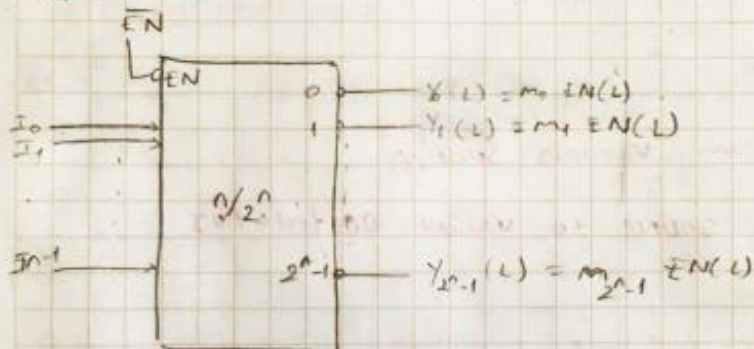
ADDER
SUBTRACTOR
MULTIPLIER
DIVIDER
COMPARATOR
PARITY GENERATOR
ERROR DETECTOR

DECODER - ENCODER
CODE CONVERTER
MULTIPLEXER - DEMULTIPLEXER
SHIFTER
ALU (Arithmetic and Logic unit)
ROM (Read only memory)
PLA (Programmable Logic Array)
Array Logic

DESIGN PROCEDURE

- 1- Understand the Device
- 2- State the Algorithm
- 3- Construct a truth Table
- 4- Obtain output Function
- 5- Construct the Logic Diagram
- 6- Check (Test) the Results

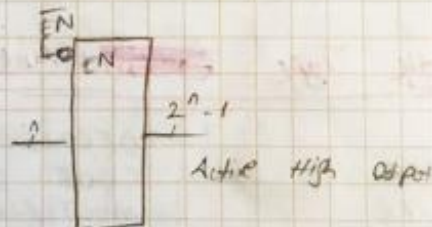
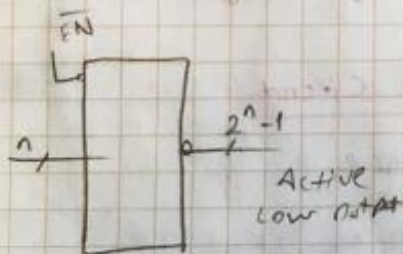
DECODER AND ENCODER



$$m_i(L) = m_i(H)$$

$$M_i(L) = m_i(H)$$

$$y_i = m_i EN(L)$$

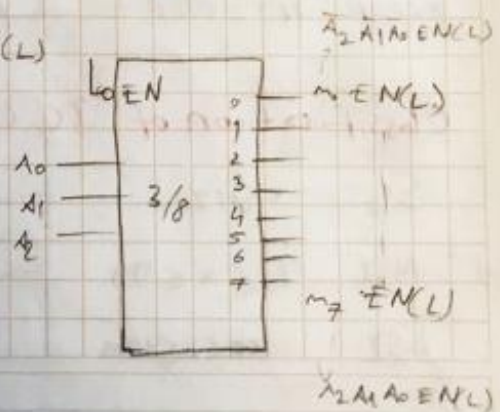


number EN in decimal is written in the output

\overline{EN}	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	1	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

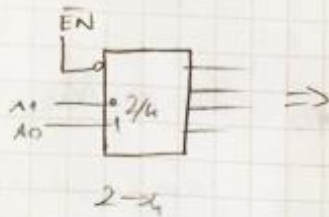
$$y_i = m_i EN(L)$$

Decoder \rightarrow an output for each minterm or maxterm written directly

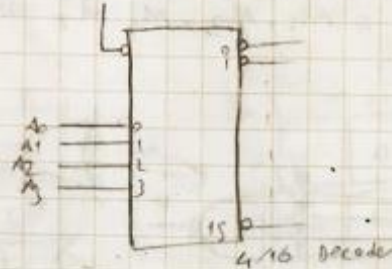


$$Y_2 A_1 A_0 EN(L)$$

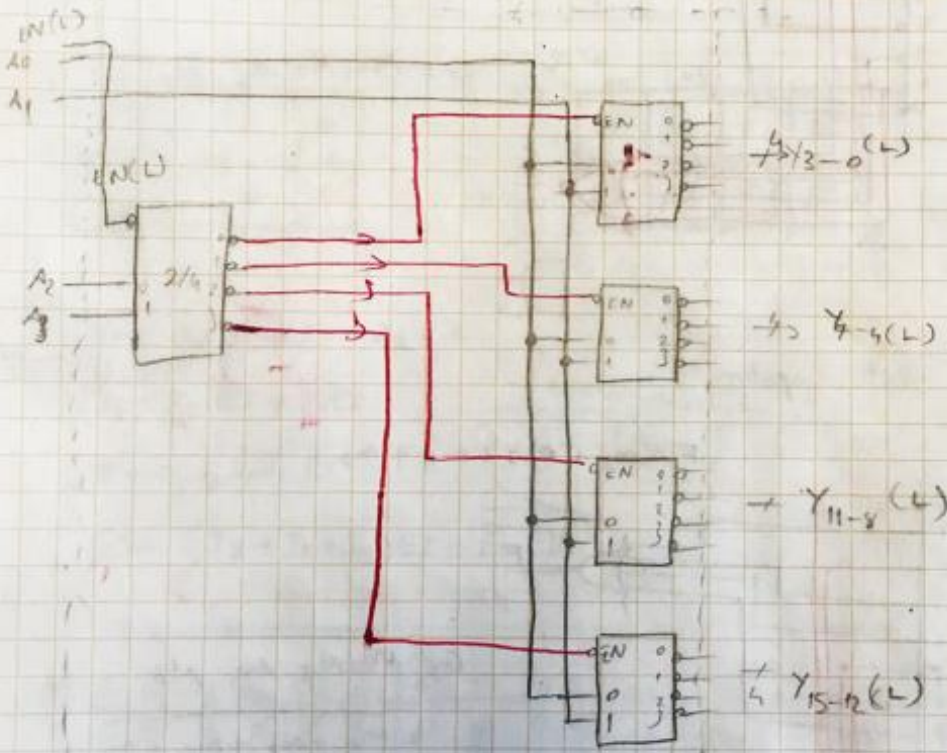
EXPANSION FORM



4 → 16 decoder

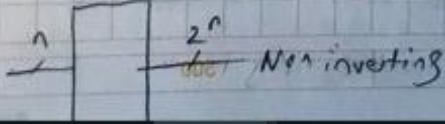
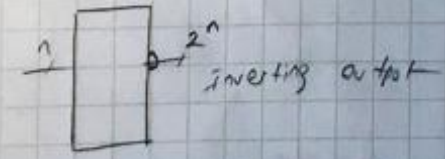


2/4 der 4/16 decoder
also drei in



Combinational Logic Design with Decoder

Decoder



Logic function

Canonical SOP form

Canonical POS form

Logic function Canonical
for the circuit