EEE 202 CIRCUIT THEORY
LAB 5

Band-Pass Filter

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Section 3

SW Implementation

Introduction

The aim of this lab is to design a band-pass filter for 50Ω load resistance with given gain graph shown in Figure.1.

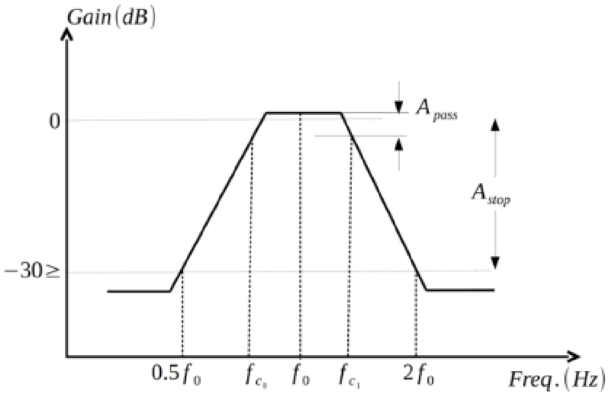

Figure.1 Lab task

The central frequency f_0 is chosen as 3 MHz. The bandwidth is $0.05f_0 = 150$ KHz. The input voltage is a sinusoidal wave with 2V amplitude.

Analysis

A second-order Butterworth filter is implemented as a band-pass filter. Second order is chosen since it will be easier to implement on hardware and will give more accurate results. The overall design is given in Figure.2. For this case, R_S and R_L are both 50Ω, the inductor and capacitor values will be found later. To design a band-pass filter, first a second-order Butterworth low-pass filter will be designed. This LPF's cut-off frequency will be equal to the BPF's bandwidth. Then, the inductor will be tuned with a series capacitor and the capacitor will be tuned with a parallel inductor. The resonance frequency is chosen as $f_0 = 3$ MHz.

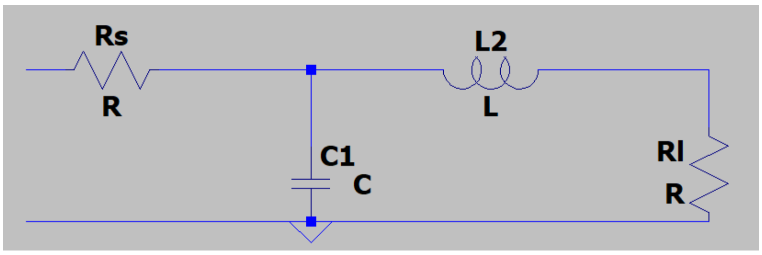

Figure.2 Generic Butterworth low-pass filter

To determine the values of C_1 and L_2, the Butterworth coefficients (N = 2) will be used from the table given in Figure.3.

N	g_1	g_2	g_3	g_4	g_5	g_6	g_7
1	2.0000	1.0000					
2	1.4142	1.4142	1.0000				
3	1.0000	2.0000	1.0000	1.0000			
4	0.7654	1.8478	1.8478	0.7654	1.0000		
5	0.6180	1.6180	2.0000	1.6180	0.6180	1.0000	
6	0.5176	1.4142	1.9318	1.9318	1.4142	0.5176	1

Figure.3 Butterworth filter coefficients table[1]

For the second order circuits, the values are:

$$C_1 = g_1 = 1.4142$$

$$L_2 = g_2 = 1.4142$$

Then, to have the cut-off frequency at $\Delta f = 150$ kHz, the values are divided by $\omega_1 = 2\pi\Delta f$;

$$C_1 = \frac{1.4142}{2\pi * 150 \text{ KHz}}, \; L_2 = \frac{1.4142}{2\pi * 150 \text{ KHz}}$$

Since the load resistance is $R_L = 50\ \Omega$, L_2 is multiplied by 50, and C_1 is divided by 50;

$$C_1 = \frac{1.4142}{2\pi * 150 \text{ KHz} * 50}, \; L_2 = \frac{1.4142 * 50}{2\pi * 150 \text{ KHz}}$$

$$C_1 = 30\ nF \ \&\ L_2 = 75.02\ \mu H$$

Then, the inductor and the capacitor are tuned to have resonance at the center frequency $f_0 = 3$ MHz ($\omega = 2\pi f_0$). This is done by connecting a capacitor C_2 in series with the inductor L_2 and connecting an inductor L_1 in parallel with the capacitor C_1. To calculate these values:

$$L_1 = \frac{1}{\omega^2 (C_1 = 30\ nF)}$$

$$C_2 = \frac{1}{\omega^2 (L_2 = 75.02\ \mu H)}$$

$$L_1 = 93.83\ nH \ \&\ C_2 = 37.53\ pF$$

[1] https://www.semanticscholar.org/paper/Design-and-development-of-band-pass-filter-for-Jijesh-Shivashankar/b75fe731917fb8d6beb62594781c4f41bf3d136f/figure/10

Using the found values above, the band-pass filter will be implemented both on LTSpice and hardware. In the hardware lab, the gain will be calculated with the formula;

$$A = 20\log\left(\frac{V_{out}}{V_{in}}\right) \tag{1}$$

Simulations

The circuit is implemented on LTSpice with the calculated values as shown in Figure.4.

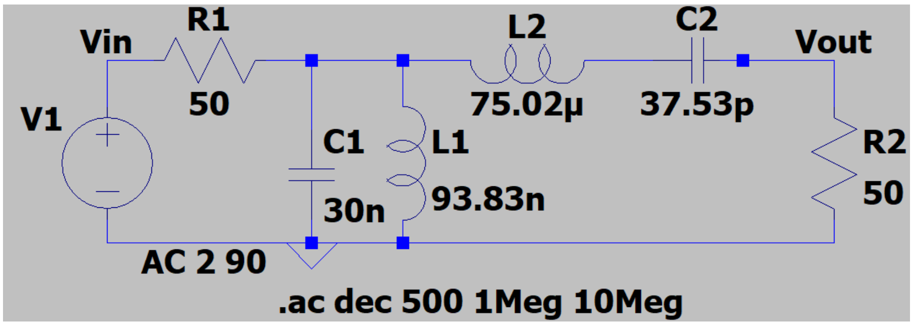

Figure.4 Band-pass filter circuit

The gain at the center frequency, the cut-off frequencies, $0.5f_0$ (1.5 MHz) and $2f_0$ (6 MHz) points are measured. The bandwidth is measured as the difference between the two cut-off frequencies. Figures.5-8 show the corresponding graphs, and the results are presented in Table.1.

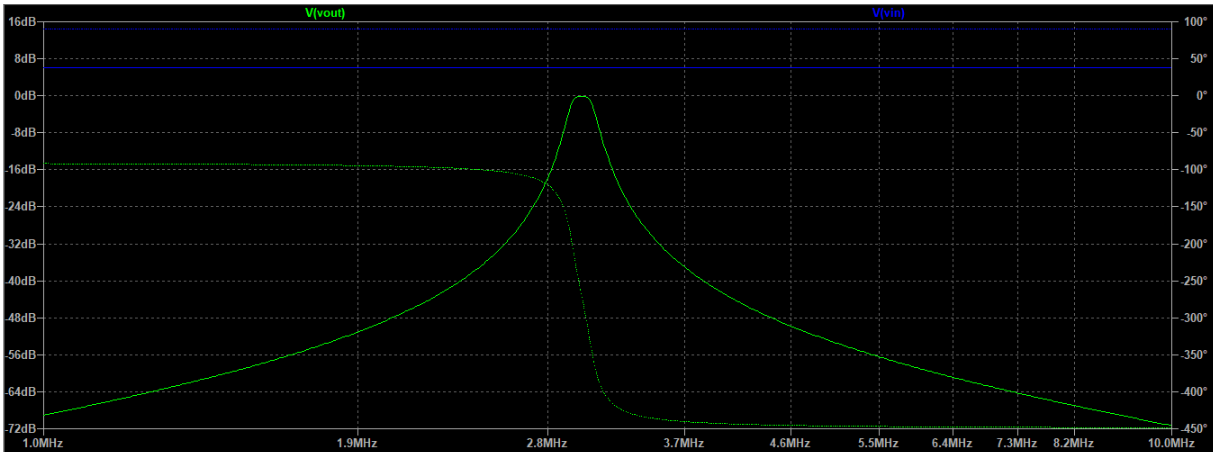

Figure.5 Output gain graph

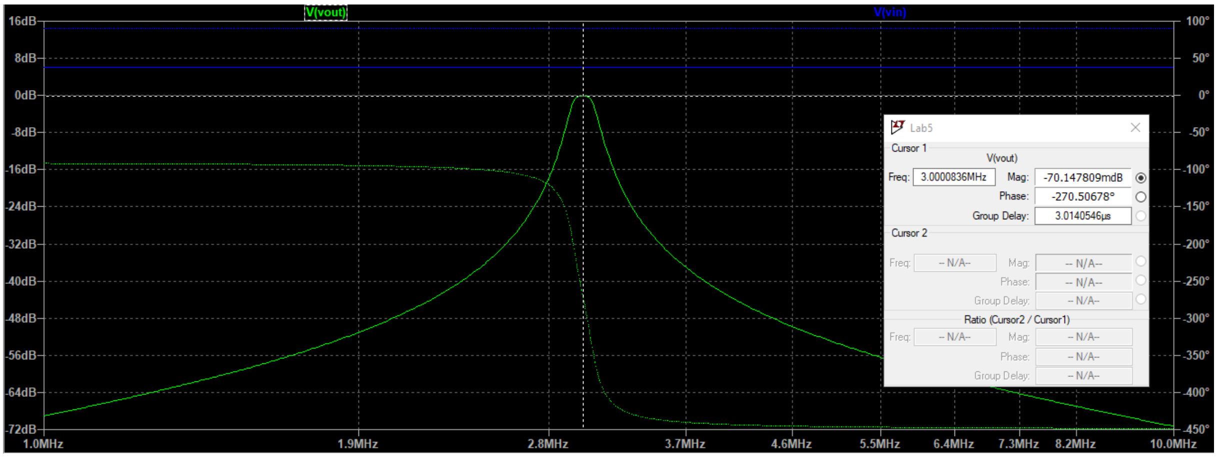

Figure.6 Gain is -70.15 mdB at the center frequency

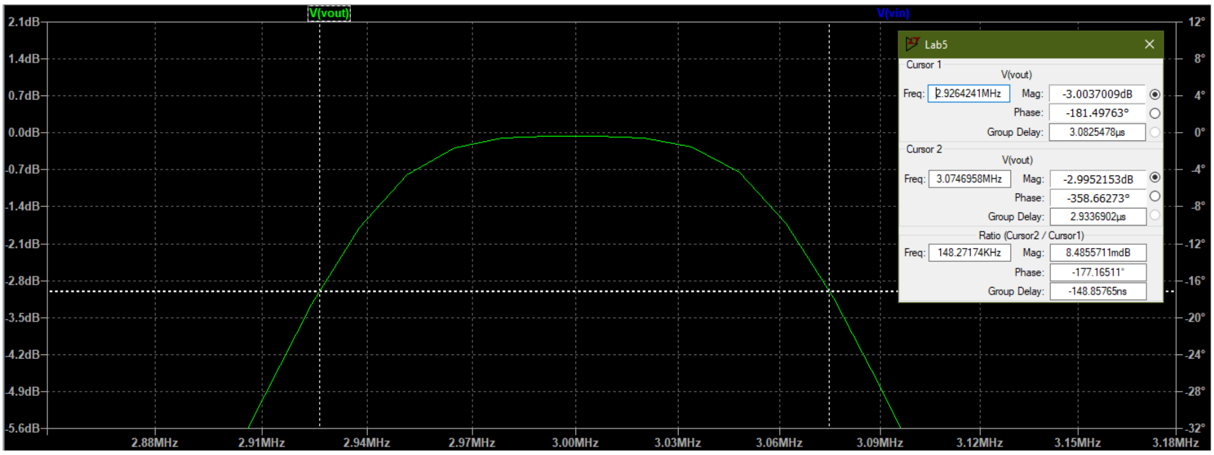

Figure.7 The cut-off frequencies f_{c1} and f_{c0} are 2.92 MHz and 3.07 MHz, bandwidth is 148.2 KHz

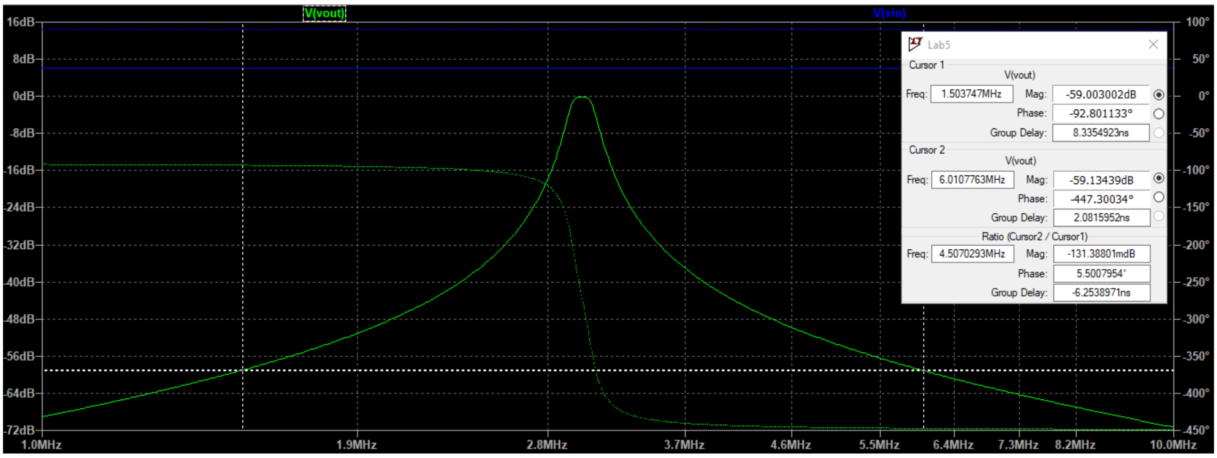

Figure.8 Gain is -59.00 dB at 1.5 MHz ($0.5f_0$) and -59.13 dB AT 6 MHz ($2f_0$)

	Theoretical value	**Measured value**	**Error**
Gain at f_0		-70.15 mdB	
Bandwidth (f_{c1} - f_{c0})	150 KHz	148.2 KHz	%1.2
Gain at $0.5f_0$	≤ -30 dB	-59.00 dB	Satisfied
Gain at $2f_0$	≤ -30 dB	-59.13 dB	Satisfied
Gain variation in the passband	≤ 3 dB	$\|-3.00 + 0.070\| = 2.93$ dB	Satisfied

Table.1 Software results

As one can see in Table.1, the errors are within the bounds, therefore all conditions for the software lab are satisfied.

Hardware Implementation

For the hardware implementation, the inductor and capacitor values were selected from the standard values. Since the source already has 50 Ω inner resistance, only the load resistor was used. The circuit is implemented on a breadboard for its ease of use. The hardware implementation circuit is shown in Figure.9.

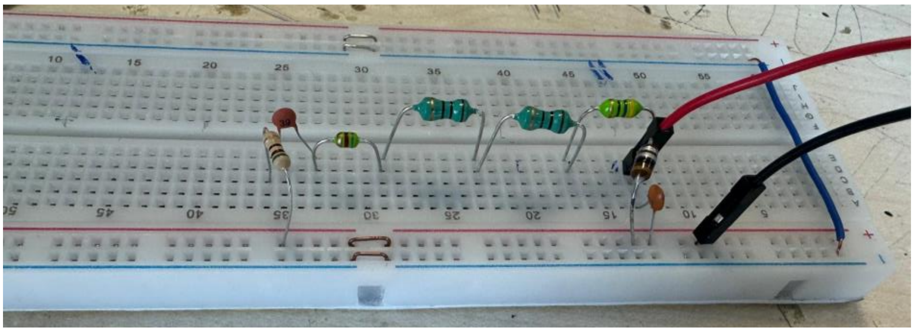

Figure.9 Hardware circuit

The input and output amplitudes are measured at various frequencies. Figures.10-14 show the measurements at the center frequency, at the cut-off frequencies, at $2f_0$ and at $0.5f_0$.

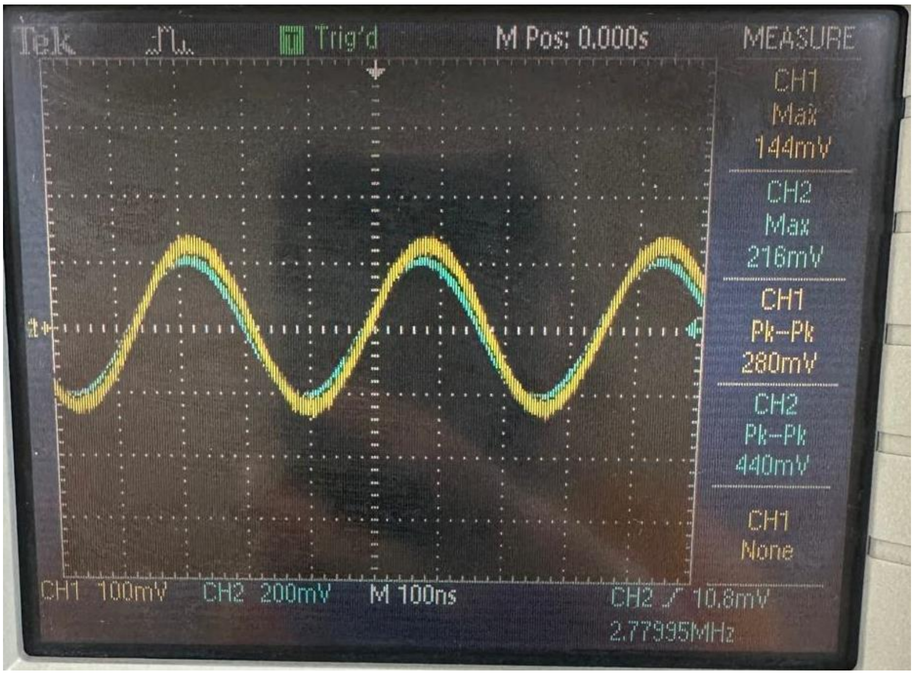

Figure.10 The center frequency is found as 2.78 MHz, Vin = 216 mV, Vout = 144 mV

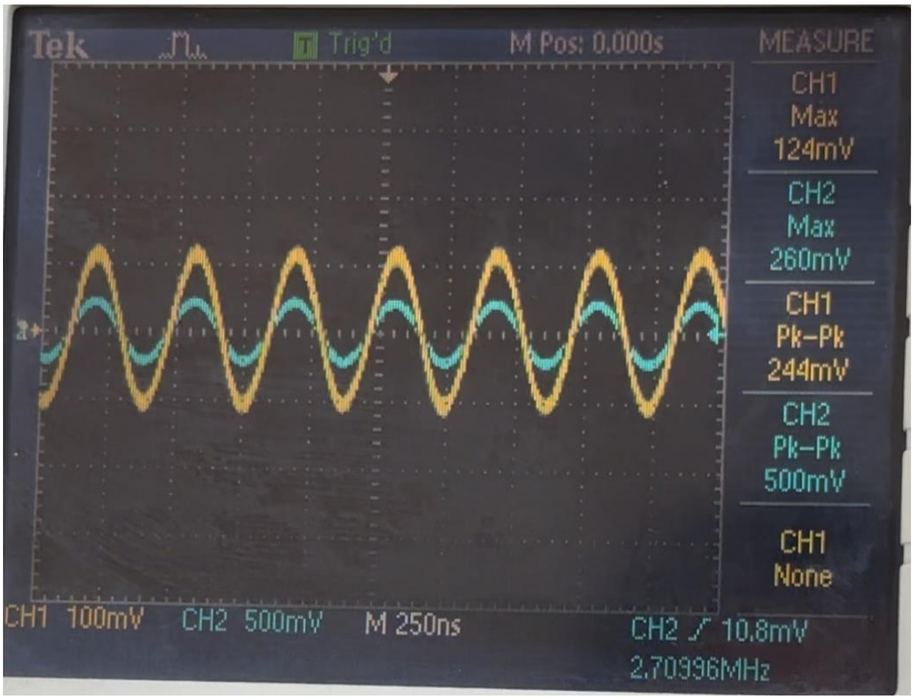

Figure.11 The first center frequency is found as 2.71 MHz, Vin = 260 mV, Vout = 124 mV

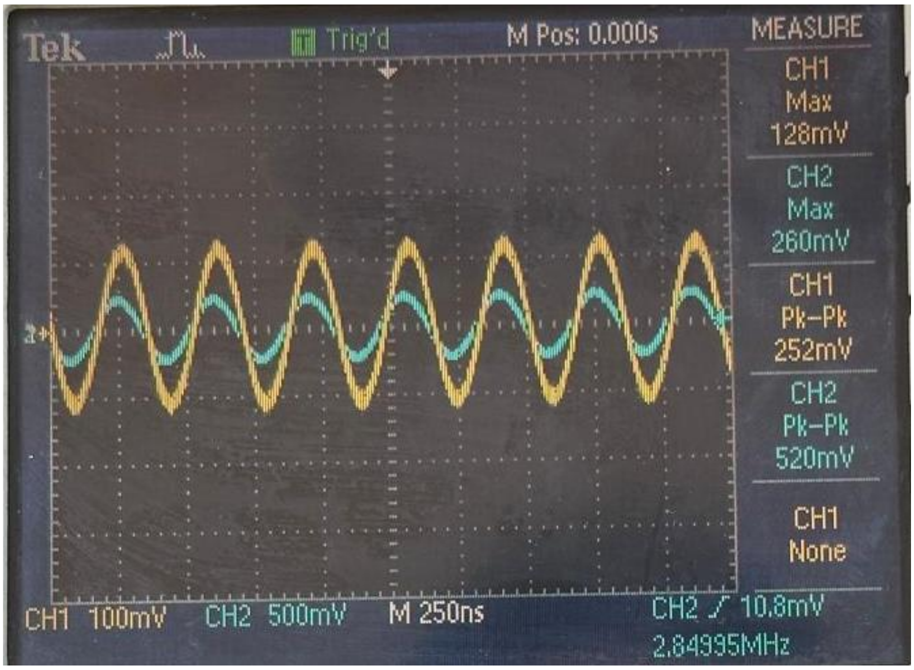

Figure.12 The second center frequency is found as 2.85 MHz, Vin = 260 mV, Vout = 128 mV

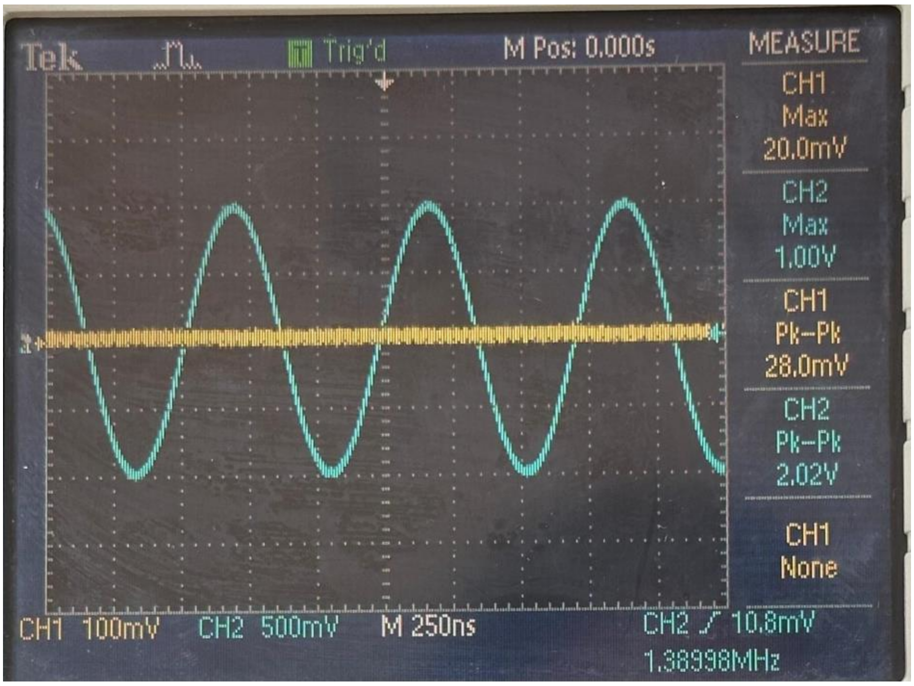

*Figure.13 At 0.5*f_0 *= 1.29 MHz, Vin = 1.00 V, Vout = 20 mV*

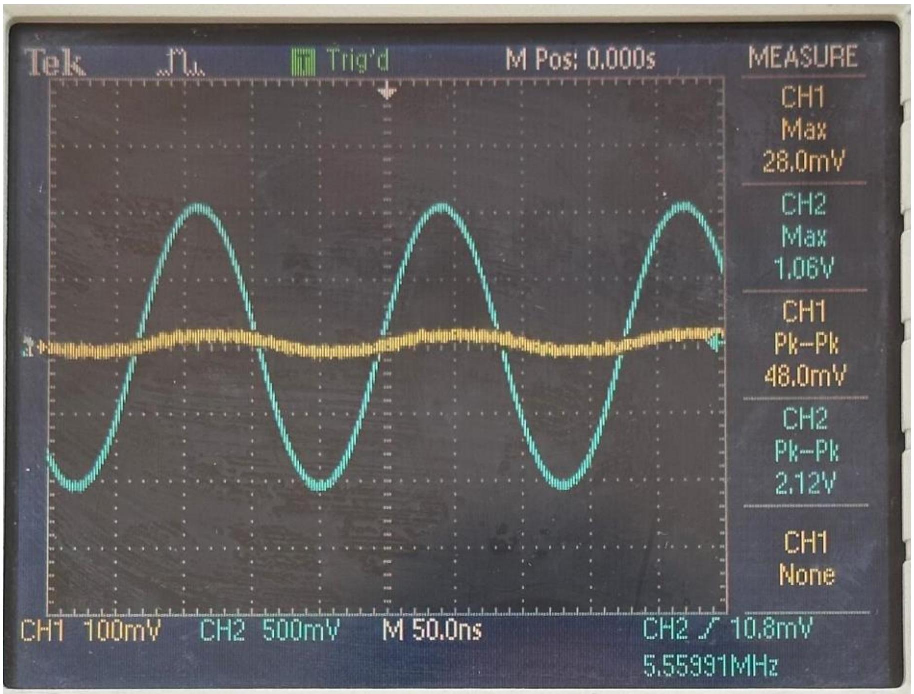

*Figure.14 At 2*f_0 *= 5.56 MHz, Vin = 1.06 V, Vout = 28 mV*

By using equation (1) from the analysis section, the dB gains are calculated for measured frequencies. The results of the hardware lab are presented in Tables.2-3.

	Frequency	V_{in}	V_{out}	Gain
Not Passband Region	**1 MHz**	1.02 V	24 mV	-32.57 dB
	1.29 MHz (0.5f_0)	1.00 V	20 mV	-33.98 dB
	2 MHz	1.02 V	20 mV	-34.15 dB
Passband Region	**2.71 MHz (f_{c0})**	260 mV	124 mV	-6.43 dB
	2.73 MHz	260 mV	140 mV	-5.38 dB
	2.78 MHz (f_0)	216 mV	144 mV	-3.52 dB
	2.82 MHz	260 mV	140 mV	-5.38 dB
	2.85 MHz (f_{c1})	260 mV	128 mV	-6.16 dB
Not Passband Region	**3 MHz**	980 mV	48 mV	-26.20 dB
	4 MHz	1.02 V	28 mV	-31.23 dB
	5 MHz	1.04 V	24 mV	-32.74 dB
	5.56 MHz (2f_0)	1.06 V	28 mV	-31.56 dB
	6 MHz	1.08 V	20 mV	-34.65 dB

Table.2 Gain table

	Theoretical value	Experimental value	Error
Center frequency (f_0)	3 MHz	2.78 MHz	%7.33
Gain at f_0		-3.52dB	
Bandwidth (f_{c1} - f_{c0})	150 KHz	140 KHz	%6.67
Gain at $0.5f_0$	$\leq$ -30 dB	-33.98 dB	Satisfied
Gain at $2f_0$	$\leq$ -30 dB	-31.56 dB	Satisfied
Gain variation in the passband	$\leq$ 3 dB	$\lvert -6.43 + 3.52 \rvert = 2.91$ dB	Satisfied

Table.3 Hardware results

As one can see from the results, all of the errors are within the bounds, therefore all conditions for the hardware lab are satisfied. By using the data in Table.2, the frequency response graph of the output gain is plotted in MATLAB. The graph is shown in Figure.15.

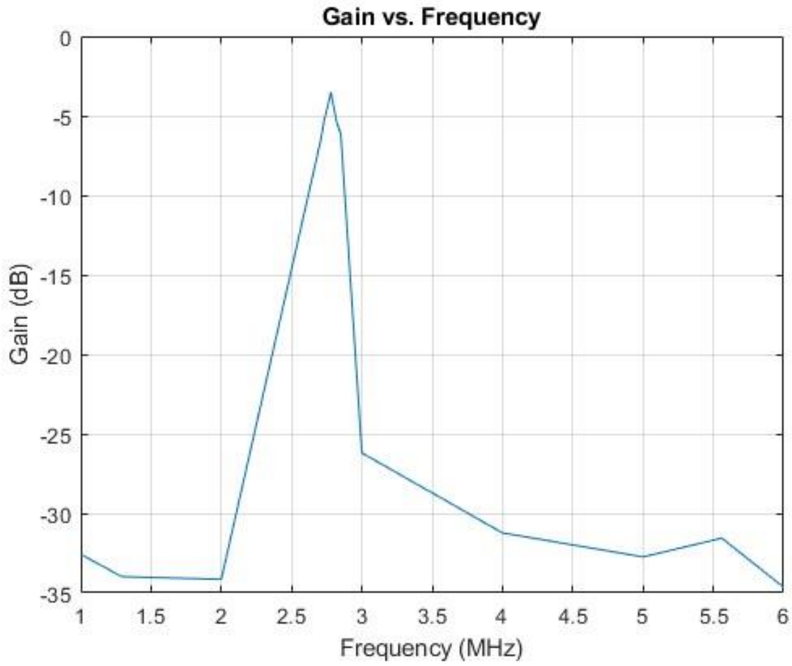

Figure.15 Frequency response graph

Conclusion

For the software implementation, the center frequency was 3 MHz and the bandwidth was obtained with an error of %1.2. In the hardware implementation, the center frequency was found as 2.78 MHz. The %7.33 error in the center frequency might be due to the usage of the standard valued components. Also, we need to consider the variances in the standard values because of their inner resistances and tolerances.

In the hardware implementation, the gain at center frequency was calculated as -3.52 dB, whereas in the software implementation it was -70.15 mdB. To find the 3-dB cut-off frequencies in the hardware implementation, instead of looking for -3 dB, I looked for -6.52 dB. The new 3-dB cut-off frequencies were found as 2.71 MHz and 2.85 MHz. The bandwidth was obtained with an error of %6.67. The other conditions were satisfied in both the software implementation and the hardware implementation.

Overall, we can conclude by the output gain graph obtained by MATLAB that a second order Butterworth filter results in some distortions in the results and to minimize the distortions and the errors, higher order Butterworth filters can be implemented. As the order of the filter increases, the accuracy also increases. But since increasing the order also results in the need of using more components and to tune more components, it would be harder to implement on hardware. All in all, the lab aimed to teach us how to design a Butterworth band-pass filter in both software and hardware and it was successful.