EEE 202 CIRCUIT THEORY
LAB 1

Time-Domain and Frequency-Domain Analyses in LTSpice

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Section 3

SW Implementation

Introduction:

In this lab, the objective is to analyze different circuits on their time-domains and frequency-domains in LTSpice and then implementing them onto hardware and observing their behavior in real life.

Analysis:

The formula for a voltage divider circuit is as follows:

$$v_{input} \cdot \frac{R_2}{R_1 + R_2} = v_{output}$$

$$10 \frac{15}{6.8 + 15} = 6.88\, V$$

In order to find the 3 dB cut-off frequency of the RL circuit the following formula is utilized:

$$f_c = \frac{R}{2\pi L}$$

where f_c is the cut-off frequency in Hz, R is the resistance in Ω and L is the inductance in H. In Part 1, for the voltage source with the internal resistance 50 Ω, f_c is calculated as:

$$\mathrm{f_c} = \frac{83}{2\pi * 47 * 10^{-6}} = 281.06\, KHz$$

In Part 2, f_c is calculated as:

$$\mathrm{f_c} = \frac{33}{2\pi * 47 * 10^{-6}} = 111.75\, KHz$$

For OPAMP circuit #1 (inverting amplifier), the equation obtained by the circuit is as follows:

$$\mathrm{V_{output}} = -\frac{\mathrm{R_2}}{\mathrm{R_1}} \mathrm{v}_{input}$$

For our case, $\frac{\mathrm{R_2}}{\mathrm{R_1}} = 3$, so the output was 3 times the magnitude of the input. Also, because of the – sign in front of the $\frac{\mathrm{R_2}}{\mathrm{R_1}}$ ratio, the output was inverted.

For OPAMP circuit #3 (integrator), the equation obtained by the circuit is as follows:

$$\mathrm{V}_{output} = -\frac{1}{\mathrm{R_1 C_1}} \int_0^{\mathrm{t}} \mathrm{V_{input}}\, \mathrm{dt}$$

Since the OPAMP becomes saturated at the peak points, we will observe trapezoid waveforms instead of regular triangular waves. This shape is due to the integrating property of the

OPAMP circuit. If we plug in our chosen values to this equation, we obtain $V_{output} = 8.50\ V$ in highs and $V_{output} = -10\ V$ in lows.

In hardware implementation for the RL circuit, the dB magnitudes are calculated by using the following formula:

$$A = 20 * \log_{10} \frac{V_{output}}{V_{input}} \qquad (*)$$

For percentile error calculations in the hardware implementation part, the following formula is used:

$$\%\ Error = \left| \frac{Experimental\ Value - Theoritical\ Value}{Theoritical\ Value} \right| * 100$$

Simulations:

Part 1: Transient Analysis

In this part, a simple voltage divider circuit is implemented. The values are selected as: R1 = 6.8 Ω and R2 = 15 Ω. Amplitude of the voltage source is 10 V (sinusoidal wave) and the frequency of the voltage source is 10 KHz.

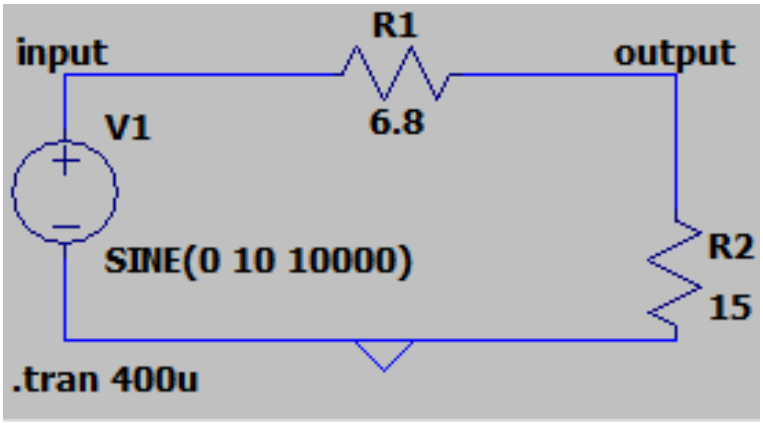

Figure 1. The voltage divider circuit

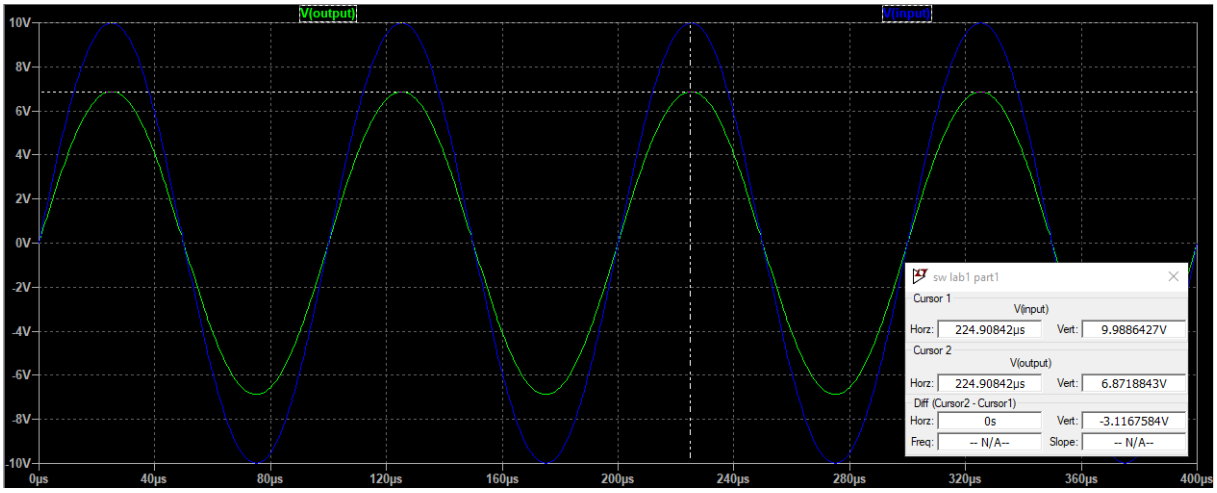

Figure 2. The graph of the input and output voltages of the voltage divider circuit

Then, R2 from the previous part is changed to an inductor to make a first order RL circuit. The values are selected as: R1 = 33 Ω and L1 = 47 uH. The amplitude of the voltage source is 8 V (sinusoidal wave) and the frequency of the voltage source is 100 KHz. The internal resistance of the signal generator is added as a parasitic property as shown in Figure 3. As we increase the frequency of the sinusoidal wave, the amplitude of the output is getting larger and larger. This shows that this circuit is essentially a high-pass filter.

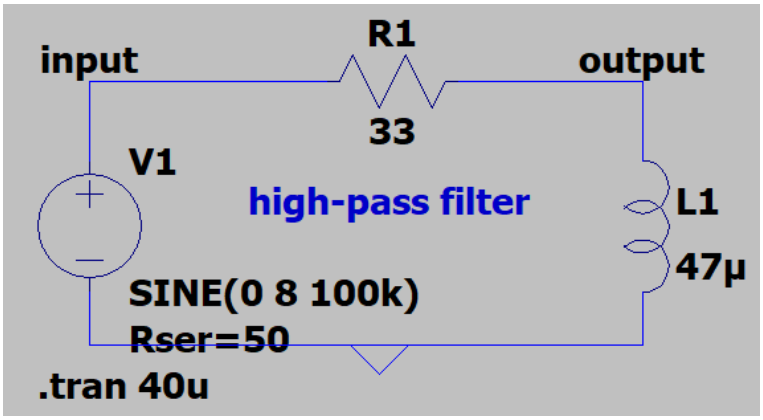

Figure 3. First order RL circuit at frequency 100 KHz

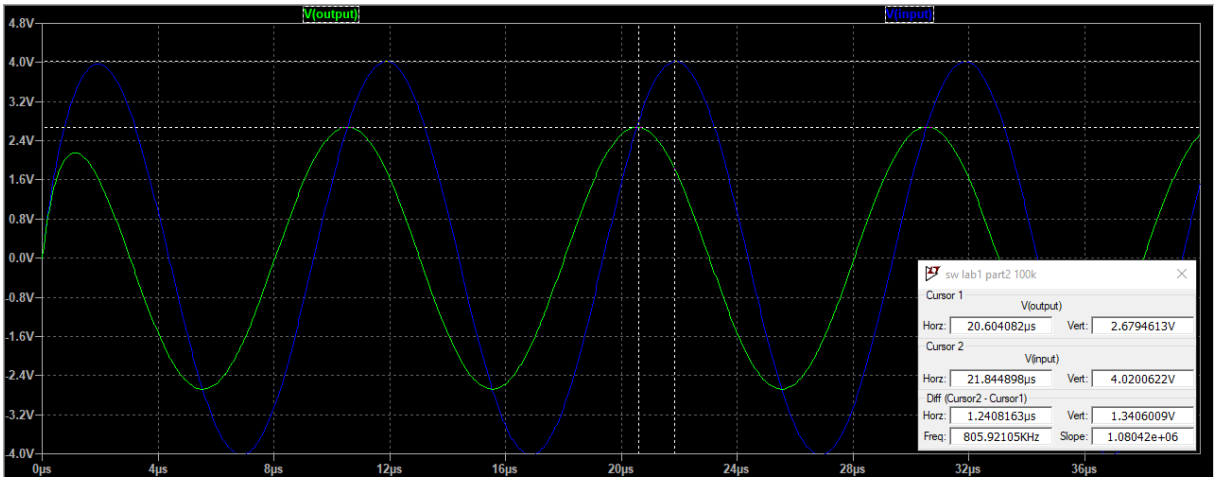

Figure 4. The graph of the input and output voltages of the simple RL circuit at 100 KHz

Then, the same circuit is implemented for both at 10 KHz and at 500 KHz.

At 10 KHz:

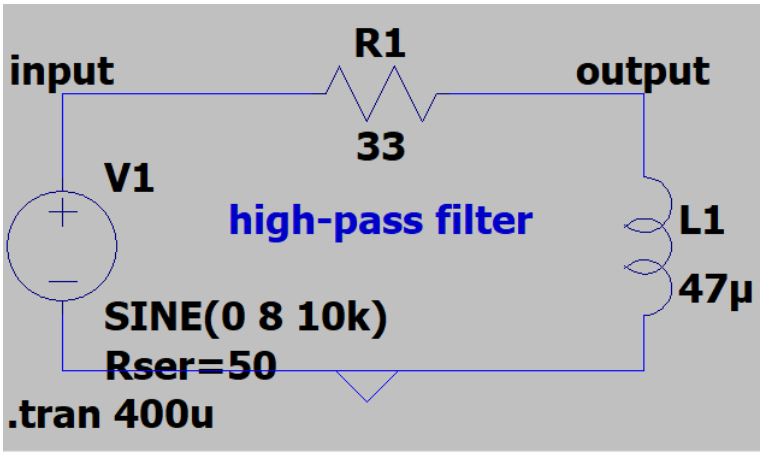

Figure 5. First order RL circuit at frequency 10 KHz

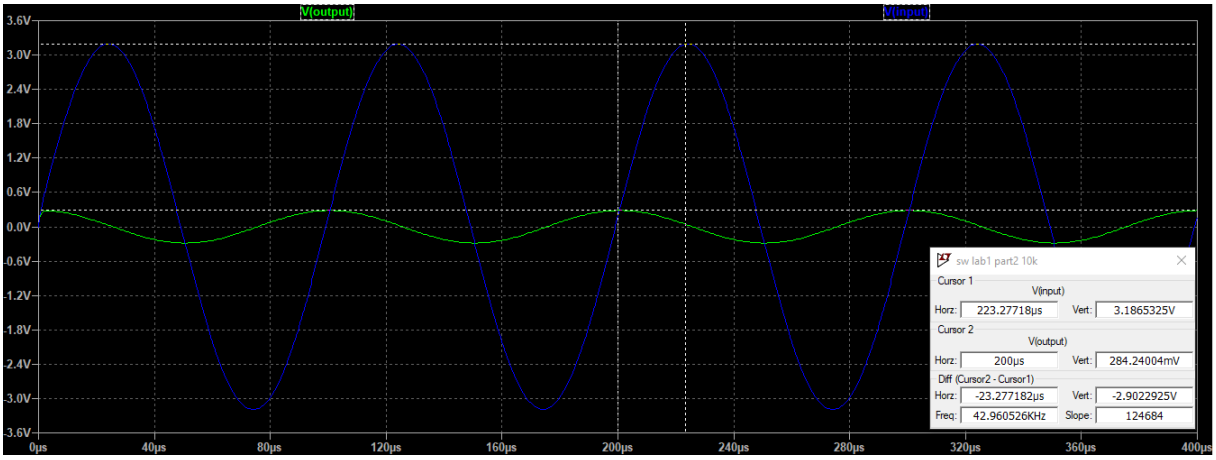

Figure 6. The graph of the input and output voltages of the simple RL circuit at 10 KHz

At 500 KHz:

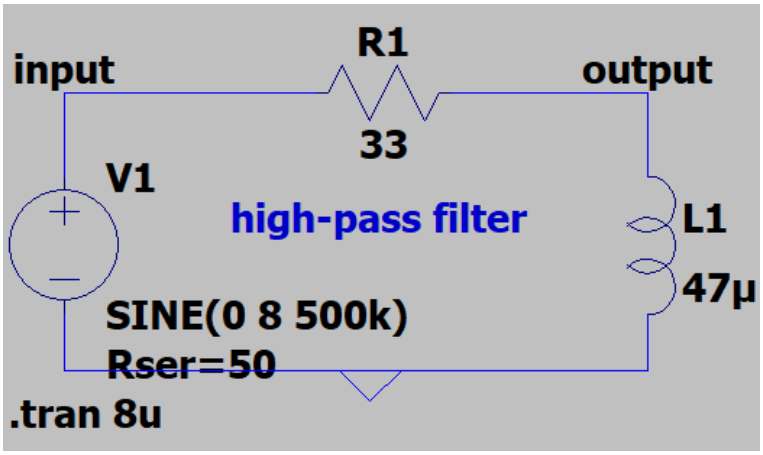

Figure 7. First order RL circuit at frequency 500 KHz

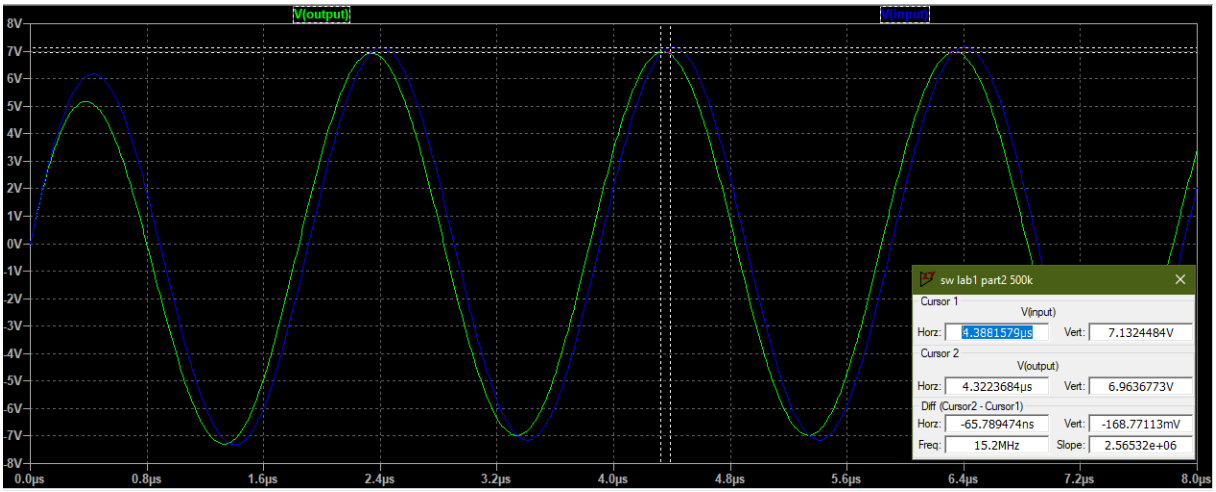

Figure 8. The graph of the input and output voltages of the simple RL circuit at 500 KHz

At 281.06 KHz, which is the cut-off frequency of the RL circuit:

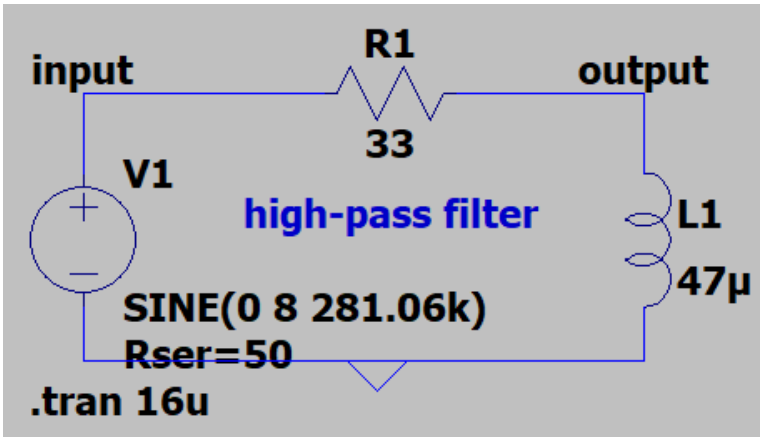

Figure 9. First order RL circuit at frequency 281.06 KHz

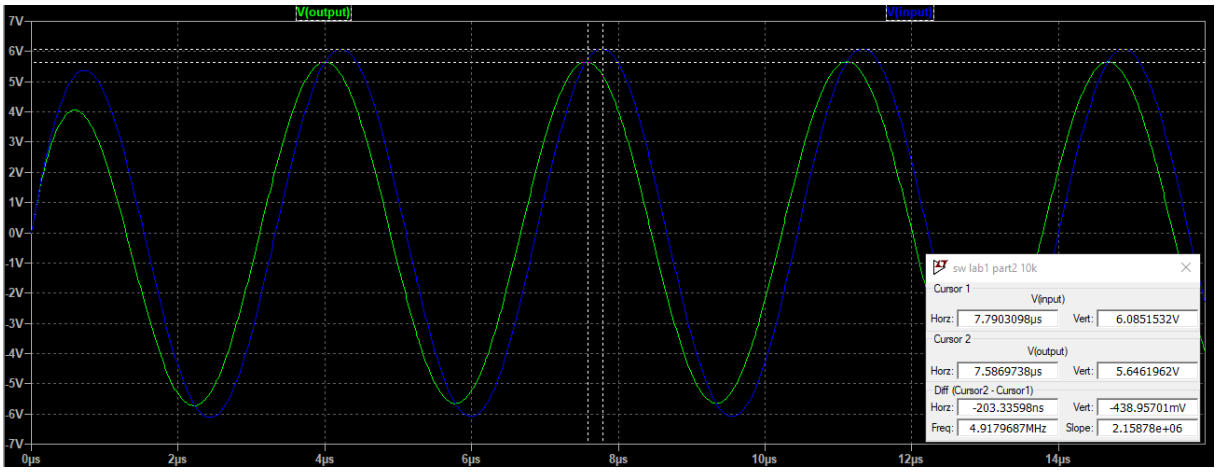

Figure 10. The graph of the input and output voltages of the simple RL circuit at the cut-off frequency (281.06 KHz)

Frequency (KHz)	Output Voltage (V)
10	0.284
100	2.68
281.06	5.65
500	6.96

Table 1. Output voltage values

Part 2: AC Analysis

In this part, the circuit from the figure 2 is implemented but this time, the voltage source is an AC source instead of a DC source. Also, the parasitic 50 Ω is removed from the circuit (will be added later on). The circuit is shown in Figure 11. The AC voltage source has an amplitude of 1. The output voltage graph is a logarithmic plot that goes from 100 Hz to 10 MHz. For this circuit, the 3 dB cut-off frequency is at 111.75 KHz.

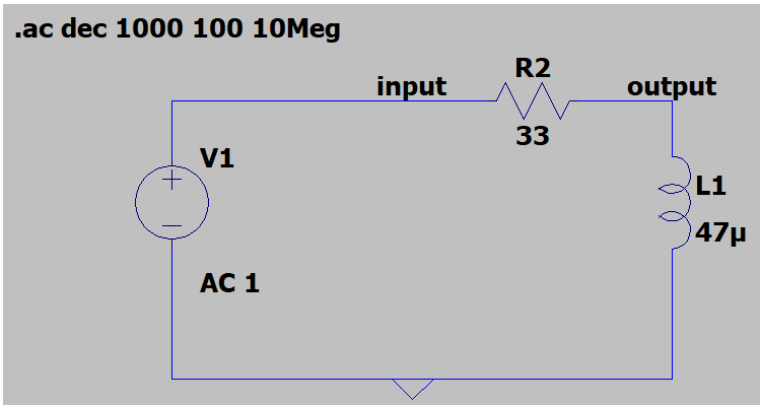

Figure 11. First order RL circuit for AC small signal analysis

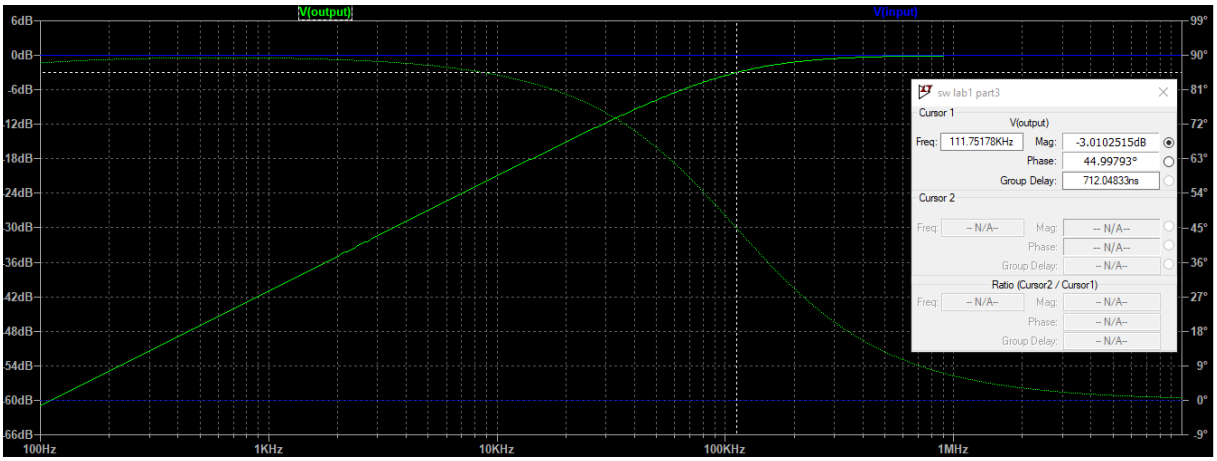

Figure 12. The graph of the input and output voltages on logarithmic axis, cursor is at the 3 dB cut-off frequency

Then the parasitic property 50 Ω is added back to the circuit to mimic the real life voltage sources. The new circuit is shown in Figure 13. The logarithmic graph is shown in Figure 14. For this circuit, the 3 dB cut-off frequency is at 281.06 KHz.

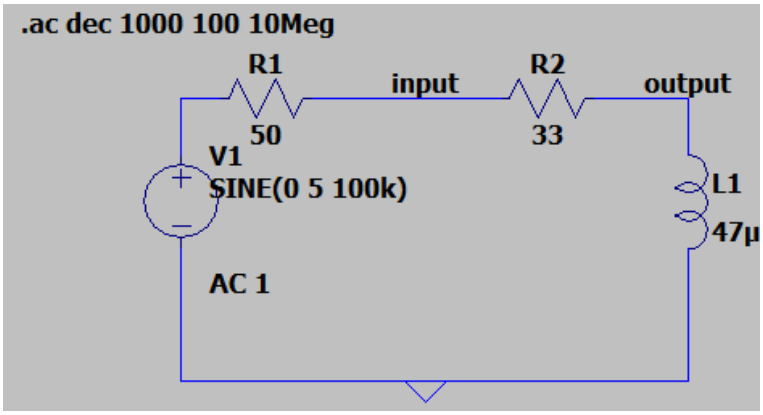

Figure 13. First order RL circuit at frequency 100 KHz for AC small signal analysis

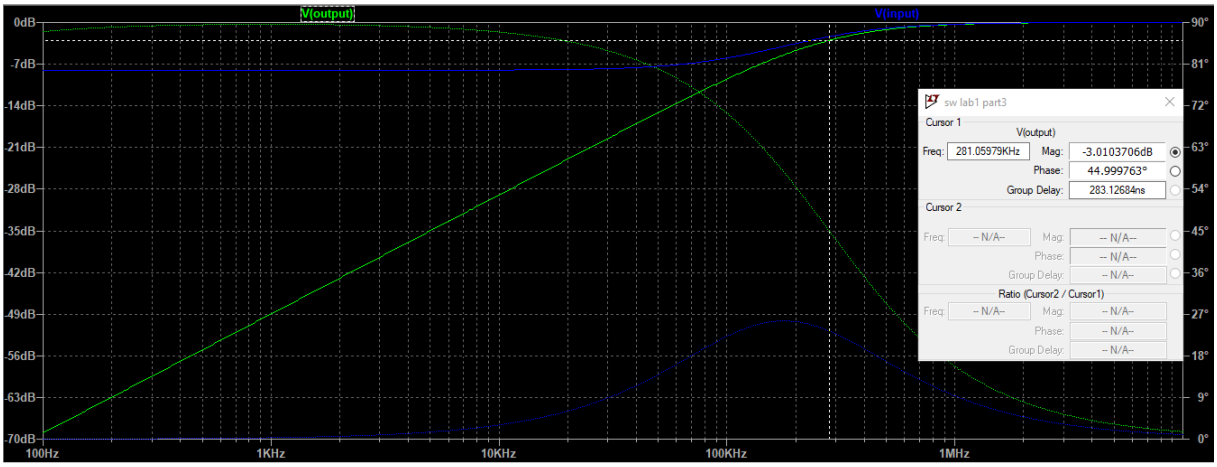

Figure 14. The graph of the input and output voltages on logarithmic axis, cursor is at the 3 dB cut-off frequency

Part 3: OPAMP Circuits

In this part, LM324 OPAMP model provided in the lab assignment is uploaded to the LTSpice and used for each OPAMP circuit. 10 V DC voltage is provided to the OPAMP. The input voltage of the circuit has an amplitude of 2 V (sinusoidal wave) and frequency 1 KHz. R3 = 2000 Ω as it said on the lab assignment and R1 and R2 as chosen so that R2/R1 ratio would be equal to 3. For this, I chose R1 = 330 Ω since it is a standard value that we have at the lab, thus making R2 = 990 Ω. The mentioned circuit is shown in Figure 15.

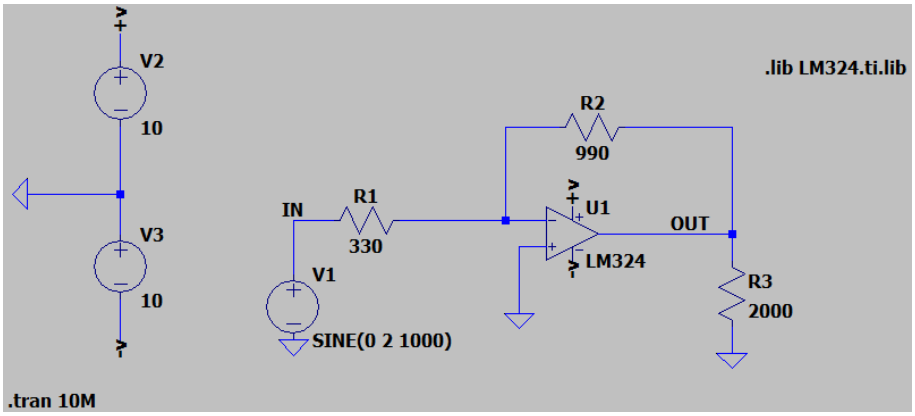

Figure 15. OPAMP circuit #1

This circuit is an inverting amplifier and its graph shows that the output voltage is 3 times the input voltage and inverted with respect to it. The graph can be seen in Figure 16.

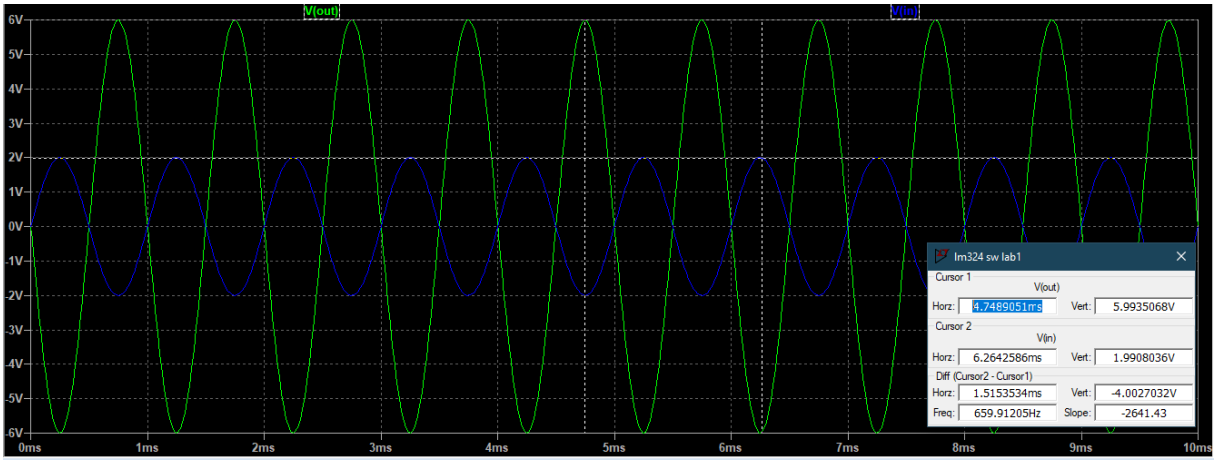

Figure 16. The graph of the input and output voltages of the OPAMP circuit #1

Then, the input voltage is changed to a square wave with 1 V amplitude, 2 ms period and %50 duty cycle as provided in the lab assignment. The rise and fall times are equal and 10 ns. The new circuit is shown in Figure 17 and its corresponding input-output voltage plot is shown in Figure 18.

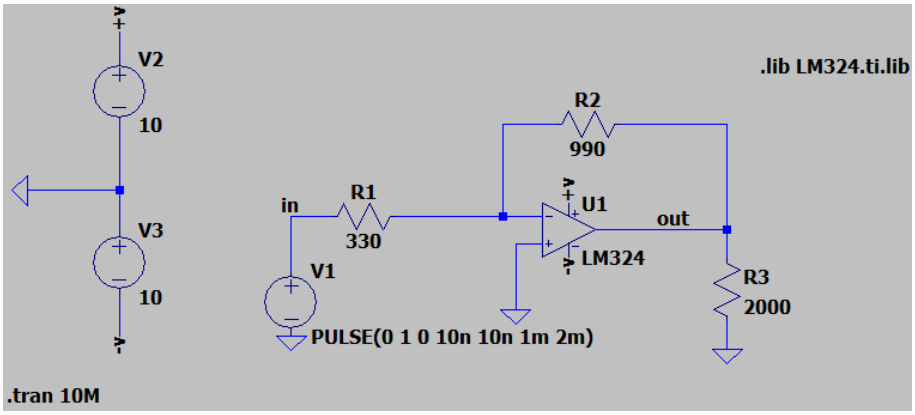

Figure 17. OPAMP circuit #2 (square wave input)

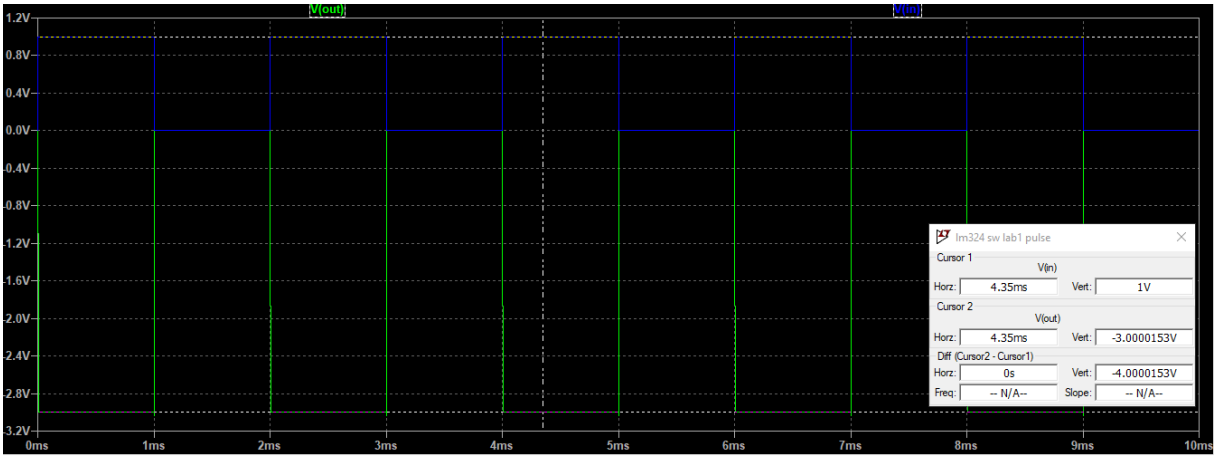

Figure 18. The graph of the input and output voltages of the OPAMP circuit #2

To saturate the OPAMP, R2 is changed to 5.6 KΩ. The saturation is observed in Figure 19. In this graph, we can see a typical saturated OPAMP behavior.

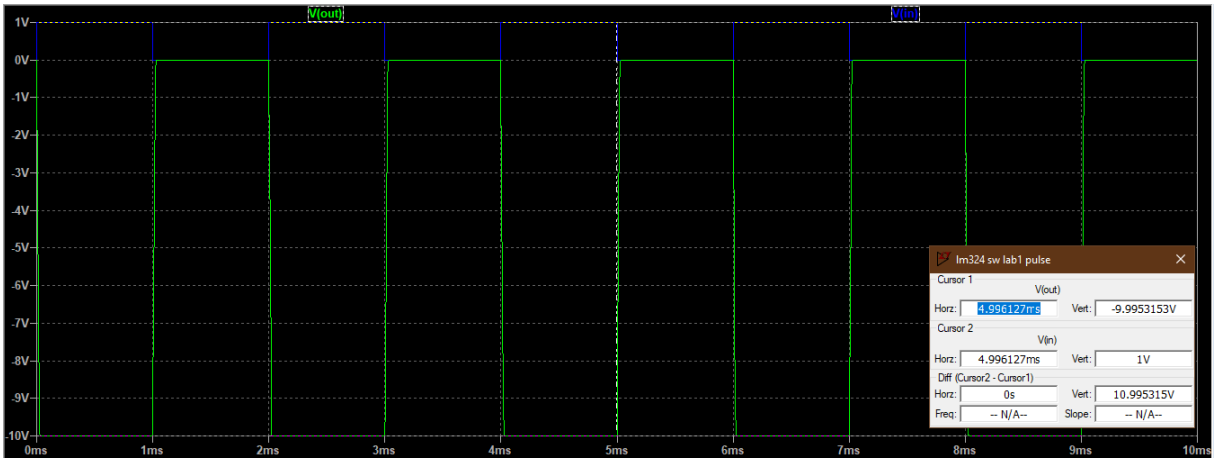

Figure 19. The graph of the input and output voltages of the new OPAMP circuit #2, OPAMP is now in SAT mode

For the last OPAMP circuit, R1 is changed to 8 KΩ and R2 is replaced with a capacitor of value 3 nF. The new circuit is shown in Figure 20 and its corresponding input-output voltage graph is shown in Figure 21. The output voltage is a saturated triangular wave and shows that this OPAMP circuit is an integrator.

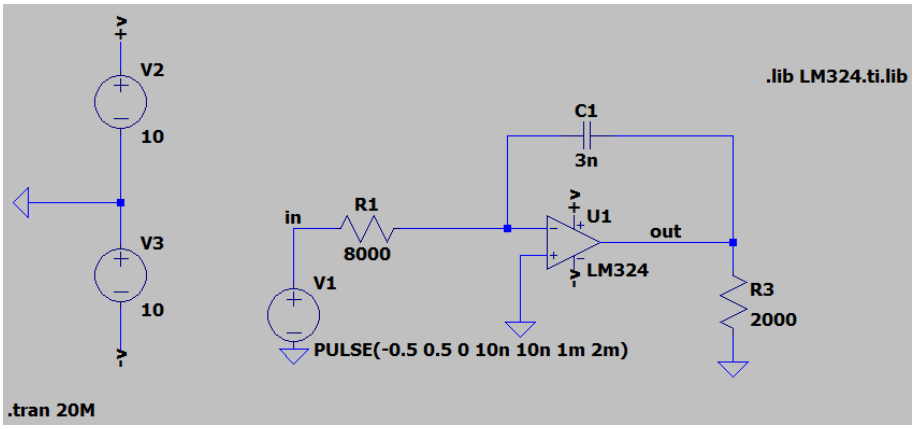

Figure 20. OPAMP circuit #3 (with capacitor)

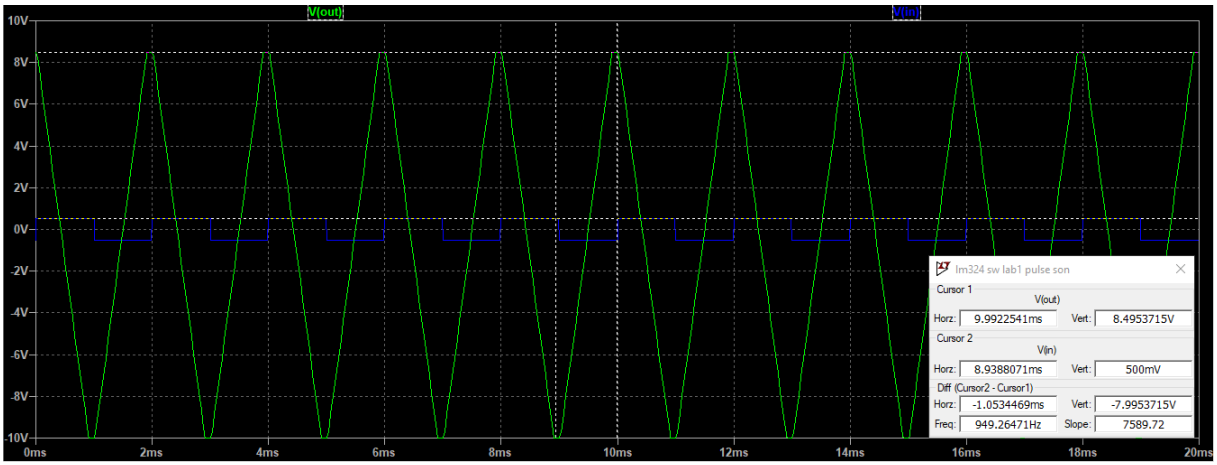

Figure 21. The graph of the input and output voltages of the OPAMP circuit #3

HW Implementation:

Part 1: RL Circuit

To implement the simulated RL circuit (Figure 3), a 33 Ω resistance and a 47 uH axial inductor are connected accordingly on a breadboard. The circuit is shown in Figure 22. The output voltage is measured by using an oscilloscope probe and shown on the oscilloscope. The frequency of the signal generator was at 10 KHz, 100 KHz, 500 KHz for three different measurements. By trial-and-error, the 3 dB cut-off frequency is measured as 323 KHz. The oscilloscope screens can be seen in Figures 23-26. Also for all frequencies, the error percentages are calculated by using the formula mentioned in the “Analysis” section with respect to Table 1.

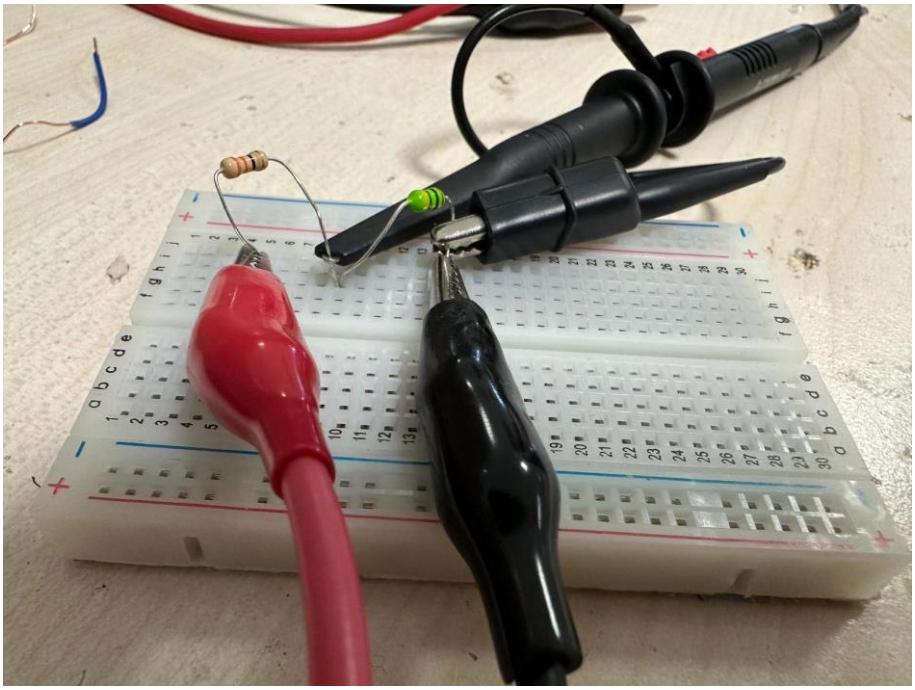

Figure 22. RL circuit in real life

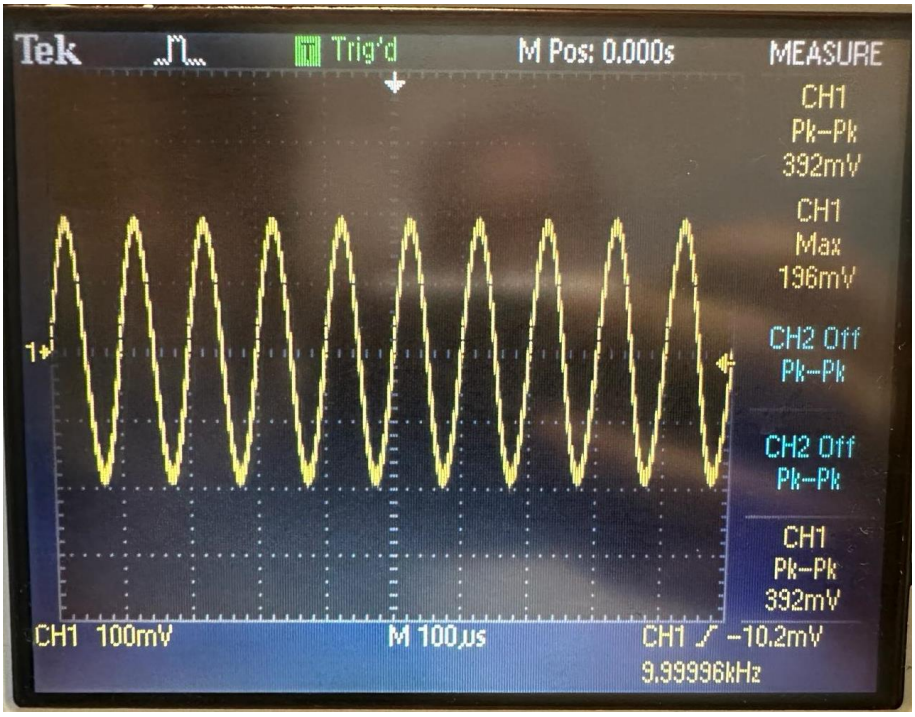

Figure 23. Oscilloscope screen when the signal generator is at 10 KHz

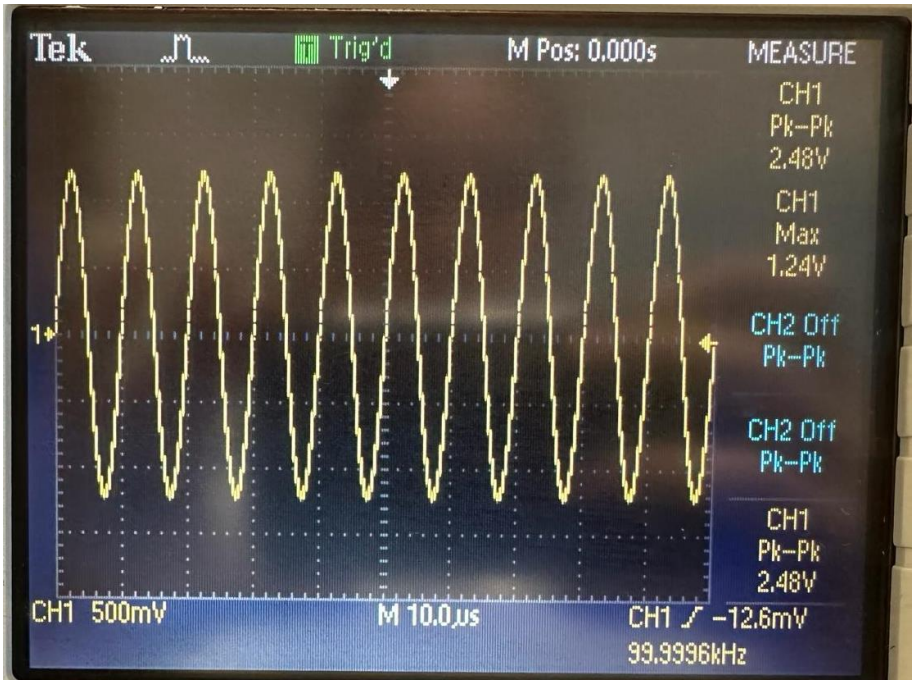

Figure 24. Oscilloscope screen when the signal generator is at 100 KHz

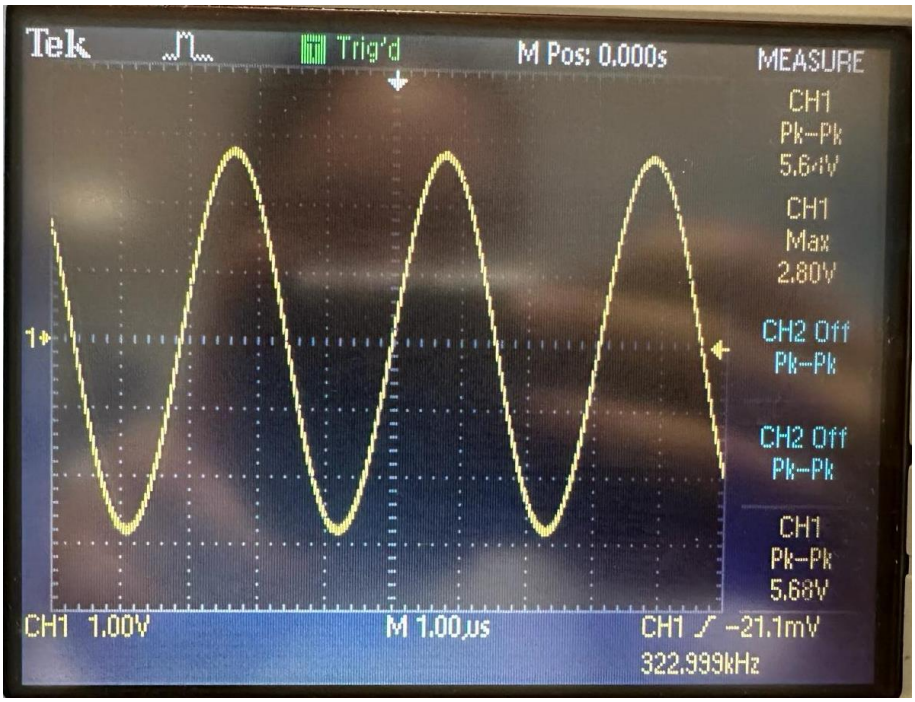

Figure 25. Oscilloscope screen when the signal generator is at 323 KHz

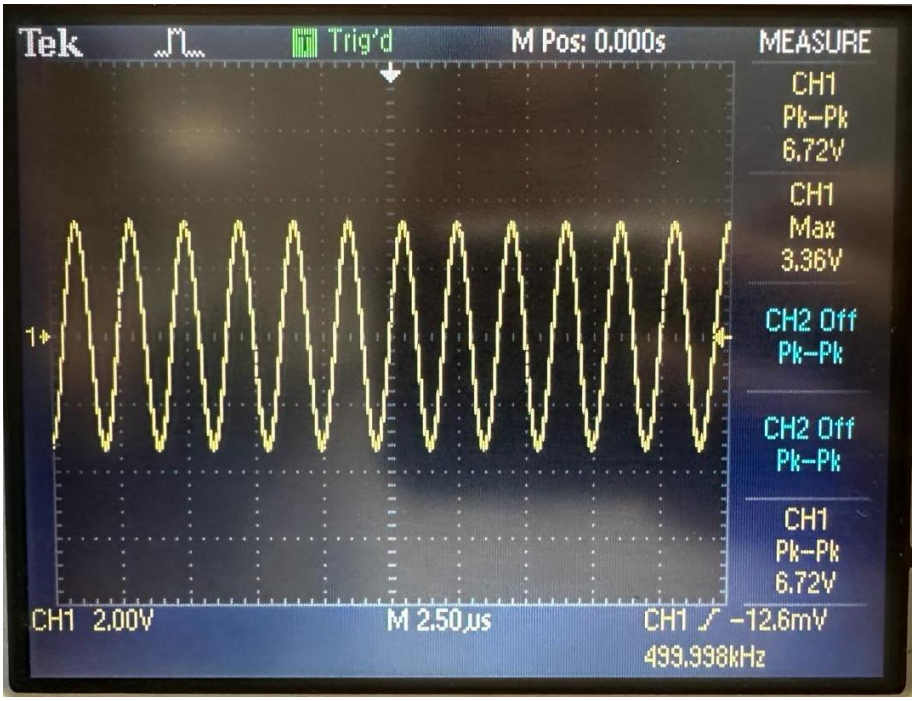

Figure 26. Oscilloscope screen when the signal generator is at 500 KHz

Frequency (KHz)	Output Voltage (V)	Error (%)
10	0.392	27.55
100	2.48	7.46
323	5.68	0.53
500	6.72	3.45

Table 2. Real-life implementation results & comparison

Then, to make our logarithmic dB magnitude plot more accurate, I also took measurements at different frequencies and calculated their corresponding dB magnitudes according to the formula (*) provided in the "Analysis" section of this document (for this case $V_{input} = 8\,V$). The values and their calculated magnitudes are provided in Table 3. The logarithmic plot is then drawn by using MATLAB (Figure 27).

Frequency (KHz)	Output Voltage (V)	A (dB)
5	0.330	-27.69
10	0.392	-26.20
15	0.488	-24.29
50	1.28	-15.92
75	1.86	-12.67
100	2.48	-10.17
125	2.96	-8.64
150	3.38	-7.48
200	4.24	-5.51
250	4.88	-4.29
300	5.44	-3.35
323	5.68	-2.97
350	5.84	-2.73
400	6.32	-2.05
450	6.56	-1.72
500	6.72	-1.51
550	7.04	-1.11

Table 3. Output voltages and at different frequencies

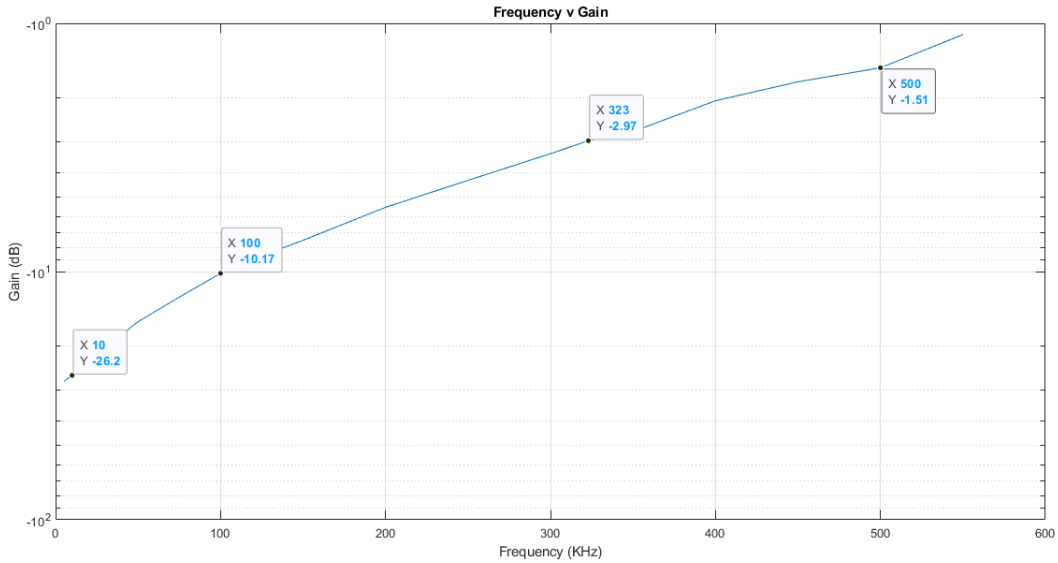

Figure 27. Logarithmic dB magnitude graph by using MATLAB

Part 2: OPAMP Circuits

The OPAMP circuit on Figure 15 is implemented on the hardware lab by using a 330 Ω resistor, a 1 K Ω resistor, a 2.2 K Ω resistor and LM324 OPAMP. Then the circuit is made on a breadboard, as shown in Figure 28. The oscilloscope screen is shown in Figure 29. Input-output voltages are noted on Table 4.

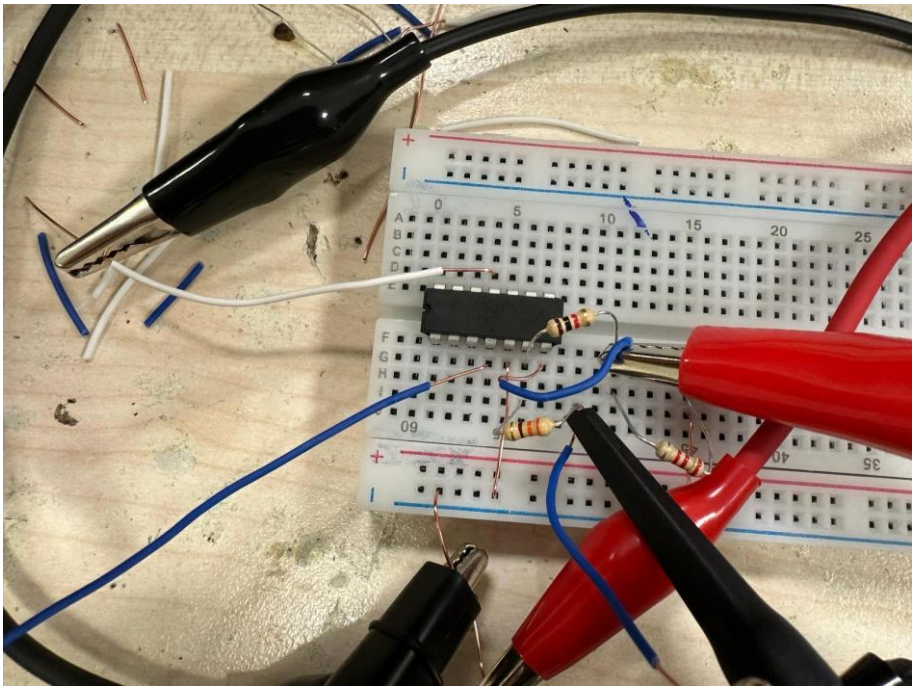

Figure 28. OPAMP circuit #1 on a breadboard

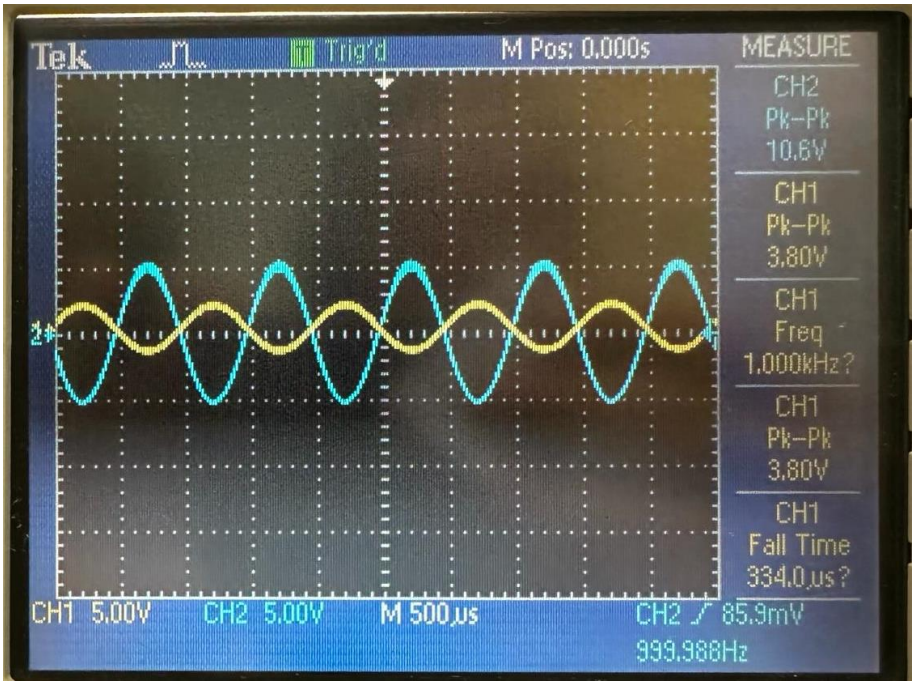

Figure 29. Oscilloscope screen (yellow == input , blue == output)

Input Voltage (V)	Output Voltage (V)
1	2.54
2	5.22
5	8.54
10	8.54

Table 4. Output voltages at different input voltages

OPAMP circuit #3 in Figure 20 is implemented by using 8.2 K Ω for R1 and 3.3 nF capacitor for C1. Input voltage configurations are changed to a square wave with 1 V amplitude. The real life circuit is shown in Figure 30 and the oscilloscope screen is shown in Figure 31.

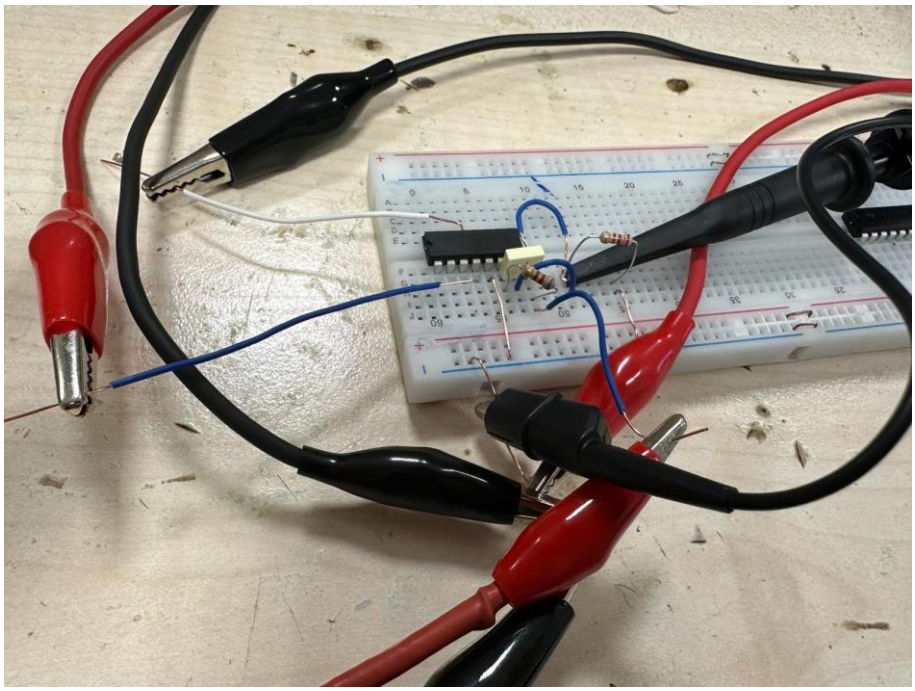

Figure 30. OPAMP circuit #3 on a breadboard

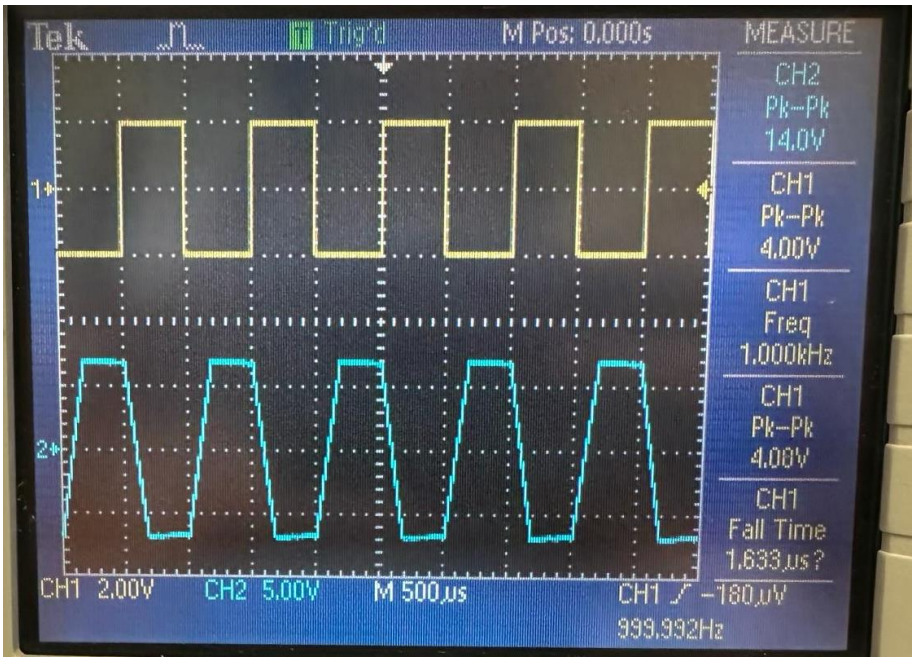

Figure 31. Oscilloscope screen (yellow == input , blue == output)

Conclusion:

For the RL circuit implementation, the error percentages varied vastly from frequency to frequency. It is observed that in lower frequencies the error percentage was higher compared to those in higher frequencies. Since we considered the series resistance of the signal generator in both LTSpice simulations and real life, the errors are most probably due to human error.

The 3 dB cut-off frequency was found as 323 KHz and it was calculated as 281.06 KHz. The error percentage of the cut-off frequency is %14.92. For the RL circuit with the ideal signal generator (no series resistance) the 3 dB cut-off frequency was calculated as 111.75 KHz. Since the magnitude of the output voltage approached to 0 as we increased the frequency, this circuit is a high-pass filter.

For OPAMP circuit #1, we observed that the circuit was an inverting amplifier and it amplified the input voltage 3 times, then inverted it with respect to the time axis. We observed that the real life measurements and the LTSpice simulations did not match due to the lack of considering the series resistance of the signal generator. This can be solved by subtracting 50 from 330 and reconnecting the circuit. When we changed the magnitude of input voltage, we observed that the OPAMP was saturated at (and after) 5 V and the magnitude of the output voltage was 8.54 V. Theoretically, the output should be 10 V in magnitude but since we did not consider the series resistance, the real life result varied.

For OPAMP circuit #2, we changed the input voltage from a sine wave to a square wave and simulated the results on LTSpice. This circuit was not implemented on the hardware lab.

The OPAMP circuit #3 is an integrator.

The aim of this lab was to learn how to make time and frequency analyses by using LTSpice. Overall, the lab was successful.