EEE 202 CIRCUIT THEORY

LAB 3

Waveform Generator

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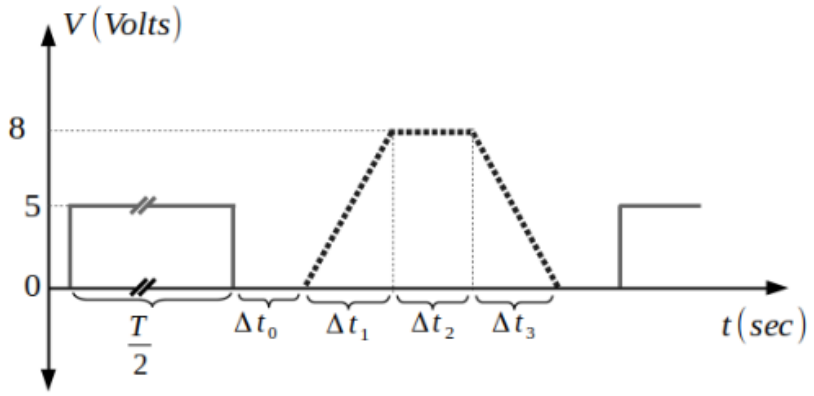
Section 3

SW Implementation

Introduction:

This labs aim is to design a circuit that generates the voltage waveform shown in Figure.1. The design should be based on OPAMPs and RC circuits. The specifications are given in Figure.2.



Input (solid gray line) is a square pulse. One period of the **output** is shown by dashed lines.

Figure.1 Waveform given in the lab prompt

$\Delta t_0 = 2ms, \quad \Delta t_1 = 2ms, \quad \Delta t_2 = 3ms, \quad \Delta t_3 = 2ms$
Input peak voltage: $5V$
Output peak voltage: $8V$
Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Figure.2 Specifications given in the lab prompt

For this experiment, f is chosen as 20 Hz. Therefore, the input is a square wave with a 5V peak-to-peak and 20 Hz frequency.

Analysis:

We need to divide the waveform into three parts:

1. Creating 2 ms (Δt_0) and 9 ms (sum of all Δt's) delays
2. Integrating both of the delayed waveforms to create the trapezoid's slanted sides
3. Subtracting one delayed and integrated waveform from the other to obtain the final waveform

In the circuit, LM324 OPAMP is used. The V_{CC} supply voltages of the OPAMPs are V_{CC}+=9.5V, V_{CC}-=0V (grounded).

To achieve 2 ms and 9 ms delays, a comparator OPAMP can be used. A reference voltage is added to the V- input of the OPAMP, which is V_{comp} = 2.5V. To the V+ input, a RC circuit is added. The comparator circuit's function is relays on the OPAMP's operating regions:

- When V+ > V_{comp} , the OPAMP is + SAT ⇒ Vout = V_{CC}+
- When V+ < V_{comp} , the OPAMP is – SAT ⇒ Vout = V_{CC}-

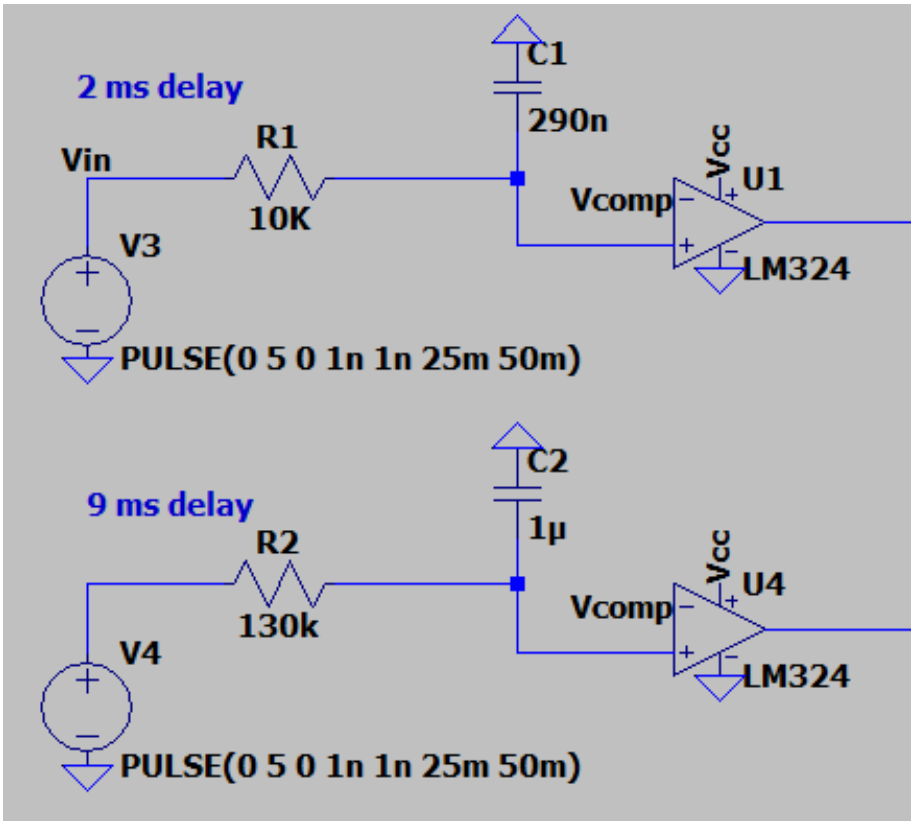


Figure.3 Delay circuits

To find the values of R and C in the RC circuits, we derive the KCL equations at the + inputs:

$$\frac{dV_C}{dt}C + \frac{V_C - V_{in}}{R} = 0 \Rightarrow \frac{dV_C}{dt} + \frac{V_C}{RC} = \frac{V_{in}}{RC} \quad (1)$$

The characteristic equation of (1) is:

$$\lambda + \frac{1}{RC} = 0 \Rightarrow \lambda = -\frac{1}{RC}$$

The natural response of (1) is:

$$V_{C,natural} = C_1 e^{-t/RC}$$

The forced response of (1) is:

$$V_{C,forced} = V_{in}$$

To find C_1, we can use the initial conditions. From Figure.1, the initial conditions are found as t = 0 & V_C = 0, thus making C_1 = -5. Then, the solution of V_C is:

$$V_C = V_{C,natural} + V_{C,forced} = -5e^{-\frac{t}{RC}} + 5$$

By using this equation, we conclude that the value of V_C should be equal to V_{comp} = 2.5V at t = 2 ms and t = 9 ms to achieve the needed delays. For t = 2 ms:

$$2.5 = -5e^{-\frac{2\text{ ms}}{R_1C_1}} + 5$$

$$R_1C_1 = 0.0029$$

and for t = 9 ms:

$$2.5 = -5e^{-\frac{9\text{ ms}}{R_2C_2}} + 5$$

$$R_2C_2 = 0.0130$$

The chosen values are:

R_1 = 10 KΩ, C_1 = 290 nF

R_2 = 130 KΩ, C_2 = 1 μF

Since the OPAMP is not LINEAR, the output voltage of the OPAMP is equal to V_{CC}+ = 9.5V when the OPAMP is +SAT, and equal to V_{CC}- = 0V when the OPAMP is –SAT.

Second step is to integrate the delayed waveforms to generate the trapezoid in the lab prompt. The integrator OPAMPs are shown in Figure.4.

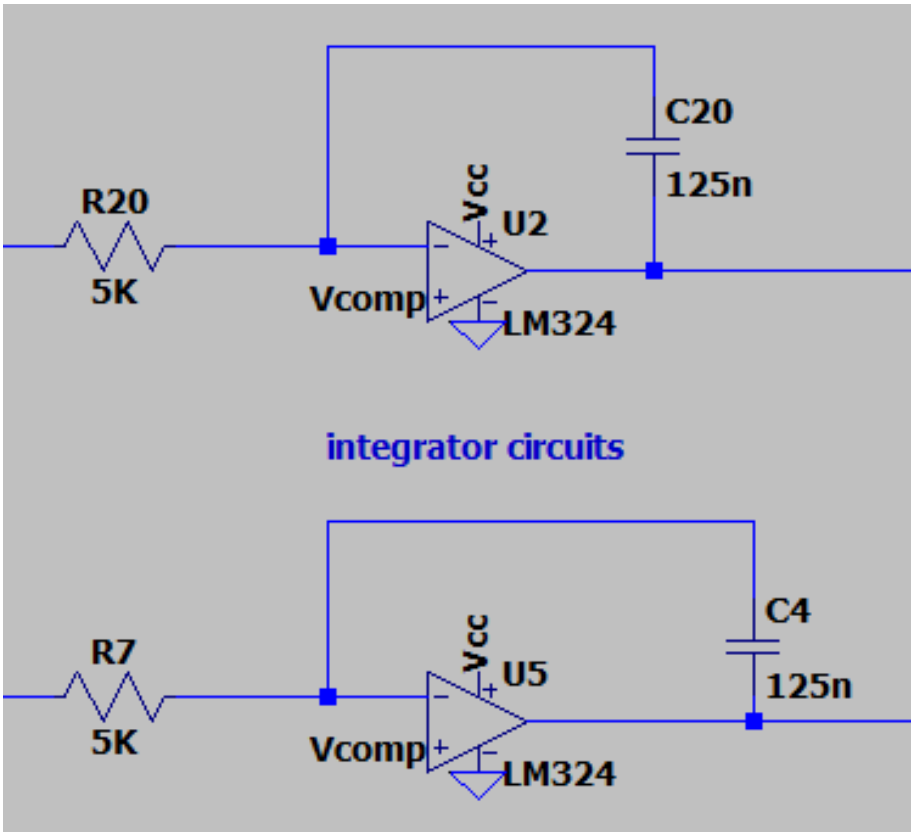


Figure.4 Integrator circuits

To derive the output equation, consider KCL at V-:

$$\frac{dV_C}{dt}C + \frac{V_- - V_{in}}{R} = 0 \Rightarrow dV_C = \frac{V_{in} - V_+}{RC}dt$$

Integrate both sides;

$$V_C = \frac{V_{in} - V_+}{RC}t + S, \text{ where S is a constant.}$$

S depends on the initial conditions. Since the initial conditions are t = 0 & V_C = 0, S = 0. Then, the solution of V_C is:

$$V_C = \frac{2.5}{RC}t$$

At t = 2 ms (since Δt_1 = 2 ms), V_C should be equal to V_{max} = 8V as required:

$$8 = \frac{2.5}{RC}(2\ ms)$$

The chosen values are:

$$R = 5\ K\Omega,\ C = 125\ nF$$

The last step is to subtract two waveforms from one another. The subtractor OPAMP is shown in Figure.5.

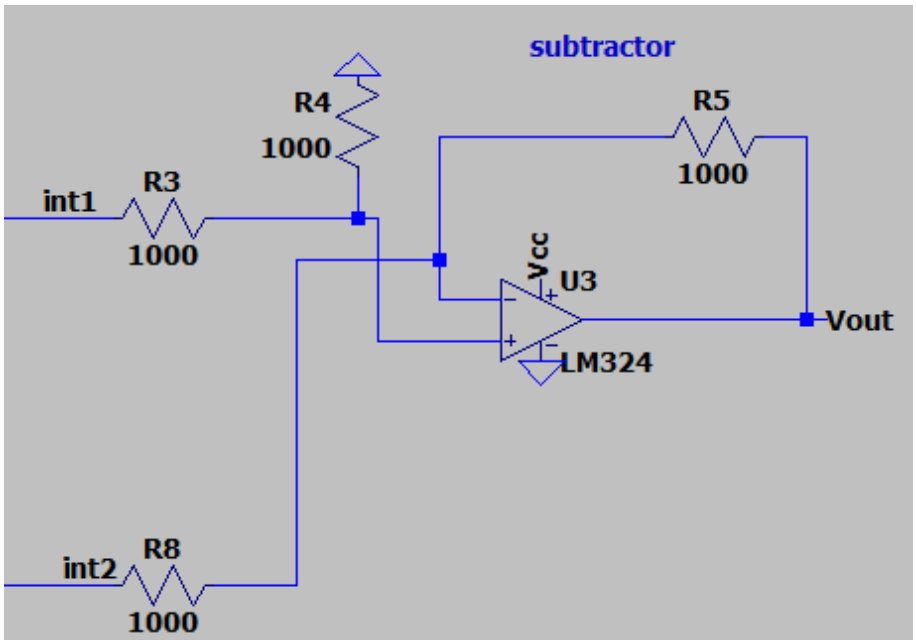


Figure.5 Subtractor circuit

KCL at V-:

$$\frac{V_{int2} - V_-}{R_8} = \frac{V_- - V_{out}}{R_5} \Rightarrow V_- = \left(\frac{V_{int2}}{R_8} + \frac{V_{out}}{R_5}\right)\frac{1}{\left(\frac{1}{R_5} + \frac{1}{R_8}\right)}$$

KCL at V+:

$$\frac{V_{int1} - V_+}{R_3} = \frac{V_+}{R_4} \Rightarrow V_+ = \frac{V_{int1}}{R_3\left(\frac{1}{R_3} + \frac{1}{R_4}\right)}$$

Assume that the OPAMP is not SAT:

$$V_- = V_+ \Rightarrow \left(\frac{V_{int2}}{R_8} + \frac{V_{out}}{R_5}\right)\frac{1}{\left(\frac{1}{R_5} + \frac{1}{R_8}\right)} = \frac{V_{int1}}{R_3\left(\frac{1}{R_3} + \frac{1}{R_4}\right)}$$

By choosing $R_3 = R_4 = R_5 = R_8$, the equation reduces to:

$$Vout = Vint1 - Vint2$$

For this subtractor, $R_3 = R_4 = R_5 = R_8 = 1$ KΩ.

Simulations:

The complete waveform generator circuit is shown in Figure.6.

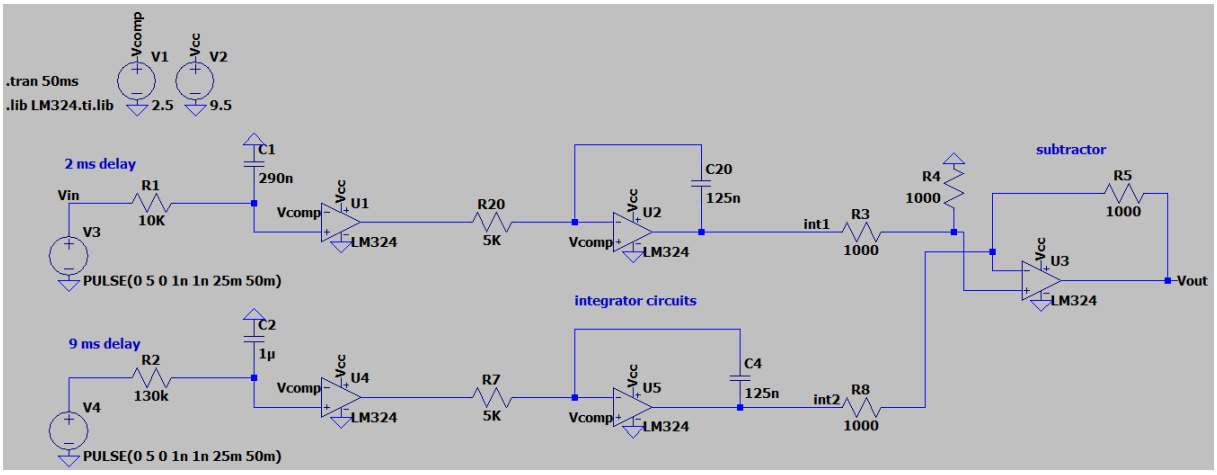


Figure.6 Waveform generator circuit

Figures.7-15 are the required plots. Table.1 holds the error calculations.

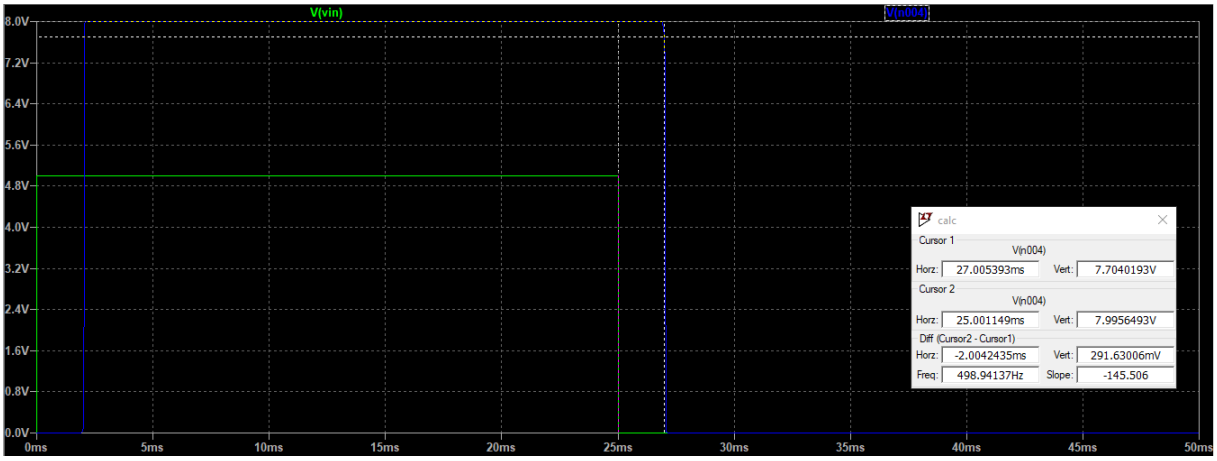


Figure.7 The 2 ms delay (result is 2.004 ms)

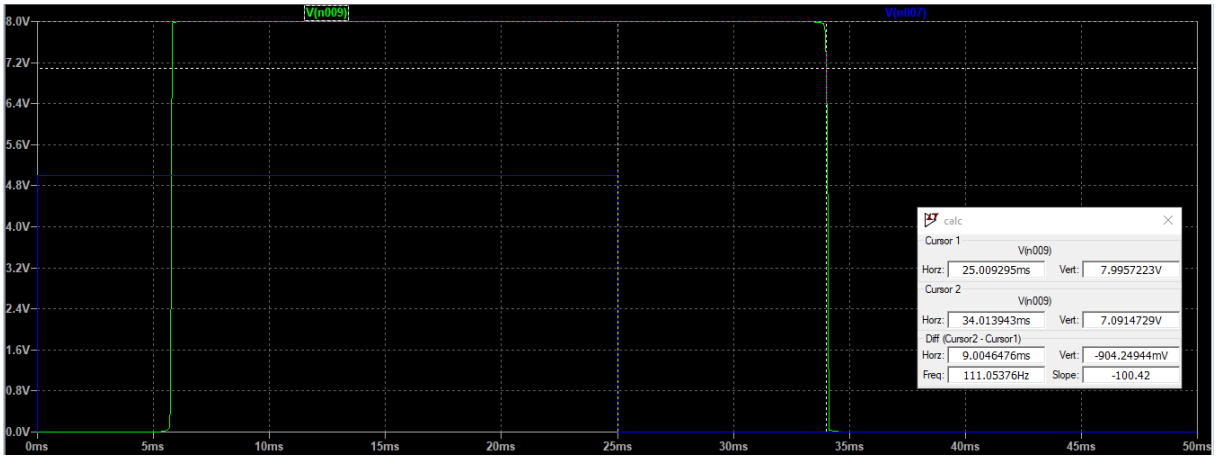


Figure.8 The 9 ms delay (result is 9.005 ms)

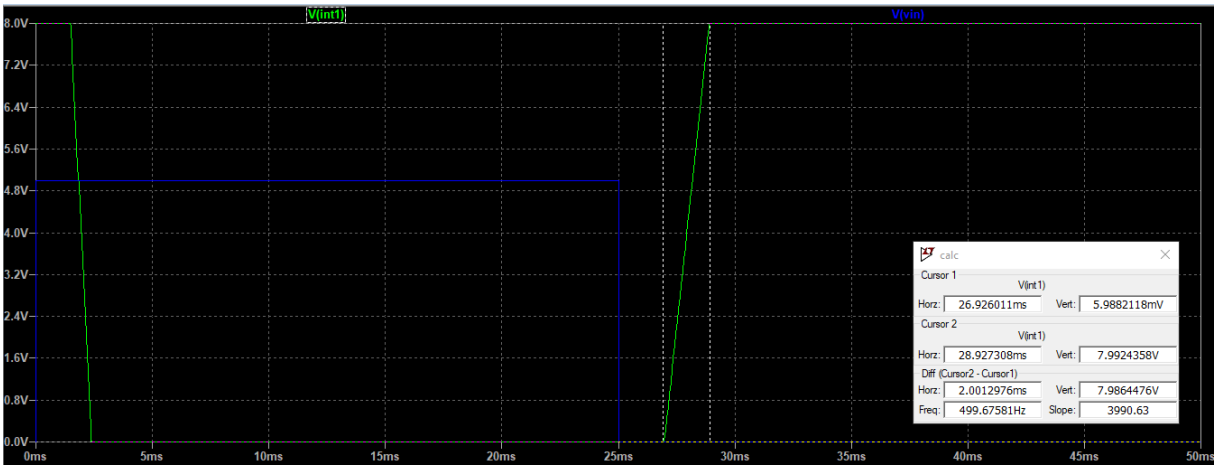


Figure.9 Output of the integrating OPAMP, which is connected to 2 ms delay, Δt_1 = 2.001 ms

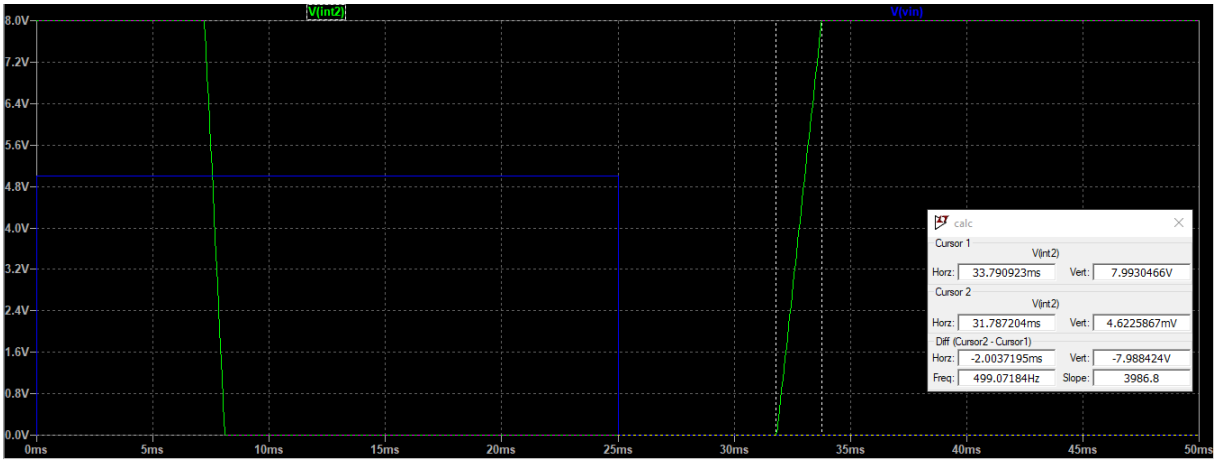


Figure.10 Output of the integrating OPAMP, which is connected to 9 ms delay, Δt_3=2.004ms

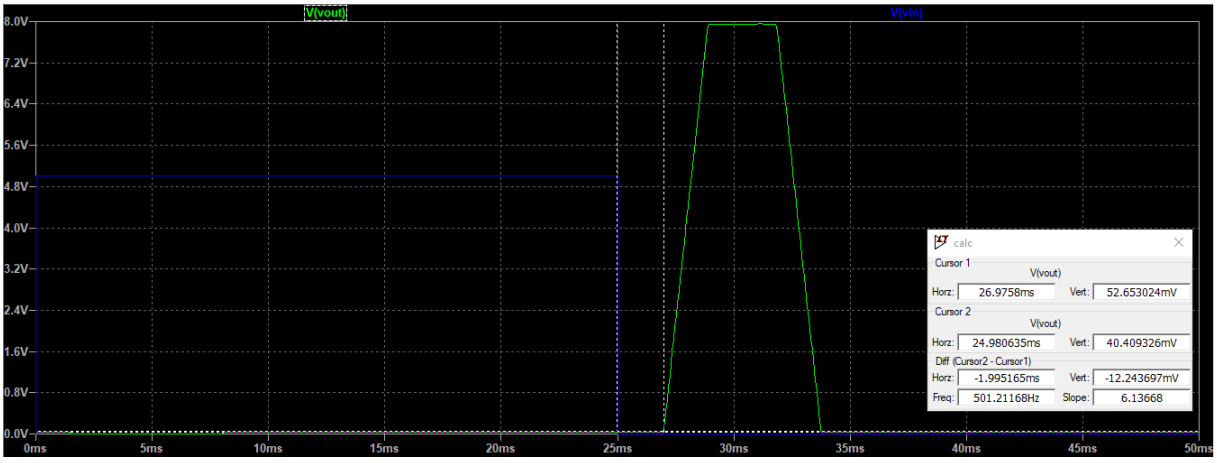


Figure.11 Δt_0 = 1.995 ms

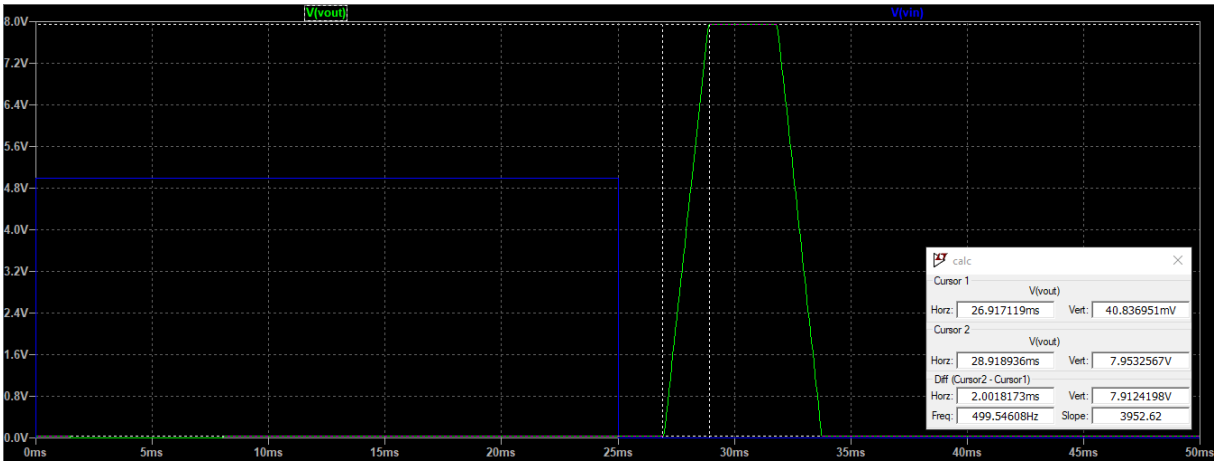


Figure.12 Δt_1 = 2.001 ms

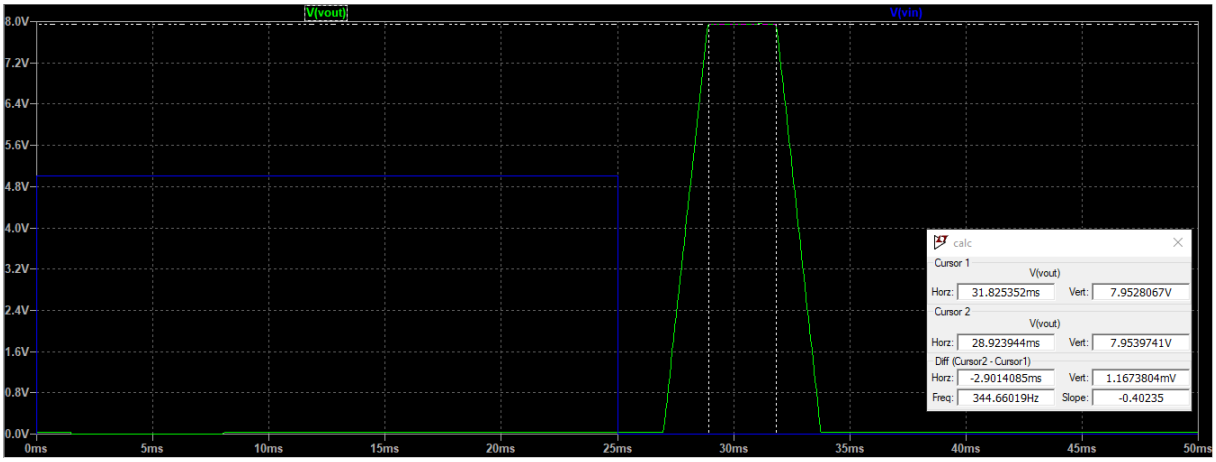


Figure.13 Δt_2 = 2.901 ms

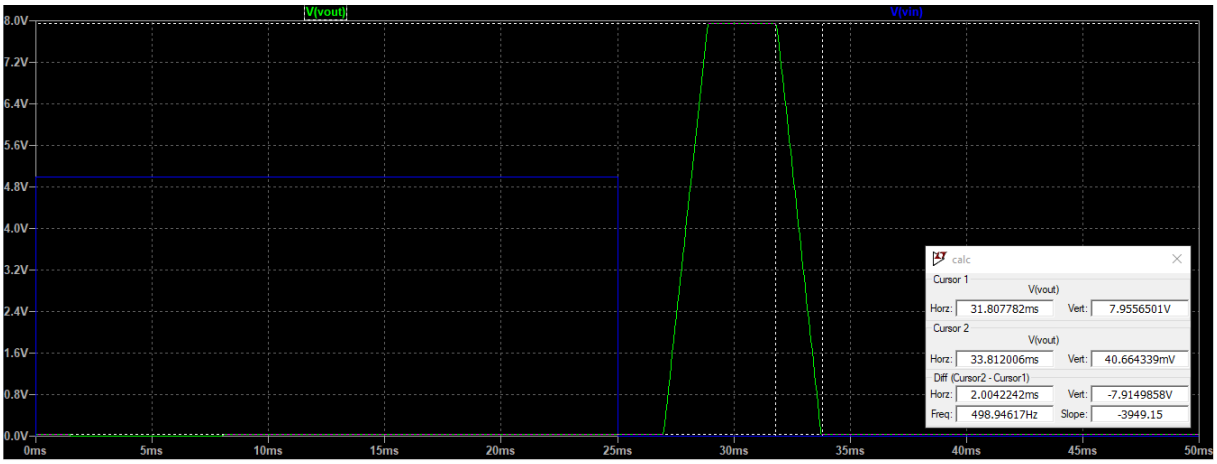


Figure.14 Δt_3 = 2.004 ms

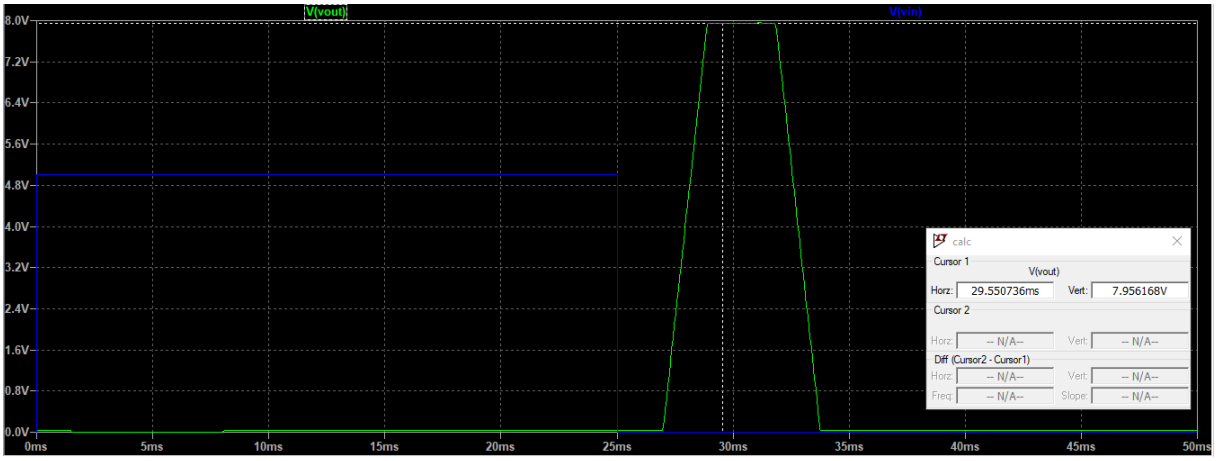


Figure.15 Maximum value of V_{out} = 7.956V

	Δt_0	**Δt_1**	**Δt_2**	**Δt_3**	**Maximum V_{out}**
Expected value	2 ms	2 ms	3 ms	2 ms	8 V
Simulation value	1.995 ms	2.001 ms	2.901 ms	2.004 ms	7.956 V
Error	%0.25	%0.05	%3.3	%0.2	%0.55

Table.1 Simulation results & error calculations

As one can see in Table.1, all the errors are within the %±10 error bound as required.

HW Implementation

In HW implementation, 2 LM324 OPAMPs are used. The circuit is constructed according to the SW implementation. The supply voltages of the OPAMPs are V_{CC}+ = 9.5 V (supplied to a red line), and V_{CC}- = 0, which are achieved by the DC voltage source in the lab. For ease of use, the circuit is constructed on a breadboard. The complete circuit can be seen in Figure.16.

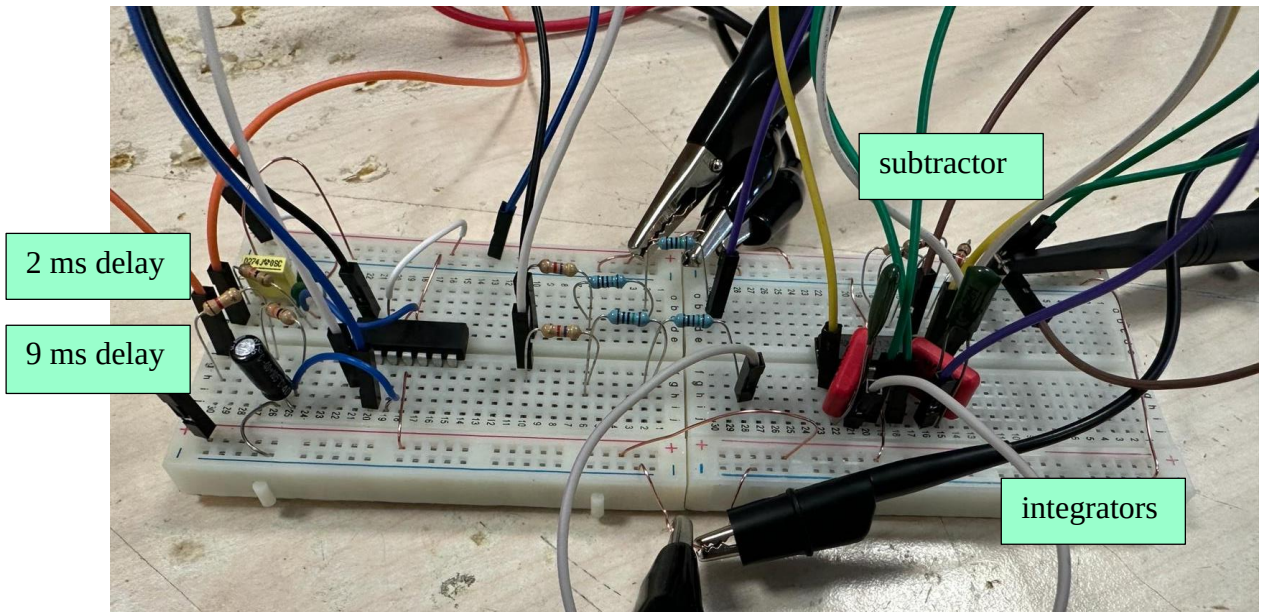


Figure.16 Waveform generator circuit on breadboard

V_{in} is a square wave with 2.5V peak-to-peak (signal generator provides the circuit twice this value), 20 Hz frequency and 1.25 V offset to make sure that the voltage stays on the positive region at all times. V_{comp} is supplied to the other red line of the breadboard with a magnitude of 2.5 V by using the other channel of the DC voltage source.

Then the measurements are taken by using the cursors of the oscilloscope, shown in Figures.17-25, and the errors are calculated in Table.2.

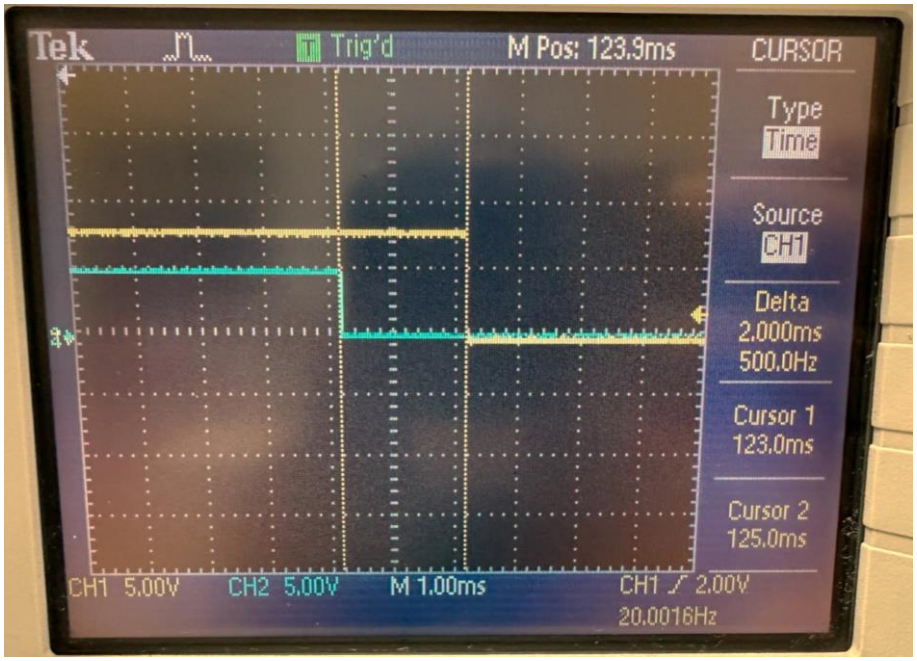


Figure.17 The 2 ms delay (shown in yellow) & V_{in} (shown in blue)

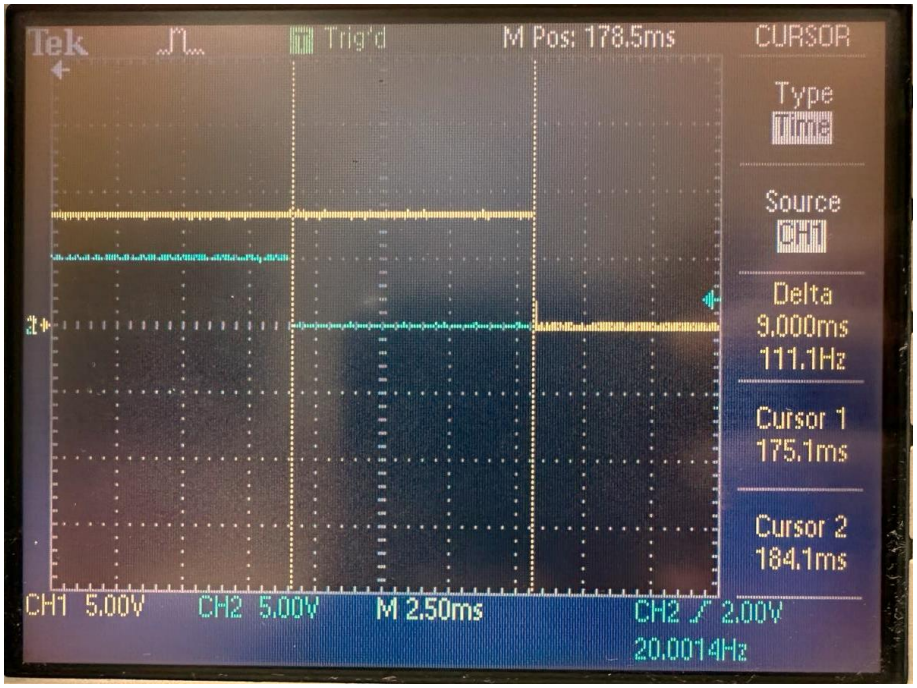


Figure.18 The 9 ms delay (shown in yellow) & V_{in} (shown in blue)

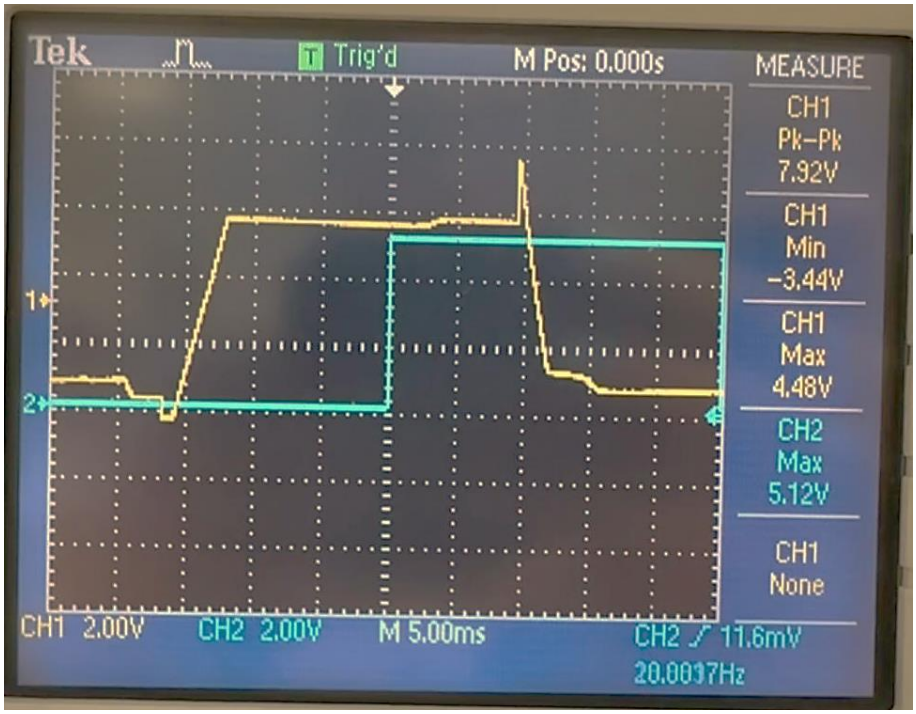


Figure.19 Output of the integrating OPAMP, which is connected to 2 ms delay

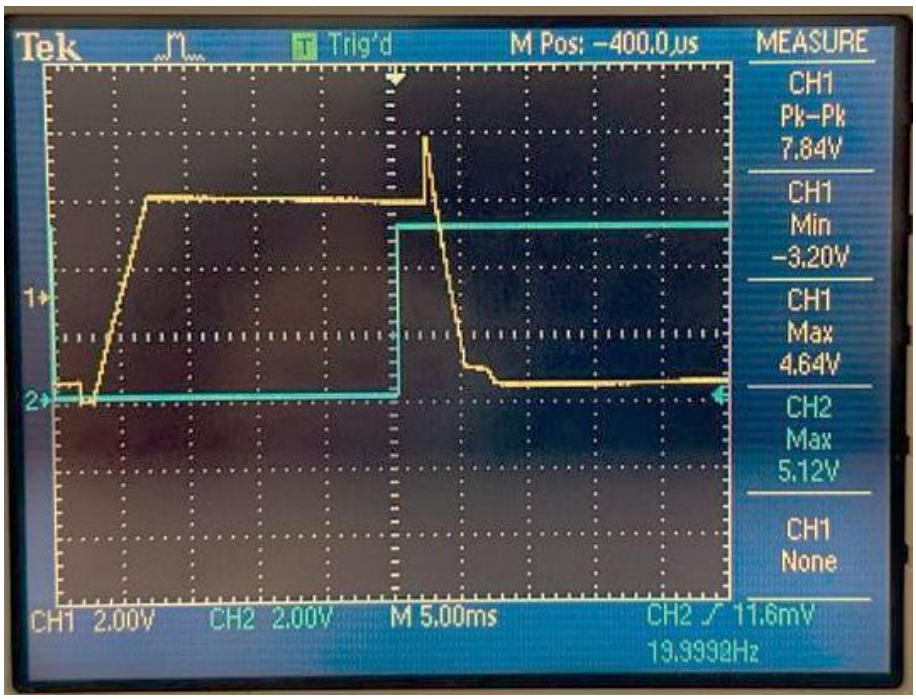


Figure.20 Output of the integrating OPAMP, which is connected to 9 ms delay

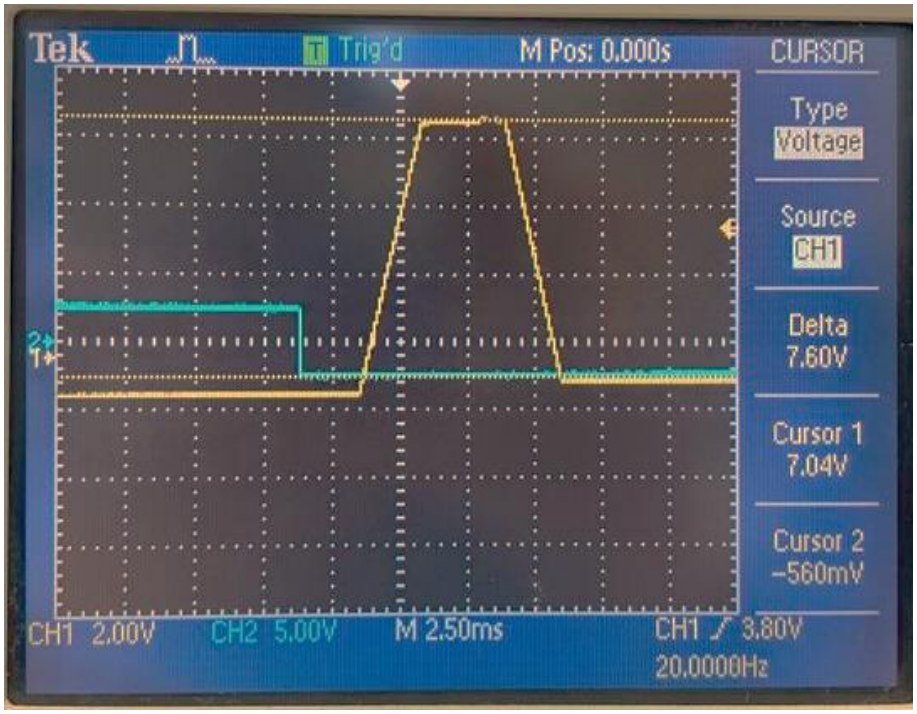


Figure.21 V_{in} (shown in blue) & V_{out} (shown in yellow), maximum V_{out} = 7.60V

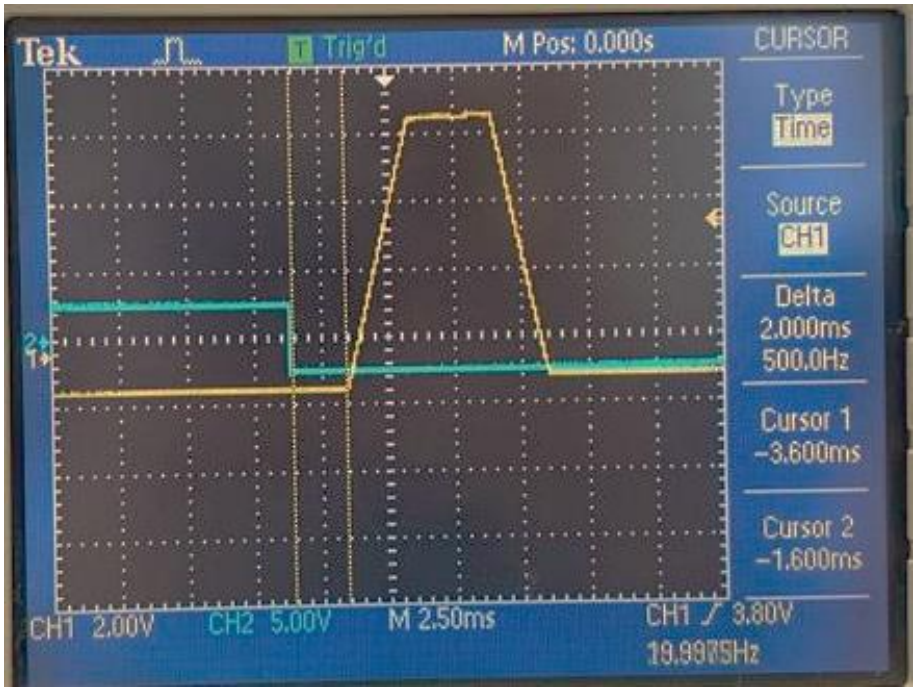


Figure.22 Δt_0 = 2.000 ms

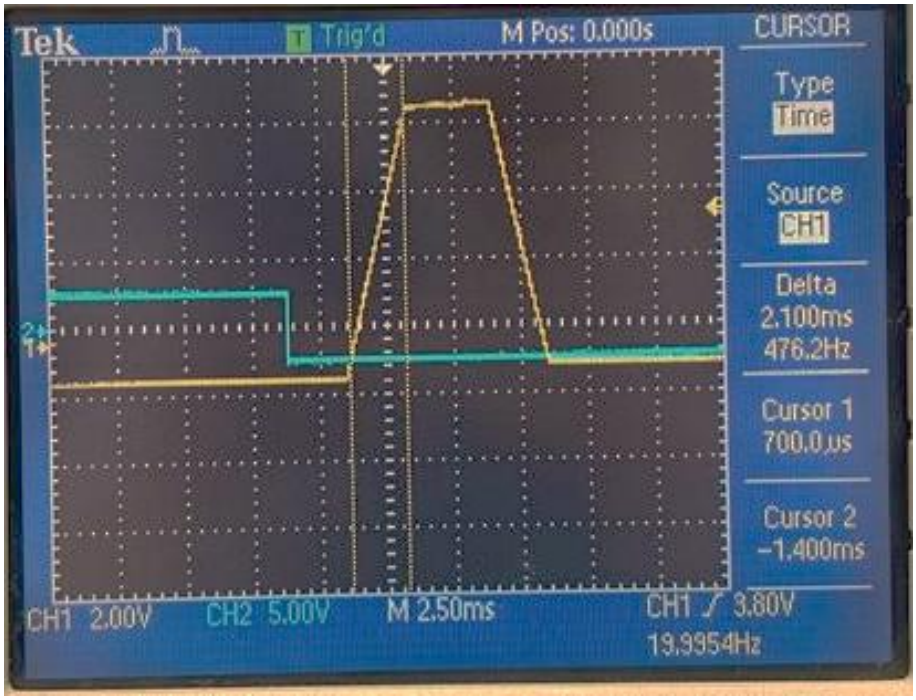


Figure.23 Δt_1 = 2.100 ms

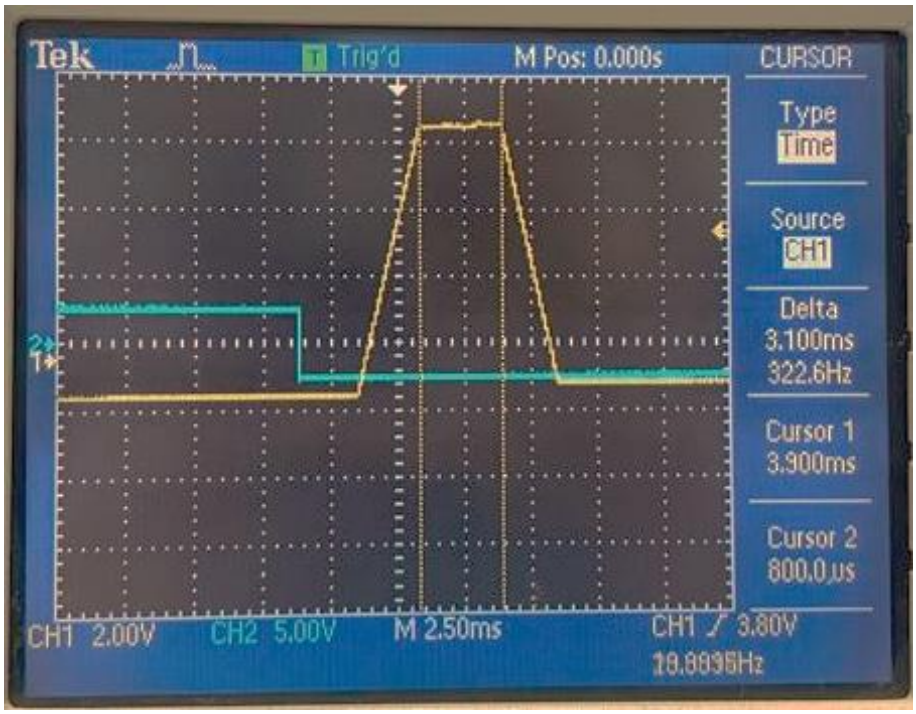


Figure.24 Δt_2 = 3.100 ms

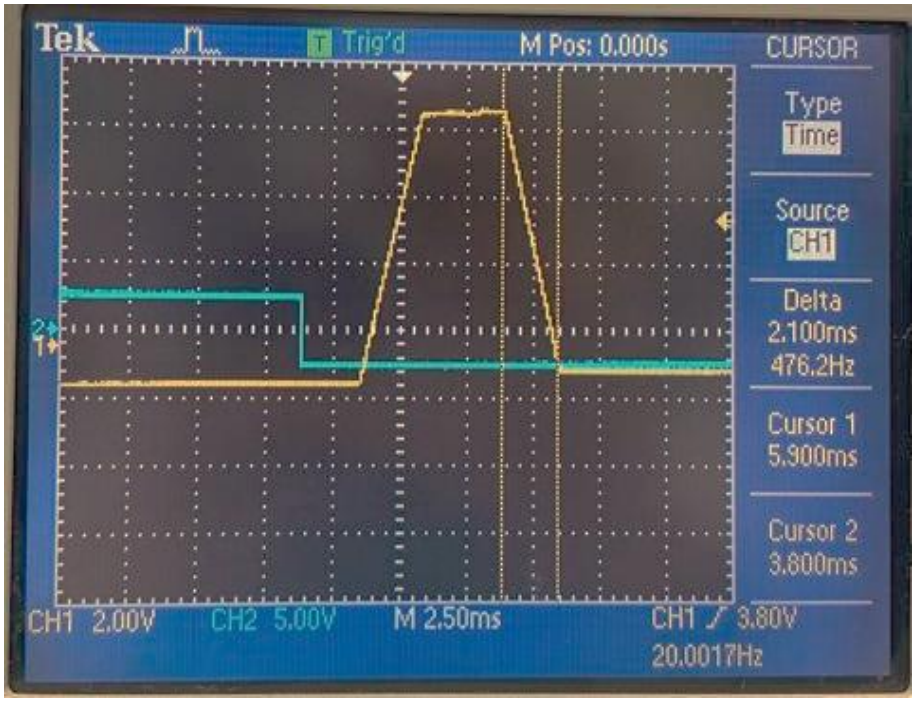


Figure.25 Δt_3 = 2.100 ms

	Δt_0	**Δt_1**	**Δt_2**	**Δt_3**	**Maximum V_{out}**
Expected value	2 ms	2 ms	3 ms	2 ms	8 V
Measured value	2.000 ms	2.100 ms	3.100 ms	2.100 ms	7.60 V
Error	0	%5	%3.33	%5	%5

Table.2 Hardware results & error calculations

As one can see in Table.2, all the errors are within the %±20 error bound as required.

Conclusion

The software results for Δt_0, Δt_1, Δt_2, Δt_3 and maximum V_{out} matched with %0.25, %0.05, %3.3, %0.2 and %0.55 percentile errors respectively. The reason of these errors can be the internal delays of the OPAMPs, which were not taken into account in the calculations and derivations of the KCL equations. However, the errors are minimal and still satisfy the %±10 error boundaries.

The hardware results for Δt_0, Δt_1, Δt_2, Δt_3 and maximum V_{out} matched with 0, %5, %3.33, %5 and %5 percentile errors respectively. The reason of these errors can be the internal delays of the OPAMPs, non-accurate values of the resistors and the capacitors (tolerances are nonzero), inner resistances of the wires and the OPAMPs, internal resistance of the signal generator or human error. The errors are high compared to the software simulations but they are still in the %±20 error boundaries. Also, since the values found and chosen for R and C at each step are not standard values, to achieve them, I had to use multiple resistors or capacitors. This could be another cause of error.

This lab was designed to teach us how to manipulate any waveform into any shape by using OPAMPs and RC circuits. It taught how to derive KCL equations at the pins of an OPAMP and how to analyze them. By choosing relevant equations & initial conditions, we can create comparators (to have delays), integrators, subtractors, etc. Overall the experiment was successful.