T.R.
GEBZE TECHNICAL UNIVERSITY
FACULTY of ENGINEERING
DEPARTMENT of COMPUTER ENGINEERING

NGSPICE SIMULATOR, MAGIC LAYOUT and TRANSISTOR LEVEL SCHEMATIC

CSE 436/536 DIGITAL INTEGRATED CIRCUITS ASSIGNMENT 1 REPORT

STUDENT
Şeyda Nur DEMİR
12 10 44 042

LECTURER
Alp Arslan BAYRAKÇI

TEACHING ASSISTANT
-

KOCAELİ, 2020

1.DESCRIPTION

The project consists of 3 parts.

1.NGSPICE SIMULATOR

In this assignment you will go through the Spice tutorial and plot every graph inside the tutorial. The Spice Tutorial is under Files > Class Materials of Teams Class Page. Take the screenshot of your Spice plots and put them inside a zip file and post that zip file before the due date.

2.MAGIC LAYOUT

Install Magic on your computer and take a screenshot of Magic. Put that in the zip file.

3.TRANSISTOR LEVEL SCHEMATIC

Draw the transistor level schematic for the oai321 logic cell given below:

$$Z = \overline{(A + B + C) \cdot (D + E) \cdot F}$$

Add the screenshot of your schematic to the zip file.

2.RULES

No cheating.

3.SUBMISSION

3.1.Files

Name your zip file as StudentName_StudentSurname_StudentId_Assignment1.zip.

3.2. Deadline

Submit your project due to 28.10.2020 17:00.

3.3.Grading

You will be graded over 100 points.

4.WHAT DID I DO?

1.NGSPICE SIMULATOR

I followed Ngspice tutorial, I took screenshots of my all steps. I completed all steps and plotted all graphs in tutorial. I added my screenshots to a subfolder named as Part1.

Note : There is an extra gif file in tutor-spice3 folder you shared with us on teams class materials, named as “tut_spice3_invertor5.gif”, but tutorial does not contain any part about of this plot. I did not plot this graph because you asked us to follow the steps in the tutorial, but I supposed to I can add required code part into the cir file.

2.MAGIC LAYOUT

I installed Magic, I opened it and I took screenshots in it. I added my screenshots to a subfolder named as Part2.

Note : This part seemed so easy to me, I think it is easy because it is our first assignment, but if I missed something I apologize to submit only Magic Layout’s first screen.

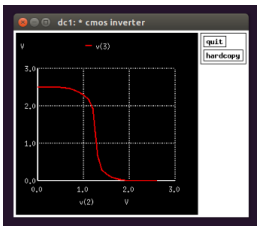
3.TRANSISTOR LEVEL SCHEMATIC

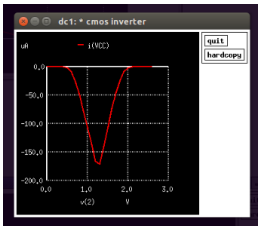
I drew the transistor level schematic for oai321 logic cell. I explained my all steps in my solution paper. Also I saw transistor sizing on internet, and I only tried to size my transistors, I think our assignment does not require transistor sizing but I added again it. I took photo of my handwritten solution about this question, I added these photos to a subfolder named as Part3.

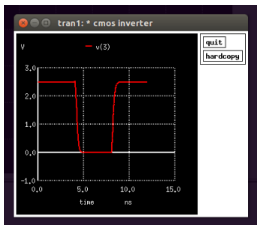
Note : Follow this link to see document about transistor sizing that I use.

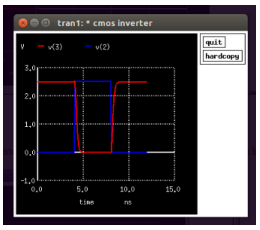
Screenshots from my submission :

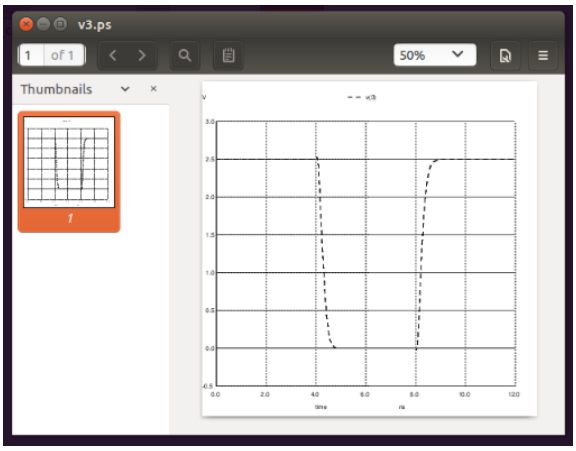
Part1

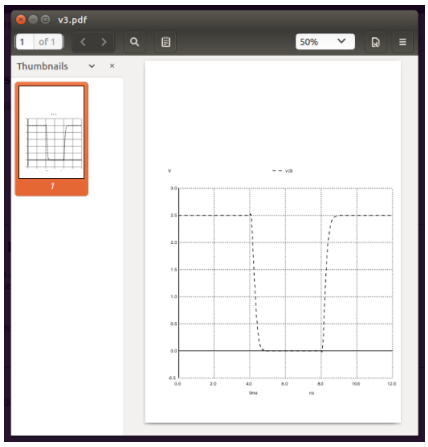




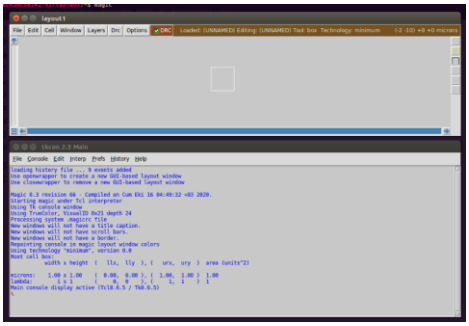




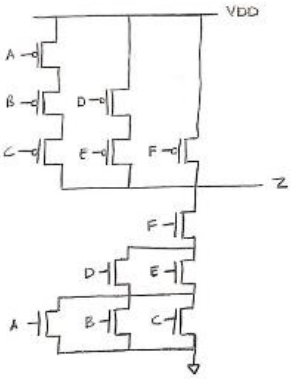




Part2



Part3



5.WHAT DID NOT I DO?

- I think I did my assignment all.

END OF THE REPORT

UPDATED : Nov 28, 2020 Wednesday 08:20 AM

STUDENT
Şeyda Nur DEMİR
12 10 44 042

LECTURER
Alp Arslan BAYRAKÇI

TEACHING ASSISTANT
-

KOCAELİ, 2020