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GEBZE TECHNICAL UNIVERSITY
FACULTY of ENGINEERING
DEPARTMENT of COMPUTER ENGINEERING

MAGIC LAYOUT, NGSPICE SIMULATOR and 2-inputs NAND GATE DESIGN

CSE 436/536 DIGITAL INTEGRATED CIRCUITS ASSIGNMENT 2 REPORT

STUDENT
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LECTURER
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TEACHING ASSISTANT
-

KOCAELİ, 2020

1.DESCRIPTION

The assignment consists of 3 parts.

In this assignment you will design a 2-input NAND gate using Magic Layout Tool and will prove that it Works as a NAND gate using Spice simulator.

For that purpose use the best form of plot in your spice tutorial and record the resultant plot in your report.

The report should contain your magic layout, your extracted Spice circuit and the resultant plot proving the functionality of a NAND gate.

Include your magic file, spice circuit and plot image in the zip file and submit that file to Teams submission page.

1.MAGIC LAYOUT

… you will design a 2-input NAND gate using Magic Layout Tool …

2.NGSPICE SIMULATOR

… will prove that it Works as a NAND gate using Spice simulator …

3.PLOT SCREENSHOT

… include plot image …

2.RULES

Name your zip file as:
StudentName_StudentSurname_StudentId_Assignment2.zip
Be careful in naming conventions. Otherwise you lose 10 points.
And no cheating.

An Important Requirement to Work On My Assignment :

You need these files to work on my assignment :

- SCN5M_DEEP.12.TSMC.tech27 (25 micron technology file)
- tsmc_cmos025 (library)

Execution Steps :

- cd File
-
- magic -T SCN5M_DEEP.12.TSMC.tech27
-
- Open > Open File … (nand2_seyda.mag)
-
- cd File
-
- ngspice
-
- source nand2_seyda.spice
-
- run
-
- plot v(VinA) v(VinB) v(Vout)
-
- exit

3.SUBMISSION

3.1.Files

Name your zip file as StudentName_StudentSurname_StudentId_Assignment2.zip.

3.2. Deadline

Submit your project due to 06.11.2020 ~~17:00~~ 23:59.

3.3.Grading

You will be graded over 100 points.

4.WHAT DID I DO?

1.MAGIC LAYOUT (nand2_seyda.mag)

I followed transistor level schematics, I drew NAND gate's inner structure before.

Then I studied truth table, making stick diagram, rules and conventions.

I followed all rules to design my gate.

2.NGSPICE SIMULATOR (nand2_seyda.spice)

I drew my gate on Magic Layout, extract it, and exttospice it.

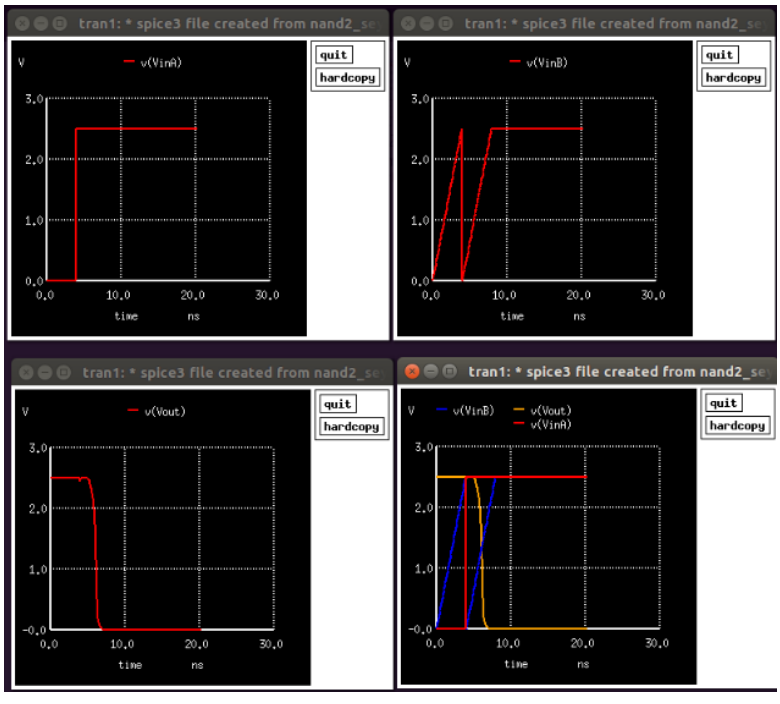
Then I run it on ngspice simulator.

- source nand2_seyda.spice
- run
- plot v(VinA) v(VinB) v(Vout)

3.PLOT IMAGE (plot.png)

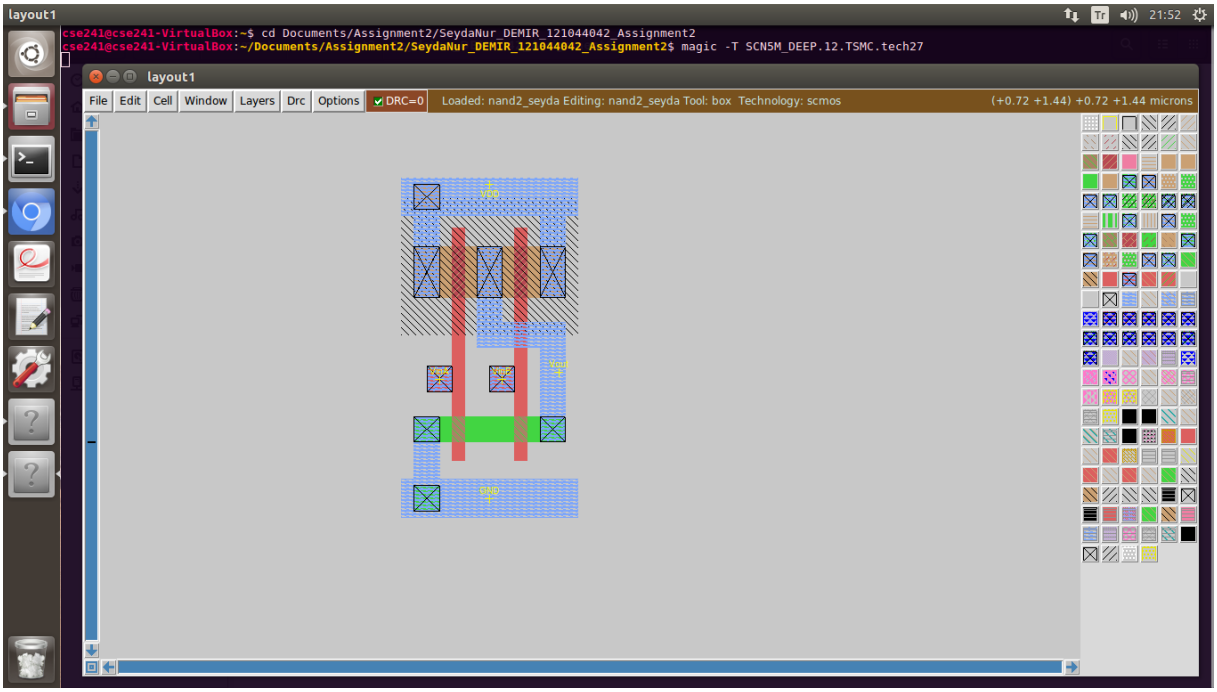
I gave values to test my design in code, extract my circuit, and plot my graphic.

- plot v(VinA)
- plot v(VinB)
- plot v(Vout)
- plot v(VinA) v(VinB) v(Vout)



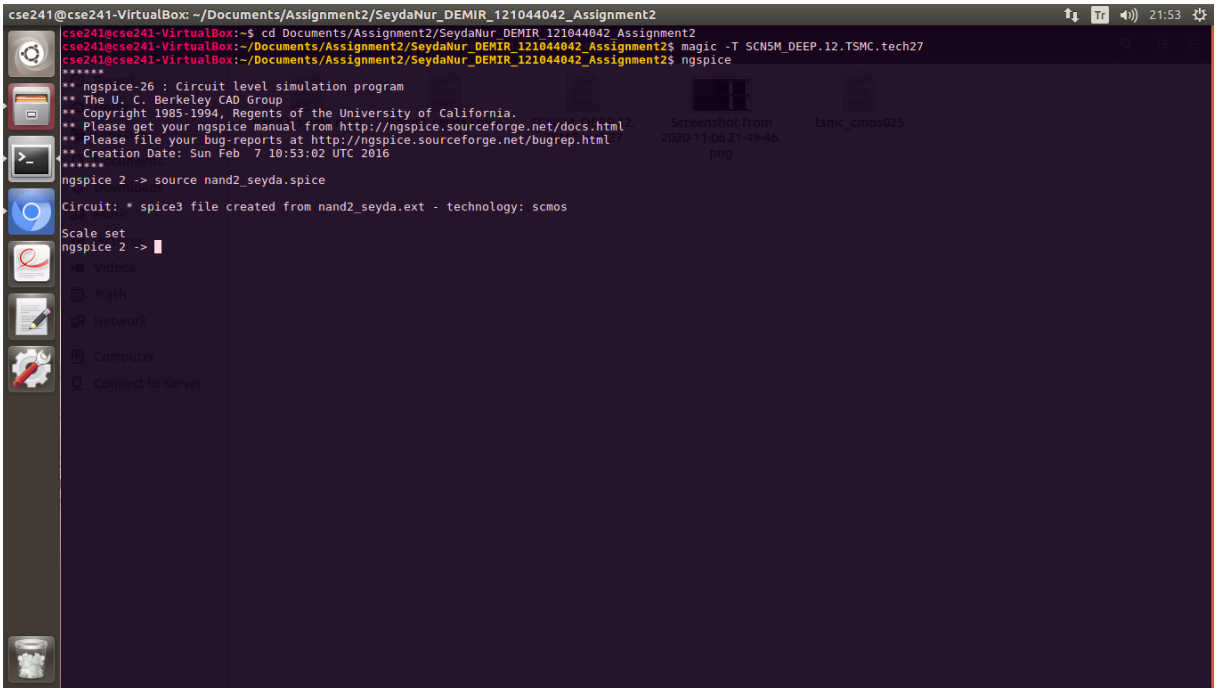
Screenshots from my assignment :

Part1 (nand2_seyda.mag)

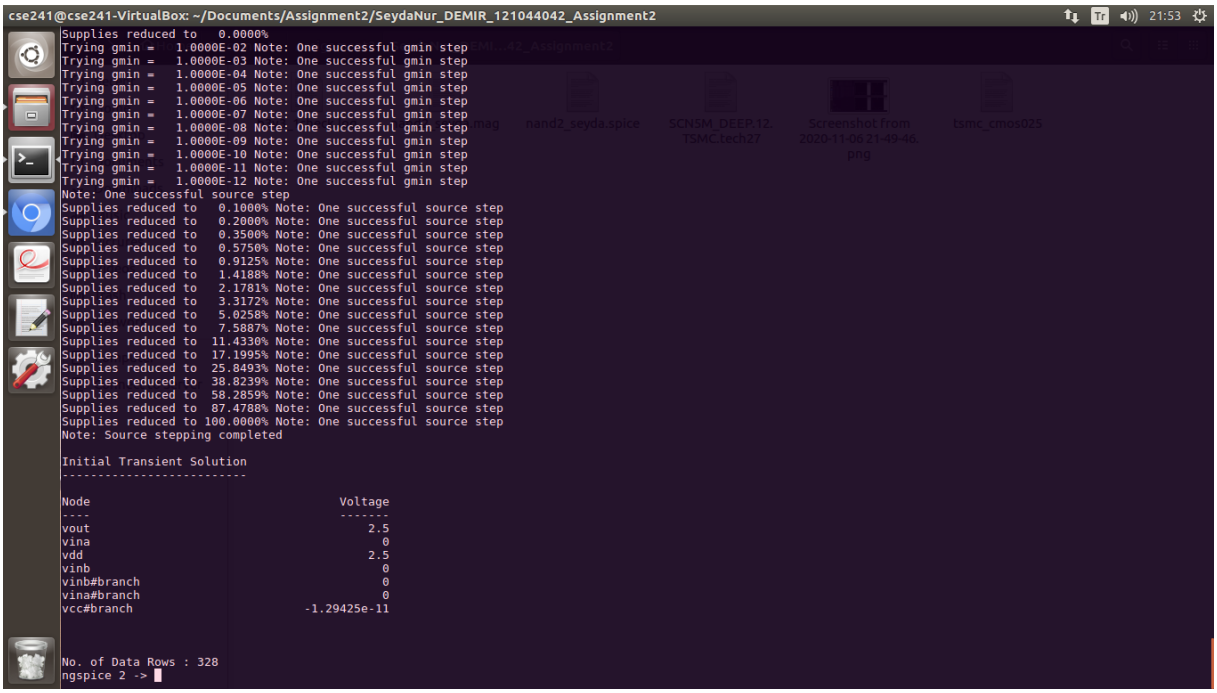


Part2 (nand2_seyda.spice)

Source nand2_seyda.spice



run

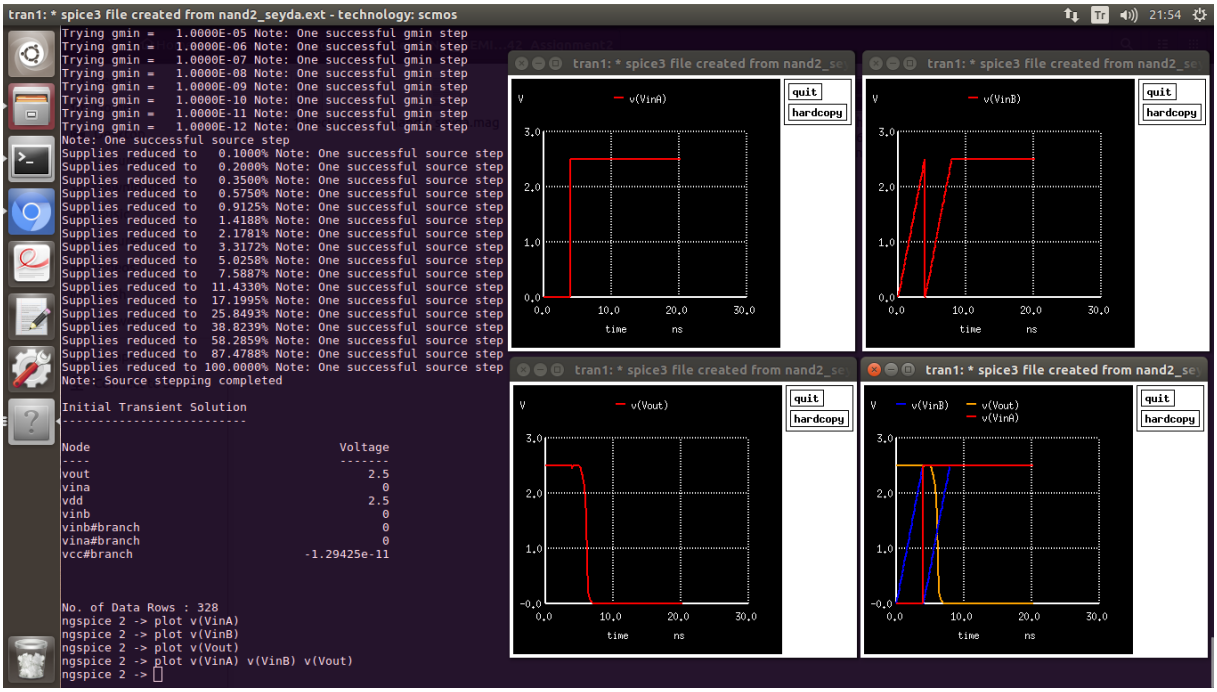


plot v(VinA)

plot v(VinB)

plot v(Vout)

plot v(VinA) v(VinB) v(Vout)



exit

```
cse241@cse241-VirtualBox: ~/Documents/Assignment2/SeydaNur_DEMIR_121044042_Assignment2
Trying gmin =   1.0000E-07 Note: One successful gmin step
Trying gmin =   1.0000E-08 Note: One successful gmin step
Trying gmin =   1.0000E-09 Note: One successful gmin step
Trying gmin =   1.0000E-10 Note: One successful gmin step
Trying gmin =   1.0000E-11 Note: One successful gmin step
Trying gmin =   1.0000E-12 Note: One successful gmin step
Note: One successful source step
Supplies reduced to   0.1000% Note: One successful source step
Supplies reduced to   0.2000% Note: One successful source step
Supplies reduced to   0.3500% Note: One successful source step
Supplies reduced to   0.5750% Note: One successful source step
Supplies reduced to   0.9125% Note: One successful source step
Supplies reduced to   1.4188% Note: One successful source step
Supplies reduced to   2.1781% Note: One successful source step
Supplies reduced to   3.3172% Note: One successful source step
Supplies reduced to   5.0258% Note: One successful source step
Supplies reduced to   7.5887% Note: One successful source step
Supplies reduced to  11.4330% Note: One successful source step
Supplies reduced to  17.1995% Note: One successful source step
Supplies reduced to  25.8493% Note: One successful source step
Supplies reduced to  38.8239% Note: One successful source step
Supplies reduced to  58.2859% Note: One successful source step
Supplies reduced to  87.4788% Note: One successful source step
Supplies reduced to 100.0000% Note: One successful source step
Note: Source stepping completed

Initial Transient Solution
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Node                                   Voltage
----                                   -------
vout                                       2.5
vina                                         0
vdd                                        2.5
vinb                                         0
vinb#branch                                  0
vina#branch                                  0
vcc#branch                       -1.29425e-11


No. of Data Rows : 328
ngspice 2 -> plot v(VinA)
ngspice 2 -> plot v(VinB)
ngspice 2 -> plot v(Vout)
ngspice 2 -> plot v(VinA) v(VinB) v(Vout)
ngspice 2 -> exit
ngspice-26 done
cse241@cse241-VirtualBox:~/Documents/Assignment2/SeydaNur_DEMIR_121044042_Assignment2$
```
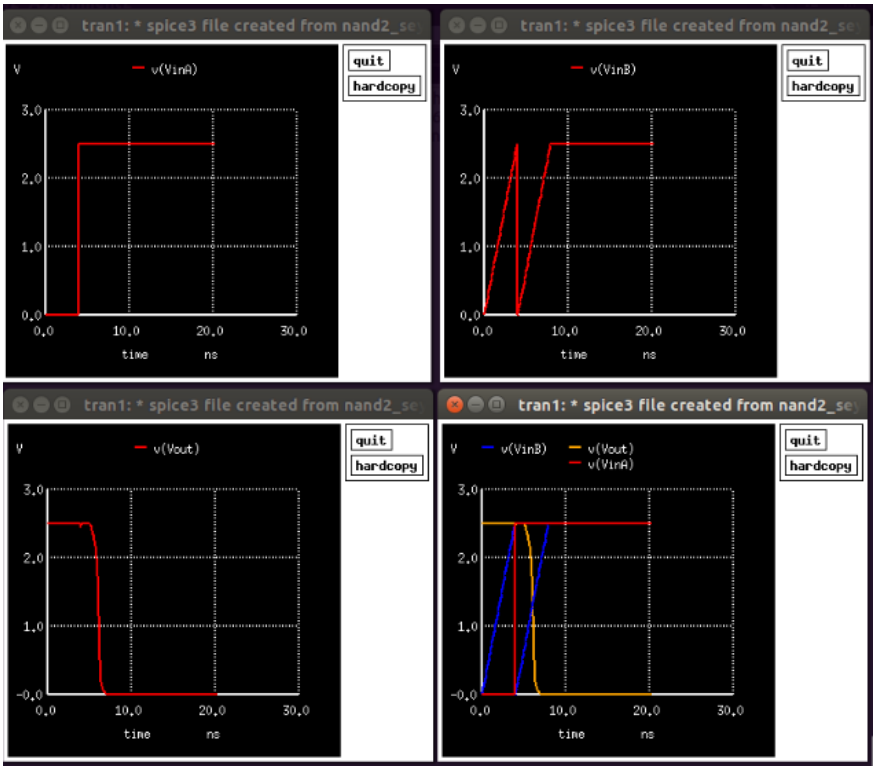
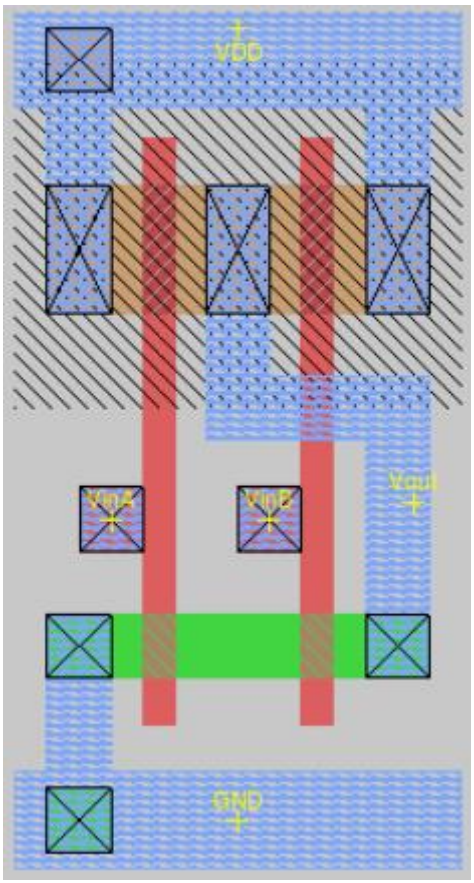
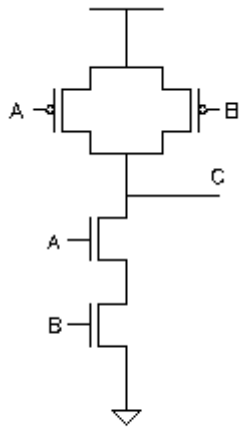

Part3 (plot.png)



Magic Layout (nand2_seyda.mag) :



Its Logic Level Schematic :

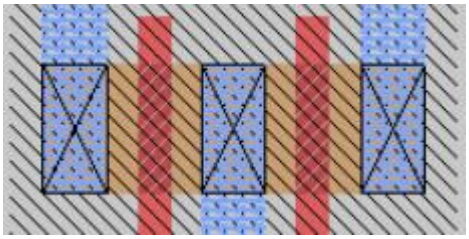


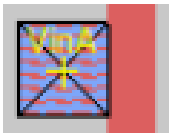
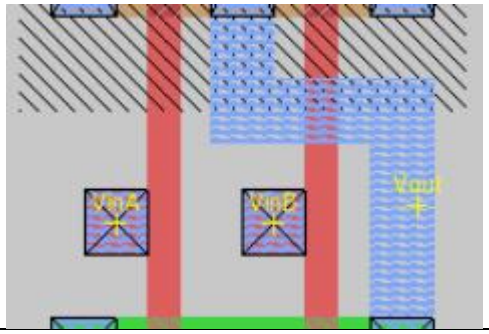
NAND

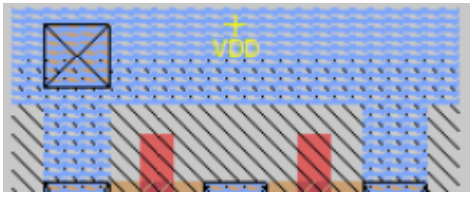
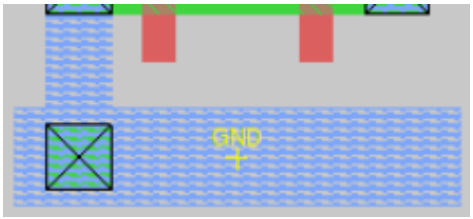
Its truth table :

2 - input NAND gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

nMOS Transistor Structure :	**pMOS Transistor Structure :**
	
VinA . VinB are **series** on nMos	VinA + VinB are **parallel** on pMos

VinA :	**VinB :**	**Vout :**
		

VDD :	**GND :**
	

Spice Simulator (nand2_seyda.spice) :

created from Magic Layout

```
* SPICE3 file created from nand2_seyda.ext - technology: scmos

.option scale=0.12u

M1000 Vout VinA VDD w_n32_n23# pmos w=8 l=2
+  ad=64 pd=32 as=112 ps=72
M1001 VDD VinB Vout w_n32_n23# pmos w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1002 a_n22_n40# VinA GND Gnd nmos w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1003 Vout VinB a_n22_n40# Gnd nmos w=4 l=2
+  ad=24 pd=20 as=0 ps=0
C0 w_n32_n23# Vout 1.9fF
C1 VinB Vout 0.2fF
C2 w_n32_n23# VDD 5.5fF
C3 w_n32_n23# VinA 2.6fF
C4 w_n32_n23# VinB 2.6fF
C5 Vout Gnd 3.2fF
C6 VinB Gnd 5.6fF
C7 VinA Gnd 5.6fF
C8 VDD Gnd 3.6fF
```

added by me

```
*--------------------------------------------------------

VCC Vdd 0 DC=2.5

VinA VinA 0 PWL(  0  0   3.9N  0     4N  2.5   7.9N  2.5   8N   2.5   )
VinB VinB 0 PWL(  0  0   3.9N  2.5   4N  0     7.9N  2.5   8N   2.5   )

.TRAN 0.1N  20.2N
.DC VINa 0 2.6 0.1

.OPTIONS TEMP=25 reltol = 1e-6

.include tsmc_cmos025

.END

*--------------------------------------------------------
```

VinA		VinB		Wanted Vout	
0	0	0	0	1	2.5
0	0	1	2.5	1	2.5
1	2.5	0	0	1	2.5
1	2.5	1	2.5	0	0

END OF THE REPORT

UPDATED : Nov 6, 2020 Friday 10:30 PM

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KOCAELİ, 2020