T.R.
GEBZE TECHNICAL UNIVERSITY
FACULTY of ENGINEERING
DEPARTMENT of COMPUTER ENGINEERING

CELL LIBRARY

CSE 436/536 DIGITAL INTEGRATED CIRCUITS
ASSIGNMENT 3 REPORT

STUDENT
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LECTURER
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TEACHING ASSISTANT
-

KOCAELİ, 2020

1.DESCRIPTION

The assignment consists of 1 part.

In this assignment, using Magic Layout Tool you will design a 0.25um TSMC process standard cell library including:

- INV
- NAND2
- NAND3
- NOR2
- NOR3
- XOR2
- XNOR2
- AOI22
- OAI22
- MUX2x1

✓ Use as few Metal layers as possible.

✓ All transistor must be at 2 lambda gate length.

✓ The cells must be at same height.

✓ The cells must as shrinked as possible.

✓ Extract each cell in Magic and simulate in Spice to verify the functionality. Test all possible inputs for each cell.

✓ Prepare a report as a manual for your library. In the report:
1. Show the stick diagram for each cell.
2. Put a small magic layout picture of each cell
3. Put the transistor level schematic of each cell.
4. Pus the Spice simulation plots showing the functionality of each cell.
5. Write down the size of each cell in lambdas.

✓ Put your report, your magic layouts (.mag files), your spice extracted circuit decks (.cir files) into a zip file. Name your zip file as:

StudentName_StudentSurname_StudentId_Assignment3.zip

Be careful in naming conventions. Otherwise you lose 10 points.

2.RULES

Obey the rules given above.
No cheating.

3.SUBMISSION

3.1.Files

Name your zip file as StudentName_StudentSurname_StudentId_Assignment3.zip.

3.2. Deadline

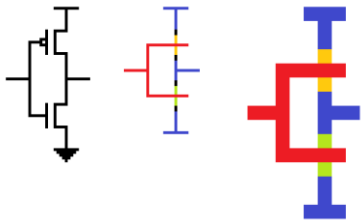
Submit your project due to 27.11.2020 17:00.

3.3.Grading

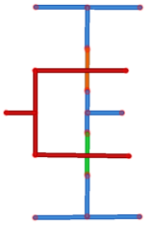
You will be graded over 100 points.

4.WHAT DID I DO?

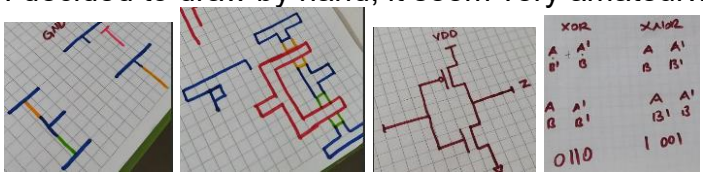
- ✓ I prepared a beautiful user manual for my library, in this manual, all work is by me, I will add sources where I used when I study, but I draw myself all of them. Only Magic layout screenshots are not from me, they are from another library, I used them for visual beauty, when I draw my own layouts, I will change them with mine's.
- ✓ I tried before drawing in paint, it was very hard…



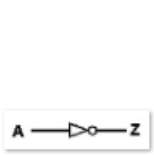
- ✓ Then I tried using fritzing tool to draw wires, but it was very bad experience…



- ✓ I decided to draw by hand, it seem very amateur…

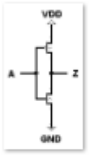


- ✓ I finally decided to draw gate and transistor level design in Logisim, and stick diagram in Paint. They looks awesome.



1_INV_GL.png

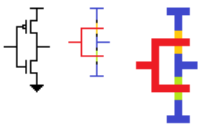
1_INV_SD.png

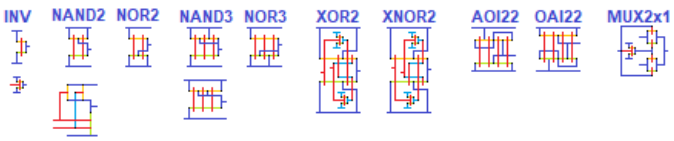


1_INV_TS.png

A	Z
0	1
1	0

1_INV_TT.png





- I will add my Logisim file and Paint file to my submission folder.

- And follows are websites I used :

Sources :

1. http://www.ece.iit.edu/~eoruklu/courses/ece429/tutorial/magic.html
2. http://opencircuitdesign.com/magic/tutorials/tut1.html
3. http://terpconnect.umd.edu/~newcomb/vlsi/magic_tut/Magic_x3.pdf
4. http://esaki.ee.boun.edu.tr/courses/ee537/magic-tut.pdf
5. https://tams.informatik.uni-hamburg.de/applets/hades/webdemos/05-switched/40-cmos/aoi22.html
6. https://www.slideshare.net/kalyanacharjya/stick-diagram
7. https://studylib.net/doc/7514853/aoi-22-design
8. https://vlsicad.ucsd.edu/
9. http://students.ceid.upatras.gr/~gef/projects/vlsi/ask2/
10. http://www.cs.unca.edu/~brock/classes/Fall2012/csci255/lectures.shtml
11. http://www.elec.canterbury.ac.nz/intranet/courses/435/bim/lab1.html
12. http://yasinkavak.blogspot.com/2015/07/cmos-transistor-designs-with-magic-vlsi.html
13. https://www.acsce.edu.in/acsce/wp-content/uploads/2020/03/VLSI-Module-3.pdf
14. http://www.vlsi-expert.com/2014/11/cmos-layout-design.html

- **Note In Turkish :** Bu sayfalardan hiçbir şey birebir alınmamıştır, sadece doğru ilerlemek adına kontrol ettiğim şeyler oldu, örneğin stick diagramda renkler için bir slaytı hep açık tuttum, veya AOI22 cell'I için ortayı nasıl parallel yapmam gerektiğini kendim bulamadım, sayfalardan baktım, bazı sayfalarda direk çizili örnekleri varmış gibi duruyor, onlar L-Edit'te PSpice'taki çalışmalar, bir de bazen doğru yaptığımı düşündüğüm halde çalışmayan kısımlar oldu, örneğin diğer ödevde bazı yerlere ne malzeme koymam gerektiğini bilmiyordum, transistor olduğunu biliyordum, birçok video izledim hem çalışmak için hem de hangi malzemeyi nasıl koyuyor öğrenmek için, tam öğrenememiştim o zaman, bu ödevde şunu öğrendim, polysilicon ile diffusionların üst üste geldiği yerde transistor oluşur. Faydalandığım kısımlar ancak ve ancak bu gibi kısımlar, kaynak eklediğim için açıklama yapmaktayım. Manual'I ayrı hazırladım, informal bir şekilde de bu raporu ayrı hazırladım. Çizimleri önce halledersem layoutlar hemen biter diye düşündüm, çizimlerde en son gözlerim çizgileri seçemez haldeydi, çok vaktimi aldı ve layoutlara geç başlamış oldum, yetişmeyecek olursa diye bir library'den layout görüntülerini ekran alıp linkleriyle koydum, manualin son halini gözümde canlandırabilmek adına, diğer tüm kısımlar bana aittir, layoutları çizdikçe hem dosyalarını hem ekran görüntülerini ekleyip düzenliyorum. (v1, saat 11:44)

- **Addition :** INV NAND2 NAND3 NOR2 NOR3 devreleri eklenmiştir. (v2, saat 00:05)

5.WHAT DID NOT I DO?

- I did not draw layouts of XOR XNOR AOI22 OAI22 MUX2x1,
  I took screenshots from another library, known as “Nangate”, from “Silvaco”.
- I will draw, but if I can catch up. I spend my time on other designs, transistor and stick diagram. I thought if I finish before them, I can be faster drawing layouts, but my time is end up.

END OF THE REPORT

UPDATED : Nov 28, 2020 Saturday 00:05

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