CELL LIBRARY MANUAL

CMOS VLSI – MAGIC LAYOUT - NGSPICE SIMULATOR

Gebze Technical University, Faculty of Engineering, Department of Computer Engineering
CSE 436/536 – Integrated Circuit Design (Fall 2020, Covid-19 Pandemic)

Assignment 3 – Cell Library (v1)

Lecturer : Alp Arslan Bayrakçi
Student : Şeyda Nur DEMİR
ID : 12 10 44 042

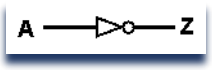
" This report studies the design of
INV, NAND2, NAND3, NOR2, NOR3, XOR2, XOR3, AOI22, OAI22, MUX2x1 cells.
It shows the gate level design, De'morgan analysis Boolean Expression, the truth table,
the transistor level schematic design, the stick diagram,
drawn layout using Magic Layout and the output signals simulated by NGSpice. "

INVERTER DESIGN

Introduction

This report studies the design of INV function.

Gate Level Design



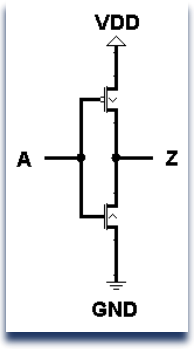
De'Morgan Analysis Boolean Expression

Z = (A)'

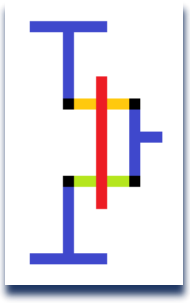
The Truth Table

A	Z
0	1
1	0

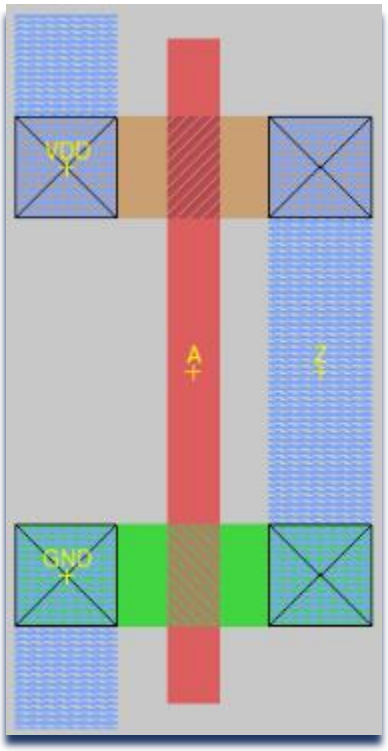
Transistor Level Schematic Design



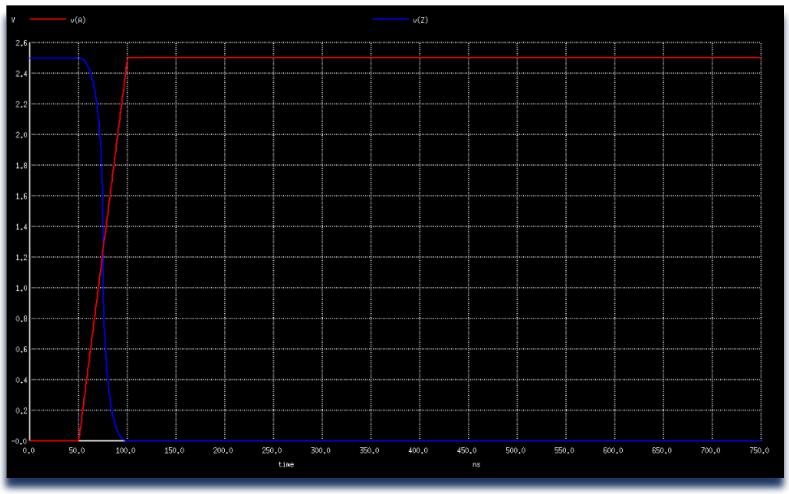
Stick Diagram



Layout (Magic)



Plot (NGSpice)

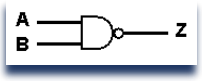


NAND2 DESIGN

Introduction

This report studies the design of NAND2 (2-INPUT NAND) function.

Gate Level Design



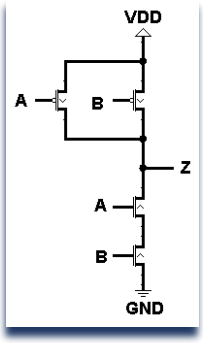
De'Morgan Analysis Boolean Expression

Z = (A.B)'

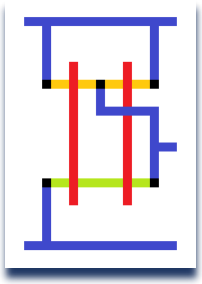
The Truth Table

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Transistor Level Schematic Design



Stick Diagram



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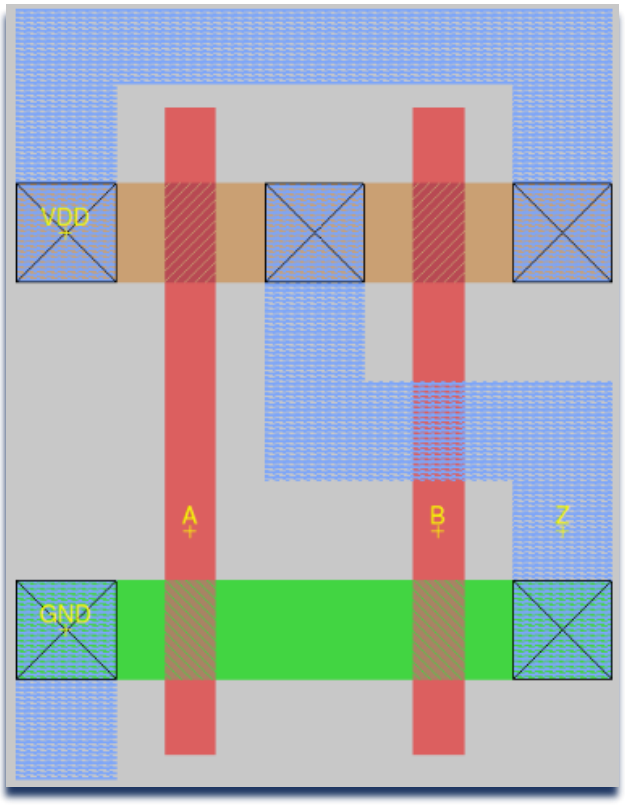
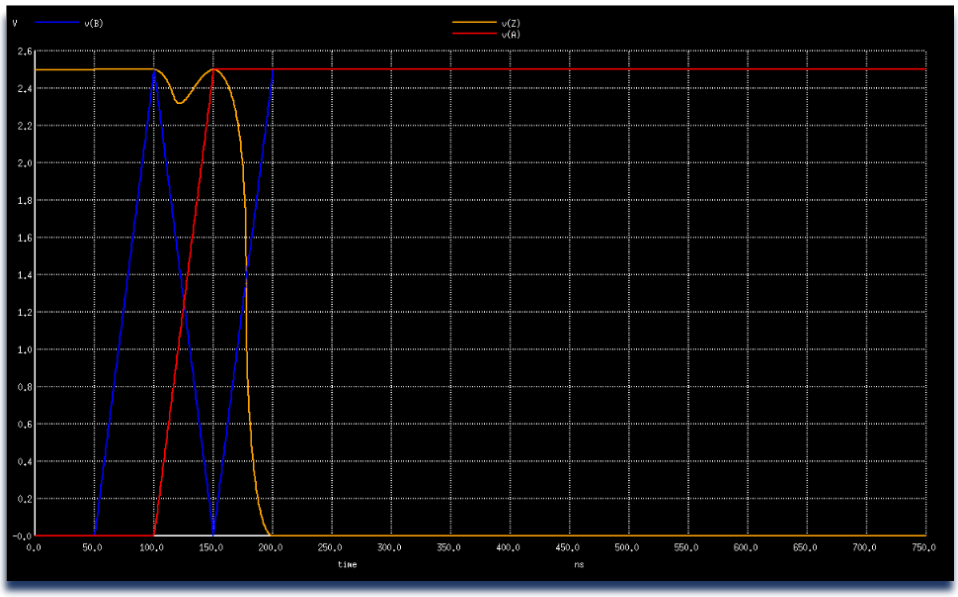


Plot (NGSpice)



NAND3 DESIGN

Introduction

This report studies the design of NAND3 (3-INPUT NAND) function.

Gate Level Design

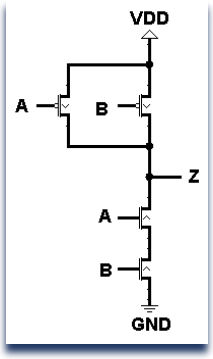
De'Morgan Analysis Boolean Expression

Z = (A.B.C)'

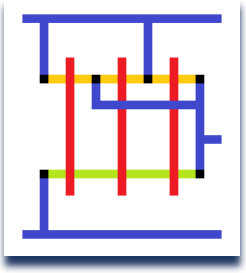
The Truth Table

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

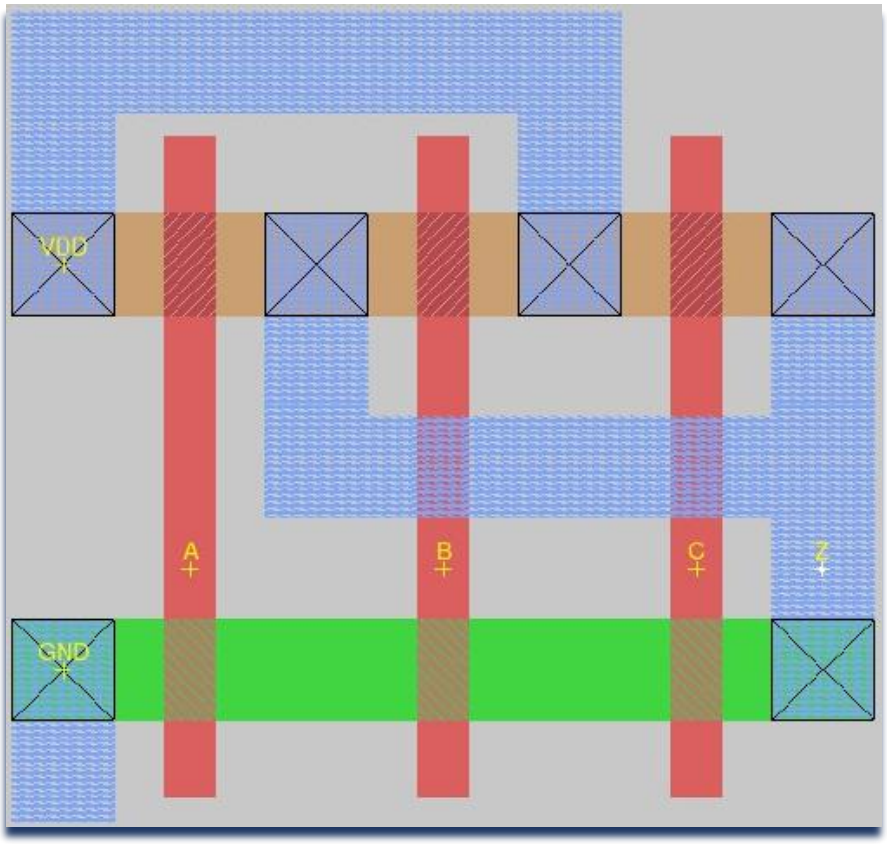
Transistor Level Schematic Design



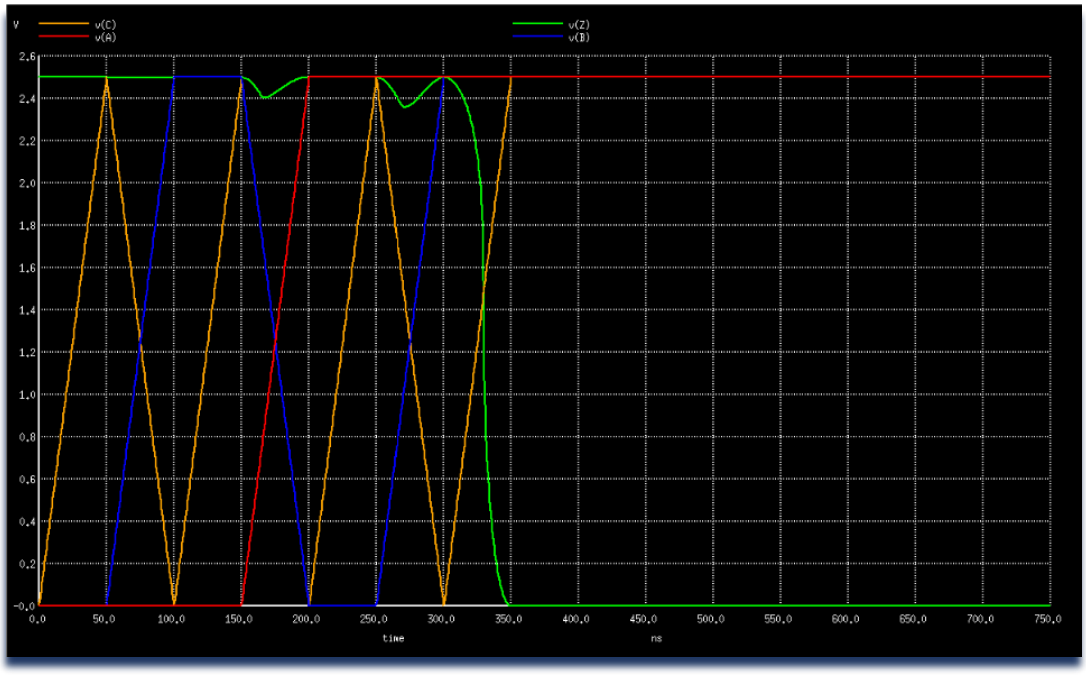
Stick Diagram



Layout (Magic)



Plot (NGSpice)

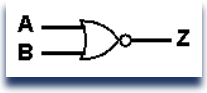


NOR2 DESIGN

Introduction

This report studies the design of NOR2 (2-INPUT NOR) function.

Gate Level Design



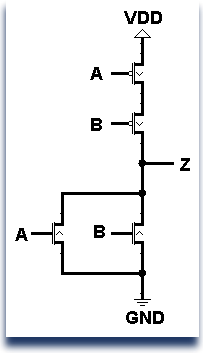
De'Morgan Analysis Boolean Expression

Z = (A+B)'

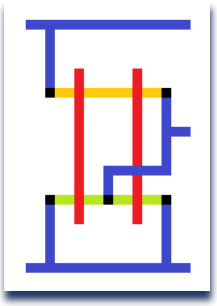
The Truth Table

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

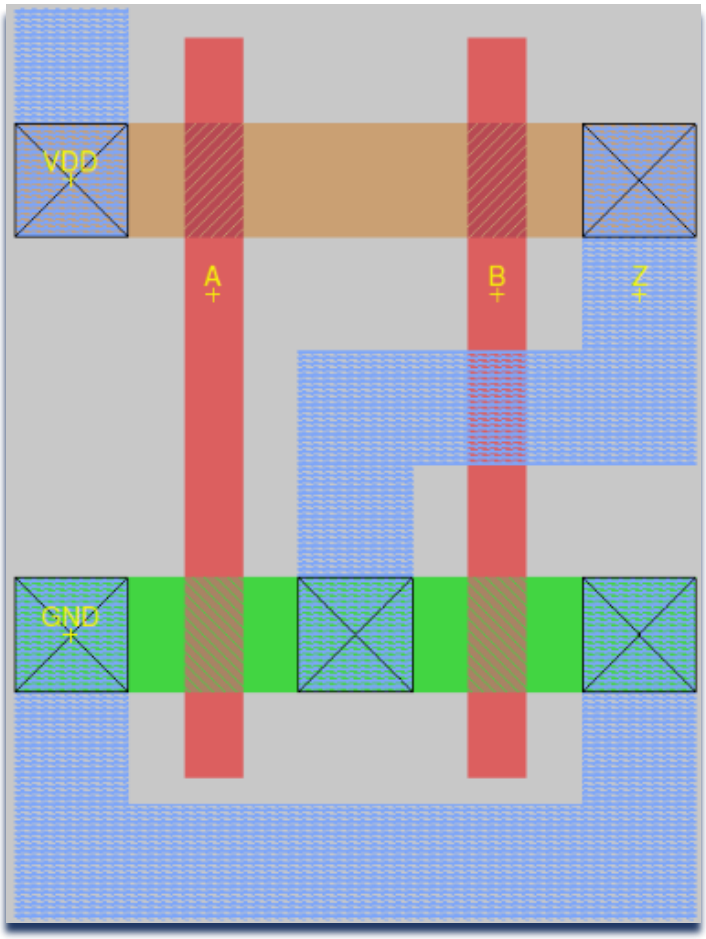
Transistor Level Schematic Design



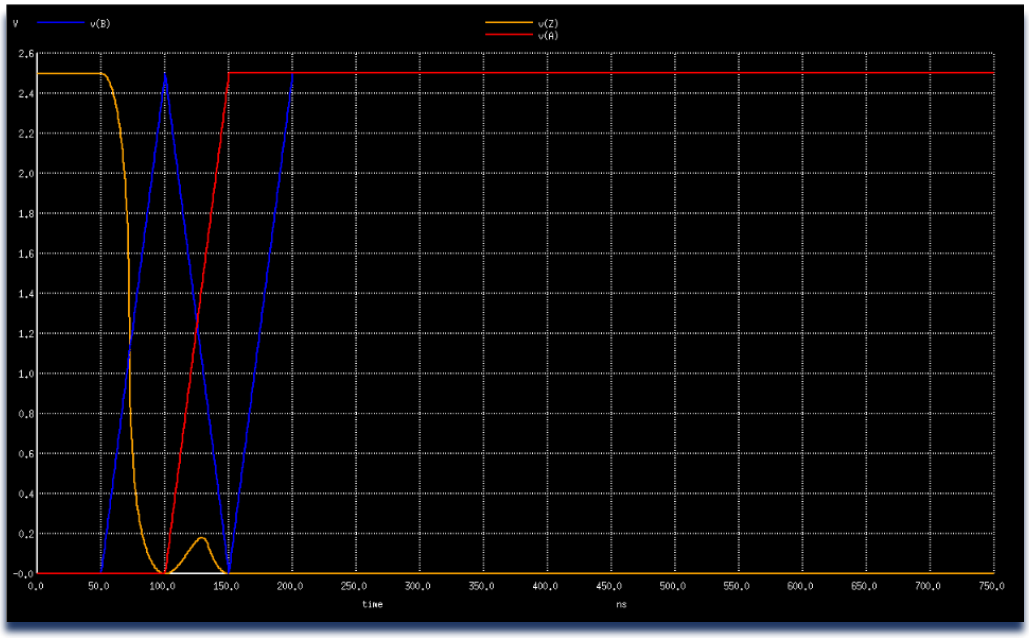
Stick Diagram



Layout (Magic)



Plot (NGSpice)



NOR3 DESIGN

Introduction

This report studies the design of NOR3 (3-INPUT NOR) function.

Gate Level Design

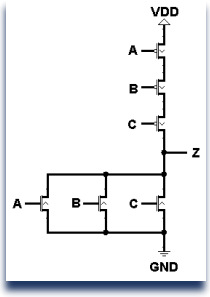
De'Morgan Analysis Boolean Expression

Z = (A+B+C)'

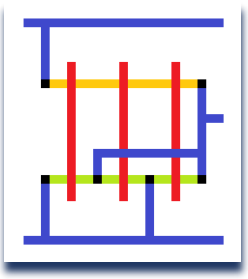
The Truth Table

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

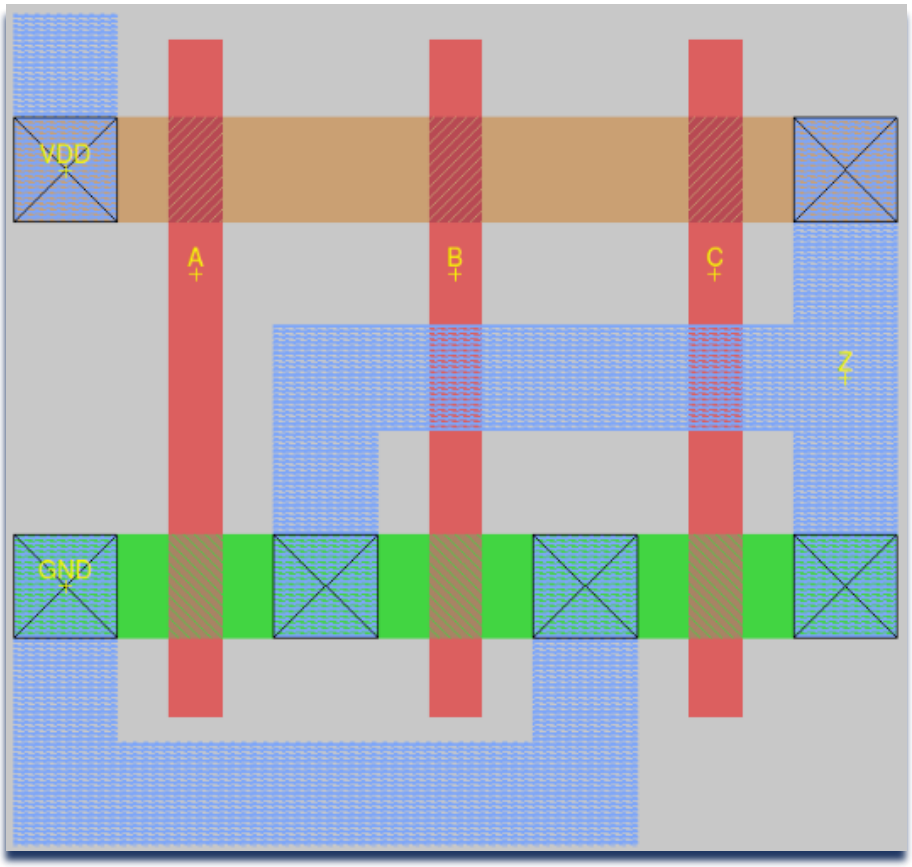
Transistor Level Schematic Design



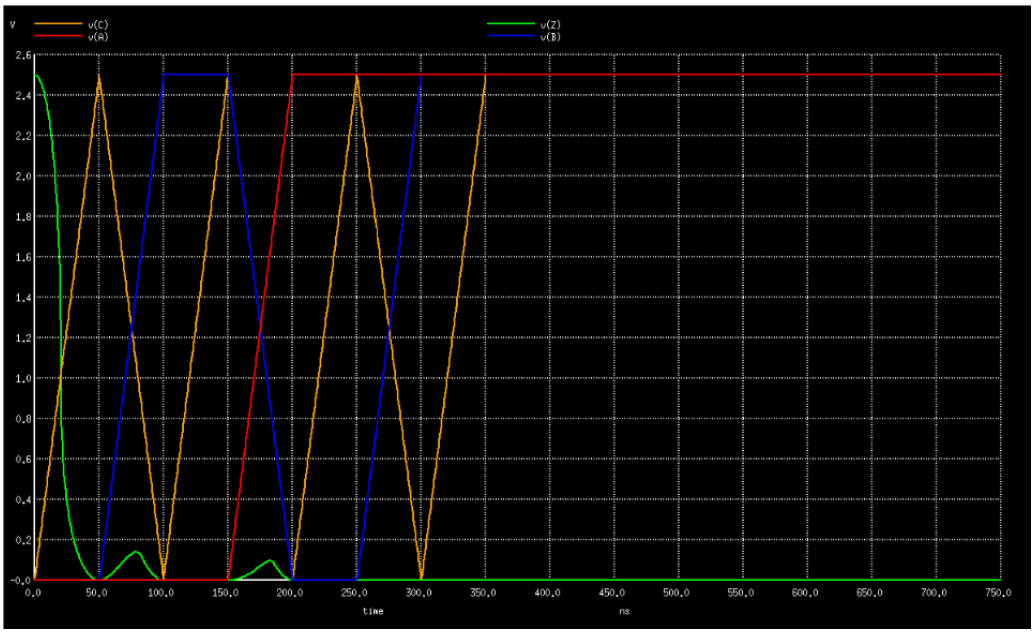
Stick Diagram



Layout (Magic)



Plot (NGSpice)



XOR2 DESIGN

Introduction

This report studies the design of XOR2 (2-INPUT XOR) function.

Gate Level Design

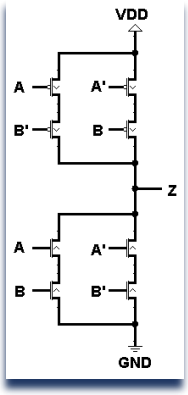
De'Morgan Analysis Boolean Expression

Z = ((A.B')+(A'.B))

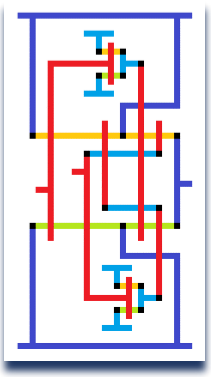
The Truth Table

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

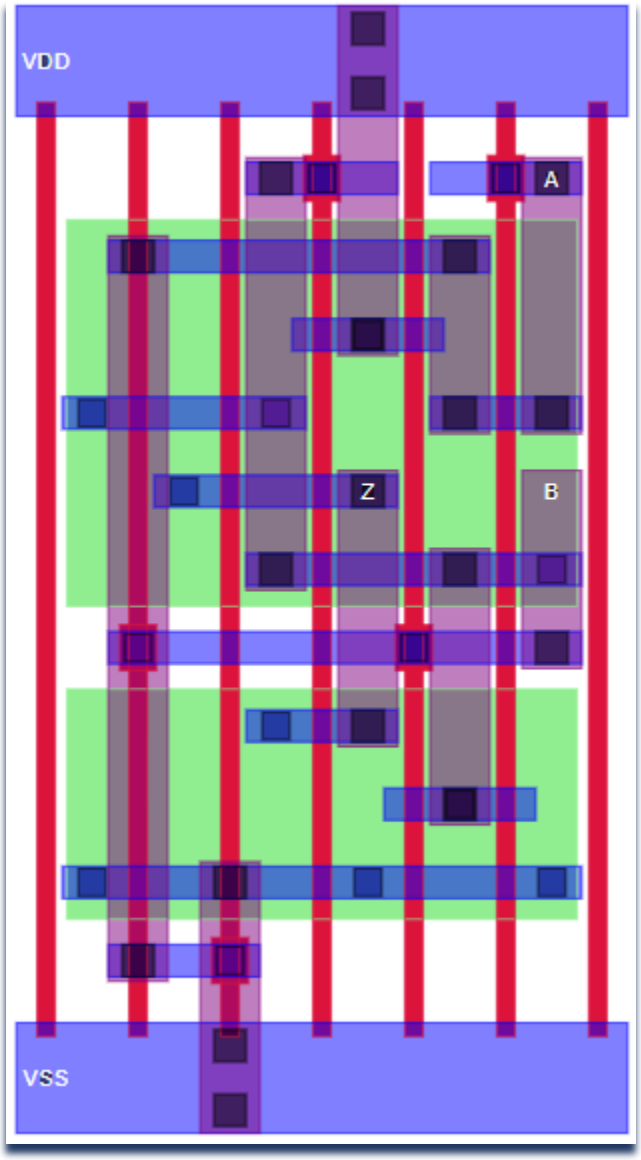
Transistor Level Schematic Design



Stick Diagram



Layout (Magic)



Follow this link, https://www.cs.upc.edu/~jpetit/CellRouting/fig/XOR2_X1_1h.svg

XNOR2 DESIGN

Introduction

This report studies the design of XNOR2 (2-INPUT XNOR) function.

Gate Level Design

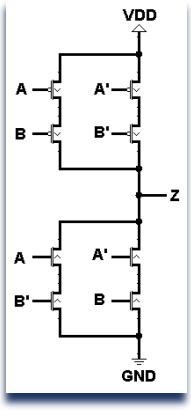
De'Morgan Analysis Boolean Expression

Z = ((A.B)+(A'.B'))

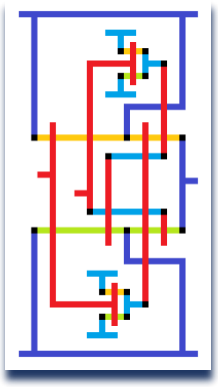
The Truth Table

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

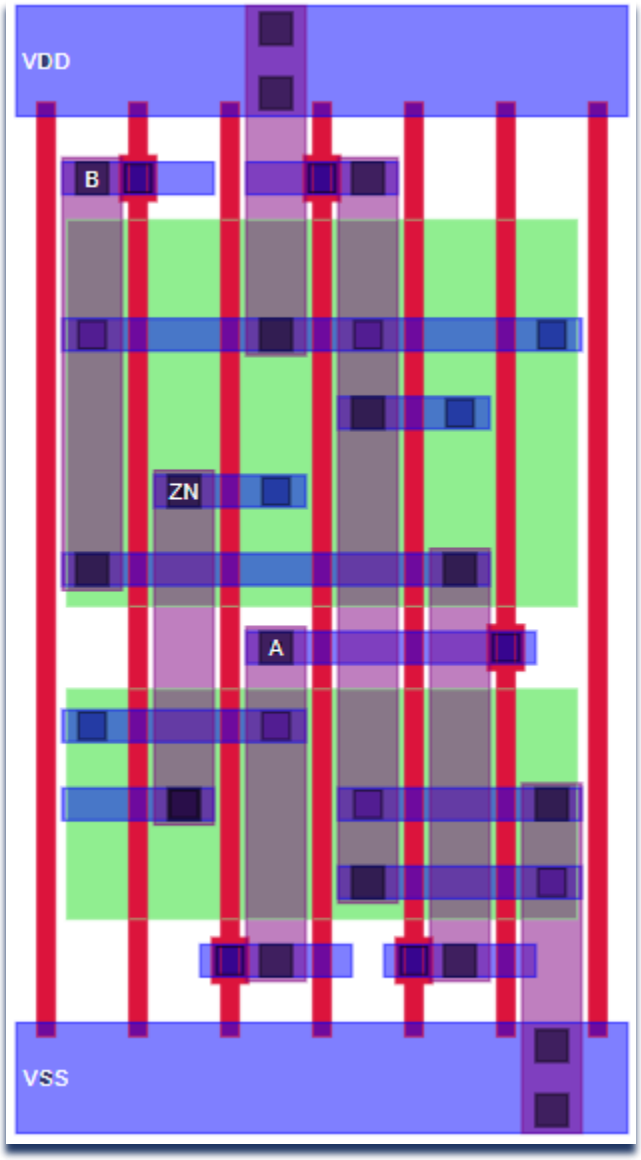
Transistor Level Schematic Design



Stick Diagram



Layout (Magic)



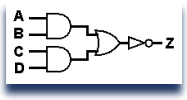
Follow this link, https://www.cs.upc.edu/~jpetit/CellRouting/fig/XNOR2_X1_1h.svg

AOI22 DESIGN

Introduction

This report studies the design of AOI22 (4-INPUT AOI22 CELL) function.

Gate Level Design



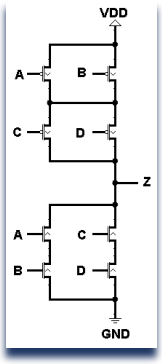
De'Morgan Analysis Boolean Expression

Z = ((A.B)+(C.D))'

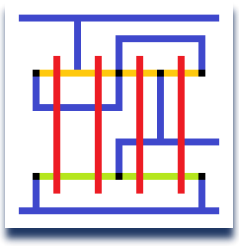
The Truth Table

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Transistor Level Schematic Design



Stick Diagram



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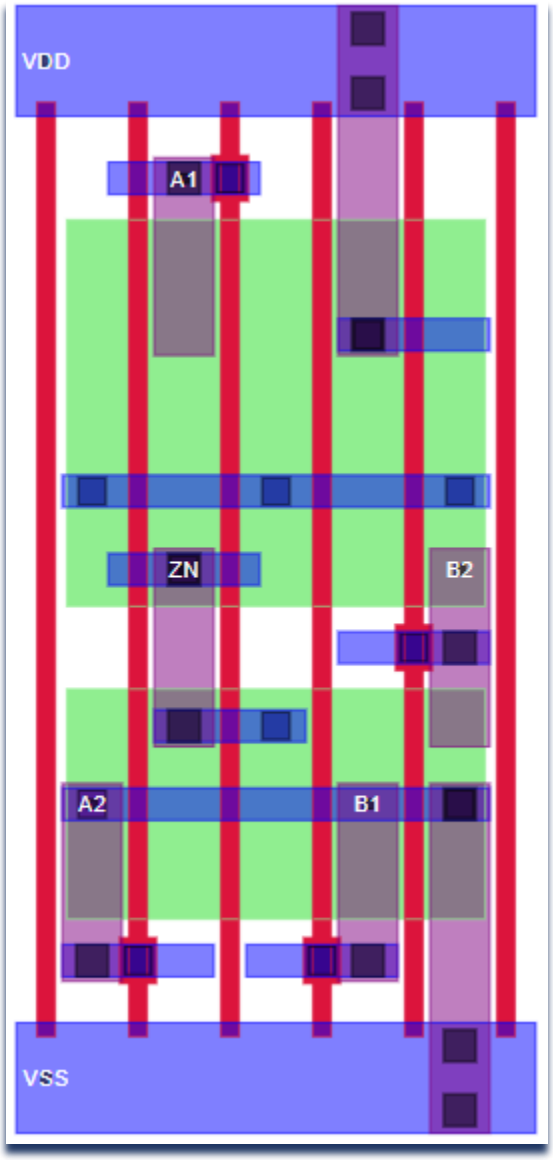


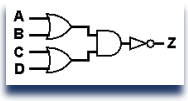
Follow this link; https://www.cs.upc.edu/~jpetit/CellRouting/fig/AOI22_X1_1h.svg

OAI22 DESIGN

Introduction

This report studies the design of OAI22 (4-INPUT OAI22 CELL) function.

Gate Level Design



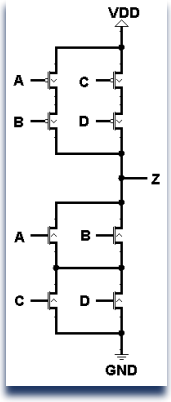
De'Morgan Analysis Boolean Expression

Z = ((A+B).(C+D))'

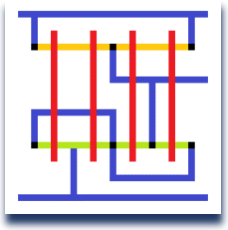
The Truth Table

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

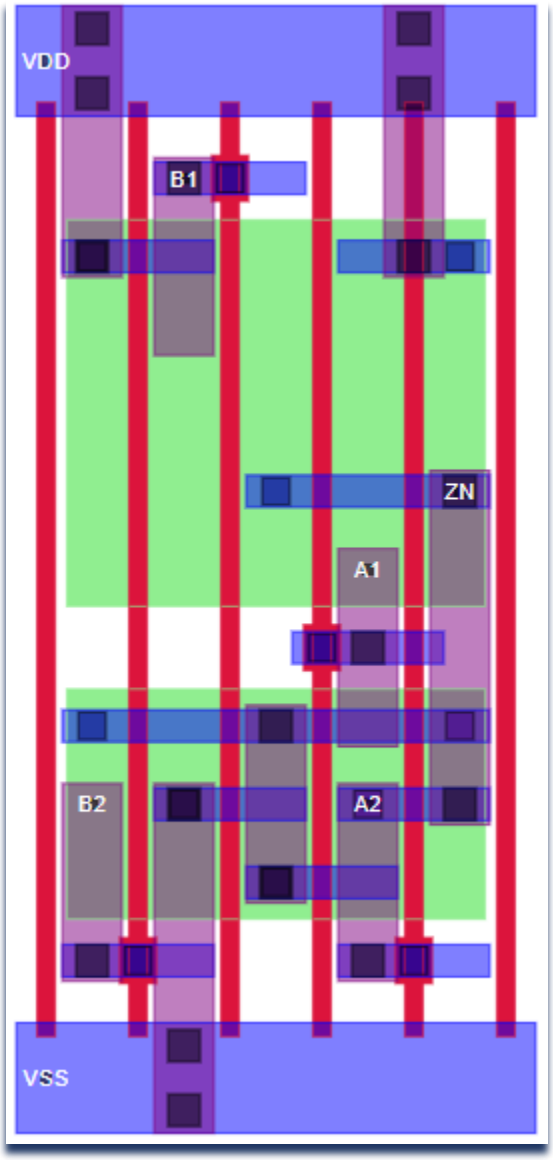
Transistor Level Schematic Design



Stick Diagram



Layout (Magic)



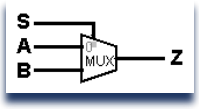
Follow this link, https://www.cs.upc.edu/~jpetit/CellRouting/fig/OAI22_X1_1h.svg

MUX2x1 DESIGN

Introduction

This report studies the design of MUX2x1 (2-INPUT 1-SELECT BIT MUX) function.

Gate Level Design



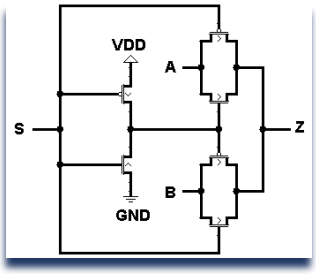
De'Morgan Analysis Boolean Expression

Z = ((A.S')+(B.S))

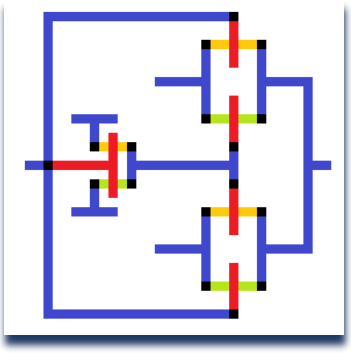
The Truth Table

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

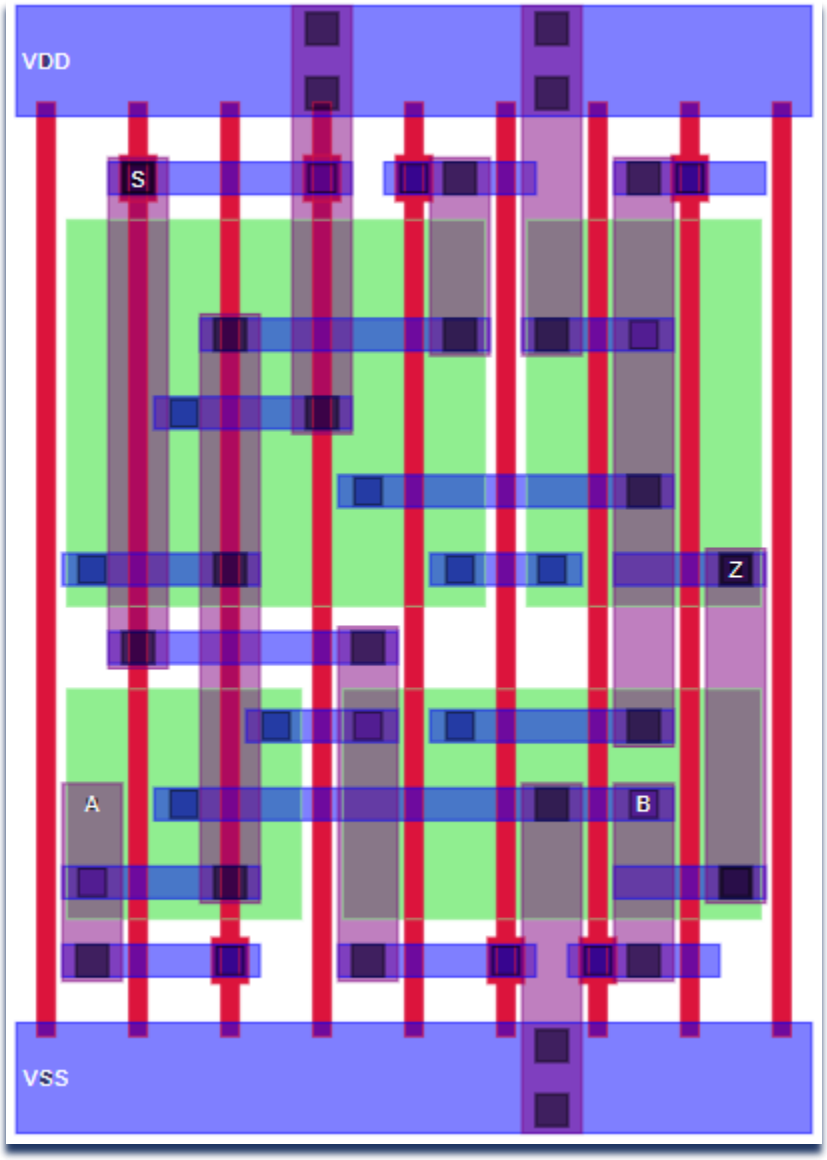
Transistor Level Schematic Design



Stick Diagram



Layout (Magic)



Follow this link, https://www.cs.upc.edu/~jpetit/CellRouting/fig/MUX2_X1_1h.svg

END of the MANUAL.

Any question, **email : sncakar@gtu.edu.tr**

(Last Update : 27/11/2020 10:50)