T.R.
GEBZE TECHNICAL UNIVERSITY
FACULTY of ENGINEERING
DEPARTMENT of COMPUTER ENGINEERING

2-bit CARRY RIPPLE ADDER

CSE 436/536 DIGITAL INTEGRATED CIRCUITS
ASSIGNMENT 4 REPORT

STUDENT
Şeyda Nur DEMİR
12 10 44 042

LECTURER
Alp Arslan BAYRAKÇI

TEACHING ASSISTANT
-

KOCAELİ, 2020

1.DESCRIPTION

Due Date 21/12/2020 17:00

- ✓ In this assignment, using Magic Layout Tool and the 0.25um cell library you designed in your previous assignment; you will design a two bit carry ripple adder.
- ✓ Then you will verify its functionality using Spice Tool.
- ✓ Use as few Metal layers as possible.
- ✓ It is a competition; thus the smallest area working design will be the winner.
- ✓ Find the worst delay (critical) path in your design and measure its delay using Spice transient analysis.
- ✓ Prepare a report as a manual for your library. In the report:
  1. Show the stick diagram for the 2-bit adder.
  2. Put a magic layout pic of your design.
  3. Report width and height of your design in lambdas.
  4. Report the critical path and its worst case delay.
  5. Put the Spice simulation plots showing the functionality of your design.
- ✓ Put your report, your magic layouts (.mag files), your spice extracted circuit decks (.cir files) into a zip file. Name your zip file as:
  StudentName_StudentSurname_StudentId_Assignment4.zip
  Be careful in naming conventions. Otherwise you lose 10 points.

2.WHAT DID I DO?

- ✓ I wrote boolean equations, designed circuit, drew stick diagram, calculate critical path, but I could not do them in magic layout, if I have time, I will do it similar with stick diagram. I may realize all gates with nand gate, and I may use hierarchical layout feature of magic, I worked “getcell, load, array, flush (tut4)”, I know how I will do this, also I changed my gates to use them properly in my design, but I could not complete my homework on time, I was very bad situation for me, I was full this week.

3.WHAT DID NOT I DO?

- ✓ I could not complete my homework on time, magic layout is missed.

2-bit Carry Ripple Adder Boolean Equations :

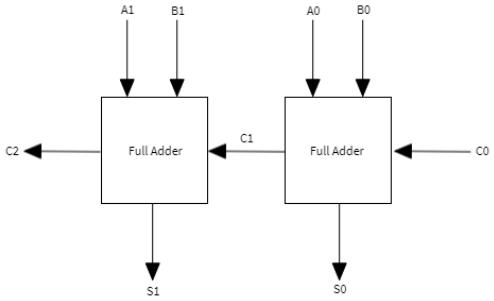
Designed with 2 “1-bit Full Adder”

Full Adder Boolean Equations :

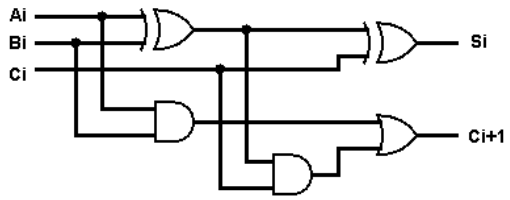
$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = (A_i \,.\, B_i) + C_i \,.\, (A_i \oplus B_i)$

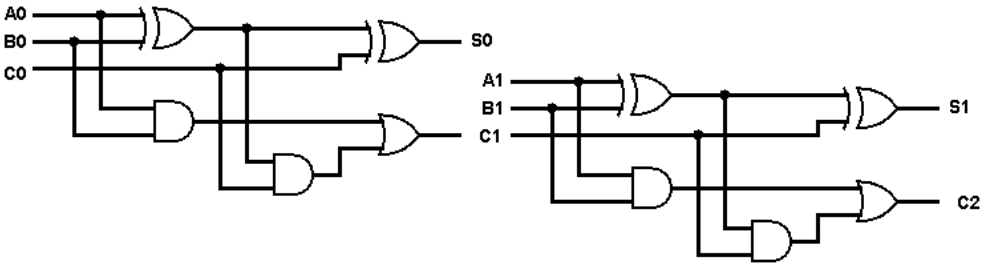
2-bit Carry Ripple Adder Design with Full Adders :



Full Adder Design with Logic Gates :



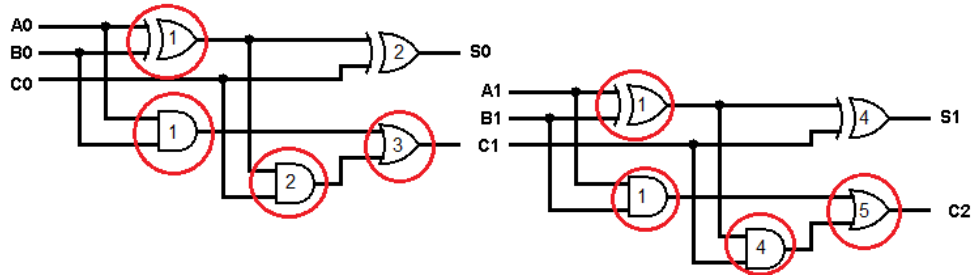
2-bit Carry Ripple Adder Design with Logic Gates :



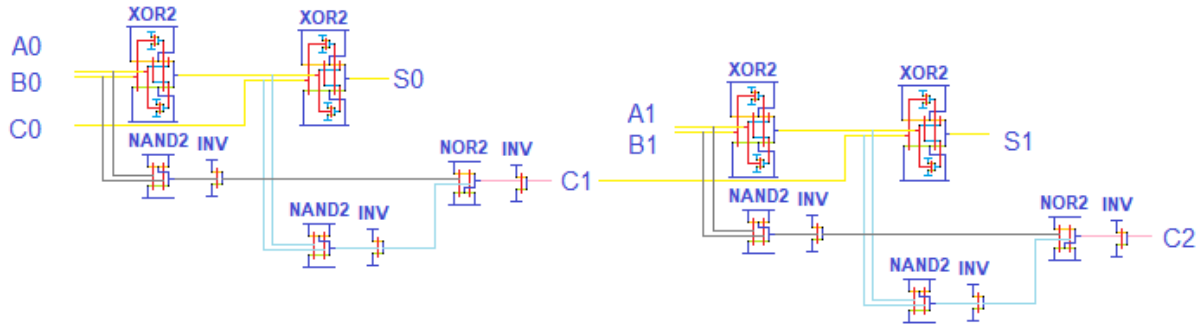
Critical Path is Marked :

Computation of C2, last Cout, is critical path.

It takes **[(*max*(t_{xor},t_{and}) = t_{xor}) + t_{and} + t_{or} + t_{and} + t_{or}]** times delay.



2-bit Carry Ripple Adder Stick Diagram (would be something like this) :



Then, Critical Path would be so in our Layout :

- ✓ Nand2+Inv instead of And gate
- ✓ Nor2+Inv instead of Or gate

It takes **[(max(t_{xor},t_{nand}+t_{inv}) = t_{xor}) + t_{nand} + t_{inv} + t_{nor} + t_{inv} + t_{nand} + t_{inv} + t_{nor} + t_{inv}]** times delay.

Its worst case delay realize on this situation : A0 : 1 A1 : 1 B0 : 1 B1 : 1

(Our 2-bit numbers are 11 and 11, and addition overflows, and C2 calculation time reaches max time, it is worst case delay.)

END OF THE REPORT

UPDATED : Dec 21, 2020 Monday 15:30

STUDENT
Şeyda Nur DEMİR
12 10 44 042

LECTURER
Alp Arslan BAYRAKÇİ

TEACHING ASSISTANT
-

KOCAELİ, 2020