CSE 436/536

Digital Integrated Circuits

Assignment 4

Due Date 21/12/2020 17:00

In this assignment, using Magic Layout Tool and the 0.25um cell library you designed in your previous assignment; you will design a two bit carry ripple adder.

Then you will verify its functionality using Spice Tool.

- ✓ Use as few Metal layers as possible.
- ✓ It is a competition; thus the smallest area working design will be the winner.
- ✓ Find the worst delay (critical) path in your design and measure its delay using Spice transient analysis.
- ✓ Prepare a report as a manual for your library. In the report:
    1. Show the stick diagram for the 2-bit adder.
    2. Put a magic layout pic of your design.
    3. Report width and height of your design in lambdas.
    4. Report the critical path and its worst case delay.
    5. Put the Spice simulation plots showing the functionality of your design.

- ✓ Put your report, your magic layouts (.mag files), your spice extracted circuit decks (.cir files) into a zip file. Name your zip file as:

  StudentName_StudentSurname_StudentId_Assignment4.zip

Be careful in naming conventions. Otherwise you lose 10 points.