CSE 436/536

Digital Integrated Circuits

Assignment 5

Due Date 22/01/2021 23:59

In this assignment, using Magic Layout Tool and the 0.25um cell library you designed in your previous assignment; you will design a four state Finite State Machine. For that purpose you need to design two D flip flops first to hold the state.

Your design will recognize the incoming “10” bit sequence. If the incoming bits are “10” it will output “1” other wise it will output a “0”. The incoming data is much slower than the clock of your circuit. Therefore a signal called ***s*** will give a one cycle pulse when a new bit arrives to the circuit. The ***in*** signal represents the incoming bit. The ***out*** signal is the 1 bit output of your circuit. Also there must be a clock input ***clk***.

Prove that your circuit works well using Spice.

Compute the delay of your circuit and the fastest clock that you can run your circuit. This is a competition again.

You will show all your results with a demo. Prepare for the demo to get better grades.