CSE 436/536

Digital Integrated Circuits

Assignment 3

Due Date 27/11/2020 17:00

In this assignment, using Magic Layout Tool you will design a 0.25um TSMC process standard cell library including:

- INV
- NAND2
- NAND3
- NOR2
- NOR3
- XOR2
- XNOR2
- AOI22
- OAI22
- MUX2x1

✓ Use as few Metal layers as possible.
✓ All transistor must be at 2 lambda gate length.
✓ The cells must be at same height.
✓ The cells must as shrinked as possible.
✓ Extract each cell in Magic and simulate in Spice to verify the functionality. Test all possible inputs for each cell.
✓ Prepare a report as a manual for your library. In the report:
   1. Show the stick diagram for each cell.
   2. Put a small magic layout picture of each cell
   3. Put the transistor level schematic of each cell.
   4. Pus the Spice simulation plots showing the functionality of each cell.
   5. Write down the size of each cell in lambdas.
✓ Put your report, your magic layouts (.mag files), your spice extracted circuit decks (.cir files) into a zip file. Name your zip file as:

   StudentName_StudentSurname_StudentId_Assignment3.zip

Be careful in naming conventions. Otherwise you lose 10 points.