MCU_Envi

Fichier: untitled.kicad_sch

Power Leg 1

Fichier: PowerLeg1.kicad_sch

Power_mesures_adaptation

Fichier: Power_mesures_adaptation.kicad_sch

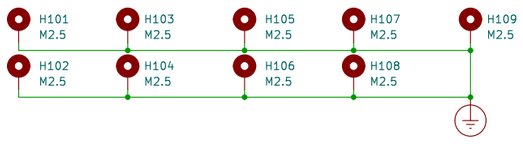
Feeder

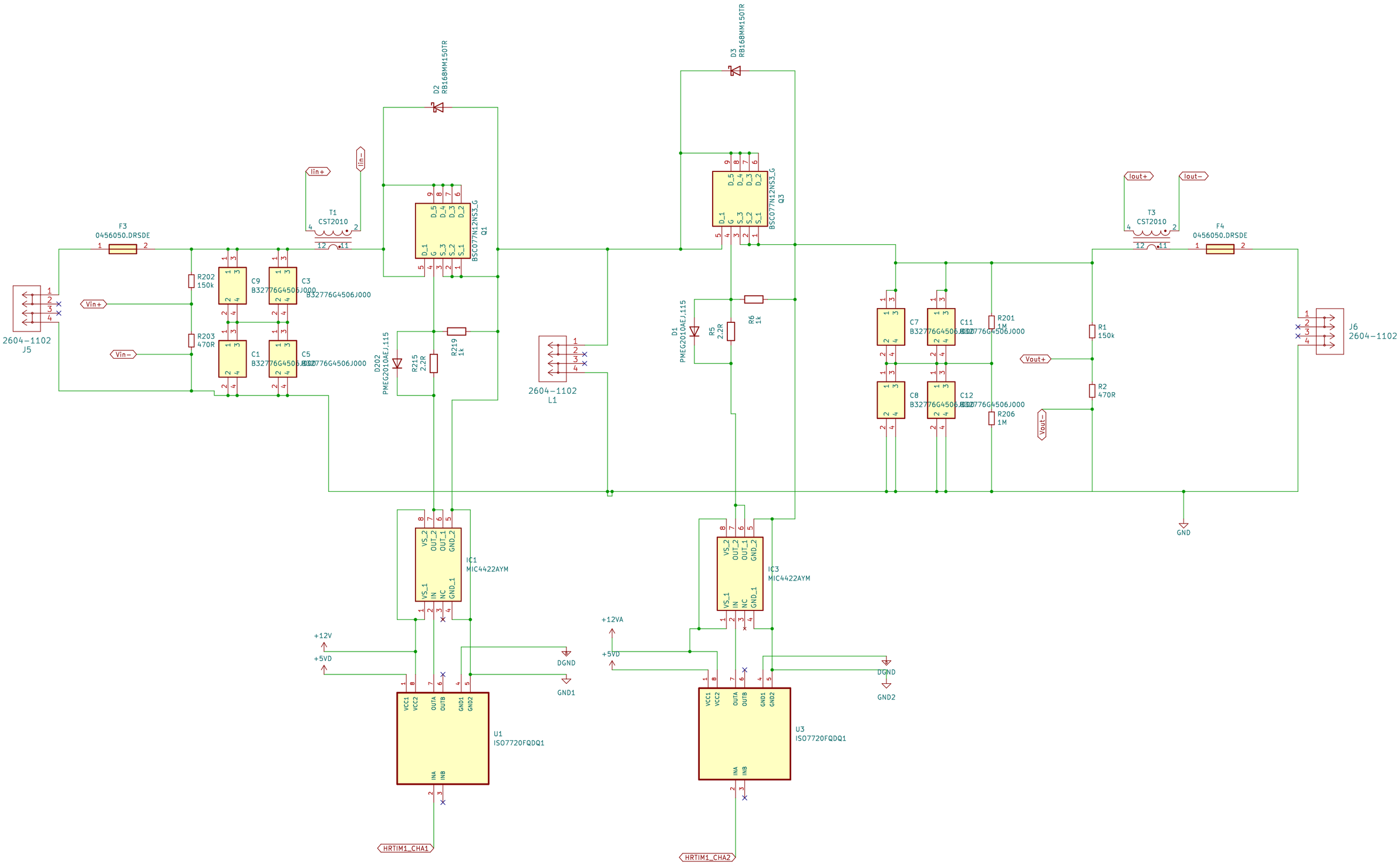
Fichier: Feeder.kicad_sch

https://www.falstad.com/circuit/circuitjs.html

All ceramic capacitor X7R 50V unless specified
All resistor to be thin film 1/8Watt unless specified

Mechanical housing
and heatsink holes




D2
RB168MM150TR
D3
RB168MM150TR
Iin+
Iin−
T1
CST2010
F3
0456050.DRSDE
Q1
BSC077N12NS3_G
Q3
BSC077N12NS3_G
Iout+
Iout−
T3
CST2010
F4
0456050.DRSDE
J5
2604−1102
Vin+
Vin−
R202
150k
R203
470R
C9
B32776G4506J000
C3
B32776G4506J000
C1
B32776G4506J000
C5
B32776G4506J000
D202
PMEG2010AEJ,115
R215
2.2R
R219
1k
L1
2604−1102
D1
PMEG2010AEJ,115
R5
2.2R
R6
1k
C7
B32776G4506J000
C11
B32776G4506J000
C8
B32776G4506J000
C12
B32776G4506J000
R201
1M
R206
1M
R1
150k
R2
470R
Vout+
Vout−
J6
2604−1102
GND
IC1
MIC4422AYM
+12V
+5VD
DGND
GND1
U1
ISO7720FQDQ1
HRTIM1_CHA1
IC3
MIC4422AYM
+12VA
+5VD
DGND
GND2
U3
ISO7720FQDQ1
HRTIM1_CHA2

Jumper that permits
to isolate the feeder supply
if faulty

Input 10-110V
@600mA max

VIN
JP501
L502
10uH
input

C519 470nF
C520 470nF
C517 4.7uF
C518 4.7uF
C501 4.7uF
C502 4.7uF
HV
HV

R501 147K
R502 14,7K

GND

Added inductor
and extra capacitors
for the input filter
as per application note

UVLO is the feeder
start-up threshold.
Configured for 9,7V
start-up.

Once started it will
operate for any VIN
higher than 8,9V

D5 is the
overvoltage
protection
that sense
the Aux voltage
NTC1 is the over
temperature
protection

Do not populate
these parts for
initial testing.
As Fault pin is
not necessary at
first

VAUX
D501 6.2V

C503 10nF
NTC501 100kNTC
C504 22nF
R503 100k
C505 1nF

22nF means
~20ms soft start

100k means
100kHz switching
frequency

U501
NCP12700
UVLO
FLT
SS
RT
COMP
VIN
DRV
CS
VCC
GND

C508 100nF 250V

Snubber circuit
As per Application
Note DN05109-D

R509 348k
C510 6.8nF 630V
D503 BAS20HT1G
D504 SURA8140T3G

R505 2.2R
R507 10R
R508 10k
Q502 TK13P25D,RQ
R506 470R
C511 100pF 1kV
MOSD
MOSS

C506 100pF C0G
R510 240m
R9 is the current
sensing resistor.
240m should give
Ipeak ~2A

VBoost
D502 BAS20HT1G
L501 100uH
VAUX
R511 10R
D505 BAS20HT1G
D506 BAS20HT1G
Q501
R504 1.4k
C507 1uF
C509 1uF
R512 1.4k

C512 2.2nF 2.5kV
C513 2.2nF 2.5kV
DGND

C514 1nF 500V
10R 1W
R513
D507 STTH4R02U
C515 10uF
GND2

T501
PA2467NL
37uH

ISat for PA2467NL
is about 2.85A

+6VJP
+6V
C521 100uF
J505
Header_2_54_01x03

Jumper that permits
to isolate the feeder if needed
External supply can provide +6V from pin 2 and 3

R516 10R

Type 2 Isolated feedback network with TL431
As per Application note DN05109-D

Explanation
https://www.onsemi.com/pub/Collateral/TND381-D.PDF

R15 is the value to change the output voltage
It should be 27K to stabilize it to 6.05V

TL431 give Vo = 6.05V
with Vo = Vref(1 + R14/R15)
6.05V = 2,5V * (1 + 38,3K/27K)

R514 1.4k
R517 38.3k
R515 10k
C516 6.8nF
U503
TL431MFDT,215
REF
R518 27k

U502
FODM217A

Passive unregulated
boost permits to supply
control IC from auxillary
as output voltage is below 9V

This feeder design is based on a Flyback DCM design largely inspired from Application Note DN05109-D

Targeted SPEC:
11-110V Input
6V Output @ 0.5A
DCM boundary @ 70% max load

External power supply
- 6V
- 100mA

Polyfuse to prevent
over-current in daisy-chained
bus with multiple sources and
sinks.

F501
0ZCH0035FF2G
350mA 1210
PWR_COM1
J501
F502
0ZCH0035FF2G
350mA 1210
PWR_COM2
J502

Low Drop Out
Linear regulator to get
Noise free +5V

U505
AZ1117CH-5.0TRG1
C527 1uF
C529 1uF
R519 1R

Isolated DCDC blocks to have +12V and +5V referenced to GND and +5V referenced to NGND

L503 22uH
C522 10uF
C523 10uF
PS501
TBA 1-0512
C524 10uF
C525 1uF
U504
MCP1799T-5002H/TT
C528 1uF
GND1

L2 22uH
C31 10uF
C32 10uF
PS1
TBA 1-0512
C34 10uF
GND2

PS502
TEA 1-0505
C530 10uF
C526 10uF

Y1
ECS-240-8-37-CKM-TR3 - 24MHz
HSE_IN
HSE_OUT
R9
220
C17
12pF
C18
12pF
GNDD

Decoupling capacitors choosen as per datasheet 5.16 Power supply scheme fig.16
+3.3V
FB1
1000 Ohm @ 100MHz
+3.3VA
C20
4,7uF
C21
100nF
C22
100nF
C23
100nF
C24
100nF
C25
1µF
C26
10nF
VREF2048
C27
1µF
C28
100nF
GNDD

STDC14 / ARM10 connector for debugger connection
Compatible with STLINKV3
STLink
FTSH-107-01-F-DV-K
+3.3V
GNDD
SWDIO
SWCLK
SWO
RST
R10
100
STLINK_RX
STLINK_TX
External debug
alt ref: 20021121-00014T1LF

LED_BUILTIN
JP1
LED
R11
330
PWR
Blue
R12
330
+3.3V
GNDD

Diode to protect Computer from overvoltage
PTC Fuse to protect Computer from VIN short
J3
USB_C_Receptacle_USB2.0
VBUS
D5
F2
+5VD
350mA
CC1
CC2
USB_D-
USB_D+
R13
5.1k
R15
5.1k
USB C configuration channels resistors 5.1k = 500mA max
SHIELD
GND
S1
A1
SBU1
SBU2
U7
WE-TVS-82400102
TVS to protect USB from electrostatic discharges
USB and TVS protection

ADC3_IN12
JP5
Temp2
ADC4_IN5
JP6
Temp
PB1
JP7
HRTIM1_SCOUT
PB6
JP8
HRTIM1_SCIN
HRTIM_SYNC
TP4
TP9
HRTIM_CHA1
TP5
TP10
HRTIM_CHA2
DGND

24Mhz HSE freq is choosen to match NucleoG474RE design.
C3 and C4 are choosen following the rule of thumb :
C3 = C4 = 2*CLoad - 2*CStray
Where CStray is the parasitic capacitance
Guesstimated at 4pF.
+BATT
+3.3V
+3.3VA
VREF2048
NRST
BOOT
PC14
RST
C19
100nF
PC14 is choosen as the bootloader physical GPIO as it has no interesting alternate functions.
I2 is tied to PC1 which is ADC1 CH7 or COMP3 INP (in current mode)
HSE_IN
HSE_OUT
PD2
PC0
PC1
I_out_mcu
V_out_mcu
PC4
PC5
PC6
PC7
PC8
PC9
USART3_TX
USART3_RX
PC10
PC11
PC12
PC13
PC14
PC15
V_in_mcu
I_in_mcu
STLINK_TX
STLINK_RX
LED_BUILTIN
HRTIM1_CHA1
HRTIM1_CHA2
USB_D-
USB_D+
SWDIO
SWCLK
ADC3_IN12
Temp_mcu
SWO
FDCAN1_RX
FDCAN1_TX
USART3_DE
ADC4_IN5
STM32G474RE LQFP64
Pin Mapping
U5
STM32G474RE

+5VD
U10
LTC2850xS8
C36
100nF
DGND
USART3_RX
USART3_DE
USART3_TX
R30
4.7k
R33
4.7k
JP13
JP14
R34
120R
JP15
R35
4.7k
A
B
RS485 Bus

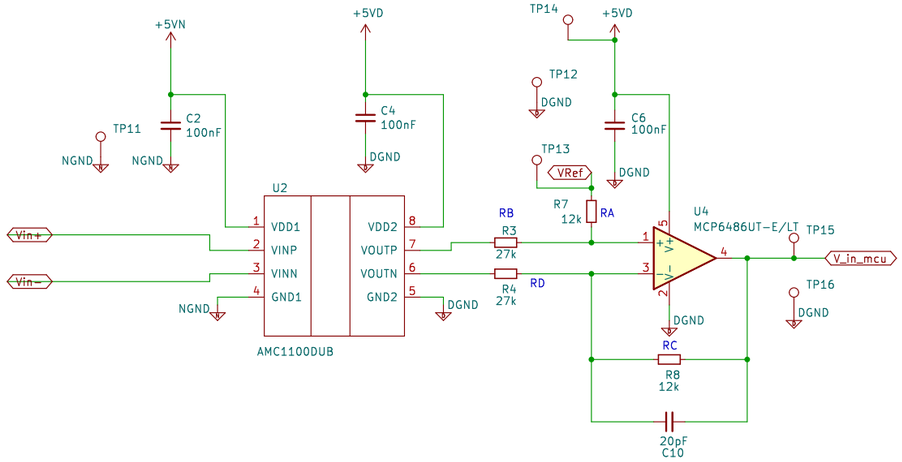
+5VD
F1
350mA
+5VD_Reg
U6
AZ1117-33
+3.3V
C29
10uF
C30
10uF
R14
1R
PTC fuse to protect MCU From a short
Resistor to increase ESR necessary for LDO stability
LDO power supply

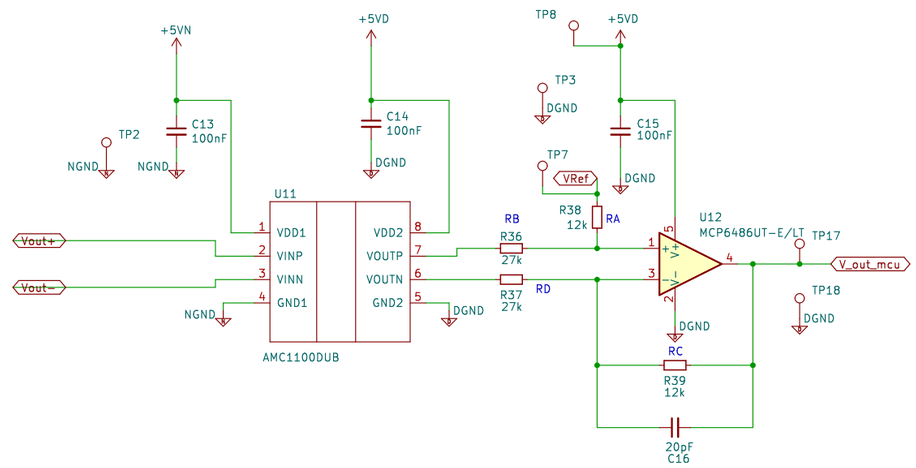
+3.3VA
+BATT
PWR_FLAG
+5VD
+5VD_Reg
GNDD

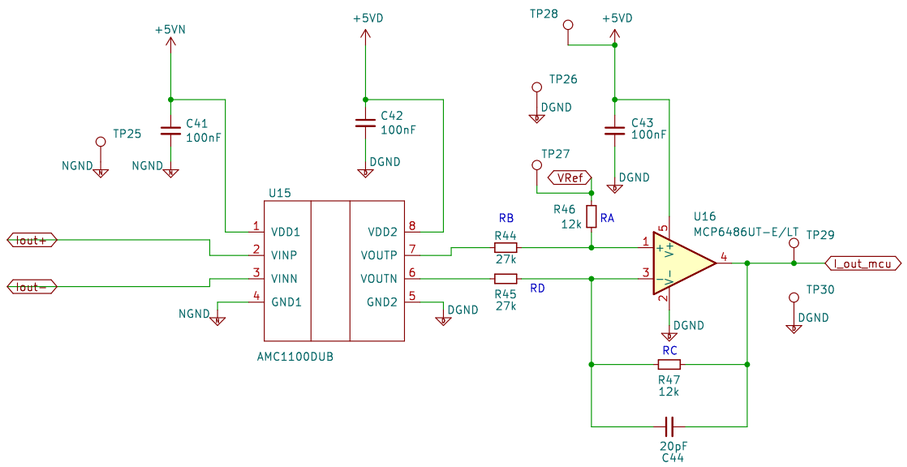
Max current flowing 0.12mA
R0 = 10kOhm
B = 3450
R = R0 * expB(1/T-1/T0)
Temperature sensor is wired to a flexible temp probe attached to the heatsink
+3.3V
R16
20k
R17
20k
Temp
Temp2
TH2
NXFT15XH103FA2B100
TH1
NXFT15XH103FA2B100
DGND

U9
TCAN334GDR
C33
100nF
FDCAN1_TX
FDCAN1_RX
TXD
RXD
SHDN
STB
VCC
GND
CANH
CANL
CAN_H
CAN_L
JP10
R22
120R
CopyLeft LibreSolar
CAN bus

RJE721881411
J1
R26
3k
+6V
R27
330R
HRTIM_SYNC
CAN_L
CAN_H
J4
R31
3k
R32
330R
Board inputs and outputs
Communication link encompasses
- Analog bus
- CAN bus
- HRTIM sync
- RS485 20Mbps bus
Communication RJ45 terminals







Low Side Voltage Measurement

Simulation available
https://tinyurl.com/2enzfg8c

Circuit can be seen as non inverting opamp
with gain : G = 1+(RC/RD) and a potential on non-inverting
input equal to Millman's theorem of :
V+ =((VOUTP-VOUTN)/RB)+(Vref/RA)/((1/RB)+(1/RA))

Measurements are thought for STM32G474RE
with either internal reference set to 2.048V (from VREFBUF register) or equivalent external voltage reference.