Φ dont care

$f(x_1, x_2, x_3, x_4) = U_1(2,4,8,9,13,15) + U_\phi(6,10,12)$

x_1x_3' .... ϕ's are assumed to be 0.

	1	2	3	4	cost
A				x	
B			x		
C		x			
D					

Simplification of General functions

Tabular (Quine-McClusky) Method.

Minterms are combined.
Adjacent minterms combined.
1st Step

x_1	x_2	x_3	x_4	
0	0	0	0	0 ✓
0	0	0	1	1 ✓
0	0	1	0	2 ✓
1	0	0	0	8 ✓
1	0	1	0	10 ✓
1	0	1	1	11
1	1	1	0	14
1	1	1	1	15

cluster them

1

Num	$x_1x_2x_3x_4$
0,1	0 0 0 –
~~0,2~~	0 0 – 0 ✓
0,8	– 0 0 0 ✓
2,10	– 0 1 0 ✓
8,10	1 0 – 0 ✓
10,11	1 0 1 – ✓
10,14	1 – 1 0 ✓
11,15	1 – 1 1 ✓
14,15	1 1 1 – ✓

2

3

Num	$x_1x_2x_3x_4$
0,8,2,10	– 0 – 0
~~0,2,8,10~~	~~– 0 – 0~~
10,11,14,15	1 – 1 –

prime implicant

$\bar{x}_1\bar{x}_2\bar{x}_3$, $\bar{x}_2\bar{x}_4$, x_1x_3

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Simplification of function (PoS) form

Sum covers "f" $\boxed{F' < S}$

$\boxed{\text{prime Implicants}}$

$$f(A,B,C,D) = \Pi_m (1,3,4,6,7)$$

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	1	0	0
11	1	1	1	1
10	1	1	1	1

C, B, A, D

$(A+B+\bar{D})$, $(C'+A+D')$, $(A+B'+C')$,

$(A+B'+D)$, (

	0		
	0		
0	0		0

Distunquished Points	Essential Prime Numbers
0101	$A+C+D'$
1010	$A'+B+D$

$$(A+C+D')(A'+B+D)(A'+B+C)$$

$$f(x_1, x_2, x_3, x_4) = U_0(0,1,3,5,7,11,14) + U_\Phi(6,10,12)$$

$\boxed{\Phi = 0}$

0	0	0	
	0	0	ϕ
			0

	0	1	3	5	7	11	14	Cost
A								
B								
C								
D								
E								
F								
G								
H								

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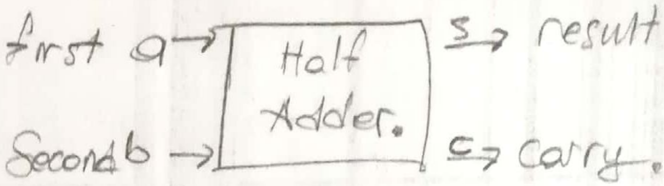
SSI
MSI
LSI
VLSI
ULSI

Half Adder

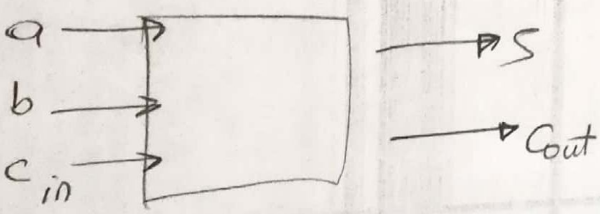


a	b	c	s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$\boxed{\bar{a}b + a\bar{b} = S}$

$\boxed{c = ab}$

Full Adder



a = first
b = second
c_{in} = Carry input
s = Result
c_{out} = Carry Out

a	b	c_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

S

a \ bc	00	01	11	10
$\bar{a}$	0	1	0	1
a	1	0	1	0

b, c

$\bar{a}\bar{b}c_{in} + \bar{a}b\bar{c}_{in} + a\bar{b}c_{in} + abc_{in}$

$S = a \oplus (b \oplus c_{in})$

$S = a \oplus (b \oplus c_{in})$

c

	0	0	1	0
	0	1	1	1

$C_{out} = ac_{in} + bc_{in} + ab$

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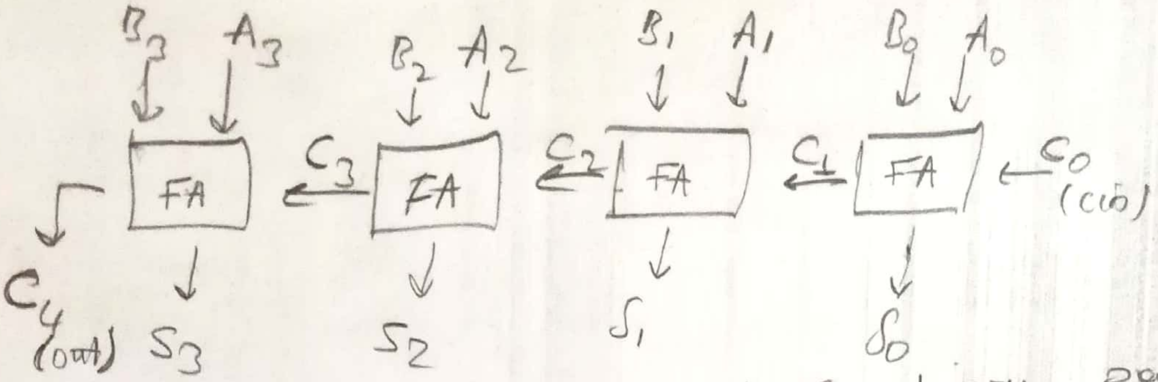
n-Bit Binary Parallel Adder.



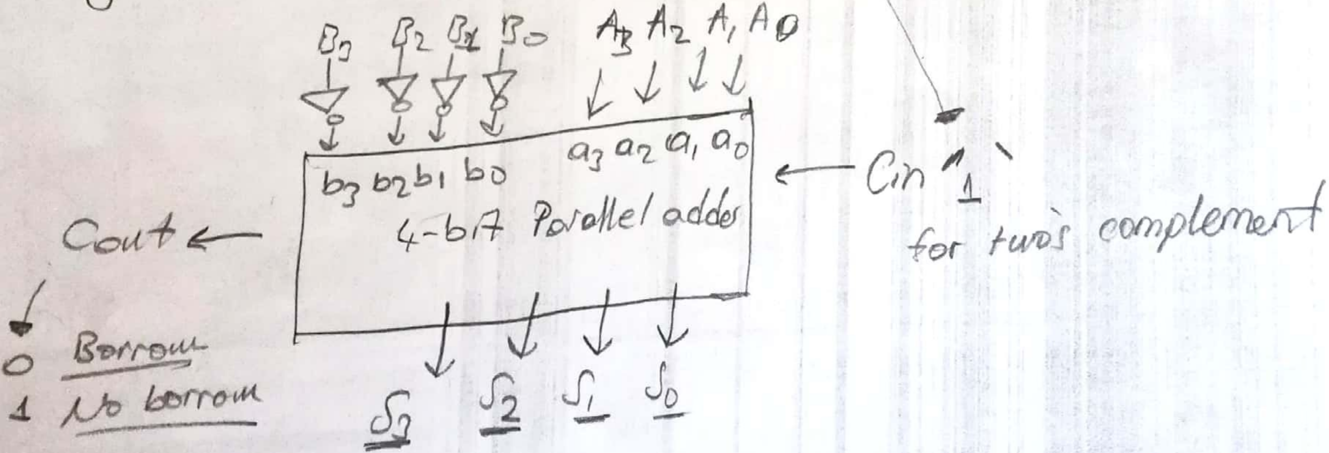
7483 IC is a 4 bit binary parallel adder.

We can find 8 bit adder by connecting 2 parallel 7483

Subtracting

Adder and not gates are enough.

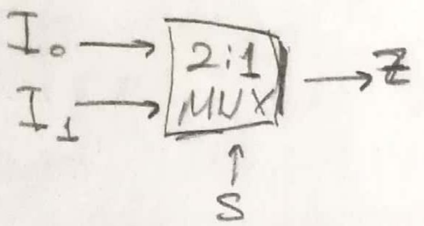
$S = A - B = A + (\bar{B} + 1)$



Multiplexer (MUX) (Data Selector)

2^n data inputs (I), n selector (control) inputs (S), 1 data inputs

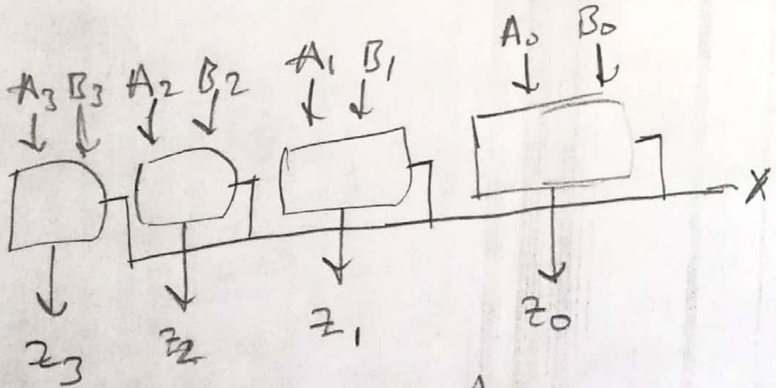
2:1 Multiplexer



if $S=0$ then $Z=I_0$
if $S=1$ " $Z=I_1$

S	Z
0	I_0
1	I_1

Paralle Connection of Multiplexer

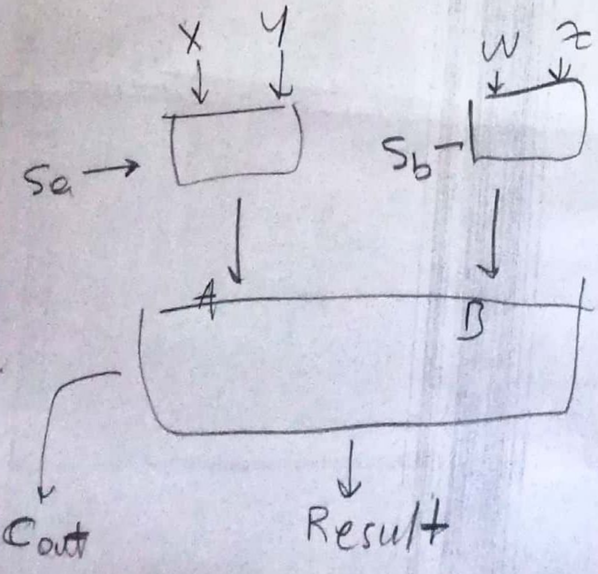


if $X=0 \rightarrow Z=A$
if $X=1 \rightarrow Z=B$

I_1	I_0	S	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Usage Of Multiplexer

The same adder circuit can be used to add different numbers.



Sa	Sb	Result
0	0	Y + W
0	1	X + Z
1	0	Y + W
1	1	Y + Z

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