**BLG 231E - Digital Circuits**

**Assignment 2**

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**1.** The truth table for a function y(A, B, C, D) is given below:

**0**

0

0

0

0

**0**

**1**

0

0

0

1

**1**

**2**

0

0

1

0

**0**

**3**

0

0

1

1

**1**

**4**

0

1

0

0

**0**

**5**

0

1

0

1

**1**

**6**

0

1

1

0

**0**

**7**

0

1

1

1

**0**

**8**

1

0

0

0

**0**

**9**

1

0

0

1

**1**

**10**

1

0

1

0

**1**

**11**

1

0

1

1

**0**

**12**

1

1

0

0

**1**

**13**

1

1

0

1

**0**

**14**

1

1

1

0

**1**

**15**

1

1

1

1

**1**

**a.** Write the expressions of y in the first and second canonical forms.

1st canonical form of y in SOP (ΣΠ) form:

y(A,B,C,D)=A’B’C’D + A’B’CD + A’BC’D + AB’C’D + AB’CD’ + ABC’D’ + ABCD’ +ABCD

2nd canonical form of y in POS (ΠΣ) form:

y(A,B,C,D)=(A+B+C+D)( A+B+C’+D)(A+B’+C+D)(A+B’+C’+D)(A+B’+C’+D’)(A’+B+C+D)(A’+B+C’+D’)( A’+B’+C+D’)

**b.** Minimize the expression in the first canonical form using axioms and theorems of Boolean algebra.

Show all steps in your minimization and write the name of the axiom/theorem/property you use on the right-hand side of the expression at each step.

=A’B’C’D + A’B’CD+A’BC’D+AB’C’D+AB’CD’+ABC’D’+ABCD’+ABCD // Consensus

=~~A’B’C’D~~ + ~~A’B’CD~~+A’BC’D+AB’C’D+AB’CD’+ABC’D’+ABCD’+ABCD+A’B’D// Absorption

=A’BC’D+AB’C’D+AB’CD’+ABC’D’+ABCD’+ABCD+A’B’D// Consensus

=A’BC’D+AB’C’D+AB’CD’+ABC’D’+~~ABCD’+ABCD+~~A’B’D+ABC// Absorption

=A’BC’D+AB’C’D+AB’CD’+ABC’D’+A’B’D+ABC// Consensus

=A’BC’D+AB’C’D+AB’CD’+~~ABC’D’~~+A’B’D+ABC+ABD’// Absorption

=A’BC’D+AB’C’D+AB’CD’+A’B’D+ABC+ABD’// Consensus

=A’BC’D+AB’C’D+~~AB’CD’~~+A’B’D+ABC+ABD’+ACD’// Absorption

=A’BC’D+AB’C’D+A’B’D+ABC+ABD’+ACD’// Consensus

=A’BC’D+~~AB’C’D~~+A’B’D+ABC+ABD’+ACD’+B’C’D// Absorption

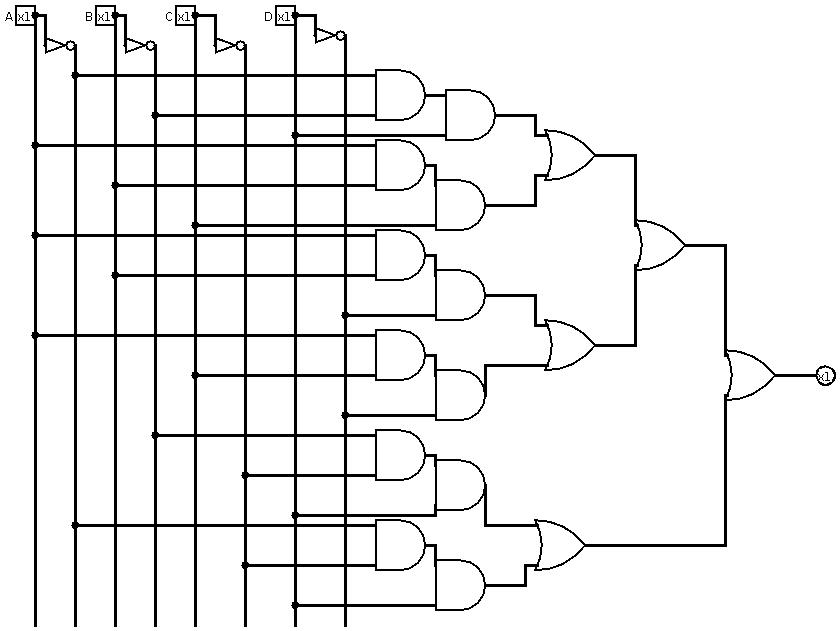
=A’BC’D+A’B’D+ABC+ABD’+ACD’+B’C’D// Consensus

=~~A’BC’D~~+A’B’D+ABC+ABD’+ACD’+B’C’D+A’C’D// Absorption

= A’B’D+ABC+ABD’+ACD’+B’C’D+A’C’D

**c.** Draw the circuit for the minimized expression in (b) using 2-input NAND gates only. Show all steps

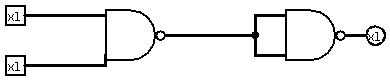
and explain your work leading up to the final circuit.



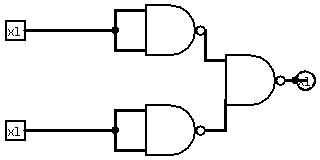
This is the circuit for A’B’D+ABC+ABD’+ACD’+B’C’D+A’C’D with using AND,OR and NOT gates. I will convert all of the AND,OR and NOT to NAND gate.



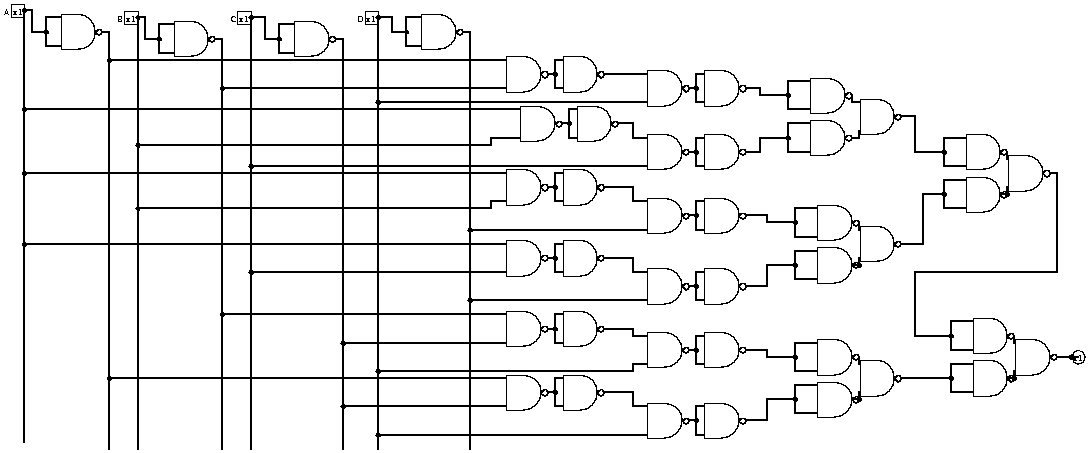
------------**→ this is equivalent of NOT gate**



**this one is equivalent of AND gate**



**this one is equivalent of OR gate**



I deleted two not gates which are come after each other, because (A’)’=A





