VMM notes

Ann Wang

March 7, 2016

1 VMM Synchronization Details

- Right now, the External Trigger Module has two options when turned on.
- So if we select the "External Trigger" button in the GUI, the module is turned on.
- Automatically it will send a acquisition reset and a FIFO (both levels of FIFOs on the FPGA) clear for every 4096 of the CKBC counter, or 102.4 microseconds. This involves turning off CKTK for the duration of the acquisition reset so the VMM does not mistake this as a configuration load. CKBC is also inhibited while we send the resets.
- If we receive an external trigger, which can be simulated using the "Send Ext Trig" button on the GUI, the module goes into a different mode.
- First it captures the BCID and Ext Trig Number (a counter which counts the number of ext trigs received thus far). These two numbers can be read by clicking the Reg5 read on the User Defined tab of the GUI
- Then it waits for approximately 200 us for the VMM FIFOs to drain. It then sets a bit up on a microblaze-interfaced register that says data is ready to be read.
- Then it waits for the GUI to take the data out and put a separate bit high, corresponding to the variable "reading_fin/reading_fin_flag". It will then send a acquisition reset. Currently there is no FIFO reset associated with this step, since we assume that all the data has come out.
- Again, during the acquisition reset, CKTK is disabled, and when we get a trigger we disable CKBC and then enable it again.

2 Registers used and variables used

- read_data corresponds to AXI_REG 77; "0144" (says we are ready to read data)

- bcid_captured & num_ext_trig correspond to AXI_REG 79; "014C"
- ext_trigger_sim corresponds to AXI_REG 78; "0148" (simulated trigger)
- ext_trigger_in_sel corresponds to AXI_REG 57, bit 25 (turns ext trig module on)
- reading_fin_flag corresponds to AXI_REG 76; "0140" (this says we are done reading)