LOGICAL DESIGN MANUAL

D. ZISSOS and G.W. COPPERWHITE

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$$+3/+6/b$$
$$\overline{AC+BC}$$
$$65:CBA$$

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Design

Manual

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Preface

The investigation of Race and Hazard phenomena in Switching Circuits has attracted considerable interest in recent years. This is possibly because a switching circuit may be tested and found to operate satisfactorily but an identical circuit using a different set of the same switching elements may fail to operate.

The cause of this is race hazards, in the form of narrow electrical pulses, which are present in the second case.

The aim of this manual is to explain the nature of these phenomena, how to detect their possible presence in circuits and to suggest simple but effective means of eliminating them, using step by step techniques at an early stage of the design, that is, before the actual circuit is realised.

Also, step by step design techniques for NOR and NAND switching circuits are introduced. The main difficulty so far has been that a minimal algebraic expression when realised directly does not result in a minimal circuit, as is the case with AND/OR and OR/AND logic. In NOR and NAND logic the switching function must first be optimised.

A chapter on Boolean Algebra has been included for completeness. A set of simple rules for minimising algebraic expressions is given, as well as a list of worked examples and a set of examples with answers.

The techniques described are used to design practical switching circuits.

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CHAPTER 1

BOOLEAN ALGEBRA

BOOLEAN ALGEBRA

Boolean Algebra is the mathematical treatment of switching circuits. It derives its name from George Boole, who first introduced it in 1847 in a paper on the mathematical analysis of logic. The adaptability of the algebra to telephone and computer switching circuits was first pointed out by C.E.Shannon in 1938 in the transactions of the A.I.E.E.

The treatment of Boolean Algebra in this book is to meet the needs of the designer of digital switching circuits. The Algebra is introduced for use as a tool to design reliable minimal switching circuits and as a means to develop logical thinking.

Variables, Operations and Laws in Boolean Algebra.

Boolean Algebra is possibly best understood if we cast our minds back to the conventional Algebra we all had to learn during our school days. Basically we learnt how to solve equations by applying certain operations on variables. The operations were addition, subtraction, multiplication and division and the variables, denoted by x, y, z etc., could have any value from minus infinity to plus infinity. The rules for applying each operation had to be learnt by heart. For example, we learnt our 'tables' and were able to solve equations using them. We had to learn that:

$8 + 2 = 10.$ $8 - 2 = 6.$ $8 \times 2 = 16.$ $8 \div 2 = 4.$ etc.

We were also taught three laws that have been found to be extremely important in the manipulation of conventional algebraic expressions. These laws were:

The Commutative Law

$A + B = B + A$
$A\,B = B\,A$

that is interchanging the order of variables in a sum or a product term does not affect the value of the algebraic expression.

The Associative Law

$A + (B + C) = (A + B) + C$
$A(B\,C) = (A\,B)\,C$

that is the variables in an algebraic expression may be grouped in any quantity, so long as they are connected by the same sign.

The Distributive Law

This law is possibly best remembered as the law that allows expanding and factorising of algebraic expressions.

For example:

the algebraic expression $f = (A + B)\,(C + D)$ can be expanded to $A\,C + A\,D + B\,C + B\,D$ by simply multiplying out the two sums.

Similarly by taking common factors, the algebraic expression $f = A\,B + A\,C + B\,D + C\,D$ can be modified to $f = A\,(B + C) + D(B + C)$.

Taking common factors again results in

$f = (A + D)(B + C)$.

In Boolean Algebra, as in the conventional Algebra, we manipulate variables in an expression according to specified rules, to derive the optimal or the form that best meets our needs. The first logical step, therefore, is to learn what the values are that the variables in a Boolean expression can have, secondly, which operations can be performed with them and finally which laws, if any, can be used to facilitate their manipulation.

Variables in Boolean Algebra

The variables in Boolean algebra can have one of two values only, namely, 0 or 1.

Operations in Boolean Algebra

The operations are addition, multiplication and inversion and the rules for each operation are:

Rules of Addition

The rules of addition are shown in Table 1. P_1 is the OR function of variables A and B and is expressed symbolically, as

$P_1 = A + B$

It is read 'P_1 equals A plus B ' or 'P_1 equals A or B'

Rules of Multiplication

Table 2 shows the rules of multiplication. P_2 is the AND function of variables A and B, and is expressed symbolically, as

$P_2 = A.B$

It is read 'P_2 equals A times B', or 'P_2 equals A and B'.

It is common practice, as in conventional algebra to omit the dots in product terms, for example

$P_2 = A.B$ can also be written as $P_2 = A\,B$

Note

At this stage it is worthwhile noting that there are no 'carries' in the above two operations, and also that the results tabulated in tables 1 and 2 are identical to the results of decimal arithmetic except for one namely 1 + 1 = 1 and not 2.

Rules of Inversion (complementation)

By definition the complement of 0 is 1, and of 1 is 0. The complement of variable A is $\underline{A}$ and is read 'NOT A'. It therefore follows that

if $A = 0$, $\underline{A} = 1$

and if $A = 1$, $\underline{A} = 0$

Laws of Boolean Algebra

The Commutative, Associative and Distributive laws that were found to apply in the conventional algebra, apply also in the Boolean algebra.

Because of the commutative law,

A + B can be modified to B + A and A B to B A.

Similarly, because of the associative law,

A + (B + C) can be modified to (A + B) + C and A(B C) to (A B) C.

The distributive law allows a Boolean expression to be expanded or factorised in exactly the same way as it does in conventional algebra. For example,

(A + B)(C + D) can be expanded to A C + A D + B C + B D,

by simply multiplying out.

Similarly a Boolean expression can be factorised in the conventional way, as the following example shows.

$$\begin{aligned} f &= A\,B + A\,C + B\,D + C\,D. \\ &= A\,(B + C) + D(B + C) \\ &= (A + D)\,(B + C) \end{aligned}$$

Comparison of the two algebras

Variables.

Whereas in the conventional algebra a variable can have any value from minus infinity to plus infinity, as well as complex values, in Boolean algebra it can only assume the value of either 0 or 1.

Operations

In Boolean Algebra there are only three basic operations, namely ADDITION, MULTIPLICATION and INVERSION. There is no division and subtraction. The table corresponding to each operation is considerably simpler than the one of the corresponding operation in conventional algebra.

Laws

Because the same laws apply in both algebras, a Boolean expression can be manipulated in exactly the same way as an expression in the conventional algebra.

Basic Boolean Relationships

From the rules of addition, multiplication and inversion the following relationships are obtained directly,

$A + 0 = A$	$A \,.\, 0 = 0$	$A + \underline{A} = 1$
$A + 1 = 1$	$A \,.\, 1 = A$	$A \,.\, \overline{\underline{A}} = 0$
$A + A = A$	$A \,.\, A = A$	

A	B	$P_1 = A + B$
0	0	$0 + 0 = 0$
0	1	$0 + 1 = 1$
1	1	$1 + 1 = 1$
1	0	$1 + 0 = 1$

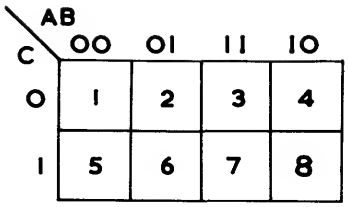
TABLE 1. ADDITION TABLE OF THE VARIABLES A AND B

A	B	$P_2 = A \cdot B$
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	1	$1 \cdot 1 = 1$
1	0	$1 \cdot 0 = 0$

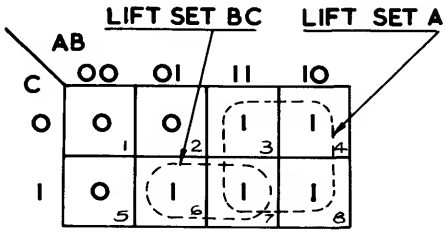
TABLE 2. MULTIPLICATION TABLE OF THE VARIABLES A AND B

A	B	C	P = A+B·C	SET No.
0	0	0	0+0·0 = 0	1
0	1	0	0 + 1·0 = 0	2
1	1	0	1 + 1·0 = 1	3
1	0	0	1+0·0 = 1	4
1	0	1	1+0·1 = 1	5
1	1	1	1+1·1 = 1	6
0	1	1	0+1·1 = 1	7
0	0	1	0+0·1 = 0	8

TABLE 3. TRUTH TABLE OF THE FUNCTION P = A + B·C



MAP 1. A THREE VARIABLE KARNAUGH MAP



MAP 2. KARNAUGH MAP OF FUNCTION A+ B·C

The Karnaugh Map

Consider the expression P = A + B C. The value of P will depend on the values of A, B and C. Now A, B and C can have eight sets of different values. Applying the rules of multiplication and addition we can determine the value of P in each case. These values of P are shown in table 3, commonly referred to as a truth table. Basically a truth table is a table which contains all the possible values that an expression can have.

Next consider map 1, known as the Karnaugh Map.

It has 8 squares and each square is specified by a corresponding set of values of A, B and C. For example, square 6 is specified by set 7 of table 3, that is A = 0, B = 1 and C = 1.

Map 1 is redrawn (Map 2) and in each square the value of P corresponding to the values of A, B and C that specify the square is entered. For example, in square 1, 0 is entered, since from the truth table P = 0 when A = B = C = 0. Similarly in square 2, 0 is also entered etc.

A Karnaugh map so far is seen to be simple a map method of representing the truth table of a Boolean function. It may appear at this stage that it has no other advantage than that of representation of information. It has, however, several advantages, which will become progressively obvious. For example, the plotting of it is quite simple. Though map 2 was derived from the truth table of the function P = A + B C, it can be plotted directly from the expression, as shown below.

Plotting of Karnaugh Maps

It is not necessary to draw the truth table of a given algebraic expression before we plot its Karnaugh Map. It can be done directly if it is realised for example that P = A in a three variable map implies a '1' entry in squares 3, 4, 7 and 8, since for all these squares A = 1, see map 2. Similarly B = 1 specifies collectively squares 2, 3, 6 and 7. Therefore the Karnaugh Map of P = B will have '1' entries in squares 2, 3, 6 and 7 since for all these squares B = 1, and '0' entries in the remaining squares. A B = 1 means that a 1 must be entered in squares 3 and 7 etc.

Now, in an AND/OR expression (sum of products), such as P = A + B C, if a product term equals 1, then the whole expression equals 1, since from the laws of addition 'one plus anything always equals one' This means that in the expression P = A + B C, P = 1, if A = 1, irrespective of the value of the second product term B C. But A = 1 specifies collectively squares 3, 4, 7 and 8 in map 2. Therefore a '1' is entered in these four squares. P is also equal to 1 if B C = 1, no matter what the value of variable A is. But B C specifies collectively squares 6 and 7. Therefore '1' is entered in square 6 a '1' is already present in square 7. Since in the remaining three squares namely 1, 3 and 5 neither of the product terms equals 1, a '0' is entered.

The same basic procedure is used for plotting the Karnaugh Map of OR/AND (product of sums) expressions.

Consider the OR/AND function f = (A + B)(A + C). Now f will be zero if the first bracket equals zero, irrespective of the value of the second bracket, or if the second bracket equals zero, also irrespective of the value of the first bracket. Now for A + B to equal 0, both A and B must equal 0 that is the entries in the squares specified by both A and B equal to 0, namely squares 1 and 5 in map 2, 0 is entered. Similarly, for A + C to equal 0, both A and C must be 0 that is the entries in the squares 1 and 2 are zero. The remaining entries must naturally be 1.

The Reading of Karnaugh Maps

Before describing the mechanics of reading Karnaugh maps, the following points should be made.

Minimal hazard-free design of switching circuits at present is essential, because of reliability and economy. A minimal Boolean expression when realised directly does not necessarily result in a minimal circuit. In certain cases the Boolean expression must be optimised before it is realised. The optimisation process described in this book always start with the minimal form of the expression. Therefore a clear, simple and effective method of simplifying Boolean expressions is obviously advantageous.

An AND/OR expression is minimal if it contains the minimum number of AND (product) terms, and if the number of variables in each AND (product) term is minimum provided the first condition is satisfied.

By analogy an OR/AND expression is minimal if it contains the minimum number of OR(sum) terms, and if the number of variables in each OR(sum) term is minimum, provided the first condition is satisfied.

To express therefore a function in its minimal AND/OR algebraic form directly from its Karnaugh map, the aim is to group the '1' entries in groups of adjacent fours (in a three variable map), whenever possible. This is because four adjacent 1 entries are collectively specified by a single term. Two adjacent '1' entries are collectively specified by a two variable product term. Therefore this set is used as 'second best'. A single '1' entry is specified by a product term containing all the three variables.

In deriving minimal Boolean expressions the aim will therefore be to group the 1 entries in groups of adjacent 4's. If this is not possible then in groups of adjacent 2's and if this also is not possible then each entry is specified separately, that is by the maximum number of letters

The minimal AND/OR expressions corresponding to Karnaugh maps 3(a), 3(b) and 3(c) are:

$\underline{A} + \underline{B}\,C$, $\underline{A}\,B + A\,\underline{B}$ and $\underline{A}\,\underline{C} + A\,C$ respectively.

The function $\underline{A}\,B + A\,\underline{B}$ is known as the exclusive OR function of variables A and B. This is because for $\underline{A}\,B + A\,\underline{B}$ to be equal to 1, either A must be equal to 0 and B equal to 1, making $\underline{A}\,B = \underline{0}.1 = 1.1 = 1$, or A must be equal to 1 and B to 0 making $A\,\underline{B} = 1.\underline{0} = 1.1 = 1$.

That is for the function $\underline{A}\,B + A\,\underline{B}$ to be equal to 1, either A or B must equal 1 but not both.

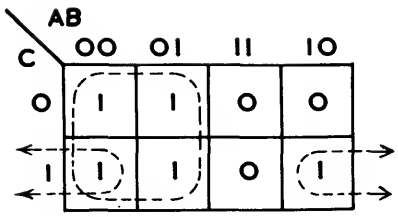
Switching function $A\,C + \underline{A}\,\underline{C}$ is known as an inclusive OR function of variables A and C. This is because for the function to equal 1, either A and C must both be equal to 1, simultaneously (making $A\,C = 1.1 = 1$), or they must both equal 0 simultaneously (making $\underline{A}.\underline{C} = \underline{0}.\underline{0} = 1.1 = 1$).

The following expressions correspond to the maps 4(a) and 4(b).

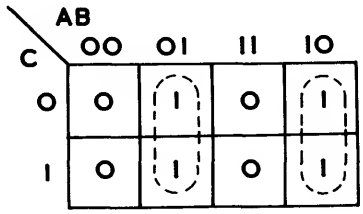
$P = \underline{A}\,\underline{B}\,\underline{C}$
$Q = \underline{A}\,\underline{C}$
$R = \underline{A}\,B + A\,\underline{C}$
$S = \underline{A} + \underline{B}$

The same entry may be taken with more than one group. Consider the Karnaugh map for X in map 5. The entries in squares 1, 4, 5 and 8 are taken together giving $X = \underline{B}$. The entry in square 6 is taken with entry in square 5, since this forms a group of 2, giving $X = \underline{A}\,C$. Therefore $X = \underline{B} + \underline{A}\,C$

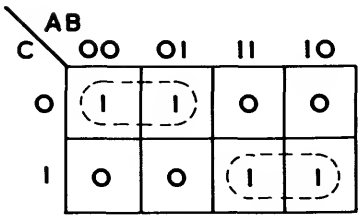
A set of basic formal theorems will now be given.



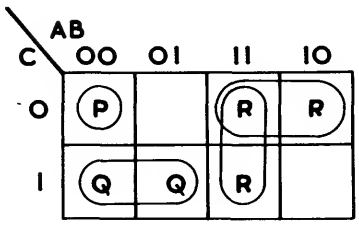
MAP 3(a)



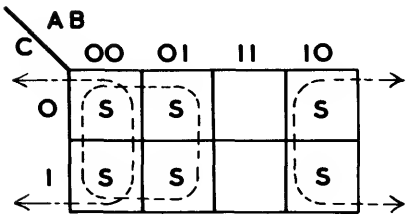
MAP 3(b)



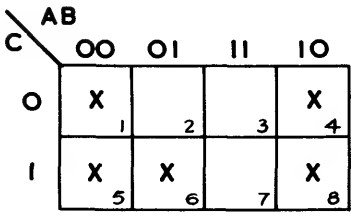
MAP 3(c)



MAP 4(a)



MAP 4(b)



MAP 5

Formal Theorems

T.1. $A + A\,B = A$

Proof
$$A + A\,B = A\,(1+B)$$
$$= A.1$$
$$= A$$

This theorem may be stated as follows.

In a sum of products (AND/OR) expression if a product term is a factor of another product term(s) the product term(s) containing it is(are) redundant.

Application of Theorem T.1. in the algebraic minimisation process of Boolean expressions

The application of this theorem is suggested as the first step in the algebraic process of minimising AND/OR Boolean expressions. Namely, the simplest AND (product) term, which may be a single variable ($A = A.1$) is first noted. The remaining AND (product) terms are next examined. If any of them contain the chosen term as a factor, they are redundant. The process is repeated.

Example

In the Boolean expression $A\,B + \underline{C}\,D + A\,B\,C\,D\,(E + F)$, AND (product) term $A\,B\,C\,D(E + F)$ is redundant, since it contains the term $A\,B$.

T.2. $A + \underline{A}\,B = A + B$

Proof
$$A + \underline{A}\,B = A(1 + B) + \underline{A}\,B$$
$$= A + B\,(A + \underline{A})$$
$$= A + B$$

Alternative proof

The above proof is rather stereotyped. The same result will be arrived at, as a result of a logical process.

We have to prove that $A + \underline{A}\,B = A + B$

Basically this means that we have to change $\underline{A}\,B$ into B. Now $B = A\,B + \underline{A}\,B$; that is all we need do is to add the term $A\,B$ to the original expression. But because A is present in the original expression, we can add any product that contains A as a factor, this of course follows from T.1. Therefore,

$$A + \underline{A}\,B = A + A\,B + \underline{A}\,B$$
$$= A + B$$

This theorem may be stated as follows:

In a sum of products (AND/OR) expression, if the complement of a product term is a factor of another product term(s) the complement term is redundant.

Application of theorem T.2. in the algebraic minimisation process of Boolean expressions

The application of this theorem is suggested as the second step in the algebraic minimisation process of AND/OR Boolean expressions. Namely, the simplest AND (product) term is first noted. The remaining AND(product) terms are next examined. If any of them contain the complement of the term under consideration as a factor, they can be rewritten with the factor partly or completely eliminated.

Example

$$A + \underline{A}\,B\,C + D\,E$$

The simplest product term is A. Because its complement $\underline{A}$ is a factor of $\underline{A}\,B\,C$, the latter is simplified to B C. No further simplification is possible.

T.3.

$$\begin{aligned} A\,B + \underline{A}\,C + B\,C &= A\,B + \underline{A}\,C \\ A\,B + \underline{A}\,C + B\,C &= A\,B + \underline{A}\,C + (A + \underline{A})B\,C \\ &= A\,B + A\,B\,C + \underline{A}\,C + \underline{A}\,B\,C \\ &= A\,B\,(1 + C) + \underline{A}\,C\,(1 + B) \\ &= A\,B + \underline{A}\,C \end{aligned}$$

Alternative Proof

In the Boolean expression $A\,B + \underline{A}\,C + B\,C$, we have to eliminate the term B C. Now, a product (AND) term in a sum of products (AND/OR) expression, is redundant if it contains as a factor a product term present in the same expression. Now, examining the product term in $A\,B + \underline{A}\,C + B\,C$, we note that the redundant term does not contain A. Therefore we multiply it by $A + \underline{A}$, which makes it $A\,B\,C + \underline{A}\,B\,C$. Now A B C is redundant because A B is already present in the expression. Similarly $\underline{A}\,B\,C$ is superfluous because of the product term B C.

Theorem 3 may be stated as follows

If a product (AND) term contains all the factors present in two product (AND) terms, one of which contains a variable (A) and the other is its complement ($\underline{A}$) then the first product (AND) term is redundant.

Application of theorem T.3. in the algebraic minimisation process of Boolean expressions

The application of this theorem is suggested as the third step in the algebraic minimisation process of AND/OR (sum of products) Boolean expressions. If an AND (product) term contains a variable and another AND (product) term contains its complement, then all product terms containing the coefficients of the variable under consideration and of its complement, are redundant.

Example

$$A\,B + \underline{A}\,C + B\,C\,D$$

The product (AND term B C D) because it contains the coefficients of A and $\underline{A}$ (B and C respectively) is redundant. Theorems 1, 2 and 3 apply to sum of products (AND/OR) expressions. Theorems 4, 5 and 6 are the equivalent theorems applied to product of sums (OR/AND) expressions.

T.4. $A(A + B) = A$

Proof

$$\begin{aligned} A(A + B) &= A\,A + A\,B \\ &= A + A\,B \\ &= A\,(1 + B) \\ &= A\,1 \\ &= A \end{aligned}$$

This theorem may be stated as follows.

In an OR/AND (product of sums) expression, if an OR (sum) term is contained in another OR term, the latter OR term is redundant. (A is considered as an OR term since it can be written as (A + 0)).
For example, in the expression

$$(A + B)\,(A + B + C + D\,E)\,(F + G)$$

the second term is redundant, because it contains the OR term (A + B).

Application of theorem T.4. in the algebraic minimisation process of Boolean expressions

T.4. constitutes the first step in the algebraic process of minimising OR/AND (product of sums) expressions. The mechanics of its application consist in examining a given OR/AND expression for the simplest possible OR (sum) term, which may be a single variable - since A can be written as (A + 0). The remaining OR (sum) terms are next examined. If any of them contain the chosen term as a factor they are redundant. The process is repeated.

Example

In the Boolean expression, $(A + B)\,(C + D)(A + B + C + D + E\,F)$, OR (sum) term $(A + B + C + D + E\,F)$ is redundant, since it contains all the variables present in OR (sums) term (A + B)

Note T.4. is the equivalent OR/AND theorem to T.1.

T.5. $A(A + B) = A\,B$

Proof

$$\begin{aligned} A(\bar{A} + B) &= A\,\bar{A} + A\,B \\ &= 0 + A\,B \\ &= A\,B \end{aligned}$$

This theorem may be stated as follows.

In an OR/AND (product of sums) expression, if the complement of an OR (sum) term is contained in another OR (sum) term, it is redundant.

Application of theorem T.5. in the algebraic minimisation process of Boolean expressions

Theorem 5 is used as the second step in the algebraic process of minimising OR/AND (product of sums) expressions. This step consists of noting the simplest OR (sum) term in the expression. The remaining terms are next examined. Its complement, if present, in any of the other OR terms is redundant.

Example

$$A\,(\underline{A} + B + C)(D + E)$$

The simplest OR term is A. OR term $\underline{A} + B + C$ contains its complement $\underline{A}$. Therefore it can be simplified to $(B + C)$

Note T.5. is the equivalent OR/AND theorem to T.2.

T.6. $(A + B)(\underline{A} + C)(B + C) = (A + B)(\underline{A} + C)$

Proof

$$\begin{aligned}(A + B)(\underline{A} + C)(B + C) &= (A.\underline{A} + \underline{A}\,B + A\,C + B\,C).(B + C)\\ &= (\underline{A}\,\overline{B} + \overline{A}\,C)(B + C)\\ &= \underline{A}\,\overline{B} + A\,B\,C + \underline{A}\,B\,C + A\,C\end{aligned}$$

A B C is redundant, because of the presence of $\underline{A}$ B (Theorem 1.)
Similarly A B C is redundant because of the presence of A C. Therefore

$$(A + B)(\underline{A} + C)(B + C) = \underline{A}\,B + A\,C$$

Considering next the R.H.S. of the equation, we get

$$\begin{aligned}(A + B)(\underline{A} + C) &= A\,\underline{A} + \underline{A}\,B + A\,C + B\,C\\ &= \underline{A}\,\overline{B} + \overline{A}\,C + B\,C\\ &= \underline{A}\,B + A\,C\end{aligned}$$

B C is redundant, because of T.3.

Application of theorem T.6. in the algebraic minimisation process of Boolean expressions

This theorem is applied in the third step of the minimisation process of OR/AND (product of sums) Boolean expressions. If an OR (sum) contains the complement of the variable in the same OR/AND expressions, then all OR terms containing the first and second OR terms are redundant.

Example

$$(A + B)(\underline{A} + C)(B + C + D)$$

OR term B + C + D is redundant because it contains all the terms present in the OR term that contains A, namely B, and all the terms present in the OR term containing $\underline{A}$, namely C.

Note T.6. is the equivalent OR/AND theorem to T.3.

T.7. $\underline{A\,B\,C} = \underline{A} + \underline{B} + \underline{C}$

Proof This theorem is best proved by plotting the Karnaugh map for each of the two expressions of the equation and showing that the two maps are identical.

See maps 6(a) and 6(b). They are identical, therefore $\underline{A\,B\,C} = \underline{A} + \underline{B} + \underline{C}$

T.8. $\underline{A + B + C} = \underline{A}\,.\,\underline{B}\,.\,\underline{C}$

Proof This theorem also is best proved by comparing the two Karnaugh maps of function $\underline{A + B + C}$ and $\underline{A}\,.\,\underline{B}\,.\,\underline{C}$

See Maps 7(a) and 7(b). Both maps are identical, therefore the theorem is proved.

T.7. and T.8. are collectively known as De Morgan's theorem, which states that to find the complement of a Boolean expression change all +'s signs to .'s, all .'s to +'s and replace each letter by its complement.

It is advisable to simplify the expression and include all product terms in brackets before complementing. The brackets remain unaffected by the complementing process.

Example

Write the complement of

$$f = A\,(\underline{B}\,\underline{C} + B\,C)$$

The expression is first minimised and then rewritten, with all its product terms included in brackets. The expression under consideration is already in its minimal form, therefore it is rewritten as:

$$f = A\,((\underline{B}\,\underline{C}) + (B\,C))$$

Applying De Morgan's theorem,

$$\begin{aligned} f &= \underline{A} + ((B + C)(\underline{B} + \underline{C})) \\ &= \overline{A} + B\,\underline{B} + B\,\overline{C} + \overline{B}\,C + C\,\underline{C} \\ &= \overline{A} + B\,\overline{C} + \underline{B}\,\overline{C} \end{aligned}$$

Note Applying De Morgan's theorem directly on a minimal AND/OR expression for f, results in a minimal OR/AND expression for $\underline{f}$. But multiplying out the minimal OR/AND expression to convert it to AND/OR, sometimes results in a non-minimal expression.

This is also the case in converting from a minimal AND/OR to OR/AND by taking out common factors. For example,

$$\begin{aligned} f &= A\,B + \underline{A}\,C \\ &= (A + \overline{A}\,C)(B + \underline{A}\,C) \\ &= (A + \overline{C})(B + \underline{A})(\overline{B} + C) \end{aligned}$$

which is not minimal as the B + C term is redundant.

The complement of a given expression can be obtained minimally from a Karnaugh Map directly by writing the AND/OR expression for the '0' entries. For example, to find the complement of $f = A.\ (\underline{B}\,\underline{C} + B\,C) = A\,\underline{B}\,\underline{C} + A\,B\,C$, we first draw its Karnaugh map - see map 8. From it we see that $\underline{f} = \overline{A} + \underline{B}\,C + B\,\underline{C}$

Derivation of minimal OR/AND expressions

The minimal OR/AND expression of a function can be derived systematically in three steps.

Step.1.

In this step the Karnaugh map of the function is plotted.

Step.2.

In the second step the minimal AND/OR expression for $\underline{f}$ is derived (by considering the 0 entries.)

Step.3.

De Morgan's theorem is applied directly to the expression derived in step.2.

C \ AB	00	01	11	10
0	1	1	1	1
1	1	1	0	1

MAP 6(a). KARNAUGH MAP OF FUNCTION $\underline{A \cdot B \cdot C}$

C \ AB	00	01	11	10
0	1	1	1	1
1	1	1	0	1

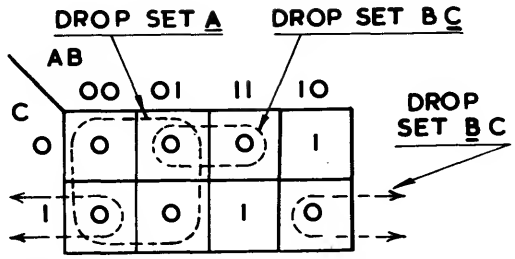
MAP 6 (b). KARNAUGH MAP OF FUNCTION $\underline{A}+\underline{B}+\underline{C}$

C \ AB	00	01	11	10
0	1	0	0	0
1	0	0	0	0

MAP 7(a). KARNAUGH MAP OF FUNCTION $\underline{A+B+C}$

C \ AB	00	01	11	10
0	1	0	0	0
1	0	0	0	0

MAP 7 (b). KARNAUGH MAP OF FUNCTION $\underline{A} \cdot \underline{B} \cdot \underline{C}$



MAP 8. KARNAUGH MAP OF FUNCTION A $[\underline{B} \cdot \underline{C} + B \cdot C]$

$A + \bar{C}\bar{B} + \bar{B}$

Example

Express Boolean expression $A\,\underline{B}\,\underline{C} + A\,B\,C$ in its minimal OR/AND form.

Step. 1.

The Karnaugh map of the expression is plotted, see map 8.

Step. 2.

The minimal AND/OR expression for $\underline{f}$ is derived by considering the 0 entries

$\underline{f} = \underline{A} + B\,\underline{C} + \underline{B}\,C$

Step. 3.

Applying De Morgan's theorem to the last expression, we get

$f = A(\underline{B} + C)(B + \underline{C})$

This is the required form.

Algebraic minimisation process of AND/OR (sum of products) Boolean expressions

Step. 1.

The simplest AND (product) term, which may be a single variable is first noted. All AND (product) terms containing this term are redundant.

Example

$A + A\,B + \underline{A}\,C + B\,D + A\,C\,E\,F + \underline{B}\,E + E\,D\,F$ ..... (1)

The simplest AND term is A. A B and A C E F are redundant, because they both include A. Therefore the original expression becomes

$A + \underline{A}\,C + B\,D + \underline{B}\,E + E\,D\,F$ ..... (2)

No further simplification is possible in this step.

Step. 2.

The simplest AND (product) term is again noted. Its complement, if present in other AND (product) terms is redundant.

In equation 2, $\underline{A}\,C$ is reduced to C.

We next examine the remaining terms in case they contain C or $\underline{C}$. etc., In this case they do not . Therefore the original expression after the second step reduces to

$A + C + B\,D + \underline{B}\,E + E\,D\,F$ ..... (3)

Step. 3.

In the third and final step each AND (product) term is examined with each other AND term in turn. If the same variable is present in two AND terms, in its true and inverted form respectively, all the remaining terms are examined. If any of them contain all the factors of the two terms under consideration (excluding of course the variable and its complement), they are redundant.

For example, AND term B D contains B and AND term $\underline{B}$ E contains $\underline{B}$. Therefore any AND term containing D E is redundant. Such term is E D F.

Therefore the minimal expression of the original function is

$A + C + B D + \underline{B} E$

Worked Examples

Example 1

Minimise the AND/OR function

$f = A B + A B C + B D$

Step. 1.

AND term A B C is redundant, because it contains AND term A B.

$\therefore \quad f = A B + B C$

Step. 2.

Since all AND terms contain the same number of variables, it does not apply, (unless of course one term is the complement of another).

Step. 3.

Similarly it does not apply in this case.

Example 2

Minimise the function

$f = A B + A B C + \underline{A} C + B C D$

Step. 1.

AND term A B C is redundant because of the presence of AND term A B.
Therefore, at the end of the first step the expression becomes

$f = A B + \underline{A} C + B C D$

Step. 2.

The expression cannot be simplified in this step.

Step. 3.

AND term B C D is redundant because it contains the AND term of the first and second AND terms when A and $\underline{A}$ are replaced by 1.

Therefore:

The minimal form of the function is

$f = A\,B + \underline{A}\,C$

Example 3

Minimise the function

$f = \underline{A}\,B\,\underline{C} + A\,D + B\,\underline{C}\,D$

Step.1.

The expression cannot be simplified as a result of the first step, since neither AND term $\underline{A}\,B\,\underline{C}$ nor AND term $B\,\underline{C}\,D$ contains AND term $A\,D$ (simplest AND term) as a factor.

Step.2.

Application of this step also does not affect the equation.

Step.3.

The first AND term contains $\underline{A}$ and the second A. This makes the third term $B\,\underline{C}\,D$ redundant, since it contains the coefficient of $\underline{A}$ namely $B\,\underline{C}$ and that of A, namely D.

Therefore the required minimal form of the equation is:

$f = \underline{A}\,B\,\underline{C} + A\,D$

Example 4

Minimise the AND/OR function

$f = A\,\underline{B}\,C + \underline{A}\,\underline{C}\,D + A\,\underline{C}$

Step.1.

This step does not affect the original equation

Step.2.

$$
\begin{aligned}
f &= A(\underline{B}\,C + \underline{C}) + \underline{A}\,\underline{C}\,D \\
&= A(\overline{B} + \underline{C}) + \underline{A}\,\overline{C}\,\overline{D} \\
&= A\,\overline{B} + \overline{A}\,C + \underline{A}\,\underline{C}\,D \\
&= A\,\overline{B} + C\,(\overline{A} + \underline{A}\,\overline{D}) \\
&= A\,\overline{B} + \overline{C}\,(A + \overline{D}) \\
&= A\,\underline{\overline{B}} + \overline{A}\,\underline{C} + \underline{C}\,D
\end{aligned}
$$

Step.3.

This step does not affect the expression derived in the previous step.

Therefore, the minimal AND/OR form of the equation is

$f = A\,\underline{B} + A\,\underline{C} + \underline{C}\,D$

Example 5

Minimise the function

$f = A + A\,\underline{B}\,\underline{C} + \underline{A}\,C\,D + (\underline{C} + \underline{D})E$

Step.1.

Because of A, AND term $A\,\underline{B}\,\underline{C}$ is redundant.

Step.2.

Also because of A, $\underline{A}$ in AND term $\underline{A}\,C\,D$ is redundant. $(\underline{C} + \underline{D})$ in AND term $(\underline{C} + \underline{D})E$ is also redundant because of C D. Therefore

$f = A + C\,D + E$

Step.3.

The application of this step does not affect the equation.

Therefore, the required minimal form is

$f = A + C\,D + E$

Example 6

Minimise the algebraic AND/OR function

$f = A\,\underline{B} + \underline{A}\,C\,D + B + \underline{C} + \underline{D}$

Step.1.

The application of this step does not affect the equation.

Step.2.

Because of the presence of variable B, variable $\underline{B}$ in AND term $A\,\underline{B}$ is redundant.

Similarly because of $\underline{C}$ and $\underline{D}$, variables C and D in AND term $\underline{A}\,C\,D$ are redundant.

Therefore,

$f = A + \underline{A} + B + \underline{C} + \underline{D}$

But $A + \underline{A} = 1$

Hence

$f = 1 + B + \underline{C} + \underline{D}$
$= 1$

There is no need to go further.

Algebraic minimisation process of OR/AND (product of sums) Boolean Expressions

Step.1.

The simplest OR (sum) term, which may be a single variable, is first noted. All OR (sum) terms containing this term are redundant.

Example

$A(A + B)(\underline{A} + C)(B + D)(A + C + E + F)(\underline{B} + E)(E + D + F)$ ..... (1)

The simplest OR term is A, since $A = (A + 0)$. OR terms $(A + B)$ and $(A + C + E + F)$ both contain this term. Therefore they are redundant.

Equation 1 therefore becomes

$A(\underline{A} + C)(B + D)(\underline{B} + E)(E + D + F)$ ..... (2)

Step.2.

The simplest OR (sum) term is again noted. Its complement, if present in other OR terms is redundant.

In equation 2, because of A, $\underline{A}$ in OR term $\underline{A} + C$ is redundant.

We next examine the remaining terms in case they contain C or $\underline{C}$ etc. In this case they do not. Therefore, the original expression after the second step reduces to

$A \cdot C\ (B + D)(\underline{B} + E)(E + D + F)$ ..... (3)

Step.3.

In the third and final step each OR (sum) term is examined with each other OR term in turn. If the same variable is present in two OR terms, in its true and inverted form respectively, all the remaining terms are examined. If any of them contain all the factors of the two terms under consideration(excluding of course the variable and its complement,) they are redundant.

For example, referring to equation 3 in step 2, we note that OR terms (B + D) and ($\underline{B}$ + E) contain B and $\underline{B}$ respectively. Therefore OR term (E + D + F) because it contains D and $\overline{E}$ is redundant.

Therefore the minimal expression of the original function is

A C (B + D)($\underline{B}$ + E)

Worked Examples

Example 1

Minimise the OR/AND function

f = (A + B)(A + B + C) (B + D)

Step. 1.

OR term (A + B + C) is redundant, because it contains OR term (A + B).
Therefore at the end of the first step the equation is reduced to

f = (A + B)(B + D)

Step. 2.

Since all OR terms contain the same number of variables, it does not apply.

Step. 3.

Similarly it does not apply in this case.

Example 2

Minimise the OR/AND function

f = (A + B)(A + B + C)($\underline{A}$ + C)(B + C + D)

Step. 1.

OR term (A + B + C) is redundant because of the presence of OR term (A + B).

Therefore at the end of the first step, the function f is reduced to

f = (A + B)($\underline{A}$ + C)(B + C + D)

Step. 2.

The expression cannot be simplified in this step.

Step.3.

OR term $(B + C + D)$ is redundant, because it contains the OR function of the first and second brackets when both A and $\underline{A}$ are replaced by 0 namely $0 + B + 0 + C = B + C$.

Therefore the minimal form of the function is

$$f = (A + B)(\underline{A} + C)$$

Example 3

Minimise the function

$$f = (\underline{A} + B + \underline{C})\ (A + D)(\ B + \underline{C} + D)$$

Step.1.

The expression cannot be simplified as a result of this step, since neither OR term $(\underline{A} + B + \underline{C})$ nor OR term $(\ B + \underline{C} + D)$ contains OR term $A + D$

Step.2.

Application of this step also does not affect the equation.

Step.3.

The first OR term contains variable $\underline{A}$ and the second OR term variable A. Therefore, the third OR term is redundant, since it is equal to the OR function of the first and second OR terms, when A and $\underline{A}$ are both replaced by 0.

Therefore, the required minimal form of the equation is

$$(\underline{A} + B + \underline{C})(A + D)$$

Example 4

Minimise the function

$$f = (A + \underline{B} + C)(\underline{A} + \underline{C} + D)(A + \underline{C})$$

Step.1.

This step does not affect the original equation.

Step.2.

$$\begin{aligned} f &= (A + \underline{B}\,\underline{C} + C\ .\ \underline{C})(\underline{A} + \underline{C} + D) \\ &= (A + \overline{B}\,\overline{C}\ )(\underline{A} + \overline{C} + \overline{D}) \\ &= (A + \underline{\overline{B}})(A + \underline{\overline{C}})(\underline{A} + \underline{C} + D) \end{aligned}$$

Step.3.

This step does not affect expression derived in previous step.

Therefore the minimal OR/AND form of the equation is

$f = (A + \underline{B})(A + \underline{C})(\underline{C} + D)$

Example 5

Minimise the function

$f = A.(A + \underline{B} + \underline{C})(\underline{A} + C + D)(E + \underline{C}\ \underline{D})$

Step.1.

Because of A, OR term $(A + \underline{B} + \underline{C})$ is redundant.

Step.2.

Also because of A, $\underline{A}$ is OR term $\underline{A} + C + D$ is redundant.

The appearance of OR term (C + D) makes $\underline{C}\ \underline{D}$; ($=\underline{C + D}$); in OR term $E + \underline{C}\ \underline{D}$ redundant.

Therefore at the end of the second step,

$f = A\ (C + D)E$

Step.3.

The application of this step does not affect the equation.

Therefore the required minimal form is

$f = A\ E\ (C + D)$

Example 6

Minimise the algebraic OR/AND function.

$f = (A + \underline{B})(\underline{A} + C + D)B\ .\ \underline{C}\ .\ \underline{D}$

Step.1.

The application of this step does not affect the equation.

Step.2.

Because of the presence of variable B, variable $\underline{B}$ in OR term $(A + \underline{B})$ is redundant.

Similarly because of the presence of $\underline{C}$ and $\underline{D}$ in the expression, variables C and D in OR term $(\underline{A} + C + D)$ are redundant.

Therefore,

$f = A\ B\ \underline{C}\ \underline{D}\ \underline{A}$
$= 0$ There is no need to go further.

Alternative Method of Minimising OR/AND functions

A comparison of the worked examples in both methods reveals that they are equivalent. If in an OR/AND expression the 'dots' and 'pluses' are interchanged, an AND/OR expression is obtained.

If the derived AND/OR expression is first minimised and then converted to OR/AND form by simply interchanging the 'dots' and 'pluses' the resultant expression is the minimal OR/AND form of the given function.

To minimise OR/AND function $f = (A + B)(A + B + C)(B + D)$ we first derive AND/OR expression f_1 by interchanging the 'dots' and 'pluses':

$$f_1 = A\,B + A\,B\,C + B\,D$$

Applying the minimisation process explained, it reduces to

$$f_1 = A\,B + B\,D$$

Reconverting to f, by interchanging the 'dots' and 'pluses' we get

$$f = (A + B)(B + D)$$

Inverted Inputs not readily available

This method of attack is used when the inverted inputs needed to realise a given switching function using AND/OR elements are not readily available, and it is desired to use the minimum number of inverters. It consists of collecting all the complemented terms together in one bracket, since a Boolean expression containing inverted terms only can be realised with <u>one inverter</u>.

Example Realise the following function using the minimum number of inverters.

$$f = \underline{A}\,\underline{B}\,D\,E + \underline{A}\,\underline{B}\,C + \underline{A}\,\underline{C}\,D\,E + A\,B$$

The procedure is to collect all the complemented terms together in one bracket.

Rearranging the terms:

$$\begin{aligned} f &= \underline{A}\,\underline{B}\,(C + D\,E) + \underline{A}\,\underline{C}\,(D\,E) + A\,B \\ &= \overline{A}\,\overline{B}\,(C + D\,E) + \overline{A}\,\overline{C}\,(C + D\,E) + A\,B \\ &= (\overline{A}\,\overline{B} + A\,C)(C + \overline{D}\,\overline{E}) + A\,B \\ &= \overline{A}\,(\overline{B} + \overline{C})(C + D\,E) + A\,B \\ &= \underline{\overline{A} + \overline{B}\,\overline{C}}.\ (C + D\,E) + A\,B \end{aligned}$$

Further Notes on Karnaugh Maps

We shall now define two terms commonly used in switching, namely LIFT SETS and DROP SETS.

LIFT SETS

An AND/OR (sum of products) expression equals 1, if at least one of its AND (products) terms equals 1 since then we have 1 + (0 or 1), which always equals 1.

In other words the minimum number of variables which must equal 1 to ensure that the AND/OR expression is equal to 1, are the variables in an AND term.

For example, in the AND/OR expression,

$f = A\,B + C\,D$

for f to be equal to 1, we must have that at least A and B both equal to 1.

By definition the smallest set of the variables in an AND/OR expression which, when equal to 1, ensure that the expression equals 1, is referred as a <u>lift set</u>.

For example, in the AND/OR expression A B + C D, A and B form one lift set, and C and D a second lift set. The lift sets can be marked on a Karnaugh map as shown in map 9.

DROP SETS

An OR/AND (product of sums) expression equals 0, if at least one of its OR (sum) terms equals 0, since then we have 0, (0 or 1), which always equals 0.

In other words the minimum number of variables which must equal 0 to ensure that the OR/AND expression is equal to 0, are the variables in an OR term.

For example in the OR/AND expression

$f = (A + B)(C + D)$

for f to equal 0, we must have that at least A and B both equal 0
or C and D both equal 0.

By definition the smallest set of variables in an OR/AND expression which, when equal to 0, ensure that the expression equals 0, is referred to as a <u>drop set</u>.

For example, in the OR/AND expression (A + B)(C + D), A and B form one drop set and C and D a second drop set. The drop sets can be marked on a Karnaugh map as shown in Map 10.

Minterms and Maxterms

A <u>minterm</u> of n variables is a Boolean product of all the n variables, with each variable present in either its true or in its complement form e.g. the minterms of two variables A and B are

$A\,B$, $\underline{A}\,B$, $A\,\underline{B}$ and $\underline{A}\,\underline{B}$

The minterms will be formed by writing the letters in alphabetical order and assigning the value ONE to letters that appear in their true form, and ZERO to letters that are complemented e.g. the 8 minterms of three variables A, b and C are:

$$m_0 = \underline{A}\,\underline{B}\,\underline{C}$$
$$m_1 = \underline{A}\,\underline{B}\,C$$
$$m_2 = \underline{A}\,B\,\underline{C}$$
$$m_3 = \underline{A}\,B\,C$$
$$m_4 = A\,\underline{B}\,\underline{C}$$
$$m_5 = A\,\underline{B}\,C$$
$$m_6 = A\,B\,\underline{C}$$
$$m_7 = A\,B\,C$$

The suffix is the decimal equivalent number corresponding to the binary number by assigning the value of '0' to variables present in their inverted form and '1' to the variables present in their true form.

For example:

2^2	2^1	2^0		
0	0	0	=	0
0	0	1	=	1
0	1	0	=	2
0	1	1	=	3
1	0	0	=	4
1	0	1	=	5
1	1	0	=	6
1	1	1	=	7

<u>Note</u>

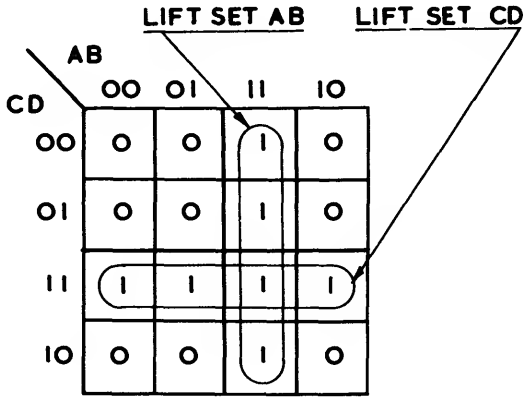
The sum of all the minterms of a given number of variables is always equal to 1, for example,

$$m_0 + m_1 + m_2 + m_3 = 1$$

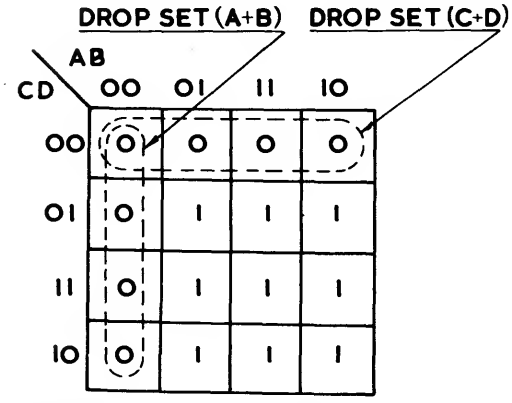
where $m_0 = \underline{A}\,\underline{B}$, $m_1 = \underline{A}\,B$, $m_2 = A\,\underline{B}$ and $m_3 = A\,B$.

A maxterm of n variables is a Boolean sum of all the n variables where each variable is present in either its true or its complement form.

e.g. the maxterms of two variables A and B are $A + B$, $\underline{A} + B$, $A + \underline{B}$ + $\underline{A} + \underline{B}$.



MAP 9. KARNAUGH MAP OF THE FUNCTION A·B + C·D WITH ALL THE LIFT SETS MARKED



MAP 10. KARNAUGH MAP OF FUNCTION (A+B)(C+D) WITH ALL THE DROP-SETS MARKED

The eight maxterms of three variables A, B and C are:

$$
\begin{aligned}
M_0 &= \underline{A} + \underline{B} + \underline{C} \\
M_1 &= \underline{A} + \underline{B} + C \\
M_2 &= \underline{A} + B + \underline{C} \\
M_3 &= \underline{A} + B + C \\
M_4 &= A + \underline{B} + \underline{C} \\
M_5 &= A + \underline{B} + C \\
M_6 &= A + B + \underline{C} \\
M_7 &= A + B + C
\end{aligned}
$$

Note that $M_0 = \underline{m_7}$

$M_1 = \underline{m_6}$

$M_2 = \underline{m_5}$ etc.

Relationship between minterm sum and maxterm product expressions

This relationship is illustrated by means of the following example.

Example

Consider the function of three variables defined by the following truth table.

A	B	C	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Express the function (i) as a sum of minterms and (ii) as a product of maxterms.

$$f = m_1 + m_5 + m_7$$

$$\underline{f} = m_0 + m_2 + m_3 + m_4 + m_6$$

$$f = \underline{m_0} \cdot \underline{m_2} \cdot \underline{m_3} \cdot \underline{m_4} \cdot \underline{m_6}$$

$$f = M_7 \cdot M_5 \cdot M_4 \cdot M_3 \cdot M_1$$

$$= (A + B + C)(A + \underline{B} + C)(A + \underline{B} + \underline{C})(\underline{A} + B + \underline{C})\,(\underline{A} + \underline{B} + C)$$

The Map Method of expressing Boolean expressions as a sum of minterms

To express a given Boolean function as a sum of minterms, we specify each 1 entry in its Karnaugh map by a lift set. This is because by definition each 1 entry in the map corresponds to a maxterm.

Example

Express the Boolean expression A + B C as a sum of minterms.

Specify each 1 entry in its Karnaugh map see map 2, we get that

$$f = A\,B\,\underline{C} + A\,B\,C + \underline{A}\,B\,C + A\,\underline{B}\,\underline{C} + A\,\underline{B}\,C$$

$$= m_6 + m_7 + m_3 + m_4 + m_5$$

$$= m_3 + m_4 + m_5 + m_6 + m_7$$

The Map Method of expressing Boolean expressions as a product of maxterms

This is achieved by including every 0 entry of the expression in a drop set, as the following example illustrates.

Example

Express the function A + B C as a product of maxterms.

From its Karnaugh map, map 2, we have that

$$f = (A + B + C)(A + \underline{B} + C)(A + B + \underline{C})$$

The same result could have been obtained using the sum for minterms expression.

For example,

$$f = m_3 + m_4 + m_5 + m_6 + m_7$$

$$= \underline{m_0 + m_1 + m_2}$$

$$= \underline{m_0} \cdot \underline{m_1} \cdot \underline{m_2}$$

$$= M_7 \cdot M_6 \cdot M_5$$

$$= (A + B + C)(A + B + \underline{C})(A + \underline{B} + C)$$

The Four different forms a Boolean expression can have

These are shown below

$$f = A\,B + C\,D \quad \text{--- AND/OR}$$

$$= (A + C)(A + D)(B + C)(B + D) \quad \text{--- OR/AND}$$

$$= \underline{A\,B \cdot C\,D} \quad \text{--- NAND/NAND}$$

$$= \underline{(A + C) + (A + D) + (B + C) + (B + D)} \quad \text{--- NOR/NOR}$$

NOTE These expressions are not necessarily in their true form.

PROBLEMS

A. Minimise the following expressions:	Answers.
1. $A.(\underline{A}+B)+B.(B+C)+B$	B
2. $(\underline{A}+\underline{B}+\underline{C}).(B+\underline{B}+\underline{C}).(C+\underline{B}+\underline{C})$	$\underline{ABC}$
3. $A.B+A.\underline{B}+\underline{A}.B+\underline{A}.\underline{B}$	1
4. $AD+BCD+ABD$	$AD+BCD$
5. $A.B.C+\underline{A}+\underline{B}+\underline{C}$	1
6. $(A+B).(\underline{A}+B)$	B
7. $(A+A.B+A.B.C).(A+B+C)$	A
8. $(A.\underline{B}+\underline{A}.B).(A.B+\underline{A}.\underline{B})$	0
9. $A.B.C.+\underline{A}.B+A.B.\underline{C}$	B
10. $A.B+\underline{A}.C+B.C$	$A.B+\underline{A}.C$
11. $A.B+A.\underline{B}+\underline{A}.\underline{B}$	$A+\underline{B}$
12. $\overline{(A.B+A.\underline{B}+\underline{A}B)}.(\underline{A}.\underline{B}+CD)$	$\underline{A}.\underline{B}$
13. $(E.D+A.B.C).(E.D+\underline{A}+\underline{B}+\underline{C})$	$E.D$
14. $(A.B+A.\underline{B}+\underline{A}B).(A+B+D+\underline{A}.\underline{B}.\underline{D})$	$A+B$
15. $\underline{A}.B+A.\underline{B}.D+BD$	$\underline{A}.B+AD$
16. $(A.\underline{B}+D).(A+\underline{B})D$	$A.D+\underline{B}.D$
17. $A.\underline{B}+D+(A+\underline{B}).D$	$A.\underline{B}+D$
18. $D.A+C.D+\underline{A}.C+A.\underline{B}.C.D.$	$A.D+\underline{A}.C$
19. $\underline{C}.\underline{A}+\underline{A}.\underline{B}+B.C+\underline{A}.\underline{C}.\underline{D}.$	$\underline{A}+B.C$
20. $A.\underline{B}+B.\underline{C}+A.\underline{B}.\underline{C}+A.B.\underline{C}.D$	$A\underline{B}+B.\underline{C}$
21. $\underline{B}\,\underline{C}+\underline{A}\,\underline{C}+AB+A\underline{C}$	$\underline{C}+AB$
22. $\underline{A}\,\underline{B}+\underline{B}\,\underline{C}+AC$	$\underline{B}+AC$
23. $AD+BC\underline{D}+(\underline{A}+\underline{B})C$	$C+AD$
24. $A\underline{B}\,\underline{C}+AC+\underline{A}BC\,\underline{D}$	$A\underline{B}+AC+BC\underline{D}$
25. $A\underline{B}+\underline{A}CD+B+\underline{C}+\underline{D}$	1
26. $ABC+\underline{A}D+(\underline{B}+C)D$	$AB\underline{C}+D$
27. $AC+\underline{A}\,\underline{B}+\underline{B}\,\underline{C}\,\underline{D}+BE\underline{C}+DE\underline{C}$	$AC+\underline{A}\,\underline{B}+\underline{B}\,\underline{D}+\underline{C}E$
28. $BC+A\underline{E}+E\underline{B}D+E\underline{C}D$	$BC+A\underline{E}+ED$
29. $AB+\underline{A}C+(\underline{B}+\underline{C})D$	$AB+\underline{A}C+D$
30. $AB+\underline{A}C+(\underline{B}+\underline{C}+\underline{D})E$	$AB+\underline{A}C+\underline{D}E$

B. Complement: Answers

1. $((A\,\underline{B} + C)D + \underline{E})F$ $((\underline{A} + B)\underline{C}+\underline{D})E + \underline{F}$

2. $A(\underline{B} + C(D + \underline{E})) + F$ $\underline{A}\,\underline{F} + B\,\underline{F}\,(\underline{C} + \underline{D}\,E)$

3. $A\,\underline{B} + (A + C\,D)\,(A + \underline{B}\,\underline{C})$ $\underline{A}$

C. By means of a Karnaugh Map, show whether the following equations are valid or not.

1. $A.B + \underline{A}.\underline{B} + B.C = A.B + \underline{A}.\,\underline{B} + \underline{A}.C$ Valid

2. $(A + B).(B + C).(C + A) = (\underline{A} + \underline{B}).(\underline{B} + \underline{C}).(\underline{C} + \underline{A})$ not valid

3. $(A + C).(A + D).(B + C).(B + D) = A.B + C.D$ Valid

D. Reduce the following expressions to a single occurence of A and $\underline{A}$.

1. $A\,G + (A + B)C + \underline{A}\,D + (\underline{A} + F)E$ $A(G + C) + B\,C + F\,E + \underline{A}(D + E)$

2. $\underline{A}\,\underline{B}\,(C + D) + \underline{X}\,\underline{Y}\,C + \underline{X}\,\underline{Y}\,D\,\underline{E} + E$ $(C + D)\underline{(A + B).(X + Y)} + E$

E. Problems in Logic
(see end of chapter for model solutions).

1. Given:-

(1) Alice never gossips.

(2) Betty gossips if, and only if, Alice is present.

(3) Clarice gossips under all conditions, even when alone.

(4) Dorothy gossips if, and only if Alice is present.

Determine the condition when there is no gossip in the room.

2. Alice, Betty, Clarice and Dorothy have engaged in a cake-baking contest and each won one of the four prizes. Three of the girls reported as follows: Alice said "Clarice was first, Betty was second". Betty said "Clarice was second, Dorothy was third". Clarice said "Alice was second, Dorothy was fourth". Each of the three girls made one correct statement and one false one. What were the results of the contest?

3. One of the four men, Adams, Baker, Charles and Davis has committed a crime. The men make the following statements:

Adams: "Charles did it"
Baker: "I didn't do it"
Charles: "Adams's statement is false"
Davis: "Adams did it".

(a) If exactly one of the four statements is true, who is the guilty man?

(b) If exactly one of the four statements is false, who is guilty?

4. Three marbles are drawn successively and at random from a sack containing marbles which are red or white or blue. Two of those drawn are red and exactly one of the following three statements is true.

(i) The first marble drawn is blue.
(ii) The third marble drawn is red.
(iii) The third marble drawn is not white.

What is the colour of the three marbles drawn?

Model Solutions to Problems in Section E

1. Let G = 1 indicate the presence of gossip in the room,

A = 1 the presence of Alice in the room,
B = 1 the presence of Betty in the room,
C = 1 the presence of Clarice in the room, and
D = 1 the presence of Dorothy in the room.

Then,

$$G = A.B + C + A.D$$
$$= C + A\,(B + D)$$

To find the condition for no gossip, G, we simply invert using De Morgan's theorem

$$\underline{G} = \underline{C}\ (\underline{A} + \underline{B}\ \underline{D})$$

that is,the conditions for no gossip are that Clarice must be absent and Alice or Betty and Dorothy must be absent.

CD \ AB	00	01	11	10
00	1	C 2	3	BCD 4
01	BC 5	6	7	8
11	9	10	11	12
10	AB 13	14	15	16

MAP 11. TABULAR REPRESENTATION OF PROBLEM E3

2. Let A1 = Alice was first,
A2 = Alice was second etc.,

$$\left.\begin{array}{l} C1 \,.\, \underline{B2} + \underline{C1} \,.\, B2 = 1 \\ C2 \,.\, \underline{D3} + \underline{C2} \,.\, D3 = 1 \\ A2 \,.\, \underline{D4} + \underline{A2} \,.\, D4 = 1 \end{array}\right) \quad (1)$$

$$\left.\begin{array}{r} \text{Now } C1 \,.\, C2 = 0 \\ B1 \,.\, C1 = 0 \\ \text{etc..} \end{array}\right) \quad (2)$$

$$(C1.\ \underline{B2} + \underline{C1}\ .\ B2)(C2\ .\ \underline{D3} + \underline{C2}\ .\ D3)(A2\ .\ \underline{D4} + \underline{A2}\ .\ D4) =$$

$$(C1\,.\,C2.\ \underline{B2}\ \underline{D3} + \underline{C1}\ .\ C2\ B2\ \underline{D3} + C1\ \underline{C2}\ \underline{B2}\ D3 + \underline{C1}\ \underline{C2}\ B2\ D3)\ .\ (A2\ \underline{D4} + \underline{A2}\ D4)$$

The first and second term of the first OR term are redundant.

$$\therefore\ = A2\ \underline{B2}\ C1\ \underline{C2}\ D3\ \underline{D4} + \underline{A2}\ B2\ \underline{C1}\ \underline{C2}\ D3\ D4$$

the second term is redundant.

i.e. Clarice was first,
Alice was second,
Dorothy was third,
Betty was fourth.

3. Algebraically the four statements can be expressed as

Adams' statement	:	$\underline{A}\ \underline{B}\ C\ \underline{D}$
Bakers' statement	:	$\underline{B}(\underline{A}\ \underline{C}\ D + A\ \underline{C}\ \underline{D} + \underline{A}\ C\ \underline{D})$
Charles' statement	:	$\underline{C}\ (\underline{A}\ \underline{B}\ D + A\ \underline{B}\ \underline{D} + \underline{A}\ B\ \underline{D})$
Davis' statement	:	$A\ \underline{B}\ \underline{C}\ \underline{D}$

where A = Adams did it,
B = Baker did it, etc.

The solution to this problem can probably be derived by reference to the map 11.

(a) From map 11, it is seen that only one of the four statements accuses Baker - single entry in square 2.

Therefore Baker is the guilty man.

(b) Again referring to map 11 it is obvious that Adams is guilty in this case, because, if any three people accuse the fourth person, then that person must be guilty. For instance, in square 4 of map 11, the peripheral information A B C D = 1000; that is, any name entered in this square is accusing Adams. Therefore, because B, C and D are entered, Adams is guilty.

4. Let B = the marble drawn is blue,
R = the marble drawn is red
and W = the marble drawn is white.

First statement is	$B\ R\ \underline{W}$	(1)
Second statement is	$B\ R\ \underline{W} + \underline{B}\ R\ W$	(2)
Third statement is	$\underline{B}\ R\ \underline{W} + \underline{B}\ R\ \underline{W} + \underline{B}\ R\ W$	(3)

Comparing the three equations it is seen that $\underline{B}\ R\ \underline{W}$ is the only term which is present in not more than one equation that is, all the marbles are red.

CHAPTER 2

STEP BY STEP DESIGN OF ABSOLUTE MINIMAL COMBINATIONAL SWITCHING CIRCUITS

DESIGN OF MINIMAL NOR/NAND COMBINATIONAL SWITCHING CIRCUITS.

SUMMARY

An all-algebraic step-by-step method of designing minimal NOR (and NAND) Combinational Switching Circuits is described. The method essentially is one of optimising the algebraic expression of the function to be realised in three steps. Theoretical justification of the design steps is given. Several examples are used to illustrate the method, including a full adder/subtractor unit and a comparator unit.

INTRODUCTION

The design method was developed to allow a set of simple rules to be produced that can be used in the design of N-variable minimal NOR/NAND circuits. Although this approach has been proved to work for three variables (1), it was not possible to test it for a larger number of variables, since no list of minimal NOR circuits of more than three-variables, to the authors' knowledge, has been published.

A minimal NOR/NOR circuit is defined as a circuit that uses the minimum number of modules and the number of connections is a minimum, provided the first condition is satisfied.

Similarly a minimal NOR/NOR expression is defined as one that contains the minimum number of NOR functions and the number of signals in each NOR function is a minimum provided condition 1 is satisfied.

For example:

$$f = \underline{\underline{A + \underline{A}\,B + C}} + \underline{\underline{X + Y + W\,Y}} + \underline{\underline{X + Y + W\,Y}}$$

is not minimal, because the third NOR function $\underline{X + Y + W\,Y}$ is redundant, being a duplicate of the second one, and the signals in the first NOR function can be simplified to $A + B + C$. Similarly, the signals of the second NOR function can be reduced to $X + Y$. Both these simplifications are carried out using basic Boolean theorems.

Since every NOR function is realised by a NOR module, it follows that the direct realisation of a minimal NOR/NOR expression results in a minimal NOR/NOR circuit, if the complements of the input signals are assumed available.

If, on the other hand, the complements of the input signals are assumed not available, then the equation has to be optimised, before it is minimally realised.

For example:

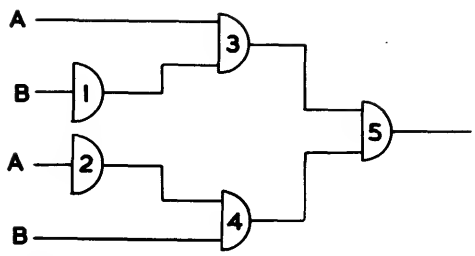
$$f = \underline{\underline{\underline{A} + B}} + \underline{\underline{A + \underline{B}}}$$

is minimal. Realising this equation results in the non-minimal circuit of circuit 1(a), whereas, realising its optimised (non-minimal) form

$$f = \underline{\underline{\underline{A + B} + B}} + \underline{\underline{A + \underline{A} + B}}$$

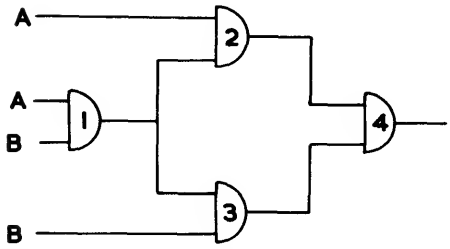
results in a minimal circuit, as shown in circuit 1(b).

The design procedure consists essentially of optimising the algebraic expression of the function to be realised.



CIRCUIT 1a. NON-MINIMAL CIRCUIT REALIZED DIRECTLY FROM MINIMAL NOR/NOR ALGBRAIC EXPRESSION

$\underline{\underline{\underline{A}+B}+\underline{A}+\underline{B}}$



CIRCUIT 1b. MINIMAL CIRCUIT REALIZED DIRECTLY FROM OPTIMAL (NON-MINIMAL) NOR/NOR ALGEBRAIC EXPRESSION

$\underline{\underline{\underline{A+B}+B}+\underline{A}+\underline{A+B}}$

OUTLINE OF THE METHOD

As mentioned above the process of optimisation of the algebraic expression consists of three steps. The fourth and last step in the design procedure deals with the circuit realisation of the optimised form of the expression.

Each step is outlined separately as follows for NOR modules:

STEP 1. DERIVATION OF THE MINIMAL OR/AND EXPRESSION OF THE FUNCTION TO BE REALISED, f

There are several ways of deriving the minimal OR/AND (product of sums) expression of a switching function.

A simple and quick method is to plot the excitation table of the function f, and from it to derive the minimal AND/OR (sum of products) expression for $\underline{f}$, by considering the 0 entries.

For example, let the function to be realised be $f = \underline{A}\,\underline{B} + A\,B\,\underline{C}$. Its excitation table is first plotted - see table 1. All its 0 entries are next included in the minimum number of drop sets, (see index) from which the minimal OR/AND expression of f is derived (equation 1).

$$\underline{f} = \underline{A}\,B + A\,\underline{B} + B\,C \qquad (1)$$

De Morgan's theorem is next applied to equation 1, which results in the minimal OR/AND expression for f (equation 2).

$$f = (A + \underline{B})(\underline{A} + B)(\underline{B} + \underline{C}) \qquad (2)$$

STEP 2. APPLICATION OF THE MERGING PROCESS

In this step two OR functions derived in step 1. are merged, if all but one signal in each two OR functions are the same, and if at least one of the two different signals is in its inverse form. For example:

$$(A + B + C)(A + B + \underline{D})$$

will be merged to $A + B + C\,\underline{D}$

whereas $(A + B + C)(A + B + D)$

will not be merged to $A + B + C\,D$, because both the different signals, namely C and D, are in their true form.

Two OR functions of all inverted terms always merge.

For example:

$(\underline{A} + \underline{B})(\underline{C} + \underline{D})$ merge to

$\underline{A}\,\underline{C} + \underline{A}\,\underline{D} + \underline{B}\,\underline{C} + \underline{B}\,\underline{D}$

Applying the merging process, equation 2 becomes

$$f = (\underline{A} + B)(\underline{B} + A\,\underline{C}) \qquad (3)$$

STEP.3. INTRODUCTION OF THE SUBSTITUTION SIGNALS

The possibility of introducing substitution signals is examined in this step. All the possible substitution signals for every single inverted term and for each product term are noted. If two or more signals can be replaced by the same signal, then they are replaced.

For example:

$$f = (A + \underline{B})(\underline{A} + B)$$

Substitution signal for $\underline{B}$ is $\underline{A}\ \underline{B}$
Substitution signal for $\underline{A}$ is $\underline{A}\ \underline{B}$

Since both $\underline{A}$ and $\underline{B}$ can be replaced by the same substitution signal $\underline{A}\ \underline{B}$ the expression is modified to $f = (\overline{A} + \underline{A}\ \underline{B})(\underline{A}\ \underline{B} + B)$.

Returning to equation 3, the substitution signals for $\underline{A}$ is $\underline{A}\ \underline{B}$, for $\underline{B}$ is $\underline{B}(\underline{A} + C)$ and for $A\ \underline{C}$ are $A.B\ \underline{C}$, $(A + C)\underline{C}$ and $(A + C)B\ \underline{C}$.

Since no two substitution signals are the same, the equation is not modified.

Step.3. of the design procedure completes the optimisation of the function.

STEP.4. CIRCUIT REALISATION

In the final step the optimised form of the function is realised. The following steps are suggested.

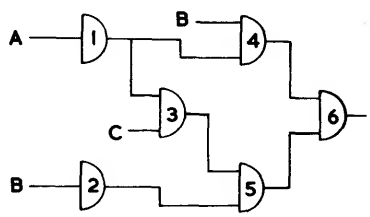
(a) Draw the final module - this is the module generating the actual function, i.e. Module 6, in circuit 2.

(b) Draw a module for each bracket (OR term) in the final form of f. These modules are referred to as driver modules - see circuit 2, modules 4 and 5.

The terms in each bracket specify the input signals to the corresponding driver module.

C \ AB	00	01	11	10
0	1	0	1	0
1	1	0	0	0

TABLE 1. EXCITATION TABLE OF SWITCHING FUNCTION $\underline{A}\ \underline{B} + A\ B\ \underline{C}$



CIRCUIT 2. MINIMAL NOR CIRCUIT REALIZING SWITCHING FUNCTION $\underline{A}\ \underline{B} + A\ B\ \underline{C}$

For example the input signals to driver module 4 corresponding to OR term $(\underline{A} + B)$, are $\underline{A}$ and B. Similarly the input signals to the driver module 5, corresponding to OR term $(\underline{B} + A\,\underline{C})$, are $\underline{B}$ and $A\,\underline{C}$.

(c) The product terms are next generated by what are referred to as product modules. It is helpful at this stage to think of the NOR module as producing the AND function of the complements of its input signals. For example, to generate $A\,\underline{C}$, signals $\underline{A}$ and C are fed to product module 3 of circuit 2.

(d) The inverted terms are generated by simply feeding the corresponding signals to NOR modules. For example, $\underline{A}$ and $\underline{B}$ are obtained from modules 1 and 2 in circuit 1 by feeding into them A and B respectively.

NAND/NAND CIRCUIT REALISATION

To realise a given function using NAND modules, interchange the 'pluses' and 'dots in the original expression. The NOR circuit configuration corresponding to the derived function will realise the initial function, if the NOR modules are replaced by NAND modules. A useful point to bear in mind when transforming Boolean functions is to include all product terms in brackets before transformation. The brackets are not affected by the transformation.

Example

Assume function $f = \underline{A}\,\underline{C} + A\,C$ is to be realised using NAND modules.

The product terms are first included in brackets,

$$f = (\underline{A}\,\underline{C}) + (A\,C).$$

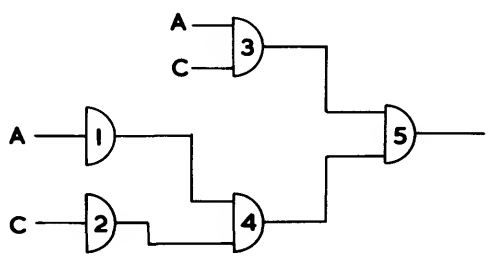
Interchanging the 'pluses' and 'dots' the modified form of the function becomes:

$$f = (\underline{A} + \underline{C})\,(A + C)$$

$$= A\,\underline{A} + A\,\underline{C} + \underline{A}\,C + C\,\underline{C}$$

$$= A\,\underline{C} + \underline{A}\,C$$

The NOR circuit corresponding to this function is shown in circuit 3. If in this circuit configuration the NOR modules are replaced by NAND modules, the function $A\,C + \underline{A}\,\underline{C}$ will be realised.



CIRCUIT 3. MINIMAL NAND CIRCUIT REALIZING SWITCHING FUNCTION $AC+\underline{A}\underline{C}$

DESIGN PROBLEMS

Design Problem 1

Function to be realised

$f = A\,B + \underline{A}\,\underline{B}$ (inclusive OR) ..... (1)

Step. 1. Minimal OR/AND expression of f

From table 2,

$\underline{f} = \underline{A}\,B + A\,\underline{B}$ ..... (2)

Applying De Morgan's Theorem to equation 2,

$f = (A + \underline{B})\,(\underline{A} + B)$ ..... (3)

Step. 2. Merging of OR terms

No merging is possible.

Step. 3. Introduction of substitution signals

Signal $\underline{B}$ in OR term $A + \underline{B}$ can be replaced by substitution signal $\underline{A}\,\underline{B}$.

Signal $\underline{A}$ in OR term $\underline{A} + B$ can also be replaced by substitution signal $\underline{A}\,\underline{B}$.

Therefore equation 3 is modified to

$f = (A + \underline{A}\,\underline{B})\,(\underline{A}\,\underline{B} + B)$ ..... (4)

This is the optimised form of the function.

Step. 4. Circuit Realisation

Circuit 1(b) shows its circuit realisation.

Design Problem 2

Function to be realised

$f = A\,\underline{B} + A\,\underline{C} + \underline{B}\,\underline{C}$ ..... (1)

Step. 1. Minimal OR/ AND form of f

From table 3,

$\underline{f} = \underline{A}\,B + \underline{A}\,C + B\,C$ ..... (2)

Applying De Morgan's Theorem to equation 2

$f = (A + \underline{B})\,(A + \underline{C})\,(\underline{B} + \underline{C})$ ..... (3)

Step 2. Merging of OR terms

OR terms $A + \underline{B}$ and $A + \underline{C}$ are merged

$f = (A + \underline{B}\,\underline{C})\,(\underline{B} + \underline{C})$ (4)

Step.3. Introduction of substitution signals

Product signal $\underline{B}\,\underline{C}$ in OR term $A + \underline{B}\,\underline{C}$ can be replaced by $\underline{A}\,\underline{B}\,\underline{C}$.

Signal $\underline{B}$ in OR term $\underline{B} + \underline{C}$ can be replaced by $\underline{B}\,C$ and $\underline{C}$ by $B\,\underline{C}$.

Since no two substitution signals are the same, equation 4 is in its final optimised form.

Step.4. Circuit Realisation

Circuit 4 shows its circuit realisation.

Design Problem 3.

Function to be realised.

$$f = \underline{A}\,C + A\,\underline{C} + B\,C + \underline{B}\,\underline{C} \quad \ldots\ldots (1)$$

Step.1. Minimal OR/AND expressions of f

From table 4,

$$\underline{f} = \underline{A}\,B\,\underline{C} + A\,\underline{B}\,C \quad \ldots\ldots (2)$$

Applying De Morgan's theorem to equation 2,

$$f = (A + \underline{B} + C)(\underline{A} + B + \underline{C}) \quad \ldots\ldots (3)$$

Step.2. Merging of OR terms

No merging is possible.

Step.3. Introduction of substitution signals

Signal $\underline{B}$ in OR term can be replaced by substitution signal $\underline{B}\,\underline{C}$. The same substitution signal can also be used in lieu of $\underline{C}$ in OR term $\underline{A} + B + \underline{C}$. Therefore the optimised form of the function f is:

$$f = (A + \underline{B}\,\underline{C} + C)(\underline{A} + B + \underline{B}\,\underline{C}) \quad \ldots\ldots (4)$$

Step.4. Circuit Realisation

Its circuit realisation is shown in circuit 5.

Design Problem 4

Function to be realised

$$f = \underline{A}\,B\,C + \underline{B}\,\underline{C} \quad \ldots\ldots (1)$$

Step.1. Minimal OR/AND expressions of f

From table 5,

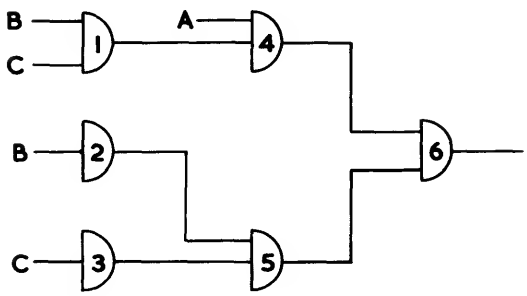
$$\underline{f} = B\,\underline{C} + A\,C + \underline{B}\,C \quad \ldots\ldots (2)$$

B \ A	0	1
0	1	0
1	0	1

TABLE 2. EXCITATION TABLE OF SWITCHING FUNCTION $AB + \underline{A}\,\underline{B}$

C \ AB	00	01	11	10
0	1	0	1	1
1	0	0	0	1

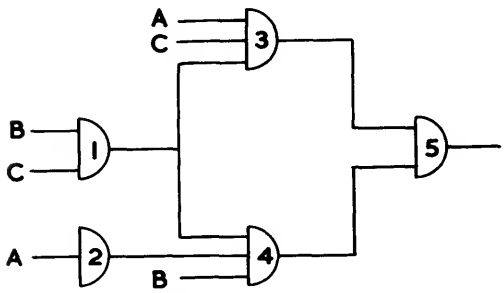
TABLE 3. EXCITATION TABLE OF SWITCHING FUNCTION $A\underline{B} + A\underline{C} + \underline{B}\,\underline{C}$



CIRCUIT 4. MINIMAL NOR CIRCUIT REALIZATION OF SWITCHING FUNCTION $A\underline{B} + A\underline{C} + \underline{B}\,\underline{C}$

C \ AB	00	01	11	10
0	1	0	1	1
1	1	1	1	0

TABLE 4. EXCITATION TABLE OF SWITCHING FUNCTION $\underline{A}C + A\underline{C} + BC + \underline{B}\,\underline{C}$



CIRCUIT 5. MINIMAL NOR CIRCUIT REALIZING SWITCHING FUNCTION $\underline{A}C + A\underline{C} + BC + \underline{B}\,\underline{C}$

C \ AB	00	01	11	10
0	1	0	0	1
1	0	1	0	0

TABLE 5. EXCITATION TABLE OF SWITCHING FUNCTION $\underline{A}BC + \underline{B}\,\underline{C}$

Applying De Morgan's theorem to equation 2,

$$f = (\underline{B} + C)\,(\underline{A} + \underline{C})\,(B + \underline{C}) \quad \ldots\ldots (3)$$

Step.2. Merging of OR terms

$$f = (\underline{B} + C)\,(\underline{C} + \underline{A}\,B) \quad \ldots\ldots (4)$$

Step.3. Introduction of substitution signals

$\underline{B}$ may be replaced by $\underline{B}\,\underline{C}$. Substitution signal $\underline{B}\,\underline{C}$ may also be used in lieu of signal $\underline{C}$ in OR term $\underline{C} + \underline{A}\,B$. Therefore equation 4 is modified to

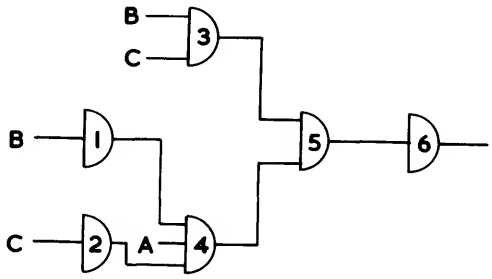
$$f = (\underline{B}\,\underline{C} + C)\,(\underline{B}\,\underline{C} + \underline{A}\,B) \quad \ldots\ldots (5)$$

But the two OR terms can now be merged resulting in equation 6.

$$f = \underline{B}\,\underline{C} + \underline{A}\,B\,C \quad \ldots\ldots (6)$$

Step.4. Circuit Realisation

Circuit 6 shows its minimal realisation.



CIRCUIT 6. MINIMAL NOR CIRCUIT REALIZATION OF SWITCHING FUNCTION $\underline{A}\,B\,C + \underline{B}\,\underline{C}$

Design Problem 5

A minimal full-adder/full-subtractor unit is to be realised using NOR modules. Its truth table is shown in table 6.

Table 6 reveals that two outputs of the required unit, namely the sum (S) and the difference (D) are the same. A circuit generating this common output signal, S, will first be realised.

A. Generation of the Sum/Difference Signal

Step.1. Minimal OR/AND expression of the Sum/Difference signal S

From table 7,

$$\underline{S} = \underline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C + A\,B\,\underline{C} \quad \ldots\ldots (1)$$

Applying De Morgans theorem to equation (1),

$$S = (A + B + C)\,(\underline{A} + B + \underline{C})\,(A + \underline{B} + \underline{C})\,(\underline{A} + \underline{B} + C) \quad \ldots\ldots (2)$$

Step.2. Merging of OR terms

In equation (2) only the first bracket can be merged with any one of the other brackets, since any two of the last three brackets differ by more than one variable. Merging the two first brackets, results in,

$$S = (B + \underline{A}\,C + A\,\underline{C})\,(A + \underline{B} + \underline{C})\,(\underline{A} + \underline{B} + C) \quad \ldots\ldots (3)$$

Step.3. Introduction of substitution signals

Substitution signals $\underline{A}\,\underline{B}\,C$ and $A\,\underline{B}\,\underline{C}$ may be used to replace product signals $\underline{A}\,C$ and $A\,\underline{C}$ respectively of the first bracket.

The same two substitution signals can be used in lieu of the $\underline{B}$ signals in the second and third bracket respectively of equation (3). The $\underline{C}$ and $\underline{A}$ signals can be replaced by $\underline{A}\,\underline{C}$.

$$S = (B + \underline{A}\,\underline{B}\,C + A\,\underline{B}\,\underline{C})\,(A + \underline{A}\,\underline{B}\,C + \underline{A}\,\underline{C})(\underline{A}\,\underline{C} + A\,\underline{B}\,\underline{C} + C) \quad \ldots\ldots (4)$$

Consider signals A and C in the product terms $A\,\underline{B}\,\underline{C}$ and $\underline{A}\,\underline{B}\,C$ respectively. Due to the presence of $\underline{A}\,\underline{C}$ in equation 4, signal A in the term $A\,\underline{B}\,\underline{C}$ can be replaced by $(A + C)$. Similarly, the $\overline{C}$ signal in $\underline{A}\,\underline{B}\,C$ is replaced by $(A + C)$

The optimised form of the equation therefore is:

$$S = (B + \underline{A}\,\underline{B}\,(A + C) + (A + C)\,\underline{B}\,\underline{C})\;(A + \underline{A}\,\underline{B}\,(A + C) + \underline{A}\,\underline{C})\;(\underline{A}\,\underline{C} + \underline{B}\,\underline{C}\,(A + C) + C) \quad \ldots\ldots (5)$$

Step.4. Circuit Realisation

Circuit 7 (NOR modules 1 - 7 only) shows the direct realisation of the optimised equation for the SUM/DIFFERENCE signal.

B. Generation of the Carry Out Signal

The steady state output signals of modules (1-7) of circuit 7 are next examined with a view to using some of these outputs to generate the required carry out signal.

These outputs are listed below, using some of the modules (1-7) in the required circuit. For that the steady state output signals of modules 1 - 7 are noted, as below:

Output of Module	1	$S1 = \underline{A}\,\underline{B}\,C$
" " "	2	$S2 = \overline{A}\,\overline{C}$
" " "	3	$S3 = \overline{A}\,\overline{B}\,C$
" " "	4	$S4 = \underline{A}\,\overline{B}\,\overline{C}$
" " "	5	$S5 = \overline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C$
" " "	6	$S6 = \overline{A}\,\overline{B}\,\overline{C}$
" " "	7	$S7 = \underline{A}\,\underline{B}\,\overline{\underline{C}} + A\,\underline{B}\,C + \underline{A}\,B\,C + A\,B\,\underline{C}$.

Comparing steady state signals S1 - S7 with table 8, it is noted that S1, S2 and S3 determine the minimum number of drop sets that include all the 0 entries in the table. Therefore:

$$\underline{K} = S1 + S2 + S3 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

This means that if S1, S2 and S3 are fed into a module, its output will be K, that is, output of module 8, in circuit 7. This is denoted by S.8.

C. Generation of the Borrow Out Signal

Similarly comparing steady signals S1 - S8 with table 9, it is seen that when signals S3, S5 and S6 are fed into a module, that module will generate the borrow out signal. Thus, the output of module 9 is the required signal.

Design Problem 6.

A minimal NOR comparator unit to compare the magnitude of two n-bit binary numbers, a and b that gives three output signals to indicate

(i) when a equals b,
(ii) when a is greater than b, or
(iii) when a is less than b,

is to be designed.

Model Solution

Let a = A B C D ..... (in binary digits)
and b = K L M N ..... (" " ")

where A and K are the most significant digits.

Because of the required variable capacity of the comparator, unit construction is chosen. The first unit, see diagram 1, compares the two most significant binary digits of the binary numbers a and b.

A INPUT	B INPUT	C OLD CARRY OLD BORROW	S SUM	K NEW CARRY	D DIFFERENCE	P NEW BORROW
0	0	0	0	0	0	0
1	0	0	1	0	1	0
0	1	0	1	0	1	1
0	0	1	1	0	1	1
1	0	1	0	1	0	0
1	1	0	0	1	0	0
0	1	1	0	1	0	1
1	1	1	1	1	1	1

TABLE 6. THE TRUTH TABLE FOR A FULL-ADDER / FULL-SUBTRACTOR UNIT

C \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

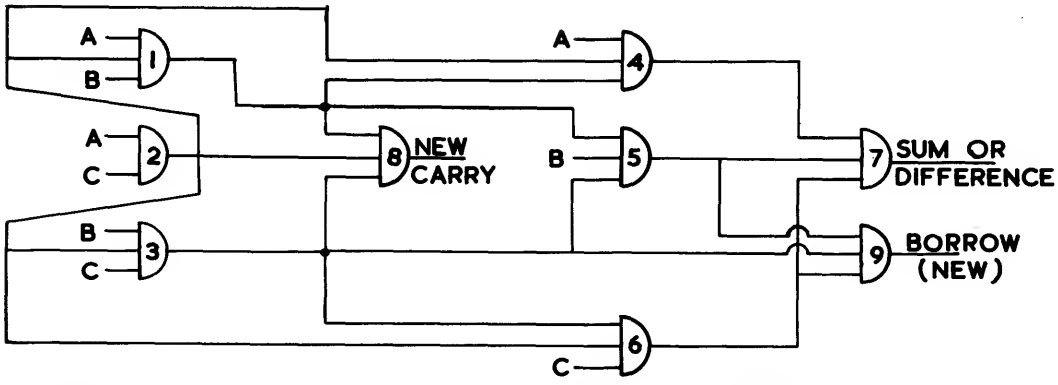
TABLE 7. EXCITATION TABLE OF THE SUM/DIFFERENCE SIGNAL S

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

TABLE 8. EXCITATION TABLE OF THE NEW CARRY SIGNAL K

C \ AB	00	01	11	10
0	0	1	0	0
1	1	1	1	0

TABLE 9. EXCITATION TABLE OF THE NEW BORROW SIGNAL P



CIRCUIT 7. MINIMAL NOR CIRCUIT OF A FULL-ADDER / FULL-SUBTRACTOR UNIT

If $Q1 = A\,\underline{K}$. $Q2 = \underline{A}\,K$ and $Q3 = A\,K + \underline{A}\,\underline{K}$

then,

Q1 = 1 if A is greater than K (i.e. if A = 1) and (K = 0)., indicating that a is greater than b.

Q2 = 1 if K is greater than A (i.e. A = 0 and K = 1) indicating that b is greater than a.

Q3 = 1 if A = K (i.e. when A = K = 0 or 1) indicating that a = b.

Note that only one output signal in unit 1 at any one time equals 1. If either Q1 or Q2 equals 1, then all the outputs of unit 2 are zeros, since they are gated with Q3. Similarly because signal Q3R3 is gated with the outputs of unit 3, they will also all be equal to zero.

If now Q1 = Q2 = 0 then the second unit will produce an output, since Q3 = 1. If B and L are not equal either Q3R1 or Q3R2 will equal to 1 with Q3R3 = 0. If however, A B = K L, then Q3R3 = 1 allowing the result of the comparison of the third most significant digits, namely, C and M to appear at the output of unit 3.

Therefore:

X1 = Q1 + Q3R1 + (Q3R3)S1+ = 1 if a is greater than b.

X2 = Q2 + Q3R2 + (Q3R3)S2+ = 1 if a is less than b and

X3 = X1. X2 if a = b.

(see diagram 2.)

The NOR circuits of units 1 and 2 are shown in circuit 8.

References.

1. Zissos D, "A List of Minimal NOR/NAND Combinational Logic Circuits".

A.T.E., Journal, 20, No.2. March, 1964.

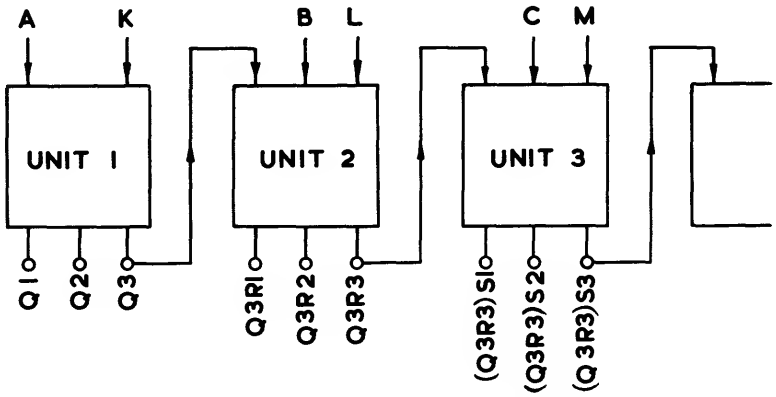


DIAGRAM 1. BLOCK DIAGRAM OF COMPARATOR UNIT (DESIGN PROBLEM 6)

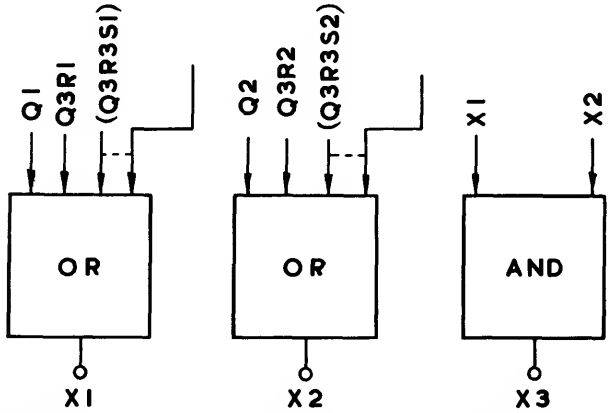
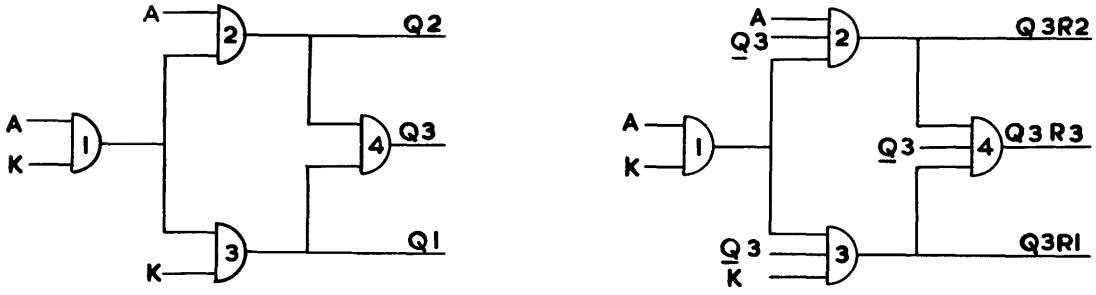


DIAGRAM 2. BLOCK DIAGRAM OF OUTPUT UNIT OF THE COMPARATOR



CIRCUIT 8. MINIMAL NOR CIRCUITS OF UNITS 1 AND 2 OF DIAGRAM 1

Classification of Boolean Functions by Index Numbers

The expression to be realised is first expressed in its minimal 'AND- OR' form, i.e. as a sum of products. The number index is then derived directly from the expression by assigning +1, +2, +4, -1, -2, and -4 to A, B, C, $\underline{A}$, $\underline{B}$, and $\underline{C}$ respectively. The numbers corresponding to all the letters in a given product are added algebraically to give a single number per product term. Each number thus derived is separated (by a stroke) from the other numbers corresponding to the remaining product terms. The numbers are finally arranged so that reading from left to right they increase algebraically.

Consider the expression:

$$f = \underline{A} + A\,\underline{B}\,\underline{C}$$

The expression is first simplified algebraically to:

$$f = \underline{A} + \underline{B}\,\underline{C}$$

The specified numerical values are next assigned to each letter:

$$\underline{A} = -1 \quad \underline{B}\,\underline{C} = -2\ -4 = -6$$

$\therefore$ index number of f = -1/-6 = -6/-1

Outline of the method

NOR - NOR Circuit Realisations for Negative Signals

By means of its index number the function to be realised is readily located in the table. The number in the third column specifies the circuit, and the fourth column indicates what changes, if any, must be made in the input signals of the reference circuit to realise the function under consideration.

Example

Assume it is required to realise $f = \underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + \underline{A}\,B\,C$

Its index number is -7/-1/+5. Referring to the table we see that the circuit realisation of this function is the same as the one for $\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C$, i.e. circuit 2, provided the A and B input signals are interchanged.
Note: The same circuit produces the NAND-NAND function of the given expression for positive signals.

NAND-NAND Circuit Realisations for Negative Signals

To realise a given function using NAND modules, interchange the 'pluses' and 'points' in the original expression. The NOR circuit configurations corresponding to the derived functions will realise the initial functions if the NOR modules are replaced by NAND modules. A useful point to bear in mind when transforming Boolean functions, is to include all product terms which were in brackets before the transformation. The brackets are not affected by the transformation.

Example

Assume $f = (\underline{A}.\underline{C}) + (A.C)$ is to be realised using NAND modules.

$$f2 = \underline{f} = (\underline{A} + \underline{C})\ .\ (A + C) = A\,\underline{A} + A.\underline{C} + \underline{A}\,C + C.\underline{C} = A.\underline{C} + \underline{A}.C \text{ (index -3/+3/a)}$$

If the NOR gates in circuit 64 are replaced by NAND gates the function $\underline{A}\,\underline{C} + A\,C$ is realised.

The rule then becomes: Transform original expression to f2 by interchanging the 'pluses' and 'points' in it. Use the circuit configuration corresponding to f2 with NAND modules to produce f.

INDEX NUMBER	MINIMAL "AND - OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-7/-1	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C}$	1	
-7/-1/+3	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C$	2	
-7/-1/+3/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	3	
-7/-1/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + \underline{A}\,B\,C$	2	B A C
-7	$\underline{A}\,\underline{B}\,\underline{C}$	4	
-7/+3/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B$	5	
-7/+3/b	$\underline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C$	1	
-7/+3/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C$	6	
-7/+3/+5/b	$\underline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	2	C B A
-7/+3/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C + B\,C$	7	
-7/+3/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + B\,C$	6	B A C
-7/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,C$	5	A C B
-7/+5/b	$\underline{A}\,\underline{B}\,\underline{C} + \underline{A}\,B\,C$	1	C B A
-7/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,C + B\,C$	6	C B A
-7/+6	$\underline{A}\,\underline{B}\,\underline{C} + B\,C$	5	C B A
-7/+7	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,C$	8	
-6/-5/-3	$\underline{A}\,\underline{B} + \underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	9	
-6/-5/-3/+7	$\underline{A}\,\underline{B} + \underline{A}\,\underline{C} + \underline{B}\,\underline{C} + A\,B\,C$	10	
-6/-5	$\underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	11	
-6/-5/+5	$A\,C + \underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	12	
-6/-5/+6	$\underline{A}\,\underline{C} + B\,C + \underline{B}\,\underline{C}$	12	B A C
-6/-5/+7	$\underline{A}\,\underline{C} + \underline{B}\,\underline{C} + A\,B\,C$	13	
-6/-3/-1	$A\,C + \underline{B}\,\underline{C} + A\,\underline{B}$	14	
-6/-3/-1/+5	$A\,\underline{B} + A\,\underline{C} + \underline{B}\,\underline{C} + \underline{A}\,B\,C$	15	
-6/-3/a	$A\,\underline{C} + \underline{B}\,\underline{C}$	16	
-6/-3/b	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C}$	11	A C B
-6/-3/+3/a	$A\,\underline{C} + \underline{A}\,C + \underline{B}\,\underline{C}$	17	
-6/-3/+3/b	$A\,B + \underline{A}\,\underline{B} + \underline{B}\,\underline{C}$	12	A C B
-6/-3/+3/+6	$\underline{A}\,C + A\,\underline{C} + B\,C + \underline{B}\,\underline{C}$	18	
-6/-3/+5	$A\,\underline{C} + \underline{A}\,B\,C + \underline{B}\,\underline{C}$	19	
-6/-3/+6/a	$A\,\underline{C} + \underline{B}\,\underline{C} + B\,C$	20	

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-6/-3/+6/b	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C} + B\,C$	12	C A B
-6/-3/+7	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C} + A\,B\,C$	13	A C B
-6/-1/a	$\underline{A} + \underline{B}\,\underline{C}$	21	
-6/-1/b	$A\,\underline{B} + \underline{B}\,\underline{C}$	16	A C B
-6/-1/+1	$A\,\underline{B} + \underline{A}\,B + \underline{B}\,\underline{C}$	17	A C B
-6/-1/+1/+6	$\underline{A}\,B + B\,C + A\,\underline{B} + \underline{B}\,\underline{C}$	18	A C B
-6/-1/+5	$A\,\underline{B} + \underline{A}\,B\,C + \underline{B}\,\underline{C}$	19	A C B
-6/-1/+6/a	$\underline{A} + \underline{B}\,\underline{C} + B\,C$	22	
-6/-1/+6/b	$A\,\underline{B} + \underline{B}\,\underline{C} + B\,C$	20	A C B
-6	$\underline{B}\,\underline{C}$	23	
-6/+1/a	$A + \underline{B}\,\underline{C}$	24	
-6/+1/b	$\underline{A}\,B + \underline{B}\,\underline{C}$	25	
-6/+1/+5	$A\,C + \underline{A}\,B + \underline{B}\,\underline{C}$	26	
-6/+1/+6/a	$\underline{A}\,B + \underline{B}\,\underline{C} + B\,C$	12	B A C
-6/+1/+6/b	$A + \underline{B}\,\underline{C} + B\,C$	27	
-6/+3/a	$A\,B + \underline{B}\,\underline{C}$	28	
-6/+3/b	$\underline{A}\,C + \underline{B}\,\underline{C}$	25	A C B
-6/+3/+3	$A\,B + \underline{A}\,C + \underline{B}\,\underline{C}$	26	A C B
-6/+3/+6/a	$A\,B + B\,C + \underline{B}\,\underline{C}$	20	A B C
-6/+3/+6/b	$\underline{A}\,C + B\,C + \underline{B}\,\underline{C}$	12	B A C
-6/+5/a	$\underline{A}\,B\,C + \underline{B}\,\underline{C}$	29	
-6/+5/b	$A\,C + \underline{B}\,\underline{C}$	28	A C B
-6/+5/+6	$A\,C + B\,C + \underline{B}\,\underline{C}$	20	A C B
-6/+6	$\underline{B}\,\underline{C} + B\,C$	30	
-6/+7	$\underline{B}\,\underline{C} + A\,B\,C$	31	
-5/-3/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C}$	32	
-5/-3/b	$\underline{A}\,\underline{C} + \underline{A}\,\underline{B}$	11	C B A
-5/-3/+1	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	33	
-5/-3/+1/+7	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	34	
-5/-3/+3	$A\,B + \underline{A}\,\underline{B} + \underline{A}\,\underline{C}$	12	B C A
-5/-3/+5	$A\,C + \underline{A}\,\underline{C} + \underline{A}\,\underline{B}$	12	C B A
-5/-3/+7/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + A\,B\,C$	35	
-5/-3/+7/b	$\underline{A}\,\underline{C} + \underline{A}\,\underline{B} + A\,B\,C$	13	C B A
-5/-2/a	$\underline{A}\,\underline{C} + B\,\underline{C}$	16	B A C
-5/-2/b	$\underline{B} + \underline{A}\,\underline{C}$	21	B A C

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-5/-2/+1	$\underline{A}B + \underline{A}\,\underline{C} + B\,\underline{C}$	14	B C A
-5/-2/+1/+3	$\underline{A}B + B\,\underline{C} + \underline{A}\,\underline{C} + A\,\underline{B}\,C$	15	B A C
-5/-2/+2	$\underline{A}\,\underline{C} + B\,\underline{C} + \underline{B}\,C$	17	B A C
-5/-2/+3	$\underline{A}\,\underline{C} + B\,\underline{C} + A\,\underline{B}\,C$	19	B A C
-5/-2/+5/a	$A\,C + \underline{A}\,\underline{C} + B\,\underline{C}$	20	B A C
-5/-2/+5/b	$\underline{B} + \underline{A}\,\underline{C} + A\,C$	22	B A C
-5/-1	$A\,\underline{B} + \underline{A}\,\underline{C}$	25	B A C
-5/-1/+1	$\underline{A}\,\underline{C} + A\,\underline{B} + \underline{A}\,B$	17	B C A
-5/-1/+1/+5	$A\,\underline{B} + A\,C + \underline{A}\,B + \underline{A}\,\underline{C}$	18	B C A
-5/-1/+5	$A\,\underline{B} + A\,C + \underline{A}\,\underline{C}$	12	A B C
-5/-1/+6	$A\,\underline{B} + \underline{A}\,\underline{C} + B\,C$	26	B A C
-5/a	$A\,\underline{B}\,\underline{C}$	36	
-5/b	$\underline{A}\,\underline{C}$	23	B A C
-5/+1/a	$\underline{A}B + A\,\underline{B}\,\underline{C}$	37	
-5/+1/b	$\underline{A}B + \underline{A}\,\underline{C}$	16	B C A
-5/+1/c	$A\,\underline{B}\,\underline{C} + \underline{A}\,\underline{B}\,C$	32	A C B
-5/+1/+3/a	$\underline{A}B + \underline{A}\,C + A\,\underline{B}\,\underline{C}$	38	
-5/+1/+3/b	$\underline{A}B + \underline{A}\,\underline{C} + A\,\underline{B}\,C$	19	B C A
-5/+1/+3/+6	$\underline{A}\,C + B\,C + \underline{A}B + A\,\underline{B}\,\underline{C}$	39	
-5/+1/+5	$\underline{A}B + \underline{A}\,\underline{C} + A\,C$	20	B C A
-5/+1/+6	$\underline{A}B + A\,\underline{B}\,\underline{C} + B\,C$	40	
-5/+1/+7	$A\,\underline{B}\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	35	A C B
-5/+2/a	$\underline{A}\,\underline{C} + B$	24	B A C
-5/+2/b	$\underline{A}\,\underline{C} + \underline{B}\,C$	25	B C A
-5/+2/+3	$A\,B + \underline{A}\,\underline{C} + \underline{B}\,C$	26	B C A
-5/+2/+5/a	$A\,C + \underline{A}\,\underline{C} + \underline{B}\,C$	12	B C A
-5/+2/+5/b	$A\,C + \underline{A}\,\underline{C} + B$	27	B A C
-5/+3/a	$A\,\underline{B}\,C + \underline{A}\,\underline{C}$	29	B A C
-5/+3/b	$A\,\underline{B}\,\underline{C} + \underline{A}\,C$	37	A C B
-5/+3/c	$A\,B + \underline{A}\,\underline{C}$	28	B A C
-5/+3/+5	$A\,B + A\,C + \underline{A}\,\underline{C}$	20	B A C
-5/+3/+6	$\underline{A}\,C + A\,\underline{B}\,\underline{C} + B\,C$	40	A C B
-5/+5/a	$\underline{A}\,B\,C + A\,\underline{B}\,\underline{C}$	41	
-5/+5/b	$A\,C + \underline{A}\,\underline{C}$	30	B A C
-5/+5/+6	$A\,C + B\,C + \underline{A}\,\underline{C}$	20	B C A

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-5/+6/a	$A\,\underline{B}\,\underline{C} + B\,C$	42	
-5/+6/b	$\underline{A}\,\underline{C} + B\,C$	28	B C A
-5/+7/a	$A\,\underline{B}\,\underline{C} + A\,B\,C$	43	
-5/+7/b	$\underline{A}\,\underline{C} + A\,B\,C$	31	B A C
-4/-3	$\underline{A}\,\underline{B} + \underline{C}$	21	C B A
-4/-3/+3	$A\,B + \underline{A}\,\underline{B} + \underline{C}$	22	C B A
-4/-2/-1	$\underline{A} + \underline{B} + \underline{C}$	44	
-4/-2	$\underline{B} + \underline{C}$	45	
-4/-2/+1	$A + \underline{B} + \underline{C}$	46	
-4/-1/a	$A\,\underline{B} + \underline{C}$	47	
-4/-1/b	$\underline{A} + \underline{C}$	45	B A C
-4/-1/+1	$A\,\underline{B} + \underline{A}\,B + \underline{C}$	48	
-4/-1/+2	$\underline{A} + B + \underline{C}$	46	B A C
-4	$\underline{C}$	49	
-4/+1/a	$A + \underline{C}$	50	
-4/+1/b	$\underline{A}\,B + \underline{C}$	47	B A C
-4/+1/+2	$A + B + \underline{C}$	51	
-4/+2	$B + \underline{C}$	50	B A C
-4/+3	$A\,B + \underline{C}$	52	
-3/-3	$A\,\underline{C} + \underline{A}\,\underline{B}$	25	C A B
-3/-3/+3/a	$A\,\underline{C} + \underline{A}\,\underline{B} + \underline{A}\,C$	17	A B C
-3/-3/+3/b	$A\,B + \underline{A}\,\underline{B} + A\,\underline{C}$	12	A C B
-3/-3/+3/+3	$A\,B + A\,\underline{C} + \underline{A}\,\underline{B} + \underline{A}\,C$	18	C B A
-3/-3/+6	$\underline{A}\,\underline{B} + A\,\underline{C} + B\,C$	26	C A B
-3/-2/a	$A\,\underline{C} + B\,\underline{C}$	53	
-3/-2/b	$A\,\underline{C} + \underline{B}$	47	A C B
-3/-2/c	$\underline{A}\,\underline{B} + B\,\underline{C}$	25	C B A
-3/-2/+1	$A\,\underline{C} + B\,\underline{C} + \underline{A}\,\underline{B}\,C$	38	C B A
-3/-2/+1/+3	$A\,\underline{C} + B\,\underline{C} + A\,B + \underline{A}\,\underline{B}\,C$	39	C B A
-3/-2/+2/a	$A\,\underline{C} + B\,\underline{C} + \underline{B}\,C$	54	
-3/-2/+2/b	$\underline{A}\,\underline{B} + B\,\underline{C} + \underline{B}\,C$	17	C A B
-3/-2/+2/+3	$A\,B + B\,\underline{C} + \underline{A}\,\underline{B} + \underline{B}\,C$	18	C A B
-3/-2/+3/a	$A\,\underline{C} + B\,\underline{C} + A\,B$	55	
-3/-2/+3/b	$A\,B + \underline{A}\,\underline{B} + B\,\underline{C}$	12	
-3/-2/+3/c	$A\,\underline{C} + \underline{A}\,C + \underline{B}$	48	A C B
-3/-2/+3/d	$A\,\underline{C} + \underline{A}\,C + B\,\underline{C}$	54	B A C
-3/-2/+5	$\underline{A}\,\underline{B} + A\,C + B\,\underline{C}$	26	C B A
-3/-1/a	$A\,\underline{B} + A\,\underline{C}$	56	

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-3/-1/b	$A\,\underline{B} + \underline{A}\,B\,\underline{C}$	37	B A C
-3/-1/c	$\underline{A}\,\underline{B} + A\,B\,\underline{C}$	29	C B A
-3/-1/+1	$A\,\underline{B} + \underline{A}\,B + A\,\underline{C}$	57	
-3/-1/+2/a	$\underline{A}\,\underline{B} + A\,B\,\underline{C} + \underline{B}\,C$	19	C A B
-3/-1/+2/b	$A\,\underline{B} + \underline{B}\,C + \underline{A}\,B\,\underline{C}$	38	B A C
-3/-1/+2/+3/a	$\underline{A}\,\underline{B} + A\,B\,\underline{C} + \underline{A}\,C + \underline{B}\,C$	15	C B A
-3/-1/+2/+5	$A\,\underline{B} + \underline{B}\,C + A\,C + \underline{A}\,B\,\underline{C}$	39	B A C
-3/-1/+3/a	$A\,\underline{C} + A\,\underline{B} + \underline{A}\,C$	57	A C B
-3/-1/+3/b	$\underline{A}\,\underline{B} + \underline{A}\,C + A\,B\,\underline{C}$	19	C B A
-3/-1/+5/a	$A\,\underline{C} + A\,\underline{B} + \underline{A}\,B\,C$	58	
-3/-1/+5/b	$A\,\underline{B} + \underline{A}\,B\,\underline{C} + A\,C$	40	B A C
-3/a	$A\,\underline{C}$	59	
-3/b	$\underline{A}\,B\,\underline{C}$	36	B A C
-3/c	$\underline{A}\,\underline{B}$	23	C B A
-3/+1/a	$A\,\underline{C} + \underline{A}\,B$	60	
-3/+1/b	$\underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	32	B C A
-3/+1/c	$A\,\underline{C} + \underline{A}\,\underline{B}\,C$	37	C A B
-3/+1/+2	$A\,\underline{C} + \underline{B}\,C + \underline{A}\,B$	61	
-3/+1/+3/a	$A\,\underline{C} + A\,B + \underline{A}\,\underline{B}\,C$	40	C A B
-3/+1/+3/b	$\underline{A}\,B + \underline{A}\,C + A\,\underline{C}$	54	B C A
-3/+1/+7	$\underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	35	C B A
-3/+2/a	$B + A\,\underline{C}$	62	
-3/+2/b	$\underline{A}\,B\,\underline{C} + \underline{B}\,C$	37	B C A
-3/+2/c	$A\,\underline{C} + \underline{B}\,C$	60	C A B
-3/+2/d	$\underline{A}\,\underline{B} + \underline{B}\,C$	16	C A B
-3/+2/+3/a	$A\,\underline{C} + \underline{A}\,C + B$	63	
-3/+2/+3/b	$A\,\underline{C} + \underline{B}\,C + \underline{A}\,C$	57	C A B
-3/+2/+3/c	$\underline{A}\,\underline{B} + \underline{B}\,C + A\,B$	20	C A B
-3/+2/+3/d	$\underline{A}\,\underline{B} + \underline{B}\,C + \underline{A}\,C$	14	C A B
-3/+2/+5	$A\,C + \underline{B}\,C + \underline{A}\,B\,\underline{C}$	40	B C A
-3/+3/a	$A\,\underline{C} + \underline{A}\,C$	64	
-3/+3/b	$A\,B + A\,\underline{C}$	65	
-3/+3/c	$A\,B + \underline{A}\,\underline{B}$	30	C B A
-3/+3/d	$\underline{A}\,\underline{B} + \underline{A}\,C$	16	C B A
-3/+3/c	$A\,\underline{B}\,C + \underline{A}\,B\,\underline{C}$	41	B A C
-3/+3/+3/a	$A\,\underline{C} + \underline{A}\,C + A\,B$	66	

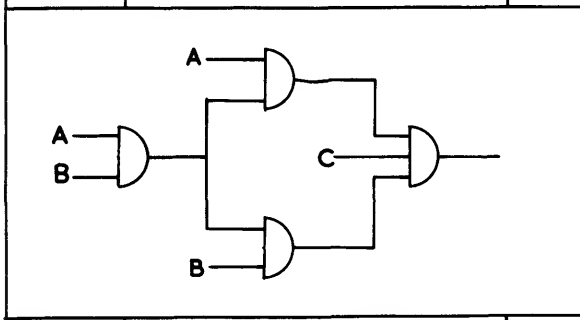
INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-3/+3/+3/b	$\underline{A}\,\underline{B} + \underline{A}\,C + A\,B$	20	C B A
-3/+3/+4	$\underline{A}\,\underline{B} + A\,B + C$	27	C B A
-3/+3/+5	$\underline{A}\,\underline{B} + A\,B + A\,C$	20	C A B
-3/+3/+6/a	$A\,B + \underline{A}\,\underline{B} + B\,C$	20	C B A
-3/+3/+6/b	$A\,\underline{C} + \underline{A}\,C + B\,C$	66	C B A
-3/+4	$\underline{A}\,\underline{B} + C$	24	C B A
-3/+5/a	$\underline{A}\,B\,C + A\,\underline{C}$	67	
-3/+5/b	$\underline{A}\,\underline{B} + A\,C$	28	C A B
-3/+5/c	$\underline{A}\,B\,\underline{C} + A\,C$	42	B A C
-3/+6/a	$A\,\underline{C} + B\,C$	68	
-3/+6/b	$\underline{A}\,\underline{B} + B\,C$	28	C B A
-3/+7/a	$\underline{A}\,\underline{B} + A\,B\,C$	31	C B A
-3/+7/b	$A\,B\,C + \underline{A}\,B\,\underline{C}$	43	B A C
-2/-1/a	$A\,\underline{B} + B\,\underline{C}$	60	B A C
-2/-1/b	$\underline{A} + B\,C$	47	B C A
-2/-1/c	$\underline{A} + \underline{B}$	45	C B A
-2/-1/+1	$A\,\underline{B} + \underline{A}\,B + B\,\underline{C}$	57	B A C
-2/-1/+2/a	$A\,\underline{B} + B\,\underline{C} + \underline{B}\,C$	54	A C B
-2/-1/+2/b	$\underline{A} + B\,\underline{C} + \underline{B}\,C$	48	B C A
-2/-1/+3	$A\,\underline{B} + \underline{A}\,C + B\,\underline{C}$	61	B A C
-2/-1/+4	$\underline{A} + \underline{B} + C$	46	C B A
-2/a	$\underline{B}$	49	- C B
-2/b	$B\,\underline{C}$	59	B - C
-2/+1/a	$\underline{A}\,B + B\,\underline{C}$	56	B A C
-2/+1/b	$\underline{A}\,\underline{B}\,C + B\,\underline{C}$	37	C B A
-2/+1/c	$A + B\,\underline{C}$	62	B A C
-2/+1/d	$A + \underline{B}$	50	- C B
-2/+1/+2/a	$\underline{A}\,B + B\,\underline{C} + \underline{B}\,C$	57	B C A
-2/+1/+2/b	$A + B\,\underline{C} + \underline{B}\,C$	63	B A C
-2/+1/+2/c	$A\,\underline{B} + \underline{B}\,C + B\,\underline{C}$	54	A C B
-2/+1/+3/a	$A\,B + B\,\underline{C} + \underline{A}\,\underline{B}\,C$	40	C B A
-2/+1/+3/b	$\underline{A}\,B + A\,\underline{B}\,C + B\,\underline{C}$	58	B A C
-2/+1/+4	$A + \underline{B} + C$	51	A C B

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF. CCT TO READ.
-2/+2	$B\underline{C} + \underline{B}C$	64	B - C
-2/+2/+3/a	$AB + B\underline{C} + \underline{B}C$	66	B A C
-2/+2/+3/b	$B\underline{C} + \underline{B}C + \underline{A}C$	57	C B A
-2/+2/+5	$AC + B\underline{C} + \underline{B}C$	66	C A B
-2/+3/a	$A\underline{B}C + B\underline{C}$	67	B A C
-2/+3/b	$\underline{A}C + B\underline{C}$	60	C B A
-2/+3/c	$AB + B\underline{C}$	65	B A C
-2/+3/d	$\underline{B} + \underline{A}C$	47	C A B
-2/+4	$\underline{B} + C$	50	C - B
-2/+5/a	$B\underline{C} + AC$	68	B A C
-2/+5/b	$\underline{B} + AC$	52	A C B
-1/a	$AB\underline{C}$	69	
-1/b	$A\underline{B}$	59	A - B
-1/c	$\underline{A}$	49	- - A
-1/+1/a	$AB\underline{C} + \underline{A}\underline{B}C$	41	C B A
-1/+1/b	$A\underline{B} + \underline{A}B$	64	A C B
-1/+1/+2	$A\underline{B} + \underline{A}B + \underline{B}C$	54	C A B
-1/+1/+3	$A\underline{B} + \underline{A}B + \underline{A}C$	54	C B A
-1/+1/+4	$A\underline{B} + \underline{A}B + C$	63	A C B
-1/+1/+5	$A\underline{B} + \underline{A}B + AC$	66	A C B
-1/+1/+6	$A\underline{B} + \underline{A}B + BC$	66	B C A
-1/+2/a	$AB\underline{C} + \underline{B}C$	67	C A B
-1/+2/b	$A\underline{B} + \underline{B}C$	53	A C B
-1/+2/c	$\underline{A} + \underline{B}C$	47	C B A
-1/+2/d	$\underline{A} + B$	50	B - A
-1/+2/+3	$AB\underline{C} + \underline{B}C + \underline{A}C$	58	C B A
-1/+2/+4	$\underline{A} + B + C$	51	C B A
-1/+2/+5	$A\underline{B} + \underline{B}C + AC$	55	A C B
-1/+3/a	$AB\underline{C} + A\underline{B}C$	70	
-1/+3/b	$AB\underline{C} + \underline{A}C$	67	C B A
-1/+3/c	$A\underline{B} + \underline{A}C$	60	A C B
-1/+3/+5	$AB\underline{C} + A\underline{B}C + \underline{A}BC$	71	
-1/+4/a	$A\underline{B} + C$	62	A C B
-1/+4/b	$\underline{A} + C$	50	C - A
-1/+5/a	$AB\underline{C} + \underline{A}BC$	70	B A C

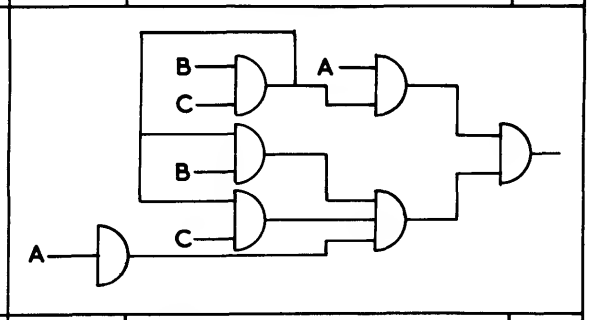
INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-1/+5/b	$A\,\underline{B} + \underline{A}\,B\,C$	67	A C B
-1/+5/c	$A\,\underline{B} + A\,C$	65	A C B
-1/+5/d	$\underline{A}\,B + A\,C$	68	B C A
-1/+6/a	$A\,\underline{B} + B\,C$	68	A C B
-1/+6/b	$\underline{A} + B\,C$	52	C B A
+1/a	A	72	
+1/b	$\underline{A}\,\underline{B}\,C$	36	C B A
+1/c	$\underline{A}\,B$		B - A
+1/+2/a	$A + B$	73	
+1/+2/b	$A + \underline{B}\,C$	62	C A B
+1/+2/c	$\underline{A}\,B + \underline{B}\,C$	60	B C A
+1/+2/+4	$A + B + C$	74	
+1/+3/a	$\underline{A}\,\underline{B}\,C + A\,B$	42	C B A
+1/+3/b	$\underline{A}\,B + A\,\underline{B}\,C$	67	B C A
+1/+3/c	$\underline{A}\,B + \underline{A}\,C$	53	C B A
+1/+3/+6	$\underline{A}\,B + \underline{A}\,C + B\,C$	55	C B A
+1/+4/a	$A + C$	73	A C -
+1/+4/b	$\underline{A}\,B + C$	62	B C A
+1/+5	$\underline{A}\,B + A\,C$	68	B C A
+1/+6/a	$A + B\,C$	75	
+1/+6/b	$\underline{A}\,B + B\,C$	65	B C A
+1/+7	$\underline{A}\,\underline{B}\,C + A\,B\,C$	43	C B A
+2/a	B	72	B - -
+2/b	$\underline{B}\,C$	59	C - B
+2/+3/a	$B + \underline{A}\,C$	62	C B A
+2/+3/b	$A\,B + \underline{B}\,C$	68	C A B
+2/+3/c	$\underline{A}\,C + \underline{B}\,C$	56	C B A
+2/+4	$B + C$	73	C B -
+2/+5/a	$B + A\,C$	75	B A C
+2/+5/b	$A\,C + \underline{B}\,C$	65	C A B
+3/a	$A\,B$	76	
+3/b	$\underline{A}\,C$	59	C B A
+3/c	$A\,\underline{B}\,C$	69	A C B
+3/+3	$A\,B + \underline{A}\,C$	68	C B A
+3/+4	$A\,B + C$	75	C B A

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
+3/+5/a	A B + A C	77	
+3/+5/b	A $\underline{B}$ C + $\underline{A}$ B C	70	C B A
+3/+5/+6	A B + A C + B C	78	
+3/+6/a	A B + B C	77	B A C
+3/+6/b	$\underline{A}$ C + B C	65	C B A
+4	C	72	C - -
+5/a	$\underline{A}$ B C	69	C B A
+5/b	A C	76	A C -
+5/+6	A C + B C	77	C B A
+6	B C	76	C B -
+6/+3	A B + B C	77	B A C
+7	A B C	79	

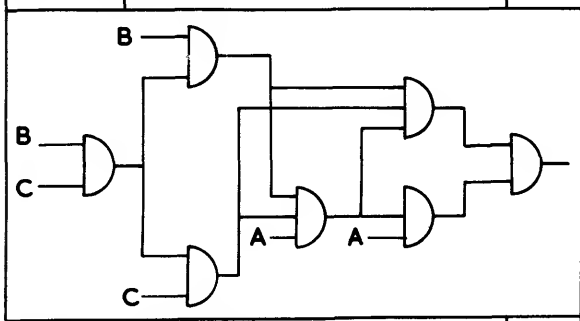
INDEX NUMBER	FUNCTION	REF. No.
-7/-1	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C}$	1



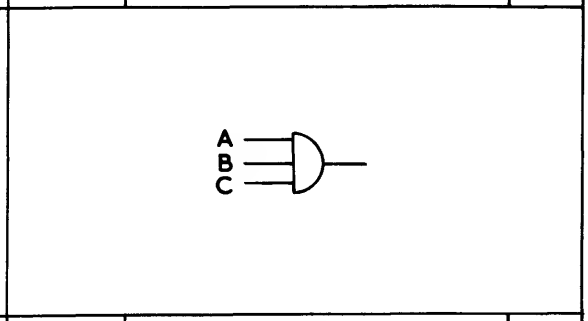
INDEX NUMBER	FUNCTION	REF. No.
-7/-1/+3	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C$	2



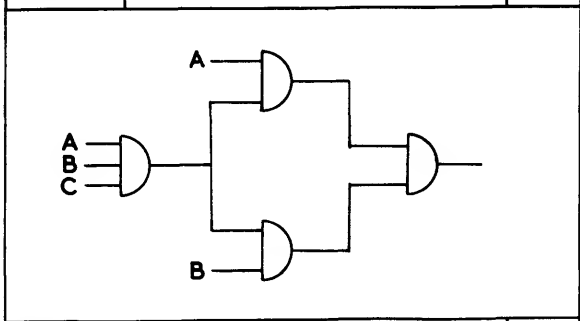
INDEX NUMBER	FUNCTION	REF. No.
-7/-1/+3/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	3



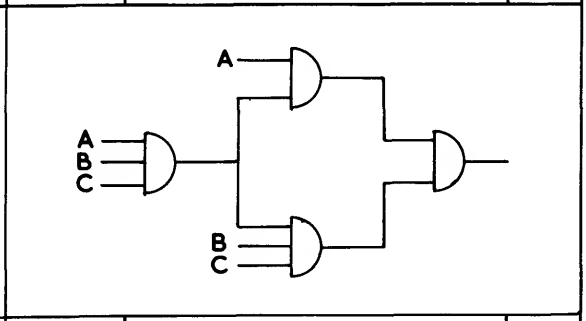
INDEX NUMBER	FUNCTION	REF. No.
-7	$\underline{A}\,\underline{B}\,\underline{C}$	4



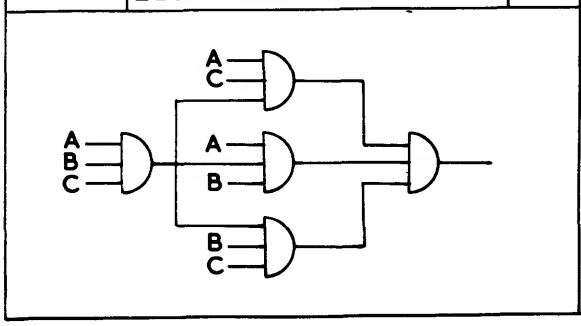
INDEX NUMBER	FUNCTION	REF. No.
-7/+3/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B$	5



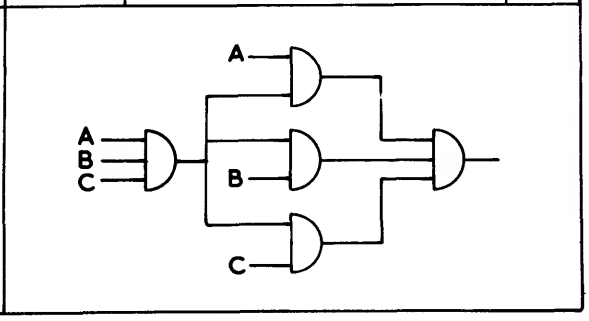
INDEX NUMBER	FUNCTION	REF. No.
-7/+3/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C$	6



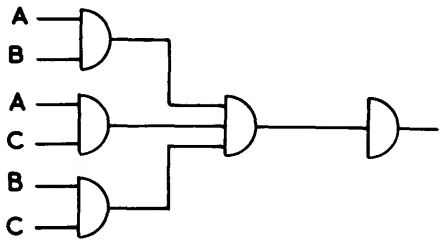
INDEX NUMBER	FUNCTION	REF. No.
-7/+3/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C + B\,C$	7



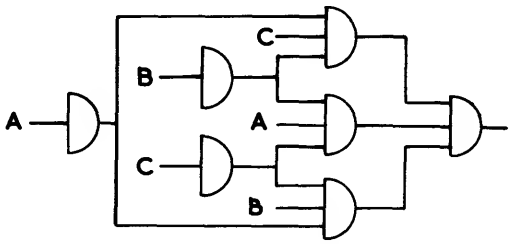
INDEX NUMBER	FUNCTION	REF. No.
-7/+7	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,C$	8



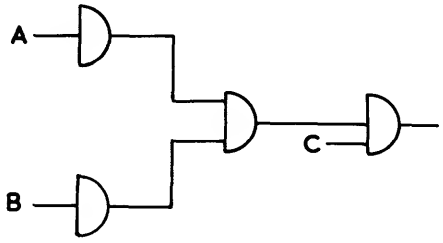
INDEX NUMBER	FUNCTION	REF No.
-6/-5/-3	$\underline{A}\underline{B} + \underline{A}\underline{C} + \underline{B}\underline{C}$	9



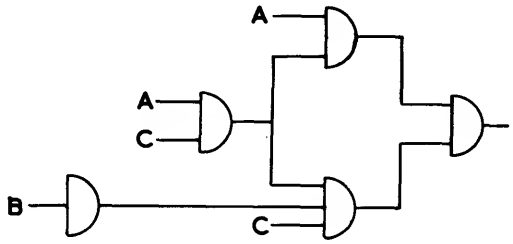
INDEX NUMBER	FUNCTION	REF No.
-6/-5/-3/+7	$\underline{A}\underline{B} + \underline{A}\underline{C} + \underline{B}\underline{C} + ABC$	10



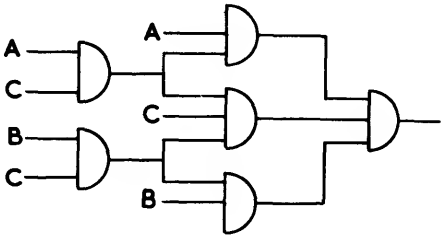
INDEX NUMBER	FUNCTION	REF No.
-6/-5	$\underline{A}\underline{C} + \underline{B}\underline{C}$	11



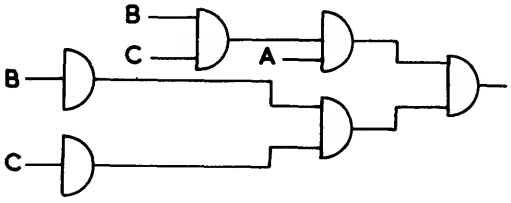
INDEX NUMBER	FUNCTION	REF No.
-6/-5/+5	$AC + \underline{A}\underline{C} + \underline{B}\underline{C}$	12



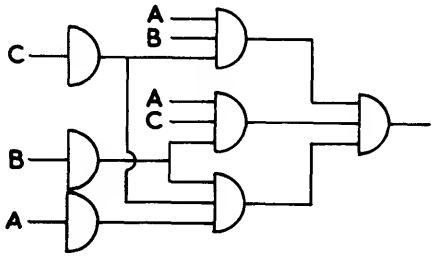
INDEX NUMBER	FUNCTION	REF No.
-6/-5/+7	$\underline{A}\underline{C} + \underline{B}\underline{C} + ABC$	13



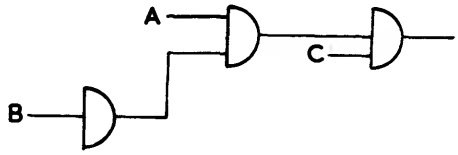
INDEX NUMBER	FUNCTION	REF No.
-6/-3/-1	$\underline{A}\underline{C} + \underline{B}\underline{C} + A\underline{B}$	14



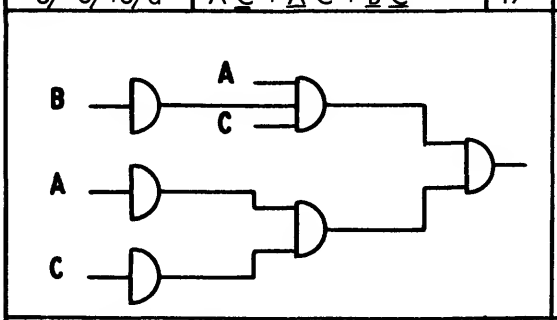
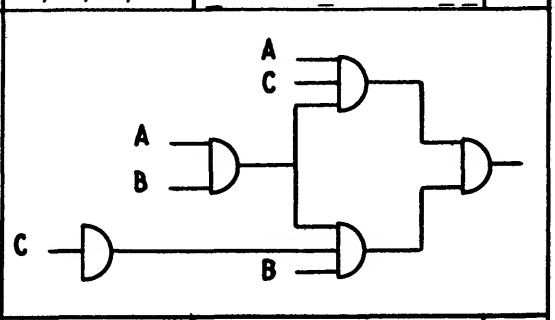
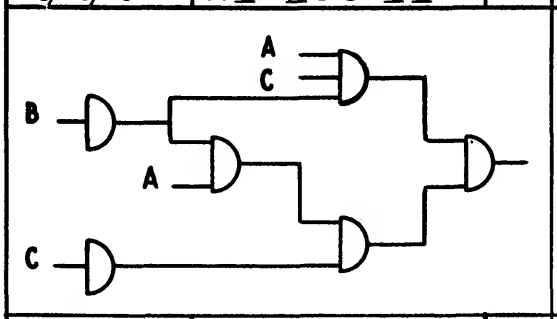
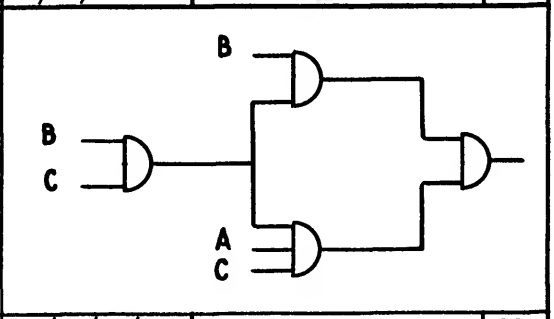
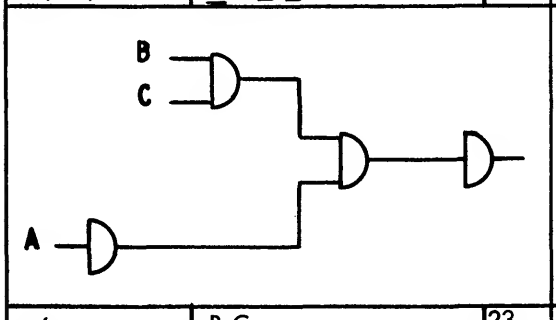
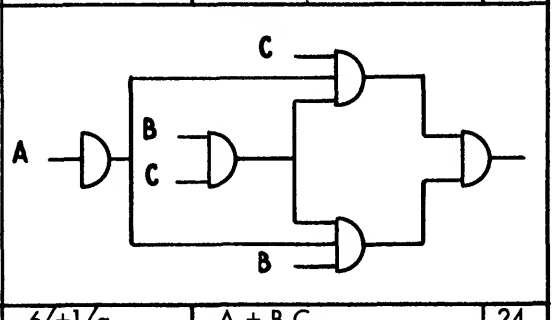
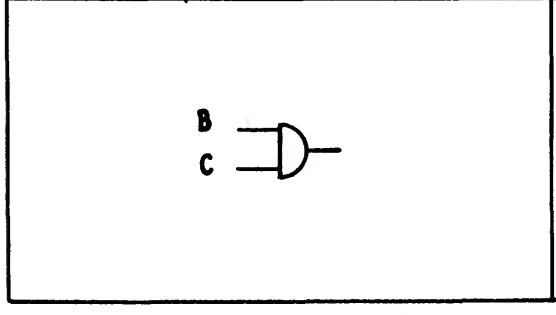
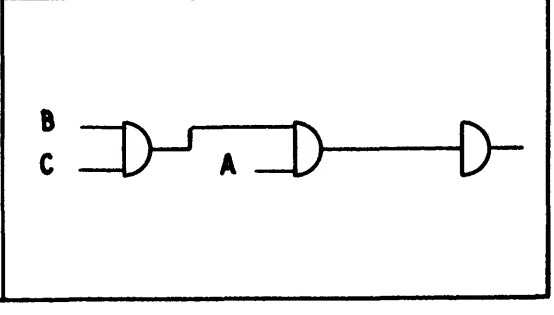
INDEX NUMBER	FUNCTION	REF No.
-6/-3/-1/45	$A\underline{B} + A\underline{C} + \underline{B}\underline{C} + \underline{A}BC$	15



INDEX NUMBER	FUNCTION	REF No.
-6/-3/a	$\underline{A}\underline{C} + \underline{B}\underline{C}$	16

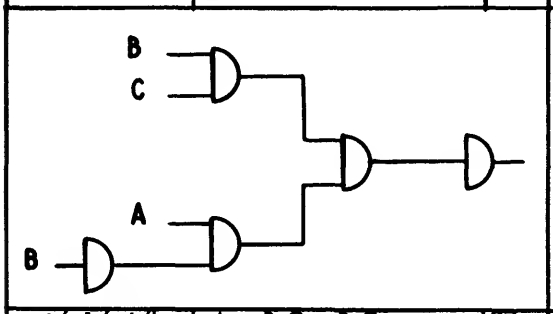
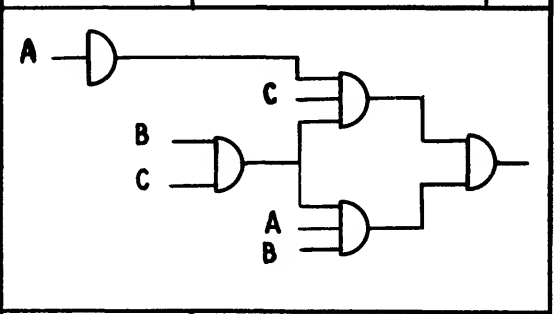
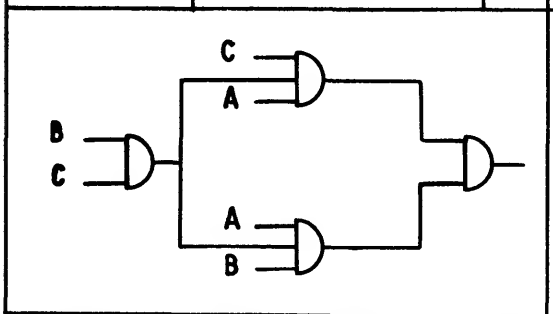
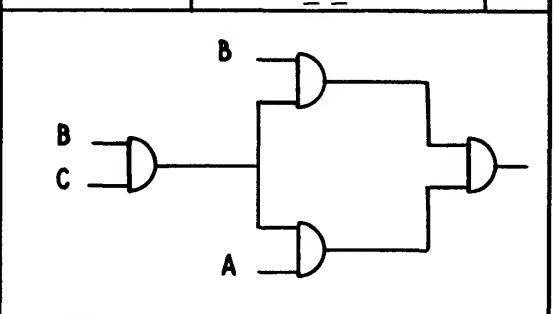
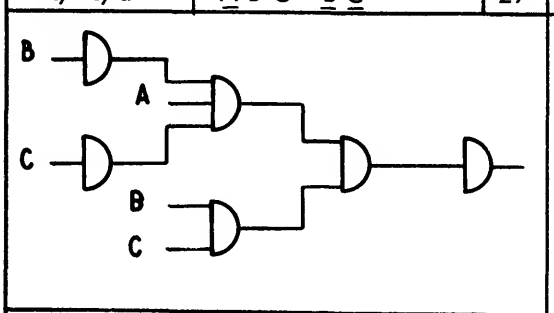
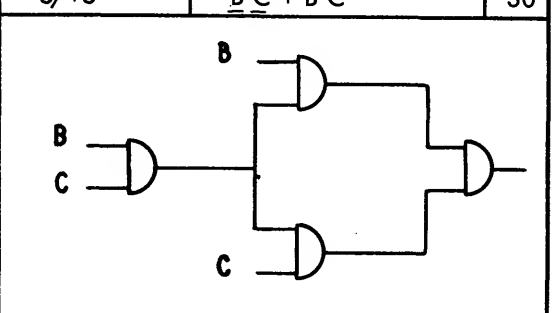
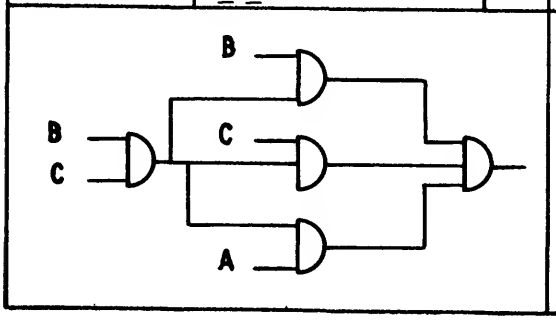
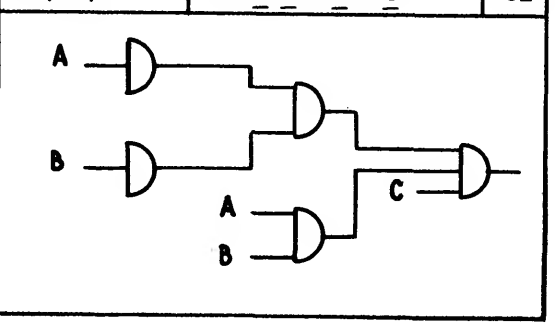


ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-6/-3/+3/a	$A\,\underline{C} + \underline{A}\,C + \underline{B}\,\underline{C}$	17	-6/-3/+3/+6	$A\,C + A\,\underline{C} + B\,C + \underline{B}\,\underline{C}$	18
					
-6/-3/+5	$A\,\underline{C} + \underline{A}\,B\,C + \underline{B}\,\underline{C}$	19	-6/-3/+6a	$A\,\underline{C} + \underline{B}\,\underline{C} + B\,C$	20
					
-6/-1/a	$\underline{A} + \underline{B}\,\underline{C}$	21	-6/-1/+6/a	$\underline{A} + \underline{B}\,\underline{C} + B\,C$	22
					
-6	$\underline{B}\,\underline{C}$	23	-6/+1/a	$A + \underline{B}\,\underline{C}$	24
					

For race hazard free circuits see next chapter.

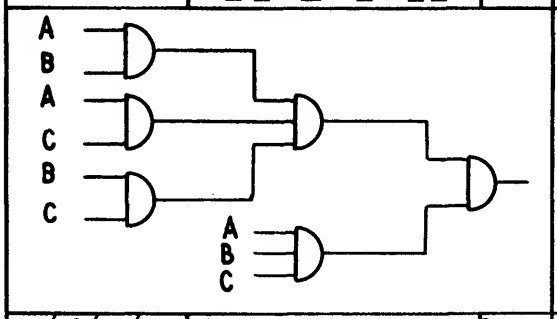
ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-6/+1/b	$\underline{A}\,B + \underline{B}\,\underline{C}$	25	-6/+1/+5	$A\,C + \underline{A}\,B + \underline{B}\,\underline{C}$	26
					
-6/+1/+6/b	$A + \underline{B}\,\underline{C} + \underline{B}\,C$	27	-6/+3/a	$A\,B + \underline{B}\,\underline{C}$	28
					
-6/+5/a	$\underline{A}\,B\,C + \underline{B}\,\underline{C}$	29	-6/+6	$\underline{B}\,\underline{C} + B\,C$	30
					
-6/+7	$\underline{B}\,\underline{C} + A\,B\,C$	31	-5/-3/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C}$	32
					

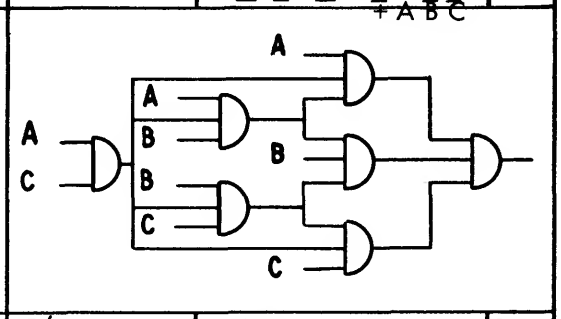
For race hazard free circuits see next chapter.

ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

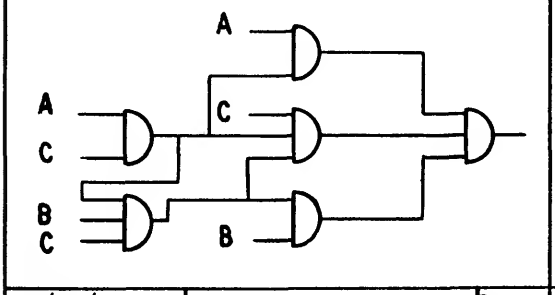
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+1	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	33



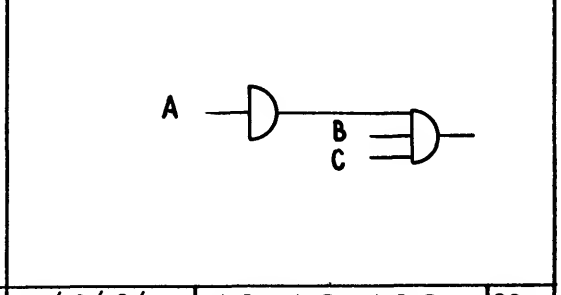
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+1/+7	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	34



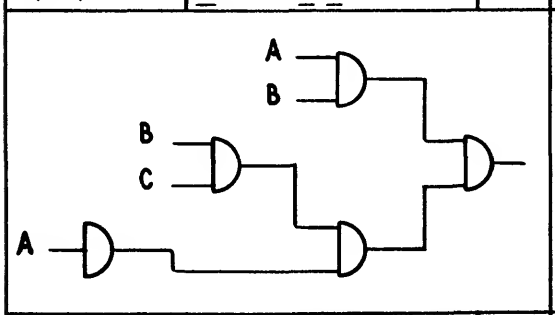
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+7/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + A\,B\,C$	35



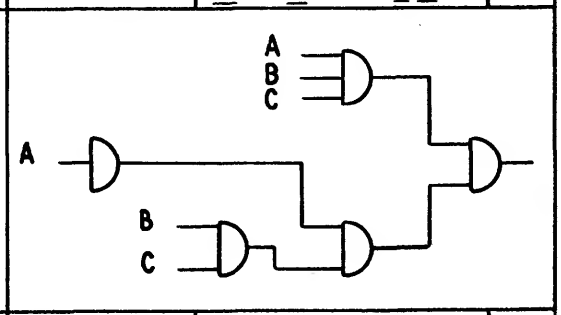
INDEX NUMBER	FUNCTION	REF No.
-5/a	$A\,\underline{B}\,\underline{C}$	36



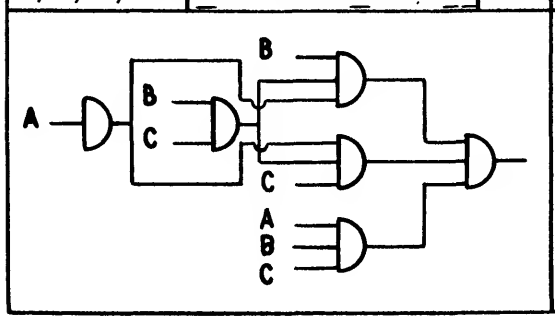
INDEX NUMBER	FUNCTION	REF No.
-5/+1/a	$\underline{A}\,B + A\,\underline{B}\,\underline{C}$	37



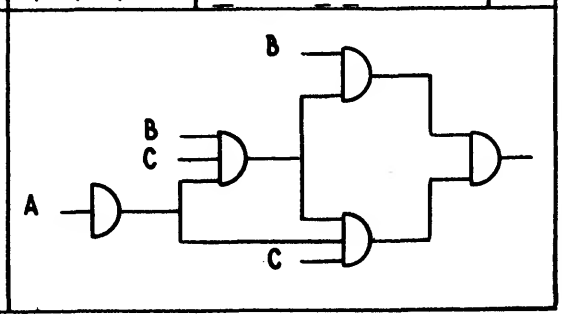
INDEX NUMBER	FUNCTION	REF No.
-5/+1/+3/a	$\underline{A}\,B + \underline{A}\,C + A\,\underline{B}\,\underline{C}$	38



INDEX NUMBER	FUNCTION	REF No.
-5/+1/+3/+6	$\underline{A}\,C + B\,C + \underline{A}\,B + A\,\underline{B}\,\underline{C}$	39

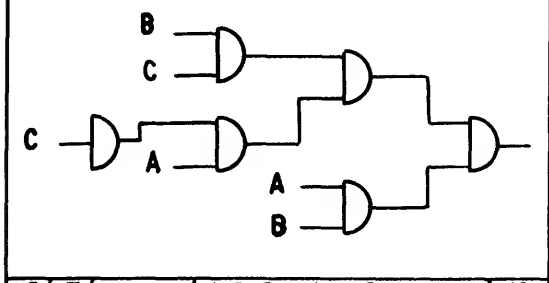
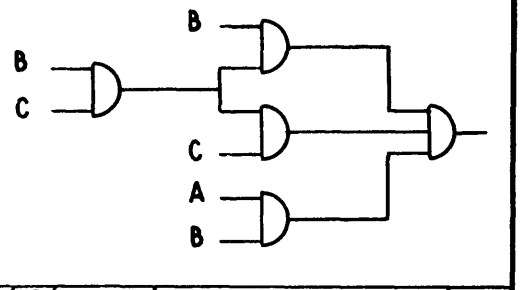
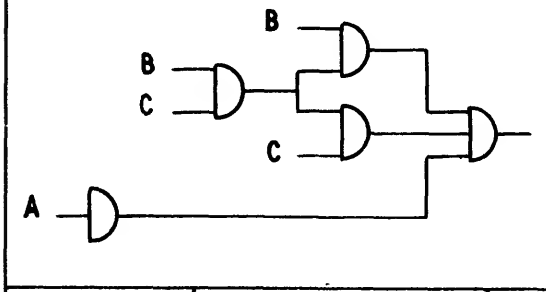
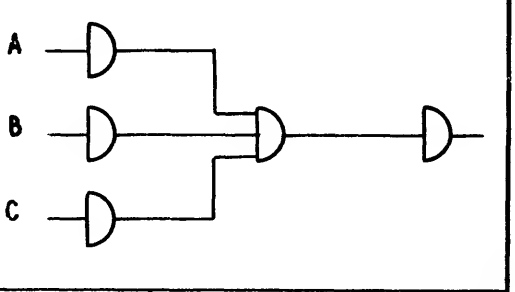
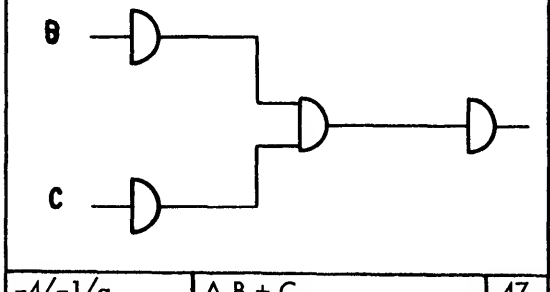
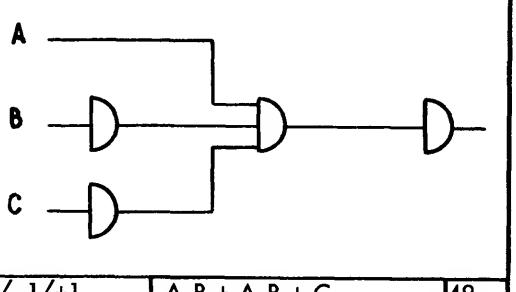
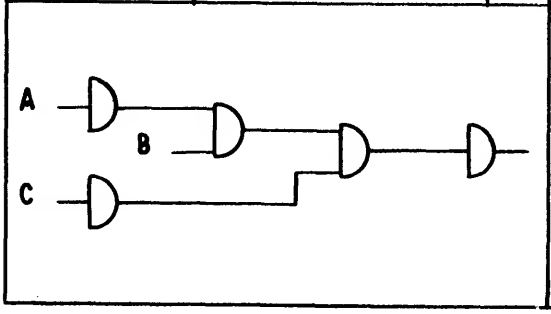
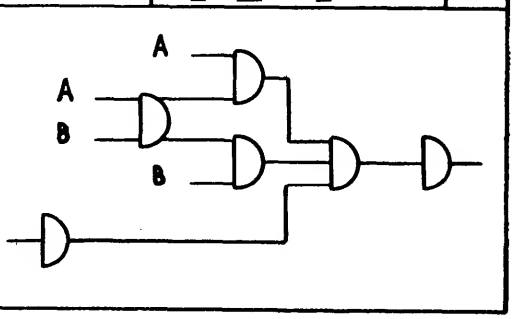


INDEX NUMBER	FUNCTION	REF No.
-5/+1/+6/a	$\underline{A}\,B + A\,\underline{B}\,\underline{C} + B\,C$	40



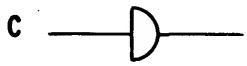
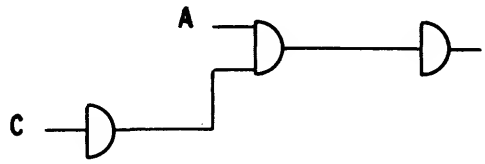
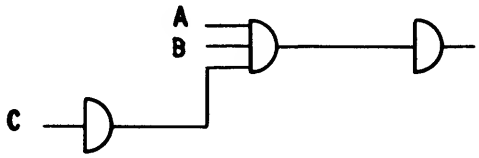
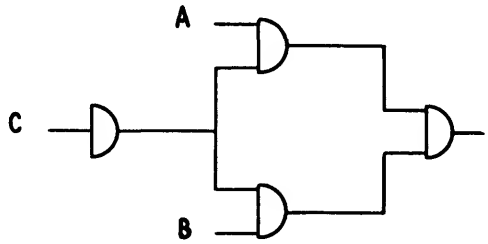
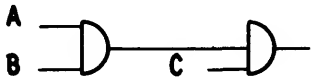
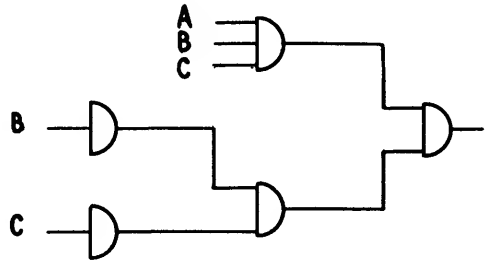
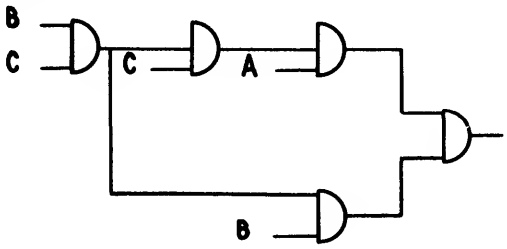
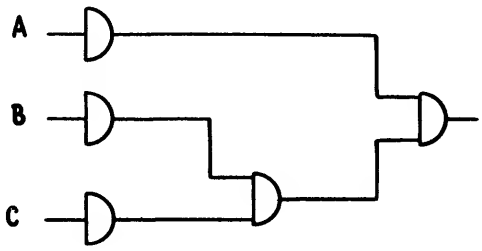
For race hazard free circuits see next chapter.

ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No	INDEX NUMBER	FUNCTION	REF No.
-5/+5/a	$\underline{A}\,B\,C + A\,\underline{B}\,\underline{C}$	41	-5/+6	$A\,\underline{B}\,\underline{C} + B\,C$	42
					
-5/+7/a	$A\,\underline{B}\,\underline{C} + A\,B\,C$	43	-4/-2/-1	$\underline{A} + \underline{B} + \underline{C}$	44
					
-4/-2	$\underline{B} + \underline{C}$	45	-4/-2/+1	$A + \underline{B} + \underline{C}$	46
					
-4/-1/a	$A\,\underline{B} + \underline{C}$	47	-4/-1/+1	$A\,\underline{B} + \underline{A}\,B + \underline{C}$	48
					

For race hazard free circuits see next chapter.

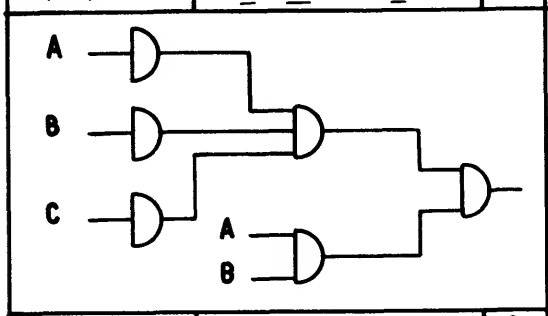
ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-4	$\underline{C}$	49	-4/+1/a	$A + \underline{C}$	50
					
-4/+1/+2	$A + B + \underline{C}$	51	-4/+3	$A\,B + \underline{C}$	52
					
-3/-2/a	$A\,\underline{C} + B\,\underline{C}$	53	-3/-2/+2/a	$A\,\underline{C} + B\,\underline{C} + \underline{B}\,C$	54
					
-3/-2/+3/a	$A\,\underline{C} + B\,\underline{C} + A\,B$	55	-3/-1	$A\,\underline{B} + A\,\underline{C}$	56
					

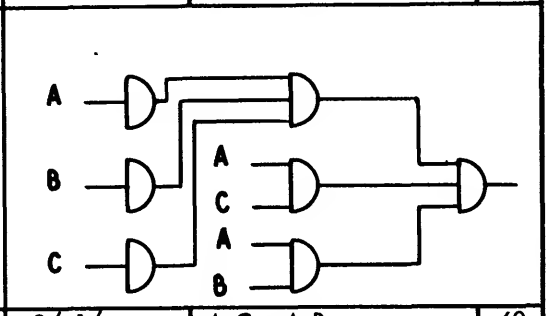
For race hazard free circuits see next chapter.

ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.
-3/-1/+1	$A\,\underline{B} + \underline{A}\,B + A\,\underline{C}$	57



INDEX NUMBER	FUNCTION	REF No.
-3/-1/+5/a	$A\,\underline{C} + A\,\underline{B} + \underline{A}\,B\,C$	58



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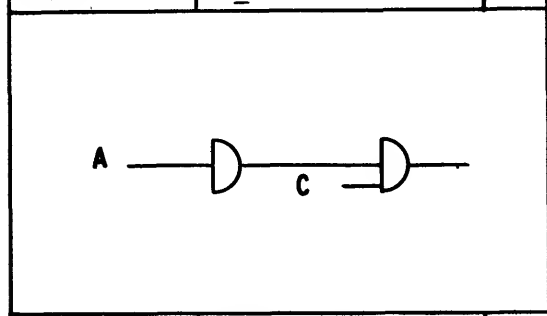
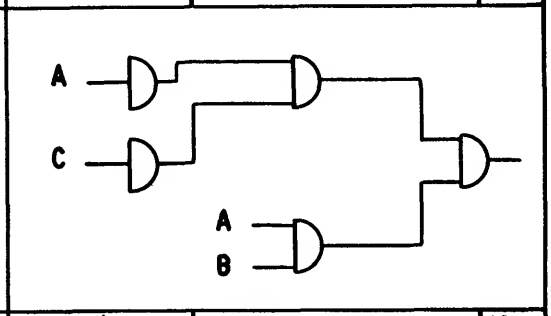
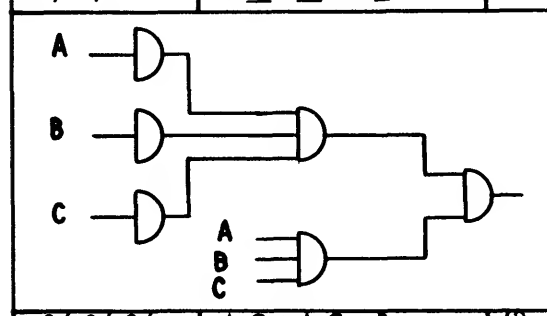
-3/a	$A\,\underline{C}$	59



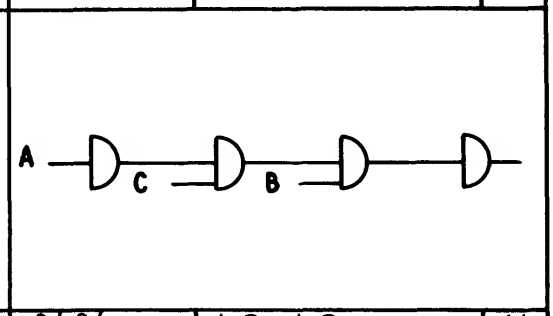
INDEX NUMBER	FUNCTION	REF No.
-3/+1/a	$A\,\underline{C} + \underline{A}\,B$	60



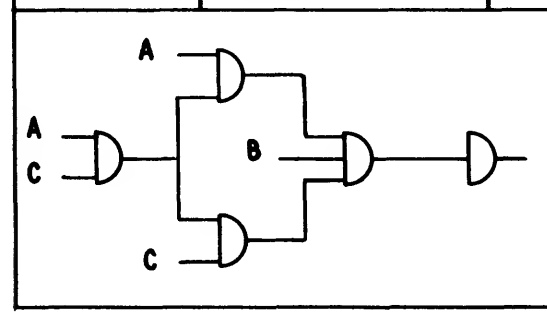
INDEX NUMBER	FUNCTION	REF No.
-3/+1/+2	$A\,\underline{C} + \underline{A}\,B + \underline{B}\,C$	61



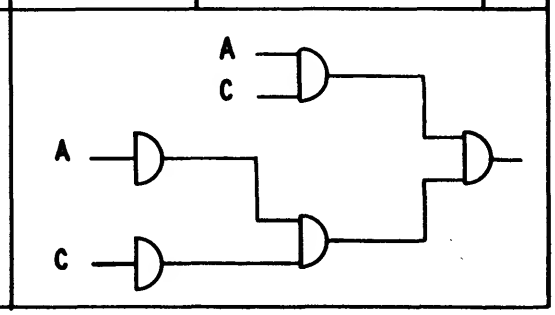
INDEX NUMBER	FUNCTION	REF No.
-3/+2/a	$B + A\,\underline{C}$	62



INDEX NUMBER	FUNCTION	REF No.
-3/+2/+3/a	$A\,\underline{C} + \underline{A}\,C + B$	63

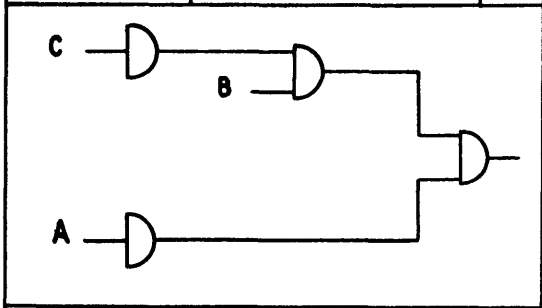
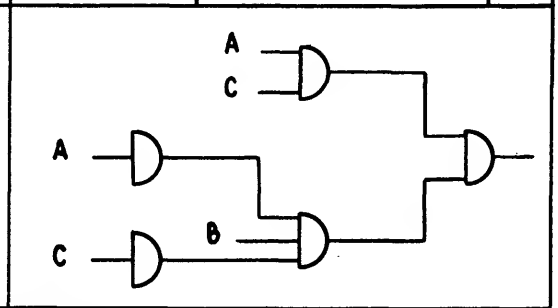
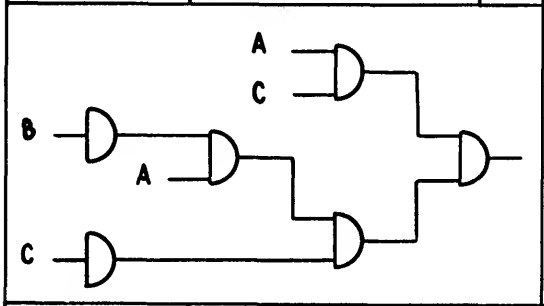
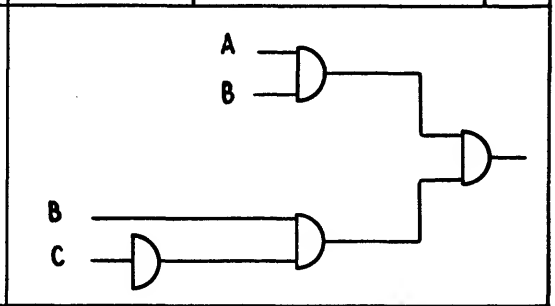
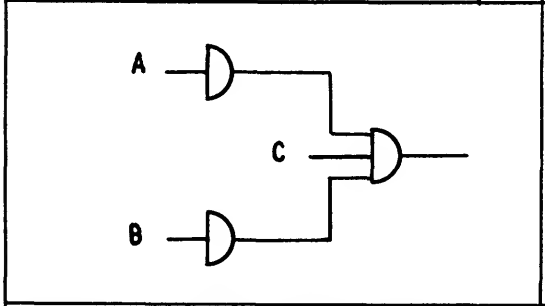
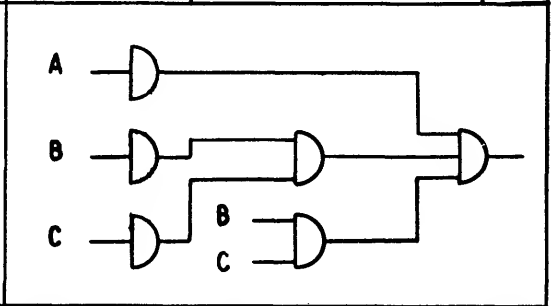
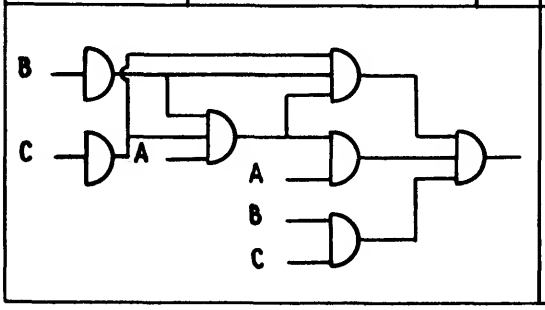
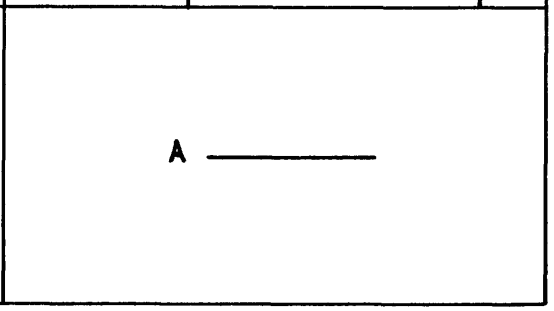


INDEX NUMBER	FUNCTION	REF No.
-3/+3/a	$A\,\underline{C} + \underline{A}\,C$	64



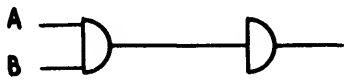
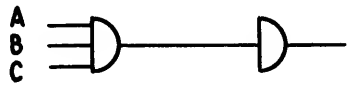
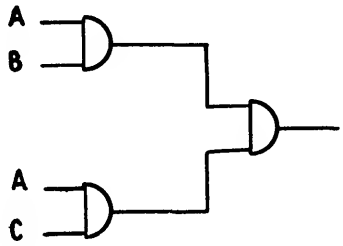
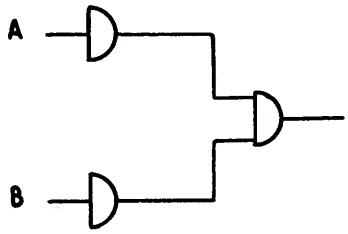
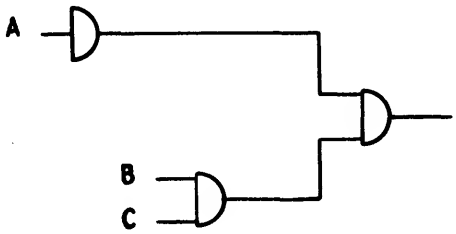
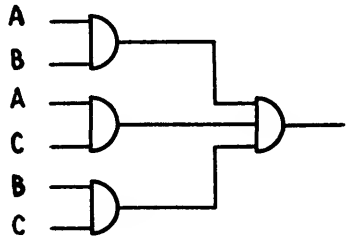
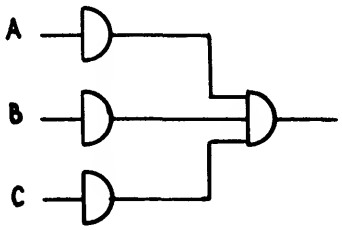
For race hazard free circuits see next chapter.

ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-3/+3/b	A B + A $\underline{C}$	65	-3/+3/+3/a	A B + A $\underline{C}$ + $\underline{A}$ C	66
					
-3/+5/a	$\underline{A}$ B C + A $\underline{C}$	67	-3/+6/a	A $\underline{C}$ + B C	68
					
-1/a	A B $\underline{C}$	69	-1/+3/a	A B $\underline{C}$ + A $\underline{B}$ C	70
					
-1/+3/+5	A B $\underline{C}$ + A $\underline{B}$ C + $\underline{A}$ B C	71	-1/a	A	72
					

For race hazard free circuits see next chapter.

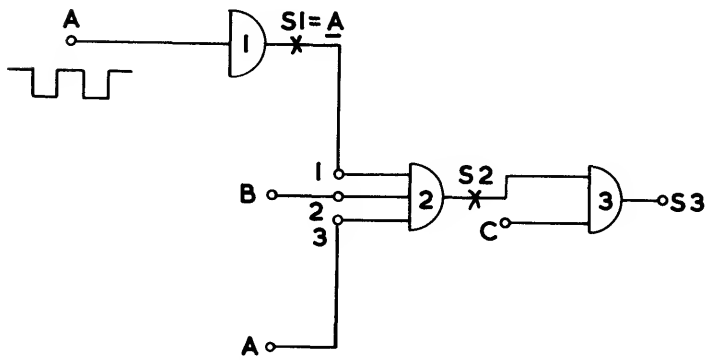
ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
+1/+2/a	A + B	73	+1/+2/+4	A + B + C	74
					
+1/+6/a	A + B C	75	+3/a	A B	76
					
+3/+5/a	A B + A C	77	+3/+5/+6	A B + A C + B C	78
					
+7	A B C	79			
					

For race hazard free circuits see next chapter.

CHAPTER 3

RACE AND HAZARD PHENOMENA IN COMBINATIONAL SWITCHING CIRCUITS



CIRCUIT 1. NOR CIRCUIT USED TO ILLUSTRATE THE EFFECTS OF RACES ON SWITCHING CIRCUITS

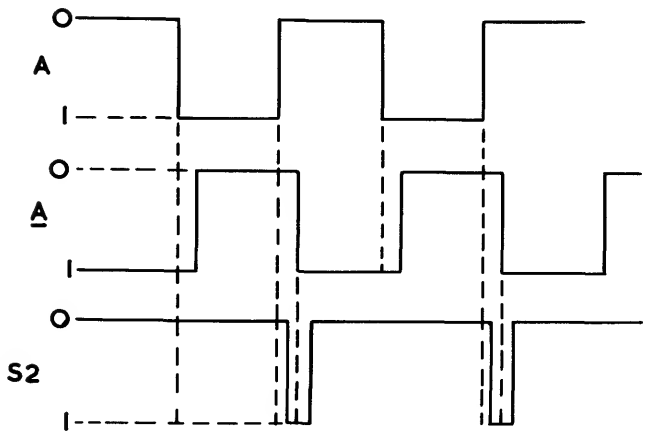


DIAGRAM 1. SIGNAL SPIKE APPEARING AT THE OUTPUT OF MODULE 2 AS A RESULT OF A CRITICAL RACE AT ITS INPUT

RACE AND HAZARD PHENOMENA IN COMBINATIONAL SWITCHING CIRCUITS

SUMMARY

A new approach to the study of race and hazard phenomena in switching circuits is suggested. Static hazards, essential hazards and dynamic hazards are shown to be one and the same phenomenon present in combinational switching circuits, whether electronic or electromechanical.

The above mentioned hazards are collectively referred to as race-hazards.

The causes of race-hazards are analysed and simple means of detecting and eliminating them (when they have to be eliminated) are suggested. A set of problems with model solutions is included.

INTRODUCTION

It is essential to understand the phenomenon of races and the resulting circuit hazards before attempting to synthesise switching circuits, for if such hazards are not eliminated, they may, on certain occasions cause temporary or even permanent malfunction of the circuit in which they are present.

A race is said to be present in a switching circuit, if two signals that feed the same switching element change during a circuit transition from one stable state to another stable state. The two signals may both be secondary or one may be a primary and the other a secondary. There can be no race between primary signals, since unless otherwise specified only one primary signal is assumed to change at a time.

If, as a result of a given race, there is a possibility that the circuit may cease to function according to its excitation table, the race is classified as critical. Otherwise it is referred to as non-critical.

If any two of the input signals to a switching element, which have the logical values 0 and 1, change to 1 and 0 respectively during a circuit transition between two adjacent states, the output of that switching module should remain unaffected by the circuit transition.

In practice, however, this may not happen. What is likely to happen is that during the circuit transition a pulse type signal appears at the output of the switching element. This is illustrated by reference to NOR circuit 1. If primary signal B is assumed to be equal to zero, the output of module 2 must not be affected by changes in A, since $S2 = A\,\bar{A} = 0$. But because of the time delay introduced by module 1, immediately following a change in primary signal A, both A and $\bar{A}$ assume the value 0. This results in a signal spike appearing at the output of module 2, as shown in diagram 1.

Mathematically this corresponds to the basic Boolean relationships

$A + \bar{A} = 1$ and
$A\,\bar{A} = 0$

not holding during transient conditions following a change in primary signal A.

It is possible for a signal spike not to manifest itself in a given switching circuit, particularly if the switching elements are slow. It may however be present in an identical circuit using a different set of the same switching elements.

The possibility of a signal spike revealing itself in a switching circuit as a result of a race in the circuit is defined as a race hazard.

The term 'hazard' indicates that in a given circuit the signal spike may or may not reveal itself. 'Race" is used to show that the cause of the hazard at the output of a switching element, is a race between signals at its input.

Referring back to NOR circuit 1, it is obvious that if during the possible appearance of the signal spike at the output of module 2, input signal C = 1, the output of NOR module 3 will not be affected by the race between signals A and $\underline{A}$. This race is therefore non-critical. But if signal C = 0, the signal spike appearing at the output of NOR module 2 may get through to the output of NOR module 3 inverted. This means that the race between primary signal A and secondary signal $\underline{A}$ may cause a temporary malfunction of NOR circuit 1. Whether this race is critical or not depends on the circuit into which the output of NOR module 3 is fed. If it is some form of trigger circuit, it may be triggered into the wrong state by the signal spike. In such a case the race is classified as critical. If on the other hand the output is fed, say, to a d.c. voltmeter, the appearance of the race hazard will not affect the meter reading. In this case the race will be classified as non-critical.

Race hazards themselves are classified as type 1 and type 0. A type 1 race hazard is one in which the signal changes temporarily from its logical '0' level to the logical '1' level - see diagram 1. A type 0 race hazard is one in which the signal assumes temporarily the value 0, as a result of the race.

Because in practice it is not possible to design minimal switching circuits which are free of races, the suggested design method consists of first designing minimal circuits ignoring the possible presence of races. All the races present are next determined and classified as critical and non-critical.

Finally all critical races are rendered non-critical before the circuit is realised.

OUTLINE OF THE METHOD

Propagation Times.

Because of the production spread in the switching elements and the wide variation in their loading, no two switching elements can be assumed to have identical propagation times. It is also possible in practice that the effective propagation time of a path containing M elements in cascade is greater than the propagation time of a path containing M + N elements in cascade. This fact may be illustrated by reference to NOR circuit 1 and diagram 2. In circuit 1, the same signal A is applied to NOR module 2 through two different paths, path A-1 containing a NOR module and path A-3 containing no switching elements. If the input signal A is a sine wave of relatively low frequency, the following phenomenon may occur, when signal B is equal to 0.

Because of the production spreads in the individual components of the NOR modules, a considerable difference may exist in the minimum voltages that are needed to switch the two transistors of NOR modules 1 and 2 ON and OFF. Let -W volts be the minimum negative voltage needed at one of the input terminals of module 1 to cause its transistor to start conducting, and -X volts be the minimum negative voltage needed to bottom (saturate) the transistor, whereas the two corresponding voltage levels for module 2 are -Y and -Z volts respectively, as shown in diagram 2(a). In steady state conditions output signal of NOR module 1 will be the complement of output signal of NOR module 6, (signals B = C = 0). During the excursion of the input signal A from M to N (see diagram 2(a)), the two input signals to NOR module 2, S1 and A, change from logical levels 1 to 0 and 0 to 1 respectively. In theory both these signals, namely secondary signal S1 and primary signal A, should change at the same time. But, if the circuit conditions mentioned above exist, primary signal A will bottom the transistor of module 1 first, causing the output of MOR module 1 to change to 0 V, before it becomes negative enough to bottom the transistor of module 2. This is equivalent so far as the NOR module 2 is concerned, to the propagation time of path A-1 containing NOR module 1, being less than the propagation time of path A-3 containing no switching elements. This phenomenon is often referred to as, 'the race has been won by the secondary signal'.

The following stipulation will therefore now be made. No two sections of a switching circuit can be assumed to have equal propagation times, nor can one section be assumed to be either faster or slower than the other.

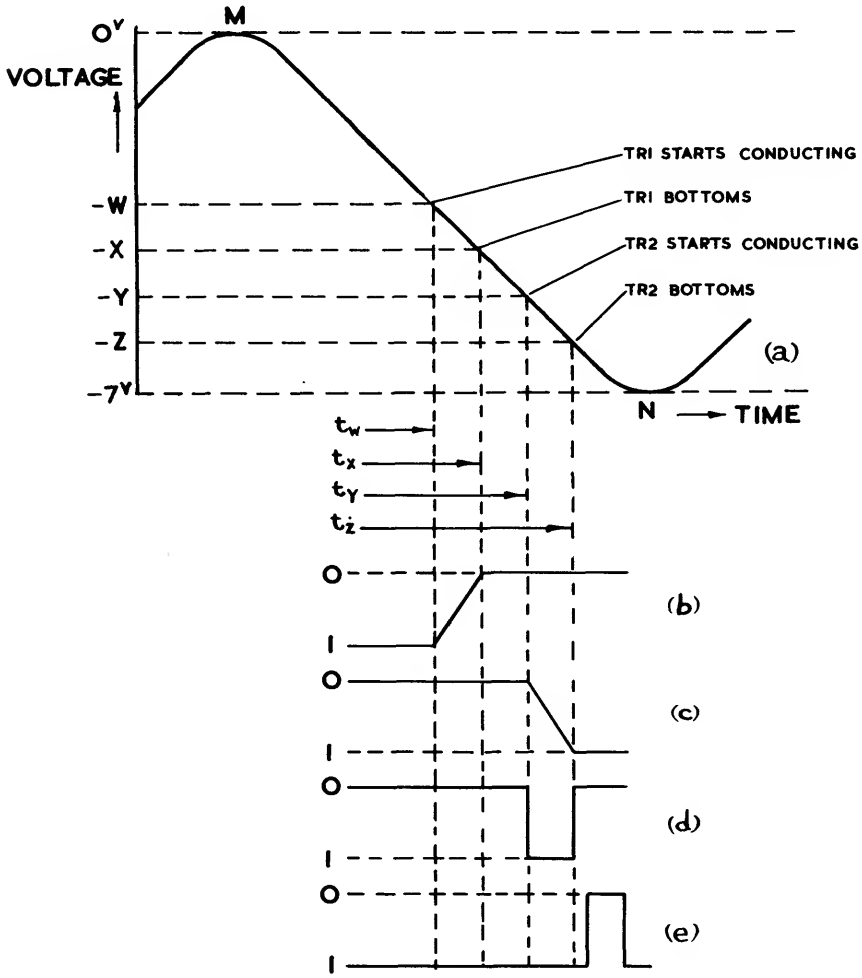


DIAGRAM 2. (ALL WAVEFORMS REFER TO CIRCUIT 1.)

a) SINE WAVE INPUT TO MODULE 1.

b) SECONDARY SIGNAL, S1, APPLIED TO NOR MODULE 2.

c) PRIMARY SIGNAL, A, APPLIED TO NOR MODULE 2.

d) TYPE-1 RACE HAZARD APPEARING AT THE OUTPUT OF MODULE 2.

e) TYPE-0 RACE HAZARD APPEARING AT THE OUTPUT OF MODULE 3.

Detection of Critical Races

The presence of races in switching circuits and their classification into critical and non-critical may be revealed either algebraically or by tabular methods.

The Algebraic Method

It has been explained previously, that, because of the finite propagation times of the switching elements, two signals that are the complement of each other during two adjacent stable states, can, if they change, assume the same value during the transition of the circuit from one state to the other. If two such signals are feeding the same switching element then a signal spike may appear at the output of the element. Algebraically this fact may be stated in the following terms.

A critical race may be present at the output of a switching element if the algebraic expression of the module output signal can be reduced either to the form $X + \underline{X}$ or $X\,\underline{X}$. In the first case the race may result in a type 0 race hazard and in the second case the race hazard is type 1.

For example, the switching function $A\,B + \underline{A}\,C$ can be reduced to $A + \underline{A}$, when $B = C = 1$. Therefore a type -0 race hazard is present at the output of circuit 2(a) during a change in signal A, if signals $B = C = 1$. Similarly the switching function $(\underline{A} + B)(A + C)$ can be reduced to $A\,\underline{A}$, by making signals B and C both equal to 0. This indicates that a type -1 race hazard is present at the output of the circuit 2(b) if signal A changes and signals B and C are both equal to 0.

The switching function $A\,B + \underline{A}\,\underline{B}$, when realised directly, will not contain race hazards, i.e. it will be speed independent, since it cannot be reduced to either $A + \underline{A}$ or $B + \underline{B}$. Similarly the switching circuit realising the function $(A + B)(\underline{A} + \underline{B})$ is also speed independent when directly realised, since it cannot be reduced to $A\,\underline{A}$ or $B\,\underline{B}$.

The Excitation Table Method

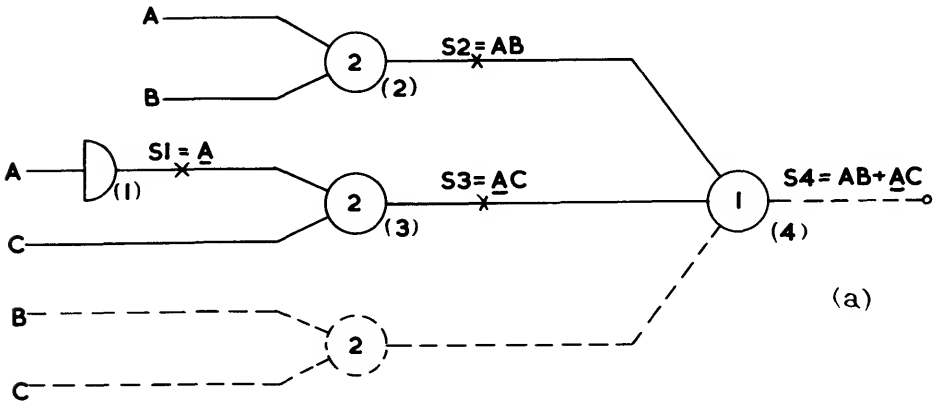
It follows from the definition of lift sets (see chapter 1) that within a lift-set the output signal is maintained at 1 by the same input signal.

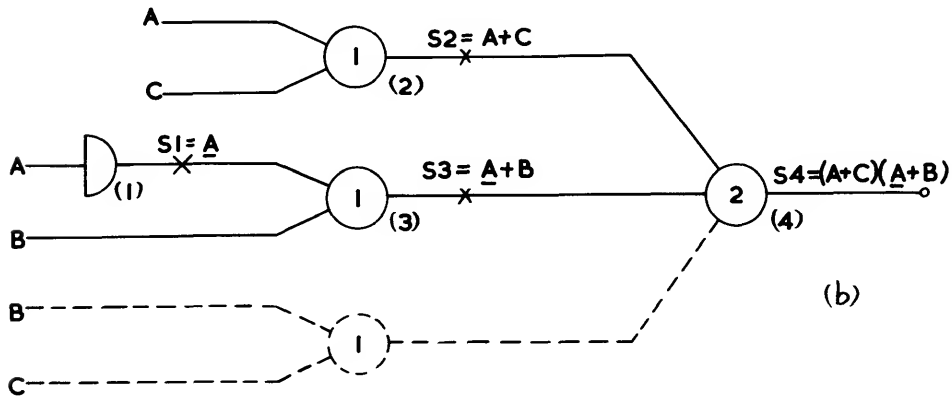
Therefore, the transition of the circuit between adjacent 1-entries within a lift-set will be free of race hazards since the input signal maintaining the output signal at 1 does not change. Moving however between two adjacent 1-entries which are not included in a lift set, implies a change of the two corresponding input signals from 10 to 01, (race). Therefore a type 0 race hazard exists at the output during the transition.

By analogy, a type 1 race hazard is present at the output of a circuit, during the transition of the circuit between two adjacent 0 entries, if they are not included in a drop set.

Referring to circuit 2(a) the presence of the type 0 race hazard at the output of the OR element could have been detected by reference to excitation table 1(a) where the adjacent 1 entries in squares 6 and 7 are not included in a lift set.

Similarly the type 1 race hazard present in switching circuit 2(b) could have been detected by reference to its excitation table 1(b) where the two 0 entries in the adjacent squares 1 and 4 are not included in a drop set.





CIRCUIT 2. (a) DIRECT CIRCUIT REALISATION OF THE SWITCHING FUNCTION AB+AC
(b) DIRECT CIRCUIT REALISATION OF THE SWITCHING FUNCTION (A+C)(A+B)

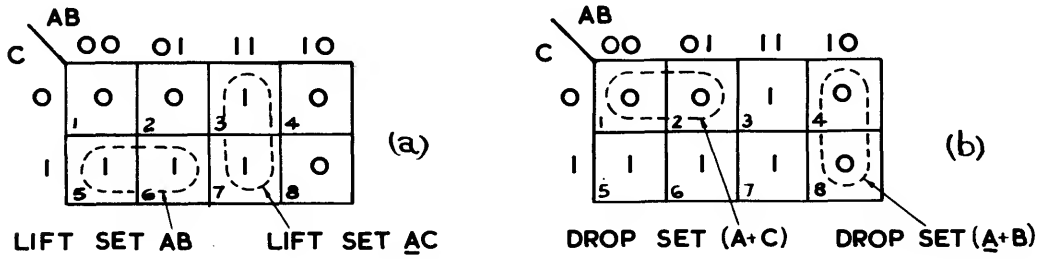


TABLE I. a) EXCITATION TABLE OF AND/OR FUNCTION AB+AC
b) EXCITATION TABLE OF OR/AND FUNCTION (A+C)(A+B)

The Transition Table Method

This method is particularly suited for detecting the presence of race hazards in sequential circuits, where the number of primary signals involved is relatively large, but the number of circuit transitions is small. It probably gives a clearer picture of what is going on in the circuit than the two previous methods and it is particularly useful for checking the final circuit. Being a systematic method, it can be used to programme a computer relatively easily.

Circuit 2(a) will be used to demonstrate the method.

The transition table of the circuit under test is plotted. See table 2.

The input signals of each switching element in turn are compared, two at a time, for all possible circuit transitions. If two of the signals change from 01 to 10 during a circuit transition, and the other input signals (if any) are ineffective, then a race hazard is present at the output of the switching element during the transition.

It is noted, with reference to table 2, that switching element 1 is race hazard free, since it is fed with a single signal only. Switching element 2 is also free of race hazards, since there can be no race between primary signals. Attention is next focussed on switching element 3. Comparing the entries in columns 3 and 4 for all possible circuit transition, reveals that the output of switching element 3 is also free of race hazards. Finally the entries in columns 5 and 6 are next examined.

The examination of these columns reveals the presence of a race in moving between rows 6 and 7, that is, when A changes and B = C = 1. The race is classified as critical or non-critical depending on whether the race hazard is allowed to exist or not.

ELIMINATION OF RACE HAZARDS

Having detected and classified the races in a switching circuit, the designer next directs his attention to methods of rendering all critical races into non-critical ones. This basically is achieved by introducing an additional signal into the module which serves to prevent the race hazard from appearing at its output terminal.

The Algebraic Method

Algebraically the presence of a race hazard in a switching circuit is revealed by the possible reduction of the switching function to the form $X + \underline{X}$ or $X\,\underline{X}$. If the switching function cannot be reduced to one of these forms, then the circuit under consideration is free of race-hazards.

The method therefore consists of modifying the algebraic expression so that it can never be reduced to $X + \underline{X}$ or $X\,\underline{X}$. This is easily achieved by the application of theorem 3.

Example

The algebraic expressions of the switching functions of circuits 2(a) and 2(b) are:

$$f = A\,B + \underline{A}\,C \quad \ldots\ldots (1)$$

and

$$f = (A + C)(\underline{A} + B) \quad \ldots\ldots (2)$$

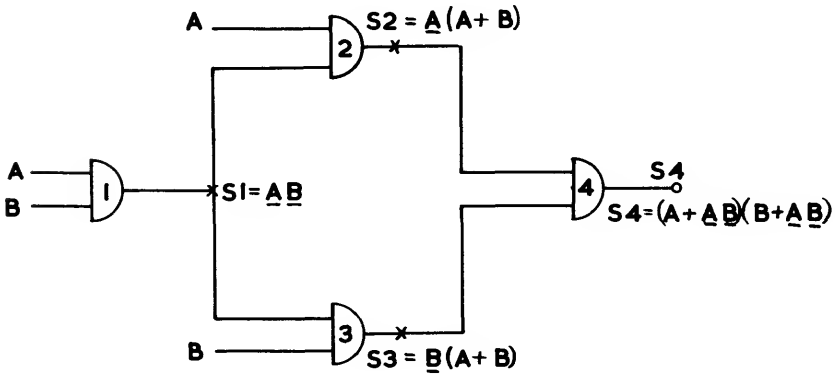
Applying theorem 3, equations 1 and 2 are modified to:

$$f = A\,B + \underline{A}\,C + B\,C \quad \ldots\ldots (3)$$

$$f = (A + C)(\underline{A} + B)(B + C) \quad \ldots\ldots (4)$$

	PRIMARY SIGNALS			SECONDARY SIGNALS			
	A	B	C	S1	S2	S3	S4
1	0	0	0	1	0	0	0
2	0	1	0	1	0	0	0
3	1	1	0	0	1	0	1
4	1	0	0	0	0	0	0
5	1	0	1	0	0	0	0
6	1	1	1	0	1	0	1
7	0	1	1	1	0	1	1
8	0	0	1	1	0	1	1

TABLE 2. TRANSITION TABLE OF SWITCHING CIRCUIT 2(a)



CIRCUIT 3. MINIMAL NOR CIRCUIT REALIZING INCLUSIVE "OR" FUNCTION AB+ AB

Neither of the last two equations can be reduced to the form $X\underline{X}$ or $X + \underline{X}$. Therefore the circuits realising equations 3 and 4 will be free of critical races.

Note

Further manipulation of the final expressions is possible provided they are not minimised. e.g. $f = A B + \underline{A} C + B C$ could be modified to $f = B(A + C) + \underline{A} C$ etc.

THE EXCITATION TABLE METHOD

The same results that were obtained algebraically may be obtained by including all the adjacent 1 entries in lift sets in the case of AND/OR (sums of products) expressions, or all the adjacent 0 entries in drop sets in the case of OR/AND (product of sums) expressions. E.g. referring to table 1(a) the type 0 race hazard that may appear in the output of the circuit realising the excitation table directly, during its transition between adjacent squares 6 and 7, is eliminated by including the two 1 entries in squares 6 and 7 in a lift set, namely B C. This corresponds to adding the product term B C in the algebraic expression of the switching function to be realised.

Similarly the type 1 static hazard that may reveal itself in the circuit directly realising excitation table 1(b) during its transition between adjacent squares 1 and 4 is eliminated by including these two 0 entries in a drop set namely (B + C). The switching expression therefore is modified to $(A + C)(\underline{A} + B)(B + C)$

THE TRANSITION TABLE METHOD

The race hazard present at the output of module 4 during the circuit transition between rows 6 and 7 of table 2, may be eliminated by the introduction of a correcting signal which equals 1 during this transient state.

In combinational circuits, the correcting signal may be allowed to be present during the two stable states on either side of the transient period in the circuit, in which the race hazard is present. (This in general does not apply to sequential circuits).

With reference to table 2, such a signal is seen to be B C.

COMPARISON OF SUGGESTED METHOD WITH THE CONVENTIONAL APPROACH

Minimal NOR circuit 3 will be used to demonstrate the fact that what conventionally are referred to as static, dynamic and essential hazards are one and the same phenomenon, referred to in this article as a race hazard.

As a result of a race between primary signal A and secondary signal S1, a race hazard is present at the output of module 2. If the race is 'won' by the primary signal it is conventionally referred to as static hazard - see diagram 3(a). If on the other hand the race is 'won' by the secondary signal S1, the hazard is referred to as essential. What is referred to conventionally as a dynamic hazard shown in diagram 3(b) is essentially a circuit hazard resulting from a race between a static race hazard and a circuit signal.

All the hazards reveal themselves pictorially in table 3.

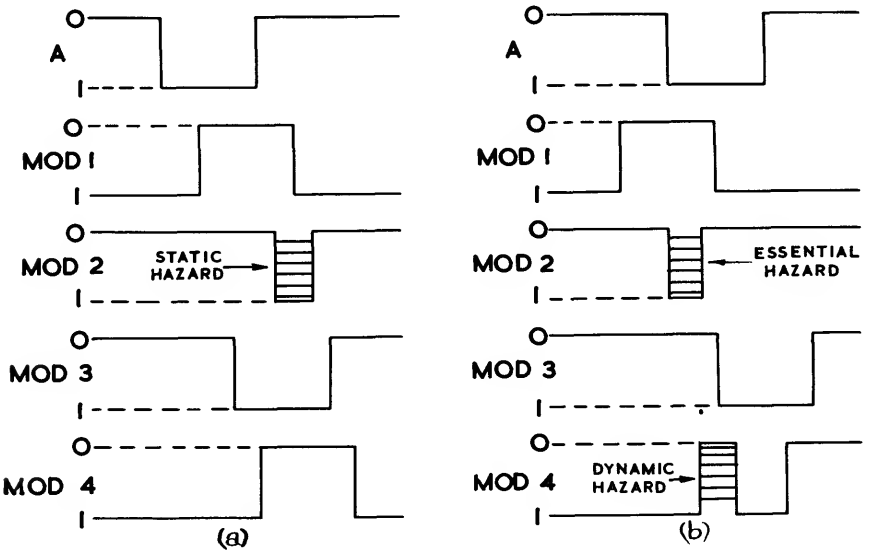


DIAGRAM 3. (a) TIME DIAGRAM OF NOR CIRCUIT 3 DRAWN ON THE ASSUMPTION THAT SIGNAL A AFFECTS MODULE 2 BEFORE SIGNAL S1.

(b) TIME DIAGRAM OF NOR CIRCUIT 3 DRAWN ON THE ASSUMPTION THAT SIGNAL S1 AFFECTS MODULE 2 BEFORE SIGNAL A.

FOR SIMPLICITY SIGNAL B IS ASSUMED TO BE 'O'.

PRIMARY SIGNALS		SECONDARY SIGNALS				
A	B	S1	S2	S3	S4	
O	O	I	O	O	I	1
O	I	O	I	O	O	2
I	I	O	O	O	I	3
I	O	O	O	I	O	4
O	O	I	O	O	I	1

TABLE 3. TRANSITION TABLE OF SWITCHING CIRCUIT 3

PROBLEMS

Problem 1

NOR circuit 3 is to be modified so that it is free of critical race-hazards.

Problem 2

Circuit 5 realises minimally the same switching function as circuit 3, namely $A\,B + \underline{A}\,\underline{B}$. All the race-hazards present in it are to be indicated.

Modify the circuit so that all critical race-hazards, if present, are completely eliminated.

Problem 3

All critical race- hazards in circuit 6 are to be eliminated.

Problem 4

Circuit 8 shows the minimal NOR realisation of a full-adder.

Indicate all the race-hazards present.

Model Answers

1. Eliminating algebraically the effect of the race at the input of module 2.

$$
\begin{aligned}
S2 &= \underline{A}\,(A + B) \\
&= (\underline{A} + 0)(A + B)(0 + B) \\
&= \underline{A}\,(A + B)B \\
&= \underline{A}\,(A.B + B.B) \\
&= \underline{A}\,(A.B + B) \\
&= \underline{A}.B
\end{aligned}
$$

Eliminating effect of race at the input of module 3,

$$
\begin{aligned}
S3 &= \underline{B}(A + B) \\
&= (\underline{B} + 0)(A + B)(A + 0) \\
&= \underline{B}(A + B)A \\
&= \underline{B}(A.A + A\,B) \\
&= A.\underline{B}
\end{aligned}
$$

Now,

$$S4 = \underline{A}\,B + A\,\underline{B}$$

$$= (A + \underline{B})\,(\underline{A} + B)$$

which is race hazard free, since it cannot be reduced to the form $X\,\underline{X}$ or $X + \underline{X}$.

Circuit 4 shows the minimal speed independent NOR circuit realisation.

2. The circuit is completely free of race hazards.

3. All the race hazards present in circuit 5 are shown in table 5.

From the transition table it is seen that the race hazards present in the output of module 5 are due to the hazards in the output of NOR modules 2 and 3. Therefore only the race hazards in the output of modules 2 and 3 need be eliminated.

The algebraic method is the best suited for modifying the circuit.

$$S2 = \underline{B}\,(B + C)$$

$$= (\underline{B} + 0)(B+C)\;(0 + C)$$

$$= \underline{B}\,(B + C)\,C$$

$$= \underline{B}(B\,C + C\,C)$$

$$= \underline{B}\,(B\,C + C)$$

$$= \underline{B}\,C$$

Similarly for S3,

$$S3 = \underline{C}\,(B + C)$$

$$= (\underline{C} + 0)\,(B + C)\,(B + 0)$$

$$= \underline{C}\,(B\,B + B\,C)$$

$$= \underline{C}\,(B + B\,C) = B\,\underline{C}$$

Circuit 7 shows the required race hazard free NOR circuit realising the switching function $A\,B\,C + \underline{B}\,\underline{C}$

4. All the race hazards present in circuit 8 are shown in transition table 6.

NOTE

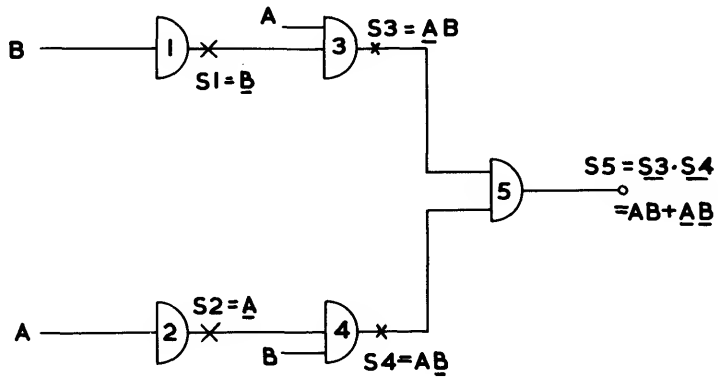
The race between primary signal A and secondary signal S1 is classified as critical so far as it is affecting module 5, and as non-critical so far as module 1 is concerned.

CONCLUSIONS

It has been shown that in combinational circuits the phenomenon conventionally referred to as static hazards, dynamic hazards and essential hazards are basically one and the same phenomenon, which results from the race between two signals. This phenomenon has been called a race hazard.

The excitation table was found to be more useful in the design of circuits from scratch, whereas the transition table provides a very clear picture of what is going on in a given circuit. The algebraic method is the simplest one, but also more prone to error. Therefore, this method is usually used for simple circuits or by experienced switching engineers.

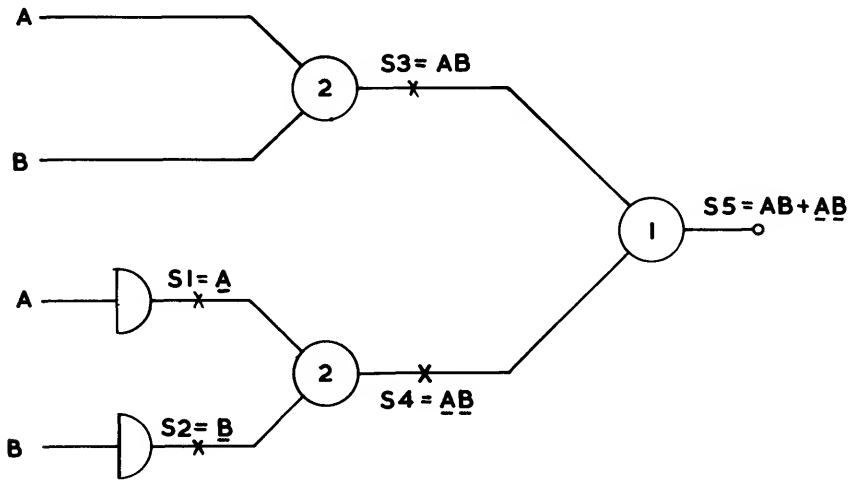
Hazards due to half pulses have not been included because it has been assumed that the circuit will always reach its stable state before the next change of a primary signal.



CIRCUIT 4. MINIMAL RACE-HAZARD-FREE CIRCUIT REALIZING THE INCLUSIVE OR FUNCTION AB+AB

PRIMARY SIGNALS		SECONDARY SIGNALS					
A	B	S1	S2	S3	S4	S5	
0	0	1	1	0	0	1	1
0	1	0	1	1	0	0	2
1	1	0	0	0	0	1	3
1	0	1	0	0	1	0	4
0	0	1	1	0	0	1	1

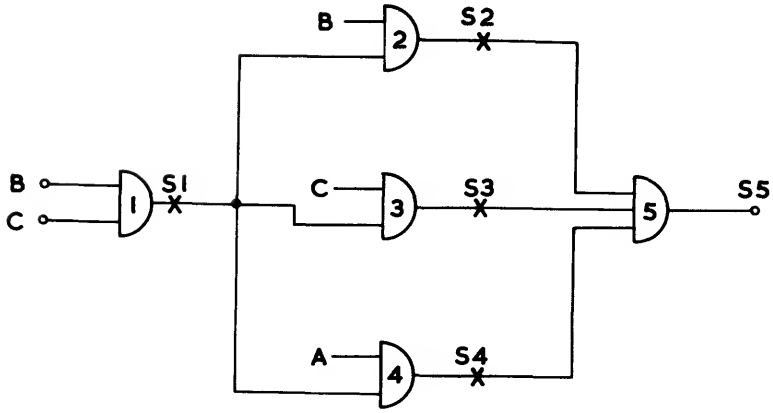
TABLE 4. TRANSITION TABLE OF SWITCHING CIRCUIT 4



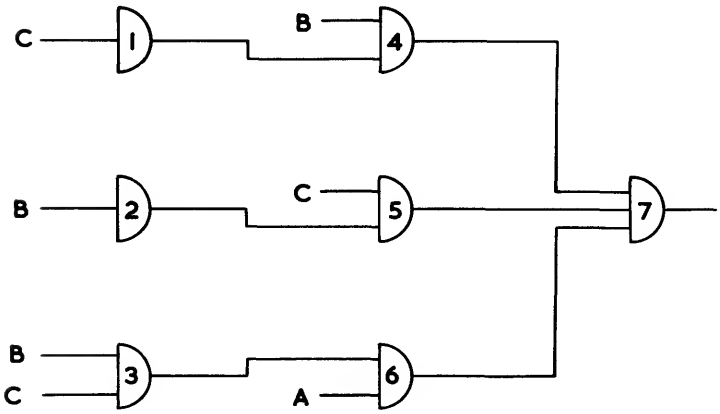
CIRCUIT 5. MINIMAL AND/OR CIRCUIT REALIZING THE INCLUSIVE "OR" FUNCTION AB+$\underline{A}\underline{B}$

	PRIMARY SIGNALS			SECONDARY SIGNALS				
	A	B	C	S1	S2	S3	S4	S5
1	0	0	0	1	0	0	0	1
2	0	1	0	0	0	1	1	0
3	1	1	0	0	0	1	0	0
4	1	0	0	1	0	0	0	1
5	1	0	1	0	1	0	0	0
6	1	1	1	0	0	0	0	1
7	0	1	1	0	0	0	1	0
8	0	0	1	0	1	0	1	0
1	0	0	0	1	0	0	0	0

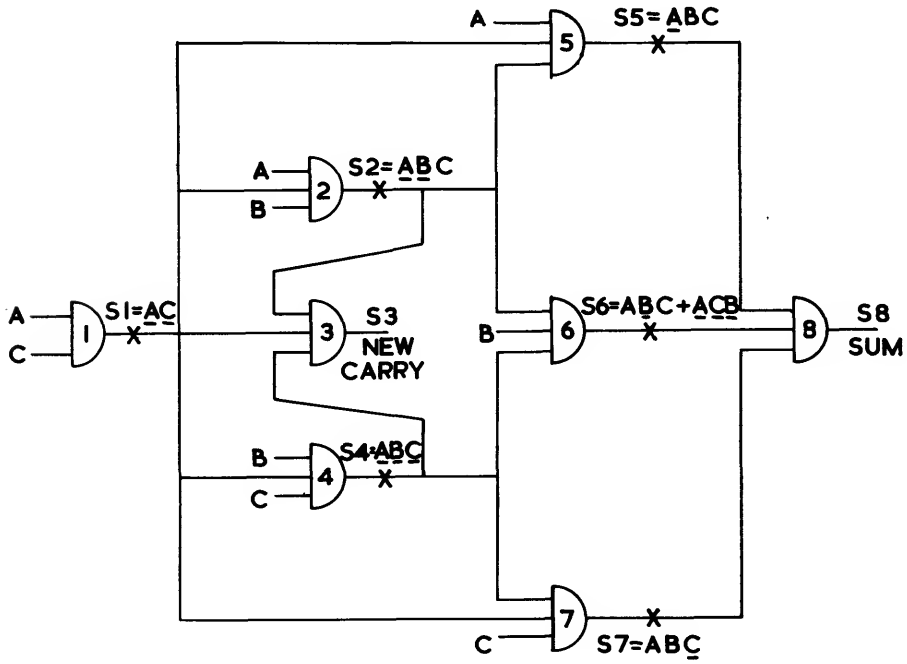
TABLE 5. TRANSITION TABLE OF 'NOR' CIRCUIT 5



CIRCUIT 6. MINIMAL 'NOR' CIRCUIT REALIZING THE SWITCHING FUNCTION $ABC + \underline{B}\underline{C}$



CIRCUIT 7. MINIMAL 'NOR' RACE-HAZARD-FREE CIRCUIT REALIZING THE SWITCHING FUNCTION $ABC + \underline{B}\underline{C}$



CIRCUIT 8. MINIMAL FULL-ADDER CIRCUIT USING 'NOR' MODULES

	PRIMARY SIGNALS			SECONDARY SIGNALS							
	A	B	C	S1	S2	S3	S4	S5	S6	S7	S8
1	0	0	0	1	0	0	0	0	1	0	0
2	0	1	0	1	0	0	0	0	0	0	1
3	1	1	0	0	0	1	0	0	0	1	0
4	1	0	0	0	0	0	1	0	0	0	1
5	1	0	1	0	0	1	0	0	1	0	0
6	1	1	1	0	0	1	0	0	0	0	1
7	0	1	1	0	0	1	0	1	0	0	0
8	0	0	1	0	1	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	1	0	0
4	1	0	0	0	0	0	1	0	0	0	1
2	0	1	0	1	0	0	0	0	0	0	1
7	0	1	1	0	0	1	0	1	0	0	0
3	1	1	0	0	0	1	0	0	0	1	0
6	1	1	1	0	0	1	0	0	0	0	1

TABLE 6. TRANSITION TABLE OF CIRCUIT 8

CHAPTER 4

STEP BY STEP DESIGN OF SPEED INDEPENDENT COMBINATIONAL SWITCHING CIRCUITS

CIRCUIT REALISATION OF MINIMAL SPEED COMBINATIONAL SWITCHING CIRCUITS

SUMMARY

A step by step design of minimal combinational switching circuits, in which the effects of critical races between signals are eliminated is described. A complete list of speed independent three variable circuits is included at the end of this chapter.

Note:

Unless otherwise specified the term race will imply a 'critical race'. The complements of the input signals will not be assumed available.

INTRODUCTION

The design of minimal AND/OR and OR/AND combinational circuits consists essentially of deriving the corresponding minimal race-free algebraic expression of their switching functions. A minimal race-free algebraic expression is a minimal algebraic expression that cannot be reduced to the form $A\,\underline{A}$ or $A + \underline{A}$. For example, of the following four minimal algebraic expressions,

$$f_1 = W X + \underline{W} Z \quad \ldots\ldots (1)$$

$$f_2 = W X + \underline{W} Z + X Z \quad \ldots\ldots (2)$$

$$f_3 = (W + X)(\underline{W} + Z) \quad \ldots\ldots (3)$$

$$f_4 = (W + X)(\underline{W} + Z)(X + Z) \quad \ldots\ldots (4)$$

the first and third are not race-free, since they reduce to $W + \underline{W}$ (when $X = Z = 1$) and $W\,\underline{W}$ (when $X = Z = 0$) respectively, whereas the second and fourth, because they cannot be reduced to either $W + \underline{W}$ or $W\,\underline{W}$ are classified as race-free minimal AND/OR and OR/AND expressions respectively.

As explained previously (see chapter 3), a minimal race-free AND/OR expression can be derived directly from the excitation table of the function by including all adjacent 1 entries in the minimum number of lift sets (see chapter 1). Similarly a minimal OR/AND expression can also be derived directly from the excitation table of the function to be realised by including all the adjacent 0 entries in the minimum number of drop sets (see chapter 1).

The design of minimal speed independent NOR/NOR and NAND/NAND circuits is essentially the same as that for minimal NOR/NOR and NAND/NAND circuits described with two modifications, namely,

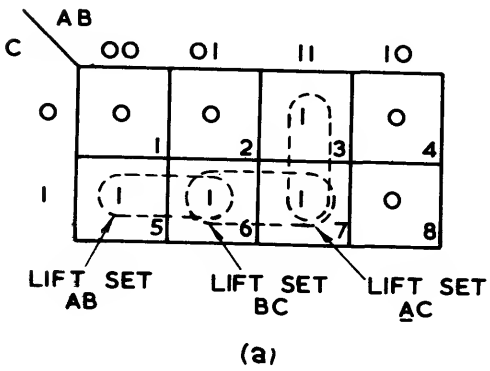
(a) In step 1, the minimal race-free algebraic expression of the function to be realised is derived, and
(b) Step 3, the introduction of substitution signals is omitted.

OUTLINE OF THE METHOD

The method will be outlined by means of design examples.

1. AND/OR Circuits

The minimal AND/OR expression of a function which includes the minimum number of lift-sets (AND terms) between all adjacent 1 - entries in the excitation table, when directly realised, results in the minimal AND/OR static hazard free circuit. E.g. the minimum number of lift-sets that include all adjacent 1 - entries in table 1(a) are $A\,B$, $\underline{A}\,C$ and $B\,C$. Therefore, circuit 1(a) realising directly the expression $f = A\,B + \underline{A}\,C + B\,C$ is the minimal AND/OR static hazard free circuit, specified by table 1(a).



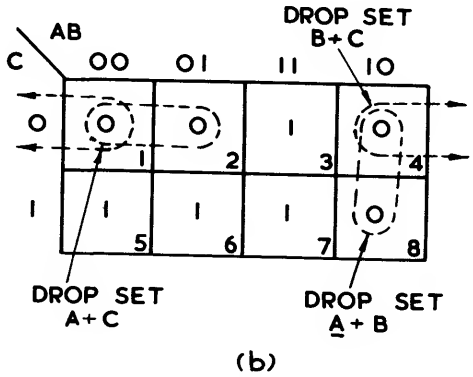
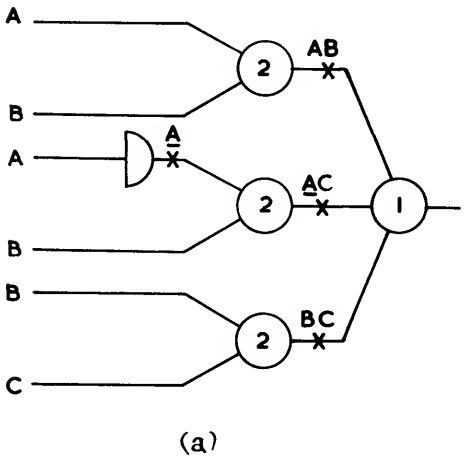
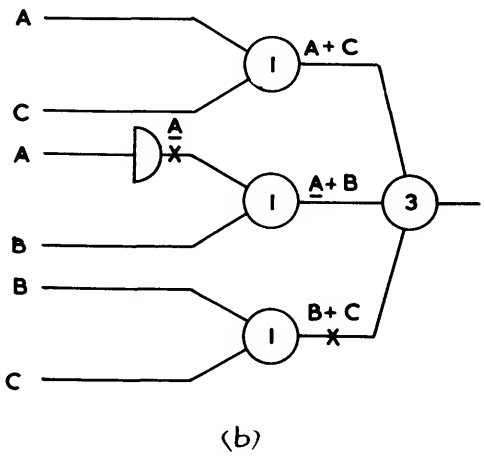


TABLE I. (a) EXCITATION TABLE OF AND/OR FUNCTION AB+ AC
(b) EXCITATION TABLE OF OR/AND FUNCTION (A+C)(A+ B)





CIRCUIT I

(a) MINIMAL AND/OR SPEED INDEPENDENT CIRCUIT REALIZATION OF EXCITATION TABLE 2(a)
(b) MINIMAL AND/OR SPEED INDEPENDENT CIRCUIT REALIZATION OF EXCITATION TABLE 2(b)

2. OR/AND Circuits

The minimal OR/AND expression of a function which includes the minimum number of drop sets (OR terms) between all adjacent 0 entries in the excitation table, when directly realised, results in the minimal OR/AND static hazard free circuit. E.g. The minimum number of drop sets that include all adjacent 0 - entries in table 1(b) are $(A + C)$ $(\underline{A} + B)$ and $(B + C)$. Therefore circuit 1(b) realising directly the expression $f = (A + C)(\underline{A} + B)(B + C)$ is the minimal OR/AND speed independent circuit, specified by table 1(b).

3. NOR/NOR Circuits

The process of optimisation of the algebraic expression of the switching function to be realised is carried out in two steps. Step 3, is included for the sake of uniformity (see design of minimal NOR/NOR circuits in a previous chapter).

DESIGN PROBLEMS

Design Problem 1

The function, whose excitation table is shown in table 1, is to be realised.

Step.1.
Minimal Speed Independent OR/AND expression for f

From either table 1(a) or 1(b),

$$f = \underline{A}\,\underline{C} + \underline{B}\,\underline{C} + A\,\underline{B} \quad \ldots\ldots (1)$$

Applying De Morgan's theorem to equation 1,

$$f = (A + C)(B + C)(\underline{A} + B) \quad \ldots\ldots (2)$$

Step.2.
Merging of OR terms

The second and third OR terms are merged. Therefore

$$f = (A + C)(B + \underline{A}\,C) \quad \ldots\ldots (3)$$

Step.3.
Introduction of Substitution signals

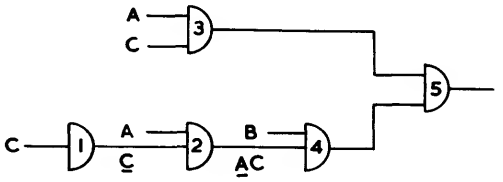
Does not apply.

Equation (3) is therefore the optimised form of the function f.

Step.4.
Circuit Realisation

Circuit 2 shows its circuit realisation.
The circuit contains a final NOR module (5).

Each OR term in equation 3 specifies a driver module - OR term $(A + C)$ specifies driver module 3 and OR term $(B + \underline{A}\,C)$ driver module 4. Driver module 3 is fed by signals A and C, and module 4 by signals B and $\underline{A}\,C$. Module 2 is the product module, generating the product term $\underline{A}\,C$ and module 1 is the inverter module generating the inverted primary signal $\underline{C}$.



CIRCUIT 2. MINIMAL SPEED INDEPENDENT NOR CIRCUIT REALIZING THE SWITCHING FUNCTION SPECIFIED BY EXCITATION TABLE I

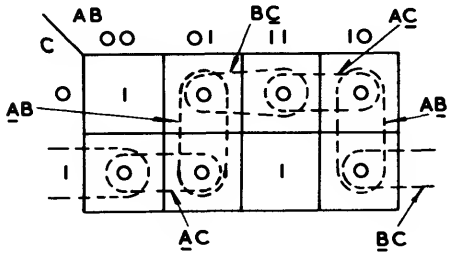
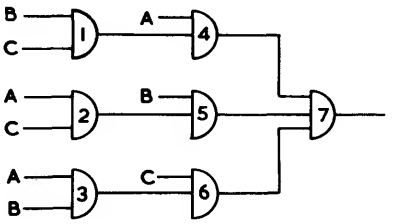


TABLE 2. EXCITATION TABLE OF THE FUNCTION $f = ABC + \underline{A}\,\underline{B}\,\underline{C}$



CIRCUIT 3. MINIMAL SPEED INDEPENDENT NOR CIRCUIT REALIZING THE FUNCTION $f = ABC + \underline{A}\,\underline{B}\,\underline{C}$

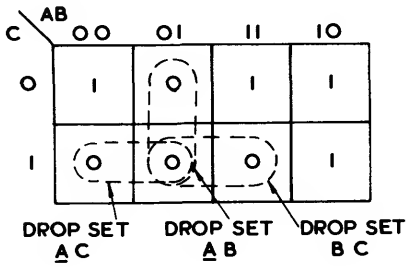
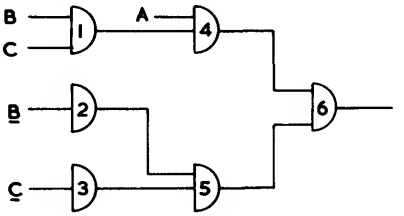


TABLE 3. EXCITATION TABLE OF THE FUNCTION $f = A\underline{B} + A\underline{C} + \underline{B}\,\underline{C}$



CIRCUIT 4. MINIMAL SPEED INDEPENDENT NOR CIRCUIT REALIZING THE FUNCTION $f = A\underline{B} + A\underline{C} + \underline{B}\,\underline{C}$

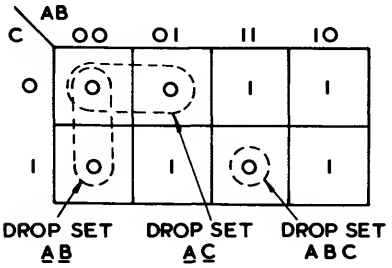
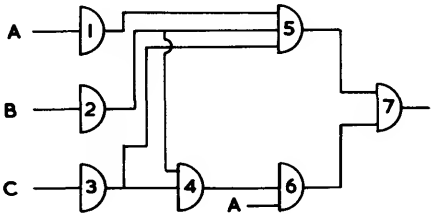


TABLE 4. EXCITATION TABLE OF THE FUNCTION $f = \underline{A}BC + A\underline{B} + A\underline{C}$



CIRCUIT 5. MINIMAL SPEED INDEPENDENT NOR CIRCUIT REALIZING THE FUNCTION $f = \underline{A}BC + A\underline{B} + A\underline{C}$

Design Problem 2.

Function to be realised.

$f = A\,B\,C + \underline{A}\,\underline{B}\,\underline{C}$

Step.1.
Minimal Speed independent OR/AND expression for f.

From table 2,

$\underline{f} = \underline{A}\,B + B\,\underline{C} + A\,\underline{C} + A\,\underline{B} + \underline{B}\,C + \underline{A}\,C$

Applying De Morgans theorem,

$f = (A + \underline{B})\,(\underline{B} + C)\,(\underline{A} + C)\,(\underline{A} + B)\,(B + \underline{C})(A + \underline{C})$

Step.2.
Merging of OR terms

The expression is next merged.

$f = (A + \underline{B}\,\underline{C})\,(\underline{A}\,\underline{B} + C)\,(B + \underline{A}\,\underline{C})$

Step.3.
Introduction of Substitution Signals

Does not apply.

Step.4.
Circuit Realisation

For circuit realisation, see NOR circuit 3.

Design Problem 3.

Function to be realised: $f = A\,\underline{B} + A\,\underline{C} + \underline{B}\,\underline{C}$

Step.1.
Minimal Speed Independent OR/AND expression for f

From table 3,

$\underline{f} = \underline{A}\,B + \underline{A}\,C + B\,C$

Applying De Morgans Theorem,

$f = (A + \underline{B})\,(A + \underline{C})\,(\underline{B} + \underline{C})$

Step.2.
Merging of OR terms

First and second OR terms are merged to $(A + \underline{B}\,\underline{C})$. Therefore,

$f = (A + \underline{B}\,\underline{C})\,(\underline{B} + \underline{C})$

Step.3.
Introduction of Substitution Signals

Does not apply.

Step.4.
Circuit Realisation

See Circuit 4.

Design Problem 4.

Function to be realised.

$f = \underline{A}\,B\,C + A\,\underline{B} + A\,\underline{C}$ ..... (1)

Step.1.

Minimal OR/AND expression of f

From table 4,

$\underline{f} = \underline{A}\,\underline{B} + \underline{A}\,\underline{C} + A\,B\,C$ ..... (2)

Applying De Morgans theorem to equation 2,

$f = (A + B)\,(A + C)\,(\underline{A} + \underline{B} + \underline{C})$ ..... (3)

Step.2.
Merging of OR terms

OR terms (A + B) and (A + C) would not normally be merged. But because both $\underline{B}$ and $\underline{C}$ are generated, they are merged. Therefore,

$f = (A + B\,C)\,(\underline{A} + \underline{B} + \underline{C})$

Step.3.
Introduction of Substitution signals.

Does not apply.

Step.4.
Circuit Realisation

see circuit 5.

Design Problem 5.

Function to be realised,

$f = \underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$ ..... (1)

Step.1.
Minimal speed independent OR/AND expression of f

From table 5,

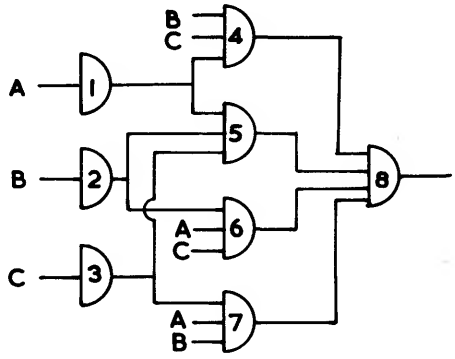
$\underline{f} = \underline{A}\,\underline{B}\,C + \underline{A}\,B\,\underline{C} + A\,B\,C + A\,\underline{B}\,\underline{C}$ ..... (2)

C \ AB	00	01	11	10
0	1	0	1	0
1	0	1	0	1

DROP ABC

DROP SET $\underline{A}\underline{B}C$ DROP SET $\underline{A}B\underline{C}$ DROP SET $A\underline{B}\underline{C}$

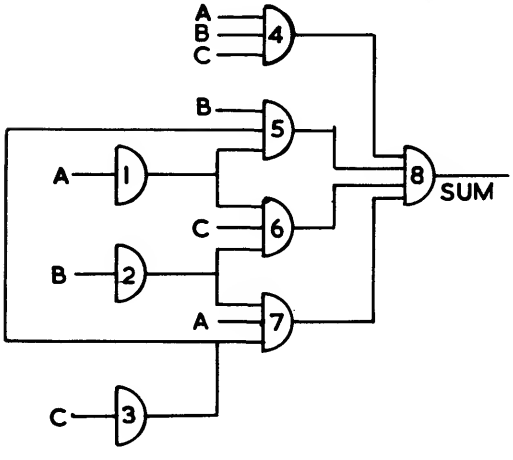
TABLE 5. EXCITATION TABLE OF THE FUNCTION $f = \underline{A}\underline{B}\underline{C} + AB\underline{C} + A\underline{B}C + \underline{A}BC$

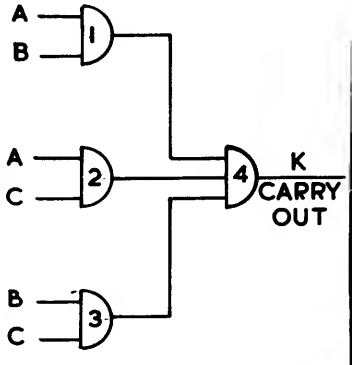


CIRCUIT 6. MINIMAL SPEED INDEPENDENT NOR CIRCUIT REALIZING THE FUNCTION $f = \underline{A}\underline{B}\underline{C} + AB\underline{C} + A\underline{B}C + \underline{A}BC$

A	0	0	1	1	1	1	0	0
B	0	1	1	0	0	1	1	0
C	0	0	0	0	1	1	1	1
S	0	1	0	1	0	1	0	1
K	0	0	1	0	1	1	1	0

TABLE 6. ADDITION TABLE OF VARIABLES A, B & C (OLD CARRY). S = SUM, K = CARRY OUT





CIRCUIT 7. SPEED INDEPENDENT NOR CIRCUIT REALIZATION OF A FULL-ADDER UNIT

Applying De Morgans theorem,

$$f = (A + B + \underline{C})\ (A + \underline{B} + C)\ (\underline{A} + \underline{B} + \underline{C})\ (\underline{A} + B + C) \quad \ldots\ldots (3)$$

Step.2.
Merging of OR terms

No merging possible.

Step.3.
Introduction of Substitution signals.

Does not apply.

Step.4.
Circuit Realisation

See Circuit 6.

Design Problem 6.

To be designed. A minimal speed independent full adder unit.

Step.1.
Minimal speed independent OR/AND expression for S(sum) and K(carry out)

From table 6,

$$\underline{S} = \underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C \text{ and} \quad \ldots\ldots (1)$$

$$\underline{K} = \underline{A}\,\underline{B} + \underline{A}\,\underline{C} + \underline{B}\,\underline{C} \quad \ldots\ldots (2)$$

Applying De Morgans theorem,

$$S = (A + B + C)\ (\underline{A} + \underline{B} + C)\ (\underline{A} + B + \underline{C})\ (A + \underline{B} + \underline{C}) \quad \ldots\ldots (3)$$

and

$$K = (A + B)\ (A + C)\ (B + C) \quad \ldots\ldots (4)$$

Step.2.
Merging of OR terms

No merging possible.

Step.3.
Introduction of Substitution signals.

Not applicable.

Step.4.
Circuit Realisation

See Circuit 7.

NAND-NAND CIRCUIT REALISATION

To realise a given function using NAND modules, interchange the 'pl uses' and 'dots' in the original expression. The NOR circuit configuration corresponding to the derived function will realise the initial function, if the NOR modules are replaced by NAND modules. A useful point to bear in mind when transforming Boolean functions is to include all product terms in brackets before the transformation. The brackets are not affected by the transformation.

Example

Assume function $f = \underline{A}\,\underline{C} + A\,C$ is to be realised using NAND modules.

The product terms are first included in brackets,

$f = (\underline{A}\,\underline{C}) + (A\,C)$

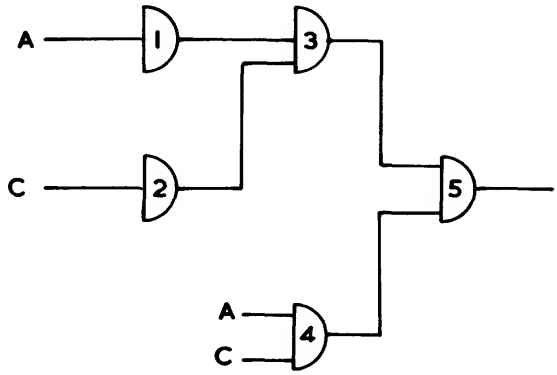
Interchanging 'pluses' and 'dots'

$= (\underline{A} + \underline{C})\,(A + C)$

$= A\,\underline{A} + A\,\underline{C} + \underline{A}\,C + C\,\underline{C}$

$= A\,\underline{C} + \underline{A}\,C$

The NOR circuit corresponding to this function is shown in circuit 8. If in this circuit configuration the NOR modules are replaced by NAND modules, the function $A\,C + \underline{A}\,\underline{C}$ will be realised.



CIRCUIT 8. SPEED INDEPENDENT NAND CIRCUIT REALIZATION OF $f = AC + \underline{A}\,\underline{C}$

INDEX NUMBER	MINIMAL "AND - OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-7/-1	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C}$	1	
-7/-1/+3	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C$	2	
-7/-1/+3/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	3	
-7/-1/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + \underline{A}\,B\,C$	2	B A C
-7	$\underline{A}\,\underline{B}\,\underline{C}$	4	
-7/+3/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B$	5	
-7/+3/b	$\underline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C$	1	
-7/+3/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C$	6	
-7/+3/+5/b	$\underline{A}\,\underline{B}\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	2	C B A
-7/+3/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C + B\,C$	7	
-7/+3/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + B\,C$	6	B A C
-7/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,C$	5	A C B
-7/+5/b	$\underline{A}\,\underline{B}\,\underline{C} + \underline{A}\,B\,C$	1	C B A
-7/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,C + B\,C$	6	C B A
-7/+6	$\underline{A}\,\underline{B}\,\underline{C} + B\,C$	5	C B A
-7/+7	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,C$	8	
-6/-5/-3	$\underline{A}\,\underline{B} + \underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	9	
-6/-5/-3/+7	$\underline{A}\,\underline{B} + \underline{A}\,\underline{C} + \underline{B}\,\underline{C} + A\,B\,C$	10	
-6/-5	$\underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	11	
-6/-5/+5	$A\,C + \underline{A}\,\underline{C} + \underline{B}\,\underline{C}$	12	
-6/-5/+6	$\underline{A}\,\underline{C} + B\,C + \underline{B}\,\underline{C}$	12	B A C
-6/-5/+7	$\underline{A}\,\underline{C} + \underline{B}\,\underline{C} + A\,B\,C$	13	
-6/-3/-1	$A\,C + \underline{B}\,\underline{C} + A\,\underline{B}$	14	
-6/-3/-1/+5	$A\,\underline{B} + A\,\underline{C} + \underline{B}\,\underline{C} + \underline{A}\,B\,C$	15	
-6/-3/a	$A\,\underline{C} + \underline{B}\,\underline{C}$	16	
-6/-3/b	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C}$	11	A C B
-6/-3/+3/a	$A\,\underline{C} + \underline{A}\,C + \underline{B}\,\underline{C}$	17	
-6/-3/+3/b	$A\,B + \underline{A}\,\underline{B} + \underline{B}\,\underline{C}$	12	A C B
-6/-3/+3/+6	$\underline{A}\,C + A\,\underline{C} + B\,C + \underline{B}\,\underline{C}$	18	
-6/-3/+5	$A\,\underline{C} + \underline{A}\,B\,C + \underline{B}\,\underline{C}$	19	
-6/-3/+6/a	$A\,\underline{C} + \underline{B}\,\underline{C} + B\,C$	20	

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-6/-3/+6/b	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C} + B\,C$	12	C A B
-6/-3/+7	$\underline{A}\,\underline{B} + \underline{B}\,\underline{C} + A\,B\,C$	13	A C B
-6/-1/a	$\underline{A} + \underline{B}\,\underline{C}$	21	
-6/-1/b	$A\,\underline{B} + \underline{B}\,\underline{C}$	16	A C B
-6/-1/+1	$A\,\underline{B} + \underline{A}\,B + \underline{B}\,\underline{C}$	17	A C B
-6/-1/+1/+6	$\underline{A}\,B + B\,C + A\,\underline{B} + \underline{B}\,\underline{C}$	18	A C B
-6/-1/+5	$A\,\underline{B} + \underline{A}\,B\,C + \underline{B}\,\underline{C}$	19	A C B
-6/-1/+6/a	$\underline{A} + \underline{B}\,\underline{C} + B\,C$	22	
-6/-1/+6/b	$A\,\underline{B} + \underline{B}\,\underline{C} + B\,C$	20	A C B
-6	$\underline{B}\,\underline{C}$	23	
-6/+1/a	$A + \underline{B}\,\underline{C}$	24	
-6/+1/b	$\underline{A}\,B + \underline{B}\,\underline{C}$	25	
-6/+1/+5	$A\,C + \underline{A}\,B + \underline{B}\,\underline{C}$	26	
-6/+1/+6/a	$\underline{A}\,B + \underline{B}\,\underline{C} + B\,C$	12	B A C
-6/+1/+6/b	$A + \underline{B}\,\underline{C} + B\,C$	27	
-6/+3/a	$A\,B + \underline{B}\,\underline{C}$	28	
-6/+3/b	$\underline{A}\,C + \underline{B}\,\underline{C}$	25	A C B
-6/+3/+3	$A\,B + \underline{A}\,C + \underline{B}\,\underline{C}$	26	A C B
-6/+3/+6/a	$A\,B + B\,C + \underline{B}\,\underline{C}$	20	A B C
-6/+3/+6/b	$\underline{A}\,C + B\,C + \underline{B}\,\underline{C}$	12	B A C
-6/+5/a	$\underline{A}\,B\,C + \underline{B}\,\underline{C}$	29	
-6/+5/b	$A\,C + \underline{B}\,\underline{C}$	28	A C B
-6/+5/+6	$A\,C + B\,C + \underline{B}\,\underline{C}$	20	A C B
-6/+6	$\underline{B}\,\underline{C} + B\,C$	30	
-6/+7	$\underline{B}\,\underline{C} + A\,B\,C$	31	
-5/-3/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C}$	32	
-5/-3/b	$\underline{A}\,\underline{C} + \underline{A}\,\underline{B}$	11	C B A
-5/-3/+1	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	33	
-5/-3/+1/+7	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	34	
-5/-3/+3	$A\,B + \underline{A}\,\underline{B} + \underline{A}\,\underline{C}$	12	B C A
-5/-3/+5	$A\,C + \underline{A}\,\underline{C} + \underline{A}\,\underline{B}$	12	C B A
-5/-3/+7/a	$A\,\underline{B}\,\underline{C} + \underline{A}\,B\,\underline{C} + A\,B\,C$	35	
-5/-3/+7/b	$\underline{A}\,\underline{C} + \underline{A}\,\underline{B} + A\,B\,C$	13	C B A
-5/-2/a	$\underline{A}\,\underline{C} + B\,\underline{C}$	16	B A C
-5/-2/b	$\underline{B} + \underline{A}\,\underline{C}$	21	B A C

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-5/-2/+1	$\underline{A}\,B + \underline{A}\,\underline{C} + B\,\underline{C}$	14	B C A
-5/-2/+1/+3	$\underline{A}\,B + B\,\underline{C} + \underline{A}\,\underline{C} + A\,\underline{B}\,C$	15	B A C
-5/-2/+2	$\underline{A}\,\underline{C} + B\,\underline{C} + \underline{B}\,C$	17	B A C
-5/-2/+3	$\underline{A}\,\underline{C} + B\,\underline{C} + A\,\underline{B}\,C$	19	B A C
-5/-2/+5/a	$A\,C + \underline{A}\,\underline{C} + B\,\underline{C}$	20	B A C
-5/-2/+5/b	$\underline{B} + \underline{A}\,\underline{C} + A\,C$	22	B A C
-5/-1	$A\,\underline{B} + \underline{A}\,\underline{C}$	25	B A C
-5/-1/+1	$\underline{A}\,\underline{C} + A\,\underline{B} + \underline{A}\,B$	17	B C A
-5/-1/+1/+5	$A\,\underline{B} + A\,C + \underline{A}\,B + \underline{A}\,\underline{C}$	18	B C A
-5/-1/+5	$A\,\underline{B} + A\,C + \underline{A}\,\underline{C}$	12	A B C
-5/-1/+6	$A\,\underline{B} + \underline{A}\,\underline{C} + B\,C$	26	B A C
-5/a	$A\,\underline{B}\,\underline{C}$	36	
-5/b	$\underline{A}\,\underline{C}$	23	B A C
-5/+1/a	$\underline{A}\,B + A\,\underline{B}\,\underline{C}$	37	
-5/+1/b	$\underline{A}\,B + \underline{A}\,\underline{C}$	16	B C A
-5/+1/c	$A\,\underline{B}\,\underline{C} + \underline{A}\,\underline{B}\,C$	32	A C B
-5/+1/+3/a	$\underline{A}\,B + \underline{A}\,C + A\,\underline{B}\,\underline{C}$	38	
-5/+1/+3/b	$\underline{A}\,B + \underline{A}\,\underline{C} + A\,\underline{B}\,C$	19	B C A
-5/+1/+3/+6	$\underline{A}\,C + B\,C + \underline{A}\,B + A\,\underline{B}\,\underline{C}$	39	
-5/+1/+5	$\underline{A}\,B + \underline{A}\,\underline{C} + A\,C$	20	B C A
-5/+1/+6	$\underline{A}\,B + A\,\underline{B}\,\underline{C} + B\,C$	40	
-5/+1/+7	$A\,\underline{B}\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	35	A C B
-5/+2/a	$\underline{A}\,\underline{C} + B$	24	B A C
-5/+2/b	$\underline{A}\,\underline{C} + \underline{B}\,C$	25	B C A
-5/+2/+3	$A\,B + \underline{A}\,\underline{C} + \underline{B}\,C$	26	B C A
-5/+2/+5/a	$A\,C + \underline{A}\,\underline{C} + \underline{B}\,C$	12	B C A
-5/+2/+5/b	$A\,C + \underline{A}\,\underline{C} + B$	27	B A C
-5/+3/a	$A\,\underline{B}\,C + \underline{A}\,\underline{C}$	29	B A C
-5/+3/b	$A\,\underline{B}\,\underline{C} + \underline{A}\,C$	37	A C B
-5/+3/c	$A\,B + \underline{A}\,\underline{C}$	28	B A C
-5/+3/+5	$A\,B + A\,C + \underline{A}\,\underline{C}$	20	B A C
-5/+3/+6	$\underline{A}\,C + A\,\underline{B}\,\underline{C} + B\,C$	40	A C B
-5/+5/a	$\underline{A}\,B\,C + A\,\underline{B}\,\underline{C}$	41	
-5/+5/b	$A\,C + \underline{A}\,\underline{C}$	30	B A C
-5/+5/+6	$A\,C + B\,C + \underline{A}\,\underline{C}$	20	B C A

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-5/+6/a	$A\,\underline{B}\,\underline{C} + B\,C$	42	
-5/+6/b	$\underline{A}\,\underline{C} + B\,C$	28	B C A
-5/+7/a	$A\,\underline{B}\,\underline{C} + A\,B\,C$	43	
-5/+7/b	$\underline{A}\,\underline{C} + A\,B\,C$	31	B A C
-4/-3	$\underline{A}\,\underline{B} + \underline{C}$	21	C B A
-4/-3/+3	$A\,B + \underline{A}\,\underline{B} + \underline{C}$	22	C B A
-4/-2/-1	$\underline{A} + \underline{B} + \underline{C}$	44	
-4/-2	$\underline{B} + \underline{C}$	45	
-4/-2/+1	$A + \underline{B} + \underline{C}$	46	
-4/-1/a	$A\,\underline{B} + \underline{C}$	47	
-4/-1/b	$\underline{A} + \underline{C}$	45	B A C
-4/-1/+1	$A\,\underline{B} + \underline{A}\,B + \underline{C}$	48	
-4/-1/+2	$\underline{A} + B + \underline{C}$	46	B A C
-4	$\underline{C}$	49	
-4/+1/a	$A + \underline{C}$	50	
-4/+1/b	$\underline{A}\,B + \underline{C}$	47	B A C
-4/+1/+2	$A + B + \underline{C}$	51	
-4/+2	$B + \underline{C}$	50	B A C
-4/+3	$A\,B + \underline{C}$	52	
-3/-3	$A\,\underline{C} + \underline{A}\,\underline{B}$	25	C A B
-3/-3/+3/a	$A\,\underline{C} + \underline{A}\,\underline{B} + \underline{A}\,C$	17	A B C
-3/-3/+3/b	$A\,B + \underline{A}\,\underline{B} + A\,\underline{C}$	12	A C B
-3/-3/+3/+3	$A\,B + A\,\underline{C} + \underline{A}\,\underline{B} + \underline{A}\,C$	18	C B A
-3/-3/+6	$\underline{A}\,\underline{B} + A\,\underline{C} + B\,C$	26	C A B
-3/-2/a	$A\,\underline{C} + B\,\underline{C}$	53	
-3/-2/b	$A\,\underline{C} + \underline{B}$	47	A C B
-3/-2/c	$\underline{A}\,\underline{B} + B\,\underline{C}$	25	C B A
-3/-2/+1	$A\,\underline{C} + B\,\underline{C} + \underline{A}\,\underline{B}\,C$	38	C B A
-3/-2/+1/+3	$A\,\underline{C} + B\,\underline{C} + A\,B + \underline{A}\,\underline{B}\,C$	39	C B A
-3/-2/+2/a	$A\,\underline{C} + B\,\underline{C} + \underline{B}\,C$	54	
-3/-2/+2/b	$\underline{A}\,\underline{B} + B\,\underline{C} + \underline{B}\,C$	17	C A B
-3/-2/+2/+3	$A\,B + B\,\underline{C} + \underline{A}\,\underline{B} + \underline{B}\,C$	18	C A B
-3/-2/+3/a	$A\,\underline{C} + B\,\underline{C} + A\,B$	55	
-3/-2/+3/b	$A\,B + \underline{A}\,\underline{B} + B\,\underline{C}$	12	
-3/-2/+3/c	$A\,\underline{C} + \underline{A}\,C + \underline{B}$	48	A C B
-3/-2/+3/d	$A\,\underline{C} + \underline{A}\,C + B\,\underline{C}$	54	B A C
-3/-2/+5	$\underline{A}\,\underline{B} + A\,C + B\,\underline{C}$	26	C B A
-3/-1/a	$A\,\underline{B} + A\,\underline{C}$	56	

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-3/-1/b	$A\,\underline{B} + \underline{A}\,B\,\underline{C}$	37	B A C
-3/-1/c	$\underline{A}\,\underline{B} + A\,B\,\underline{C}$	29	C B A
-3/-1/+1	$A\,\underline{B} + \underline{A}\,B + A\,\underline{C}$	57	
-3/-1/+2/a	$\underline{A}\,\underline{B} + A\,B\,\underline{C} + \underline{B}\,C$	19	C A B
-3/-1/+2/b	$A\,\underline{B} + \underline{B}\,C + \underline{A}\,B\,\underline{C}$	38	B A C
-3/-1/+2/+3/a	$\underline{A}\,\underline{B} + A\,B\,\underline{C} + \underline{A}\,C + \underline{B}\,C$	15	C B A
-3/-1/+2/+5	$A\,\underline{B} + \underline{B}\,C + A\,C + \underline{A}\,B\,\underline{C}$	39	B A C
-3/-1/+3/a	$A\,\underline{C} + A\,\underline{B} + \underline{A}\,C$	57	A C B
-3/-1/+3/b	$\underline{A}\,\underline{B} + \underline{A}\,C + A\,B\,\underline{C}$	19	C B A
-3/-1/+5/a	$A\,\underline{C} + A\,\underline{B} + \underline{A}\,B\,C$	58	
-3/-1/+5/b	$A\,\underline{B} + \underline{A}\,B\,\underline{C} + A\,C$	40	B A C
-3/a	$A\,\underline{C}$	59	
-3/b	$\underline{A}\,B\,\underline{C}$	36	B A C
-3/c	$\underline{A}\,\underline{B}$	23	C B A
-3/+1/a	$A\,\underline{C} + \underline{A}\,B$	60	
-3/+1/b	$\underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	32	B C A
-3/+1/c	$A\,\underline{C} + \underline{A}\,\underline{B}\,C$	37	C A B
-3/+1/+2	$A\,\underline{C} + \underline{B}\,C + \underline{A}\,B$	61	
-3/+1/+3/a	$A\,\underline{C} + A\,B + \underline{A}\,\underline{B}\,C$	40	C A B
-3/+1/+3/b	$\underline{A}\,B + \underline{A}\,C + A\,\underline{C}$	54	B C A
-3/+1/+7	$\underline{A}\,B\,\underline{C} + \underline{A}\,\underline{B}\,C + A\,B\,C$	35	C B A
-3/+2/a	$B + A\,\underline{C}$	62	
-3/+2/b	$\underline{A}\,B\,\underline{C} + \underline{B}\,C$	37	B C A
-3/+2/c	$A\,\underline{C} + \underline{B}\,C$	60	C A B
-3/+2/d	$\underline{A}\,\underline{B} + \underline{B}\,C$	16	C A B
-3/+2/+3/a	$A\,\underline{C} + \underline{A}\,C + B$	63	
-3/+2/+3/b	$A\,\underline{C} + \underline{B}\,C + \underline{A}\,C$	57	C A B
-3/+2/+3/c	$\underline{A}\,\underline{B} + \underline{B}\,C + A\,B$	20	C A B
-3/+2/+3/d	$\underline{A}\,\underline{B} + \underline{B}\,C + \underline{A}\,C$	14	C A B
-3/+2/+5	$A\,C + \underline{B}\,C + \underline{A}\,B\,\underline{C}$	40	B C A
-3/+3/a	$A\,\underline{C} + \underline{A}\,C$	64	
-3/+3/b	$A\,B + A\,\underline{C}$	65	
-3/+3/c	$A\,B + \underline{A}\,\underline{B}$	30	C B A
-3/+3/d	$\underline{A}\,\underline{B} + \underline{A}\,C$	16	C B A
-3/+3/c	$A\,\underline{B}\,C + \underline{A}\,B\,\underline{C}$	41	B A C
-3/+3/+3/a	$A\,\underline{C} + \underline{A}\,C + A\,B$	66	

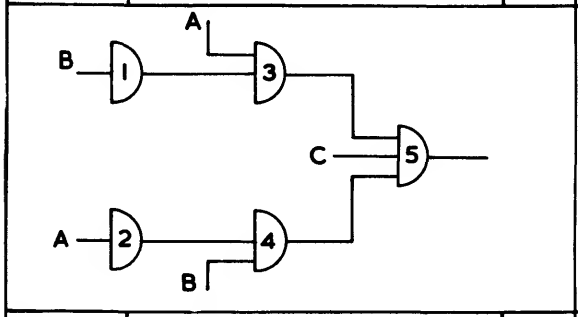
INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-3/+3/+3/b	$\underline{A}\,\underline{B} + \underline{A}\,C + A\,B$	20	C B A
-3/+3/+4	$\underline{A}\,\underline{B} + A\,B + C$	27	C B A
-3/+3/+5	$\underline{A}\,\underline{B} + A\,B + A\,C$	20	C A B
-3/+3/+6/a	$A\,B + \underline{A}\,\underline{B} + B\,C$	20	C B A
-3/+3/+6/b	$A\,\underline{C} + \underline{A}\,C + B\,C$	66	C B A
-3/+4	$\underline{A}\,\underline{B} + C$	24	C B A
-3/+5/a	$\underline{A}\,B\,C + A\,\underline{C}$	67	
-3/+5/b	$\underline{A}\,\underline{B} + A\,C$	28	C A B
-3/+5/c	$\underline{A}\,B\,\underline{C} + A\,C$	42	B A C
-3/+6/a	$A\,\underline{C} + B\,C$	68	
-3/+6/b	$\underline{A}\,\underline{B} + B\,C$	28	C B A
-3/+7/a	$\underline{A}\,\underline{B} + A\,B\,C$	31	C B A
-3/+7/b	$A\,B\,C + \underline{A}\,B\,\underline{C}$	43	B A C
-2/-1/a	$A\,\underline{B} + B\,\underline{C}$	60	B A C
-2/-1/b	$\underline{A} + B\,C$	47	B C A
-2/-1/c	$\underline{A} + \underline{B}$	45	C B A
-2/-1/+1	$A\,\underline{B} + \underline{A}\,B + B\,\underline{C}$	57	B A C
-2/-1/+2/a	$A\,\underline{B} + B\,\underline{C} + \underline{B}\,C$	54	A C B
-2/-1/+2/b	$\underline{A} + B\,\underline{C} + \underline{B}\,C$	48	B C A
-2/-1/+3	$A\,\underline{B} + \underline{A}\,C + B\,\underline{C}$	61	B A C
-2/-1/+4	$\underline{A} + \underline{B} + C$	46	C B A
-2/a	$\underline{B}$	49	- C B
-2/b	$B\,\underline{C}$	59	B - C
-2/+1/a	$\underline{A}\,B + B\,\underline{C}$	56	B A C
-2/+1/b	$\underline{A}\,\underline{B}\,C + B\,\underline{C}$	37	C B A
-2/+1/c	$A + B\,\underline{C}$	62	B A C
-2/+1/d	$A + \underline{B}$	50	- C B
-2/+1/+2/a	$\underline{A}\,B + B\,\underline{C} + \underline{B}\,C$	57	B C A
-2/+1/+2/b	$A + B\,\underline{C} + \underline{B}\,C$	63	B A C
-2/+1/+2/c	$A\,\underline{B} + \underline{B}\,C + B\,\underline{C}$	54	A C B
-2/+1/+3/a	$A\,B + B\,\underline{C} + \underline{A}\,\underline{B}\,C$	40	C B A
-2/+1/+3/b	$\underline{A}\,B + A\,\underline{B}\,C + B\,\underline{C}$	58	B A C
-2/+1/+4	$A + \underline{B} + C$	51	A C B

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF. CCT TO READ.
-2/+2	$B\underline{C} + \underline{B}C$	64	B - C
-2/+2/+3/a	$AB + B\underline{C} + \underline{B}C$	66	B A C
-2/+2/+3/b	$B\underline{C} + \underline{B}C + \underline{A}C$	57	C B A
-2/+2/+5	$AC + B\underline{C} + \underline{B}C$	66	C A B
-2/+3/a	$A\underline{B}C + B\underline{C}$	67	B A C
-2/+3/b	$\underline{A}C + B\underline{C}$	60	C B A
-2/+3/c	$AB + B\underline{C}$	65	B A C
-2/+3/d	$\underline{B} + \underline{A}C$	47	C A B
-2/+4	$\underline{B} + C$	50	C - B
-2/+5/a	$B\underline{C} + AC$	68	B A C
-2/+5/b	$\underline{B} + AC$	52	A C B
-1/a	$AB\underline{C}$	69	
-1/b	$A\underline{B}$	59	A - B
-1/c	$\underline{A}$	49	- - A
-1/+1/a	$AB\underline{C} + \underline{A}\underline{B}C$	41	C B A
-1/+1/b	$A\underline{B} + \underline{A}B$	64	A C B
-1/+1/+2	$A\underline{B} + \underline{A}B + \underline{B}C$	54	C A B
-1/+1/+3	$A\underline{B} + \underline{A}B + \underline{A}C$	54	C B A
-1/+1/+4	$A\underline{B} + \underline{A}B + C$	63	A C B
-1/+1/+5	$A\underline{B} + \underline{A}B + AC$	66	A C B
-1/+1/+6	$A\underline{B} + \underline{A}B + BC$	66	B C A
-1/+2/a	$AB\underline{C} + \underline{B}C$	67	C A B
-1/+2/b	$A\underline{B} + \underline{B}C$	53	A C B
-1/+2/c	$\underline{A} + \underline{B}C$	47	C B A
-1/+2/d	$\underline{A} + B$	50	B - A
-1/+2/+3	$AB\underline{C} + \underline{B}C + \underline{A}C$	58	C B A
-1/+2/+4	$\underline{A} + B + C$	51	C B A
-1/+2/+5	$A\underline{B} + \underline{B}C + AC$	55	A C B
-1/+3/a	$AB\underline{C} + A\underline{B}C$	70	
-1/+3/b	$AB\underline{C} + \underline{A}C$	67	C B A
-1/+3/c	$A\underline{B} + \underline{A}C$	60	A C B
-1/+3/+5	$AB\underline{C} + A\underline{B}C + \underline{A}BC$	71	
-1/+4/a	$A\underline{B} + C$	62	A C B
-1/+4/b	$\underline{A} + C$	50	C - A
-1/+5/a	$AB\underline{C} + \underline{A}BC$	70	B A C

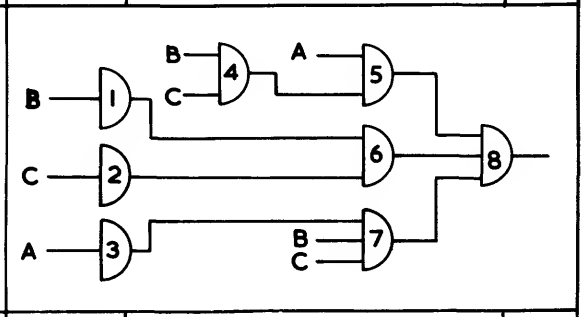
INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
-1/+5/b	$A\,\underline{B} + \underline{A}\,B\,C$	67	A C B
-1/+5/c	$A\,\underline{B} + A\,C$	65	A C B
-1/+5/d	$\underline{A}\,B + A\,C$	68	B C A
-1/+6/a	$A\,\underline{B} + B\,C$	68	A C B
-1/+6/b	$\underline{A} + B\,C$	52	C B A
+1/a	A	72	
+1/b	$\underline{A}\,\underline{B}\,C$	36	C B A
+1/c	$\underline{A}\,B$		B - A
+1/+2/a	$A + B$	73	
+1/+2/b	$A + \underline{B}\,C$	62	C A B
+1/+2/c	$\underline{A}\,B + \underline{B}\,C$	60	B C A
+1/+2/+4	$A + B + C$	74	
+1/+3/a	$\underline{A}\,\underline{B}\,C + A\,B$	42	C B A
+1/+3/b	$\underline{A}\,B + A\,\underline{B}\,C$	67	B C A
+1/+3/c	$\underline{A}\,B + \underline{A}\,C$	53	C B A
+1/+3/+6	$\underline{A}\,B + \underline{A}\,C + B\,C$	55	C B A
+1/+4/a	$A + C$	73	A C -
+1/+4/b	$\underline{A}\,B + C$	62	B C A
+1/+5	$\underline{A}\,B + A\,C$	68	B C A
+1/+6/a	$A + B\,C$	75	
+1/+6/b	$\underline{A}\,B + B\,C$	65	B C A
+1/+7	$\underline{A}\,\underline{B}\,C + A\,B\,C$	43	C B A
+2/a	B	72	B - -
+2/b	$\underline{B}\,C$	59	C - B
+2/+3/a	$B + \underline{A}\,C$	62	C B A
+2/+3/b	$A\,B + \underline{B}\,C$	68	C A B
+2/+3/c	$\underline{A}\,C + \underline{B}\,C$	56	C B A
+2/+4	$B + C$	73	C B -
+2/+5/a	$B + A\,C$	75	B A C
+2/+5/b	$A\,C + \underline{B}\,C$	65	C A B
+3/a	$A\,B$	76	
+3/b	$\underline{A}\,C$	59	C B A
+3/c	$A\,\underline{B}\,C$	69	A C B
+3/+3	$A\,B + \underline{A}\,C$	68	C B A
+3/+4	$A\,B + C$	75	C B A

INDEX NUMBER	MINIMAL "AND-OR" BOOLEAN EXPRESSION	REFERENCE CIRCUIT	A B C IN REF CCT. TO READ.
+3/+5/a	A B + A C	77	
+3/+5/b	A $\underline{B}$ C + $\underline{A}$ B C	70	C B A
+3/+5/+6	A B + A C + B C	78	
+3/+6/a	A B + B C	77	B A C
+3/+6/b	$\underline{A}$ C + B C	65	C B A
+4	C	72	C - -
+5/a	$\underline{A}$ B C	69	C B A
+5/b	A C	76	A C -
+5/+6	A C + B C	77	C B A
+6	B C	76	C B -
+6/+3	A B + B C	77	B A C
+7	A B C	79	

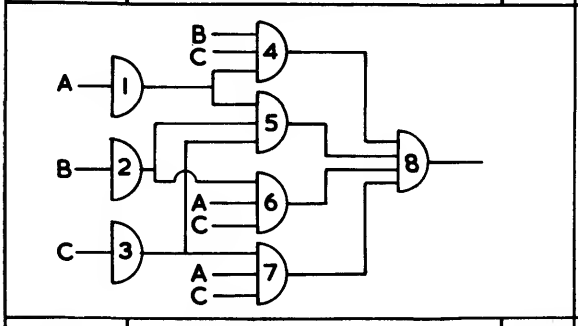
INDEX NUMBER	FUNCTION	REF No.
-7/-1	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C}$	1



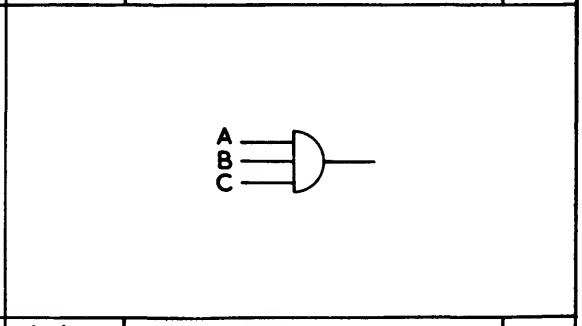
INDEX NUMBER	FUNCTION	REF No.
-7/-1/+3	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + \underline{A}\,\underline{B}\,C$	2



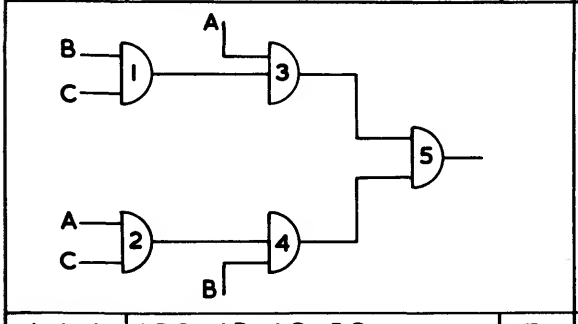
INDEX NUMBER	FUNCTION	REF No.
-7/-1/+3/+5	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,\underline{C} + A\,\underline{B}\,C + \underline{A}\,B\,C$	3



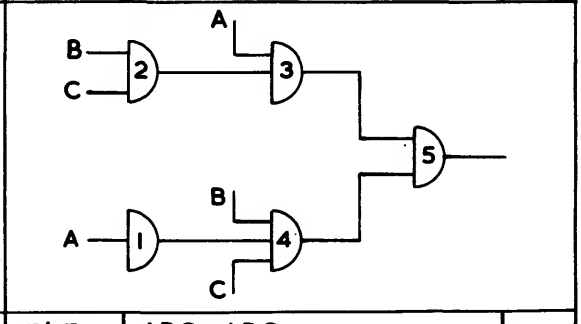
INDEX NUMBER	FUNCTION	REF No.
-7	$\underline{A}\,\underline{B}\,\underline{C}$	4



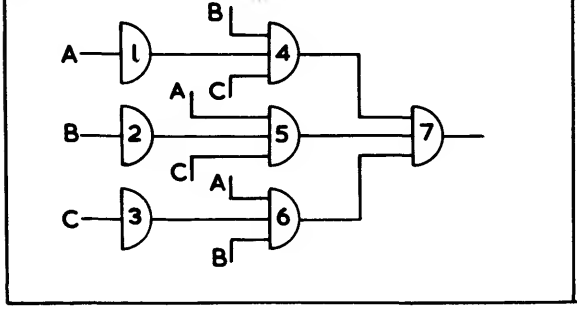
INDEX NUMBER	FUNCTION	REF No.
-7/+3/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B$	5



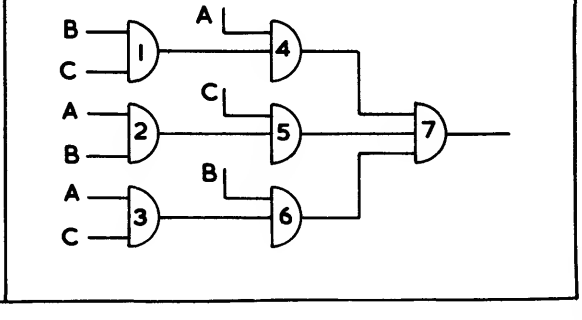
INDEX NUMBER	FUNCTION	REF No.
-7/+3/+5/a	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C$	6



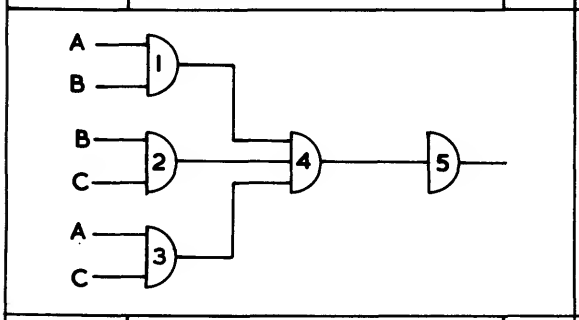
INDEX NUMBER	FUNCTION	REF No.
-7/+3/+5/+6	$\underline{A}\,\underline{B}\,\underline{C} + A\,B + A\,C + B\,C$	7



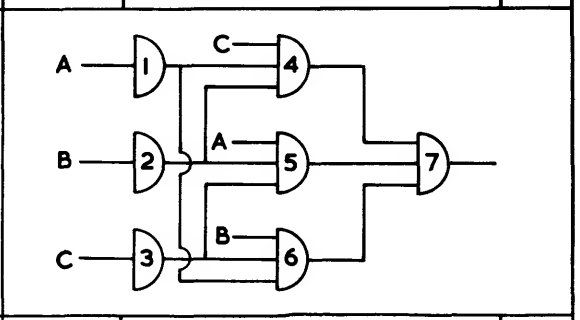
INDEX NUMBER	FUNCTION	REF No.
-7/+7	$\underline{A}\,\underline{B}\,\underline{C} + A\,B\,C$	8



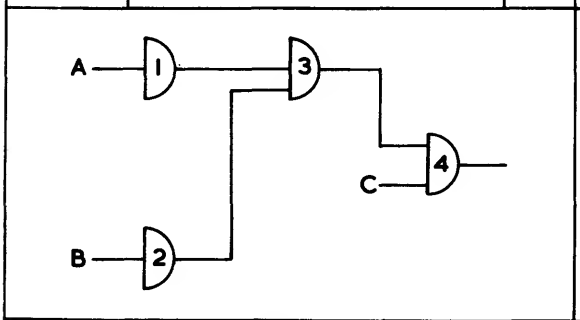
INDEX NUMBER	FUNCTION	REF No.
-6/-5/-3	$\underline{A}\underline{B} + \underline{A}\underline{C} + \underline{B}\underline{C}$	9



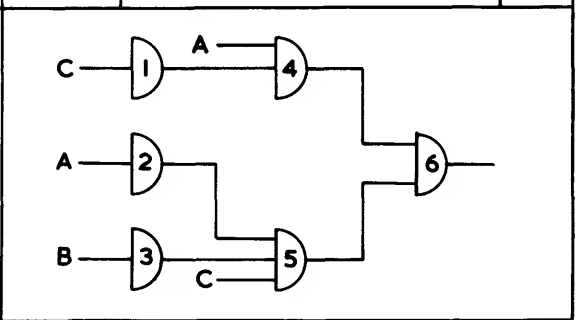
INDEX NUMBER	FUNCTION	REF No.
-6/-5/-3/+7	$\underline{A}\underline{B} + \underline{A}\underline{C} + \underline{B}\underline{C} + ABC$	10



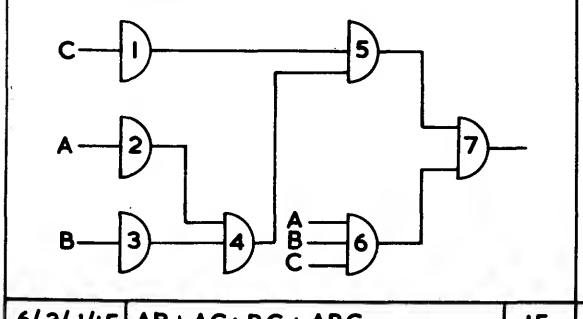
INDEX NUMBER	FUNCTION	REF No.
-6/-5	$\underline{A}\underline{C} + \underline{B}\underline{C}$	11



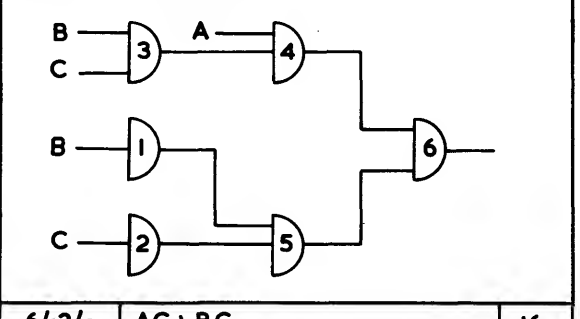
INDEX NUMBER	FUNCTION	REF No.
-6/-5/+5	$AC + \underline{A}\underline{C} + \underline{B}\underline{C}$	12



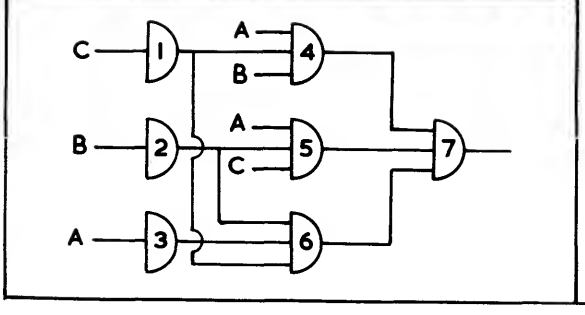
INDEX NUMBER	FUNCTION	REF No.
-6/-5/+7	$\underline{A}\underline{C} + \underline{B}\underline{C} + ABC$	13



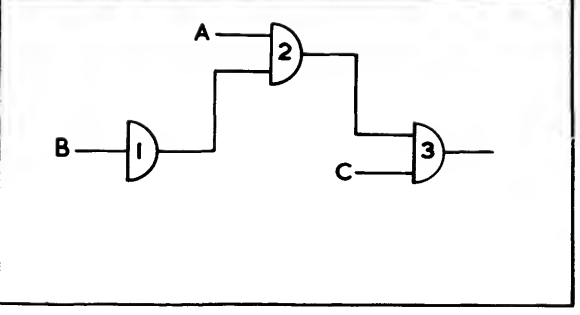
INDEX NUMBER	FUNCTION	REF No.
-6/-3/-1	$\underline{A}\underline{C} + \underline{B}\underline{C} + \underline{A}\underline{B}$	14



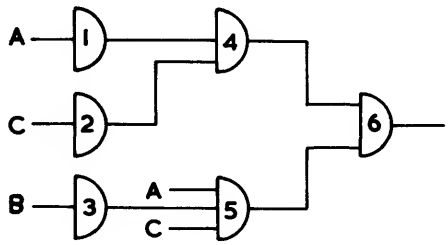
INDEX NUMBER	FUNCTION	REF No.
-6/-3/-1/+5	$\underline{A}\underline{B} + \underline{A}\underline{C} + \underline{B}\underline{C} + \underline{A}BC$	15



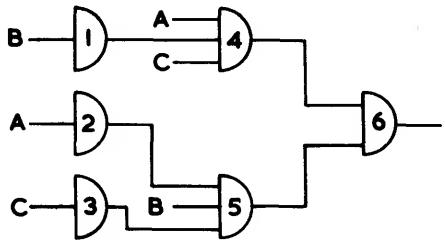
INDEX NUMBER	FUNCTION	REF No.
-6/-3/a	$\underline{A}\underline{C} + \underline{B}\underline{C}$	16



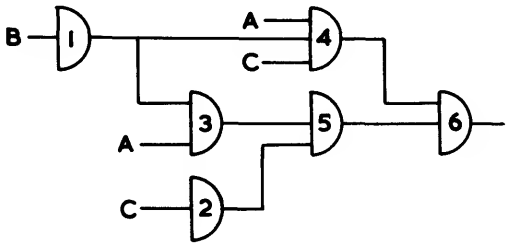
INDEX NUMBER	FUNCTION	REF No.
-6/-3/+3/a	$A\underline{C}+\underline{A}C+\underline{B}\,\underline{C}$	17



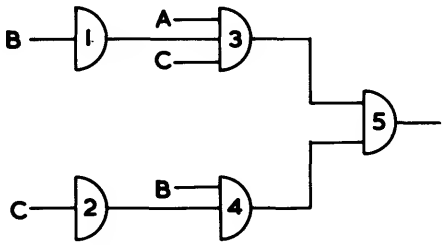
INDEX NUMBER	FUNCTION	REF No.
-6/-3/+3/6	$\underline{A}C+A\underline{C}+BC+\underline{B}\,\underline{C}$	18



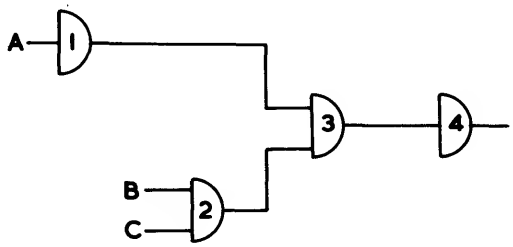
INDEX NUMBER	FUNCTION	REF No.
-6/-3/+5	$A\underline{C}+\underline{A}BC+\underline{B}\,\underline{C}$	19



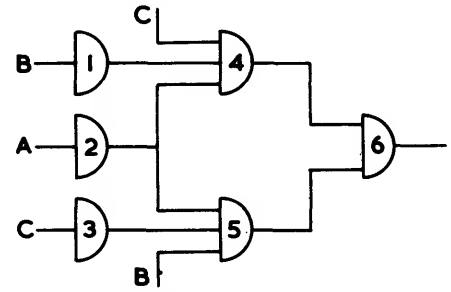
INDEX NUMBER	FUNCTION	REF No.
-6/-3/+6/a	$A\underline{C}+\underline{B}\,\underline{C}+BC$	20



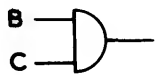
INDEX NUMBER	FUNCTION	REF No.
-6/-1/a	$\underline{A}+\underline{B}\,\underline{C}$	21



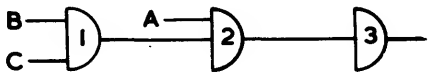
INDEX NUMBER	FUNCTION	REF No.
-6/-1/+6/a	$\underline{A}+\underline{B}\,\underline{C}+BC$	22

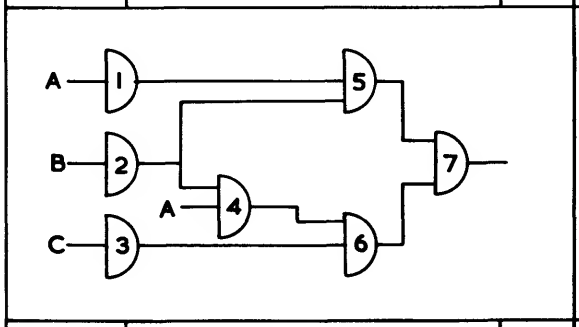
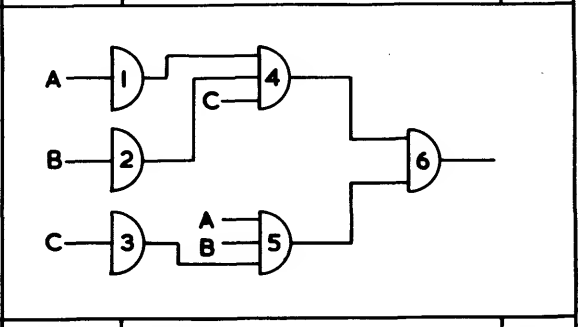
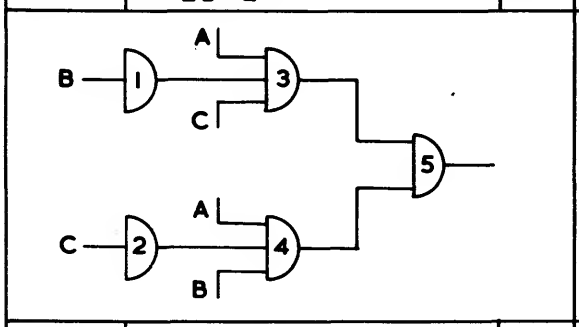
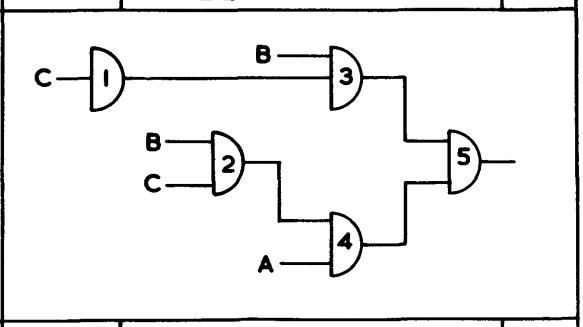
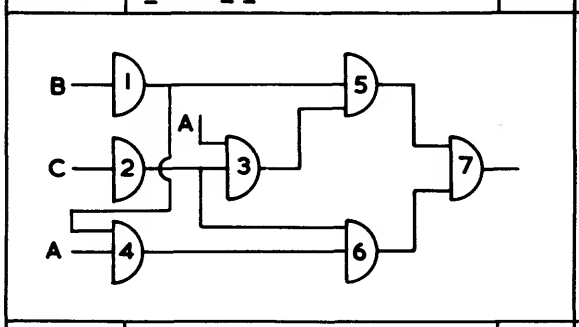
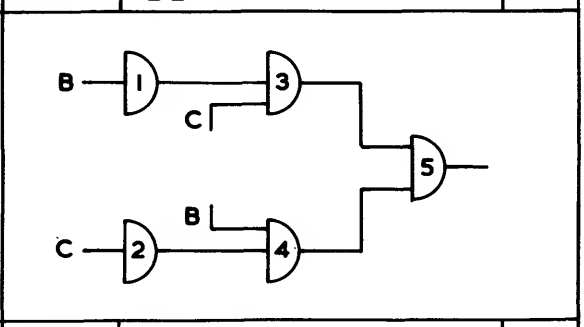
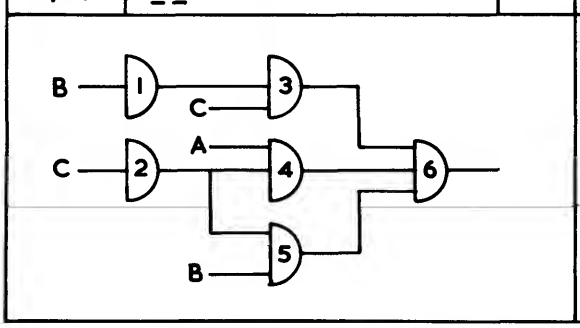
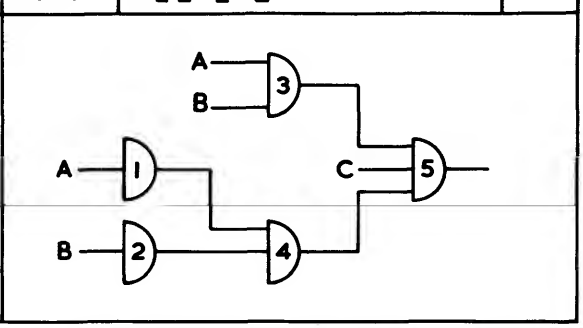


INDEX NUMBER	FUNCTION	REF No.
-6	$\underline{B}\,\underline{C}$	23

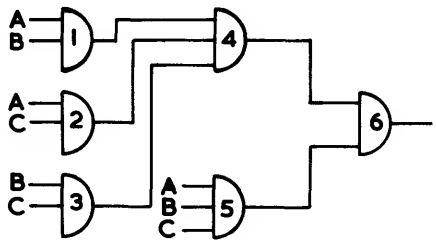


INDEX NUMBER	FUNCTION	REF No.
-6/+1/a	$A+\underline{B}\,\underline{C}$	24

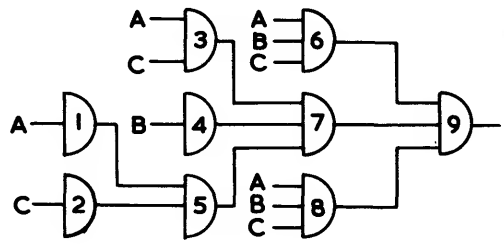


INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-6/+1/b	$\underline{A}B + \underline{B}\underline{C}$	25	-6/+1/+5	$AC + \underline{A}B + \underline{B}\underline{C}$	26
					
-6/+1/+6/b	$A + \underline{B}\underline{C} + \underline{B}C$	27	-6/+3/a	$AB + \underline{B}\underline{C}$	28
					
-6/+5/a	$\underline{A}BC + \underline{B}\underline{C}$	29	-6/+6	$\underline{B}\underline{C} + BC$	30
					
-6/+7	$\underline{B}\underline{C} + ABC$	31	-5/-3/a	$A\underline{B}\underline{C} + \underline{A}B\underline{C}$	32
					

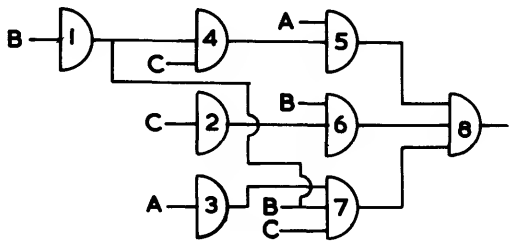
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+1	$A\underline{B}\underline{C} + \underline{A}B\underline{C} + \underline{A}\underline{B}C$	33



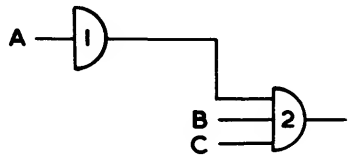
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+1/+7	$\underline{A}\underline{B}\underline{C} + \underline{A}B\underline{C} + \underline{A}\underline{B}C + ABC$	34



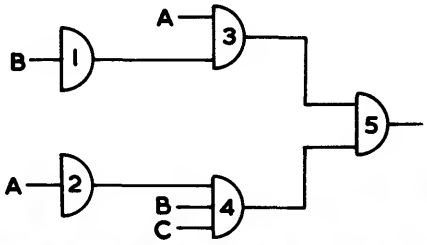
INDEX NUMBER	FUNCTION	REF No.
-5/-3/+7/a	$A\underline{B}\underline{C} + \underline{A}B\underline{C} + ABC$	35



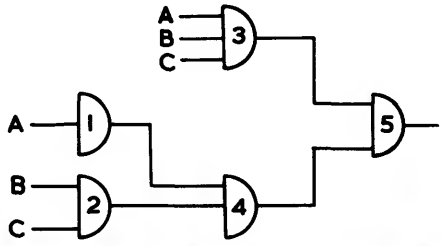
INDEX NUMBER	FUNCTION	REF No.
-5/a	$A\underline{B}\underline{C}$	36



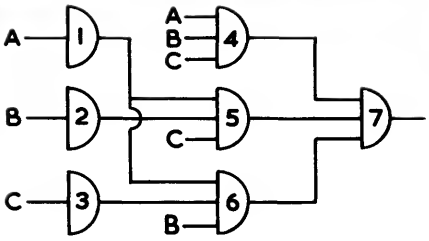
INDEX NUMBER	FUNCTION	REF No.
-5/+1/a	$\underline{A}B + A\underline{B}\underline{C}$	37



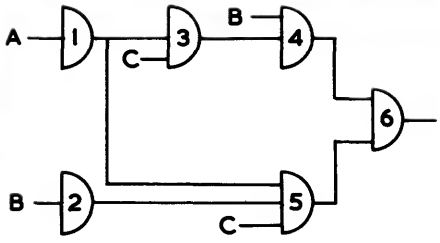
INDEX NUMBER	FUNCTION	REF No.
-5/+1/+3/a	$\underline{A}B + \underline{A}C + A\underline{B}\underline{C}$	38



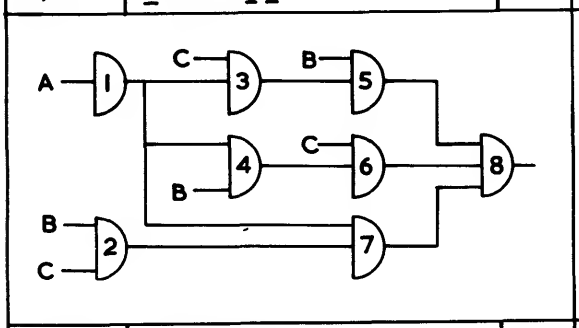
INDEX NUMBER	FUNCTION	REF No.
-5/+1/+3/+6	$\underline{A}C + BC + \underline{A}B + A\underline{B}\underline{C}$	39



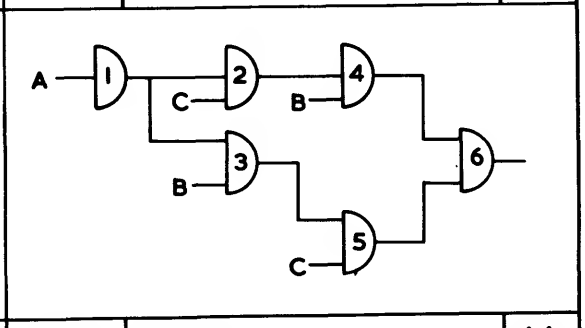
INDEX NUMBER	FUNCTION	REF No.
-5/+1/+6/a	$AB + ABC + BC$	40



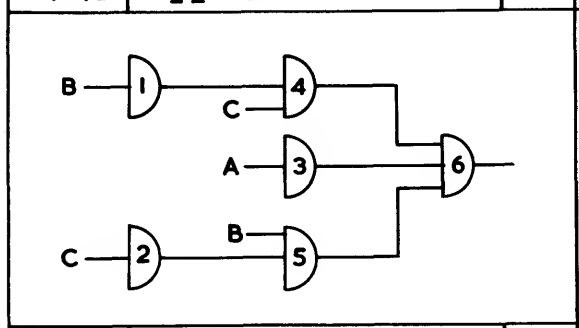
INDEX NUMBER	FUNCTION	REF No.
-5/+5/a	$\underline{A}BC+A\underline{B}\underline{C}$	41



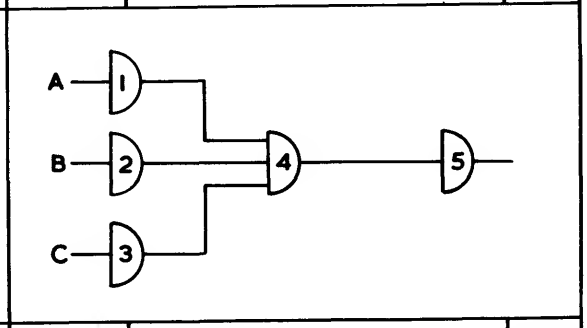
INDEX NUMBER	FUNCTION	REF No.
-5/+6	$A\underline{B}\underline{C}+BC$	42



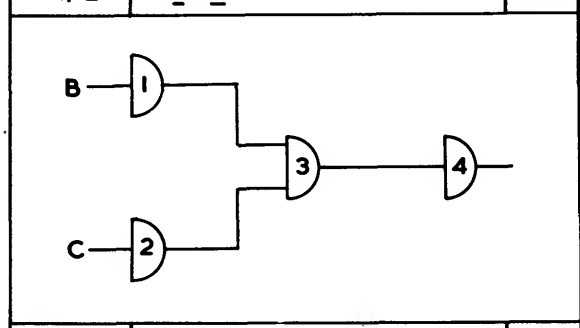
INDEX NUMBER	FUNCTION	REF No.
-5/+7/a	$A\underline{B}\underline{C}+ABC$	43



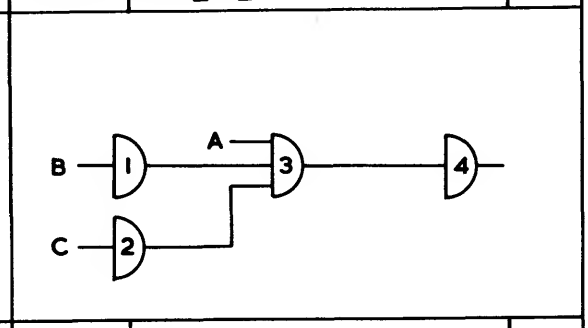
INDEX NUMBER	FUNCTION	REF No.
-4/-2/-1	$\underline{A}+\underline{B}+\underline{C}$	44



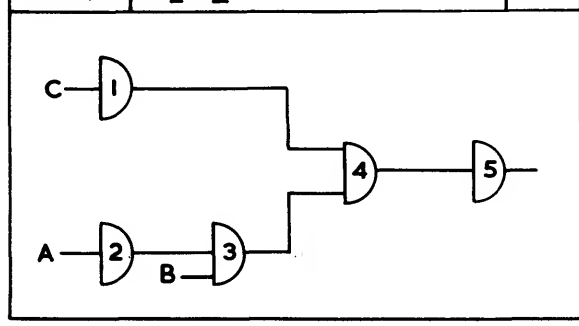
INDEX NUMBER	FUNCTION	REF No.
-4/-2	$\underline{B}+\underline{C}$	45



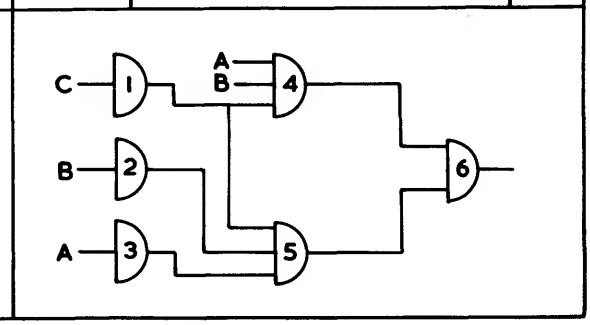
INDEX NUMBER	FUNCTION	REF No.
-4/-2/+1	$A+\underline{B}+\underline{C}$	46

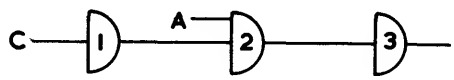
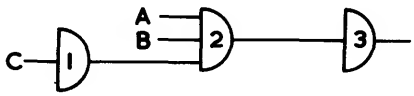
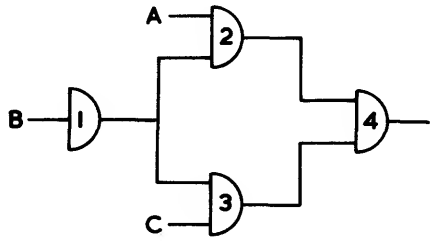
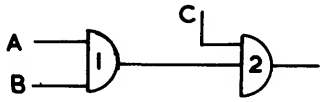
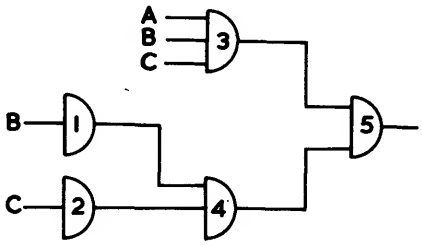
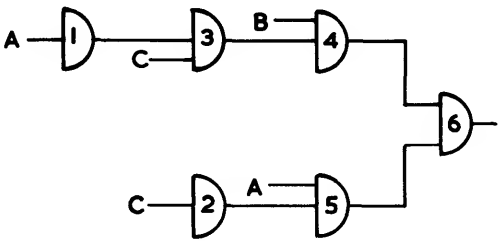
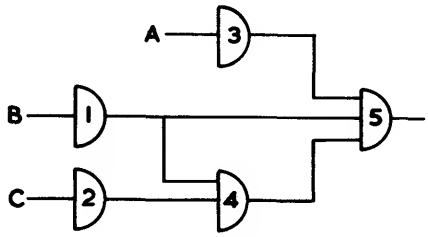


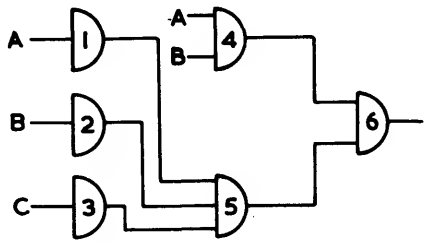
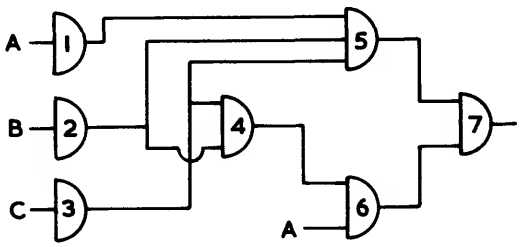
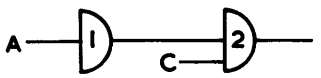
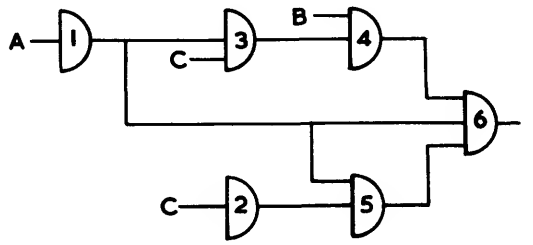
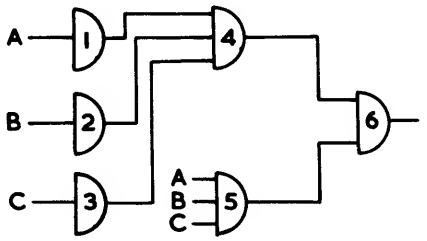
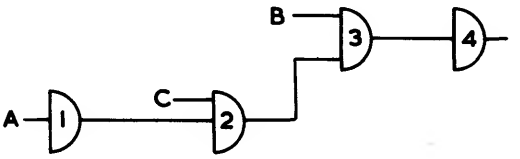
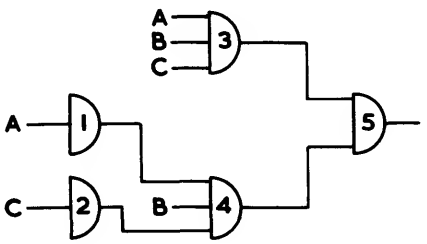
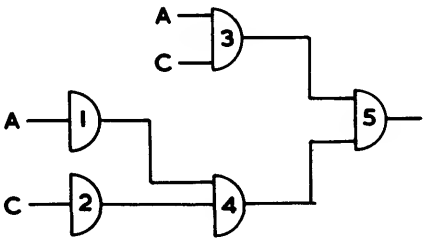
INDEX NUMBER	FUNCTION	REF No.
-4/-1/a	$A\underline{B}+\underline{C}$	47



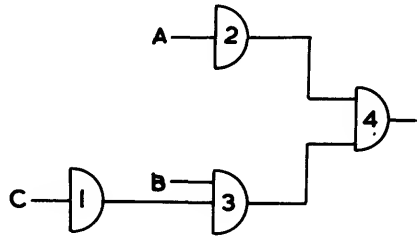
INDEX NUMBER	FUNCTION	REF No.
-4/-1/+1	$A\underline{B}+\underline{A}B+\underline{C}$	48



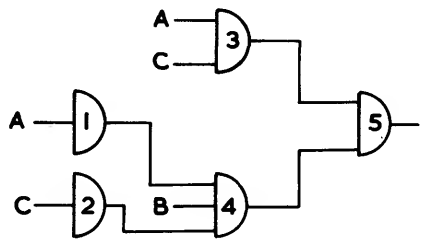
INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-4	$\underline{C}$	49	-4/+1/a	$A+\underline{C}$	50
					
-4/+1/+2	$A+B+\underline{C}$	51	-4/+3	$AB+\underline{C}$	52
					
-3/-2/a	$A\underline{C}+B\underline{C}$	53	-3/-2/+2/a	$A\underline{C}+B\underline{C}+\underline{B}C$	54
					
-3/-2/+3/a	$A\underline{C}+B\underline{C}+AB$	55	-3/-1	$A\underline{B}+A\underline{C}$	56
					

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
-3/-1/+1	$A\underline{B}+\underline{A}B+A\underline{C}$	57	-3/-1/+5/a	$A\underline{C}+A\underline{B}+\underline{A}BC$	58
					
-3/a	$A\underline{C}$	59	-3/+1/a	$A\underline{C}+\underline{A}B$	60
					
-3/+1/+2	$A\underline{C}+\underline{A}B+\underline{B}C$	61	-3/+2/a	$B+A\underline{C}$	62
					
-3/+2/+3/a	$A\underline{C}+\underline{A}C+B$	63	-3/+3/a	$A\underline{C}+\underline{A}C$	64
					

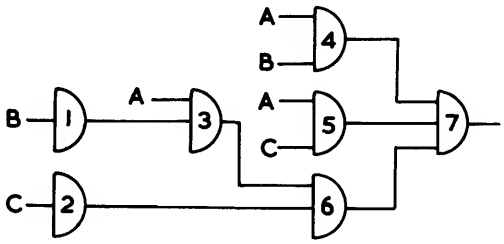
INDEX NUMBER	FUNCTION	REF No.
-3/+3/b	$AB + A\underline{C}$	65



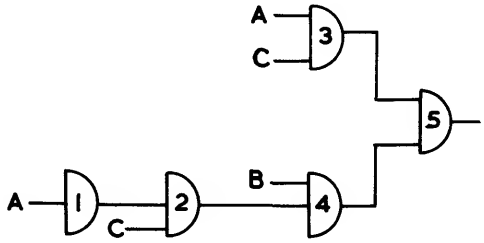
INDEX NUMBER	FUNCTION	REF No.
-3/+3/+3/a	$AB + A\underline{C} + \underline{A}C$	66



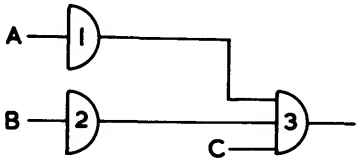
INDEX NUMBER	FUNCTION	REF No.
-3/+5/a	$\underline{A}BC + A\underline{C}$	67



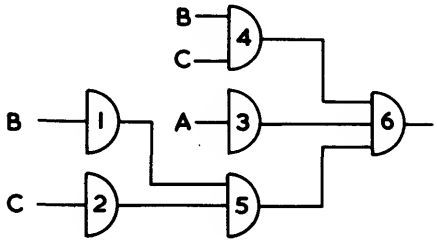
INDEX NUMBER	FUNCTION	REF No.
-3/+6/a	$A\underline{C} + BC$	68



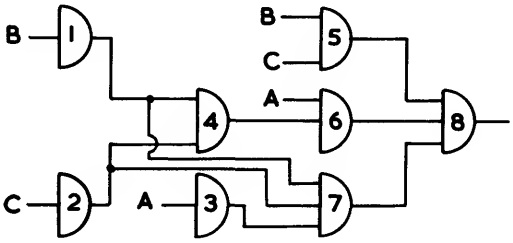
INDEX NUMBER	FUNCTION	REF No.
-1/a	$AB\underline{C}$	69



INDEX NUMBER	FUNCTION	REF No.
-1/+3/a	$AB\underline{C} + A\underline{B}C$	70

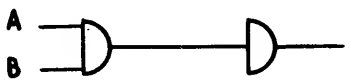
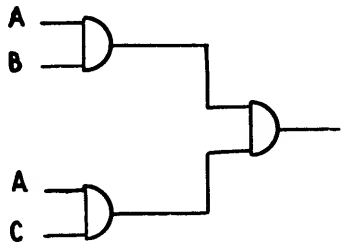
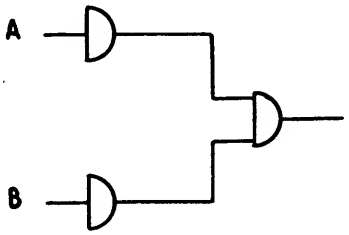
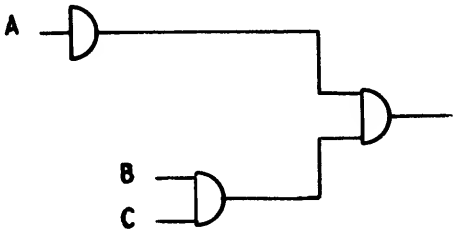
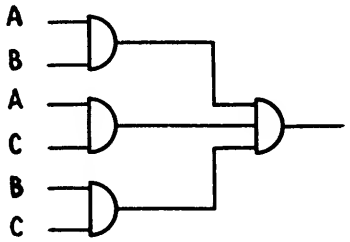
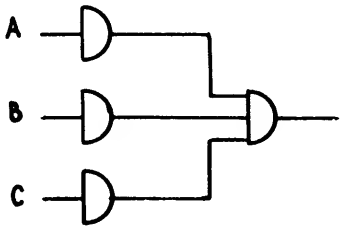


INDEX NUMBER	FUNCTION	REF No.
-1/+3/+5	$AB\underline{C} + A\underline{B}C + \underline{A}BC$	71



INDEX NUMBER	FUNCTION	REF No.
+1/a	A	72

ABSOLUTE MINIMAL COMBINATIONAL CIRCUITS

INDEX NUMBER	FUNCTION	REF No.	INDEX NUMBER	FUNCTION	REF No.
+1/+2/a	A + B	73	+1/+2/+4	A + B + C	74
					
+1/+6/a	A + B C	75	+3/a	A B	76
					
+3/+5/a	A B + A C	77	+3/+5/+6	A B + A C + B C	78
					
+7	A B C	79			
					

CHAPTER 5

SYNTHESIS OF SEQUENTIAL CIRCUITS

SEQUENTIAL CIRCUITS

Race hazards, when they are present in combinational circuits, may produce unwanted pulses during a transient state of the circuit. Such hazards, however, do not cause a permanent malfunction of the combinational circuit, since its steady state output signal is determined solely by the input signals of the circuit.

A race hazard, if present in a sequential circuit, may result in a permanent malfunction of the circuit. Therefore the elimination of race hazards in sequential circuits is essential. A method of achieving this, that is, the design of speed independent circuits, is suggested in the report.

The basic design of sequential circuits based on D. A. Huffman's stability criteria is well established and used extensively.

This basic design is also used in this book with two additional steps. One step is introduced to detect positively the presence of race hazards and their possible effects on the circuit operation. The second step is mainly concerned with means of rendering all races non-critical.

For the sake of completeness, the topic of sequential circuits will be divided into two chapters.

This chapter will deal exclusively with the basic design steps, ignoring the phenomenon of races. In the next chapter, chapter 6, race hazards and their effects in sequential circuits are analysed. Finally, effective means of rendering all races in sequential circuits non-critical are introduced.

Appendix 1 introduces the study of probability of occurance of race hazards and explains how, using algebraic methods the degree of criticallity of each race hazard on circuit operation is determinec

The Design Method Applies to all types of Switching Circuits

Definition

Switching circuits can be divided into two classes, namely combinational and sequential circuits.

A combinational circuit is a circuit which at any moment produces a steady state output signal(s) that is/are complarely determined by the combination of its input signals at that moment. That is, at any instant the steady state output signal(s) of a combinational circuit is/are directly related to the state of the input signals present at the time. This output-input signal relationship can be expressed algebraically. For example, the output signal P, of a two-input AND gate, can be expressed as a function of the two input signals, A and B, as in equation 1.

$$P = A.B \qquad (1)$$

A sequential circuit is a circuit whose output signal(s) is/are no longer determined by the input signals of the moment, but depends also on what the input signals have been in the past.

Assumption

Unless otherwise specified, only one input signal will be assumed to change at a time.

Example

Consider the electromechanical relay circuit 1.

To light lamp L1 in 1(b), relays A and B must be operated - that is, switches X1 and X2 must be closed.

To light lamp L2, relay C as well as relays A and B must also be operated. Now to operate relay C, relay A must be operated before relay B. In other words lamp L2 will be ON if the switches X1 and X2 are closed, but only if switch X1 is closed before switch X2.

By definition, the first circuit, namely relays A and B and circuit 1(b), is a combinational circuit, whereas the second circuit, comprising relays A, B and C and circuit 1(c), is a sequential circuit.

Secondary Signals

A secondary signal is a signal which is generated within the circuit and is specified by the sequence of the input signals. In circuit 1, signal C is a secondary signal.

Design Procedure Based on Huffman's Stability Criteria

The Design procedure which is carried out systematically in the following steps, will be illustrated by working through the design of a two way counter.

Design example 1. A two way counter

Requirement

It is required to design a switching circuit which will accept a train of input pulses, X, at its input terminal but will allow every alternative pulse to get through only - see diagram 1.

Intuitive Design

The required circuit is so simple that the overall system can be designed intuitively. Since it is a cyclic circuit, only one cycle of operation need be considered. Any circuit assuming four states related to the input signal X as shown in diagram 2, is essentially a two way counter. Now every circuit state is specified by a different combination of electric signals. Let the four states S0, S1, S2 and S3 be specified by $\underline{A}\,\underline{B}$, $\underline{A}\,B$, $A\,B$ and $A\,\underline{B}$ respectively, - see diagram 2. The output signal Z is therefore equal to $A\,\underline{B}$.

The next step in the design procedure is to generate these two signals A and B, referred to as secondary signals.

Again, referring to diagram 2, it is seen that secondary signal A must change from 0 to 1 when B = 1 and X = 0 (that is when $B\,\underline{X} = 1$) and must remain at its '1' value when X changes to 1 (that is when $A\,X = 1$). So the algebraic expression of A is

$$A = B\,\underline{X} + A\,X \quad \ldots\ldots\ldots\

The presence of the secondary signals is first assumed. At this stage the circuit can be visualised as a black box, generating the secondary signals A and B as shown in diagram 3.

The assumption of the presence of the secondary signals A and B allows the designer to treat the sequential circuit as a combinational circuit.

If the circuit is to be realised using, say NOR modules, the design procedure described in a previous chapter can be used, as follows:

Step.1. Minimal OR/AND expressions of A and B

$$A = (A + \underline{X})\ (B + X) \qquad (3)$$

and

$$B = (\underline{A} + \underline{X})\ (B + X) \qquad (4)$$

Step.2. Merging of OR terms

No merging is possible.

Step.3. Introduction of substitution signals

There are no common substitution signals.

Step.4. Circuit Realisation

Circuit 2 shows its circuit realisation.

Instead of inverting secondary signal A to generate $\underline{A}$, the outputs of modules 2 and 3 can be used, as shown in circuit 2.

Note: No steps have been taken to investigate the presence and eliminate race hazards from the circuit. The race phenomenon is fully investigated in the following chapter.

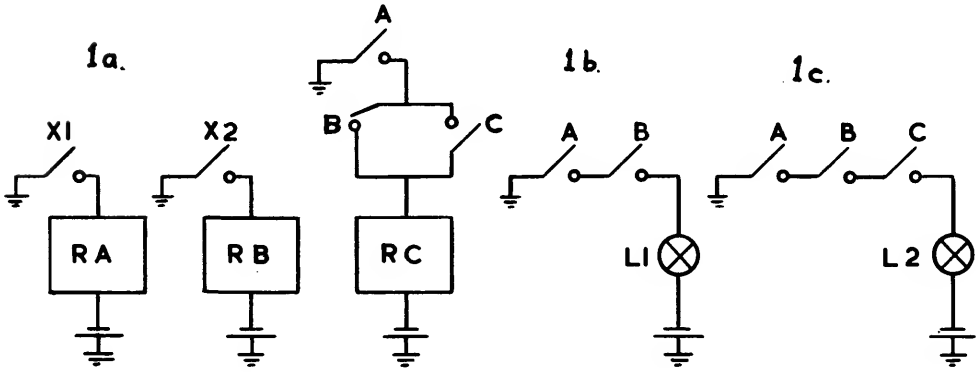
Systematic Design

A step by step design procedure will now be described. The two way counter will be used as an example.

Step.1. The Sequence Diagram

This is basically a system design step. The designer draws in a diagramatic form the exact response of the system to all the possible input signals without any ambiguity. At this stage, no consideration needs to be given to the hardware of the system.

In the diagram each node represents a state. The transition between two states is shown by a line connecting the two nodes that correspond to the two states. The signal that causes the transition is marked either above or below the transition line. For example, let the appearance of the signal X in a system, when it is in state S0, cause it to assume state S1. This transition is shown in diagram 4 by connecting nodes S0 and S1 by a line. The arrow indicates the direction of the transition and the label X shows the signal responsible for the transition. Similarly the line joining S1 to S0 marked Z, shows that the system moves to state S0 from S1 when the signal Z is present.



CIRCUIT 1. ELECTROMECHANICAL RELAY CIRCUITS DEMONSTRATING THE DIFFERENCE BETWEEN COMBINATIONAL AND SEQUENTIAL OPERATIONS

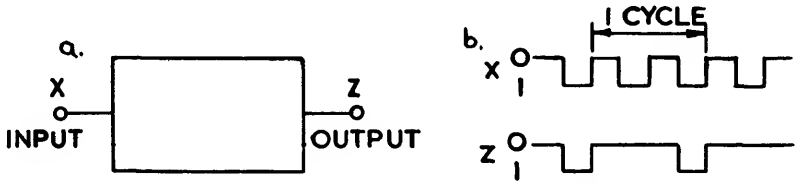


DIAGRAM 1. (a) BLOCK DIAGRAM OF TWO-WAY COUNTER
(b) INPUT AND OUTPUT SIGNALS

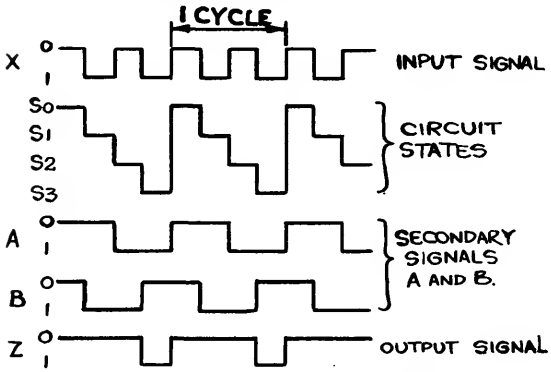


DIAGRAM 2. CIRCUIT STATE DIAGRAM OF THE TWO-WAY COUNTER.

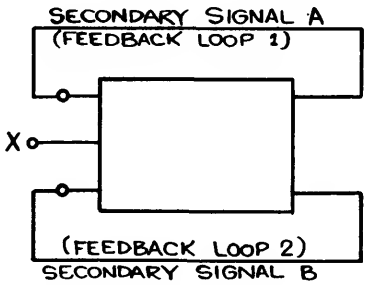
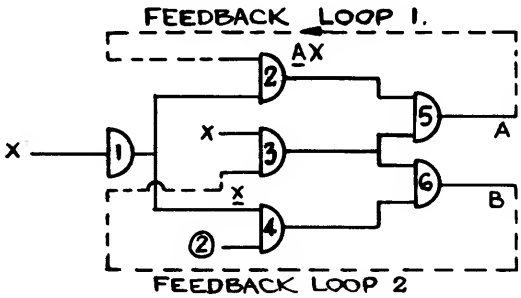


DIAGRAM 3. BLOCK DIAGRAM OF A SEQUENTIAL CIRCUIT (TWO-WAY COUNTER) INDICATING FEEDBACK LOOPS



CIRCUIT 2. MINIMAL TWO-WAY COUNTER USING NOR MODULES
[RACE HAZARDS HAVE NOT BEEN ELIMINATED COMPLETELY]

A loop round a node indicates that the system does not change its state. Referring to diagram 4, the loop round node S0 indicates that the circuit remains in state S0 when the signal Z is present etc.

In this particular diagram both loops are superfluous, since if the system assumes the state, say, S0 with a Z signal and only changes to state S1 with an X signal, it is obviously implied that it stays in state S0 with a signal Z.

It has already been mentioned that the response of the system to all possible conditions must be specified without ambiguity. Diagram 4 is incomplete, because the response of the system to the following combinations of input signals : X $\underline{Z}$, $\underline{X}$ Z, $\underline{X}$ and $\underline{Z}$, has not been specified.

Returning to the two way counter, diagram 5 shows its sequence diagram.

There are two points worthwhile mentioning at this stage. The first point is that one obviously must aim to draw a sequence diagram that uses the minimum number of states, since in general every additional state will require extra circuitry. However, if the sequence diagram includes more states than necessary, the third step will eliminate them. Therefore this point is more useful than essential. The second design example will illustrate this.

Step.2. The Sequence Table

This step, unlike step 1, is not a design step. In this step the information expressed in the sequence diagram is converted to tabular form. This is because it is more convenient to eliminate redundant states and derive the secondary signal equations, when the response of the circuit is expressed in a tabular form.

The mechanics of the conversion are as follows. A table is drawn with as many rows, as there are states in the sequence diagram. The same label is used for a state in the sequence diagram and the corresponding state in the sequence table.

Table 1, having four rows is drawn to correspond to diagram 5. Each row is made to correspond to a circuit state. Let rows 1, 2, 3 and 4 correspond to states S0, S1, S2 and S3. The rows 1, 2, 3 and 4 are next designated the lavels S0, S1, S2 and S3 respectively.

The columns of the table are next drawn to correspond to all possible combinations of input signals. In the case under consideration, there are two possible states of the input signals, namely, X = 0 and X = 1. Therefore the table is divided to two columns. The first column corresponds to when the input signal X = 0 and the second to X = 1.

The entry in each square of the sequence table indicates the destination of the circuit, when it is in a state that corresponds to the row heading and its input signal is specified by the column heading. For example the entry in square 1 of table 1, specifies the destination of the circuit when it is in state S0 and the input signal is X = 0. From the sequence diagram (5) this is shown to be S0 - that is, the circuit does not change state. Therefore S0 is entered in square 1. The entry in square 2 is S1, since if the circuit is in state S0 and the input signal is X = 1 the sequence diagram (5) shows a transition to state S1 etc.

The entry in square 1 is the same as the row heading, in other words the destination and the state of the moment are identical. This shows no change in the circuit state, that is a stable state. The entry in square 2, on the other hand, indicates a destination different to the state of the moment, that is an astable state. To discriminate between stable and astable states, the former are ringed - see table 1.

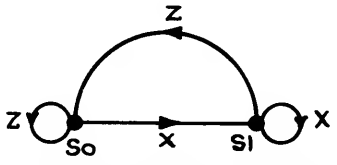


DIAGRAM 4. A TWO-STATE SEQUENCE DIAGRAM

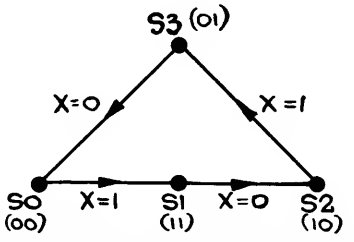


DIAGRAM 5. SEQUENCE DIAGRAM OF A TWO-WAY COUNTER

	X=0	X=1
S0	S0 (1)	S1 (2)
S1	S2 (3)	S1 (4)
S2	S2 (5)	S3 (6)
S3	S0 (7)	S3 (8)

TABLE 1. SEQUENCE TABLE OF A TWO-WAY COUNTER DERIVED DIRECTLY FROM DIAGRAM 5

AB \ X	0	1
00	00 (1)	01 (2)
01	11 (3)	01 (4)
11	11 (5)	10 (6)
10	00 (7)	10 (8)

TABLE 2. EXCITATION TABLE OF A TWO-WAY COUNTER DERIVED DIRECTLY FROM SEQUENCE TABLE 1

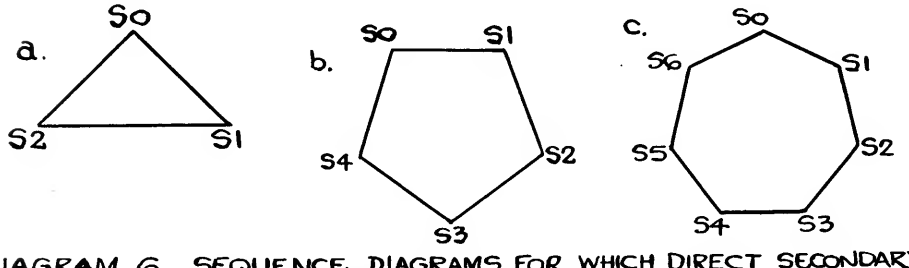


DIAGRAM 6. SEQUENCE DIAGRAMS FOR WHICH DIRECT SECONDARY SIGNAL ALLOCATION CANNOT BE USED

Step.3. Merging of the sequence table

It has been pointed out previously that for the sake of economy the aim is to keep the number of states in a sequence diagram to minimum. An experienced designer will achieve this in step.1. However, it is possible that in step 1, more states than the absolute minimum have been used. This step is used to reduce this number to a minimum, if not already minimum. This is achieved by a process called the merging of states. The rules for merging are:

1. Two rows may be merged if the entries in corresponding columns of each row are alike, or if the entry in one of the rows is blank.

2. When circled and uncircled entries are merged, the resulting entry is circled.

For example the two rows

(S1)	S2	S4	--
S1	--	S4	(S3)

merge to

(S1)	S2	S4	(S3)

The usefulness of this step may not be apparent at this stage, because it cannot be used to reduce table 1. However, it is a useful step to include in the design procedure, although it is not essential.

Step.4. Allocation of Secondary Signals

It has been mentioned before that every system state is specified by a unique combination of secondary signals. Now, n secondary signals specify 2^n states. Therefore to specify the four states S0, S1, S2 and S3 of the sequence table, two secondary signals A and B are needed, since signals A and B can assume the values 00, 01, 11 and 10.

In allocating secondary signals, care must be exercised to ensure that a given transition requires the change of one secondary signal only, otherwise the system may fail to operate according to its sequence diagram. In other words critical races between secondary signals must be eliminated at this stage or rendered non-critical.

If for example the values A B = 00, 11, 10 and 01 are allocated to states S0, S1, S2 and S3 respectively, the following state of affairs may take place.

Consider the circuit to be in stable state S0. Both secondary signals A and B are 00. When the input signal X changes to 1, both the secondary signals begin to change to 1 simultaneously according to the sequence diagram. But both signals cannot assume the same value simultaneously. If secondary signal B changes faster than A, the circuit temporarily moves to state S3, and it stays there - that is instead of moving from state S0 to S1, the circuit may move to state S3, causing a complete malfunction of the system.

The following allocation of secondary signals avoids races between secondary signals.

	AB
S0	00
S1	01
S2	11
S3	10

Table 2 is the same as table 1, where each state has been replaced by the corresponding secondary signals. This table is known as the excitation table.

Note: The allocation of secondary signals may become easier by the pattern modification of the final sequence diagram, using the following procedure.

If the secondary signals specifying one state contain say, an even number of 1's then, any adjacent state must contain an odd number of 1's (zero is considered an even number). This means that it is not possible to allocate secondary signals, without introducing races, to states specified by nodes of a triangular shape or of any closed shape that contains an odd number of sides. Diagram 6 shows such transition diagrams.

Since allocation of secondary signals to such sequence diagrams is impossible, the next logical step is to modify them. The patterns shown in diagram 7 are suggested as a solution to this problem. They differ from the conventional cube shapes in the fact that they are two dimensional and that they are derived directly from the Karnaugh map. They can be extended indefinitely.

The solution of the problem consists in modifying the pattern so that it fits into one of the shapes shown in diagram 6.

Let us consider the pattern shown in diagram 6(a). To fit it into diagram 8(a), we insert a fourth state S3. This means in moving from S2(A B = 11) to S0 (A B = 00), we design the circuit so that secondary signal B changes first to 0 and the change of B to 0 causes the change of A to 0. This is commonly referred to as multiple switching - see diagram 8(a). Similarly diagram 6(b) is modified to diagram 8(b) and 6(c) to 8(c) etc.

At present a more systematic method of allocating secondary signals is being developed.

Note: The sequence table will obviously have to be modified.

Step 5. The Secondary Signal Equations

In the fifth step the equation of the secondary signals are derived directly from the excitation table. For convenience, table 2 is redrawn as two more conventional separate tables 3(a) and 3(b). From them, the required algebraic form of the equation is derived.

For example,

$$A = B\,\underline{X} + A\,X$$
$$B = B\,\overline{\underline{X}} + \underline{A}\,X$$

minimal AND/OR, or

$$A = (B + X)(A + \underline{X})$$
$$B = (B + X)(\underline{A} + \underline{X})$$

minimal OR/AND etc.

Step.6. Circuit Realisation of the Secondary Equations

The presence of the secondary signals in the right hand side of the equation are first assumed. Then the outputs of the circuit are fed to the appropriate input terminals, as shown in circuit 2.

Note: At this state only races between secondary signals have been eliminated in the design. The phenomenon of races in sequential circuits is examined in the next chapter.

Design Example 2. A Forward Shift Register

Requirements

A one bit forward shift register is to be designed, into which the signal at its input terminal is to be transferred into it by the application of a forward shift pulse, F.

The circuit must be capable of being connected to a chain of similar registers to form an n-bit forward shift register.

Let us consider the step by step design of bit 2 in diagram 9.

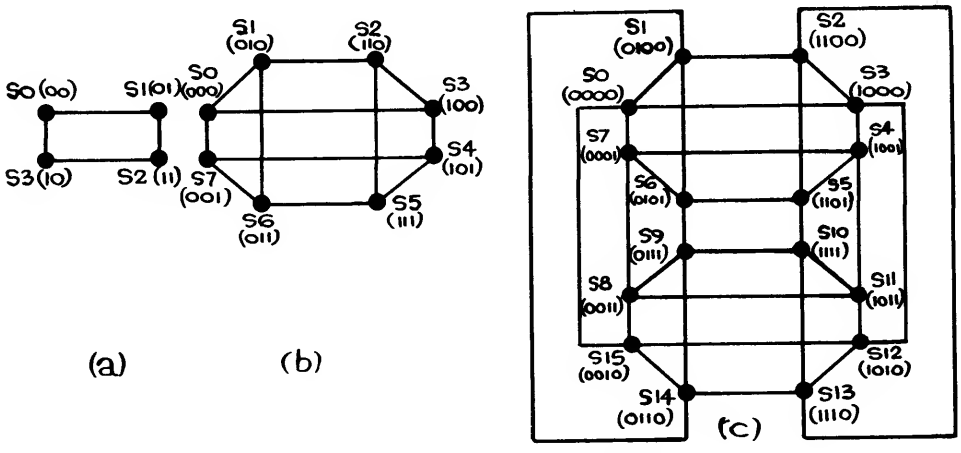
Step.1. The Sequence Diagram

Diagram 10 shows the sequence diagram of bit 2 (diagram 9). The store 'fills' if the input signal, X, is 1 with a forward shift pulse F. It remains in the full state if the signal X is 1 and the shift pulse is applied. The store empties when the input signal X is equal to 0 and the shift pulse is applied.

It is to be noted that the response of the circuit to all four possible input signal conditions, namely, $\underline{F}\,\underline{X}$, $\underline{F}\,X$, $F\,X$, $F\,\underline{X}$, in both circuit states, S0 and S1 has been specified without ambiguity.

A store operating according to diagram 10 will function satisfactorily, if used by itself. When such a store however is used as a unit of n-bit shift register, as in diagram 9, it will malfunction. To explain this, let us assume that the n-bit register is completely empty. If a '1' signal is now applied at the input of the first unit, the contents of the shift register related to the input pulses are shown in table 4(a).

If the output of unit 1 is connected directly to the input of unit 2, the following misoperation will occur. During the presence of the first shift pulse and with a delay equal to the propagation time of the first unit, the output of the first unit appears at the input terminal of the second unit. But according to its sequence diagram, the simultaneous presence of F and X at the input of unit 2 will cause it to fill. Units 3, 4, ...will follow suit, as shown in diagram 11.



B \ A	0	1
0	S0	S1
1	S3	S2

C \ AB	00	01	11	10
0	S0	S1	S2	S3
1	S7	S6	S5	S4

CD \ AB	00	01	11	10
00	S0	S1	S2	S3
01	S7	S6	S5	S4
11	S8	S9	S10	S11
10	S15	S14	S13	S12

DIAGRAM 7. TRANSITION DIAGRAMS SHOWING ALL THE ADJACENCIES FOR (a) 2 SECONDARY SIGNALS, (b) 3 SECONDARY SIGNALS AND (c) 4 SECONDARY SIGNALS. THE TABLES ARE THE CORRESPONDING KARNAUGH MAPS FROM WHICH THEY WERE DERIVED

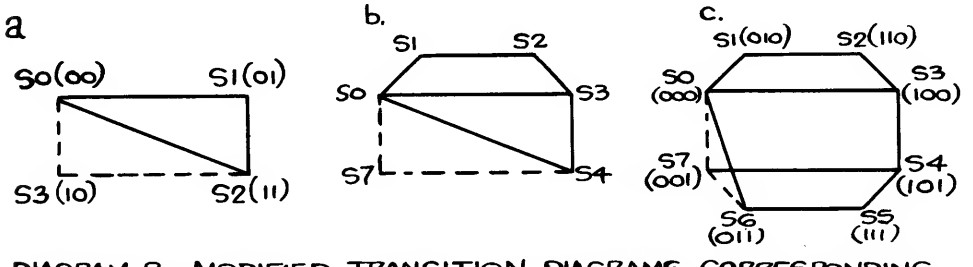


DIAGRAM 8. MODIFIED TRANSITION DIAGRAMS CORRESPONDING TO DIAGRAMS 6 (a), (b) AND (c)

X \ AB	00	01	11	10
0	0	1	1	0
1	0	0	1	1

A

X \ AB	00	01	11	10
0	0	1	1	0
1	1	1	0	0

B

TABLE 3. EXCITATION TABLES OF SECONDARY SIGNALS A & B DERIVED DIRECTLY FROM TABLE 2

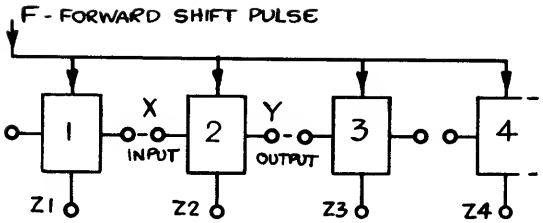


DIAGRAM 9. BLOCK DIAGRAM OF AN n-BIT FORWARD SHIFT REGISTER

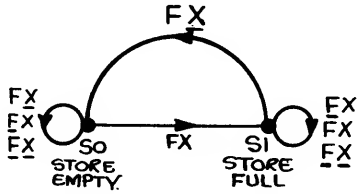


DIAGRAM 10. SEQUENCE DIAGRAM FOR A 1-BIT SHIFT REGISTER

DURING & AFTER SHIFT PULSE	CONTENTS OF SHIFT REGISTER				
	1	2	3	4	n
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
n	1	1	1	1	1
INITIALLY	0	0	0	0	0

TABLE 4a. STATE OF AN n-BIT SHIFT REGISTER (INITIALLY EMPTY) WHEN A "1" IS PRESENT AT ITS INPUT

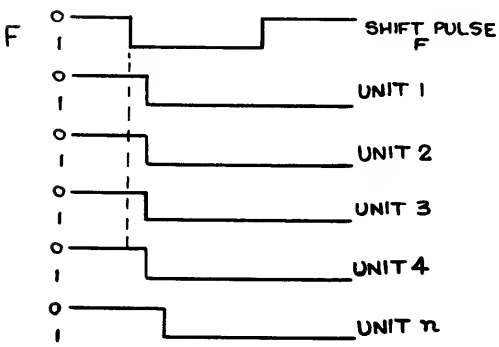


DIAGRAM 11. STATE OF THE 'n'-BIT SHIFT REGISTER, EACH BIT OF WHICH FUNCTIONS AS PER DIAG. 10

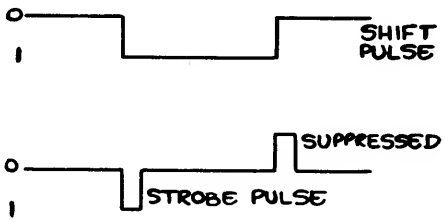


DIAGRAM 12. THE GENERATION OF A STROBE PULSE

This would have been avoided if the duration of the shift pulse is less than the propagation time of each unit. This can be achieves in practice by differentiating the shift pulse, which gives two 'narrow' pulses as shown in diagram 12. One of these pulses is suppressed and the other used.

This system however has been rejected by the authors because it assumes that the pulse width is less than the propagation time of the unit, which is opposite to the fundamental assumption that no part of a circuit can be assumed faster or slower than another part.

An alternative approach is to prevent the output of the unit to be fed to the input to the next unit, until the shift pulse has disappeared. A sequence diagram meeting this demand is shown in diagram 13. Table 4(b) shows the relationship between the 2 states of the store and the corresponding output fed to the next stage.

Step.2. Sequence table

The sequence table derived from diagram 13 is shown in table 5.

Entries 5, 8, 14 and 15 are referred to as 'blank' entries, and the designer may use them as he wishes, to optimise his algebraic equations specifying the secondary signals. This is because the circuit never enters any of these squares.

For example, once the circuit has entered square 7, it can only go to square 6.

Step.3. Merging of the sequence table

No merging is possible.

Step.4. Allocation of Secondary Signals

Let the values of the secondary signals A and B, corresponding to circuit states S0, S1, S2 and S3 be 00, 01, 11 and 10 respectively. Table 6 shows the resulting excitation table.

Step.5. The secondary signal equations

For convenience table 6 is redrawn as two separate tables, 7(a) and 7(b). From them the required form of the equation is derived. For example,

$$A = F\,A + \underline{F}\,B$$
$$B = F\,X + \underline{F}\,B$$

minimal AND/OR, or

$$A = (B + F)(A + \underline{F})$$
$$B = (B + F)(X + \underline{F})$$

Step.6. Circuit Realisation of the Secondary Equations

A NOR circuit realisation of the equation is shown in circuit 3.

Note:
This circuit may not function satisfactorily in practice because only races between secondary signals have been eliminated in the design. The phenomenon of races in sequential circuits is examined in the next chapter.

DESIGN EXAMPLE 3

A circuit is to be designed that gives an output when both its d.c. input signals X1 and X2 are present, but only if signal X1 has arrived before X2.

Note: Circuit 1 shows the electromechanical relay circuit realisations of the solution to this problem.

Step.1. The Sequence diagram

Let us assume that the circuit has an initial state S0, corresponding to the 'no signal received yet' condition. Because there are two input signals, there exist four possible input signal conditions, namely, $\underline{X1}$, $\underline{X2}$, $\underline{X1}$, X2, X1, X2 and X1, $\underline{X2}$. At each circuit state the response to all possible input signal conditions must be specified without ambiguity.

Circuit State S0

Input Signal Condition $\underline{X1}$ $\underline{X2}$.

Circuit remains in state S0, since there has been no change in the input condition - see diagram 14.

Input Signal Condition $\underline{X1}$ X2.

The Circuit does not respond to this input condition, since it does not constitute part of the input signal sequence ($\underline{X1}$ $\underline{X2}$ to X1 $\underline{X2}$ - to X1 X2) we are looking for.

Input Signal Condition X1 $\underline{X2}$.

This is the first stage of the sequence we are looking for, therefore we record this by directing the circuit to assume a different state namely S1.

Input Signal Condition X1 X2.

(The circuit is in state S0). Since it is assumed that only one input signal changes at a time, this input signal condition can only have been assumed by a change of X2 from 0 to 1, that is only if the input signal sequence is 01 to 11. This input signal condition, therefore, if it appears when the circuit is in the S0 state, is ignored.

We can now consider the response of the circuit when it is in state S1, since its response in state S0 has been specified for all possible (four) input signal conditions.

Circuit State S1

Input Signal Condition $\underline{X1}$ $\underline{X2}$.

The circuit returns to its initial state, S0, since its presence in state S1 implies that signal X1 was the last to change to 0.

Input Signal Condition X1 $\underline{X2}$.

Circuit remains in state S1, since this condition is part of the sequence we want to record.

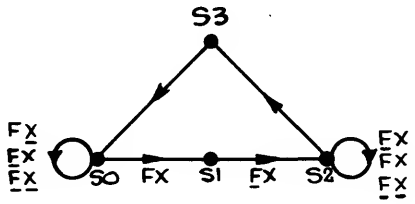


DIAGRAM 13. MODIFIED SEQUENCE DIAGRAM FOR A 1-BIT SHIFT REGISTER

CIRCUIT STATES	STATE OF THE STORE	OUTPUT FED TO NEXT STAGE
S0	EMPTY	0
S1	FULL	0
S2	FULL	1
S3	EMPTY	1

TABLE 4b. TABLE SHOWING THE RELATIONSHIP BETWEEN THE STATES & THE OUTPUT SIGNAL OF A ONE-BIT SHIFT REGISTER

	FX 00	01	11	10	AB
S0	S0 1	S0 2	S1 3	S0 4	00
S1	5	S2 6	S1 7	8	01
S2	S2 9	S2 10	S2 11	S3 12	11
S3	S0 13	14	15	S3 16	10

TABLE 5. SEQUENCE TABLE DERIVED DIRECTLY FROM DIAG. 13

AB \ FX	00	01	11	10
00	00	00	01	00
01		11	01	
11	11	11	11	10
10	00			10

TABLE 6. EXCITATION TABLE DERIVED FROM TABLE 5

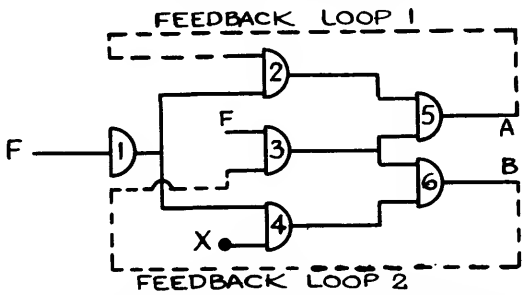
AB \ FX	00	01	11	10
00	0	0	0	0
01		1	0	
11	1	1	1	1
10	0			1

A

AB \ FX	00	01	11	10
00	0	0	1	0
01		1	1	
11	1	1	1	0
10	0			0

B

TABLE 7. EXCITATION TABLES OF SECONDARY SIGNALS A & B DERIVED DIRECTLY FROM TABLE 6



CIRCUIT 3. MINIMAL ONE-BIT FORWARD SHIFT REGISTER USING NOR MODULES [RACE HAZARDS HAVE NOT BEEN ELIMINATED COMPLETELY]

Input Signal Condition X1 X2.

The existance of the input signal condition X1 X2, implies that input signal X2 has changed last. Therefore this represents the last step in the sequence of the input signals we are looking for. This last step can therefore be expressed algebraically in the form

$$Z = S0 \,.\, X1 \,.\, X2 \qquad (6)$$

Input Signal Condition $\underline{X1}$ X2.

This input signal condition can only have been assumed as a result of a change of the signal X1 from the logical level '1' to '0'. This state completely destroys the sequence of input signals we are looking for, therefore, the circuit is directed to state S0.

Step.1. is now completed.

Step.2. The Sequence Table

This, unlike step 1. is a routine step. Table 8 shows the sequence table directly derived from diagram 14.

Step.3. Merging of the Sequence Table

No merging is possible.

Step.4. Allocation of the secondary Signals

Let secondary signal values A = 0 and A = 1 correspond to circuit states S0 and S1, respectively, resulting in excitation table 9.

Step.5. The Secondary Signal Equations

From table 9,

$$A = X1\,(\underline{X2} + A) \qquad (7)$$

Step.6. AND/OR Circuit Realisation of the Secondary Equations

Circuit 4 shows its realisation using NOR (NAND) modules.

Note: The race-hazards that may be present in this circuit have not been investigated. See next chapter for the investigation of the race-hazard phenomenon.

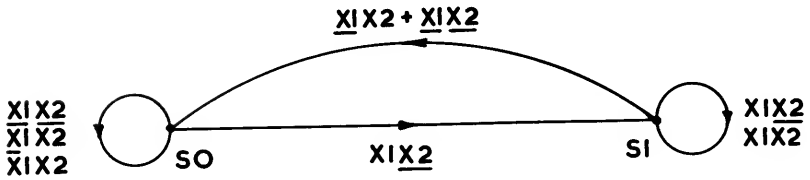


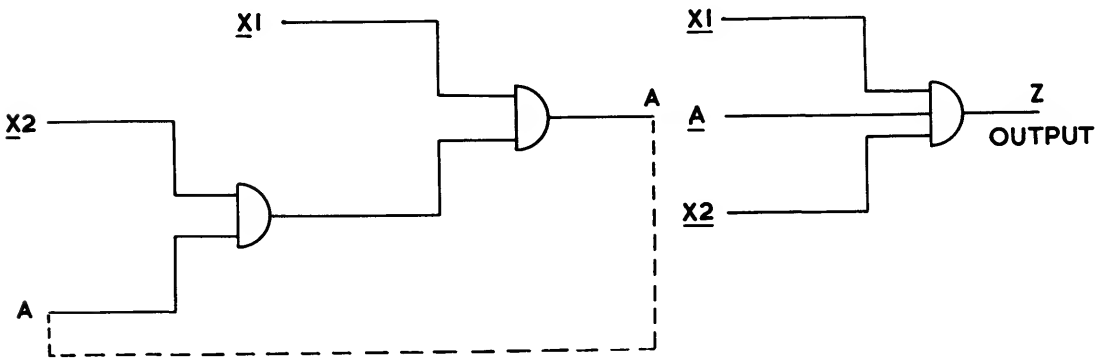
DIAGRAM 14. SEQUENCE DIAGRAM OF PROBLEM 3

	X1X2				A
	00	01	11	10	
SO	SO	SO	SO	S1	0
S1	SO	SO	S1	S1	1

TABLE 8. SEQUENCE TABLE OF DESIGN PROBLEM 3

A	X1X2			
	00	01	11	10
0	0	0	0	1
1	0	0	1	1

TABLE 9. EXCITATION TABLE OF DESIGN PROBLEM 3



CIRCUIT 4. CIRCUIT REALIZATION OF DESIGN PROBLEM 3

DESIGN EXAMPLE 4

A circuit is to be designed that has two input and one output terminals which produces an output pulse Z coincident with any X2 input pulse which follows exactly two consecutive X1 input pulses. Only one input pulse may be present at any one time.

Step.1. The Sequence Diagram

See diagram 15.

Step.2. The Sequence Table

See table 10.

Step.3. Merging of the Sequence Table

No merging is possible.

Step.4. Allocation of the Secondary Signals

Before allocating secondary signals, the sequence diagram is examined in case an odd number of direct circuit transitions form a closed loop. Such a loop must be eliminated, since in such cases, allocation of secondary signals avoiding races is impossible - see diagram 8. Diagram 15 shows that the S0 - S1, S1 - S2 and S2 - S0 circuit transitions form a triangle. The direct circuit transition S2 - S0 is therefore broken into two, namely S2 - S1 and S1 - S0. This is possible because square 6 of table 10(a) is a blank entry.

Similarly circuit transition S0 - S7 - S0 contains seven direct transitions. From table 10(a) it can be seen that in square 30 entry S0 can be replaced by entry S1 directly, since the entry of square 6 is now S0 - see table 10(b).

The diagram can now be readily 'fitted' into diagram 16, which allows immediately the secondary signal allocation that is shown in table 10(b).

Step.5. The Secondary Signal Equations

From Table 11, the minimal AND/OR equations for the three secondary signals are:

$$A = A\,\underline{X2} + B\,\underline{C}\,\underline{X1}\,\underline{X2}$$

$$B = B\,\underline{C}\,\underline{X2} + \underline{A}\,C\,\underline{X2} + A\,B\,\underline{C} + \underline{A}\,B\,C + B\,X1 + \underline{A}\,\underline{C}\,X1$$

$$C = A\,B\,C + A\,C\,\underline{X1} + \underline{A}\,\underline{B}\,C + C\,\underline{X1}\,\underline{X2} + A\,B\,X1$$

Step.6. Circuit Realisation of the Secondary Equations

The AND/OR circuit realisation of the secondary equations is shown in circuit 5(a).

The equation of the required output signal $Z = S6$
$= \underline{A}\,\underline{B}\,C$

see circuit 5(b).

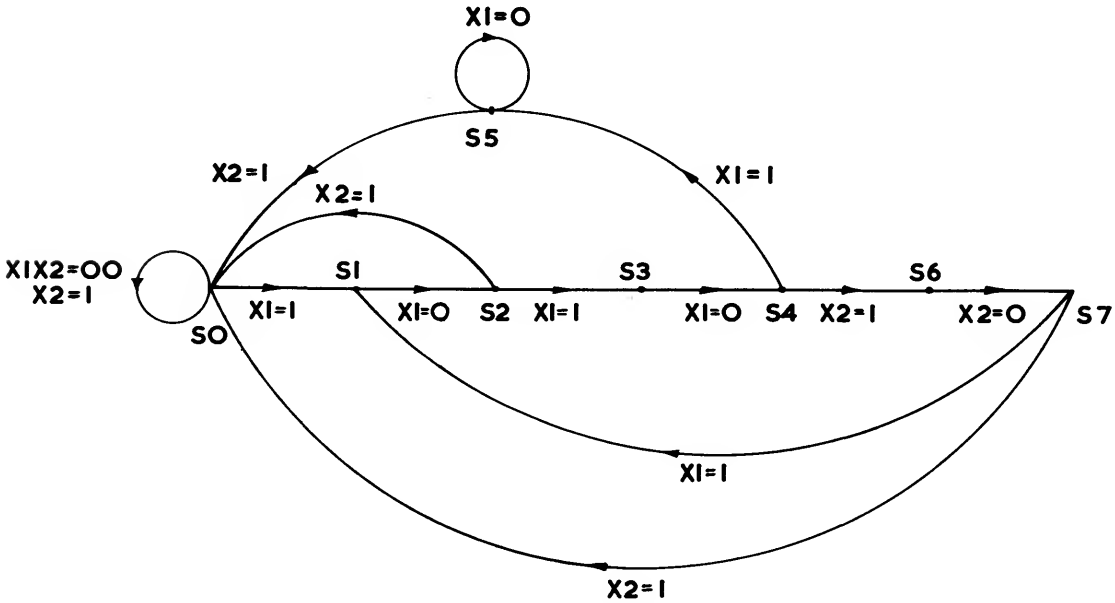


DIAGRAM 15. SEQUENCE DIAGRAM OF DESIGN PROBLEM 4

	X1X2 00	01	11	10
S0	(S0) 1	(S0) 2	3	S1 4
S1	S2 5	6	7	(S1) 8
S2	(S2) 9	S0 10	11	S3 12
S3	S4 13	14	15	(S3) 16
S4	(S4) 17	S6 18	19	S5 20
S5	(S5) 21	S0 22	23	(S5) 24
S6	S7 25	(S6) 26	27	28
S7	(S7) 29	S0 30	31	S1 32

(a)

	X1X2 00	01	11	10	ABC
S0	(S0)	(S0)		S1	000
S1	S2	S0		(S1)	010
S2	(S2)	S1		S3	110
S3	S4			(S3)	111
S4	(S4)	S6		S5	101
S5	(S5)	S0		(S5)	100
S6	S7	(S6)			001
S7	(S7)	S1		S1	011

(b)

TABLE 10. (a) SEQUENCE TABLE OF DESIGN PROBLEM 4

(b) MODIFIED SEQUENCE TABLE OF DESIGN PROBLEM 4

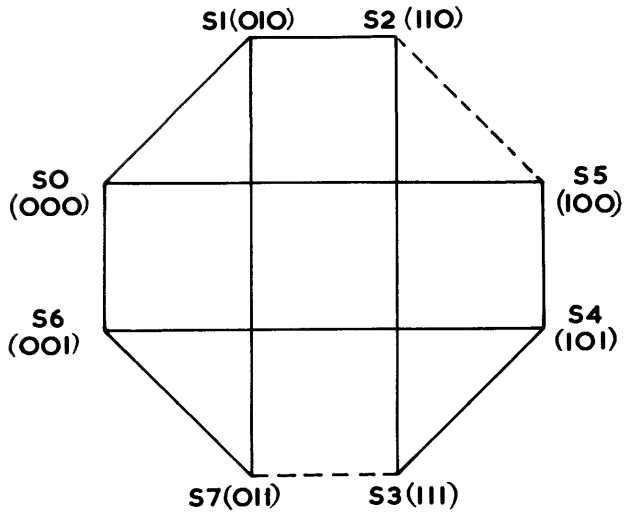


DIAGRAM 16. TRANSITION DIAGRAM OF DESIGN PROBLEM 4

ABC \ X1X2	00	01	11	10
000	000	000		010
010	110	000		010
110	110	010		111
111	101			111
101	101	001		100
100	100	000		100
001	011	001		
011	011	010		010

ABC \ X1X2	00	01	11	10
000	0	0		0
010	1	0		0
110	1	0		1
111	1			1
101	1	0		1
100	1	0		1
001	0	0		
011	0	0		0

A

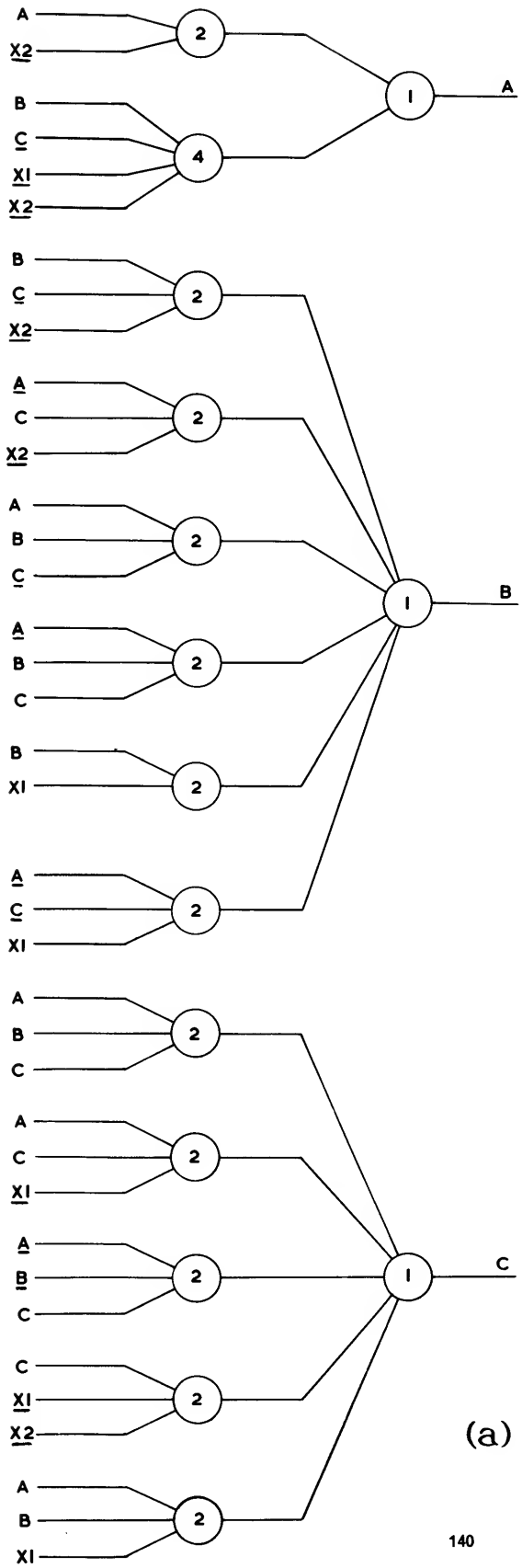
ABC \ X1X2	00	01	11	10
000	0	0		1
010	1	0		1
110	1	1		1
111	0			1
101	0	0		0
100	0	0		0
001	1	0		
011	1	1		1

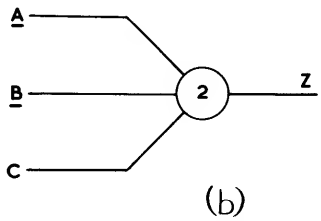
B

ABC \ X1X2	00	01	11	10
000	0	0		0
010	0	0		0
110	0	0		1
111	1			1
101	1	1		0
100	0	0		0
001	1	1		
011	1	0		0

C

TABLE II. EXCITATION TABLES OF DESIGN PROBLEM 4





CIRCUIT 5. AND/OR CIRCUIT REALIZATION OF PROBLEM 4

Notes:

1. State S7 in the sequence diagram may be omitted. The circuit may be directed to state S0 with X2 = 0. It is suggested that the circuit is redesigned with the above modification included.

2. The race-hazards that may be present in this circuit have not been investigated. See next chapter for the investigation of the race-hazard phenomenon.

DESIGN EXAMPLE 5

A circuit is to be synthesised with three input and one output terminals which produces an output pulse, Z, coincident with input pulse X3, but only if the input pulse signals appear in the sequence X1, X2, X3. Only one input pulse can be present at a time.

Step.1. The Sequence Diagram

See diagram 17.

Circuit State S0

Corresponds to the 'no signal of the required sequence received yet' condition.

Circuit State S1

Corresponds to the first pulse, X1, in the required sequence being received.

Circuit State S2

Corresponds to the first pulse in the required sequence having been received.

Circuit State S3

Corresponds to the second pulse, X2, in the required sequence being received.

Circuit State S4

Corresponds to the second pulse in the required sequence having been received.

Circuit State S5

Corresponds to the third pulse, X3, in the required sequence being received.

Step.2. The Sequence Table

See Table 12(a).

Step.3. Merging of the Sequence Table

No merging possible.

Step.4. Allocation of the Secondary Signals

Before allocating secondary signals, the sequence diagram is examined in case an odd number of direct circuit transitions form a closed loop. Such closed loops in the sequence diagram

must be eliminated, since in such cases the allocation of secondary signals avoiding races is impossible - see diagram 8. Diagram 17 shows that

(a) the S0 - S1, S1 - S2 and S2 - S0 circuit transitions form a closed loop (triangle). From Table 12(a) we see that instead of moving directly from state S2 to state S0, that is, from square 12 to square 4 (of diagram 12(a)), we can go to square 8 from square 12 and from square 8 to square 4, as shown in table 12(b). This technique is referred to as multiple switching.

(b) To modify the S2 - S3 - S4 - S2 transition loop, we can direct the circuit to state S1.

(c) Similarly the S4 - S0 with X2 = 1 direct circuit transition (square 19 to square 3 of table 12 (a)). is broken into two transitions, namely S4 - S1 - S0, as shown in Table 12(b).

The sequence diagram can now be readily 'fitted' into the standard form shown in diagram 18, which allows immediately the secondary signal allocation that is shown in Table 12(b).

Step.5. The Secondary Signal Equations

From table 13, the following set of equations is derived.

$$\underline{A} = X3 + C\,\underline{X2} + \underline{A}\,(\underline{B} + X1 + X2)$$

$$\underline{B} = \underline{A}\,\underline{B}\,\underline{X1} + \underline{A}\,\underline{C}\,X2 + \underline{A}\,X3$$

$$\underline{C} = \underline{A}\,\underline{B}\,\underline{X3} + \underline{C}\,\underline{X2} + X1 + \underline{A}\,X2.$$

Step.6. NOR/NAND Circuit Realisation of the Secondary Signals

The optimisation technique described in chapter 2, is next used to optimise their form.

Inverting

$$A = \underline{X3}\,(\underline{C} + X2)\,(A + B\,\underline{X1}\,\underline{X2})$$

$$B = (A + B + X1)\,(A + C + \underline{X2})\,(A + \underline{X3})$$

$$C = (A + B + X3)\,(C + X2)\,\underline{X1}\,(A + \underline{X2})$$

Merging

Equations do not merge.

Substitution Signals

$$A = \underline{X3}\,(\underline{C}\,\underline{X2} + X2)\,(A + (A + B + X1)\,\underline{X1}\,\underline{X2})$$

$$B = (A + B + X1)\,(A + C + C\,\underline{X2})\,(A + \underline{X3})$$

$$C = (A + B + X3)\,(C + X2)\,\underline{X1}\,(A + C + C\,\underline{X2})$$

(see circuit 6).

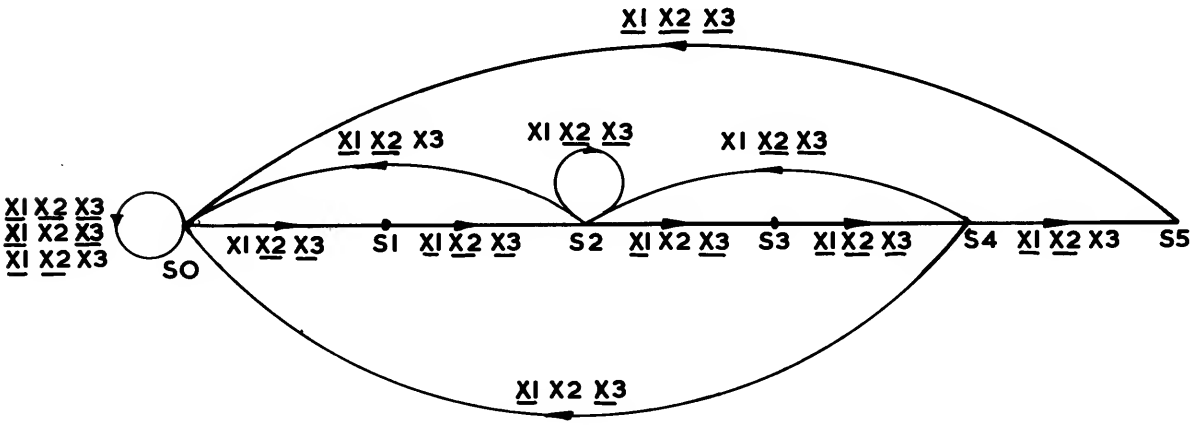


DIAGRAM 17. SEQUENCE DIAGRAM OF DESIGN PROBLEM 5

X1X2X3	000	100	010	001
SO	(SO) 1	S1 2	(SO) 3	(SO) 4
S1	S2 5	(S1) 6	7	8
S2	(S2) 9	(S2) 10	S3 11	SO 12
S3	S4 13	14	(S3) 15	16
S4	(S4) 17	S2 18	SO 19	S5 20
S5	SO 21	22	23	(S5) 24

(a)

X1 X2 X3	000	100	010	001	ABC
SO	(SO)	S1	(SO)	(SO)	000
S1	S2	(S1)	SO	SO	010
S2	(S2)	(S2)	S3	S1	110
S3	S4		(S3)		111
S4	(S4)	S1	S1	S5	011
S5	SO			(S5)	001

(b)

TABLE 12. (a) SEQUENCE TABLE OF DESIGN PROBLEM 5

(b) MODIFIED SEQUENCE TABLE OF DESIGN PROBLEM 5

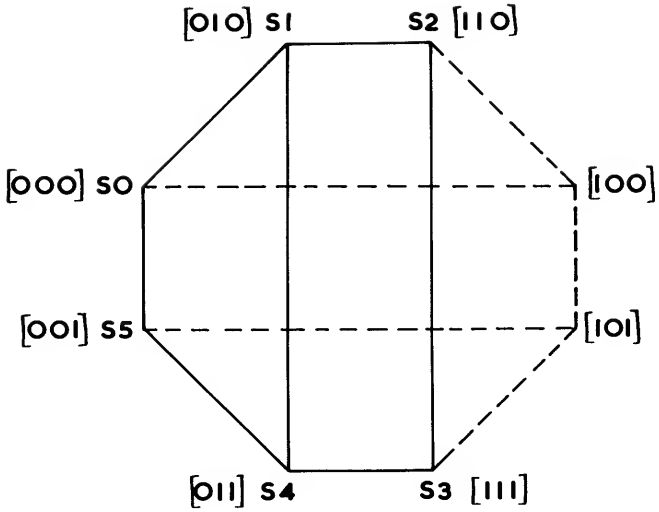
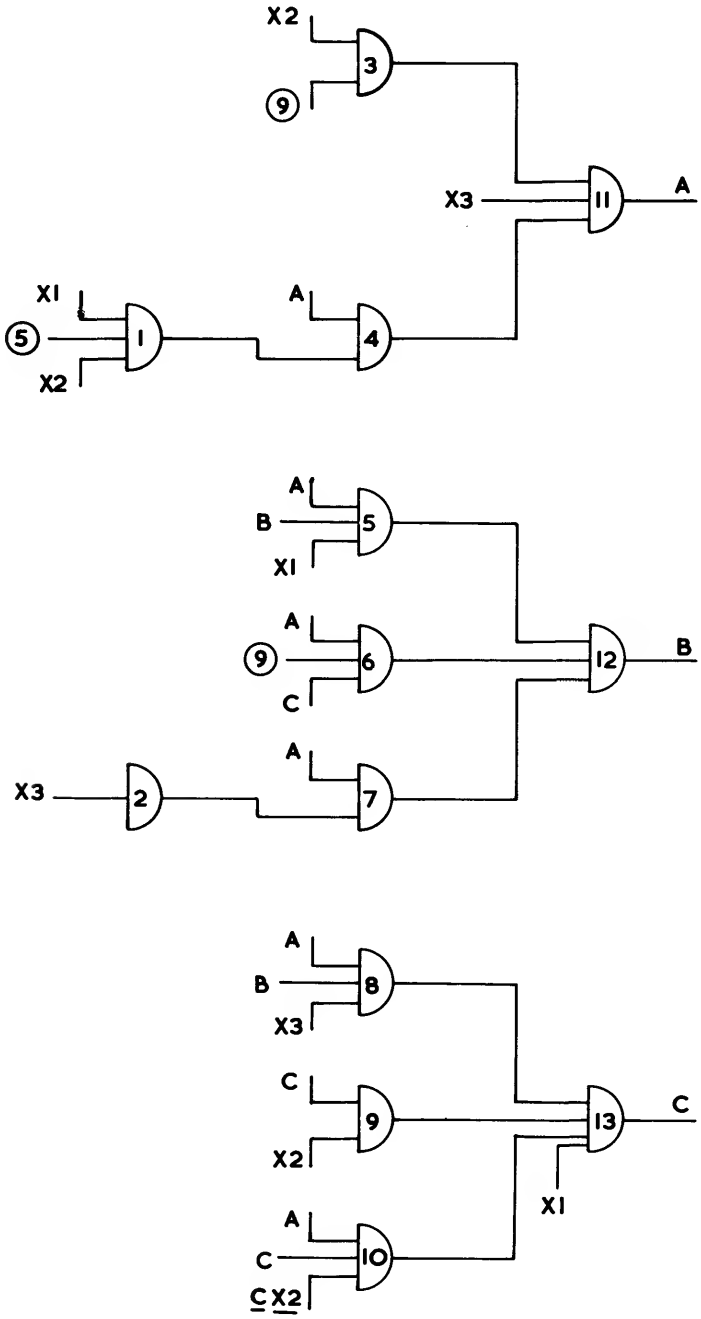


DIAGRAM 18. TRANSITION DIAGRAM OF DESIGN PROBLEM 5

ABC \ X1 X2 X3	000	100	010	001
000	000	010	000	000
010	110	010	000	000
110	110	110	111	010
111	011		111	
011	011	010	010	001
001	000			001

TABLE 13. EXCITATION TABLE OF DESIGN PROBLEM 5



CIRCUIT 6. CIRCUIT REALIZATION OF PROBLEM 5

The output signal Z = circuit state S5 (diagram 17). Algebraically it can be expressed as:

$$S5 = \underline{A}\ C\ X3.$$

Note: The presence of any race-hazards in this circuit have not been investigated. The race-hazard phenomenon is examined in some detail in the next chapter.

DESIGN EXAMPLE 6

A complement plus One Unit.

The design of a unit which accepts a binary number in serial form (least significant digit first) at its input and generates its complement - plus - one at its output terminal will be considered.

It will be assumed that the logical levels '0' and '1' correspond to the signal levels '0' and '1' respectively.

Essentially the unit has to pass unmodified all digits up to and including the first '1' signal and negate the remaining. For example:

INPUT	REQUIRED OUTPUT
1 0 1 1 0 0	0 1 0 1 0 0
0 1 1 0 0 1	1 0 0 1 1 1

The input signal X is transferred into the unit by means of a shift pulse S.

Step.1. The Sequence Diagram

See Diagram 19.

Step.2. The Sequence Table

This is directly derived from diagram 19. See table 14(a).

Step.3. Merging of the Sequence Table

No merging is possible.

Step.4. Allocation of the Secondary Signals

In this case the allocation of secondary signals is straightforward and is shown in Table 14(a). Table 14(b) shows the excitation table resulting from the given allocation of secondary signals.

Step.5. The Secondary Signal Equations

From table 14(b) the following set of minimal equations is directly derived.

$$\underline{A} = \underline{B} + \underline{A}\ \underline{S}$$
$$\underline{B} = \underline{B}\ S + \underline{B}\ \underline{X}$$

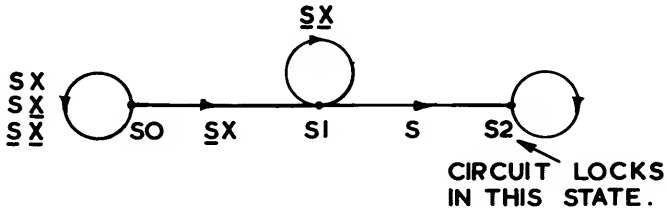


DIAGRAM 19. SEQUENCE DIAGRAM OF PROBLEM 6

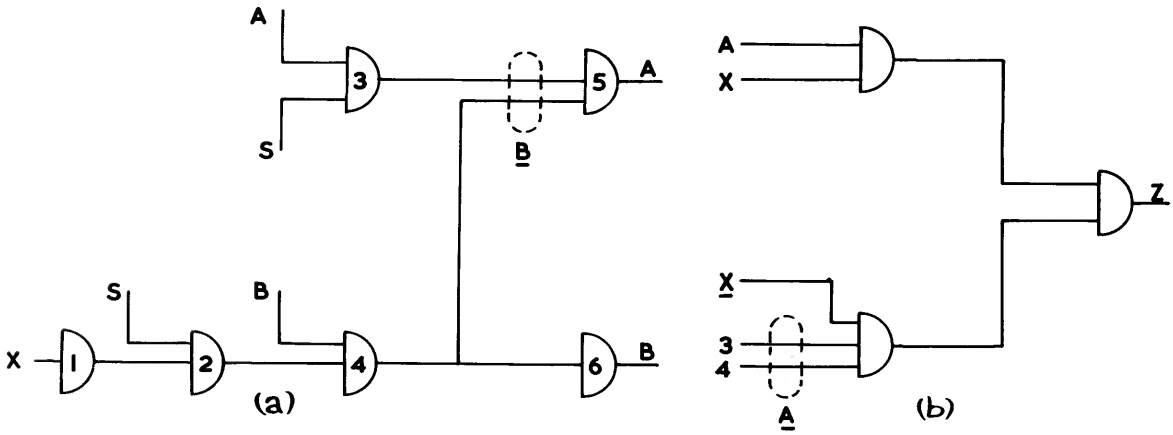
AB \ SX	00	01	11	10
00	S0	S1	S0	S0
01	S1	S1	S2	S2
11	S2	S2	S2	S2

(a)

AB \ SX	00	01	11	10
00	00	01	00	00
01	01	01	11	11
11	11	11	11	11
10				

(b)

TABLE 14. (a) SEQUENCE TABLE OF DESIGN PROBLEM 6
(b) EXCITATION TABLE OF DESIGN PROBLEM 6



CIRCUIT 7. (a) CIRCUIT REALIZATION OF PROBLEM 6
(b) THE COMBINATIONAL PART OF THE UNIT

X	0	1	ABC
S0	S0	S1	000
S1	S2	S1	010
S2	S2	S3	110
S3	S4	S3	111
S4	S4	S5	011
S5	S0	S5	001

(a)

ABC \ X	0	1
000	000	010
010	110	010
110	110	111
111	011	111
011	011	001
001	000	001

(b)

TABLE 15. (a) SEQUENCE TABLE OF DESIGN PROBLEM 7.

(b) EXCITATION TABLE OF DESIGN PROBLEM 7

X	0	1
S0	S0	S1
S1	S2	S1
S2	S2	S3
S3	S4	S3
S4	S4	S5
S5	S6	S5
S6	S6	S7
S7	S8	S7
S8	S8	S9
S9	S0	S9

(a)

ABCD \ X	0	1
0000	0000	0100
0100	1100	0100
1100	1100	1000
1000	1010	1000
1010	1010	1110
1110	0110	1110
0110	0110	0010
0010	0011	0010
0011	0011	0001
0001	0000	0001

(b)

TABLE 16. (a) SEQUENCE TABLE OF DESIGN PROBLEM 8.

(b) EXCITATION TABLE OF DESIGN PROBLEM 8

Step.6. NOR(NAND) Circuit Realisation of the Secondary Equations

The optimisation technique described in chapter 2, is next used to optimise their form.

Inverting

$$A = B(A + S)$$

$$B = (B + \underline{S})(B + X)$$

Merging

$$A = B(A + S)$$

$$B = B + \underline{S}\,X$$

Substitution Signals

There are no suitable substitution signals that can be usefully used in this case.

The equations derived after the merging process are therefore in their optimised form, and circuit 7(a) shows their direct realisation.

The assumption of the value '1' by the secondary signal A may be used to indicate that the input signal X is to be inverted. Therefore algebraically the output signal Z is expressed as

$$Z = X\,\underline{A} + \underline{X}\,A$$

and its realisation is shown in circuit 7(b).

Note :

The presence of any race-hazards in this circuit have not been investigated. The race-hazard phenomenon is examined in some detail in the next chapter.

DESIGN EXAMPLE 7

The step-by-step design of a three-way counter will be considered.

Step.1. The Sequence Diagram

The requirements are so simple in this case, that this step is by-passed.

Step.2. The Sequence Table

This is shown in table 15(a).

Step.3. Merging of the Sequence Table

The table cannot be merged.

Step.4. Allocation of the Secondary Signals

The allocated values of the secondary signals A, B and C are shown on the right-hand side of table 15(a). The corresponding excitation table is shown as table 15(b).

Step.5. The Secondary Signal Equations

From table 15(b) the following set of minimal equations is directly derived.

$$\underline{A} = \underline{B} + \underline{X}\,C + \underline{A}\,X$$

$$\underline{B} = \underline{B}\,\underline{X} + \underline{A}\,C\,X$$

$$\underline{C} = \underline{B}\,\underline{X} + \underline{C}\,\underline{X} + \underline{A}\,\underline{C}$$

Step.6. NOR(NAND) Circuit Realisation of the Secondary Equations

The suggested optimisation technique in chapter 2 will now be used to optimise their form.

Inverting

$$A = B\,(X + \underline{C})\,(A + \underline{X})$$

$$B = (B + X)\,(A + \underline{C} + \underline{X})$$

$$C = (B + X)\,(C + X)\,(A + C)$$

Merging

Not possible.

Substitution Signals

After the introduction of the substitution signals, the above set of equations changes to:

$$A = (B + X)\,(X + \underline{C}\,\underline{X})\,(A + \underline{C}\,\underline{X})$$

$$B = (B + X)\,(A + \underline{A}\,\underline{C} + C\,\underline{X}) = (B + X)(A + \underline{A}\,\underline{C} + (C + X)\underline{X})$$

$$C = (B + X)\,(C + X)\,(A + C)$$

This is the final (optimised) form of the equations and circuit 5 of the next chapter shows their circuit realisation.

Note:

For the investigation and correction of the race-hazards present in the circuit see next chapter.

DESIGN EXAMPLE 8

The step-by-step design of a five-way counter will finally be described.

Step.1. The Sequence Diagram

As in the case of the three-way counter this step is by-passed.

Step.2. The Sequence Table

This is shown in Table 16(a).

Step.3. Merging of the Sequence Table

The table cannot be merged.

Step.4. Allocation of the Secondary Signals

The allocated values of the secondary signals A. B and C are shown in Table 16(b).

Table 16(b) is the circuit's excitation table.

Step.5. The Secondary Signal Equations

From the excitation table, the following set of minimal equations is directly derived.

$$\underline{A} = B\,C\,\underline{X} + \underline{A}\,\underline{B} + \underline{A}\,X$$

$$\underline{B} = \underline{B}\,\underline{X} + \underline{A}\,C\,X + D + A\,\underline{C}\,X$$

$$\underline{C} = \underline{C}\,X + B\,\underline{C} + \underline{A}\,\underline{C} + D\,X$$

$$\underline{D} = B + A + \underline{C}\,\underline{X} + \underline{D}\,X$$

Step.6. NOR/NAND Circuit Realisation of Secondary Signals

The optimisation technique described in chapter 2 is next used to optimise the above equations before they are finally realised.

Inverting

$$A = (\underline{B} + \underline{C} + X)\,(A + B)\,(A + \underline{X})$$

$$B = (B + X)\,(A + \underline{C} + \underline{X})\,\underline{D}\,(\underline{A} + C + \underline{X})$$

$$C = (C + \underline{X})\,(\underline{B} + C)\,(A + C)\,(\underline{D} + \underline{X})$$

$$D = \underline{A}\,\underline{B}\,(C + X)\,(D + \underline{X})$$

Merging

$$A = (\underline{B} + \underline{C} + X)\,(A + B\,\underline{X})$$

$$B = (B + X)(A + \underline{C} + \underline{X})\,\underline{D}\,(\underline{A} + C + \underline{X})$$

$$C = (C + \underline{B}\,\underline{X})\,(A + C)\,(\underline{D} + \underline{X})$$

$$D = \underline{A}\,\underline{B}\,(C + X)\,(D + \underline{X})$$

Substitution Signals

$$A = (\underline{B}\,\underline{X} + \underline{C}\,\underline{X} + X)(A + \underline{X}\,(B + X))$$

$$B = (B + X)(A + \underline{A}\,\underline{C} + C\,\underline{X})\,\underline{D}\,(\underline{A}\,\underline{C} + C + \underline{C}\,\underline{X}) =$$
$$(B + X)(A + \underline{A}\,\underline{C} + (C + X)\,\underline{X})\,\underline{D}\,(\underline{A}\,\underline{C} + C + \underline{C}\,\underline{X})$$

$$C = (C + \underline{B}\,\underline{X})\,(A + C)\,(\underline{B}\,\underline{X} + \underline{D}\,(B + X))$$

$$D = \underline{A}\,\underline{B}\,(C + X)\,(D + \underline{B}\,\underline{X})$$

This is the final (optimised) form of the secondary signal equations and their direct realisation is shown in circuit 8 of the next chapter.

Note:

The analysis of all the race-hazards present in this circuit and their correction is considered in the next chapter.

CHAPTER 6

RACE AND HAZARD PHENOMENA IN SEQUENTIAL CIRCUITS

A routine method allowing the correction of race-hazards to a high degree of reliability is described.

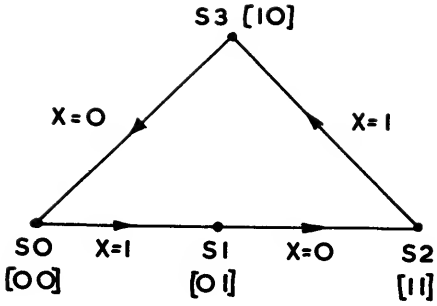
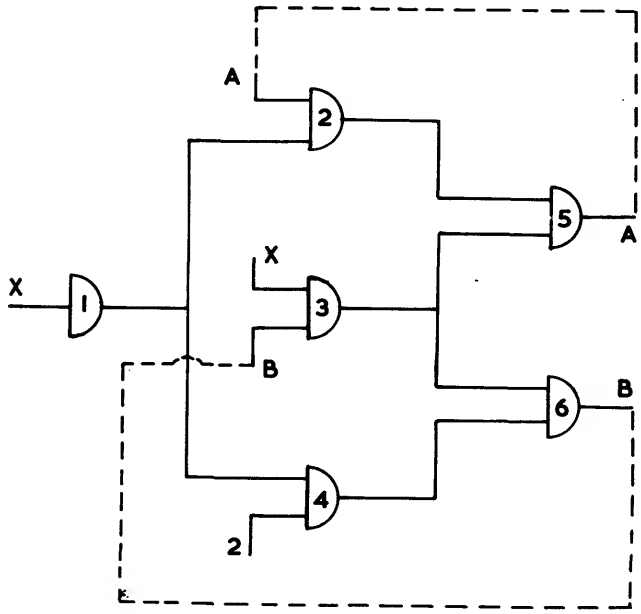


DIAGRAM I. SEQUENCE DIAGRAM OF CIRCUIT I



CIRCUIT I. MINIMAL TWO-WAY COUNTER DESIGNED IN THE PREVIOUS CHAPTER

CIRCUIT STATES.	PRIMARY SIGNAL.	OUTPUT OF MODULE						CLASSIFICATION OF THE RACE - HAZARD
		ONE	TWO	THREE	FOUR	FIVE	SIX	
	X	X	AX	BX	AX	A	B	
SO	0	1	0	1	0	0	0	
					RH1	RH2		RH1 NON-CRITICAL RH2 CRITICAL
S1	1	0	1	0	0	0	1	
					RH3			RH3 CRITICAL
S2	0	1	0	0	0	1	1	
				RH4				RH4 CRITICAL
S3	1	0	0	0	1	1	0	
			RH5				RH6	RH5 CRITICAL RH6 CRITICAL
SO	0	1	0	1	0	0	0	

TABLE I. TRANSITION TABLE OF CIRCUIT I

RACE AND HAZARD PHENOMENA IN SEQUENTIAL CIRCUITS

Race and hazard phenomena in switching circuits are transient phenomena, occurring only during circuit transitions between two adjacent stable circuit states.

Since in the case of the combinational switching circuits the steady-state output signals are determined completely by the combination of the input signals of the moment, any circuit malfunctions due to signal races is confined to the transient states of the circuit.

The steady state condition of the circuit is not affected by signal races.

This, however, is not always the case with sequential circuits. A signal race may result in the permanent mis-operation of the circuit.

Diagram 1 shows the sequence diagram of the minimal two-way-counter shown in circuit 1. Consider the circuit transition of the counter from state S0 to state S1. During this transition secondary signal A remains constant at the logical level '0', whereas secondary signal B changes from 0 to 1. If as a result of a signal race, secondary signal A assumes temporarily the value 1 after secondary signal B has changed to 1, the following circuit mis-operation will occur. The counter moves to circuit state S2 (11) from state S1 (01). But state S2 with X = 1 is an astable state, causing the S2 - S3 transition to take place. That is, instead of the circuit assuming the stable state S1, because of the race-hazard considered it assumes the stable state S3.

Because race hazards are a chance phenomenon, their absence from a given circuit configuration unless systematically verified does not preclude their absence from identical circuit configurations using a different set of switching elements. Means therefore for detecting the probability of their presence and their possible effect on the operation of a given sequential circuit must therefore constitute an essential step in the design routine.

The determination of the presence of race hazards and of their effects in sequential circuits will be explained by examining the minimal two-way counter of circuit 1. A design routine step will next be suggested which will be used to eliminate critical race hazards present in the circuits designed in the previous chapter.

The following stipulation is made:

The outcome of any race, whether between secondary signals, or between secondary and primary signals etc. cannot be assumed. In other words a change in a secondary signal may affect a module before the change of the primary signal that has caused it.

Unless otherwise specified only one primary signal will be assumed to change at a time.

OUTLINE OF THE METHOD

Circuit 1. shows the minimal NOR (NAND) circuit realisation of a two-way counter, designed using the conventional procedure described in the previous chapter. It will now be examined with a view to determining all the race-hazards present in it. A race hazard (the possible appearance of a signal spike) is present at the output of a switching module if, during a circuit transition at least two of its input signals change from 0 to 1 and 1 to 0 respectively and the remaining input signals are ineffective. A signal is ineffective if its presence at the input of a module does not affect the output. For example a signal at the input of an AND gate is ineffective during a circuit transition, if the value of the output of that gate during that transition is 0.

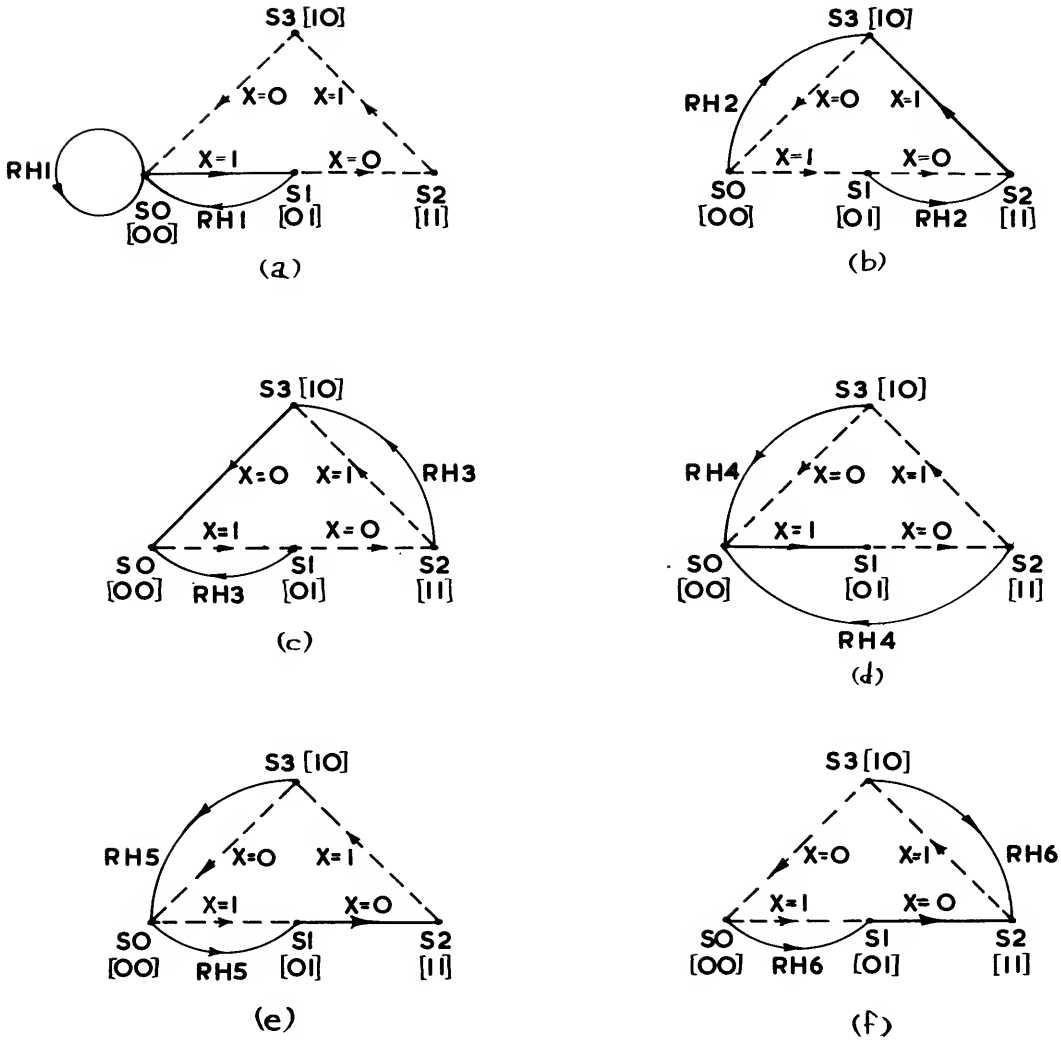


DIAGRAM 2. TRANSITION DIAGRAMS SHOWING ALL POSSIBLE CIRCUIT TRANSITIONS DUE TO RACE HAZARDS PRESENT IN CIRCUIT I

The steady-state outputs of all the modules can readily be determined as a function of the primary and secondary signals, since each circuit state is defined completely by a set of primary and secondary signals. The steady state outputs of the modules of circuit 1 are plotted in Table. 1.

Table 1. can now be used to determine the presence of race-hazards at the output of each module. This is achieved by examining simultaneously the columns corresponding to the input signals of each module in turn.

Module 1.

Since there is only one input signal, there can be no race-hazard at its output.

Module 2.

To determine the presence of race-hazards at the output of module 2, the columns corresponding to modules 1 and 5 are examined simultaneously.

The S0 - S1 transition is hazard-free, since only one signal (output of module 1) changes from 1 to 0, whereas the second signal (output of module 5) remains at 0.

The S1 - S2 involves the change of both signals from 0 to 1, therefore this transition is also hazard-free. The S2 - S3 is also hazard-free, since the output of module 5 does not change.

The S3 - S0 circuit transition invplves the change of the output of module 1 from 0 to 1 and of the output of module 5 from 1 to 0. Therefore a race-hazard is present at the output of module 2 during the S3 - S0 transition, which is referred to as RH5 (race-hazard 5) in table 1.

Using the same procedure the remaining hazards are also marked - see table 1.

Having determined the presence of all the race-hazards possible in the circuit, the next step is to investigate their effects on the circuit operation

Because a race-hazard appears during a circuit transition between two adjacent stable states, it is not possible to determine whether the hazard has appeared before or after the change over of the circuit. For example race-hazard RH1 at the output of module 4 may appear either before or after secondary signal B changes from 0 to 1. Therefore the effect of the presence of the race-hazards in each of the two adjacent stable states will always be examined.

Race-hazard RH1. The presence of race-hazard RH1 at the output of module 4, is to cause the output of module 6 (secondary signal B) to assume the logical level 0.

If the hazard appears while the circuit is still in stable state S0, it will obviously have no effect at all on the circuit operation.

If on the other hand RH1 appears after the circuit has assumed state S1, it will cause secondary signal B to change to 0 temporarily. That is, the circuit moves temporarily to state S0 - see diagram 2(a). But at the end of the race-hazard it will move back to state S1, as shown in diagram 2(a)

Because race-hazard RH1 does not affect permanently the S0 - S1 state, it is classified as NON-CRITICAL.

It may however, be critical, if for example, the output of module 6 is used to drive another counter.

Race-hazard R.H.2. If race-hazard R.H.2. appears while the circuit is still in the S0 state, it will cause the S0 - S3 transition. But circuit state S3 with X = 1 is a stable state, hence the circuit will lock in that state - see diagram 2(b). If on the other hand the circuit has assumed the S1 state when race-hazard R.H.2. appears, it will move to state S2 - see diagram 2 (b). But this is an astable state for X = 1, and the circuit moves to state S3, which is a stable configuration with X = 1.

Therefore the appearance of race-hazard R.H.2. will cause the permanent malfunction of the circuit, and this is therefore classified as CRITICAL.

Using the same method, all the possible effects of the remaining race-hazards on the circuit operation are determined - see diagram 2. Their classification is shown in Table.1.

Derivation of the Correcting (blanking) Signals

The derivation of the general correcting signal Kmn needed to blank out a race-hazard during a circuit transition from stable state Sm to stable state Sn will now be considered.

Switching the Correcting Signal ON

To eliminate a possible race between the switching ON of the correcting signal and the race-hazard, the correcting signal Kmn is switched ON during stable state Sm. This ensures that the correcting signal Kmn has reached its steady state value before the transition to circuit state Sn. Algebraically this is equivalent to adding a term Sm to the minimal equation for Kmn, Kmn = Smn. Therefore the equation now becomes:

$$Kmn = Sm + Smn$$

Switching the Correcting Signal OFF

To avoid switching OFF the correcting signal Kmn before stable state Sn has been reached, it is necessary to derive a signal which indicates that stable state Sn has been reached. But the only' positive indication that stable state Sn has been reached is the transition (complete or partial) of the circuit to the next stable state Sp. But in most cases the correcting signal Kmn prevents the transition of the circuit to stable state Sp.

To explain this, consider the effect of the correcting signal K01 on the S1 - S2 circuit transition. If correcting signal K01 is present in the S1 state, it will prevent secondary signal A from changing to 1 and thus the circuit does not move to state S2.

It can therefore be seen that the correcting signal K01, though preventing the complete transition of the circuit to stable state S2, it allows the circuit to assume an intermediate state in which the primary signal has the value corresponding to state S2, whereas the secondary signals have the values corresponding to state S1. Such an intermediate state can therefore be used to switch the correcting signal K01 off.

The equation for the general correcting signal Kmn now therefore becomes

$$Kmn = Sm + Smn + Sn \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

Table 2 is the transition table of the two-way counter. From table 2 and equation (1) the following set of equations of the correcting signals is derived:

$$K01 = S0 + S01 + S1$$
$$K12 = S1 + S12 + S2$$
$$K23 = S2 + S23 + S3$$
$$K30 = S3 + S30 + S0$$

Circuit 2 shows the two-way counter with the correcting signals inserted. Correcting signal K01 ensures that signal A is kept at its '0' logical level during the S0 - S01 transition. Similarly correcting signal K12 keeps the output of driver module 4 at logical level '0' in the S1 - S12 transition, thus preventing secondary signal B from changing to 0.....etc.

The general rule is: To keep the secondary signal at the logical level '0', apply the correcting signal to one of its inputs directly, whereas to keep it at the logical level '1', apply the correcting signal to its driver module which may change it due to a race-hazard.

The circuit realisation of the correcting signals will now be examined.

From table 2,

$$K01 = \underline{A}\,\underline{B}\,\underline{X} + \underline{A}\,\underline{B}\,X + \underline{A}\,B\,X = \underline{A}\,\underline{B} + \underline{A}\,X = \underline{A}(\underline{B} + X) \quad \ldots\ldots (2)$$

$$K12 = \underline{A}\,B\,X + \underline{A}\,B\,\underline{X} + A\,B\,\underline{X} = \underline{A}\,B + B\,\underline{X} = B(\underline{A} + \underline{X}) \quad \ldots\ldots (3)$$

$$K23 = A\,B\,\underline{X} + A\,B\,X + A\,\underline{B}\,X = A\,B + A\,X = A(B + X) \quad \ldots\ldots (4)$$

$$K30 = A\,\underline{B}\,X + A\,\underline{B}\,\underline{X} + \underline{A}\,\underline{B}\,\underline{X} = A\,\underline{B} + \underline{B}\,\underline{X} = \underline{B}(A + \underline{X}) \quad \ldots\ldots (5)$$

Now, referring to circuit 2,

$$\underline{A} = \underline{A}\,X\,\underline{K30} + \underline{B}\,\underline{X}\,\underline{K23} + K01 \quad \ldots\ldots (6)$$

$$\underline{B} = \underline{B}\,\underline{X}\,\underline{K23} + A\,X\,\underline{K12} + K30 \quad \ldots\ldots (7)$$

Substituting (7) in (2) we get

$$K01 = \underline{A}\,(\underline{B}\,\underline{X}\,\underline{K23} + A\,X\,\underline{K12} + K30 + X \quad \ldots\ldots (8)$$

During the presence of the correcting signal K01, secondary signal A is constant, whereas secondary signal B changes. Therefore although the basic Boolean relationships $P + \underline{P} = 1$ and $P.\underline{P} = 0$, do not hold for the variable B, they hold for the variable A.

Equation (8) can now be reduced to

$$K01 = \underline{A}\,(\underline{B}\,\underline{X}\,\underline{K23} + K30 + X) \quad \ldots\ldots (9)$$

It must be noted at this stage, that the signals within the bracket of equation (8) must not be modified, since they are available in this form in the circuit. In other words a term may be discarded completely but not modified.

Using the same procedure the equations for the remaining correcting signals are next derived.

$$K12 = B(\underline{A} + \underline{X}) = B(\underline{A}\ X\ \underline{K30} + \underline{B}\ \underline{X}\ \underline{K23} + K01 + \underline{X})$$

$$= B(\underline{A}\ X\ \underline{K30} + K01 + \underline{X}),$$ since B is constant during the S1 - S2 transition.

$$K23 = A(B + X)$$

$$K30 = \underline{B}(A + \underline{X})$$

Circuit 3 shows the correcting circuits for all possible transitions.

It must be repeated at this stage, not all the circuits need be used in practice. The decision of what correcting signals must be introduced into the initial minimal circuit remains with the designer. The decision has to be made in the light of the degree of safety, circuit economy etc.

Degree of Circuit Reliability Achieved by the Introduction of the Correcting Signals

The degree of reliability introduced by this form of correcting signal is possibly best determined by examining the performance of the two-way counter before and after the introduction of the correcting signals. More specifically, correcting signal K01 will be examined in some detail.

An examination of circuit 3(a) generating the correcting signal K01, reveals that in it, there exists a race hazard, which may affect the value of K01 during the S0 - S1 circuit transition that is, in the S01 state. But the chances of this happening are remote, because there are three signals changing during this transition, namely, output of module 3 from 1 to 0, K30 from 0 to 1 and X from 0 to 1. In the S01 transient state, both the last two signals have the value of 1.

For the value of A to change to '1' during the S0 - S1 circuit transition there must now be coincidence between two race-hazards at the input of module 5. Since a race hazard is a chance phenomenon, the possibility of both being revealed at the same time at the input of a module, specially when one hazard is delayed with respect to the other by two modules (7 and 8) is remote. Circuit 4 will possibly help to visualise this phenomenon even better.

The effect of the remaining correcting signals or their corresponding parts of the two-way counter are the same.

As with most of the topics included in this manual, research is being carried out continually on sequential circuits. To avoid the time delay between the finished reports and their publications, the authors will be pleased to send copies of their findings immediately to all those interested, on request.

The correction of the race-hazards in sequential circuits using the method described, becomes essentially a routine procedure consisting of the following steps.

Step.1.

In this step the transition table of the sequential circuit to be corrected is plotted, by first introducing the values of the primary and secondary signals for each stable state (these values are given). Since the outputs of all the other modules are a function of the primary and secondary signals only, their values for each stable circuit state can also be inserted in the transition table.

Step.2.

The columns corresponding to the input signals of each module in turn are examined next, two at a time. If during a given circuit transition two signals change from 01 to 10 and none of the remaining input signals, if present, are equal to 1 during the same transition, then a race-hazard is present at the output of the module under consideration.

Step.3.

In the third step, the effect of each race-hazard on the circuit performance is determined. During a certain circuit transition the value of a secondary signal changes e.g. 0 to 1. Now if during the same transition, the effect of a race-hazard on this secondary signal is to make it change from 0 to 1, then this race-hazard is non-critical. Consider R.H.1. in table 1. Because secondary signal B changes during S0 - S1 transition from 0 to 1, then R.H.1. can have no critical effect since it in turn is tending to alter the value to 1.

Step.4.

The correcting signals are first expressed in their standard form - that is

$$Kmn = Sm + Smn + Sn + Klm$$

By simplifying and taking common factors, it reduces to a bracket (OR term) multiplied by a factor. In its minimal form the factor is constant, whereas all the terms within the bracket change during the corresponding circuit transition. For example, equation 2 becomes,

$$K01 = \underline{A}\,(\underline{B} + X + K30)$$

A remains constant during the S0 - S1 circuit transition whereas the bracket $(\underline{B} + X + K30)$ changes from $(1 + 0 + 1)$ to $(0 + 1 + 0)$.

Step.5.

The inverted secondary signals within the bracket are first replaced by the sum of the inputs to their corresponding module. For example, $\underline{B}$ in equation 2 is replaced by $\underline{B}\ X\ \underline{K23}$, $A\ X\ \underline{K12}$ and K30 - that is, by the input signals to module 6 of circuit 2. The bracket is then minimised. A term may be eliminated but not modified within a bracket, since each term is the output of a module. The secondary signals multiplying the bracket, when present in their true form, are next replaced. For example, equation 3 is modified from

$$K12 = B(\underline{A}\ X\ \underline{K30} + K01 + X)$$

to $$\underline{3}\ .\ \underline{4}\ .\ \underline{K30}\ (2 + K01 + \underline{X})\ .$$

No further minimisation is possible. The correcting signals outside the 'bracket', if present are redundant and may therefore be eliminated.

EXAMPLE 1

The Correction of Race-hazards in the Three-Way Counter

The Circuit has been designed in the previous chapter.

Step.1.

Table 3. - its transition table - is plotted.

Step.2.

The race-hazards are determined and marked, as shown in table 3.

Step.3.

R.H.1. is non-critical, since the output of module 7 is '0' in the S0 and S1 circuit state.

R.H.3. is also non-critical, since, if it does reveal itself it will affect secondary signal A, which is the signal responsible for the S1-S2 circuit transition, etc..

Step.4.

The equations of the correcting signals are first derived in their standard form.

$$K01 = S0 + S01 + S1 = \underline{A}\,\underline{B}\,\underline{C}\,\underline{X} + \underline{A}\,\underline{B}\,\underline{C}\,X + \underline{A}\,B\,\underline{C}\,X = \underline{A}\,\underline{B}\,\underline{C} + \underline{A}\,\underline{C}\,X$$

$$= \underline{A}\,\underline{C}\,(\underline{B} + X) = \underline{A}\,\underline{C}\,(\underline{B} + X + K50) \quad \ldots\ldots (10)$$

$$K12 = S1 + S12 + S2 = \underline{A}\,B\,\underline{C}\,X + \underline{A}\,B\,\underline{C}\,\underline{X} + A\,B\,\underline{C}\,\underline{X} = \underline{A}\,B\,\underline{C} + B\,\underline{C}\,\underline{X} = B\,\underline{C}\,(\underline{A} + \underline{X})$$

$$= B\,\underline{C}\,(\underline{A} + \underline{X} + K01) \quad \ldots\ldots (11)$$

$$K23 = S2 + S23 + S3 = A\,B\,\underline{C}\,\underline{X} + A\,B\,\underline{C}\,X + A\,B\,C\,X = A\,B\,\underline{C} + A\,B\,X = A\,B\,(\underline{C} + X)$$

$$= A\,B\,(\underline{C} + X + K12) \quad \ldots\ldots (12)$$

$$K34 = S3 + S34 + S4 = A\,B\,C\,X + A\,B\,C\,\underline{X} + \underline{A}\,B\,C\,\underline{X} = A\,B\,C + B\,C\,\underline{X} = B\,C\,(A + \underline{X})$$

$$= B\,C\,(A + \underline{X} + K23) \quad \ldots\ldots (13)$$

$$K45 = S4 + S45 + S5 = \underline{A}\,B\,C\,\underline{X} + \underline{A}\,B\,C\,X + \underline{A}\,\underline{B}\,C\,X = \underline{A}\,B\,C + \underline{A}\,C\,X = \underline{A}\,C\,(B + X)$$

$$= \underline{A}\,C\,(B + X + K34) \quad \ldots\ldots (14)$$

$$K50 = S5 + S50 + S0 = \underline{A}\,\underline{B}\,C\,X + \underline{A}\,\underline{B}\,C\,\underline{X} + \underline{A}\,\underline{B}\,\underline{C}\,\underline{X} = \underline{A}\,\underline{B}\,C + \underline{A}\,\underline{B}\,\underline{X} = \underline{A}\,\underline{B}\,(C + \underline{X})$$

$$= \underline{A}\,\underline{B}\,(C + \underline{X} + K45) \quad \ldots\ldots (15)$$

The above equations are next optimised, first by substituting for the inverted signals within the bracket and minimising, followed by substituting for the true signals outside the bracket.

$$K01 = \underline{A}\,\underline{C}\,(\underline{B} + X + K50) = \underline{A}\,\underline{C}\,(\underline{B}\,\underline{X}\,\underline{K45} + K50 + \underline{A}\,C\,X\,\underline{K12}\,\underline{K34} + X + K50)$$

$$= \underline{A}\,\underline{C}\,(\underline{B}\,\underline{X}\,\underline{K45} + K50 + X) \quad \ldots\ldots (16)$$

(See circuit 7(a)).

$$K12 = B\,\underline{C}\,(A + \underline{X} + K01) = B\,\underline{C}\,(\underline{A} + \underline{C}\,\underline{X} + K01) = B\,\underline{C}\,(K01 + K50 + \underline{K23}\,C\,\underline{X} + \underline{A}\,(C + X) + \underline{B}\,\underline{X}\,\underline{K45} + \underline{C}\,\underline{X} + K01)$$

$$= B\,\underline{C}\,(K01 + K50 + \underline{A}\,(C + X) + \underline{C}\,\underline{X})$$

$$= B\,\underline{C}\,(K01 + K50 + 2 + 5)$$

$$= \underline{K50} \,.\, \underline{3} \,.\, \underline{4} \,.\, \underline{C}\,(K01 + K50 + 2 + 5)$$

$$= \underline{3} \,.\, \underline{4} \,.\, \underline{C}\,(K01 + 2 + 5) \quad \ldots\ldots (17)$$

(See circuit 7 (b)).

$$K23 = A\,B\,(\underline{C} + \underline{X} + K12) = A\,B\,(K12 + \underline{B}\,\underline{K45}\,\underline{X} + \underline{C}\,\underline{X} + \underline{A}\,\underline{C} + X + K12)$$

$$= A\,B\,(K12 + \underline{C}\,\underline{X} + X) = A\,B\,(K12 + 5 + X)$$

$$= \underline{K01}\,\underline{K50}\,\underline{1}\,\underline{2}\,\underline{4}\,\underline{3}\,\underline{K50}\,\underline{4}\,(K12 + 5 + X)$$

$$= \underline{1}\,\underline{2}\,\underline{3}\,\underline{4}\,(K12 + 5 + X) \quad \ldots\ldots (18)$$

(See circuit 7(c))

$$K34 = B\,C\,(A + \underline{X} + K23) = B\,C\,(A + \underline{K23}\,C\,\underline{X} + K23)$$

$$= \underline{3}\,\underline{K50}\,\underline{4}\,\underline{K12}\,\underline{4}\,\underline{5}\,\underline{6}\,(A + 1 + K23)$$

$$= \underline{3}\,\underline{4}\,\underline{5}\,\underline{6}\,(A + 1 + K23) \quad \ldots\ldots (19)$$

(See circuit 7(d)).

$$K45 = \underline{A}\,C\,(B + X + K34) = \underline{A}\,\underline{K12}\,\underline{4}\,\underline{5}\,\underline{6}\,(B + X + K34)$$

$$= \underline{A}\,\underline{4}\,\underline{5}\,\underline{6}\,(B + X + K34) \quad \ldots\ldots (20)$$

(See Circuit 7(e)).

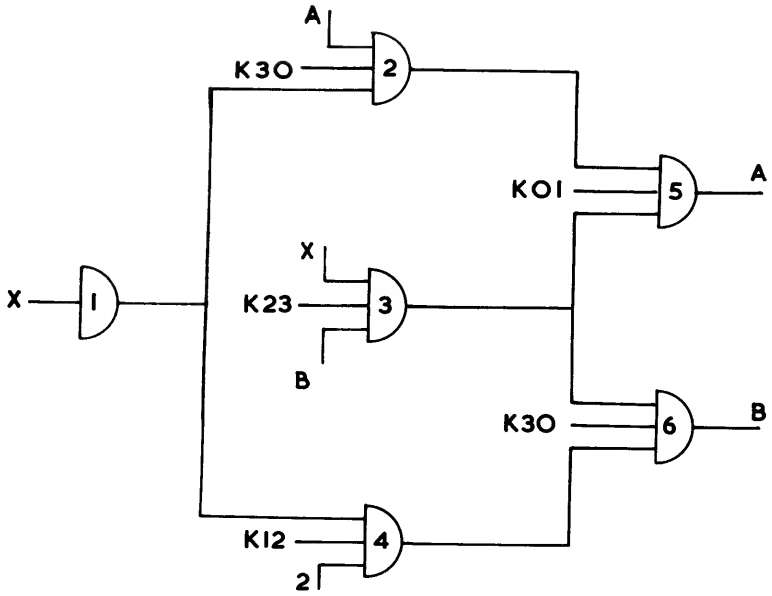
$$K50 = \underline{A}\,\underline{B}\,(C + \underline{X} + K45) = \underline{A}\,\underline{B}\,(C + \underline{C}\,\underline{X} + K45)$$

$$= \underline{A}\,\underline{B}\,(C + 5 + K45) \quad \ldots\ldots (21)$$

(See circuit 7(f)).

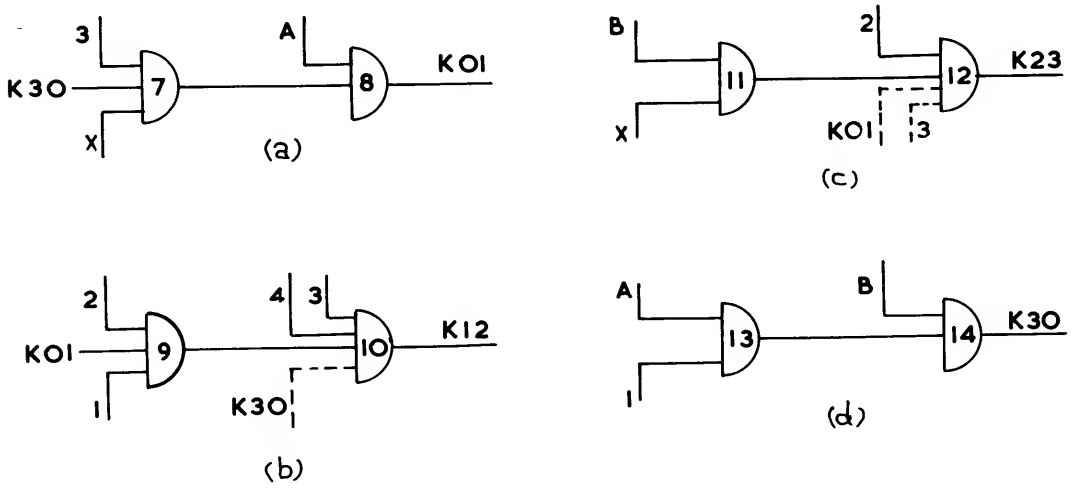
CIRCUIT STATES	X	A	B
S0	0	0	0
S01	1	0	0
S1	1	0	1
S12	0	0	1
S2	0	1	1
S23	1	1	1
S3	1	1	0
S30	0	1	0

TABLE 2. TRANSITION TABLE OF CIRCUIT I SHOWING THE PRIMARY & SECONDARY SIGNALS ONLY

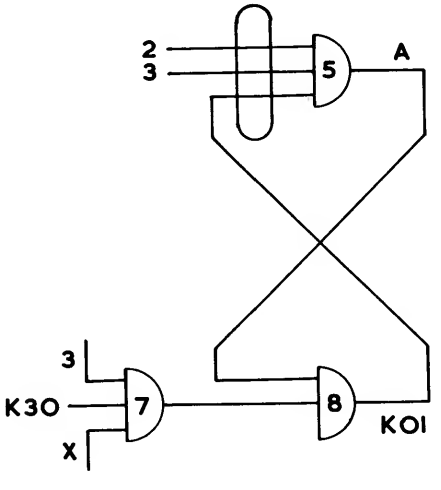


CIRCUIT 2. MINIMAL TWO-WAY COUNTER AFTER THE INTRODUCTION OF THE CORRECTING SIGNALS

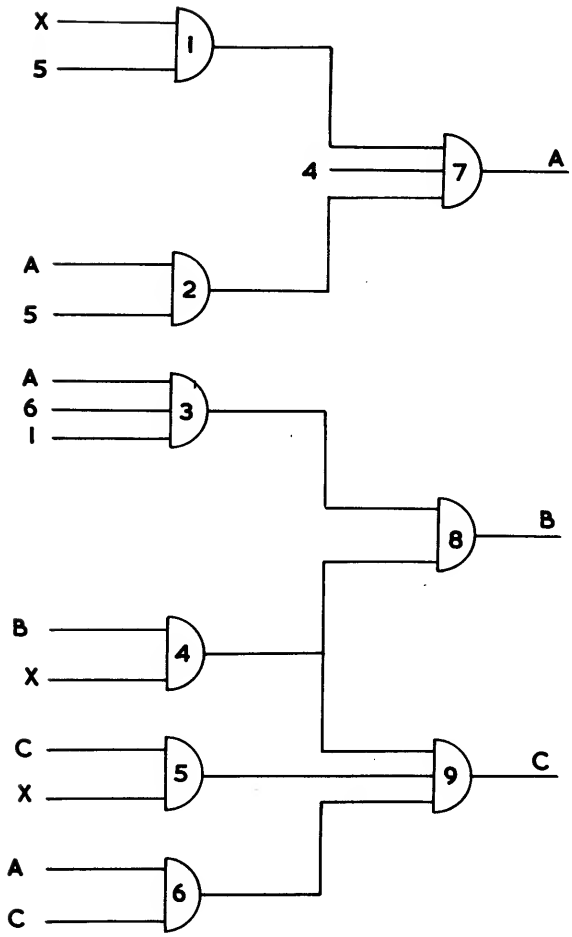
NOTE - THE NUMBER AT THE INPUT OF A MODULE INDICATES THE ORIGIN OF THE INPUT SIGNAL - E.G. OUTPUT OF MODULE 2 IS CONNECTED TO THE INPUT OF MODULE 4.



CIRCUIT 3. CORRECTING CIRCUITS FOR THE TWO-WAY COUNTER OF CIRCUIT 1



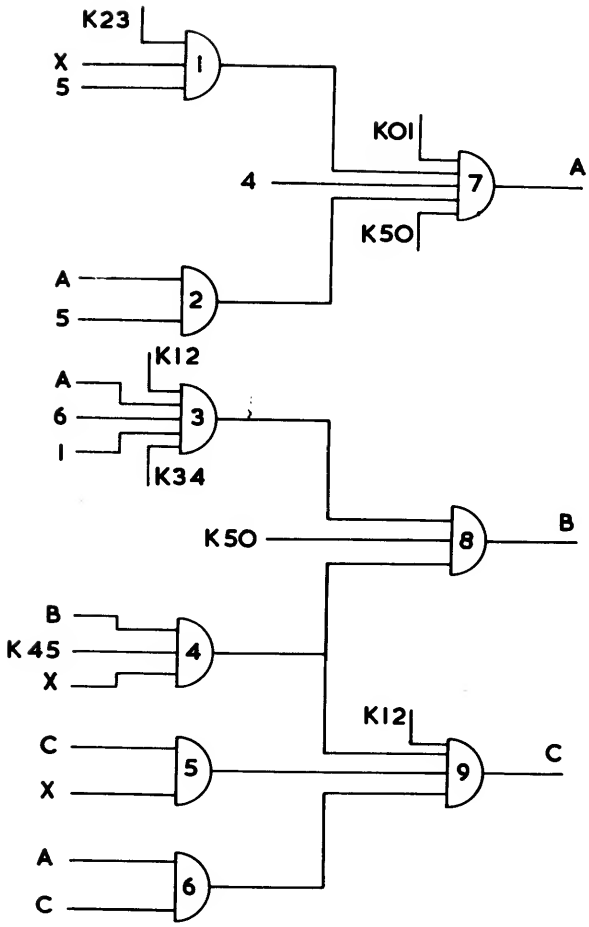
CIRCUIT 4. CORRECTING CIRCUIT K01 AND CORRESPONDING CORRECTED MODULE 5 DRAWN IN A FORM OF A TOGGLE



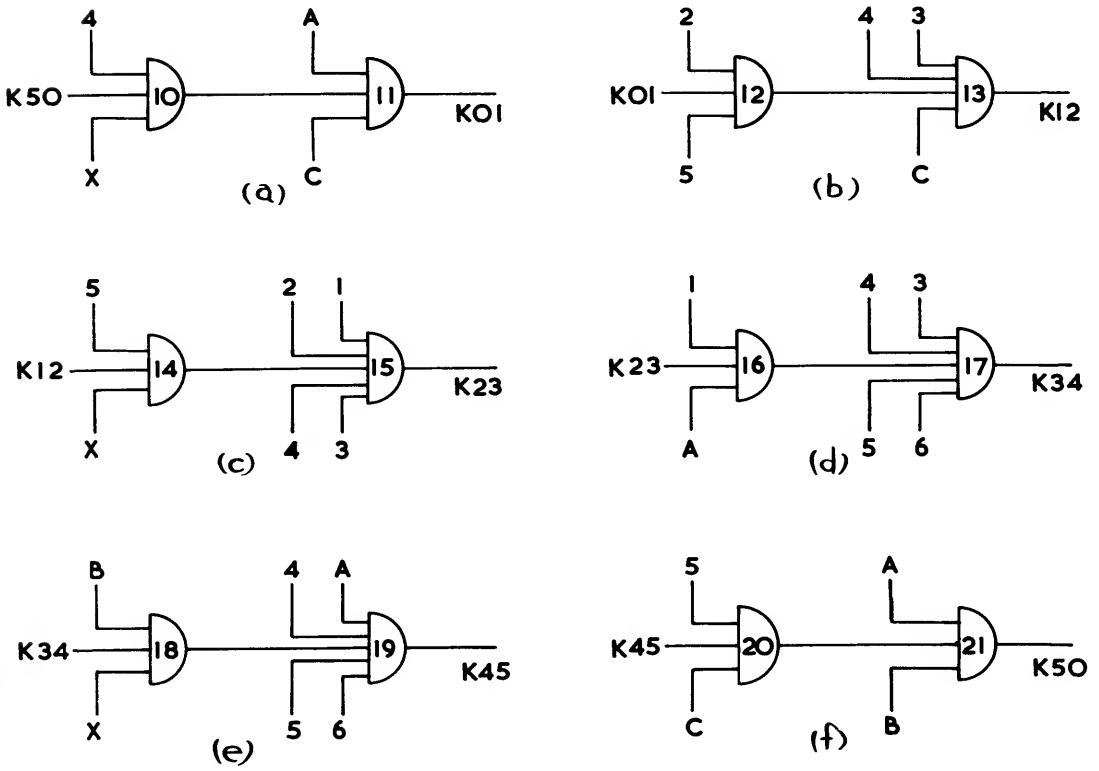
CIRCUIT 5. MINIMAL THREE-WAY COUNTER

CIRCUIT STATES	PRIMARY SIGNAL	OUTPUT OF MODULE									CLASSIFICATION OF THE RACE-HAZARDS
		ONE	TWO	THREE	FOUR	FIVE	SIX	SEVEN	EIGHT	NINE	
	X	CX	A[C+X]	ACX	BX	CX	AC	A	B	C	
S0	0	0	0	0	1	1	1	0	0	0	
		RH1						RH2			RH1 NON-CRITICAL RH2 CRITICAL
S1	1	0	1	0	0	0	1	0	1	0	
		RH3		RH4						RH5	RH3 NON-CRITICAL RH4/RH5 CRITICAL
S2	0	0	0	0	0	1	0	1	1	0	
		RH6									RH6 CRITICAL
S3	1	0	0	0	0	0	0	1	1	1	
				RH7							RH7 CRITICAL
S4	0	1	1	0	0	0	0	0	1	1	
					RH8						RH8 CRITICAL
S5	1	0	1	1	0	0	0	0	0	1	
		RH9						RH10	RH11		RH9 NON CRITICAL RH10/RH11 CRITICAL.
S0	0	0	0	0	1	1	1	0	0	0	

TABLE 3. TRANSITION TABLE OF CIRCUIT 5



CIRCUIT 6. MINIMAL THREE-WAY COUNTER AFTER THE INTRODUCTION OF THE CORRECTING SIGNALS



CIRCUIT 7. CORRECTING CIRCUITS FOR THE MINIMAL THREE-WAY COUNTER SHOWN IN CIRCUIT 6

EXAMPLE 2

The Correction of Race-hazards in the Five Way Counter

The circuit has been designed in the previous chapter.

Step. 1.

Table 4 - its transition table is plotted.

Step. 2.

The race-hazards are determined and marked, as shown in table 4.

Step. 3.

The effect of each race-hazard on the circuit operation is determined, and is accordingly classified as critical of non-critical, irrespective of the degree of the probability of its occurence.

Step. 4.

The equations of the correcting signals are first derived in their standard form.

$$K01 = S0 + S01 + S1 = \underline{A}\,\underline{B}\,\underline{C}\,\underline{D}\,\underline{X} + \underline{A}\,\underline{B}\,\underline{C}\,\underline{D}\,X + \underline{A}\,B\,\underline{C}\,\underline{D}\,X$$

$$= \underline{A}\,\underline{C}\,\underline{D}\,(\underline{B} + X) = \underline{A}\,\underline{C}\,\underline{D}\,(\underline{B} + X + K90) \quad \ldots\ldots (22)$$

$$K12 = S1 + S12 + S2 = \underline{A}\,B\,\underline{C}\,\underline{D}\,X + \underline{A}\,B\,\underline{C}\,\underline{D}\,\underline{X} + A\,B\,\underline{C}\,\underline{D}\,\underline{X}$$

$$= B\,\underline{C}\,\underline{D}\,(\underline{A} + \underline{X}) = B\,\underline{C}\,\underline{D}\,(\underline{A} + \underline{X} + K01) \quad \ldots\ldots (23)$$

$$K23 = S2 + S23 + S3 = A\,B\,\underline{C}\,\underline{D}\,\underline{X} + A\,B\,\underline{C}\,\underline{D}\,X + A\,\underline{B}\,\underline{C}\,\underline{D}\,X$$

$$= A\,\underline{C}\,\underline{D}\,(B + X) = A\,\underline{C}\,\underline{D}\,(B + X + K12) \quad \ldots\ldots (24)$$

$$K34 = S3 + S34 + S4 = A\,\underline{B}\,\underline{C}\,\underline{D}\,X + A\,\underline{B}\,\underline{C}\,\underline{D}\,\underline{X} + A\,\underline{B}\,C\,\underline{D}\,\underline{X}$$

$$= A\,\underline{B}\,\underline{D}\,(\underline{C} + \underline{X}) = A\,\underline{B}\,\underline{D}\,(\underline{C} + \underline{X} + K23) \quad \ldots\ldots (25)$$

$$K45 = S4 + S45 + S5 = A\,\underline{B}\,C\,\underline{D}\,\underline{X} + A\,\underline{B}\,C\,\underline{D}\,X + A\,B\,C\,\underline{D}\,X$$

$$= A\,C\,\underline{D}\,(\underline{B} + X) = A\,C\,\underline{D}\,(\underline{B} + X + K34) \quad \ldots\ldots (26)$$

$$K56 = S5 + S56 + S6 = A\,B\,C\,\underline{D}\,X + A\,B\,C\,\underline{D}\,\underline{X} + \underline{A}\,B\,C\,\underline{D}\,\underline{X}$$

$$= B\,C\,\underline{D}\,(A + \underline{X}) = B\,C\,\underline{D}\,(A + \underline{X} + K45) \quad \ldots\ldots (27)$$

$$K67 = S6 + S67 + S7 = \underline{A}\,B\,C\,\underline{D}\,\underline{X} + \underline{A}\,B\,C\,\underline{D}\,X + \underline{A}\,\underline{B}\,C\,\underline{D}\,X$$

$$= \underline{A}\,C\,\underline{D}\,(B + X) = \underline{A}\,C\,\underline{D}\,(B + X + K56) \quad \ldots\ldots (28)$$

$$K78 = S7 + S78 + S8 = \underline{A}\,\underline{B}\,C\,\underline{D}\,X + \underline{A}\,\underline{B}\,C\,\underline{D}\,\underline{X} + \underline{A}\,\underline{B}\,C\,D\,\underline{X}$$

$$= \underline{A}\,\underline{B}\,C\,(\underline{D} + \underline{X}) = \underline{A}\,\underline{B}\,C\,(\underline{D} + \underline{X} + K67) \quad \ldots\ldots (29)$$

$$K89 = S8 + S89 + S9 = \underline{A}\,\underline{B}\,C\,D\,\underline{X} + \underline{A}\,\underline{B}\,C\,D\,X + \underline{A}\,\underline{B}\,\underline{C}\,D\,X$$

$$= A\,B\,D\,(C + X) = A\,B\,D\,(C + X + K78) \quad \ldots\ldots (30)$$

$$K90 = S9 + S90 + S0 = \underline{A}\,\underline{B}\,\underline{C}\,D\,X + \underline{A}\,\underline{B}\,\underline{C}\,D\,\underline{X} + \underline{A}\,\underline{B}\,\underline{C}\,\underline{D}\,\underline{X}$$

$$= \underline{A}\,\underline{B}\,\underline{C}\,(D + \underline{X}) = \underline{A}\,\underline{B}\,\underline{C}\,(D + \underline{X} + K89) \quad \ldots\ldots (31)$$

The above equations are next optimised, first by substituting for the inverted signals within the bracket and minimising, followed by substituting for the true signals outside the bracket.

$$K01 = \underline{A}\,\underline{C}\,\underline{D}\,(\underline{B}\,\underline{X} + \underline{A}\,C\,X + D + A\,\underline{C}\,X + X + K34 + K90)$$

$$= \underline{A}\,\underline{C}\,\underline{D}\,(\underline{B}\,\underline{X} + X + K90) = \underline{A}\,\underline{C}\,\underline{D}\,(4 + X + K90) \quad \ldots\ldots (32)$$

(See circuit 9(a)).

$$K12 = B\,\underline{C}\,\underline{D}\,(\underline{A} + B\,\underline{X} + K01) = B\,\underline{C}\,\underline{D}\,(B\,C\,\underline{X}\,\underline{K23} \,.\, \underline{K34} \,.\, \underline{K45} \,.\, \underline{K78} +$$

$$+ \underline{A}(\underline{B} + X) + K67 + B\,\underline{X} + K02\,) = B\,\underline{C}\,\underline{D}\,(\underline{A}\,(\underline{B} + X) + B\,\underline{X} + K01)$$

$$= B\,\underline{C}\,\underline{D}\,(3 + 1 + K01\,) = \underline{D} \,.\, \underline{4} \,.\, \underline{5} \,.\, \underline{6}\,\underline{C} \,.\, \underline{D}\,(3 + 1 + K01)$$

$$= \underline{D} \,.\, \underline{4} \,.\, \underline{5} \,.\, \underline{6} \,.\, \underline{C}\,(1 + 3 + K01) \quad \ldots\ldots (33)$$

(See circuit 9(b)).

$$K23 = A\,\underline{C}\,\underline{D}\,(B + X + K12) = \underline{2} \,.\, \underline{3} \,.\, \underline{D} \,.\, (B + X + K12) \quad \ldots\ldots (34)$$

(See circuit 9(c)).

$$K34 = A\,\underline{B}\,\underline{D}\,(\underline{C} + \underline{X} + K23) = A\,\underline{B}\,\underline{D}\,(\underline{C} + \underline{B}\,\underline{X} + K23)$$

$$= A\,\underline{B}\,\underline{D}\,(\underline{C}\,(B + X) + \underline{A}\,\underline{C} + D + D\,(B + X) + \underline{B}\,\underline{X} + K23)$$

$$= A\,\underline{B}\,\underline{D}\,(\underline{C}\,(B + X) + \underline{B}\,\underline{X} + K23)$$

$$= \underline{2} \,.\, \underline{3} \,.\, \underline{B} \,.\, \underline{D}\,(7 + 4 + K23) \quad \ldots\ldots (35)$$

(see circuit 9(d)).

$$K45 = A\,C\,\underline{D}\,(\underline{B} + X + K34) = A\,C\,\underline{D}\,(D + \underline{B}\,\underline{X} + \underline{A}\,C\,(\underline{B} + X) + A\,\underline{C}\,X + X + K34)$$

$$= A\,C\,\underline{D}\,(\underline{B}\,\underline{X} + X + K34)$$

$$= \underline{2} \cdot \underline{3} \cdot \underline{7} \cdot \underline{8} \cdot \underline{9} \cdot \underline{D} \quad (4 + X + K34) \quad \ldots\ldots (36)$$

(See circuit 9(e)).

$$K56 = B\,C\,\underline{D}\,(A + \underline{X} + K45) = B\,C\,\underline{D}\,(A + B\,\underline{X} + K45)$$

$$= \underline{4} \cdot \underline{5} \cdot \underline{6} \cdot \underline{D} \cdot \underline{7} \cdot \underline{8} \cdot \underline{9} \cdot \underline{D} \cdot (A + B\,\underline{X} + K45)$$

$$= \underline{4} \cdot \underline{5} \cdot \underline{6} \cdot \underline{7} \cdot \underline{8} \cdot \underline{9} \cdot \underline{D} \cdot (A + 1 + K45) \quad \ldots\ldots (37)$$

(See circuit 9(f)).

$$K67 = \underline{A}\,C\,\underline{D}\,(B + X + K56) = \underline{A} \cdot \underline{7} \cdot \underline{8} \cdot \underline{9} \cdot \underline{D}\,(B + X + K56) \quad \ldots\ldots (38)$$

(See circuit 9(g)).

$$K78 = \underline{A}\,\underline{B}\,C\,(\underline{D} + \underline{X} + K67) = \underline{A}\,\underline{B}\,C\,(A + B + \underline{C}\,\underline{X} + \underline{D}\,(B + X) + \underline{B}\,\underline{X} + K67).$$

$$= \underline{A}\,\underline{B}\,C\,(\underline{D}\,(B + X) + \underline{B}\,\underline{X} + K67)$$

$$= \underline{A} \cdot \underline{B} \cdot \underline{7} \cdot \underline{8} \cdot \underline{9}\,(11 + 4 + K67) \quad \ldots\ldots (39)$$

(See Circuit 9(h)).

$$K89 = \underline{A}\,\underline{B}\,D\,(C + X + K78)$$

$$= \underline{A} \cdot \underline{B} \cdot \underline{A} \cdot \underline{B} \cdot \underline{10} \cdot \underline{11} \cdot (C + X + K78) \quad \ldots\ldots (40)$$

$$= \underline{A} \cdot \underline{B} \cdot \underline{10} \cdot \underline{11}\,(C + X + K78)$$

(See Circuit 9(i)).

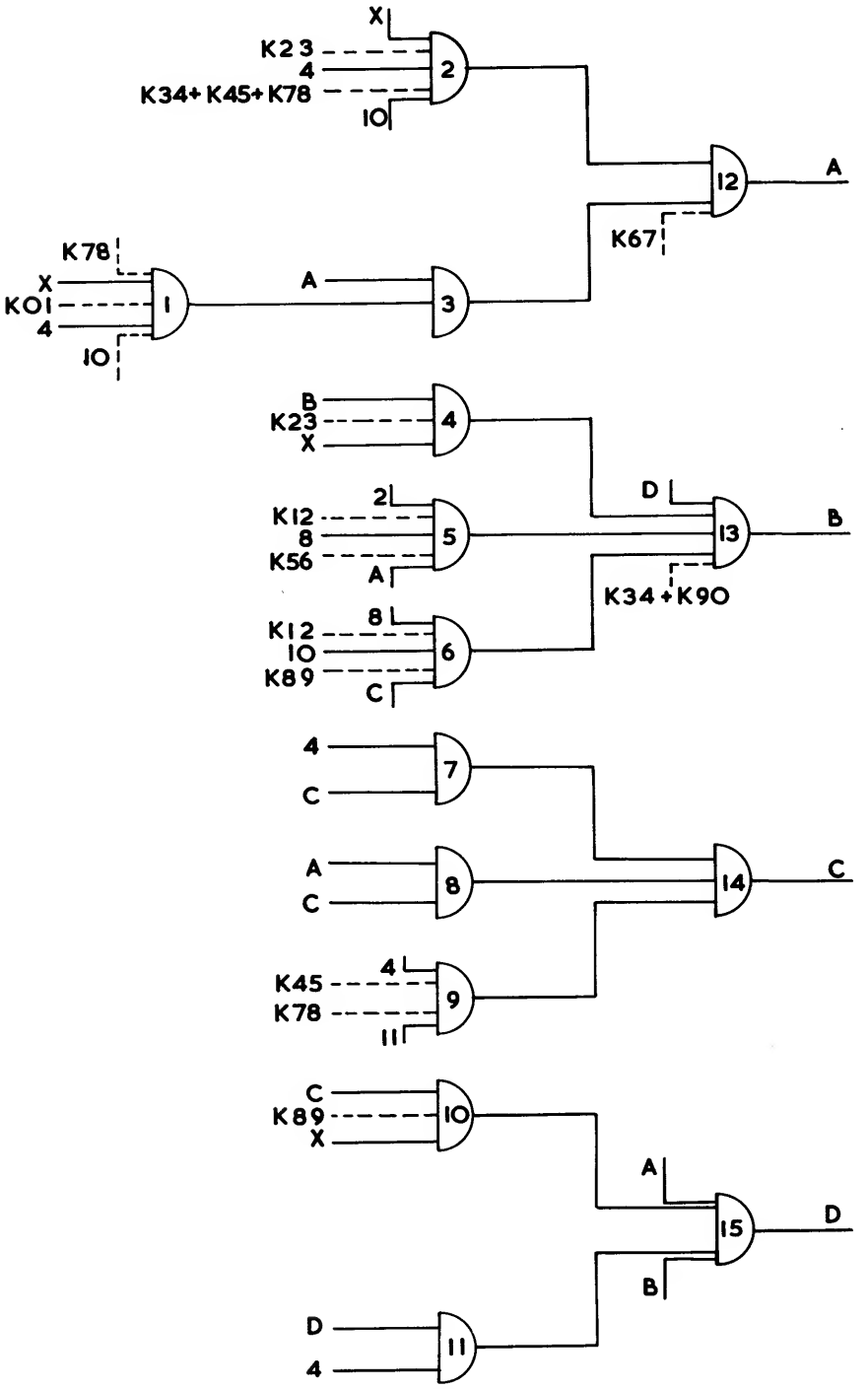
$$K90 = \underline{A}\,\underline{B}\,\underline{C}\,(D + \underline{X} + K89)$$

$$= \underline{A}\,\underline{B}\,\underline{C}\,(D + \underline{C}\,\underline{X} + K89) \quad \ldots\ldots (41)$$

(See circuit 9(j)).

NOTE:

The probability of a race-hazard being revealed may be further reduced by introducing all the possible substitution signals for $\underline{X}$ inside the bracket. For example, if in the last equation $\underline{B}\,\underline{X}$ as well as $\underline{C}\,\underline{X}$ were substituted for $\underline{X}$, then, in the S9 - S0 circuit transition the race would be between secondary signal $\overline{D}$ changing from 1 to 0 and product signals $\underline{B}\,\underline{X}$ and $\underline{C}\,\underline{X}$ both changing from 0 to 1.

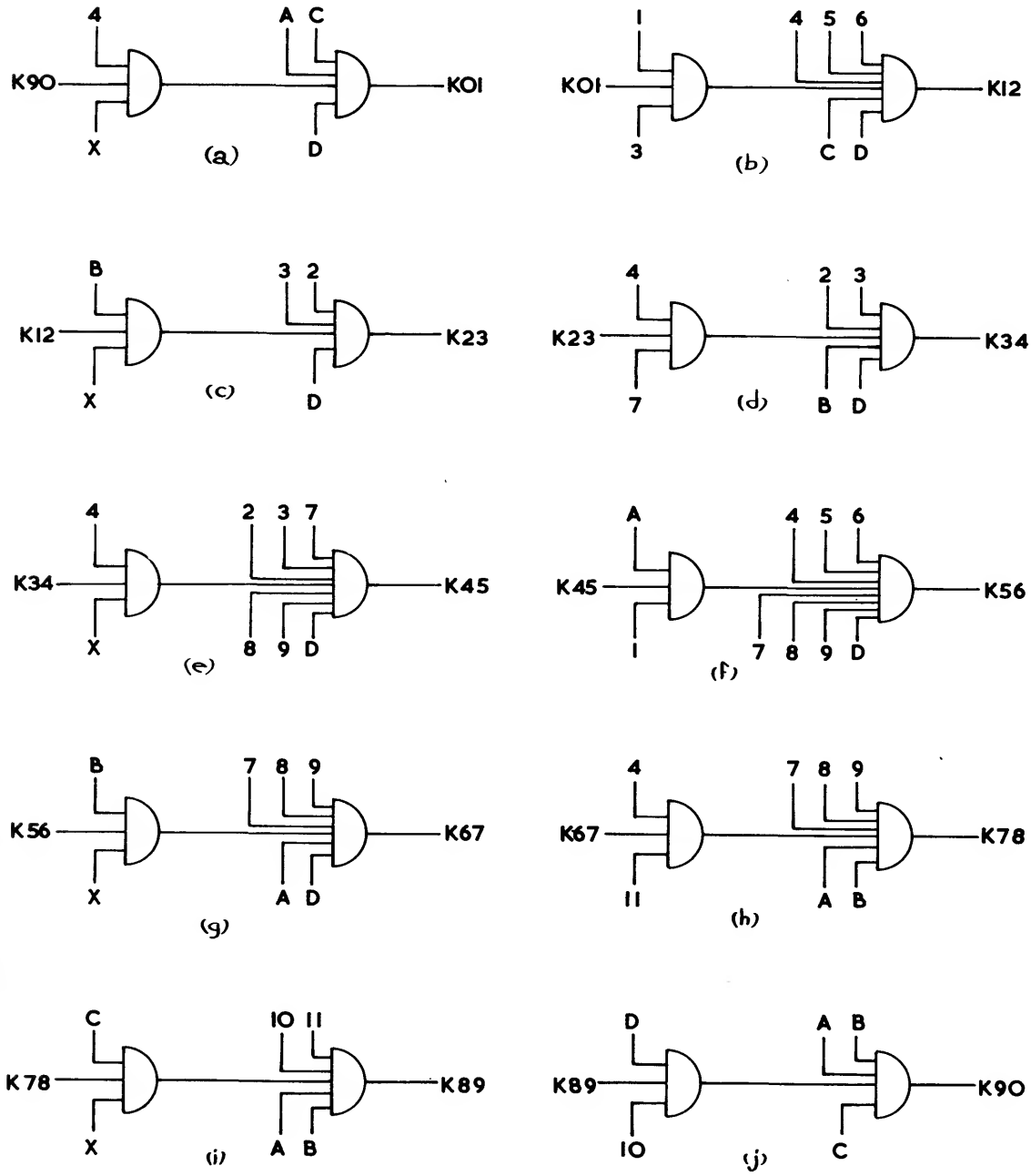


CIRCUIT 8. MINIMAL FIVE-WAY COUNTER WITH CORRECTING SIGNALS

NOTE - THE NUMBER AT THE INPUT OF A MODULE INDICATES THE ORIGIN OF THE INPUT SIGNAL - E.G. OUTPUT OF MODULE 4 IS CONNECTED TO THE INPUT OF MODULE 2.

CIRCUIT STATES	PRIMARY SIGNAL	OUTPUT OF MODULE															CLASSIFICATION OF THE RACE-HAZARD
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	X	$B\underline{X}$	$BC\underline{X}$	$A[B+X]$	$\underline{B}\underline{X}$	$\underline{A}C[B+X]$	$A\underline{C}X$	$\underline{C}[B+X]$	$\underline{A}\underline{C}$	$D[B+X]$	$\underline{C}\underline{X}$	$\underline{D}[B+X]$	A	B	C	D	
S0	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	
		RH1	RH2							RH3						RH4	RH1/RH4 CRITICAL RH2/RH3 NON-CRITICAL
S1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	
			RH5			RH6	RH7										RH5 NON-CRITICAL RH6/RH7 CRITICAL
S2	0	1	0	0	0	0	0	1	0	0	1	1	1	1	0	0	
			RH8		RH9												RH8/RH9 CRITICAL
S3	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	
		RH10	RH11							RH12	RH13			RH14			RH10/RH12/RH13 NON-CRIT. RH11/RH14 CRITICAL .
S4	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	
		RH15	RH16							RH17							RH15 NON-CRITICAL RH16 / RH17 CRITICAL
S5	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	
				RH18		RH19											RH18 NON-CRITICAL RH19 CRITICAL
S6	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	0	
					RH20								RH21				RH20 NON-CRITICAL RH21 CRITICAL
S7	1	0	0	1	0	1	0	0	0	0	0	1	0	0	1	0	
		RH22	RH23							RH24							RH22/23/24 CRITICAL
S8	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	
		RH25					RH26				RH27						RH25/RH27 CRITICAL RH26 NON-CRITICAL
S9	1	0	0	1	0	0	0	1	1	1	0	0	0	0	0	1	
		RH28	RH29									RH30		RH31			RH28/RH31 CRITICAL RH29/RH30 NON-CRIT.
S0	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	

TABLE 4. TRANSITION TABLE OF CIRCUIT 8



CIRCUIT 9. CORRECTING CIRCUITS FOR THE MINIMAL FIVE-WAY COUNTER OF CIRCUIT 8

Appendix

CRITICALLITY OF RACE-HAZARDS.

A race-hazard appearing at the output of a secondary-signal module during a circuit transition in which the module output itself changes is non-critical, otherwise it is critical, so far as the circuit operation is concerned.

PROBABILITY OF RACE-HAZARDS.

A signal-race at the input of a (NOR) module will only reveal itself in the form of a race-hazard at the output of the module if the time taken for one of the signals to change from the logical 0 level is greater than the time taken for the other signal to change from the 1 logical level to the 0 logical level, otherwise there will be no race-hazard at the output. This switch-on to switch-off time ratio is defined as the race-hazard probability and is symbolised by P.

The condition for a race-hazard to appear therefore can be expressed in the form:

$$P = \frac{\text{time taken for the 0 to 1 signal change}}{\text{time taken for the 1 to 0 signal change}}$$

when P is greater than 1, a race-hazard will reveal itself
when P is less than or equal to 1, a race-hazard will not reveal itself.

EXAMPLE.

Table 1 is the transition table of the two-way counter shown in circuit 2. The race-hazards present at all points of the circuit are shown on the table. The following symbolic notation is used:

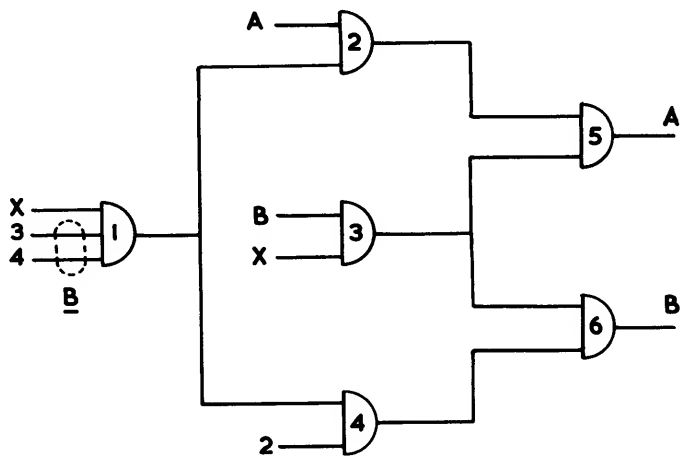
RHmkl.....specifies the race-hazard (RH) that may be revealing itself at the output of module 'm' during the circuit transition from state 'k' to state 'l'.

tmn.....refers to the propagation time of module 'n', and
tlxy.....is used to express symbolically the delay introduced by the lead connecting module 'x' to module 'y'.

Using this notation, the probability of each race-hazard is now expressed algebraically in the right-hand column of table 1.

CIRCUIT STATES	INPUT SIGNAL X	MOD 1 $B\underline{X}$	MOD 2 $A[\underline{B}+X]$	MOD 3 $\underline{B}\underline{X}$	MOD 4 $A[\underline{B}+X]$	MOD 5 A	MOD 6 B	RACE-HAZARD CRITICALITY.	RACE-HAZARD PROBABILITY
SO	0	0	1	1	0	0	0		
SO1	1	RH101						CRITICAL	$P_{101} = \frac{tlX1}{tlX3+tm3+tl31}$
S1	1	0	1	0	0	0	1		
S12	0				RH412			CRITICAL	$P_{412} = \frac{tlX1+tm1+tl14}{tlX1+tm1+tl12+tm2+tl24}$
S2	0	1	0	0	0	1	1		
S23	1			RH323				CRITICAL	$P_{323} = \frac{tlX3}{tlX1+tm1+tl14+tm4+tl46+tm6}$
S3	1	0	0	0	1	1	0		
S30	0	RH130					RH630	RH130 NON-CRIT. RH630 CRITICAL	$P_{630} = \frac{tlX3+tm3+tl36}{tlX1+tm1+tl12+tm2+tm24+tm4+tl46}$
SO	0	0	1	1	0	0	0		

TABLE 1. TRANSITION TABLE OF TWO-WAY COUNTER SHOWN IN CIRCUIT 3.



CIRCUIT 2. TWO-WAY COUNTER USING NOR/NAND MODULES.

ELIMINATION OF RACE-HAZARDS.

Race-hazards in combinational circuits can always be eliminated by the introduction of a D.C. correcting (blanking) signal.

For example, the race-hazard present in circuit 1 realising directly the switching function $A B + \underline{A} C$ was eliminated by the addition of the correcting signal B C. The derivation of the correcting signals in combinational circuits is based on the Boolean theorem.

$$A B + \underline{A} C = A B + \underline{A} C + B C$$

In sequential circuits the complete elimination of race-hazards is not always possible, because the correcting signal itself may be subject to a signal-race. However, the introduction of such correcting signals greatly reduces the probability factor of race-hazards, as shown below.

The correcting signal Kmn needed to blank out a race-hazard that appears during the Sm to Sn (or vice versa) transition can be expressed algebraically by the following general equation:

$$Kmn + Sm + Smn + Sn$$

Correcting signal Kmn is applied directly to the input of the module which is subject to the race-hazard in question.

EXAMPLE.

Assume that it is required to blank out race-hazard RH101 in circuit 2. Substituting in the above general equation, we get:

$$\begin{aligned} K01 &= S0 + S01 + S1 \\ &= \underline{A}\,\underline{B}\,\underline{X} + \underline{A}\,\underline{B}\,X + \underline{A}\,B\,X \\ &= \overline{A}\,\overline{B} + \underline{A}\,\overline{X} \\ &= \overline{\underline{A}}\,(\overline{\underline{B}} + \overline{X}) \end{aligned}$$

Circuit 3 shows its NOR circuit realisation.

The probability factor of the correcting signal, K01, referred to module 1 is:

$$P\ 101 = \frac{tlx7 + tm7 + tl78 + tm8 + tl81}{tlx3 + tm3 + tl37 + tm7 + tl78 + tm8 + tl81}$$

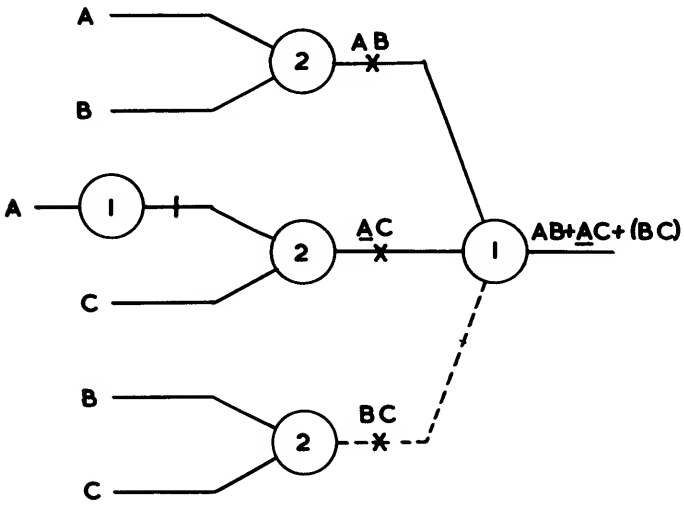
and the probability factor of the race-hazard RH101 referred to the same module as derived in the previous section is:

$$P101 = \frac{tlx1}{tlx3 + tm3 + tl31}$$

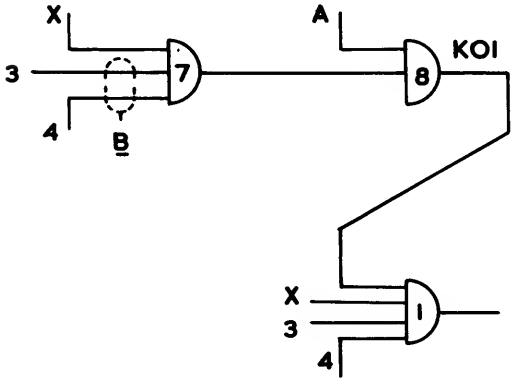
THE CONDITION FOR THE RACE-HAZARD RH101 TO REVEAL ITSELF IN ADDITION TO THE ABOVE TWO EXPRESSIONS BEING GREATER THAN 1, THE FOLLOWING TWO INEQUALITIES MUST ALSO BE SATISFIED SIMULTANEOUSLY:

$$\frac{tlx1}{tlx3 + tm3 + tl37 + tm7 + tl78 + tm8 + tl81} \quad \text{is greater than 1.}$$

$$\frac{tlx7 + tm7 + tl78 + tm8 + tl81}{tlx3 + tm3 + tl31} \quad \text{is greater than 1.}$$



CIRCUIT 1.



CIRCUIT 3. CORRECTING CIRCUIT FOR RACE-HAZARD RH 101.

CONCLUSION.

Race-hazards are probably the biggest single cause of failures of digital control and computer circuits. The reason for this is the fact that although a signal-race may reveal itself in the form of a race-hazard in some circuits, it may not show itself in other identical circuits due to production spreads in the time delays of the switching modules. Therefore the detection of race-hazards is an essential step in the testing of circuits.

The advantages of the suggested type of correcting circuits compared to the conventional method of introducing in the 'fast' signal paths are:

1. The correcting circuits are additive- that is, they need only be introduced in circuits in which the race-hazard probability factor is greater than 1, since other identical circuit configurations may have probability factors less than 1 depending on the tolerance of the switching modules, and their corresponding lead delays.

2. A delay introduced directly in a 'fast' signal path to delay the '0' to '1' signal change, will also delay the '1' to '0' signal change in the same path, thus probably introducing a race-hazard in another circuit transition.

3. Any degree of reduction in the race-hazard probability may be achieved.

Finally, it is generally accepted that this step-by-step approach to the race-hazard phenomenon gives a clear picture to both the designing and testing engineer of what is going on in the circuit.

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About this book

The investigation of Race and Hazard phenomena in Switching Circuits has attracted considerable interest in recent years. This is possibly because a switching circuit may be tested and found to operate satisfactorily but an identical circuit using a different set of the same switching elements may fail to operate. The cause of this is race hazards, in the form of narrow electrical pulses, which are present in the second case.

The aim of this manual is to explain the nature of these phenomena, how to detect their possible presence in circuits, and to suggest simple but effective means of eliminating them, using step by step techniques at an early stage of the design, that is before the actual circuit is realised.

Also, step by step design techniques for NOR and NAND switching circuits are introduced. The main difficulty so far has been that a minimal algebraic expression when realised directly does not result in a minimal circuit, as is the case with AND/OR and OR/AND logic. In NOR and NAND logic the switching function must first be optimised.

A chapter on Boolean Algebra has been included for completeness. A set of simple rules for minimising algebraic expressions is given, as well as a list of worked examples and a set of examples with answers.

The techniques described are used to design practical switching circuits.

One of the most useful features of the book is the reference list of switching circuits.

The book has been developed from courses given at the Liverpool College of Technology by the authors. Its main appeal is to design electronic engineers in communication, computer, data processing and control activities.

Pitman

LOGICAL DESIGN MANUAL

Zissos and Copperwhite