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MICROELECTRONIC CIRCUITS

Adel S. Sedra

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Kenneth C. Smith

University of Toronto

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PREFACE

Microelectronics Circuits, fifth edition, is intended as a text for the core courses in electronic circuits taught as majors in electrical and computer engineering. It should also prove useful to engineers and other professionals wishing to update their knowledge through self-study.

As was the case with the first four editions, the objective of this book is to develop in the reader the ability to analyze and design electronic circuits, both analog and digital, discrete and integrated. While the application of integrated circuits is covered, emphasis is placed on transistor circuit design. This is done because of our belief that even if the majority of those studying the book were not to pursue a career in IC design, knowledge of what is inside the IC package would enable intelligent and innovative application of such chips. Furthermore, with the advances in VLSI technology and design methodology, IC design itself is becoming accessible to an increasing number of engineers.

PREREQUISITES

The prerequisite for studying the material in this book is a first course in circuit analysis. As a review, some important material is included here in appendices; specifically, two-port network parameters in Appendix B; source extraction theorems in Appendix C; single-domain constant circuits in Appendix D; and a domain analysis in Appendix E. No prior knowledge of physical electronics is assumed. All required device physics is included, and Appendix A provides a brief description of IC fabrication.

NEW TO THIS EDITION

Although the philosophy and pedagogical approach of the first four editions have been retained, several changes have been made to both organization and coverage.

1. The book has been reorganized into three parts. Part I: Devices and Basic Circuits, composed of the first five chapters, provides a coherent and reasonably comprehensive single semester introductory course in electronics. Similarly, Part II: Analog and Digital Integrated Circuits (Chapters 6–10) presents a body of material suitable for a second one-semester course. Finally, four carefully chosen subjects are included in Part III: Selected Topics. These can be used as enhancements or substitutions for some of the material in earlier chapters, as resources for projects or thesis work, and/or as part of a third course.
2. Each chapter is organized so that the essential “must-cover” topics are placed first, and the more specialized material appears last. This allows considerable flexibility in teaching and learning from the book.
3. Chapter 4, MOSFETs, and Chapter 5, BJT's, have been completely rewritten, updated, and made completely independent of each other. The MOSFET chapter is placed first to reflect the fact that it is currently the most significant electronics device by a wide margin. However, if desired, the BJT can be covered first. Also, the identical structure of the two chapters makes teaching and learning the second device easier and faster.

4. To make the book course competitive, both Chapters 4 and 5 include material on amplifiers and digital logic circuits. In addition, the frequency response of the basic common source (common emitter) amplifier is included. This is important for students who might not take a second course in electronics.
5. A new chapter on integrated circuit (IC) amplifiers (Chapter 6) is added. It begins with a comprehensive comparison between the MOSFET and the BJT. Typical parameter values of devices produced by modern submicron fabrication processes are given and utilized in the examples, exercises, and end-of-chapter problems. The study of each amplifier configuration includes its frequency response. This should make the study of amplifier frequency response more interesting and somewhat easier.
6. The material on differential and multivoltage amplifiers in Chapter 7 has been rewritten to present the MOSFET differential pair first. Here also, the examples, exercises, and problems have been expanded and updated to utilize parameter values representative of modern submicron technologies.
7. Throughout the book, greater emphasis is placed on MOSFET circuits.
8. To make room for new material, some of the topics that have become less or non-existent, such as JFETs and TTL, or have remained highly specialized, such as GaAs devices and circuits, have been removed from the book. However, they are made available on the CD accompanying the book and on the book's website.
9. As a study aid and for easy reference, many summary tables have been added.
10. The review exercises, examples, and end-of-chapter problems have been updated and their numbers and variety increased.
11. The SPICE sections have been rewritten and the SPICE examples now utilize selectable entry. To enable further experimentation, the files for all SPICE examples are provided on the CD and website.

THE CD-ROM AND THE WEBSITE

A CD-ROM accompanies this book. It contains much useful supplementary information and material, intended to enrich the student's learning experience. These include: (1) A Student's Edition of OrCAD PSpice 9.2, (2) The input files for all the SPICE examples in the book, (3) A link to the book's website accessing PowerPoint slides of every figure in this book that students can print and carry over as a valuable learning notes, (4) Bonus test material of specialized topics not covered in the current edition of the textbook. These include: JFETs, GaAs devices and circuits, and TTL circuits.

A website for the book has been set up (www.electronicsbook.org). Its content will change frequently to reflect new developments in the field. It features SPICE models and files for all PSpice examples, links to industrial and academic websites of interest, and a message center to communicate with the authors. There is also a link to the Higher Education Group of OUP (Oxford University Press) so professors can receive complete text support.

EMPHASIS ON DESIGN

It has been my philosophy that circuit design is best taught by pointing out the various trade-offs available in selecting a circuit configuration, and in selecting component values for a given configuration. The emphasis on design has been increased in this edition by including more design examples, exercise problems, and end-of-chapter problems. Those exercises and

end-of-chapter problems that are considered "design oriented" are indicated with a D. Also, the most valuable design aid, SPICE, is utilized throughout the book, as already outlined.

EXERCISES, END-OF-CHAPTER PROBLEMS, AND ADDITIONAL SOLVED PROBLEMS

Over 450 exercises are integrated throughout the text. The answer to each exercise is given below the exercise so students can check their understanding of the material as they read. Solving these exercises should enable the reader to gauge his or her grasp of the preceding material. In addition, more than 1300 end-of-chapter problems, about a third of which are new to this edition, are provided. The problems are keyed to the individual sections and their degree of difficulty is indicated by a rating system: difficult problems are marked with a asterisk (*), more difficult problems with two asterisks (**), and very difficult (and time consuming) problems with three asterisks (***) . We must admit, however, that this classification is by no means exact. Our rating is individual and dependent to some degree on your thinking and recall at the time a particular problem was created. Answers to about half the problems are given in Appendix H. Complete solutions for all exercises and problems are included in the *Instructor's Manual*, which is available from the publisher for those institutions who adopt the book.

As in the previous four editions, many examples are included. The examples, and indeed most of the problems and exercises, are based on real circuits and anticipate the applications encountered in designing real-life circuits. This edition continues the use of numbered solution steps in the figures for many examples, as an attempt to increase the dynamics of the classroom.

A recurring request from many of the students who used earlier editions of the book has been for solved problems. To satisfy this need, a book of additional problems with solutions is available with this edition (see the list of available ancillaries later in this preface).

AN OUTLINE FOR THE READER

The book starts with an introduction to the basic concepts of electronics in Chapter 1. Signals, their frequency spectra, and their analog and digital forms are presented. Amplifiers are introduced as circuit building blocks and their various types and models are studied. The basic concept of digital electronics, the digital logic inverter, is defined in terms of its voltage transfer characteristic, and its various implementations using voltage and current switches are discussed. This chapter also establishes some of the terminology and conventions used throughout the text.

The next four chapters are devoted to the study of electronic devices and basic circuits and constitute the bulk of Part I of the text. Chapter 2 deals with operational amplifiers, their technical characteristics, simple applications, and limitations. We have chosen to discuss the op-amp as a circuit building block at this early stage simply because it is easy to deal with and because the student can experiment with op-amp circuits that perform non-trivial tasks with relative ease and with a sense of accomplishment. We have found this approach to be highly motivating to the student. We should point out, however, that part of all of this chapter can be skipped and studied at a later stage (for instance in conjunction with Chapter 7, Chapter 8, and/or Chapter 9) with no loss of continuity.

Chapter 3 is devoted to the study of the most fundamental electronic device, the pn junction diode. The diode terminal characteristics and its inventory of models and basic circuit

applications are presented. To understand the physical operation of the diode, and indeed of the MOSFET and the IGBT, a concise but substantial introduction to semiconductors and the $p-n$ junction is provided. This material is placed near the end of the chapter (Section 3.7) so that part or all of it can be skipped by those who have already had a course in physical electronics.

Chapters 4 and 5 deal with the two major electronic devices—the MOS field-effect transistor (MOSFET) and the bipolar junction transistor (BJT), respectively. These two chapters have an identical structure and are completely independent of each other and thus can be covered in either order. Each chapter begins with a study of the device structure and its physical operation, leading to a description of its technical characteristics. Then, to establish in the reader a high degree of familiarity with the operation of the transistor as a logic element, a large number of examples are presented of dc circuits utilizing the device. The large-signal operation of the basic common-source (common-emitter) circuit is then studied and used to delineate the region over which the device can be used as a linear amplifier (in these regions where it can be used as a switch). This makes clear the need for biasing the transistor and leads naturally to the study of biasing methods. At this point, the biasing methods used are mostly for discrete circuits, leaving the study of IC biasing to Chapter 6. Next, small-signal operation is studied and small-signal models are derived. This is followed by a study of the basic configurations of discrete circuit amplifiers. The internal capacitive effects that limit the high-frequency operation of the transistor are then studied, and the high-frequency equivalent circuit model is presented. This model is then used to determine the high-frequency response of a common-source (common-emitter) amplifier. As well, the low-frequency response resulting from the use of coupling and bypass capacitors is also presented. The basic digital logic inverter circuit is then studied. Both chapters conclude with a study of the transistor models used in SPICE, together with circuit-simulation examples using PSpice. This description should indicate that Chapters 4 and 5 contain the essential material for a first course in electronics.

Part II: Analog and Digital Integrated Circuits (Chapters 6–10) begins with a comprehensive compilation and comparison of the properties of the MOSFET and the IGBT. The comparison is facilitated by the provision of typical parameter values of devices fabricated with modern process technologies. Following a study of biasing methods employed in IC amplifier design (Section 6.3), and some basic background material for the analysis of high-frequency amplifier response (Section 6.4), the various configurations of single-stage IC amplifiers are presented in a systematic manner. In each case, the MOS circuit is presented first. Some transistor-pair configurations that are usually treated in a single stage, such as the cascode and the Darlington circuit, are also specified. Each section includes a study of the high-frequency response of the particular amplifier configuration. Again, we believe that this “in-depth” study of frequency response is superior to the traditional approach of postponing all coverage of frequency response to a later chapter. As in other chapters, the more specialized material, including advanced current mirror and current source concepts, is placed in the second half of the chapter, allowing the reader to skip some of this material in a first reading. This chapter should provide an excellent preparation for an in-depth study of analog IC design.

The study of IC amplifiers is continued in Chapter 7 where the emphasis is on two major topics: differential amplifiers and multistage amplifiers. Here again, the MOSFET differential pair is treated first. Also, frequency response is discussed where needed, including in the two examples of multistage amplifiers.

Chapter 8 deals with the important topic of feedback. Practical circuit applications of negative feedback are presented. We also discuss the stability problem in feedback amplifiers and low-frequency compensation in some detail.

Chapter 9 integrates the material on analog IC design presented in the preceding three chapters and applies it to the analysis and design of two major analog IC functional blocks: op amps and data converters. Both CMOS and bipolar op amps are studied. The data converter sections provide a bridge to the study of digital CMOS logic circuits in Chapter 10.

Chapter 10 builds on the introduction to CMOS logic circuits in Section 4.10 and includes a carefully selected set of topics on static and dynamic CMOS logic circuits that round out the study of analog and digital ICs in Part II.

The study of digital circuits is contained in the last two of the four selected-topics chapters that comprise Part III. Specifically, Chapter 11 deals with memory and related circuits, such as latches, flip-flops, and translatable and sizable multipliers. As well, two somewhat specialized but significant digital circuit technologies are studied: charge-coupled logic (CCIL) and BiCMOS. The ten digital chapters (10 and 11) together with the earlier material on digital ICs should prepare the reader well for a subsequent course on digital IC design or VLSI circuits.

The next two chapters of Part III, Chapters 12 and 13, are application or system oriented. Chapter 12 is devoted to the study of analog filter design and tuned amplifiers. Chapter 13 presents a study of sinusoidal oscillators, wave-form generators, and other nonlinear signal-processing circuits.

The last chapter of the book, Chapter 14, deals with various types of amplifier output stages. Thermal design is studied, and examples of IC power amplifiers are presented.

The eight appendices contain much useful background and supplementary material. We wish to draw the reader's attention in particular to Appendix A, which provides a concise introduction to the important topic of IC fabrication technology including IC layout.

COURSE ORGANIZATION

The book contains sufficient material for a sequence of two single-semester courses (each of 40 to 50 lecture hours). The organization of the book provides considerable flexibility in course design. In the following, we suggest various possibilities for the two courses.

The First Course

The most obvious package for the first course consists of Chapters 1 through 5. However, if time is limited, some or all of the following sections can be postponed to the second course: 1.6, 1.7, 2.6, 2.7, 2.8, 3.6, 3.8, 4.8, 4.9, 4.10, 4.11, 5.8, 5.9, and 5.10. It is also quite possible to omit Chapter 2 altogether from this course. Also, it is possible to concentrate on the MOSFET (Chapter 4) and cover the BJT (Chapter 5) only partially and/or more quickly. Covering Chapter 5 thoroughly and Chapter 4 only partially and/or more quickly is also possible—but not recommended! An entirely analog first course is also possible by omitting Sections 1.7, 4.10, and 5.10. A digitally oriented first course is also possible. It would consist of the following sections: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.1–3.2, 3.3, 3.4, 3.7, 4.1, 4.2, 4.3, 4.4, 4.10, 4.12, 5.1, 5.2, 5.3, 5.4, 5.10, 5.11, all of Chapter 10, and selected topics from Chapter 11. Also, if time permits, some material from Chapter 2 on op amps would be beneficial.

The Second Course

An excellent place to begin the second course is Chapter 6 where Section 6.2 can serve as a review of the MOSFET and BJT characteristics. Indeed, the second course would cover

Chapters 5 through 10 assuming, of course, that the first course covered Chapters 1 through 4. If time is short, either Chapter 10 can be dropped or a subsequent course on digital circuits and/or some sections of Chapters 4–9 can be omitted. One possibility would be to de-emphasize bipolar circuits by omitting some or all of the bipolar sections in Chapters 6, 7, and 9. Another would be to reduce somewhat the coverage of feedback (Chapter 8). Also, data converters can be easily deleted from the second course. Still, for Chapter 9, perhaps only CMOS op amps need to be covered and the 741 deleted or incorporated. It is also possible to replace some of the material from Chapters 6–10 by selected topics from Chapters 11–14. For instance, in an entirely analog second course, Chapter 10 can be replaced by a selection of topics from Chapters 11–14.

ANCILLARIES

A complete set of ancillary materials is available with this text to support your course.

For the Instructor

The *Instructor's Manual with Transparency Masters* provides complete worked solutions to all the exercises in each chapter and all the end-of-chapter problems in the text. It also contains 200 transparency masters that duplicate the figures in the text most often used in class.

A set of Transparency Masters of the 200 most important figures in the book.

A *PowerPoint CD* with slides of every figure in the book and each corresponding caption.

For the Student and the Instructor

The CD-ROM included with every new copy of the textbook contains SPICE input files, a Student Edition of OrCAD PSpice 9.2 Line Edition, a link to the website featuring PowerPoint slides of the book's illustrations, and bonus topics.

Laboratory Experiments for Microelectronic Circuits, 5th edition, by Kenneth C. Smith (KCU), contains laboratory experiments and instructions for the major topics studied in the text. *KCU's Problems and Solutions for Microelectronic Circuits, 5th edition*, by Kenneth C. Smith (KCU), contains hundreds of additional study problems with complete solutions for students who want more practice.

SPICE, 2nd edition, by Gordon Roberts of McGill University and Aneel Sohra, provides a detailed treatment of SPICE and its application in the analysis and design of circuits of the type studied in this book.

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Many of the changes in this fifth edition were made in response to feedback received from some of the instructors who adopted the fourth edition. We are grateful to all those who took the time to write to us. In addition, the following reviewers provided detailed commentary on the fourth edition and suggested many of the changes that we have incorporated in this revision. To all of them, we extend our sincere thanks: Maurice Aburame, Bucknell University; Patrick J. Chapman, University of Illinois at Urbana-Champaign; Alice Davis, San Jose State University; Paul M. Fisher, New Mexico State University; Renuk Chariabegi, St. John's

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Abel S. Sedra
Kenneth C. Smith

MICROELECTRONIC CIRCUITS



DEVICES AND BASIC CIRCUITS

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INTRODUCTION

Part I, *Devices and Basic Circuits*, introduces the most fundamental and essential devices for the study of electronic circuits. At the same time, it constitutes a complete package for a first course on the subject.

Besides silicon diodes and transistors, the basic electronic devices, the op-amp is studied in Part I. Although not an electronic device in the most fundamental sense, the op-amp is commercially available as an integrated circuit (IC) package and has well-defined terminal characteristics. Thus, despite the fact that the op-amp's internal circuitry is complex, typical linear instrumentation (20 or more transistors) its almost ideal behavioral behavior makes it possible to treat the op-amp as a circuit element and to use it in the design of power electronics, as we do in Chapter 2, without any knowledge of its internal construction. We should caution, however, that the study of op-amps can be delayed to a later point, and Chapter 2 can be skipped with no loss of continuity.

The most basic silicon device is the diode. In addition to learning about diodes and a sample of their applications, Chapter 3 also introduces the general topic of device modeling for the purpose of circuit analysis and design. As in Section 3.7 provides a substantial introduction to the physical operation of semiconductor devices. This subject is then continued in Section 4.1 for the MOSFET and in Section 5.1 for the BJT. Taken together, these three sections provide a physical background sufficient for the study of electronic circuits at the level presented in this book.

The heart of this book, and of any electronics course, is the study of the two transistor types in use today: the MOS field-effect transistor (MOSFET) in Chapter 4 and the bipolar junction transistor (BJT) in Chapter 5. These two chapters have been written to be completely independent of one another and thus can be studied in either desired order. Furthermore, the two chapters have the same structure, making it easier and faster to study the second device, as well as to draw comparisons between the two device types.

Chapter 1 provides both an introduction to the study of electronics and a number of important concepts for the study of amplification (Sections 1.1–1.6) and of digital circuits (Section 1.7).

Each of the five chapters concludes with a section on the use of SPICE, which is used in circuit analysis and design. Of particular importance here are the device models employed by SPICE. Finally, note that, as in most of the chapters of this book, the *background material* is placed near the beginning of a chapter while the *good-to-know topics* are placed in the latter part of the chapter. Some of this latter material, therefore, is skipped in a first course and covered at a later time, when needed.

CHAPTER 1

Introduction to Electronics

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INTRODUCTION

The subject of this book is modern electronics, a field that has come to be known as **microelectronics**. Microelectronics refers to the integrated-circuit (IC) technology that at the time of this writing is capable of producing circuits that contain millions of components in a small piece of silicon (known as a **silicon chip**) whose area is on the order of 100 mm^2 . One such microelectronic circuit, for example, is a complete digital computer, which accordingly is known as a **microcomputer** or, more generally, a **microprocessor**.

In this book we shall study electronic devices that can be used singly in the design of discrete circuits, or as components of an integrated-circuit (IC) chip. We shall study the design and analysis of interconnections of these devices, which form discrete and integrated circuits of varying complexity and perform a wide variety of functions. We shall also learn about available IC chips and their application in the design of electronic systems.

The purpose of this first chapter is to introduce some basic concepts and terminology. In particular, we shall learn about signals and about one of the most important signal processing techniques: electronic circuits are designed to perform, namely, signal amplification. We shall then focus at models for linear amplifiers. These models will be employed in subsequent chapters in the design and analysis of actual amplifying circuits.

Whereas the amplifier is the basic element of analog circuits, the logic inverter plays this role in digital circuits. We shall therefore take a preliminary look at the digital inverter, its circuit function, and important characteristics.

In addition to motivating the study of electronics, this chapter serves as a bridge between the study of linear circuits and that of the subject of this book: the design and analysis of electronic circuits.

1.1 SIGNALS

Sigⁿals contain information about a variety of things and activities in our physical world. Examples abound. Information about the weather is contained in signals that represent the air temperature, pressure, wind speed, etc. The voice of a radio announcer reading the news into a microphone provides us with the signal that contains information about world affairs. On board the atoms of a nuclear reactor, instruments are used to measure a multitude of relevant parameters, each instrument producing a signal.

To extract required information from a set of signals, the observer (be it a human or a machine) invariably needs to process the signals in some predetermined manner. This signal processing is usually most conveniently performed by electronic systems. For this to be possible, however, the signal must first be converted into an electric signal, that is, a voltage or a current. This process is accomplished by devices known as transducers. A variety of transducers exist, each suitable for one of the various forms of physical signals. For instance, the sound waves generated by a human can be converted into electric signals using a microphone, which is in effect a pressure transducer. It is not our purpose here to study transducers; rather, we shall assume that the signals of interest already exist in the electrical domain and represent them by one of the two equivalent forms shown in Fig. 1.1. In Fig. 1.1(a) the signal is represented by a voltage source $v_s(t)$ having a source resistance R_s . In the alternate representation of Fig. 1.1(b) the signal is represented by a current source $i_s(t)$ having a source resistance R_s . Although the two representations are equivalent, that in Fig. 1.1(a) (known as the Thévenin form) is preferred when R_s is low. The representation of Fig. 1.1(b) (known as the Norton form) is preferred when R_s is high. The reader will come to appreciate this point later in this chapter when we study the different types of amplifiers. For the time being, it is important to be familiar with Thévenin's and Norton's theorems (for a brief review, see Appendix D) and to note that for the two representations in Fig. 1.1 to be equivalent, their parameters are related by

$$v_s(t) = R_s i_s(t)$$

From the discussion above, it should be apparent that a signal is a time-varying quantity that can be represented by a graph such as that shown in Fig. 1.2. In fact, the information content of the signal is represented by the changes in its magnitude as time progresses; that is, the information is contained in the "wiggles" in the signal waveform. In general, such waveforms are difficult to characterize mathematically. In other words, it is not easy to describe succinctly an arbitrary-looking waveform such as that of Fig. 1.2. Of course, such a

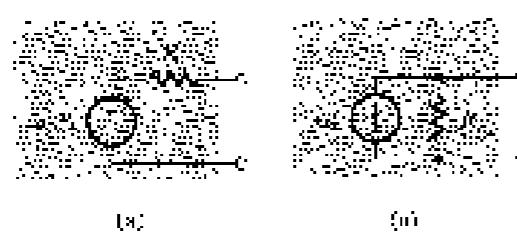


FIGURE 1.1 Two alternative representations of a signal source: (a) the Thévenin form, and (b) the Norton form.



FIGURE 1.2 An arbitrary voltage signal $v(t)$.

description is of great importance for the purpose of designing appropriate signal-processing circuits that perform desired functions on the given signal.

EXERCISES

- 1.1. A signal source is represented by a voltage source $v_s(t) = 10t$, where the open-circuit voltage is 10 V . What is the output resistance, assuming current $i_s(t) = 10t$? What is the equivalent Norton current source? What is the equivalent Thévenin voltage source?
- 1.2. For the circuit shown in Fig. 1.1(a), $v_s(t) = 10\text{ V}$, $R_s = 10\text{ k}\Omega$, $i_s(t) = 10t$, $R_s = 10\text{ k}\Omega$. Calculate the output voltage $v_o(t)$ at the terminals of the load resistor R_L .
- 1.3. A periodic square-wave voltage of 100 V and 100 Hz is applied to the terminals of a 100- Ω load resistor. Calculate the average power delivered to the load.
- 1.4. A 100- Ω load resistor is connected to a 100-V DC voltage source. Calculate the average power delivered to the load.

1.2 FREQUENCY SPECTRUM OF SIGNALS

An extremely useful characterization of a signal, and for that matter of any arbitrary function of time, is in terms of its frequency spectrum. Such a description of signals is obtained through the mathematical tools of Fourier series and Fourier transform. We are not interested at this point in the details of these transformations, suffice it to say that they provide the means for representing a voltage signal $v_s(t)$ or a current signal $i_s(t)$ as the sum of sine waves signals of different frequencies and amplitudes. This makes the sine wave a very important signal in the analysis, design, and testing of electronic circuits. Therefore, we shall briefly review the properties of the sine wave.

Figure 1.3 shows a sine-wave voltage signal $v_s(t)$,

$$v_s(t) = V_m \sin \omega t \quad 1.1$$

¹ The reader who has not yet studied these topics should not be alarmed. No detailed application of this material will be made until Chapter 6. Nevertheless, a general understanding of Section 1.2 should be very helpful when studying early parts of this book.

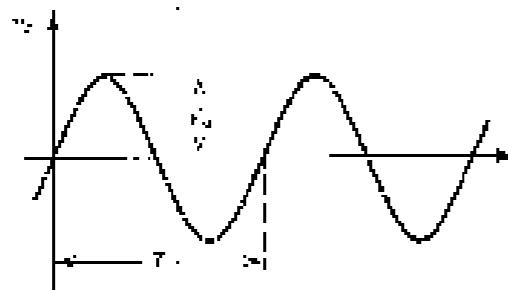


FIGURE 1.3 A sine wave voltage signal $v(t) = V_m \sin(\omega t + \phi)$, amplitude V_m , and frequency $f = 1/T$ Hz. The angular frequency $\omega = 2\pi f$ rad/s.

where V_m denotes the peak value or amplitude in volts and ω denotes the angular frequency in radians per second; that is, $\omega = 2\pi f$ rad/s, where f is the frequency in hertz, $f = 1/T$ Hz, and T is the period in seconds.

The sine-wave signal is completely characterized by its peak value V_m , its frequency f , and its phase with respect to an arbitrary reference time. In the case depicted in Fig. 1.3, the time origin has been chosen so that the phase angle is 0. It should be mentioned that it is common to express the amplitude of a sine-wave signal in terms of its root-mean-square (rms) value, which is equal to the peak value divided by $\sqrt{2}$. Thus the rms value of the sinusoid $v(t)$ of Fig. 1.3 is $V_m/\sqrt{2}$. For instance, when we speak of the total power supplied to our home as being 120 V, we mean that it has a sine waveform, $120\sqrt{2}$ volts peak with.

Returning now to the representation of signals as the sum of sinusoids, we note that the Fourier series is utilized to accomplish this task for the special case when the signal is a periodic function of time. On the other hand, the Fourier transform is more general and can be used to obtain the frequency spectrum of a signal whose waveform is an arbitrary function of time.

The Fourier series allows us to express a given periodic function of time as the sum of an infinite number of sinusoids whose frequencies are harmonically related. For instance, the symmetrical square-wave signal in Fig. 1.4 can be expressed as

$$v(t) = \frac{4V}{\pi} \left[\sin \omega_0 t - \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t - \dots \right] \quad (1.3)$$

where V is the amplitude of the square wave and $\omega_0 = 2\pi/T$. (T is the period of the square wave.) is called the fundamental frequency. Note that because the amplitudes of the harmonics progressively decrease, the infinite series can be truncated, with the truncated series providing an approximation to the square waveform.

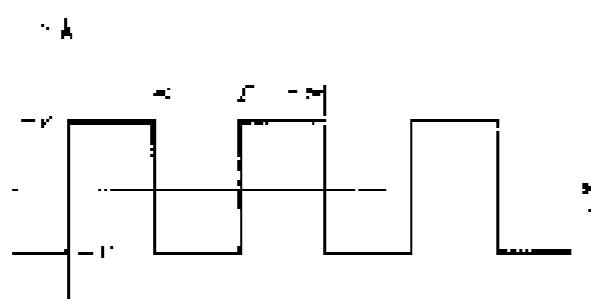


FIGURE 1.4 An asymmetric square-wave signal of amplitude V .

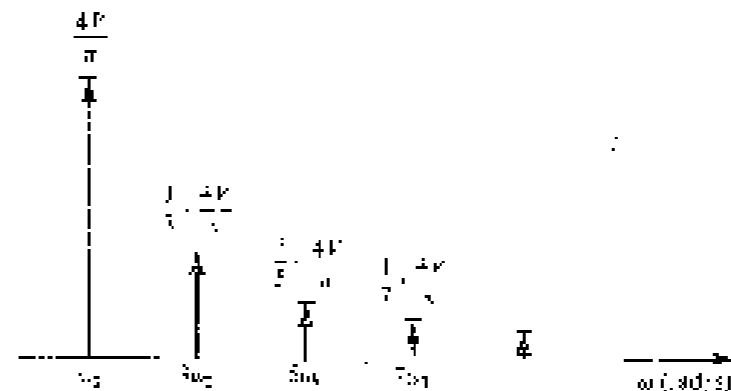


FIGURE 1.5 The frequency spectrum (also known as the line spectrum) of the periodic square wave of Fig. 1.4.

The sinusoidal components in the series of Eq. (1.3) constitute the frequency spectrum of the square-wave signal. Such a spectrum can be graphically represented as in Fig. 1.5, where the horizontal axis represents the angular frequency ω in radians per second.

The Fourier transform can be applied to a nonperiodic function of time, such as that depicted in Fig. 1.2, and provides its frequency spectrum as a continuous function of frequency, as indicated in Fig. 1.6. Unlike the case of periodic signals, where the spectrum consists of discrete frequencies (at ω_0 and its harmonics), the spectrum of a non-periodic signal contains all possible frequencies. Nevertheless, the essential parts of the spectrum of practical signals are usually confined to relatively short segments of the frequency axis—an observation that is very useful in the processing of such signals. For instance, the spectrum of audible sounds such as speech and music extends from about 20 Hz up to about 20 kHz—a frequency range known as the audio band. Here we should note that although some musical tones have frequency as above 20 kHz, the human ear is incapable of hearing frequencies that are much above 20 kHz. As another example, analog video signals have their spectra in the range of 1 MHz to 4.5 MHz.

We conclude this section by noting that a signal can be represented either by the manner in which its waveform varies with time, as for the voltage signal $v(t)$ shown in Fig. 1.2, or in terms of its frequency spectrum, as in Fig. 1.6. The two alternative representations are known as the time-domain representation and the frequency-domain representation, respectively. The frequency-domain representation of $v_s(t)$ will be denoted by the symbol $V_s(\omega)$.

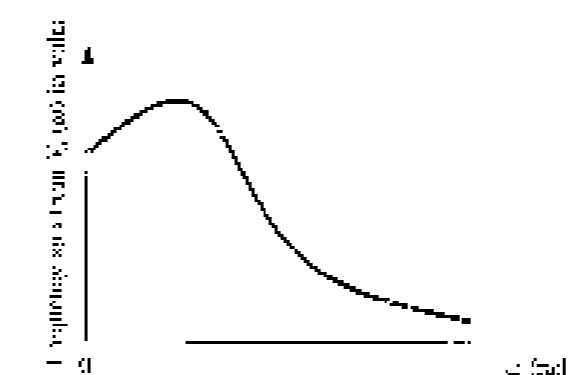


FIGURE 1.6 The frequency spectrum of an arbitrary waveform such as that in Fig. 1.2.

EXERCISES

- 1.3 Find the frequency of the 10 sin ωt sine wave signal with a period of 1 ms.
Ans. $f = 1000 \text{ Hz}$; $\omega = 2\pi \times 10^3 \text{ rad/s}$
- 1.4 What is the period T of the periodic voltage waveform shown in (a)? (a) $f = 60 \text{ Hz}$
(b) $f = 1 \text{ kHz}$
- 1.5 A 100-V AC voltage source is connected in series with a 100- Ω resistor. If the current in the circuit is 1 A, what is the power dissipated by the resistor? How many joules does this amount of energy represent in 1 s?
Ans. 100 W, 100 J
- 1.6 When the square-wave signal of Fig. 1.2, where Fourier series is given in Eq. (1.2), is applied to a resistor, the total power consumed is calculated to be (in Joules) $P = 1/T \int_0^T v^2(t) dt = 2400$. Calculate the average magnitude of each of the harmonic components. That is, $P = P_0 + P_2 + P_4 + \dots$, which may be found directly from the equation. Verify that the two approaches are equivalent. What fraction of the energy is in the fundamental (P_0) in its first five harmonics ($P_0 + P_1 + P_2 + P_3 + P_4$)? Hint: In what number of harmonics is 90% of the energy? (Note that in calculating harmonics, the fundamental (P_0) is the first, the second (P_1) is the second, etc.)
Ans. 0.894, 0.025, 0.012

1.3 ANALOG AND DIGITAL SIGNALS

The voltage signal depicted in Fig. 1.2 is called an **analog signal**. The name derives from the fact that such a signal is an analog to the physical signal that it represents. The magnitude of an analog signal can take on any value; that is, the amplitude of an analog signal exhibits a continuous variation over its range of activity. The vast majority of signals in the world around us are analog. Electronic circuits that process such signals are known as **analog circuits**. A variety of analog circuits will be studied in this book.

An alternative form of signal representation is that of a sequence of numbers, each number representing the signal magnitude at a certain point of time. The resulting signal is called a **digital signal**. To see how a signal can be represented in this form, that is, how signals can be converted from analog to digital form, consider Fig. 1.7(a). Here the curve represents a voltage signal, identical to that in Fig. 1.2. At equal intervals along the time axis we have marked the time instants t_0, t_1, t_2 , and so on. At each of these time instants the magnitude of the signal is measured, a process known as **sampling**. Figure 1.7(b) shows a representation of the signal of Fig. 1.7(a) in terms of its samples. The signal c (Fig. 1.7(c)) is defined only at the sampling instants; it no longer is a continuous function of time, but rather, it is a **discrete-time signal**. However, since the magnitude of each sample can take any value in a certain range, the signal in Fig. 1.7(b) is still an analog signal.

Now if we represent the magnitude of each of the signal samples in Fig. 1.7(b) by a number having a finite number of digits, then the signal amplitude will no longer be continuous; rather, it is said to be **quantized**, **discretized**, or **digitized**. The resulting digital signal then is simply a sequence of numbers that represent the magnitudes of the successive signal samples.

The choice of number system to represent the signal samples affects the type of digital signal produced and has a profound effect on the complexity of the digital circuits required

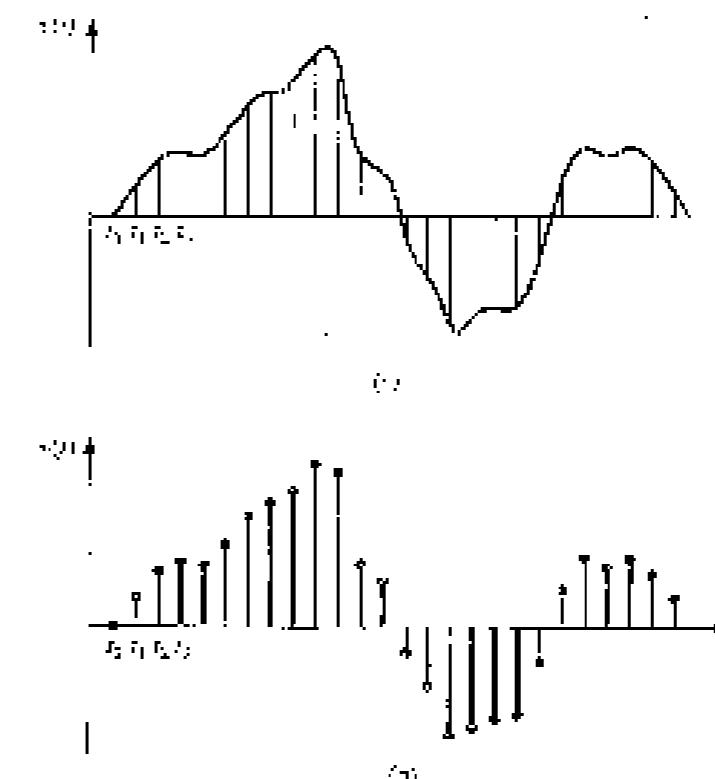


FIGURE 1.7 Sampling the continuous-time voltage signal in (a) results in the discrete-time signal in (b).

to process the signals. It turns out that the binary number system results in the simplest possible digital circuits and devices. In a binary system, each digit is the number taken on one of only two possible values, denoted 0 and 1. Correspondingly, the digital signals in binary systems need have only two voltage levels, which can be labeled low and high. As an example, in some of the digital circuits studied at this point, the levels are 0 V and -5 V. Figure 1.8 shows the time variation of such a digital signal. Observe that the waveforms alternate with 0 V representing a 0 signal, or logic 0, and -5 V representing logic 1.

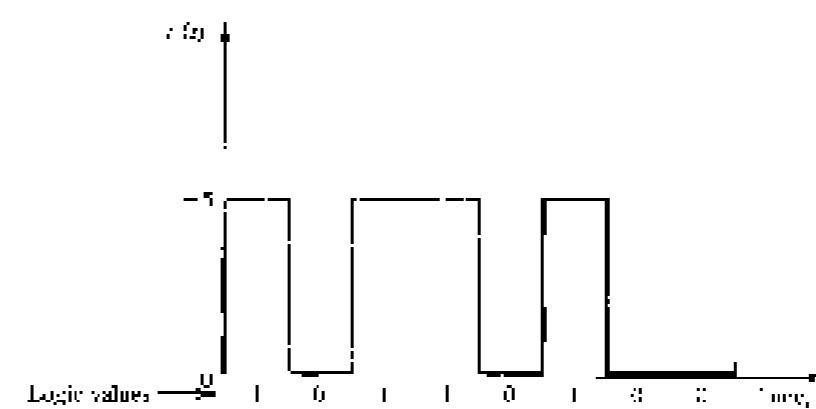


FIGURE 1.8 Variation of a discrete-time binary digital signal with time.

If we use N binary digits (bits) to represent each sample of the analog signal, then the digitized-analog value can be expressed as

$$D = b_0 2^0 + b_1 2^1 + b_2 2^2 + \dots + b_{N-1} 2^{N-1} \quad (1.3)$$

where b_0, b_1, \dots, b_{N-1} denote the N bits and have values of 0 or 1. Here bit b_0 is the least significant bit (LSB), and bit b_{N-1} is the most significant bit (MSB). Conventionally, this binary number is written as $b_{N-1} b_{N-2} \dots b_0$. We observe that such a representation quantizes the analog sample into one of 2^N levels. Obviously the greater the number of bits (i.e., the longer the N), the closer the digital word D approximates the magnitude of the analog sample. That is, increasing the number of bits reduces the quantization error and increases the resolution of the analog-to-digital conversion. This improvement is, however, usually obtained at the expense of more complexity and hence increased circuit implementation. It is not our purpose here to delve into this topic any deeper; we merely want the reader to appreciate the nature of analog and digital signals. Nevertheless, it is an opportune time to introduce a very important circuit building block of modern electronic systems: the analog-to-digital converter (A/D or ADC) shown in block form in Fig. 1.9. The ADC accepts at its input the samples of an analog signal and provides for each input sample the corresponding N -bit digital representation (according to Eq. 1.3) at its N output terminals. Thus although the voltage at the input might be, say, 6.57 V, at each of the output terminals (say, at the b_0 terminal), the voltage will be either low (0 V) or high (5 V) if b_0 is supposed to be 0 or 1, respectively. We shall study the ADC and its dual circuit, the digital-to-analog converter (D/A or DAC) in Chapter 9.

Once the signal is in digital form, it can be processed using digital circuits. Of course, digital circuits can deal also with signals that do not have an analog origin, such as the signals that represent the various instructions of a digital computer.

Since digital circuits deal exclusively with binary signals, their design is simpler than that of analog circuits. Furthermore, digital systems can be designed using a relatively few different kinds of digital circuit blocks. However, a large number (e.g., hundreds of thousands or even millions) of each of these blocks are usually needed. Thus the design of digital circuits poses its own set of challenges to the designer but provides reliable and economic implementations of a great variety of signal processing functions, some of which are not possible with analog circuits. At the present time, almost all of the signal processing operations are being performed digitally. Examples abound us abound: from the digital watch and the telephone to digital audio systems and, more recently, digital television. Moreover, some long-standing analog systems such as the telephone communication system are now almost entirely digital. And we should not forget the most important of all digital systems, the digital computer.

The basic building blocks of digital systems are logic circuits and memory circuits. We shall study both in this book, beginning in Section 1.7 with the most fundamental digital circuit, the digital logic inverter.



FIGURE 1.9 Block diagram representation of the analog-to-digital converter (ADC).

One final remark: Although the digital processing of signals is at present all pervasive, there remain many signal-processing functions that are best performed by analog circuits. Indeed, many electronic systems include both analog and digital parts. It follows that a good electronics engineer must be proficient in the design of both analog and digital circuits, of mixed-signal or mixed-mode design as it is currently known. Such is the aim of this book.

EXERCISE

- (1) Consider an 8-bit word D with a maximum value of 255. If the word is represented in binary form, what is the range of the word? What is the minimum value of the word? What is the maximum value of the word? What is the range of the word? What is the minimum value of the word? What is the maximum value of the word?
- (2) What happens if the digital word D in Exercise 1 is represented in binary form? What is the range of the word? What is the minimum value of the word? What is the maximum value of the word?
- (3) Suppose the digital word D in Exercise 1 is represented in binary form. If the word is 8 bits long, what is the range of the word? What is the minimum value of the word? What is the maximum value of the word?

1.4 AMPLIFIERS

In this section, we shall introduce a fundamental signal-processing function that is employed in some form in almost every electronic system, namely, signal amplification. We shall study the amplifier as a circuit building block. It is considered in external characteristics and leave the design of its internal circuit to later chapters.

1.4.1 Signal Amplification

From a conceptual point of view the simplest signal-processing task is that of signal amplification. The need for amplification arises because transducers provide signals that are said to be "weak," that is, in the microvolt (μV) or millivolt (mV) range and possessing little energy. Such signals are too small for reliable processing, and processing is much easier if the signal magnitude is made larger. The functional block that accomplishes this task is the signal amplifier.

It is appropriate at this point to discuss the need for linearity in amplifiers. When amplifying a signal, care must be exercised so that the information contained in the signal is not changed and no new information is introduced. That is, when feeding the signal shown in Fig. 1.2 to an amplifier, we want the output signal of the amplifier to be an exact replica of that at the input, except of course for having larger magnitude. In other words, the "wiggles" in the output waveform must be identical to those in the input waveform. Any change in waveform is considered to be distortion and is obviously undesirable.

An amplifier that preserves the jitters of the input waveform is characterized by the relationship

$$v_o(t) = A v_i(t) \quad (1.4)$$

where v_i and v_o are the input and output signals, respectively, and A is a constant representing the magnitude of amplification, known as amplifier gain. Equation 1.4 is a linear relationship; hence the amplifier it describes is a linear amplifier. It should be easy to see that if the relationship between v_o and v_i contains higher powers of v_i , then the waveform of v_o will no longer be identical to that of v_i . The amplifier is then said to exhibit nonlinear distortion.

The amplifiers discussed so far are primarily intended to operate on very small input signals. Their purpose is to make the signal magnitude larger and therefore are thought of as voltage amplifiers. The preamplifier in the home stereo system is an example of a voltage amplifier. However, it usually does more than amplify the signal; specifically, it performs some shaping of the frequency spectrum of the input signal. This topic, however, is beyond our needs at this moment.

At this time we wish to mention another type of amplifier, namely, the power amplifier. Such an amplifier may provide only a modest amount of voltage gain but substantial current gain. Thus while absorbing little power from the input signal source to which it is connected, often a preamplifier, it delivers large amounts of power to its load. An example is found in the power amplifier of the home stereo system, whose purpose is to provide voltage source to drive the loudspeaker, which is the amplifier load. Here we should note that the loudspeaker is the output transducer of the stereo system; it converts the electric output signal of the system into an acoustic signal. A further appreciation of the need for linearity can be acquired by reflecting on the power amplifier. A linear power amplifier uses both positive and negative passages to be reproduced without distortion.

1.4.2 Amplifier Circuit Symbol

The signal amplifier is obviously a two-port network. Its function is conveniently represented by the circuit symbol of Fig. 1.10(a). This symbol clearly distinguishes the input and output ports and indicates the direction of signal flow. Thus, in subsequent diagrams it will not be necessary to label the two ports "input" and "output." For generality we have shown the amplifier to have two input terminals that are distinct from the two output terminals. A more common situation is illustrated in Fig. 1.10(b), where a common terminal exists between the input and output ports of the amplifier. This common terminal is used as a reference point here to call the circuit ground.

1.4.3 Voltage Gain

A linear amplifier accepts an input signal $v_{in}(t)$ and provides at the output, across a load resistance R_L (see Fig. 1.11(a)), an output signal $v_{out}(t)$ that is a magnified replica of $v_{in}(t)$. The voltage gain of the amplifier is defined by

$$\text{Voltage gain } (A_v) = \frac{v_{out}}{v_{in}} \quad (1.5)$$

Fig. 1.11(b) shows the transfer characteristic of a linear amplifier. If we apply to the input of this amplifier a sinusoidal voltage of amplitude V , we obtain at the output a sinusoid of amplitude $A_V V$.

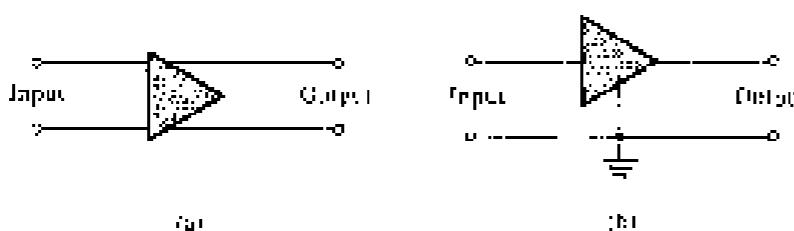


FIGURE 1.10: (a) General symbol for an amplifier. (b) An amplifier with a common terminal (ground) between the input and output ports.

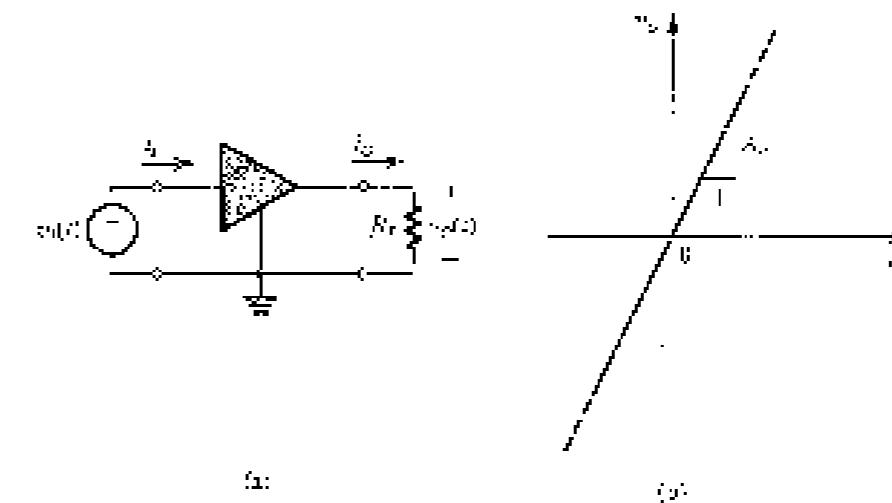


FIGURE 1.11: (a) A voltage amplifier fed with signal $v_{in}(t)$ and connected to a load resistance R_L . (b) Transfer characteristic of a linear voltage amplifier with voltage gain A_v .

1.4.4 Power Gain and Current Gain

An amplifier increases the signal power, an important factor that distinguishes an amplifier from a transformer. In the case of a transformer, although the voltage delivered to the load could be greater than the voltage feeding the input side (the primary), the power delivered to the load (from the secondary side of the transformer) is less than or at most equal to the power supplied by the signal source. On the other hand, an amplifier provides the load with power greater than that obtained from the signal source. That is, amplifiers have power gain. The power gain of the amplifier in Fig. 1.11(a) is defined as

$$\text{Power gain } (A_p) = \frac{\text{load power } (P_L)}{\text{input power } (P_i)} \quad (1.6)$$

$$= \frac{v_{out} i_o}{v_{in} i_i} \quad (1.7)$$

where i_o is the current that the amplifier delivers to the load (R_L), $i_i = v_{in}/R_i$, and i_i is the current the amplifier draws from the signal source. The current gain of the amplifier is defined as

$$\text{Current gain } (A_i) = \frac{i_o}{i_i} \quad (1.8)$$

From Eqs. (1.5) to (1.8) we find that

$$A_p = A_v A_i \quad (1.9)$$

1.4.5 Expressing Gain in Decibels

The amplifier gains defined above are ratios of similarly dimensioned quantities. Thus they will be expressed either as dimensionless numbers or, for emphasis, as V/V for the voltage gain, A/A for the current gain, and W/W for the power gain. Alternatively, for a number of reasons, some of them historical, electronic engineers express amplifier gain with a logarithmic measure. Specifically the voltage gain A_v can be expressed as

$$\text{Voltage gain in decibels} = 20 \log A_v \quad (1.8)$$

and the current gain A_i can be expressed as

$$\text{Current gain in decibels} = 20 \log A_i \quad \text{dB}$$

Since power is related to voltage (or current) squared, the power gain A_p can be expressed in decibels as

$$\text{Power gain in decibels} = 10 \log A_p \quad \text{dB}$$

The absolute values of the voltage and current gains are used because in some cases A or A_i may be negative numbers. A negative gain A_v simply means that there is a 180° phase difference between input and output signals; it does not imply that the amplifier is attenuating the signal. On the other hand, an amplifier whose voltage gain is, say, -20 dB is in fact inverting the input signal by a factor of 10 (i.e., $A_v = 0.1 \text{ V/V}$).

1.4.6 The Amplifier Power Supplies

Since the power delivered to the load is greater than the power drawn from the signal source, the question arises as to the source of this additional power. The answer is found by observing that amplifiers need dc power supplies for their operation. These dc sources supply the extra power delivered to the load as well as any power that might be dissipated in the internal circuit of the amplifier (such power is referred to as heat). In Fig. 1.12(a) we have not explicitly shown these dc sources.

Figure 1.12(b) shows an amplifier that requires two dc sources: one positive of value V_1 and one negative of value V_2 . The amplifier has two terminals, labeled V^+ and V^- , for connection to the dc supplies. But the amplifier to operate, the terminal labeled V^+ has to be connected to the positive side of a dc source whose voltage is V_1 and whose negative side is connected to the circuit ground. Also, the terminal labeled V^- has to be connected to the negative side of a dc source whose voltage is V_2 and whose positive side is connected to the circuit ground. Now, if the current drawn from the positive supply is denoted I_1 and that from the negative supply is I_2 (see Fig. 1.12(a)), then the dc power delivered to the amplifier is

$$P_d = V_1 I_1 + V_2 I_2$$

If the power dissipated in the amplifier circuit is denoted $P_{\text{dissipated}}$, the power-balance equation for the amplifier can be written as

$$P_{\text{in}} + P_d = P_s + P_{\text{dissipated}}$$

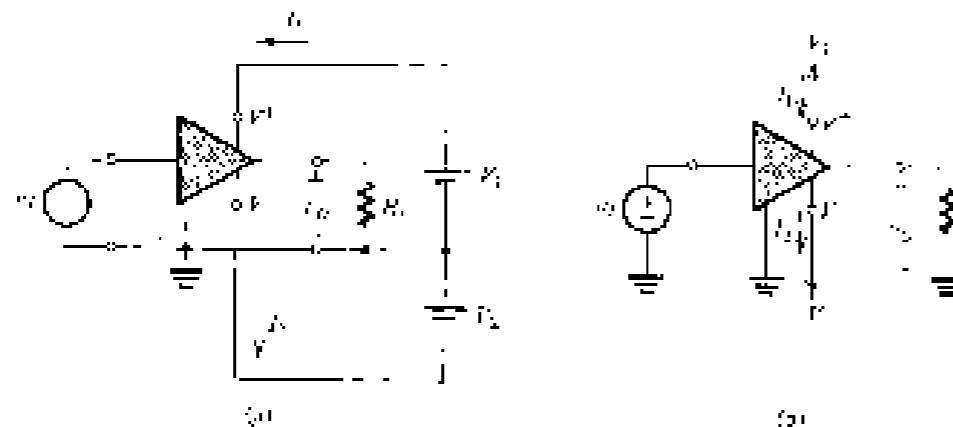


FIGURE 1.12 An amplifier that requires two dc supplies (second op-amp not for operation).

where P_s is the power drawn from the signal source and P_d is the power delivered to the load. Since the power drawn from the signal source is usually small, the **amplifier efficiency** is defined as

$$\eta = \frac{P_d}{P_s} \times 100 \quad (1.16)$$

The power efficiency is an important performance parameter for amplifiers. Such a large amount of power. Such amplifiers, called power amplifiers, are used, for example, as output amplifiers of stereo systems.

In order to simplify circuit diagrams, we shall adopt the convention illustrated in Fig. 1.12(c). Here the V^+ terminal is shown connected to an arrowhead pointing upward and the V^- terminal to an arrowhead pointing downward. The corresponding voltage is indicated next to each arrowhead. Note that in many cases we will not explicitly show the connections of the amplifier to the dc power sources. Finally, we note that some amplifiers require only one power supply.



Example 1.12 Consider an amplifier operating from ± 10 V power supplies. It is fed with a sinusoidal voltage having 1 V peak and delivers a sinusoidal voltage output of 9 V peak to a 1 kΩ load. The amplifier draws a current of 9.5 mA from each of its two power supplies. The input current of the amplifier is found to be sinusoidal with 0.1 mA peak. Find the voltage gain, the current gain, the power ratio, the power drawn from the dc supplies, the power dissipated in the amplifier, and the amplifier efficiency.

Solution

$$A_v = \frac{9}{1} = 9 \text{ V/V}$$

or

$$A_v = 20 \log 9 = 19.1 \text{ dB}$$

$$I_1 = \frac{9 \text{ V}}{2 \text{ k}\Omega} = 9 \text{ mA}$$

$$A_i = \frac{I_2}{I_1} = \frac{0.1}{9} = 0.01 \text{ A/A}$$

or

$$A_i = 20 \log 0.01 = -39.1 \text{ dB}$$

$$P_s = V_{\text{in}} I_{\text{in}} = \frac{0.1 \text{ V}}{\sqrt{2} \text{ k}\Omega} \cdot 0.1 \text{ mA} = 43.5 \text{ mW}$$

$$P_d = V_{\text{out}} I_{\text{out}} = \frac{9 \text{ V}}{\sqrt{2} \text{ k}\Omega} \cdot 9.5 \text{ mA} = 0.05 \text{ mW}$$

$$A_p = \frac{P_d}{P_s} = \frac{0.05}{43.5} = 810 \text{ W/W}$$

or

$$A_p = 10 \log 810 = 26.1 \text{ dB}$$

$$P_{\text{dc}} = 10 \times 0.5 + 10 \times 0.5 = 10 \text{ W}$$

$$\begin{aligned} P_{\text{dc power}} &= P_{\text{dc}} - P_{\text{d}} - P_{\text{c}} \\ &= 100 - 50.5 - 10.5 = 39.0 \text{ mW} \\ \beta &= \frac{P_{\text{d}}}{P_{\text{c}}} = 130 = 21.0\% \end{aligned}$$

From the above example we observe that the amplifier converts some of the dc power it draws from the power supplies to signal power that it delivers to the load.

1.4.7 Amplifier Saturation

Practically speaking, the amplifier transfer characteristic is a straight line over only a limited range of input and output voltages. For an amplifier operated from two power supplies the output voltage cannot exceed a specific positive limit, and cannot decrease below a specified negative limit. The resulting transfer characteristic is shown in Fig. 1.13, with the positive and

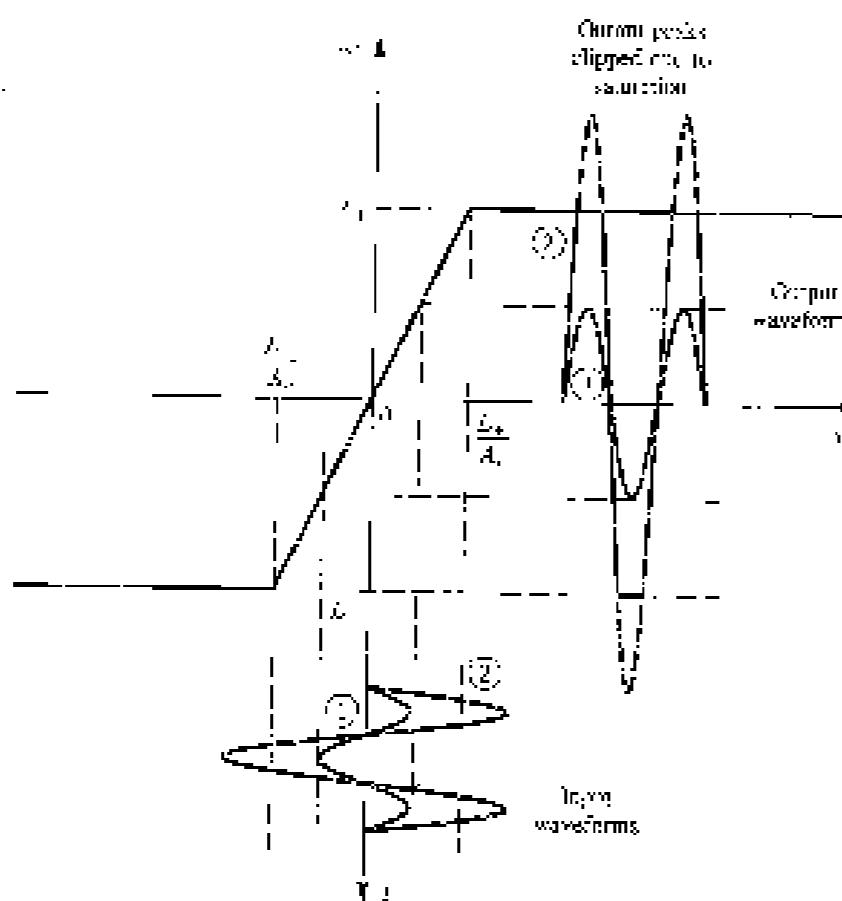


FIGURE 1.13 An amplifier circuit designer she has to linearize except for output waveform.

negative saturation levels denoted V_d and V_u , respectively. Each of the two saturation levels is usually within a volt or so of the voltage of the corresponding power supply.

Obviously, in order to avoid distorting the output signal waveform, the input signal swing must be kept within the linear range of operation.

$$\frac{V_d}{A_v} < v_i < \frac{V_u}{A_v}$$

Figure 1.14 shows two input waveforms and the corresponding output waveforms. We note that the peaks of the larger waveform have been clipped off because of amplifier saturation.

1.4.8 Nonlinear Transfer Characteristics and Biasing

Except for the output voltage, as often discussed above, the amplifier transfer characteristics have been assumed to be perfectly linear. In practical amplifiers the transfer characteristic may exhibit non-linearities of various magnitudes, depending on how elaborate the amplifier circuit is and/or how much effort has been expended in the design to ensure linear operation. Consider as an example the transfer characteristic depicted in Fig. 1.14. Such a characteristic is typical of simple amplifiers that are energized from a single positive power supply. The transfer characteristic is obviously non-linear and, because of the single-supply operation, is not centered around the origin. Fortunately, a simple technique exists for obtaining linear amplification from an amplifier with such a nonlinear transfer characteristic.

The technique consists of biasing the circuit to operate at a point near the middle of the transfer characteristic. This is achieved by applying a dc voltage V_b , as indicated in Fig. 1.14, where the operating point is labeled Q and the corresponding dc voltage at the output is V_Q . The point Q is known as the quiescent point, the dc bias point, or simply the operating point. The time-varying signal to be amplified, $v_i(t)$, is then superimposed on the dc bias voltage V_b , as indicated in Fig. 1.14. Note, as the total instantaneous input $v_i(t)$,

$$v_i(t) = V_b + v_i(t)$$

varies around V_b . At instantaneous operating point moves up and down the transfer curve around the dc operating point Q . In this way, one can determine the waveform of the total instantaneous output voltage $v_o(t)$. It can be seen that by keeping the amplitude of $v_i(t)$ sufficiently small, the instantaneous operating point can be confined to an almost linear segment of the transfer curve centered about Q . This in turn results in the large varying junction of the output being proportional to $v_i(t)$; that is,

$$v_o(t) = V_Q + v_o(t)$$

with

$$v_o(t) = \alpha_{\text{v}} v_i(t)$$

where α_{v} is the slope of the almost linear segment of the transfer curve, that is,

$$\alpha_{\text{v}} = \left. \frac{dv_o}{dv_i} \right|_{v_i=0}$$

In this manner, linear amplification is achieved. Of course, there is a limitation: The input signal must be kept sufficiently small. Increasing the amplitude of the input signal will cause

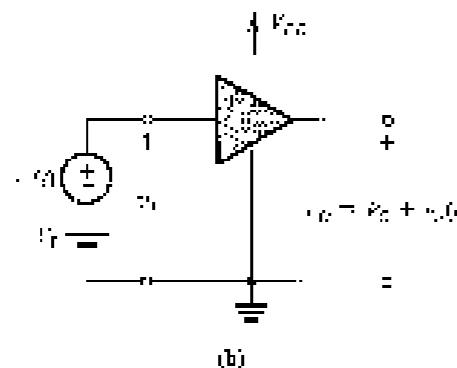
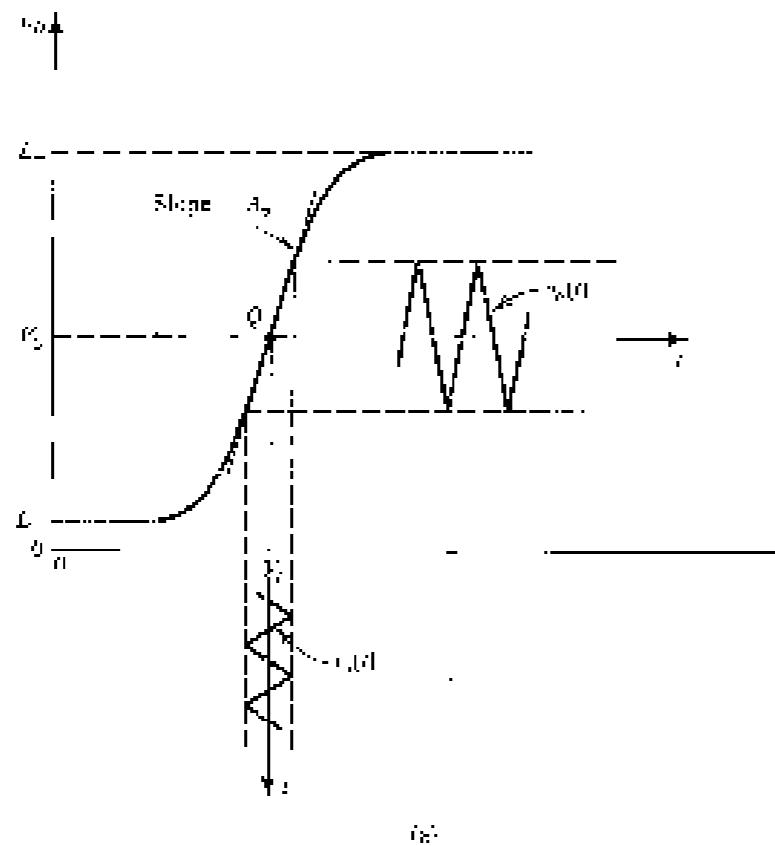


FIGURE 1.14 (a) An amplifier transfer characteristic that shows considerable nonlinearity. (b) To obtain linear operation the amplifier gain A_v is chosen so the signal amplitude is kept small. Observe that this amplifier is operated from a single power supply, V_{DD} .

the operation to be no longer restricted to an almost linear segment of the transfer curve. This in turn results in a distorted output signal waveform. Such nonlinear distortion is undesirable. The output signal contains additionalurious information that is not part of the input. We shall use this biasing technique and the associated small-signal approximation frequently in the design of transistor amplifiers.



A transistor amplifier has the transfer characteristic

$$v_o = 10 \cdot 10^{-3} e^{10v_i} \quad (1.14)$$

which applies for $v_i > 0$ V and $v_o > 0$ V. Find the limits L_1 and L_2 and the corresponding values of v_i . Also, find the value of the bias voltage V_b that results in $V_o = 5$ V and the voltage gain at the corresponding operating point.

Solution

The limit L_1 is obviously 0 V. The corresponding value of v_i is obtained by substituting $v_o = 0$ V in Eq. (1.14), that is,

$$v_i = 0.693 \text{ V}$$

The limit L_2 is determined by $v_i = 0$ and is thus given by

$$L_2 = 10 \cdot 10^{-3} \approx 10 \text{ V}$$

To bias the device so that $V_o = 5$ V we require a dc input v_i , whose value is obtained by substituting $v_o = 5$ V in Eq. (1.14) to find,

$$v_i = 0.673 \text{ V}$$

The gain at the operating point is obtained by evaluating the derivative $d v_o / d v_i$ at $v_i = 0.673$ V. The result is

$$A_v = -200 \text{ V/V}$$

which indicates that this amplifier in an inverting one; that is, the output is 180° out of phase with the input. A sketch of the amplifier transfer characteristic (not to scale) is shown in Fig. 1.15, from which we observe the inverting nature of the amplifier.

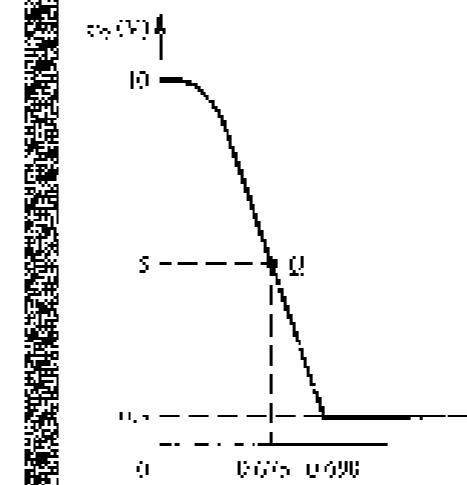


FIGURE 1.15 A sketch of the transfer characteristic for Example 1.2. Note that this amplifier is inverting; i.e., with a gain that is negative.

Once an amplifier is properly biased and the input signal is kept sufficiently small, the operation is assumed to be linear. We can then employ the techniques of linear circuit analysis to analyze the signal operation of the amplifier circuit. This is the topic of Sections 1.5 and 1.6.

1.4.3 Symbol Convention

At this point, we draw the reader's attention to the terminology used above and which we shall employ throughout the book. Total instantaneous quantities are denoted by a lowercase symbol with an uppercase subscript, for example, $i_{\text{L}}(t)$, $v_{\text{C}}(t)$. Direct-current (dc) quantities will be denoted by an uppercase symbol with an uppercase subscript, for example, I_{L} , V_{C} . Power-supply (dc) voltages are denoted by an uppercase V with a double-letter uppercase subscript, for example, V_{DD} . A similar notation is used for the dc current drawn from the power supply, for example, I_{DD} . Finally, a sinusoidal signal quantities will be denoted by a lowercase symbol with a lowercase subscript (for example, $i_{\text{L}}(t)$, $v_{\text{C}}(t)$). If the signal is a sine wave, then its amplitude - denoted by an uppercase letter with a lowercase subscript, for example, I_{L} , V_{C} . This notation is illustrated in Fig. 1.18.

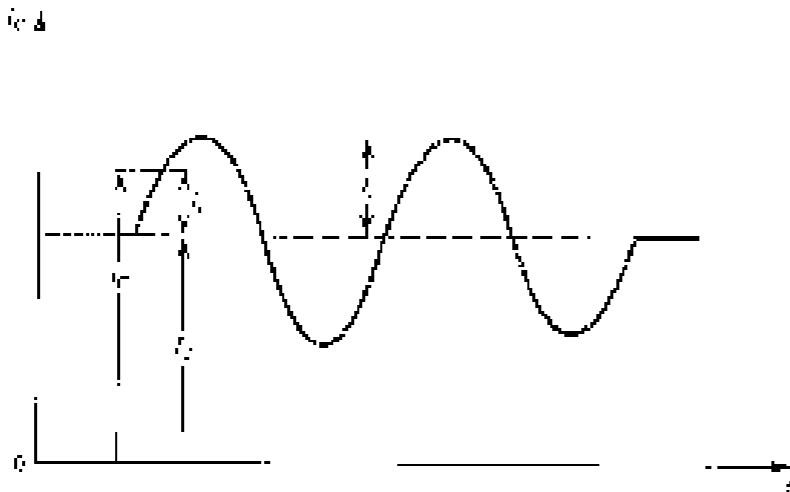


FIGURE 1.16 Symbolic covariance complex of the Δ_0 state function.



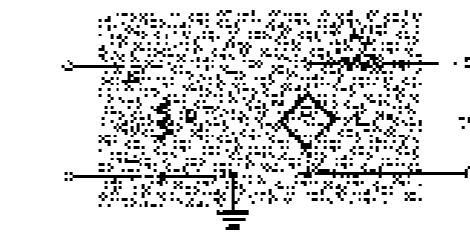
40-TRI project, which is being run in the small journalistic outlet (2013-2014) from the US, and the Chronicle 12 will be published in 2014. The newspaper will be printed in English, and it will be publishing news and commentaries dealing with the political, social and cultural life of the country. The project is funded by the US government and the US Embassy in Tashkent.

1.5 CIRCUIT MODELS FOR AMPLIFIERS

A good part of this book is concerned with the design of amplifier circuits using transistors or operational amplifiers. Such circuits will vary in complexity from those using a single transistor to those with 20 or more devices, in order to be able to apply the resulting amplifier circuit, i.e., building block in a system, one must have to characterize, or model, its resulting behavior. In this section, we study simple but effective amplifier models. These models apply irrespective of the complexity of the actual circuit of the amplifier. The values of the model parameters can be found either by analyzing the amplifier circuit or by performing measurements at the amplifier terminals.

1.5.1 Voltage Amplifiers

Figure 1.17(a) shows a circuit model for the voltage-controlled voltage source having a gain function A_{v1} , an input resistance R_i that accounts for the fact that the amplifier draws an input current from the signal source, and an output resistance R_o that accounts for the change in output voltage as the amplifier is loaded up to



1



i

FIGURE 1.17 (a) Circuit model for the voltage source for the voltage amplifier with no signal source and load.

supply output current to a load. To be specific, we show in Fig. 1.1-3(b) the amplifier needed with a signal voltage source v_1 having a resistance R_1 , and connected at the output to a load resistance R_L . The nonzero output resistance R_o causes only a fraction β of v_{out} to appear across the output. Using the voltage-divider rule we obtain

$$r_i = A_{i,i} \rho_i \frac{R_i}{R_i + g}$$

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$$A_0 = \frac{d_0}{\rho_0} + A_{\infty} \frac{\theta_0}{\theta_0 - \theta_0^*}, \quad (112)$$

It follows that in order not to lose gain in coupling the amplifier output to a load, the output resistance R_o should be much smaller than the load resistance R_L . In other words, for a given R_L one must design the amplifier so that its R_o is much smaller than R_L . Furthermore, there are applications in which R_L is known to vary over a certain range. In order to keep the output voltage v_o as constant as possible, the amplifier is designed with R_o much smaller than the largest value of R_L . An ideal voltage amplifier is one with $R_o = 0$. Equation (1.17) indicates it is that for $R_L = \infty$, $A_o = A_{\infty}$. Thus A_{∞} is the voltage gain of the unloaded amplifier, or the open-circuit voltage gain. It should also be clear that in specifying the voltage gain of an amplifier, one must also specify the value of R_L and the value at which this gain is measured or calculated. If a load resistance is not specified, it is normally assumed that the given voltage gain is the open-circuit gain A_{∞} .

The finite input resistance R_i introduces non-linear voltage-divider action at the input, with the result that only a fraction of the source signal V_s actually reaches the input terminals of the amplifier; that is,

$$z_i' \sim \rho_i \frac{R_i}{\rho_i R_i + R} \quad (1.19)$$

It follows that in order not to lose a significant portion of the input signal in coupling the signal source to the amplifier input, the amplifier must be designed to have an input resistance R_i much greater than the resistance of the signal source, $R_s \gg R_i$. Furthermore, there are applications in which the source resistance is known to vary over a certain range. To minimize the effect of this variation on the value of the signal that appears at the input of the amplifier, the design ensures that R_i is much greater than the largest value of R_s . An ideal voltage amplifier is one with $R_i = \infty$. In this ideal case both the current gain and power gain become infinite.

The overall scheme may (1/2) say as follows: see for Fig. 1(2) and 1(3).

$$\frac{R_i}{k} = A_{i,i} \frac{R_i}{R_i + S} \frac{S_i}{R_i + S}$$

There are situations in which one is interested not in voltage gain but only in a significant power g_{out} . For instance, the source signal can have a respectable voltage but a source resistance which is much greater than the load resistance. Connecting the source directly to the load would result in significant signal attenuation. In such a case, one requires an amplifier with a high input resistance (much greater than the source resistance) and a low output impedance (much smaller than the load resistance) but with a modest or large gain for overall gain. Such an amplifier is referred to as a buffer amplifier. We shall encounter buffer amplifiers often throughout the book.

EXERCISES

1.5.2 Cascaded Amplifiers

To meet given amplifier specifications the need often arises to design the amplifier as a cascade of two or more stages. The stages are usually not identical, rather each is designed to serve a specific purpose. For instance, the first stage is usually required to have a large input resistance, and the final stage in PC practice is usually designed to have a low output resistance. To illustrate the analysis and design of cascaded amplifiers, we consider a practical example.



Figure 1-18 depicts an example of a cascade of three stages. The input port is fed by a signal source with a source resistance of $100 \text{ k}\Omega$ and develops an output from a load resistance of 100Ω . The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last or output stage has unity gain but a low output resistance. We wish to evaluate the overall voltage gain. That is, we want to calculate g_m and the power gain.

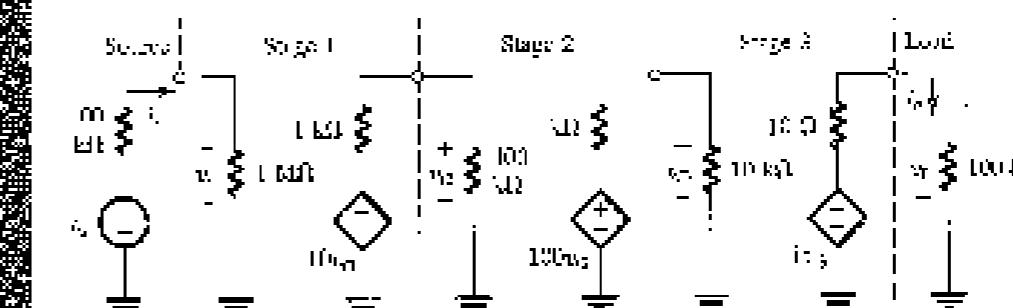


FIGURE 1-18 Cross-sections of the human eye.

Solution:

The fraction of source signal appearing at the input terminals of the amplifier is obtained using the voltage-divider rule at the input, as follows:

$$\frac{v_2}{v_s} = \frac{1 \text{ M}\Omega}{1 \text{ M}\Omega + 100 \text{ k}\Omega} = 0.009 \text{ V/V}$$

The voltage gain of the first stage is obtained by considering the input resistance of the second stage to be the load of the first stage; that is,

$$A_{v1} = \frac{v_3}{v_2} = 100 \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega + 1 \text{ k}\Omega} = 9.9 \text{ V/V}$$

Similarly, the voltage gain of the second stage is obtained by considering the input resistance of the third stage to be the load of the second stage;

$$A_{v2} = \frac{v_4}{v_3} = 100 \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 1 \text{ k}\Omega} = 9.09 \text{ V/V}$$

Finally, the voltage gain of the output stage is as follows:

$$A_{v3} = \frac{v_o}{v_4} = 1 \frac{100 \text{ }\Omega}{10 \text{ }\Omega + 10 \text{ }\Omega} = 0.909 \text{ V/V}$$

The total gain of the three stages in cascade can now be found from

$$A_v = \frac{v_o}{v_s} = A_{v1} A_{v2} A_{v3} = 819 \text{ V/V}$$

ANSWER

To find the voltage gain from source to load, we multiply A_v by the factor representing the loss of gain at the input; that is,

$$\begin{aligned} \frac{v_o}{v_s} &= \frac{A_v v_s}{R_s R_o} = A_v \frac{v_s}{R_o} \\ &\approx 819 \times 0.909 = 736 \text{ mV} \end{aligned}$$

or 27.1 dB.

The current gain is found as follows:

$$\begin{aligned} A_i &= \frac{i_o}{i_s} = \frac{v_o / 100 \text{ }\Omega}{v_s / 1 \text{ M}\Omega} \\ &= 0.009 \times 819 = 6.18 \times 10^4 \text{ A/A} \end{aligned}$$

or 136.3 dB.

The power gain is found from

$$\begin{aligned} A_p &= \frac{P_o}{P_s} = \frac{v_o i_o}{v_s i_s} \\ &= A_v A_i = 819 \times 6.18 \times 10^4 = 50.9 \times 10^7 \text{ W/W} \end{aligned}$$

or 98.3 dB. Note that

$$A_p(\text{dB}) = \frac{1}{2}[A_v(\text{dB}) + A_i(\text{dB})]$$

A few comments on the cascade amplifier in the above example are in order. To avoid losing signal strength at the amplifier input where the signal is usually very small, the first stage is designed to have a relatively large input resistance (1 MΩ), which is much larger than the source resistance. The trade-off appears to be a moderate voltage gain (10 V/V). The second stage does not need to have such a high input resistance, either, but we need to realize the bulk of the required voltage gain. The third and final, or output, stage is not asked to provide any voltage gain; rather, it functions as a buffer amplifier, providing a relatively large input resistance and a low output resistance, much lower than R_o . It is this stage that enables connecting the amplifier to the 10 kΩ load. These points can be made more concrete by solving the following exercises.

EXERCISES

- 1.4.1 What is the overall voltage gain of the cascade amplifier in Example 1.3 if no voltage loss is at the input?
- 1.4.2 For the cascade amplifier in Example 1.3, what is the current gain?
- 1.4.3 For the cascade amplifier in Example 1.3, what is the power gain?
- 1.4.4 Model the three-stage amplifier of Example 1.3. Realize the voltage and current gains of each stage. What are the values of A_{v1} , A_{v2} , and A_{v3} ? What is the value of A_i ? What is the value of A_p ? Assume $v_s = 10 \text{ mV}$ and $R_s = 1 \text{ M}\Omega$.
- 1.4.5 Model the three-stage amplifier of Example 1.3. Realize the voltage and current gains of each stage. What are the values of A_{v1} , A_{v2} , and A_{v3} ? What is the value of A_i ? What is the value of A_p ? Assume $v_s = 10 \text{ mV}$ and $R_s = 1 \text{ M}\Omega$.

1.5.3 Other Amplifier Types

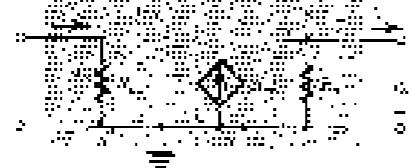
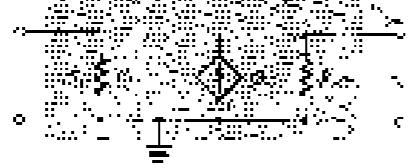
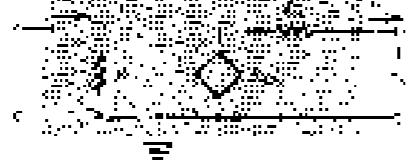
In the design of an electronic system, the signal of interest—whether at the system input or an intermediate stage, or at the output—can be either a voltage or a current. For instance, some transistors have very high output resistances and can be more appropriately modeled as current sources. Similarly, there are amplifiers in which the output current rather than the voltage is of interest. Thus, although it is the most popular, the voltage amplifier considered above is just one of four possible amplifier types. The other three are the current amplifier, the transconductance amplifier, and the transresistance amplifier. Table 1.1 shows the four amplifier types, their circuit models, the definition of the gain parameters, and the ideal values of their input and output resistances.

1.5.4 Relationships Between the Four Amplifier Models

Although for a given amplifier a particular one of the four models in Table 1.1 is more preferable, any of the four can be used to model the amplifier. In fact, simple relationships can be derived to relate the parameters of the various models. For instance, the open-circuit voltage gain A_{ov} can be related to the short-circuit current gain A_i as follows: The open-circuit output voltage given by the voltage amplifier model of Table 1.1 is $A_{ov} v_s$. The current amplifier model in the same table gives an open-circuit output voltage of $A_i v_s R_o$. Equating these two values and noting that $i = v/R$ gives

$$A_{ov} = A_i \sqrt{\frac{R_o}{R_s}} \quad (1.4)$$

TABLE 1.1 The Four Amplifier Types

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{v0} = \frac{V_C}{V_B} \quad (\text{V/V})$	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{i0} = \frac{I_C}{I_B} \quad (\text{A/A})$	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_{o0} = \frac{I_C}{V_B} \quad (\text{A/V})$	$R_i = \infty$ $R_o = 0$
Transresistance Amplifier		Open-Circuit Transresistance $R_{o0} = \frac{V_C}{I_B} \quad (\text{V/A})$	$R_i = 0$ $R_o = 0$

Similarly, we can show that

$$A_{i0} = G_{o0} R_o \quad (1.15)$$

and

$$A_{r0} = \frac{R_o}{R_i} \quad (1.16)$$

The expressions in Eqs. (1.14) to (1.16) can be used to relate any two of the gain parameters, A_{v0} , A_{i0} , G_{o0} , and R_{o0} .

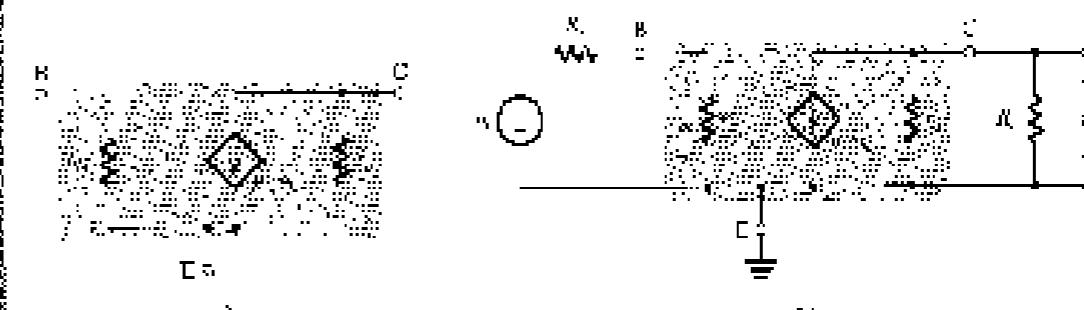
From the amplifier circuit models given in Table 1.1, we observe that the input resistance R_i of the amplifier can be determined by applying an input voltage v_B and measuring the resulting input current i_B (i.e., $R_i = v_B/i_B$). The output resistance is found as the ratio of the open-circuit output voltage to the short-circuit output current. Alternatively, the output resistance can be found by eliminating the input signal source (then v_B and i_B will both be zero) and applying a voltage signal v_C to the output of the amplifier. If we denote the current drawn from v_C to the output terminals as i_C (note that i_C is opposite in direction to i_B), then $R_o = v_C/i_C$. Although these techniques are conceptually elegant, in actual practice more refined methods are employed at measuring R_i and R_o .

The amplifier models discussed above are **unilateral**: that is, signal flow is unidirectional, from input to output. Most real amplifiers show some reverse transmission, which is usually undesirable but must nonetheless be modeled. We shall not pursue this point

further at this time except to mention that more complete models for linear two-port networks are given in Appendix H. Also, in Chapters 4 and 5, we will augment the models of Table 1.1 to take into account the nonreciprocal nature of some microwave amplifiers.

1.5.1 Bipolar Junction Transistor (BJT) Model

The bipolar junction transistor (BJT), which will be studied in Chapter 5, is a three-terminal device that when dc biased and operated with small signals can be modeled by the linear circuit shown in Fig. 1.19(a). The three terminals are the base (B), the emitter (E), and the collector (C). The base of the model is a transverse diode with a short-circuit transconductance g_{o0} and an output resistance R_o .



(a) Bipolar junction transistor (BJT) model.



(b)



(c)

FIGURE 1.19 (a) Small-signal circuit model for a bipolar junction transistor (BJT). (b) The BJT connected as a common-emitter amplifier with the collector terminal between input and output. (c) An alternative small-signal circuit model for the BJT.

(a) With the emitter used as a common terminal between input and output, Fig. 1.19(b) shows a transistor amplifier shown as a common-emitter or grounded-emitter circuit. Derive an expression for the voltage gain v_C/v_B and evaluate its magnitude for the case $R_i = 3\text{ k}\Omega$, $r_o = 2.5\text{ M}\Omega$, $g_{o0} = 40\text{ m A/V}$, $r_s = 100\text{ k}\Omega$, and $R_o = 5\text{ k}\Omega$. What would the gain value be if the effects of r_s were neglected?

(b) An alternative model for the transistor in which a current amplifier rather than a transconductance amplifier is used is shown in Fig. 1.19(c). What must the short-circuit current gain β be? Give both an expression and a value.

Solution

(a) Using the voltage-divider rule, we determine the fraction of input signal that appears at the amplifier outputs:

$$v_{\text{out}} = v_B \frac{r_o}{r_o + R_o} \quad (1.17)$$

Next we determine the output voltage v_o by multiplying the current $i_{o,k}$ by the resistance $(R_1 \parallel R_2)$:

$$v_o = -\beta_{oi} i_{o,k} (R_1 \parallel R_2) \quad (1.18)$$

Substituting for $i_{o,k}$ from Eq. (1.17) yields the voltage-gain expression:

$$\frac{v_o}{v_i} = -\frac{\beta_{oi}}{r_e + R_s} g_m (R_1 \parallel R_2) \quad (1.19)$$

Observe that the gain is negative, indicating that this amplifier is inverting. For the given component values,

$$\begin{aligned} \frac{v_o}{v_i} &= \frac{3.5}{2.5} \times 40 \times (5 \parallel 100) \\ &= -65.5 \text{ V/V} \end{aligned}$$

Neglecting the effect of r_o , we obtain

$$\begin{aligned} \frac{v_o}{v_i} &= \frac{2.5}{2.5 + 5} \times 40 \times 5 \\ &= -65.2 \text{ V/V} \end{aligned}$$

which is quite close to the value obtained accounting for r_o . This is for coupling since $r_o \gg R_s$.

On the model in Fig. 1.10b, α is equivalent to that in Fig. 1.19a:

$$\beta_{oi} = \mu_{oi} r_o$$

But $\beta_{oi} = r_{o,k}/r_{e,k}$ thus,

$$\beta = g_m r_o$$

For the values given,

$$\begin{aligned} \beta &= (17 \text{ mA/V}) \times 2.5 \text{ k}\Omega \\ &= 10.5 \text{ A/A} \end{aligned}$$

EXERCISES

1.37 Consider the common-emitter amplifier shown in Fig. 1.19a. If the input voltage is $v_i = 10 \text{ mV}$ and the output voltage is $v_o = -100 \text{ mV}$, calculate the overall voltage gain.

1.38 Consider the common-emitter amplifier whose circuit diagram is in Fig. 1.19a. If the input voltage signal v_i is connected to a voltage source R_s , having a resistance of $100 \text{ }\Omega$, and the output voltage v_o is connected to the ground rail, then what is the overall voltage gain?

$$\begin{aligned} v_o &= -\frac{\beta_{oi}}{r_e + R_s} (R_1 \parallel R_2) v_i \\ &= -\frac{10.5}{100 + 100} (5 \parallel 100) \times 10 \text{ mV} \\ &= -10.5 \text{ mV} \end{aligned}$$

1.19 Consider a transistor-based amplifier having the model shown in the third column of Table 1.1. Let the amplifier be fed with a current source i_s having a resistance R_s , and let the output be connected to a load resistance R_L . Suppose the overall gain is given by

$$\frac{v_o}{v_i} = \frac{\beta_{oi}}{R_s + R_L} \frac{R_1}{R_1 + R_2}$$

1.20 Calculate the magnitude of the open-loop gain, A_{OL} , the closed-loop gain, A_{CL} , the voltage gain, A_V , the output voltage, v_o , and the output current, i_o , for the circuit shown in Fig. 1.20. The values of the components are given in the figure.

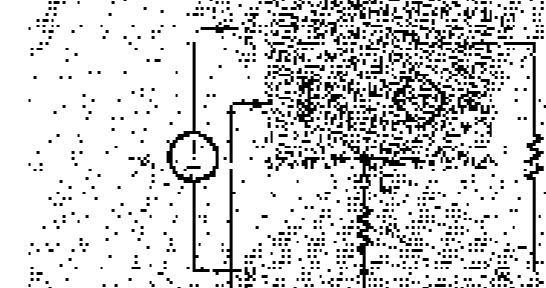


FIGURE 1.20

Answers to Odd-Numbered Problems

1.6 FREQUENCY RESPONSE OF AMPLIFIERS

From Section 1.2 we know that the input signal to an amplifier can always be expressed as the sum of sinusoidal signals. It follows that the important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies. Such a characterization of amplifier performance is known as the amplifier frequency response.

1.6.1 Measuring the Amplifier Frequency Response

We shall introduce the subject of amplifier frequency response by showing how it can be measured. Figure 1.20 depicts a linear voltage amplifier fed at its input with a sine wave signal of amplitude V_0 and frequency ω_0 . As the figure indicates, the signal measured at the output is

$$\begin{aligned} v_o &= V_0 \sin(\omega_0 t + \delta) \\ v_o &= V_0 \sin(\omega_0 t + \delta) \end{aligned}$$

FIGURE 1.20 Measuring the frequency response of a linear amplifier. At the test frequency ω_0 , the gain is characterized by its magnitude (V_o/V_i) and phase δ .

amplified output also is sinusoidal with exactly the same frequency as. This is an important point to note. Whenever a sine wave signal is applied to a linear circuit, the resulting output is sinusoidal with the same frequency as the input. In fact, the sine wave is the only signal that does not change shape as it passes through a linear circuit. Observe, however, that the output sinusoid will in general have a different amplitude and will be shifted in phase relative to the input. The ratio of the amplitude of the output sinusoid (V_o) to the amplitude of the input sinusoid (V_i) is the magnitude of the amplifier gain (or transmission) at the test frequency ω . Also, the angle ϕ is the phase of the amplifier transmission at the test frequency ω . If we denote the amplifier transmission, or transfer function as it is more commonly known, by $T(\omega)$, then

$$\begin{aligned} T(\omega) &= \frac{V_o}{V_i} \\ \angle T(\omega) &= \phi \end{aligned}$$

The response of the amplifier to a sinusoid of frequency ω is completely described by $|T(\omega)|$ and $\angle T(\omega)$. Now, to obtain the complete frequency response of the amplifier we simply change the frequency of the input sinusoid and measure the new value for $|T(\omega)|$ and $\angle T$. The end result will be a linear plot of gain magnitude $|T(\omega)|$ versus frequency and a table and/or graph of phase angle $\angle T(\omega)$ versus frequency. These two plots together can tell us the frequency response of the amplifier: the first is known as the **magnitude or amplitude response**, and the second is the **phase response**. Finally, we should mention that it is a common practice to express the magnitude of transmission in decibels and thus plot $20 \log |T(\omega)|$ versus frequency.

1.6.2 Amplifier Bandwidth

Figure 1.21 shows the magnitude response of an amplifier. It indicates that the gain is almost constant over a wide frequency range, roughly between ω_1 and ω_2 . Signals whose frequencies are below ω_1 or above ω_2 will experience lower gain, with the gain decreasing as we move further away from ω_1 and ω_2 . The band of frequencies over which the gain is the amplifier is often referred to within a certain number of decibels (usually 2 dB). It is called the **amplifier bandwidth**. Normally the amplifier is designed so that its bandwidth coincides with the spectrum of the signals it is required to amplify. If this were not the case, the amplifier would distort the frequency spectrum of the input signal, with different components of the input signal being amplified to different amounts.

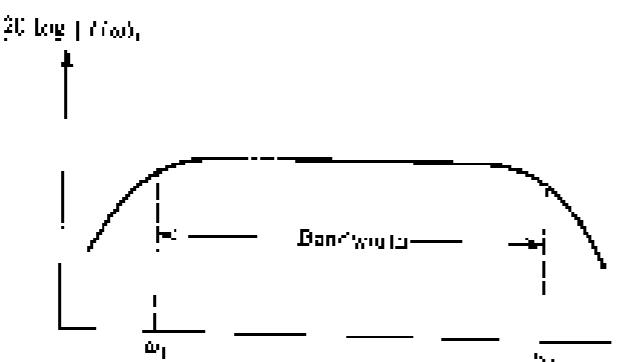


FIGURE 1.21 A schematic response of an amplifier. Note that magnitude of the output is greater than the ratio of the output $V_o(\omega)$ to the input $V_i(\omega)$.

1.6.3 Evaluating the Frequency Response of Amplifiers

Above, we described the method used to measure the frequency response of an amplifier. We now briefly discuss the method for analytically obtaining an expression for the frequency response. What we are about to say is just a preview of this important subject whose detailed study starts in Chapter 4.

To evaluate the frequency response of an amplifier one has to employ the amplifier equivalent circuit model, taking into account all reactive components.² Circuit analysis proceeds in the usual fashion, but with inductances and capacitances represented by their reactances. An inductance L has a resistance or impedance $j\omega L$, and a capacitance C has a resistance or impedance $1/j\omega C$ or, equivalently, a susceptance or admittance $j\omega C$. Thus in a *frequency-domain* analysis we deal with impedances and/or admittances. The result of the analysis is the **amplifier transfer function** $T(\omega)$:

$$T(\omega) = \frac{V_o(\omega)}{V_i(\omega)}$$

where $V_i(\omega)$ and $V_o(\omega)$ denote the input and output signals, respectively. $T(\omega)$ is generally a complex function whose magnitude $|T(\omega)|$ gives the magnitude of transmission, or the magnitude response of the amplifier. The phase of $T(\omega)$ gives the phase response of the amplifier.

In the analysis of a circuit to determine its frequency response, the algebraic manipulations can be considerably simplified by using the complex frequency variable s . In terms of s , the impedance of an inductance L is sL and that of a capacitance C is $1/sC$. Replacing the reactive elements with their impedances and performing standard circuit analysis, we obtain the transfer function $T(s)$:

$$T(s) = \frac{V_o(s)}{V_i(s)}$$

Subsequently, we replace s by $j\omega$ to determine the transfer function, or physical frequency, $T(j\omega)$. Note that $T(j\omega)$ is the same function we call $T(\omega)$ above;³ the additional $j\omega$ is included in order to emphasize that $T(j\omega)$ is obtained from $T(s)$ by replacing s with $j\omega$.

1.6.4 Single-Time-Constant Networks

In analyzing amplifier circuits to determine their frequency response, one is greatly aided by knowledge of the frequency response characteristics of single-time-constant (STC) networks. An STC network is one that is composed of, or can be reduced to, one reactive component (inductance or capacitance) and one resistance. Examples are shown in Fig. 1.22. An STC network formed of an inductance L and a resistance R has a time constant $\tau = L/R$. The time constant τ of an STC network composed of a capacitance C and a resistance R is given by $\tau = CR$.

Appendix D presents a study of STC networks and their responses to sinusoidal, step, and pulse inputs. Knowledge of this material will be needed at various points throughout this book, and the reader will be encouraged to refer to the Appendix. At this point we need in particular the frequency response results; we will, in fact, briefly discuss this important topic, now.

² Note that in the models considered up to now no transient components have been included. These were simplified models and cannot be used to predict the amplitude-frequency response.

³ At this stage, we are not up to simply analyzing the $T(j\omega)$. We will not yet be fully familiarized with complex analysis until Chapter 6. A brief review of *s*-plane analysis is presented in Appendix B.

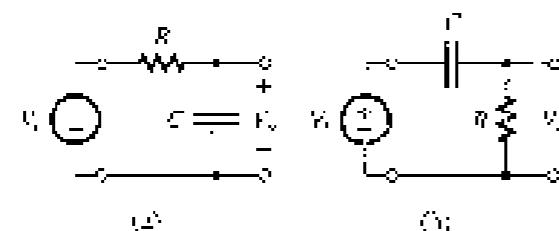


FIGURE 1.22 Two examples of STC networks: (a) a low-pass network and (b) a high-pass network.

TABLE 1.2 Frequency response of STC networks

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\frac{K}{1 + (s/\omega_0)}$	$\frac{Ks}{s + \omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\frac{K}{1 + j(\omega/\omega_0)}$	$\frac{Kj\omega}{j\omega + \omega_0}$
Magnitude Response, $ T(j\omega) $	$\frac{ K }{\sqrt{1 + (\omega/\omega_0)^2}}$	$\frac{ K }{\sqrt{1 + (\omega_0/\omega)^2}}$
Phase Response, $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dB)	K	0
Transmission at $\omega = \infty$	0	K
3-dB Frequency	$\omega_0 = 1/C; Y = \text{line conductance}$ $\omega = \sqrt{Y/C}$	
Time Plots	In Fig. 1.23	In Fig. 1.24

Most STC networks can be classified into two categories,² low-pass (LP) and high-pass (HP), with each of the two categories displaying distinctly different signal responses. As an example, the STC networks shown in Fig. 1.22(a) is of the low-pass type and that in Fig. 1.22(b) is of the high-pass type. To see the reasoning behind this classification, observe that the transfer function of each of these two circuits can be expressed as a voltage-divider ratio, with the divider composed of a resistor and a capacitor. Now, recalling how the impedance of a capacitor varies with frequency ($Z_C = 1/j\omega C$) it is easy to see that the transmission of the circuit in Fig. 1.22(a) will decrease with frequency and approach zero as ω approaches ∞ . Thus the circuit of Fig. 1.22(a) acts as a low-pass filter;³ it passes low-frequency sine-wave inputs with little or no attenuation (at $\omega = 0$, the transmission is unity) and attenuates high-frequency input sinusoids. The circuit of Fig. 1.22(b) does the opposite: its transmission is unity at $\omega = \infty$ and decreases as ω is reduced, reaching 0 by $\omega = 0$. The latter circuit, therefore, performs as a high-pass filter.

Table 1.2 provides a summary of the frequency response results for STC networks of both types.⁴ Also, sketches of the magnitude and phase responses are given in Figs. 1.23 and 1.24.

² An important exception is the all-pass STC network shown in Fig. 1.22(c).

³ A filter is a circuit that passes a signal in a specified frequency band (the passband) and severely attenuates (blocks) signals in another frequency band (the filter stopband). It has been studied in Chapter 13.

⁴ The transfer functions in Table 1.2 are given in general form. For the circuit of Fig. 1.22, $K = 1$ and $\omega_0 = 1/CR$.

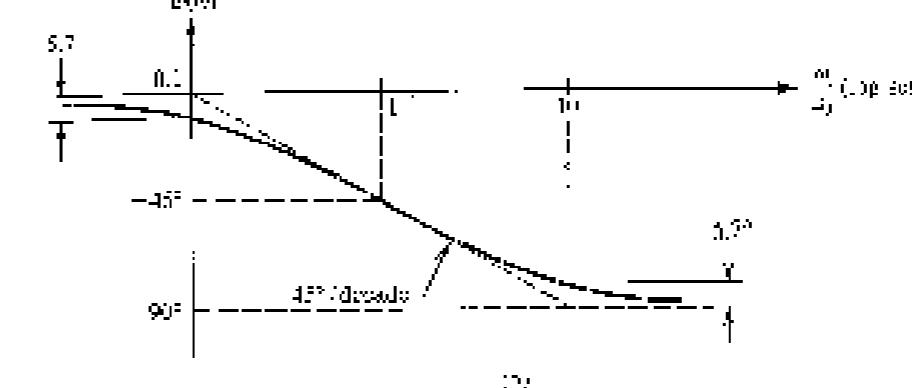
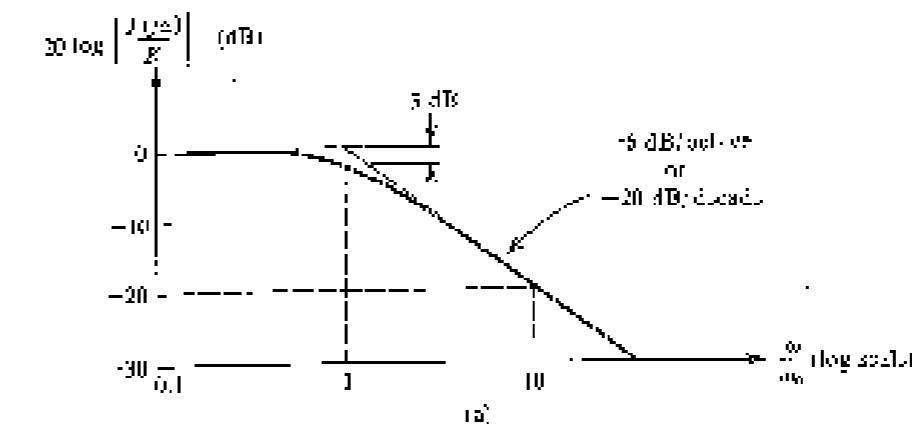


FIGURE 1.23 (a) Magnitude and (b) phase plots of the low-pass STC networks of the low-pass type.

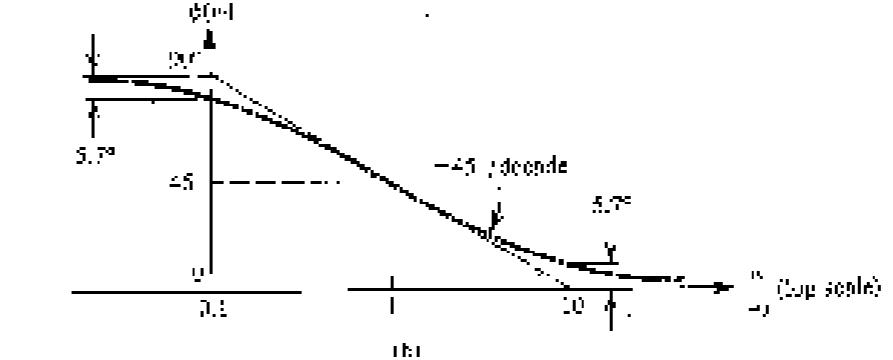
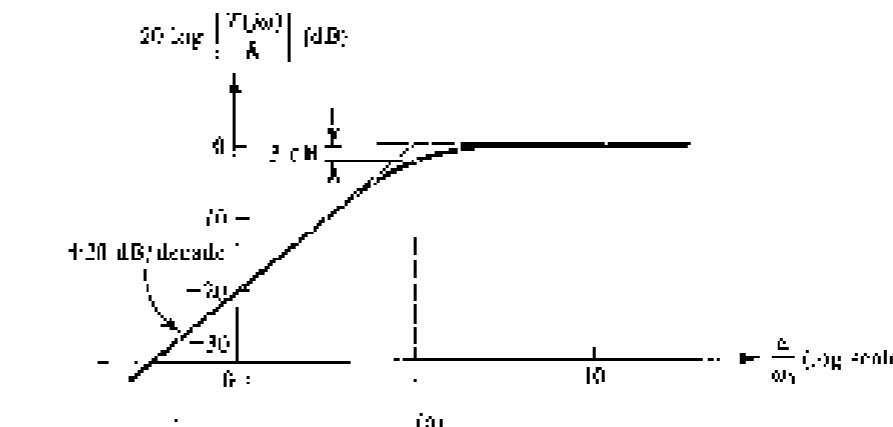


FIGURE 1.24 (a) Magnitude and (b) phase plots of the high-pass STC networks of the high-pass type.

These frequency-response diagrams are known as Bode plots and the 3-dB frequency (ω_0) is also known as the corner frequency or break frequency. The reader is urged to become familiar with this information and to consult Appendix D if further clarifications are needed. In particular, it is important to develop a facility for the rapid determination of the time constants of an STC circuit.



Figure 1.25 shows a voltage amplifier having an input resistance R_i , an input capacitance C_i , a gain factor μ , and an output resistance R_o . The amplifier is fed with a voltage source V_i having an output resistance R_s , and a load of resistance R_L is connected in the output.



FIGURE 1.25 Circuit for Example 1.5.

(a) Derive an expression for the amplifier voltage gain V_o/V_i as a function of frequency. From this find expressions for the dc gain and the 3-dB frequency.

(b) Calculate the values of the dc gain, the 3-dB frequency, and the frequency at which the gain becomes 0.1dB (i.e., unity). For the case $R_s = 20\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $C_i = 60\text{ pF}$, $\mu = 144\text{ V/V}$, $R_o = 200\text{ k}\Omega$, and $R_L = 1\text{ k}\Omega$.

(c) Find $v_o(t)$ for each of the following inputs:

- $v_i = 0.1 \sin 10^3 t \text{ V}$
- $v_i = 0.1 \sin 10^5 t \text{ V}$
- $v_i = 0.1 \sin 10^6 t \text{ V}$
- $v_i = 0.1 \sin 10^8 t \text{ V}$

Solution

(a) Utilizing the voltage-division rule, we can express V_o in terms of V_i as follows

$$V_o = V_i \frac{Z}{Z + R_o}$$

where Z is the amplifier input impedance. Since Z is composed of two parallel elements it is more easily easier to work in terms of $\Gamma = 1/Z$. Toward this end we divide the numerator and denominator by R_o , thus obtaining

$$\begin{aligned} V_o &= V_i \frac{1}{1 + R_o Y_i} \\ &= V_i \frac{1}{1 + R_o (1/R_i + K)} \end{aligned}$$

Thus,

$$\frac{V_o}{V_i} = \frac{1}{1 + (R_o/R_i) + K R_o}$$

This expression can be put in the standard form for a low-pass STC network (see the caption of Table 1.2) by extracting $[1 + (R_o/R_i)]$ from the denominator; thus we have

$$\frac{V_o}{V_i} = \frac{1}{1 + (R_o/R_i) + \frac{1}{K C_i (R_o R_i) / (R_o - R_i)}} \quad (1.20)$$

At the output side of the amplifier we can use the voltage-divider rule to write

$$V_o = A V_i \frac{R_o}{R_o + R_i}$$

This equation can be combined with Eq. (1.20) to obtain the amplifier transfer function as

$$\frac{V_o}{V_i} = \mu \frac{1}{1 + (R_o/R_i) + \frac{1}{1 + (R_o/R_i) + (R_o/R_i) (1 + (R_o/R_i) K)}} \quad (1.21)$$

We note that only the last term in this expression is new compared with the expression derived in the introduction. This factor is a result of the input capacitance C_i , with the time constant being

$$\begin{aligned} \tau &= C_i \frac{R_o K}{R_o - R_i} \\ &= C_i R_o / R_i \end{aligned} \quad (1.22)$$

We could have obtained this result by inspection: From Fig. 1.25 we see that the input circuit is an STC network and that its time constant can be found by reducing V_i to zero, with the result that the resistance seen by C_i is R_o , in parallel with R_i . The transfer function in Eq. (1.21) is of the form $K(1 + (R_o/R_i) + \Gamma)$, which corresponds to a low-pass STC network. The dc gain is found as

$$K = \frac{V_o}{V_i} (\gamma = 0) = \mu \frac{1}{1 + (R_o/R_i)} \frac{1}{1 + (R_o/R_i)} \quad (1.23)$$

The 3-dB frequency ω_0 can be found from

$$\omega_0 = \frac{1}{\tau} = \frac{1}{C_i (R_o R_i)} \quad (1.24)$$

Since the frequency response of the amplifiers of the low-pass STC type, the Bode plots for the gain, magnitude and phase ω , will take the form shown in Fig. 1.23, where K is given by Eq. (1.23) and ω_0 is given by Eq. (1.24).

(b) Substituting the measured values given into Eq. (1.23) results in

$$K = 14 \cdot \frac{1}{1 + (20/100)} \frac{1}{1 + (20/100)} = 100 \text{ V/V}$$

After the amplifier has a dc gain of 40 dB, Substituting the measured values into Eq. (1.24) gives the 3-dB frequency

$$\begin{aligned} \omega_0 &= \frac{1}{60 \text{ pF} \cdot (20 \times 100 \times 100 \text{ k}\Omega)} \\ &= \frac{1}{80 \times 10^{-12} \times 20 \times 100 \times (20 + 10^3) \times 10^3} = 10^5 \text{ rad/s} \end{aligned}$$

Thus,

$$\omega_0 = \frac{f_0}{2\pi} = 159.3 \text{ kHz}$$

Since the gain A_f is off at the rate of -20 dB/decade , starting at ω_0 (see Fig. 1.23a), the ratio A_f/A is two decades (or factor of 100) at this we have

$$\text{unity-gain frequency} = 100 \cdot \omega_0 = 10^5 \text{ rad/s or } 15.92 \text{ MHz}$$

(c) To find $v_o(s)$ we need to determine the gain margin (order of phase) at $10^2, 10^3, 10^4, \text{ and } 10^5 \text{ rad/s}$. This can be done either approximately utilizing the Bode plots of Fig. 1.23 or exactly utilizing the expression for the amplitude transfer function.

$$T(j\omega) = \frac{V_o}{V_i}(j\omega) = \frac{100}{1 + j(\omega/10^5)}$$

We shall do both:

(i) For $\omega = 10^2 \text{ rad/s}$, which is $(\omega_0/10)^2$, the Bode plots of Fig. 1.23 suggest that $|T| = K = 100$ and $\phi = -2^\circ$. The transfer function expression gives $|T| = 100$ and $\phi = -\tan^{-1} 10^{-4} = 0^\circ$. Thus,

$$v_o(s) = 13.92 \sin(10^2 s) V$$

(ii) For $\omega = 10^3 \text{ rad/s}$, which is $(\omega_0/10)^3$, the Bode plots of Fig. 1.23 suggest that $|T| = K = 100$ and $\phi = -5.7^\circ$. The transfer function expression gives $|T| = 90.5$ and $\phi = -\tan^{-1} 0.1 = -5.7^\circ$. Thus,

$$v_o(s) = 9.05 \sin(10^3 s) V$$

(iii) For $\omega = 10^4 \text{ rad/s} = \omega_0/2 = 100 \sqrt{2} = 70.7 \text{ rad/s}$ or 37 dB and $\phi = -45^\circ$. Thus,

$$v_o(s) = 7.07 \sin(10^4 s) V$$

(iv) For $\omega = 10^5 \text{ rad/s}$, which is $(100\omega_0)$, the Bode plots suggest that $|T| = 1$ and $\phi = -90^\circ$. The transfer function expression gives

$$T = 1 \quad \text{and} \quad \phi = -\tan^{-1} 0.01 = 90.4^\circ.$$

Thus,

$$v_o(s) = 0.1 \sin(10^5 s) V$$

1.6.5 Classification of Amplifiers Based on Frequency Response

Amplifiers can be classified based on the shape of the magnitude response curve. Figure 1.26 shows typical frequency response curves for various amplifier types. In Fig. 1.26(a) the gain remains constant over a wide frequency range but falls off at low and high frequencies. This is a common type of frequency response found in audio amplifiers.

As will be shown in later chapters, internal capacitances in the device (a transistor's case) the fall-off of gain at high frequencies, just as C_d did in the circuit of Example 1.5. On the other hand, the fall-off of gain at low frequencies is usually caused by coupling capacitors used to connect one amplifier stage to another, as indicated in Fig. 1.27. This practice is usually adopted to simplify the design process of the different stages. The coupling capacitors are usually also quite large (in terms of a microfarad or a few tens of microfarads) so that their resistance (impedance) is small at the frequencies of interest. Nevertheless, at sufficiently low frequencies the reactance of a coupling capacitor will become large enough to cause part of the signal being coupled to appear as a voltage drop across the coupling capacitor and thus not reach the subsequent stage. Coupling capacitors will thus cause loss of gain at low frequencies and cause the gain to be zero at dc. This is not at all surprising since from Fig. 1.27 we observe that the coupling capacitor, acting together with the input resistance of the subsequent stage, forms a

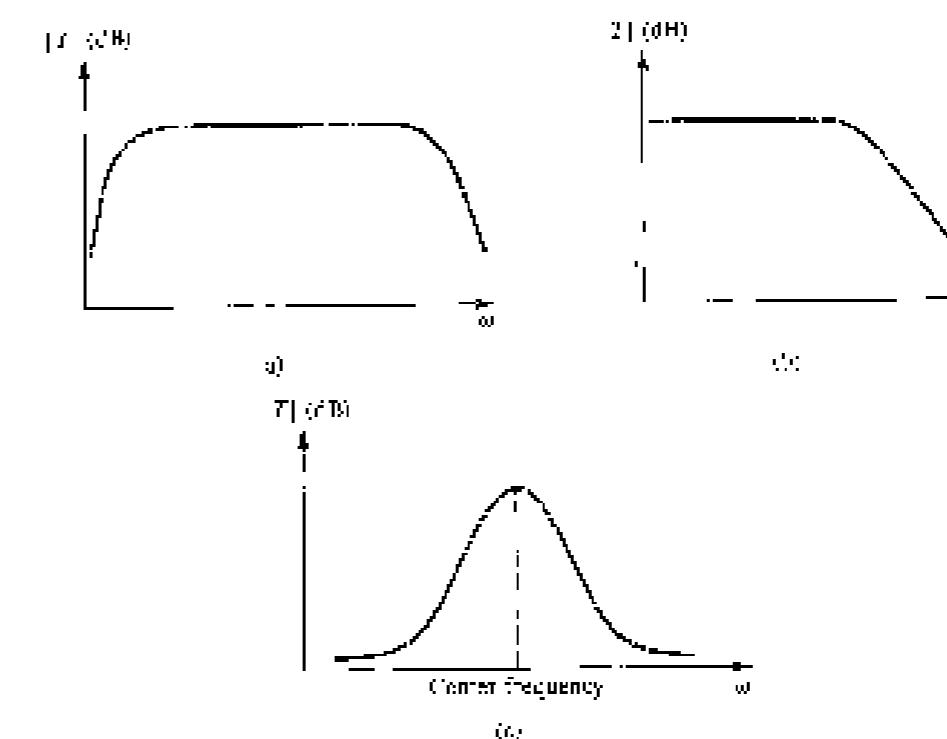


FIGURE 1.26 Frequency response for (a) a passive coupled amplifier, (b) a direct-coupled amplifier, and (c) a tuned audio-frequency amplifier.

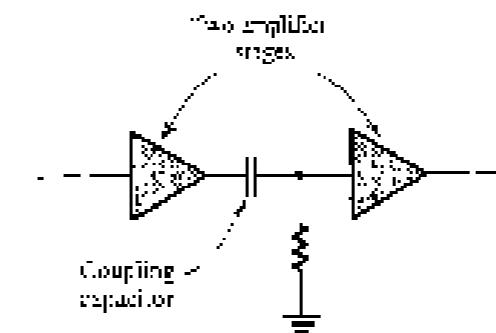


FIGURE 1.27 Use of a cascaded-multiple-stage amplifier.

high-pass RC circuit. It is the frequency response of this high-pass circuit that accounts for the shape of the amplifier frequency response in Fig. 1.26(a) at the low-frequency end.

There are many applications in which it is important that the amplifier maintains its gain at low frequencies down to dc. Furthermore, monolithic integrated-circuit (IC) technology does not allow the fabrication of large coupling capacitors. Thus IC amplifiers are usually designed as directly coupled or dc amplifiers (as opposed to capacatively coupled or ac amplifiers). Figure 1.26(b) shows the frequency response of a dc amplifier. Such a frequency response characterizes what is referred to as a low-pass amplifier.

In a number of applications, such as in the design of radio and TV receivers, the need arises for an amplifier whose frequency response peaks around a certain frequency (called the center frequency) and falls off on both sides of this frequency, as shown in Fig. 1.26(c).

Amplifiers with such a response are called tuned amplifiers, bandpass amplifiers, or bandpass filters. A tuned amplifier forms the heart of the front-end or tuner of a communication receiver; by adjusting its center frequency to coincide with the frequency of a desired communications channel (e.g., a radio station), the signal of this particular channel can be received while those of other channels are attenuated or filtered out.

EXERCISES

- E1.21 Consider a voltage-controlled voltage-controlled oscillator (VCO) with a gain of 1000 and a 2-pole low-pass filter with corner frequencies of 100 Hz, 10 kHz, 100 kHz, 300 kHz, and 1 MHz.

Ans: 60 dB, 4.25 rad/s, 20 dB, 8 dB

- E1.22 Consider a two-stage voltage-controlled oscillator (VCO) with a total gain of 100000 and a 2-pole low-pass filter with corner frequencies of 100 Hz, 10 kHz, 100 kHz, 300 kHz, and 1 MHz. If the amplitude of the second stage is given by $V_2 = V_1 \cdot 10^4 \cdot \sin(2\pi f t)$, determine the value of f for which the second stage has a minimum output voltage of at least 10% of its maximum value. Hint: The highest value that V_2 can attain is 100000 times the maximum value of V_1 , which is 100000 times the value of V_{100} .

- E1.23 Consider the oscillator circuit shown in Fig. E1.23. Let the output resistance of the first voltage-controlled oscillator (VCO) be $R_1 = 100 \Omega$. Sketch the small-signal representation of the second voltage-controlled oscillator (VCO), including the resistive load R_2 . The resulting equivalent circuit is shown in Fig. E1.24, where V_{100} is the common voltage control voltage, $V_{100} = V_{1001} + V_{1002}$, and V_{1001} is the output voltage of the second voltage-controlled oscillator (VCO). Compute the phase shift $\Delta\phi$ between the outputs of the two voltage-controlled oscillators. Assume $V_{1001} = 0$ V. Is it a high-pass SLC oscillator? What can be suggested about the potential feature that the oscillator exhibits at low frequencies?



FIGURE E1.23

1.7 DIGITAL LOGIC INVERTERS⁷

The logic inverter is the most basic element in digital circuit design; it plays a role parallel to that of the amplifier in analog circuits. In this section we provide an introduction to the logic inverter.

1.7.1 Function of the Inverter

As its name implies, the logic inverter inverts the logic value of its input signal. Thus for a logic 0 input, the output will be a logic 1, and vice versa. In terms of voltage levels, consider

⁷If a detailed study of this section can be postponed to us, before study of the CMOS inverter (see Section 4.10).

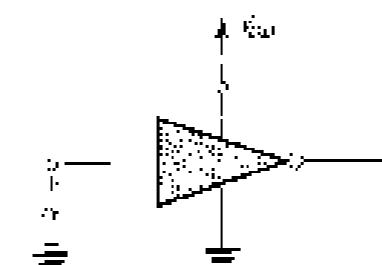


FIGURE 1.28 A typical inverter using an op-amp.

the inverter shown in black form in Fig. 1.28. When v_i is low (close to 0 V), the output v_o will be high (close to V_{DD}), and vice versa.

1.7.2 The Voltage Transfer Characteristic (VTC)

To quantify the operation of the inverter, we utilize its voltage transfer characteristic (VTC), as it is usually abbreviated. First we refer the reader to the amplifier considered in Example 1.2 whose transfer characteristic is sketched in Fig. 1.15. Observe that the transfer characteristic indicates that this inverting amplifier can be used as a logic inverter. Specifically, if the input is high ($v_i > 0.95$ V), v_o will be low (0.1 V). On the other hand, if the input is low (v_i close to 0 V), the output will be high (v_o close to 10 V). Thus to use this amplifier as a logic inverter, we utilize its extreme regions of operation. This is exactly the reasoning for its use as a signal amplifier, where it would be biased in the middle of the transfer characteristic, and the signal kept sufficiently small so as to restrict operation to a short, almost linear segment of the transfer curve. Digital applications, on the other hand, make use of the gross nonlinearity exhibited by the VTC.⁸

With these observations in mind, we show in Fig. 1.29 a possible VTC of a logic inverter. For simplicity, we are using three straight lines to approximate the VTC, which is really a nonlinear curve such as that in Fig. 1.15. Observe that the output high level,

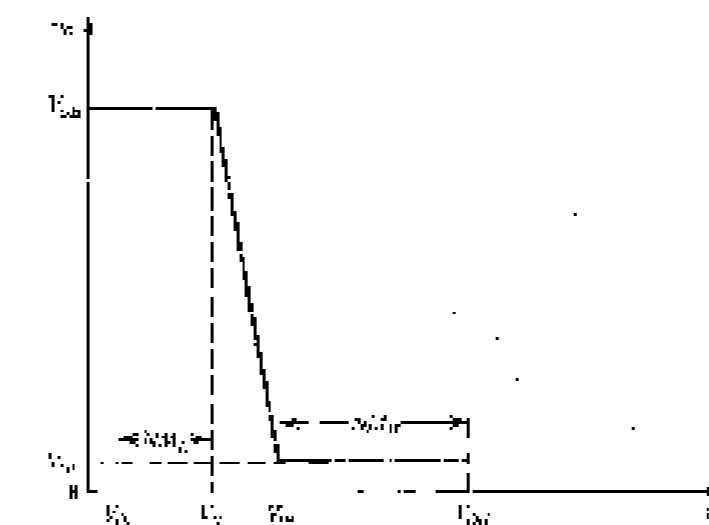


FIGURE 1.29 Voltage transfer characteristic of an inverter. The VTC is approximated by three straight-line segments. Note the logic parameters of the VTC (V_{OH} , V_{OL} , V_{L1} , and V_{L2}) and width of determining the noise margins (ΔV_{OL} and ΔV_{OL}).

denoted V_{OL} , does not depend on the exact value of v_1 as long as v_1 does not exceed the voltage labeled V_{IL} , where v_1 exceeds V_{IL} , the output decreases and the inverter enters its amplification region of operation, also called the transition region. It follows that V_{IL} is an important parameter of the inverter VTC. It is the minimum value that v_1 can have while being interpreted by the inverter as representing a logic 0.

Similarly, we observe that the output low level, denoted V_{OL} , does not depend on the exact value of v_1 as long as v_1 does not fall below V_{IH} . Thus, V_{IH} is an important parameter of the inverter VTC. It is the maximum value that v_1 can have while being interpreted by the inverter as representing a logic 1.

1.7.3 Noise Margins

The insensitivity of the inverter output to the exact value of v_1 within allowed regions is a great advantage that digital circuits have over analog circuits. To quantify this insensitivity property, consider the situation that occurs often in a digital system where an inverter (or a logic gate based on the inverter circuit) is driving another similar inverter. If the output of the driving inverter is high at V_{OH} , we see that we have a "margin of safety" equal to the difference between V_{OH} and V_{IH} (see Fig. 1.29). In other words, if for some reason a disturbing signal (called "noise voltage," or simply noise) is superimposed on the output of the driving inverter, the driven inverter would not be "bedazzled" so long as the noise does not decrease the voltage at its input below V_{IH} . Thus we can say that the inverter has a noise margin for high input, NM_H , of

$$NM_H = V_{OH} - V_{IH} \quad (1.25)$$

Similarly, if the output of the driving inverter is low at V_{OL} , the driven inverter will provide a high output even if noise corrupts the V_{OL} level slightly, raising it up to nearly V_{OH} . Thus we can say that the inverter exhibits a noise margin for low input, NM_L , of

$$NM_L = V_{OL} - V_{IH} \quad (1.26)$$

In summary, four parameters, V_{OH} , V_{OL} , V_{IH} , and V_{IL} , define the VTC of an inverter and determine its noise margins, which can quantitatively measure the ability of the inverter to tolerate variations in the input signal levels. In this regard, observe that changes in the input signal level within the noise margins are rejected by the inverter. That noise is not allowed to propagate further through the system, is a definite advantage of digital over analog circuits. Alternatively, we can think of the inverter as restoring the signal levels to standard values (V_{OH} and V_{OL}) even when it is presented with corrupted signal levels (within the noise margins). As a summary, useful for future reference, we present a listing of the definitions of the important parameters of the inverter VTC in Table 1.3.

TABLE 1.3 Important Parameters of the Inverter VTC

V_{IL}	Output low level
V_{IH}	Output high level
V_{IOH}	Maximum value of v_2 interpreted by the inverter as a logic 0
V_{IOL}	Minimum value of v_1 interpreted by the inverter as a logic 1
NM_H	Noise margin for high input = $V_{OH} - V_{IH}$
NM_L	Noise margin for low input = $V_{OL} - V_{IH}$

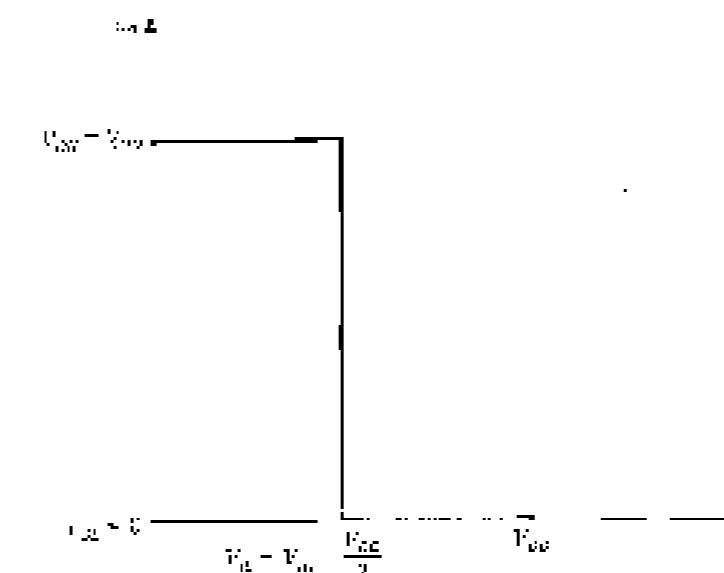


FIGURE 1.30 The VTC of an ideal inverter.

1.7.4 The Ideal VTC

The question naturally arises as to what constitutes an ideal VTC for an inverter. The answer follows directly from the preceding discussion. An ideal VTC is one that maximizes the noise margins and distributes them equally between the low and high input regions. Such a VTC is shown in Fig. 1.30 for an inverter operated from a dc supply V_{DD} . Observe that the output high level, V_{OH} , is at its maximum possible value of V_{DD} , and the output low level is at its minimum possible value of 0 V. Observe also that the threshold voltages V_{IL} and V_{IH} are equalized and placed in the middle of the power supply voltage ($V_{DD}/2$). Thus the width of the transition region between the high and low output regions has been reduced to zero. The transition region, though obviously very important in amplifying applications, is of no value in digital circuits. The ideal VTC exhibits a steep transition at the threshold voltage $V_{DD}/2$ with the gain in the transition region being infinite. The noise margins are now equal:

$$NM_H = NM_L = V_{DD}/2 \quad (1.27)$$

We will see in Chapter 4 that inverter circuits designed using the complementary metal-oxide semiconductor (CMOS) technology come very close to realizing the ideal VTC.

1.7.5 Inverter Implementation

Inverters are implemented using transistors (Chapters 4 and 5) operating as voltage-controlled switches. The simplest inverter implementation is shown in Fig. 1.31. The switch is controlled by the inverter input voltage v_1 . When v_1 is low, the switch will be open and $v_2 = V_{DD}$ since no current flows through R . When v_1 is high, the switch will be closed and, assuming an ideal switch, $v_2 = 0$.

Transistor switches, however, as we will see in Chapters 4 and 5, are not perfect. Although their off resistances are very high and thus an open switch closely approximates

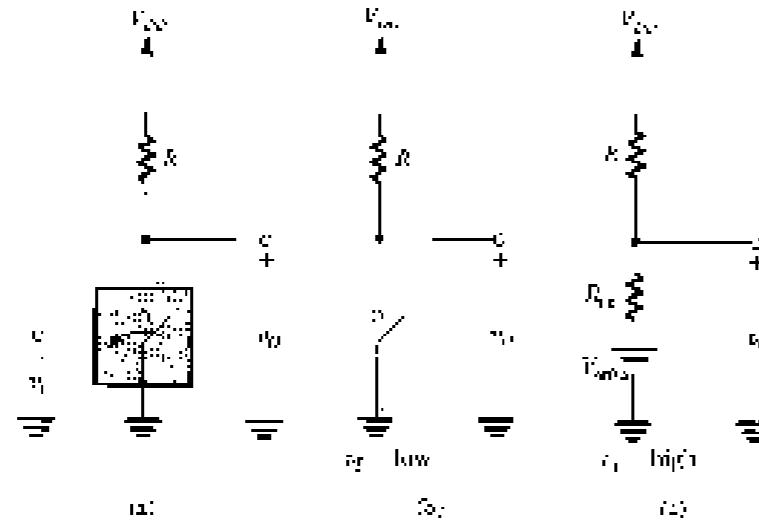


FIGURE 1.31 (a) The simplest implementation of a logic inverter using a voltage-controlled switch; (b) equivalent circuit when v_2 is low; (c) equivalent circuit when v_1 is high. Note that the switch is "closed" to close when v_2 is high.

An open circuit, the "on" switch is a finite closure or "on" resistance, R_{on} . Furthermore, some switches (e.g., those implemented using bipolar transistors; see Chapter 5) exhibit an additional "off" voltage, V_{off} . The result is that when v_1 is high, the inverter has the equivalent circuit shown in Fig. 1.31(c), from which V_{DD} can be found:

More elaborate implementations of the logic inverter exist, and we show two of these in Figs. 1.32(a) and 1.32(b). The circuit in Fig. 1.32(a) utilizes a pair of complementary switches, the "pull-up" (PU) switch connects the output node to V_{DD} , and the "pull-down" (PD) switch connects the output node to ground. When v_2 is low, the PU switch will be

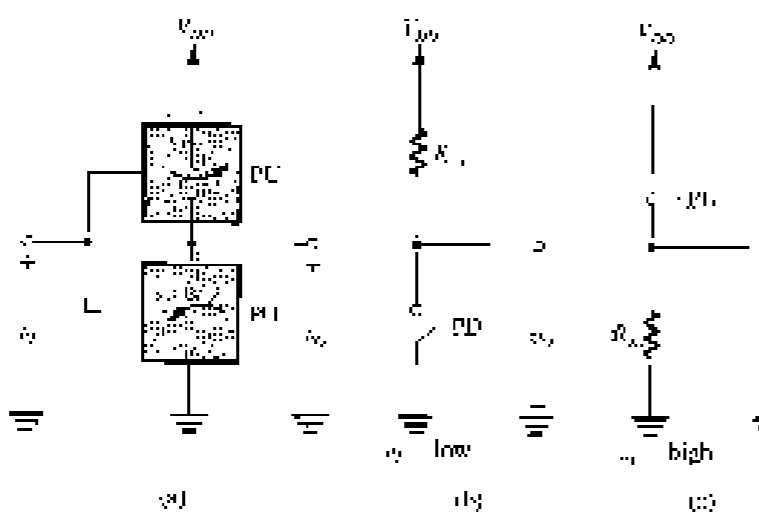


FIGURE 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 4.10.

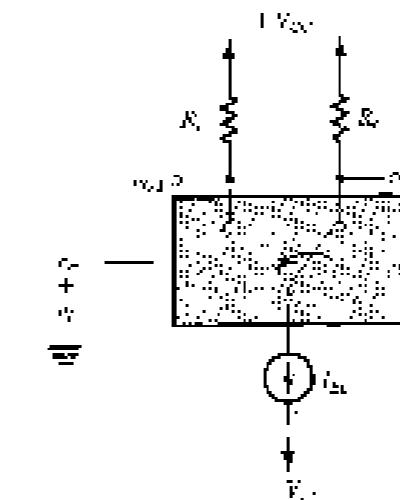


FIGURE 1.33 A digital inverter implementation using a double-throw switch to steer the constant current I_{DQ} . When v_2 is high, $v_0 = V_{DD}$; when v_2 is low, $v_0 = 0$. This is the basis of the emitter-coupled logic (ECL) studied in Chapters 7 and 11.

closed and the PU switch open, resulting in the equivalent circuit of Fig. 1.32(a). Observe that in this case R_{on} of the PU connects the output to V_{DD} , thus establishing $V_{DD} = V_{DD}$. Also observe that no current flows and thus no power is dissipated in the circuit. Next, if v_2 is raised to the logic 1 level, the PU switch will open while the PD switch will close, resulting in the equivalent circuit shown in Fig. 1.32(c). Here R_{on} of the PD switch connects the output to ground, thus establishing $V_{DD} = 0$. Here again no current flows, and no power is dissipated. The superiority of this implementation over that using the single pull-down switch and a resistor (known as a pull-up resistor) should be obvious. This circuit constitutes the basis of the CMOS inverter that we will study in Section 4.10. Note that we have not included offset voltages in the equivalent circuits because MOS switches do not exhibit a voltage offset (Chapter 3).

Finally, consider the inverter implementation of Fig. 1.31. Here a double-throw switch is used to steer the constant current I_{DQ} into one of two resistors connected to the positive supply V_{DD} . The reader is urged to show that if a high v_2 results in the switch being connected to R_{on} , the logic inversion function is realized at v_0 . Note that the output voltage is independent of the switch resistance. This current steering or current-scoupled logic arrangement is the basis of the fastest available digital logic circuits, called emitter-coupled logic (ECL), introduced in Chapter 7 and studied in Chapter 11.

1.2.5 Power Dissipation

Digital systems are implemented using very large numbers of logic gates. For space and other economic considerations, it is desirable to implement the system with as few integrated circuit (IC) chips as possible. It follows that one must pack as many logic gates as possible on an IC chip. At present, 100,000 gates or more can be fabricated on a single IC chip in what is known as very-large-scale integration (VLSI). To keep the power dissipated in the chip in acceptable limits (imposed by thermal considerations), the power dissipation per gate must be kept to a minimum. Indeed, a very important performance measure of the logic inverter is the power it dissipates.

The simple inverter of Fig. 1.31 obviously dissipates no power when v_2 is low and the switch is open. In the other case, however, the power dissipation is approximately V_{DD}^2/R and can be substantial. This power dissipation occurs even if the inverter is not switching

and is thus known as static power dissipation. The inverter of Fig. 1.52 exhibits no static power dissipation, a definite advantage. Unfortunately, however, another component of power dissipation arises when a capacitance exists between the output node of the inverter and ground. This is always the case, for the devices that implement the switches have internal capacitance, the wires that connect the inverter output to other circuits have capacitance, and, of course, there is the input capacitance of whatever circuit the inverter is driving. Now, as the inverter is switched from one state to another, current must flow through the switches to charge (and discharge) the total capacitance. These currents give rise to power dissipation in the switches, called dynamic power dissipation. In Chapter 4, we shall study dynamic power dissipation in the CMOS inverter, and we shall show how an inverter switched at a frequency f Hz exhibits a dynamic power dissipation:

$$P_{\text{diss}} = fCV_{\text{DD}}^2 \quad (1.23)$$

where C is the capacitance between the output node and ground and V_{DD} is the power-supply voltage. This result applies (approximately) to all inverter circuits.

1.7.7 Propagation Delay

Whether the dynamic behavior of amplifiers is specified in terms of their frequency response, that of inverters is characterized in terms of the time delay between switching of v_i from low to high or vice versa and the corresponding change appearing at the output. Such a delay, called propagation delay, arises for two reasons. The transistors that implement the switches exhibit finite (nonzero) switching times, and the capacitance that is inevitably present between the inverter output node and ground needs to charge (or discharge, as the case may be) before the output reaches its required level of V_{DD} or 0 . We shall analyze the inverter switching times in subsequent chapters. Such a study depends on a thorough familiarity with the time response of single-time-constant (SIC) circuits. A review of this subject is presented in Appendix D. For our purposes here, we remind the reader of the key equation in determining the response to a step function:

Consider a step function input applied to an SIC network after the low-pass or high-pass type, and let the network have a time constant τ . The output steady-state is given by

$$v(t) = Y_u - (Y_u - Y_s)e^{-t/\tau} \quad (1.24)$$

where Y_u is the final value, that is, the value toward which the response is heading, and Y_s is the value of the response immediately after $t = 0$. This equation states that the output at any time $t > 0$ is equal to the difference between the final value Y_u and a gap whose initial value is $Y_u - Y_s$, and that is shrinking exponentially.

Consider the inverter of Fig. 1.51(a) with a capacitor $C = 10 \text{ pF}$ connected between the output and ground. Let $V_{\text{DD}} = 5 \text{ V}$, $R = 1 \text{ k}\Omega$, $R_s = 100 \text{ }\Omega$, and $V_{\text{DDH}} < 0.1 \text{ V}$. If at $t = 0$, v_i goes low and neglecting the delay time of the switch, that is, assuming that it opens immediately, find the time for the output to reach $\frac{1}{2}(V_{\text{DD}} - V_{\text{DDH}})$. The time to this 50% point on the output waveform is defined as the low-to-high propagation delay, τ_{PHL} .

Solution

First we determine V_{DDH} , which is the voltage of the output prior to $t = 0$. From the equivalent circuit in Fig. 1.21(b), we find

$$\begin{aligned} V_{\text{DDH}} &= V_{\text{DD}} + \frac{V_{\text{DD}} - V_{\text{DDH}}}{R + R_{\text{on}}} R_{\text{on}} \\ &= 5 + \frac{5 - 0.1}{1 + 1} \times 0.1 = 0.55 \text{ V} \end{aligned}$$

Next, when the switch opens at $t = 0$, the circuit takes the form shown in Fig. 1.54(a). Since the voltage across the capacitor cannot change instantaneously, at $t = 0$ the output will sit at 0.55 V.

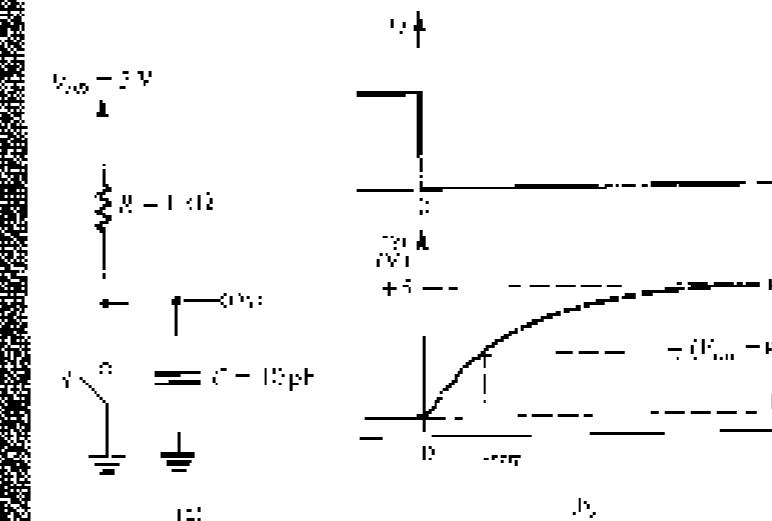


FIGURE 1.54 Example 1.56: (a) The inverter circuit after the switch opens ($t = 0$); (b) Waveforms of v_i and v_{out} . Observe that the switch is assumed to open instantaneously, that is, v_i drops to V_{DDH} and heading toward V_{DD} .

Now the capacitor charges through R_s and r_s toward V_{DD} . The output waveform will be as shown in Fig. 1.54(b), and its equation can be obtained by substituting in Eq. 1.24. Let $v_i = 0$ and $v_{\text{out}}(0) = 0.55 \text{ V}$. Thus,

$$v_{\text{out}}(t) = 5 - 5 + 0.55 e^{-t/\tau}$$

where $\tau = CR$. To find τ_{PHL} , we substitute

$$\begin{aligned} v_{\text{out}}(t_{\text{PHL}}) &= \frac{1}{2}(V_{\text{DD}} + V_{\text{DDH}}) \\ &= \frac{1}{2}(5 + 0.55) \end{aligned}$$

The result is

$$\begin{aligned} t_{\text{PHL}} &= 0.69\tau \\ &= 0.69RC \\ &= 0.69 \times 10^3 \times 10^{-10} \\ &= 6.9 \text{ ns} \end{aligned}$$

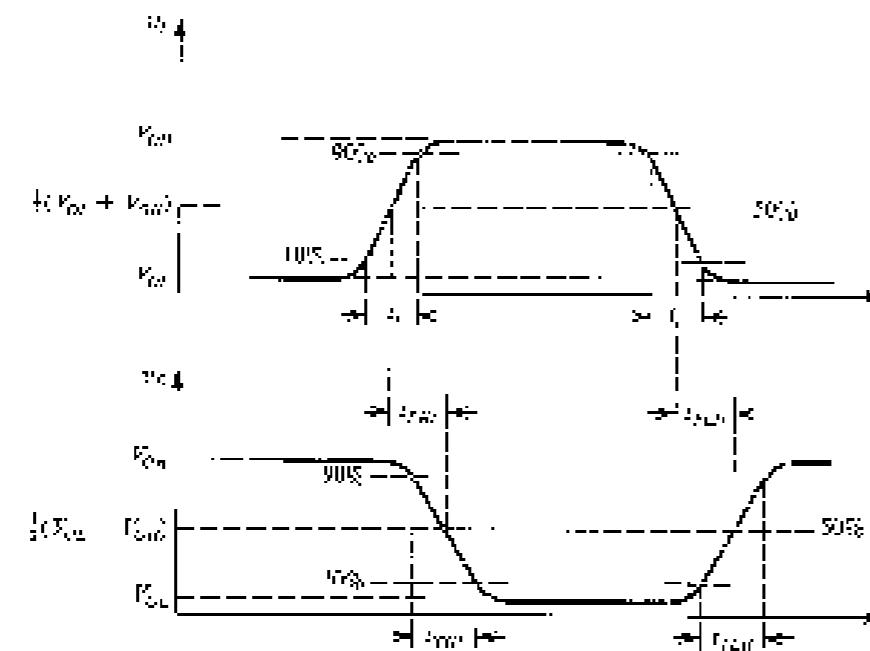


FIGURE 1.35 10-million-e-propagation delays and transition times of the logic inverter.

We conclude this section by showing in Fig. 1.25 the formal definition of the propagation delay of an inverter. As shown, an input pulse with finite (nonzero) rise and fall times is applied. The inverted pulse at the output exhibits finite rise and fall times (labeled t_{R90} and t_{F90} , where the subscript 90% denotes transition, LH denotes low-to-high, and HL denotes high-to-low). There is also a delay time between the input and output waveforms. The usual way to specify the propagation delay is to take the average of the high-to-low propagation delay, t_{PHL} , and the low-to-high propagation delay, t_{PLH} . As indicated, these delays are measured between the 10% points of the input and output waveforms. Also note that the transition times are specified using the 10% and 90% points of the output (denoted $V_{out} = 10\%$ and $V_{out} = 90\%$).

EXERCISES

- 1.24. For the inverter of Fig. 1.23, if $V_{DD} = 12\text{V}$ and $\pm 10\%$ is the supply voltage range, calculate t_{PLH} and t_{PHL} assuming steady-state power dissipation assuming that the inverter is dissipating 10 mW at 100% duty cycle.
- Ans. 2.5 ns
- 1.25. Find the output power dissipated in an inverter operating from a 5-V power supply. The inverter has a 2-pF capacitive load and is supplied at 50 MHz.
- Ans. 2.5 mW

1.8 CIRCUIT SIMULATION USING SPICE

The use of computer programs to simulate the operation of electronic circuits has become an essential step in the circuit design process. This is especially the case for circuits that are to be fabricated in integrated circuit form. However, even circuits that are assembled on a printed-circuit board using discrete components can and do benefit from circuit simulation. Circuit simulation enables the designer to verify that the design will meet specifications when actual components (with their many imperfections) are used, and it can also provide additional insight into circuit operation allowing the designer to fine-tune the final design prior to fabrication. However, notwithstanding the advantages of computer simulation, it is not a substitute for a thorough understanding of circuit operation. It should be performed only at a later stage in the design process and, most certainly, after a paper-and-pencil design has been done.

Among the various circuit-simulation programs available for the computer-aided numerical analysis of microelectronic circuits, SPICE (Simulation Program with Integrated Circuit Emphasis) is generally regarded to be the most widely used. SPICE is an open-source program which has been under development by the University of California at Berkeley since the early 1970s. PSpice is a commercial personal-computer version of SPICE that is now commercially available from Cadence. Also available from Cadence is PSpice A/D—an advanced version of PSpice that can model the behavior and, hence, simulate circuits that process both analog and digital signals.⁵ SPICE was originally a text-based program. The user had to describe the circuit to be simulated and the type of simulation to be performed using an input text file called a netlist. The simulation results were also displayed as text. As an example of more recent developments, Cadence provides a graphical interface called OrCAD Capture CIS (Component Information System) for circuit-schematic entry and editing. Such graphical interface tools are referred to in the literature as schematic editor, schematic editor, or schematic capture tools. Furthermore, PSpice A/D includes a graphical postprocessor, called Probe, to numerically analyze and graphically display the results of the PSpice simulations. In this text, "using PSpice" or "using SPICE" loosely refers to using Capture CIS, PSpice A/D, and Probe to simulate a circuit and to numerically analyze and graphically display the simulation results.

An evaluation (student) version of Capture CIS and PSpice A/D are included on the CD accompanying this book. These correspond to the OrCAD Family Release 9.2 (sic) (student level—also from Cadence). Furthermore, the circuit diagrams entered in Capture CIS (called Capture Schematics) and the corresponding PSpice simulation files (.circuit SPICE examples in this book) can be found on the text's CD and website (www.cadencetech.org). Access to these files will allow the reader to undertake further experimentation with these circuits, including investigating the effect of changing component values and operating conditions.

It is not our objective in this book to teach the reader how SPICE works nor the intricacies of using it effectively. This can be found in the SPICE books listed in Appendix B. Our objective in the sections of this book devoted to SPICE (usually the last section of each chapter) is twofold: to describe the models that are used by SPICE to represent the various electronic devices, and to illustrate how useful SPICE can be in investigating circuit operation.

⁵ Such circuits are called mixed-signal circuits, and the simulation programs that can simulate such circuits are called mixed-signal simulators.

SUMMARY

- A dc-biased signal source can be represented in a circuit by V_{DC} , a current source I_{DC} , or a voltage source with a source resistance R_s in series with the source. In a dependent source, I_s is in parallel with a source resistance R_s . The Thévenin voltage (V_{TH}) is open-circuit voltage between the source terminals equal to the Norton current (I_N) is equal to the short-circuit current between the source terminals. For the two resistors, Δ is equivalent, $\Delta = R_s$.
- The sine wave signal is completely characterized by its peak value (amplitude), A (the peak $\sqrt{2}$), its frequency (f), its reactance ($X_L = 2\pi f L$ or $X_C = 1/(2\pi f C)$ where L is the inductance in Henrys, and C is the capacitance in Farads), and its phase with respect to an arbitrary reference time.
- A signal can be represented either by its waveform versus time, or as the sum of sinusoids. This latter representation is known as the frequency spectrum of the signal.
- Analog signals have magnitudes that can assume any value. Discrete circuits that process analog signals are called analog circuits. Sampling the magnitude of an analog signal at discrete intervals of time and representing each signal sample by a number results in a digital signal. Digital signals are processed by digital circuits.
- The simplest digital signals are obtained when the binary system is used. An individual digital signal then assumes one of only two possible values: low and high (say, 0V and $\pm V$, corresponding to logic 0 and logic 1, respectively).
- An analog-to-digital converter (ADC) provides a digital output of the digits of the binary number representing the analog signal sample applied to its input. The output digital signal can then be processed by logic circuits. Refer to Fig. 1.13 and Fig. 1.12.
- The transfer characteristic, i_o versus v_o , is often a straight line with a slope equal to the voltage gain. Refer to Fig. 1.11.
- Amplifiers increase the signal power and thus require dc power supplies for their operation.
- The amplifier voltage gain can be expressed as a ratio A_v in Np/V or in dBs, $20 \log |A_v|$ dB. Similarly, for current gain, A_i , A_i/A_{in} or $20 \log |A_i|$ dB. For power gain, A_p , W/W or $10 \log |A_p|$ dB.
- Linear amplification can be obtained from a device having a linear transfer characteristic, by connecting it in biasing and keeping the input signal an ac voltage well. Refer to Fig. 1.12.
- Depending on the signal to be amplified (voltage or current) and on the desired range of amplitude and frequency, we

choose when the inverter is switched and has a capacitor load. The total power dissipation is given approximately by $P = V_{DD}^2$.

- An inverter's important performance parameter is t_{PD} versus its propagation delay (see Fig. 1.6 for definition).

PROBLEMS 1.2

CIRCUIT BASICS

As a review of the basics of circuit analysis and in order to become familiar with their importance for the study of electronic circuits, this section presents a number of easy circuit analysis problems. For a summary of Thévenin's and Norton's theorems, refer to Appendix D. The problems are grouped in appropriate categories.

RESISTORS AND OHM'S LAW

1.1 Ohm's law relates V to I for a resistor. For each of the resistors, follow the first dictum given:

- (a) $V = 1.123$, $I = 11$ V
- (b) $V = 10$ V, $I = 1$ mA
- (c) $R = 10\,k\Omega$, $I = 10$ mA
- (d) $R = 100\,k\Omega$, $V = 10$ V

1.2 Measurements indicate various resistors breakdown below V_{BD} . Calculate the power dissipated in the resistor and the power rating necessary for safe operation using standard components with power ratings of 0.25 W, $1/4$ W, $1/2$ W, 1 W, or 2 W.

- (a) $1\,\text{m}\Omega$ conducting 50 mA
- (b) $1\,\text{k}\Omega$ conducting 40 mA
- (c) $10\,\text{k}\Omega$ conducting 4 mA
- (d) $10\,\text{k}\Omega$ conducting 1 mA
- (e) $1\,\text{k}\Omega$ dropping 20 V
- (f) $1\,\text{k}\Omega$ dropping 11 V

1.3 Ohm's law and the power law for a resistor value V , I , R , and P , making only two variables independent. For each pair identified before, find the other two:

- (a) $R = 1\,\text{k}\Omega$, $I = 10$ mA
- (b) $V = 10$ V, $I = 1$ mA
- (c) $V = 10$ V, $P = 1$ W
- (d) $I = 10$ mA, $P = 0.1$ W
- (e) $R = 1\,\text{k}\Omega$, $P = 1$ W

COMBINING RESISTORS

1.4 You are given three resistors whose values are $15\,\text{M}\Omega$, $20\,\text{k}\Omega$, and $20\,\text{k}\Omega$. How many different resistances can you

create using series and parallel combinations of these? Hint: Use ohm's law to reduce the problem to one which is smaller than the sum of the two resistors. If one is particularly difficult, testing the circuit is surely indicated, in which case the set and when connected in parallel, is said to "short" the pair. If the original resistor is $10\,\text{k}\Omega$, what is the value of the shunting resistor or to notice the combined value by the $10\,\text{k}\Omega$, $10\,\text{k}\Omega$, $> 10\,\text{k}\Omega$? What is the test for "shunting" a $10\,\text{k}\Omega$ resistor by $1\,\text{M}\Omega$? By $20\,\text{k}\Omega$? By $10\,\text{k}\Omega$?

VOLTAGE DIVIDERS

1.5 Figure P1.5(a) shows a two-resistor voltage divider. Its function is to generate a voltage V_x (smaller than the source-supply voltage V_{DD}) at its output node X . The circuit, looking out at node X , is equivalent to that shown in Fig. P1.5(b). Calculate just this is the Thévenin equivalent of the voltage divider circuit. Find expressions for V_x and R_x :

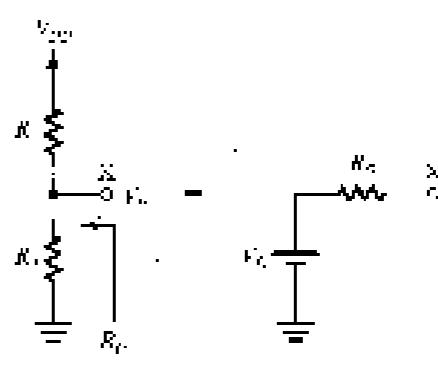


FIGURE P1.5

¹Estimated current problems are marked with a circled 1; more difficult problems are marked with a circled 2; and very difficult problems are marked with a circled 3.

*Design project problems are marked with a circled D.

P1.7 A two-resistor voltage divider employing a 5.5-kΩ and a 3-kΩ resistor is connected to a 9-V ground-referenced power supply to provide a relatively low voltage. Sketch the circuit. Assuming that, in red terms, what output voltage (measured to ground) and equivalent output resistance (assuming the resistors used are 10% local), have $\pm 2\%$ gain/bias; i.e., R_o , what are the extreme output voltages and resistances that can occur?

P1.8 You are given three resistors, each of 10 kΩ, and a 9-V battery whose negative terminal is connected to ground. With a voltage divider having some or all of your resistors, how many available voltage sources of magnitude less than 9 V can you design? Like them in value, small or high. What is the output resistance if, e.g., the load resistance of 1 kΩ?

P1.9 Two resistors, with nominal values of 4.7 kΩ and 10 kΩ, are used in a voltage divider with a 12-V supply to obtain a minimum 1.0-V output. Assuming the resistor R_1 is to be used, what is the total output voltage produced? Which resistor will be shorted (parallelled) by what load resistor to create a voltage-divider output of 1.000 V? If an current source of exactly 1.00 kΩ is also required, what do you suggest? What should R_2 be? (The requirement is 10.0 V and 1.0 kΩ will not work using the original 4.7-kΩ and 10-kΩ resistors.)

CURRENT DIVIDERS

P1.10 Current dividers play an important role in circuit design. There are many ways to develop a facility for dealing with current dividers in circuit analysis. Figure P1.10 shows a two-resistor current divider fed with an ideal current source I . Show that

$$I_1 = \frac{R_2}{R_1 + R_2} I$$

$$I_2 = \frac{R_1}{R_1 + R_2} I$$

and find the voltage V that develops across the current divider.

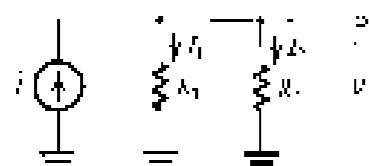


FIGURE P1.10

P1.11 Design a simple current divider with two resistors provided to a 4-kΩ load or 20% of the available from the source.

D1.12 A designer schedules for a complementary-pair voltage-controlled voltage source (a signal current, I , at a load resistance R_L) to provide a relatively low voltage. Sketch the circuit. Assuming that, in red terms, what output voltage (measured to ground) and equivalent output resistance (assuming the resistors used are 10% local, i.e., have $\pm 2\%$ gain/bias; i.e., R_o , what are the extreme output voltages and resistances that can occur?)

D1.13 A particular electronic signal source generates currents in the range 0 mA to 1 mA under the condition that its voltage not exceed 1 V. For load-coupling ratios of 10 to 100 across the generator, the output voltage is -20 mV , assumed to be reduced by some unknown amount. The circuit dimension occurring, for example, at the peak of a signal sine wave, will lead to undesirable signal distortion that must be avoided. This suggests loads to be considered, what must be done? What is the value of R_o and if you must use 100 resistors are needed? What is (are) load(s) value(s)?

THEVENIN-EQUIVALENT CIRCUITS

P1.14 For the circuit in Fig. P1.11, find the Thevenin-equivalent circuit between terminals 1 and 2, for 2 and 3, and for 1 and 3.

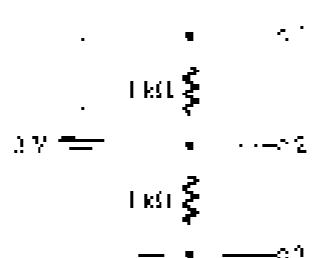


FIGURE P1.11

P1.15 Through repeated application of Thévenin's theorem, find the Thevenin-equivalent of the circuit in Fig. P1.15 between node 4 and ground, and hence find the current that flows through a load resistor of 10^3 Ω connected between node 4 and ground.

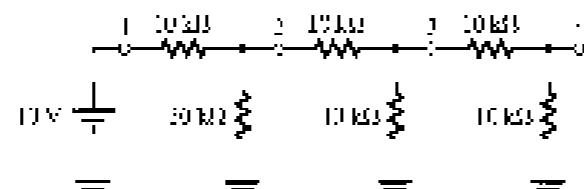


FIGURE P1.15

P1.17 Design a simple current divider with two resistors provided to a 4-kΩ load or 20% of the available from the source.

CIRCUIT ANALYSIS

P1.16 For the circuit shown in Fig. P1.6, find the current in all the nodes and the voltage (with respect to ground) of their nodes in nodes using two methods:

- (a) Current: Define branch currents I_1 and I_2 in R_1 and R_2 , respectively; form two equations; and solve them.
- (b) Voltage: Define the node voltage V in the common node; identify a single equation, and solve it.

Which method do you prefer? Why?

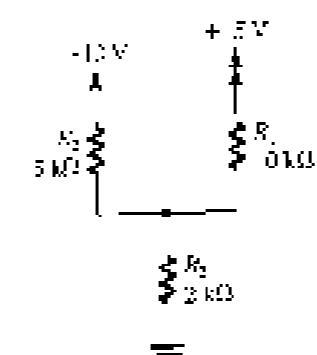


FIGURE P1.16

P1.17 The circuit shown in Fig. P1.7 represents the equivalent circuit to an unbalanced bridge. It is required to calculate the current in the detector branch (R_3) and the voltage across it. Although this can be done using loop or node equations, it must never appear to be possible! Find the Thevenin equivalent of the circuit to the left of node 1 and the Thevenin equivalent of the circuit to the right of node 2. Then solve the resulting simplified circuit.

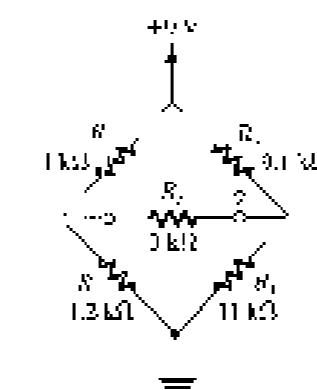


FIGURE P1.17

P1.18 For the circuit in Fig. P1.8, find the equivalent resistance R_{eq} to ground. To do this apply a voltage V_0 between terminal 3 and ground and find the current drawn from V_0 . Note that you

can expand on special properties of the circuit to get the result directly. Note, if R_1 is raised to 1.4 kΩ, what does R_{eq} become?

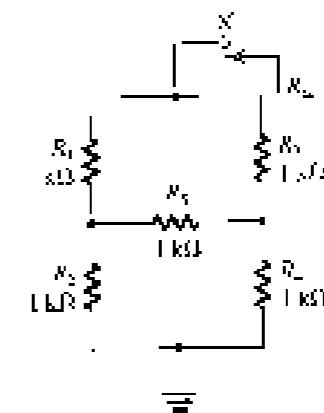


FIGURE P1.18

AC CIRCUITS

P1.19 The periodicity of periodic waveforms, such as sine waves or square waves, can be completely specified using only one of the possible parameters: either frequency, ω in radians per second (rads); (cyclic) period T , in seconds (s); (as well) each of λ , ν , τ , θ , ϕ , α , β , γ , δ ; or ω in degrees per second. Using standard prefixes associated with the basic units, using scientific notation, and using separate vibration of both λ and ν , for example, a particular period may be specified as 10^6 ns , $0.1\text{ }\mu\text{s}$, $10^{-1}\text{ }\mu\text{s}$, 10^2 ps , or $1 \times 10^7\text{ s}$. For the definition of the various prefixes used in electronics, see Appendix D. For each of the choices listed below, express the time period in scientific notation, associated with a basic unit, less than 10^{-3} rather than 10^{12} (ps).

- (a) $T = 10^{-6}\text{ ms}$
- (b) $f = 1\text{ GHz}$
- (c) $\nu = 5.28 \times 10^7\text{ rad/s}$
- (d) $T = 0\text{ s}$
- (e) $f = 1\text{ Hz}$
- (f) $\omega = 1\text{ rad/s}$
- (g) $\tau = 10^{-9}\text{ MHz}$

P1.20 Find the complex impedance Z of each of the AC lumped-harmonic elements at 60 Hz, 100 kHz, and -1 GHz:

- (a) $R = 1\text{ k}\Omega$
- (b) $C = 0\text{ nF}$
- (c) $C = 2\text{ pF}$
- (d) $L = 10\text{ }\mu\text{H}$
- (e) $L = 1\text{ }\mu\text{H}$

P1.21 Find the complex impedance at 10 kHz of the following networks:

- (a) 1 kΩ in series with $10\text{ }\mu\text{F}$
- (b) $1\text{ }\mu\text{F}$ in parallel with $0.01\text{ }\mu\text{F}$

- (c) $300 \text{ k}\Omega$ in parallel with 100 pF
 (d) $130 \text{ }\mu\text{A}$ in series with 10 mH

SECTION 1.1: SIGNALS

1.22 Any given signal source provides an open-circuit voltage, v_o , and a short-circuit current, i_s . For the following sources, calculate the internal resistance, R_i ; the Norton current, i_n ; and the Thevenin voltage, v_T :

- (a) $v_o = 10 \text{ V}$, $i_s = 0.01 \mu\text{A}$
 (b) $v_o = 0.1 \text{ V}$, $i_s = 10 \text{ nA}$

1.23 A particular signal source provides an output of 30 mV when loaded by a $10\text{-k}\Omega$ resistor and 10 mV when loaded by a $10\text{-M}\Omega$ resistor. Calculate the Thevenin voltage, Norton current, and source resistance.

1.24 A temperature sensor is specified to provide $2 \text{ mV}/^\circ\text{C}$. When connected to a load resistance of $10 \text{ M}\Omega$, the output voltage was measured to change by 10 mV , corresponding to a change in temperature of 10°C . What is the source resistance of the sensor?

1.25 Refer to the Thevenin and Norton representations of the signal source (Fig. 1.7). If the current supplied by the source is denoted i_s and the voltage appearing between the source output terminals is denoted v_o , sketch and clearly label i_s , $v_{T(s)}$, i_n , for $0 < v_o < v_T$.

1.26 The connection of a signal source to an associated signal processor or amplifier generally involves some degrees of signal loss as measured at the processor or amplifier input. Considering the two signal-source representations shown in Fig. 1.1, provide two sketches showing each signal source representation connected to the input terminals (and corresponding input resistance) of a signal processor. What signal processor input resistance will result in 90% of the open-circuit voltage being delivered to the processor? What input resistance will result in 90% of the short-circuit signal current entering the processor?

SECTION 1.2: FREQUENCY SPECTRUM OF SIGNALS

1.27 To familiarize yourself with typical values of angular frequency or conventional frequency f , and period T , complete the entries in the following table:

Case #	Angular frequency (rad/s)	Frequency (Hz)	Period (s)
1	1×10^1	1×10^1	1×10^{-1}
2	1×10^6	1×10^6	1×10^{-6}
3	9.28×10^3	90	1×10^{-3}
4	1×10^6	1×10^6	1×10^{-6}
5	—	—	—

1.28 For the following pairs of rms values of some important sine waves, calculate the corresponding other value:

- (a) $117 \text{ V}_{\text{rms}}$, a house AC-power voltage in North America
 (b) $33.9 \text{ V}_{\text{rms}}$, a somewhat common peak voltage in receiver circuits
 (c) $220 \text{ V}_{\text{rms}}$, a household power voltage in parts of Europe
 (d) $230 \text{ V}_{\text{rms}}$, a high-voltage transmission-line voltage in North America

1.29 Give expressions for the sine-wave voltage signals having:

- (a) 10-V peak amplitude and 10-kHz frequency
 (b) 12-V rms and 50-Hz frequency
 (c) 0.2-V peak-to-peak and 100-kHz frequency
 (d) 100-mV peak and 1-ms period

1.30 Using the information provided by Eq. (1.21) in association with Fig. 1.4, choose six bits of digital representation by $s_7 = 1/2 + 2/4 + 4/8 + 8/16 + 16/32 + 32/64 + 64/128 + \dots$. Sketch the waveform. What is its average value? Its peak-to-peak value? Its lowest value? Its highest value? Its frequency? Its period?

1.31 Measurements taken of a v_o sine-wave signal using a frequency-selective voltmeter (called a spectrum analyzer) show its spectrum in terms of adjacent components (spurious) located at 98 kHz and 136 kHz of an otherwise 64 mV and 10 mV respectively. For this signal, when an ideal direct measurement of the fundamental shows its frequency and amplitude to be? What is the rms value of the fundamental? What are the peak-to-peak amplitude and period of the originating square wave?

1.32 What is the fundamental frequency of the highest-frequency square wave for which the 13th harmonic is nearly available by a relatively gentle distortion? What is the fundamental frequency of the lowest-frequency square wave for which the 10th and 11th of the higher harmonics are directly heard? (Note that the psychoacoustic properties of human hearing allow us to sense the lower harmonics as well.)

1.33 Find the amplitude of a symmetrical square wave of period T that provides the same power as a sine wave of peak amplitude V_p and the same frequency. Does this result depend on equality of the waveforms of the two waveforms?

SECTION 1.3: ANALOG AND DIGITAL SIGNALS

1.34 Give the binary representation of the following decimal numbers: $3, 5, 6, 25$, and 57 .

1.35 Consider a 4-bit digital word $b_3b_2b_1b_0$ in a format called 2's complement magnitude, in which the most-significant bit, b_3 , is interpreted as a sign bit—0 for positive and 1 for negative values. List the values that can be represented by this word. What is peculiar about the representation of zero for a particular analog-to-digital converter (ADC), such

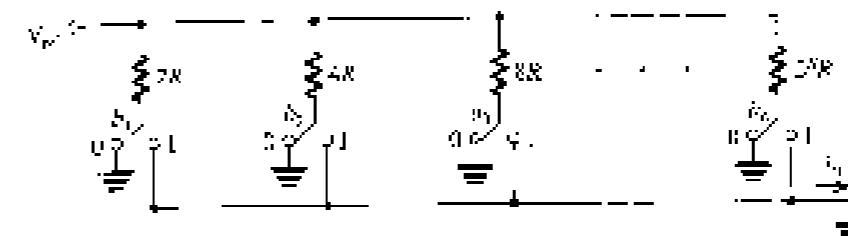


FIGURE P1.37

change in b_0 corresponds to a 0.5-V change in the analog input. What is the full range of the analog signal that can be represented? What signed-magnitude digital code results for an input, $b^* = 2.5 \text{ V} / 2^N + 2.0 \text{ V} / 2^N + 1.5 \text{ V} / 2^N + 2.8 \text{ V} / 2^N$?

1.36 Consider an N -bit ADC whose analog input varies between v_a and V_{DD} (where the subscript TS denotes "full-scale").

(a) Show that the least significant bit (LSB) corresponds to a change in the analog signal of $V_{DD}/2^N - 1$. This is the resolution of the converter.

(b) Consider yourself that the maximum error in the conversion (called the quantization error) is just the resolution; that is, the quantization error is $V_{DD}/2^N - 1$.

(c) For $V_{DD} = 10 \text{ V}$, how many bits are required to obtain a resolution of 5 mV or better? What is the actual resolution obtained? What is the resulting quantization error?

1.37 Figure P1.37 shows the circuit of an N -bit digital-to-analog converter (DAC). Each of the N bits of the digital word to be converted controls one of the switches. When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog voltage is the sum of V_{DD} is a constant reference voltage.

(a) Show that

$$V_o = \frac{V_{DD}}{R} \left(\frac{b_N}{2^N} + \frac{b_{N-1}}{2^{N-1}} + \dots + \frac{b_1}{2^1} + \frac{b_0}{2^0} \right)$$

(b) What bit is the LSB? What is 1 V LSB?

(c) For $V_{DD} = 10 \text{ V}$, $R = 5 \text{ M}\Omega$, and $N = 6$, find the maximum value of V_o obtained. What is the change in V_o resulting from the LSB changing from 0 to 1?

1.38 In compact-disc (CD) audio technology, the audio signal is sampled at 44.1 kHz . Each sample is represented by 16 bits. What is the speed of this system in bits/second?

SECTION 1.4: AMPLIFIERS

1.39 Various input bias and load considerations are measured as listed below using rms values. For each, find the voltage, current, and power gains (A_v , A_i , and A_p , respectively) both in dBs and in dB.

- (a) $v_i = 100 \text{ mV}$, $i_i = 100 \text{ pA}$, $v_o = 10 \text{ V}$, $R_o = 100 \text{ M}\Omega$

- (b) $v_i = 10 \text{ }\mu\text{V}$, $i_i = 100 \text{ nA}$, $v_o = 2 \text{ V}$, $R_o = 10 \text{ k}\Omega$

1.40 An amplifier operating from $\pm 5 \text{ V}$ supplies power to a $2.5\text{-V}_{\text{rms}}$ sine wave across a $10\text{-k}\Omega$ load when provided with a $0.5\text{-V}_{\text{rms}}$ input from which $1.0 \text{ nA}_{\text{rms}}$ is drawn. The average current in each supply is measured to be 10 mA . Find the voltage gain, current gain, and power gain expressed in dBs and in dB, as well as the supply power, amplifier dissipation, and amplifier efficiency.

1.41 An op-amp using balanced power supplies is known to saturate for signals extending within $\pm 2 \text{ V}$ of either supply. For linear operation, its gain is 500 V/V . What is the rms value of the largest undistorted sine-wave output available, and power needed, with $\pm 5\text{-V}$ supplies? With $\pm 15\text{-V}$ supplies?

1.42 Symmetrically saturated amplifiers, operating in the balanced-clipping mode, can be used to convert sine waves to pseudo-square waves. For an amplifier with a small signal gain of 1000 and clipping levels of $\pm 2 \text{ V}$, what peak value of input sinusoid is needed to produce an output whose extremes are just at the edges of a bipolar 50% (top) 50% (bottom) 25% of the time?

1.43 A particular amplifier operating from a single supply exhibits clipped peaks for signals extended beyond $\pm 1 \text{ V}$ and below 1.5 V . What is the peak value of the largest possible undistorted sine wave when this amplifier is biased at 4 V ? At what bias point is the largest undistorted sine wave available?

D*1.44 An amplifier designed using a single enhancement-mode metal-oxide-semiconductor (MOS) transistor has the transfer characteristic

$$v_o = 10 \cdot g_i v_i - 2^5$$

where v_i and v_o are in volts. This transfer characteristic is valid for $2 \leq v_i \leq v_o \leq 2$ and v_i positive. At the limits of this region the amplifier saturates.

(a) Sketch and clearly label the transfer characteristic. What are the saturation levels v_o and v_i and the corresponding values of v_i ?

(b) Box the β amplifiers to obtain a de output voltage of 5 V. What value of input dc voltage V_{in} is required?

(c) Calculate the value of the rms input voltage ratio at the bias point.

(d) The sinusoidal output voltage is superimposed on the dc bias voltage V_b ; that is,

$$v_o = V_b + V_{osc}$$

Find the resulting v_o . Using the approximation $\cos^2 \theta \approx 1 - \frac{1}{2}\sin^2 \theta$, express v_o as the sum of a dc component, a signal component, and a noise component, and a sinusoidal component with a peak-to-peak value. The noise component is a white noise and is a result of the nonlinear transfer characteristic of the amplifier. It is required to limit the ratio of the second harmonic component to the fundamental component to 1% (this is known as the second-harmonic distortion). What is the corresponding upper limit on V_b ? What current will it require?

SECTION 1.5: CIRCUIT MODELS FOR AMPLIFIERS

1.45 Consider the voltage-amplifier circuit model shown in Fig. 1.19(b), in which $A_{in} = 10$ V/V under the following conditions:

(a) $R_1 = 10\text{k}\Omega$, $R_2 = 10\text{k}\Omega$

(b) $R_1 = R_2$, $R_2 = R$

(c) $R_1 = R_2/10$, $R_2 = R/10$

Calculate the overall voltage gain v_o/v_i in each case, expressed both directly and in dB.

1.46 An amplifier with 20 dB of well-signd open-circuit voltage gain, an input resistance of 1 M Ω , and an output resistance of 10 k Ω drives a load of 100 k Ω . What voltage and power gains (expressed in dB) would you expect with the load connected? (The amplifier has a peak output-current limitation of 100 mA, where the rms value of the signal sine wave input to which an undistorted output is possible.) What is the corresponding output power available?

1.47 A 10-mV signal source having an internal resistance of 100 k Ω is connected to an amplifier for which the input resistance is 10 k Ω , the open-circuit voltage gain is 1000 V/V, and the output resistance is 1 k Ω . The amplifier is connected to a 10-k Ω load. What overall voltage gain results as measured from the source internal resistance to the load? Where did all the gain get lost? Would the gain be if the source was connected directly to the load? What is the ratio of the output gain? This ratio is a third measure of the gain of the amplifier stage?

1.48 A reference diode with a gain of 1 V/V has an input resistance of 1 M Ω and an output resistance of 10 k Ω . It is connected between a 1-V, 200 k Ω source and a 100-k Ω load.

What load voltage v_{load} (V) and the corresponding voltage, current, and power values expressed in dB?

1.49 Consider the cascade amplifier of Example 1.3. Find the overall voltage gain that is obtained when the first and second stages are interchanged. Compare this value with the result in Example 1.3, and comment.

1.50 You are given two amplifiers, A and B, to connect in cascade between a 1-V, 200-k Ω source and a 100-k Ω load. The amplifiers have voltage gains, input resistances, and output resistances as follows: For A, 100 V/V, 10 k Ω , 10 k Ω , respectively; for B, 100 V/V, 100 k Ω , 100 k Ω , respectively. You are free to decide how the amplifiers should be connected. To proceed, evaluate the ten possible connections between source and load, namely, SABL and SBAL. Find the voltage gain for each path as a ratio and in dB. Which amplifier configuration is best?

1.51 A designer has available voltage amplifiers with an input resistance of 10 k Ω , an output resistance of 10 k Ω , and an open-circuit voltage gain of 100. A 10-mV sine signal, and it is required to provide a signal of at least 2 V rms in a 1-k Ω load. How many amplifiers stages are required? What is the output voltage ratio to be obtained?

1.52 Design a amplifier that provides 0.5 W of signal power in a 10-k Ω load resistance. The signal source provides a 10-mV rms signal and has a resistance of 0.5 M Ω . If we type of voltage amplifier stages are available:

(a) A high-current-resistance type with $R_i = 1\text{ M}\Omega$, $A_{in} = 10$, and $R_o = 10\text{k}\Omega$

(b) A medium-type with $A_{in} = 10\text{k}\Omega$, $A_{in} = 100$, and $R_o = 1\text{ M}\Omega$ for a low-current-resistance type with $R_i = 10\text{k}\Omega$, $A_{in} = 1$, and $R_o = 20\text{k}\Omega$.

Design a suitable amplifier using a combination of these stages. Your design should use the minimum number of stages and should ensure that the signal level is not reduced below 10 mV at any point in the amplifier chain. Find the load voltage and power output required.

1.53 It is required to design a voltage amplifier to be driven from a signal source having a 10-mV peak-to-peak sine and a series resistance of 10 k Ω to supply a power of 0.1 mW across a 1-k Ω load.

(a) What is the required voltage gain from the source to the load?

(b) If the peak current available from the source is 0.1 mA, what is the largest input resistance allowed? For the design with this value of R_i , find the overall current gain and voltage gain.

(c) If the amplifier power supply V_{cc} is the peak value of the output signal, and $V_{cc} = 5$ V, what is the largest output voltage allowed?

(d) For the design with $R_i = 10\text{k}\Omega$ and $R_o = 1\text{ M}\Omega$, what is the required value of requirement voltage gain, i.e., $\frac{R_o}{R_i} = \frac{100}{10} = 10$?

(e) If, as a possible design option, you are able to increase R_o to the greatest value of the form $1 \times 10^n \text{ M}\Omega$ and it causes R_o to the peak value of the form $1 \times 10^n \text{ }\Omega$, find (f) the input resistance achievable, (g) the output resistance achievable, and (h) the open-circuit voltage gain, now subject to meet the specifications.

1.54 A voltage amplifier with an input resistance of 10 k Ω , an output resistance of 10 k Ω , and a gain of 1000 V/V is connected between a 100-k Ω source with an open-circuit voltage of 0.1 mV and a 10-k Ω load. Find the answers:

(a) What output voltage is obtained?

(b) What is the voltage gain from source to load?

(c) What is the voltage gain from the amplifier input to the load?

(d) If the output voltage zero is the load is twice the normal and there are signs of interstage amplifier overdrive, i.e., the load, in and value of a single resistor that would produce the desired output? Choose an arrangement that would cause minimum dissipation in operating circuit. (Hint: Use parallel rather than series connection.)

1.55 A current amplifier has values $R_i = 1\text{ k}\Omega$, $R_o = 10\text{k}\Omega$, and $A_{in} = 100$ A/A, is to be connected between a 100-mV source with a resistance of 100 k Ω and a load of 1 k Ω . What are the values of current gain, I_{out} , of voltage gain, v_{out}/v_i , and of power gain expressed directly in dB?

1.56 A transconductance amplifier with $A_g = 2\text{ k}\Omega$, $G_{in} = 40$ mV/A, and $R_o = 20\text{k}\Omega$ is fed with a voltage source having a source resistance of 2 k Ω and is loaded with a 1-k Ω resistance. Find the design goal realized.

1.57 A designer is required to provide a 10-mV, 10-k Ω load, the signal voltage, $v_s = 0.1 + 20\sin(\omega t)$, an input signals v_i and its load having a source resistance of 10 k Ω . She has a number of unidirectional amplifiers for which the input and output resistances are 100 k Ω and $G_{in} = 20$ mV/A, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. Hint: In your design, arrange to feed currents:

1.58 Figure 21.36 shows a transconductance amplifier whose output is fed back to its input. Find the input resistance R_{in} of the resulting voltage-controlled voltage source. Hint: Apply a test

voltage v_s between the two input terminals, and find the current i_s drawn from the source. Then, $R_{in} = v_s/i_s$.

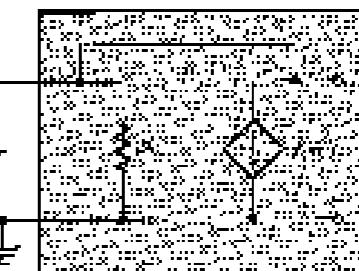


FIGURE P1.58

1.59 It is required to design a amplifier to sense the collector-emitter output voltage of a transistor and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transistor is specified to vary in the range of 1 k Ω to 10 k Ω . Also, the load resistance varies in the range of 1 k Ω to 0 k Ω . The change in load voltage corresponding to the specified change in R_s should be 1.0% of load. Similarly, the change in load voltage corresponding to the specified change in R_L should be limited to 10%. Also, consider that to a 10-mV transconductance-output current voltage, the amplifier should provide a maximum of 5% across the load. What size of amplifier is required? Sketch a circuit model, and specify the values of its parameters. Specify operating voltage for R_s and R_L in the form $1 \times 10^n \Omega$.

1.60 It is required to design an amplifier to serve the short-circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 k Ω to 10 k Ω . Similarly, the load resistance is known to vary over the range of 1 k Ω to 10 k Ω . The change in load current corresponding to the specified change in R_s is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in R_L should be 10% at most. Also, for a nominal short-circuit output current of the transducer of 10 mA, an amplifier is required to provide a minimum of 1 mA through the load. What size of amplifier is required? Sketch the circuit model. The amplifier and specify values to its parameters. Select appropriate values for R_s and R_L in the form $1 \times 10^n \Omega$.

1.61 It is required to design an amplifier to sense an open-circuit output voltage of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 k Ω to 10 k Ω . Also, the load resistance is known to

very low ($\approx 10^{-12} \text{ A}$). Since $\beta = 1000$, the change in the current supplied by the load corresponding to the specified change in R_L is to be 1.2% at most. Similarly, the change in load voltage corresponding to the specified change in R_L is to be $\pm 10\%$ at most. Note that, assuming the input current and output voltage to be of 1 mA, the amplifier is required to provide a maximum of 1 mA current through the load. What type of amplifier is required? Sketch the complete circuit and specify values for the parameters for R_s and R_L (specify values in the range $1 \times 10^3 \text{ } \Omega$).

P1.62 It is required to design an amplifier to sense the short-circuit current output of a Hall-effect and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of $1 \text{ k}\Omega$ to $10 \text{ k}\Omega$. Similarly, the load resistance is known to vary in the range of $1 \text{ k}\Omega$ to $10 \text{ k}\Omega$. The change in load voltage corresponding to the specified change in R_s should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in R_L is to be limited to 10%. Also, for a nominal transducer short-circuit output current of 1 mA, the amplifier is required to provide a minimum voltage across the load of 1 V. What type of amplifier is required? Sketch the circuit and specify the values of the model parameters. For R_s and R_L , specify appropriate values in the range $1 \times 10^3 \text{ } \Omega$.

P1.63 For the circuit in Fig. P1.63, show that

$$\frac{R_s}{R_s + R_L} = \frac{-2R_s}{R_s + (2 + \beta)R_s}$$

and

$$\frac{1}{A_v} = \frac{R_s}{R_s + (2 + \beta)R_s}$$

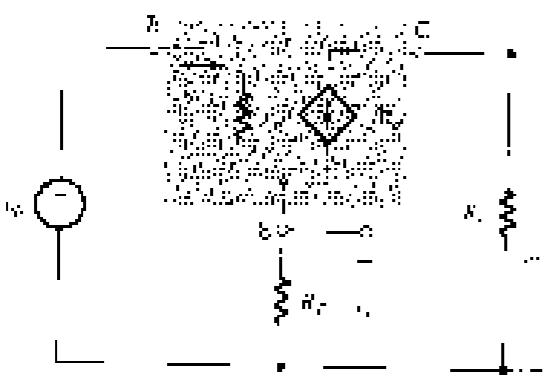
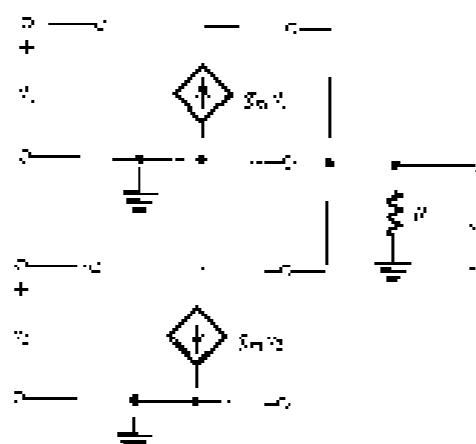


FIGURE P1.63

P1.64 An amplifier with an input resistance of $10 \text{ }\mu\Omega$, when driven by a current source of $1 \text{ }\mu\text{A}$ and a source resistance of $10 \text{ }\Omega$, has a short-circuit output current of 10 mA and an open-circuit output voltage of 10 V. When driving a $1 \text{ k}\Omega$ load, what are the values of the voltage gain, current gain, and power gain expressed in terms of mV , mA , and W ?

P1.65 Figure P1.65(a) shows two transconductance amplifiers connected in series configuration. The β values of α and β are $\beta_1 = 100 \text{ mA/V}$ and $\beta = 5 \text{ k}\Omega$; if $v_o = v_i = 1 \text{ V}$, find the value of v_o . Also, find the value for the case $v_o = 1.0 \text{ V}$ and $v_i = 0.99 \text{ V}$. Note: This circuit is called a differential amplifier and is given the symbol shown in Fig. P1.65(b). A particular type of differential amplifier based on an operational amplifier will be analyzed in the next section.



SECTION 1.67: FREQUENCY RESPONSE OF AMPLIFIERS

P1.66 Using the voltage-divider rule, derive the transfer function $V_{o1}(s) = V_{o1}(0)/V_{i1}(s)$ of the circuit shown in Fig. 1.23, and show that its transfer functions are of the form given at the top of Fig. 1.12.

P1.67 Figure P1.67 shows a signal source connected to the input of an amplifier. Here R_s is the source resistance, and R_i and C_i are the input resistance and input capacitance,

respectively, of the amplifier. Derive an expression for $V_{o1}(s)/V_{i1}(s)$, and show that it is of the low-pass SIC type. Find the 3-dB frequency for the case $R_s = 20 \text{ k}\Omega$, $R_i = 20 \text{ k}\Omega$, and $C_i = 5 \text{ }\mu\text{F}$.

P1.68 Measurements of the frequency response of an amplifier yield the data in the following table:

(MHz) (dB) (MHz) (dB)

	0	40	90
1	10	40	90
2	0.1	37	-15
3	0.01	30	-30
4	0	0	0

From available information, sketch the magnitude-frequency characteristic and clearly label the magnitude-frequency response (i.e., provide a scale plot for this amplifier).

P1.69 For the circuit shown in Fig. P1.69, find the magnitude $|V_{o1}(s)| = |V_{o1}(s)/V_{i1}(s)|$, and arrange it in the approximate form given from Table 1.2. Is it a high-pass or a low-pass network? What is its corner frequency at very high frequencies? (Perform this directly, as well as by letting $s \rightarrow \infty$ in your expression for $V_{o1}(s)$.) What is the corner frequency ω_0 for $R_s = 1.0 \text{ k}\Omega$, $R_i = 10 \text{ }\mu\text{A}$, and $C = 0.1 \text{ }\mu\text{F}$? Find ω_c when the value of $|V_{o1}(s)|$ is

Approximate	10	10 ³	10 ⁶	10 ⁹	10 ¹²
10 dB	0	20	40	60	80

Provide approximate absolute values for the missing node resistances, switch, and clearly label the magnitude-frequency response (scale plot) of this amplifier.

P1.70 The unity-gain voltage amplifier in the circuit of Fig. P1.70 has infinite input resistance ∞ and zero output resistance and thus functions as a passive buffer. Determine respectively, the overall gain V_{o1}/V_{i1} and the frequency ω_c at which the gain of each of each RC circuit is 1.0 dB down (*i.e.*, at 1-dB frequency in terms of CR^2).

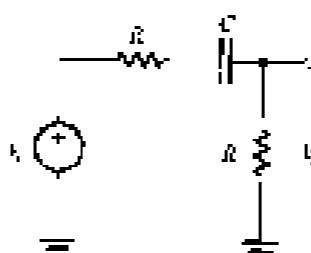


FIGURE P1.68

P1.69 It is required to couple a voltage source V_s with a resistance R_s to a load R_L via a capacitor C . Derive an expression for the transfer function $V_{o1}(s)/V_{i1}(s)$ in terms of V_s , R_s , and C , so that it is of the high-pass SIC type. For $R_s = 1 \text{ k}\Omega$ and $R_L = 20 \text{ k}\Omega$, let the smallest replace capacitor that will yield, in a 1-dB frequency no greater than 10 Hz,

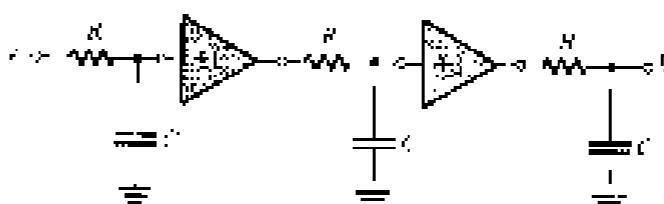


FIGURE P1.72

P1.74 A designer wishes to have the overall low-pass filter 3-dB frequency of a three-stage amplifier to 10 kHz, considering that, at each node (Node A, between the output of the first stage and the input of the second stage; and Node B, between the output of the second stage and the input of the third stage), the ground is grounded with a small capacitor. While doing so, the overall frequency response of the amplifier, at a certain frequency f_c , rises to node A and then to node B, forcing the 3-dB frequency from 2 MHz to 150 kHz and 15 kHz, respectively. Let us know that each amplifier stage has an input resistance of 100 k Ω , what current resistance must the driving stage have to make $R_o \gg R_i$ near R_o ? What design would you suggest for the corner in which it is necessary to solve the design problem most conveniently?

P1.75 An amplifier requires an input resistance of 100 k Ω and an output resistance of 1 k Ω to be source-coupled to a 1-MHz feedback with a 1-k Ω load. Available capacitors have values only of the form $1 + 10^{-k}$ F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each stage is less than 100 Hz? What actual corner frequencies result? For the circuit in which the basic amplifier has an open-loop voltage gain (A_{vL}) of 100 V/V, find an expression for $T(s) = V_o(s)/V_i(s)$.

***1.76** A voltage-controlled voltage-controlled junction

$$A_v = \frac{100}{1 + j \frac{f}{f_{c1}} + \frac{R_o^2}{R_1^2}}$$

$$R_o \leq \frac{1}{2\pi f_{c1} C_1 (1/R_1)}$$

$$C_1 \geq \frac{A_{vL}(1 - \alpha)/100}{(R_1 || R_o)}$$

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.25 and 1.27), sketch a Bode plot for A_v . Give approximate values for the gain margin ($\alpha = 10$ dB, 10 3 Hz, 10 2 Hz, 10 4 Hz, 10 5 Hz, 10 6 Hz, and 10 7 Hz) and the band width of the amplifier (defined as the frequency range over which the gain is within 3 dB of the maximum value).

***1.77** For the circuit shown in Fig. P1.77, first evaluate $T(s) = V_o(s)/V_i(s)$; then the corresponding cutoff frequency

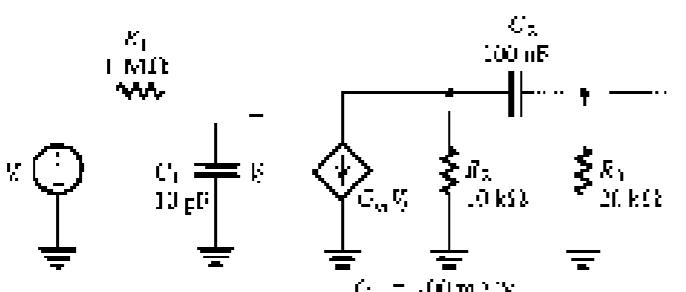


FIGURE P1.77

frequency. Second, evaluate $T_c(s) = V_o(s)/V_{o(0)}$, i.e., the corresponding cutoff frequency. Because of the negative feedback in the standard form (see Table 1.2), and owing back to some low-pass filter function, $T_c(s) = T(s)/T_{c(0)}$. For what is Bode magnitude plot for $T(s)$? What is the bandwidth between 3-dB cutoff points?

***1.78** A non-conductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source V_s , two voltage-controlled resistances R_1 and R_2 , and its current is connected to a load consisting of a resistance R_L in parallel with a capacitance C_L . For given values of R_1 , R_2 , and C_L , it is required to specify the values of the equivalent parameters R_o , G_{oL} , and R_i under the following design constraints:

- (a) At least, 90% of the input signal is lost in coupling losses and in the inductor (i.e., $V_o(0) = 0.1V_s(0)$).
- (b) The 3-dB frequency of the amplifier is equal to or greater than a specified value f_{c1} .
- (c) The dc gain $V_o(0)/V_s(0)$ is equal to or greater than a specified value α .

Show that these constraints can be met by selecting

$$R_o \leq \frac{100}{1 + j \frac{f}{f_{c1}} + \frac{R_o^2}{R_1^2}}$$

$$R_i \leq \frac{1}{2\pi f_{c1} C_1 (1/R_1)}$$

$$C_1 \geq \frac{A_{vL}(1 - \alpha)/100}{(R_1 || R_o)}$$

Find R_1 , R_2 , and C_1 for $R = 50$ k Ω , $\alpha = 20\%$, $A_{vL} = 50$, $R_o = 10$ k Ω , $C_L = 10$ pF, and $f_{c1} = 3$ MHz.

***1.79** Use the voltage-divider rule to find the transfer ratio $V_o(s)/V_i(s)$ of the circuit in Fig. P1.79. Show that the transfer function can be made independent of frequency if the condition $C_1 R_1 = C_2 R_2$ is met. Under this condition the circuit is called a compensated attenuator and is frequently

employed in the design of oscilloscope probes. Find the transmission of the compensated attenuator in terms of R_1 and R_2 .

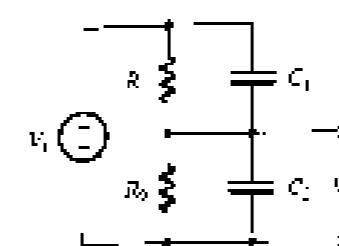


FIGURE P1.79

***1.80** An amplifier with a 3-dB corner frequency of the type shown in Fig. 1.2 is specified to have a phase shift of one-half, no greater than $\pm 45^\circ$ over the amplifier bandwidth, which extends from 100 Hz to 10 kHz. It has been found that the sum reflected in the dominant decay rate is determined by the response of a high-pass STC circuit and that at the highest frequency and ω_c is determined by a low-pass STC circuit. Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.26) to calculate the dynamic power dissipation.

- (a) Find the worst-case value of the noise margins.
- (b) Assuming that the inverter is in the logic-0 state for 50% of the time and in the logic-1 state 50% of the time, find the average static power dissipation in a typical circuit. The power supply is 5 V.
- (c) Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.26) to calculate the dynamic power dissipation.
- (d) Find the propagation delay t_p .

***1.81** Consider an inverter implemented as in Fig. 1.31(a). Let $V_{DD} = 5$ V, $R_s = 2$ k Ω , $C_{in} = 0.1$ pF, $R_o = 50$ k Ω , $V_D = 1$ V and $V_{DD} = 2$ V.

SECTION 1.73 DIGITAL LOGIC INVERTERS

1.81 A particular logic inverter is specified to have $V_D = 1.3$ V, $V_{DD} = 1.7$ V, $V_G = 0$ V, and $V_{DD} = 1.2$ V. Find the high and low noise margins, NM_H and NM_L .

1.82 The voltage-controlled characteristic of a particular logic inverter is modeled by three straight line segments in the manner shown in Fig. 1.26. If $V_A = 1.5$ V, $V_D = 2.5$ V, $V_C = 0.5$ V, and $V_{DD} = 4$ V, find:

- (a) The noise margins
- (b) The value of α at which $V_D = V_D$ (known as the inverter threshold)
- (c) The voltage gain in the transition region

1.83 For a particular inverter design using a power supply $V_{DD} = 5$ V, $V_{DD} = 0$ V, $V_{DD} = 1.5$ V, $V_D = 0.4V_{DD}$, and $V_D = 0.6V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 1 V, what value of V_D is required?

1.84 A logic circuit family that used to be very popular is Transistor-Transistor Logic (TTL). The TTL logic gates and other building blocks are available commercially in small-scale integrated (SSI) and medium-scale integrated (MSI) packages. Such packages can be assembled on printed-circuit boards to implement a digital system. The device data sheet specifies $t_{pd} = 1$ pF. Also find t_{pd} (see Fig. 1.35).

provide the following specifications of the basic TTL inverter (of the SN7400 series):

- (a) Input level required to ensure a logic-0 level is the output MIN (minimum) 0.8 V
- (b) Output level required to ensure a logic-1 level is the output MAX (maximum) 0.8 V
- (c) Logic-1 output voltage: MIN 2.4 V, TYP 2.2 V, MAX 0.4 V
- (d) Logic-0 output current: TYP 0.22 mA, MAX 5 mA
- (e) Logic-1-level supply current: TYP 1 mA, MAX 2 mA
- (f) Propagation delay time to logic-0 level (t_{pd}): TYP 7 ns, MAX 15 ns
- (g) Propagation delay time to logic-1 level (t_{pd}): TYP 11 ns, MAX 23 ns

- (a) Find the worst-case values of the noise margins.
- (b) Assuming that the inverter is in the logic-0 state for 50% of the time and in the logic-1 state 50% of the time, find the average static power dissipation in a typical circuit. The power supply is 5 V.
- (c) Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.26) to calculate the dynamic power dissipation.
- (d) Find the propagation delay t_p .

***1.82** Consider an inverter implemented as in Fig. 1.31(a). Let $V_{DD} = 5$ V, $R_s = 2$ k Ω , $C_{in} = 0.1$ pF, $R_o = 50$ k Ω , $V_D = 1$ V and $V_{DD} = 2$ V.

(e) Find V_{DD} , V_{DD} , NM_H , and NM_L .

(f) The inverter is driving a current-mode inverter. Each of these load inverters is a fan-out inverter, as they are usually 3-to-1. It is specified to require an input current of 0.2 mA when the input voltage (of the fan-out inverter) is high and zero current when the input voltage is low. Notice that the input currents of the fan-out inverters will have to be supplied through R_o of the driving inverter. Find the resulting value of V_{DD} and of NM_H , as a function of the number of fan-out inverters N . Hence find the maximum value N that can have while the inverter is still providing an NM_H value at least equal to its NM_H .

(g) Find the static power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high, and driving the maximum fan-out load in (b).

1.86 A logic inverter is implemented using the arrangement of Fig. 1.32 with switches having $R_s = 1$ k Ω , $V_{DD} = 5$ V, and $V_D = V_{DD} - V_{DD}/2$.

- (a) Find V_{DD} , V_{DD} , NM_H , and NM_L .
- (b) It uses two switches, one pair from 0 V to +2 V and assuming the switches operate instantaneously—that is, at $t = 0$, PF opens, and PF closes. Find an expression for t_{pd} assuming that a capacitance C is connected between the output node and ground. Hence find the minimum propagation delay t_{pd} to $C = 1$ pF. Also find t_{pd} (see Fig. 1.35).

(c) Repeat (b) for v_1 being instantaneous from 15 V to 0 V. Again assume the FET opens with V_D across instantaneous drain current expression for v_{DS} , and hence find v_{DS} and v_{DS} .

1.87 For the circuit shown in Fig. 1.39, let $V_{DD} = 5V$, $I_s = 1\text{ mA}$, and $R_g = R_d = 5\text{ k}\Omega$. Find V_{OL} and V_{OH} .

1.88 Consider a logic inverter of the type shown in Fig. 1.32, with $V_{DD} = 5\text{ V}$, and let a 10-pF capacitor pulse the gate terminal between the output node and ground. If the inverter is switched at the rate of 100 MHz, use the expression in eq. (1.28) to estimate the dynamic power dissipation. What is the average current drawn from the dc power supply?

01.89** We wish to investigate the design of the inverter shown in Fig. 1.31(a). In particular we wish to determine the value for R (selection of a suitable value for R) determined by two considerations: propagation delay, and power dissipation.

(a) Show that if the switch opens instantaneously (and again assume the low switch opens instantaneously), the output voltage obtained across a load capacitance C will be

$$v_o(t) = V_{DD} - (V_{DD} - V_{DD})e^{-t/R}$$

where $v_i \sim 1\text{ V}$. Hence show that the time required for v_{DD} to reach its 99% limit, $\frac{1}{2}(V_{DD} - V_{DD})$, is

$$t_{99\%} = 0.69CR$$

(b) Following a steady state, v_i goes high and remaining flat the switch closes immediately, and has the equivalent circuit in Fig. 1.31, show that the output falls exponentially according to,

$$v_{DD}(t) = V_{DD} - (V_{DD} - V_{DD})e^{-t/R}$$

where $v_i = 0.9(V + R_{in}) = 0.9R_{in}$ for $R_{in} \gg R$. Hence show that the time for $v_{DD}(t)$ to reach the 99% point is

$$t_{99\%} = 0.69C/R_{in}$$

(c) Use the results of (a) and (b) to obtain the inverter propagation delay, t_{PD} , as the average of $t_{99\%}$ and $t_{99\%}$:

$$t_{PD} = 0.35CR(1 + R_{in}/R)$$

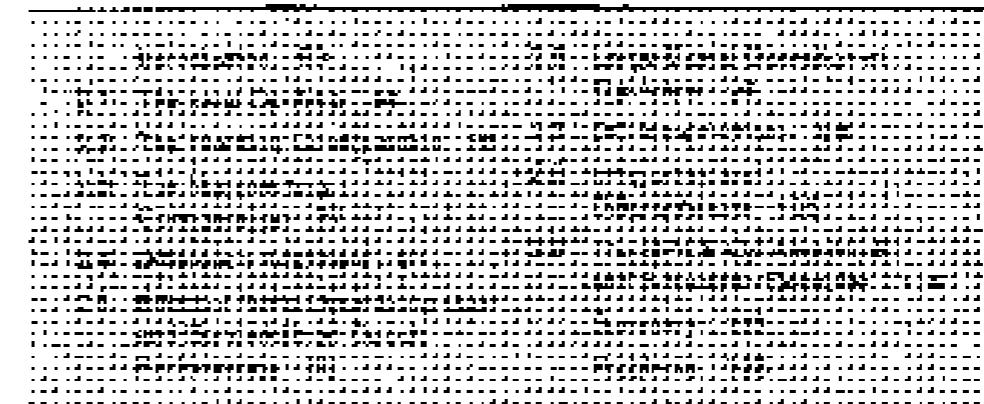
(d) Assuming the V_{DD} of the inverter current is smaller than R_{in} , show that for an inverter that spends half the time in the 0 state and half the time in the 1 state, the average static power dissipation is

$$P = \frac{1}{2} \frac{V_{DD}^2}{R}$$

(e) Now that we understand in selecting R there should be obvious, show that for $V_{DD} = 5\text{ V}$ and $C = 10\text{ pF}$, to obtain a propagation delay t_{PD} greater than 10 ns and a power dissipation no greater than 10 mW, R should be in a specific range. Find that range and select an appropriate value for R . Then determine the resulting values of t_{PD} and P .

CHAPTER 2

Operational Amplifiers



INTRODUCTION

Having learned basic amplifier concepts and terminology, we are now ready to undertake the study of a circuit building block of universal importance: the operational amplifier (op-amp). Op-amps have been in use for a long time, their initial applications being primarily in the areas of analog computation and sophisticated instrumentation. Early op-amps were constructed from discrete components (vacuum tubes and, later, transistors, and resistors), and their cost was prohibitively high (items of 10 dollars). In the mid-1960s the first integrated-circuit (IC) op-amp was produced. This unit (the μA 702) was made up of a relatively large number of transistors and resistors all on the same silicon chip. Although its characteristics were potentially inferior to standard discrete op-amps, and its price was still quite high, its appearance heralded a new era in electronic circuit design. Electronics engineers started using op-amps in large quantities, which caused their price to drop dramatically. They also demanded better quality techniques. Semiconductor manufacturers responded quickly, and within the year or a few years, high-quality op-amps became available at extremely low prices (less of μ s). From a large number of suppliers.

One of the reasons for the popularity of the op-amp is its versatility. As we will shortly see, one can do almost anything with an op-amp. Equally important is the fact that the IC op-amp has characteristics that closely approach the assumed ideal. This implies that it's quite

easy to design circuits using the IC op amp. Also, op-amp circuits work at performance levels that are quite close to those predicted theoretically. It is for this reason that we are studying op amps at this early stage. It is expected that by the end of this chapter the reader should be able to design nontrivial circuit successfully using op amps.

As already implied, an IC op amp is made up of a large number (several) of transistors, resistors, and (usually) one capacitor connected in a rather complex circuit. Since we have not yet studied transistor circuits, the circuit inside the op-amp will not be discussed in this chapter. Rather, we will treat the op-amp as a circuit building block and study its terminal characteristics and its applications. This approach is quite satisfactory in many common applications. Nevertheless, for the more difficult and demanding applications it is quite useful to "see what is inside" the op-amp package. This topic will be studied in Chapter 9. Finally, it should be mentioned that more advanced applications of op-amps will appear in later chapters.

2.1 THE IDEAL OP AMP

2.1.1 The Op-Amp Terminals

From a signal point-of-view the op-amp has three terminals: two input terminals and one output terminal. Figure 2.1 shows the symbol we shall use to represent the op-amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal. As explained in Section 1.4, amplifiers require dc power to operate. Most IC op-amps require two dc power supplies, as shown in Fig. 2.2. Two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage V_{DD} and a negative voltage $-V_{SS}$, respectively. In Fig. 2.2(a)

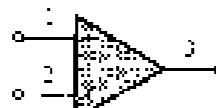


FIGURE 2.1 Circuit symbol for the op-amp.

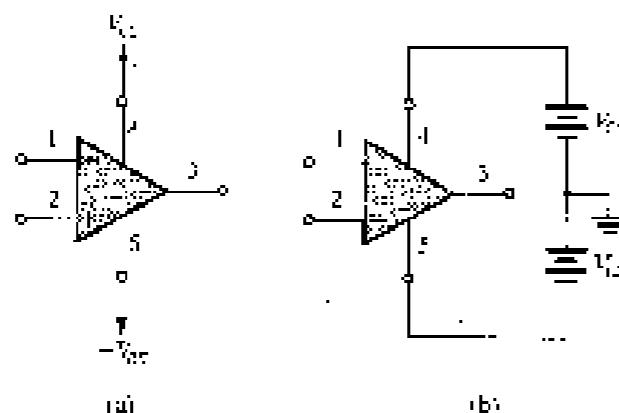


FIGURE 2.2 The op-amp should be connected to dc power supplies.

we explicitly show the two dc power supplies as batteries with a common ground. It is interesting to note that the reference grounding point in op-amp circuits is just the common terminal of the two power supplies; that is, no terminal of the op-amp package is physically connected to ground. In what follows we will not explicitly show the op-amp power supplies.

In addition to the three signal terminals and the two power-supply terminals, an op-amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling; both functions will be explained in later sections.



2.1.2 Function and Characteristics of the Ideal Op Amp

We now consider the circuit function of the op-amp. The op-amp is designed to sense the difference between the voltage signals applied at its two input terminals (i.e., the quantity $v_2 - v_1$) and multiply this by a number A , and cause the resulting voltage $A(v_2 - v_1)$ to appear at output terminal 3. Here it should be emphasized that when we talk about the voltage v_1 at a terminal we mean the voltage between that terminal and ground; thus v_1 means the voltage applied between terminal 1 and ground.

The ideal op-amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current out of terminal 2 are both zero. In other words, the input impedance of an ideal op-amp is supposed to be infinite.

How about the output terminal 3? This terminal is supposed to act as the output terminal of an ideal voltage source. That is, the voltage between terminal 3 and ground will always be equal to $A(v_2 - v_1)$, independent of the current that may be drawn from terminal 3 into a load impedance. In other words, the output impedance of an ideal op-amp is supposed to be zero.

Putting together all of the above, we arrive at the equivalent circuit model shown in Fig. 2.3. Note that the output is in phase with the same sign as v_2 and is out of phase with v_1 (has the opposite sign of v_1). For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a “-” sign, while input terminal 2 is called the **non-inverting input terminal** and is distinguished by a “+” sign.

As can be seen from the above description, the op-amp responds only to the difference signal $v_2 - v_1$ and hence ignores any signal common to both inputs. That is, if $v_1 = v_2 = 1\text{ V}$, then the output will—ideally—be zero. We call this property **common-mode rejection**, and we can note that an ideal op-amp has zero common-mode gain or, equivalently, infinite common-mode rejection. We will have more to say about this point later. For the time being note that the op-amp is a **differential-input single-ended-output amplifier** with the latter term referring to the fact that the output appears between terminal 3 and

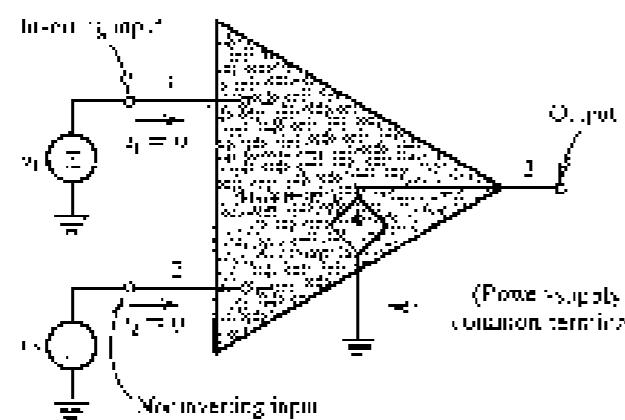


FIGURE 2.3. Aqueous! test of the ideal no. 3 sample.

TABLE 2.3 The Benefits of Helped Options

1. Unbiased input phasor ratio
 2. Zero output impedance
 3. Zero common-mode gain (or equivalently, infinite common-mode rejection)
 4. Infinite open-loop gain, A
 5. Infini-gain with

ground. Furthermore, gain A is called the **differential gain**, for obvious reasons. Perhaps not so obvious is another name that we will attach to A : the **open-loop gain**. The reason for this name will become obvious later on when we "close the loop" around the op-amp and do the analysis again; the closed-loop gain.

An important characteristic of op-amps is that they are direct-coupled or dc amplifiers where dc stands for direct coupled (dc could equally well stand for direct current, since a direct-coupled amplifier is one that amplifies signals whose frequency is as low as zero). The fact that op-amps are direct-coupled devices will allow us to use them in many important applications. Unfortunately, though, the direct-coupling property can cause some serious practical problems, as will be discussed in a later section.

How about bandpass? The ideal op-amp has a gain A that vanishes constant down to zero frequency and up to infinite frequency. That is, ideal op-amps will amplify signals only in frequency with equal gain, and are thus said to have infinite bandwidth.

We have discussed all of the properties of the ideal op-amp except for one, which in fact is the most important. This has to do with the value of A . The ideal op-amp should have a gain A whose value is very large and ideally infinite. One may justifiably ask: If the gain A is infinite, how are we going to use the op-amp? The answer is very simple: In almost all applications the op-amp will not be used alone in a so-called open-loop configuration. Rather we will use other components to apply feedback to close the loop around the op-amp as will be illustrated in detail in Section 2.2.

For future reference, Table 2.1 lists the characteristics of the ideal organization.

Some op-amps are designed to have differential outputs. This topic will be discussed in Chapter 9. In this chapter we consider ourselves at single-ended output op-amps, which constitute the vast majority of commercially available op-amps.

3.1.3 Differential and Common-Mode Signals

The differential input signal $v_{d,i}$ is simply the difference between the two output signals v_i and v_{-i} , that is:

$$2\lambda_1 - \lambda_2 - \lambda_3 = 2\lambda_1$$

The "complementary input signal" $v_{1,2}$ is the average of the two input signals v_1 and v_2 , namely,

$$v_{1,2} = \frac{1}{2}(v_1 + v_2) \quad (2.2)$$

Equations (2.1) and (2.2) can be used to express the input signals s_1 and s_2 in terms of their difference and conjugate-mosaic components as follows:

$$c = c_{\text{MB}} - v_s/2 \quad (2.3)$$

5

$$\beta_i = \beta_{i,\lambda} + \gamma_i/2 \quad (2.4)$$

These equations can now lead to the pictorial representation in Fig. 2.

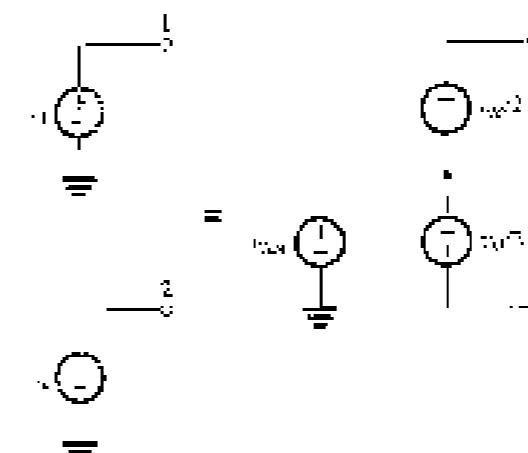


FIGURE 2.4 Representation of the signal $s(t) = \cos(\omega_0 t)$ in terms of basis functions and complex mode amplitude.

100

- The following table gives the values of ΔE for the various transitions observed in the spectra of the different compounds. The values of ΔE for the absorption bands in the visible region are also given. The values of ΔE for the absorption bands in the visible region are also given.

- 2.3 The circuit of a particular op-amp can be described by the circuit shown in Fig. E2.3. Suppose it is a unity-gain follower. For the case of $v_1 = 10 \text{ mV}$, $R = 10 \text{ k}\Omega$, and $\mu = 10^6$, find the value of the open-loop gain A .

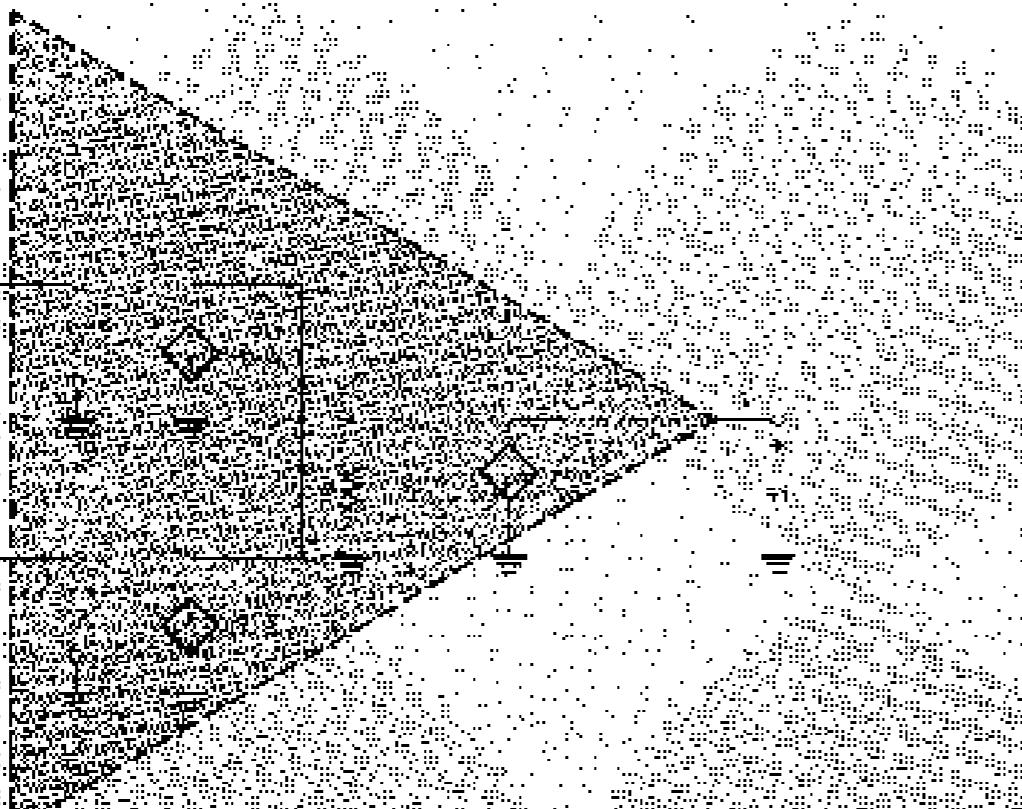


FIGURE E2.3 A circuit diagram showing an operational amplifier (op-amp) with its non-inverting input terminal 1 connected to ground. The inverting input terminal 2 is connected to the output terminal 3 through a resistor R . The output terminal 3 is also connected to ground. A voltage source v_1 is connected between terminal 1 and ground.

2.2 THE INVERTING CONFIGURATION

As mentioned above, op-amps are not used alone; rather, the op-amp is connected to passive components in a feedback circuit. There are two such basic circuit configurations employing an op-amp and two resistors: the inverting configuration, which is studied in this section, and the non-inverting configuration, which we shall study in the next section.

Figure 2.5 shows the inverting configuration. It consists of one op-amp and two resistors R_1 and R_2 . Resistor R_2 is connected from the output terminal of the op-amp, terminal 3, back to the inverting or negative input terminal, terminal 1. We speak of R_2 as applying negative feedback. If R_2 were connected between terminals 3 and 2 we would have called it positive feedback. Note also that R_2 closes the loop around the op-amp. In addition to closing R_2 , we have grounded terminal 2 and connected a resistor R_1 between terminal 1 and an input signal source

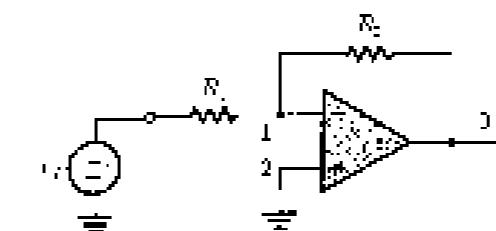


FIGURE 2.5 The inverting closed-loop configuration.

with a voltage v_1 . The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and ground). Terminal 3 is, of course, a convenient point to take the output, since the impedance level there is ideally zero. Thus the voltage v_3 will depend on the value of the current i_2 , right? Simplified to a load impedance connected between terminal 3 and ground,

2.2.1 The Closed-Loop Gain

We now wish to analyze the circuit in Fig. 2.5 to determine the closed-loop gain G , i.e.,

$$G = \frac{v_3}{v_1}$$

We will do so assuming the op-amp to be ideal. Figure 2.6(a) shows the equivalent circuit, and the analysis proceeds as follows: The gain A is very large (ideally infinite). If we assume the test circuit is "working" and predicting a finite output voltage at terminal 3, then the voltage between the op-amp input terminals should be negligibly small and ideally zero. Specifically, if we call the output voltage v_3 , then, by definition,

$$v_3 - v_1 = \frac{R_2}{A} = 0$$

It follows that the voltage at the inverting input terminal, v_1 , is given by $v_1 = v_3$. That is, because the gain A approaches infinity, the voltage v_1 approaches and ideally equals v_3 . In other words, the two input terminals "measure each other in potential." We also speak of a "virtual short circuit" that exists between the two input terminals. Here the word *virtual* should be emphasized, and we should not make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A virtual short circuit means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain A . The terminal 2 happens to be connected to ground; thus $v_2 = 0$ and $v_1 = 0$. We speak of terminal 1 as being a virtual ground, that is, having zero voltage but not physically connected to ground.

Now that we have determined v_1 we are in a position to apply Ohm's law and find the current i_2 through R_2 (see Fig. 2.6) as follows:

$$i_2 = \frac{v_3 - v_1}{R_2} = \frac{v_3 - 0}{R_2} = \frac{v_3}{R_2}$$

Where will this current go? It cannot go into the op-amp, since the load of v_3 has an infinite input impedance and hence draws zero current. It follows that i_2 will have to flow through R_1 to the low-impedance terminal 2. We can then apply Ohm's law to R_1 and determine v_0 , that is,

$$\begin{aligned} v_0 &= v_1 - i_2 R_1 \\ &= 0 - \frac{v_3}{R_2} R_1 \end{aligned}$$

Thus,

$$\frac{v_3}{v_1} = \frac{R_2}{R_1}$$

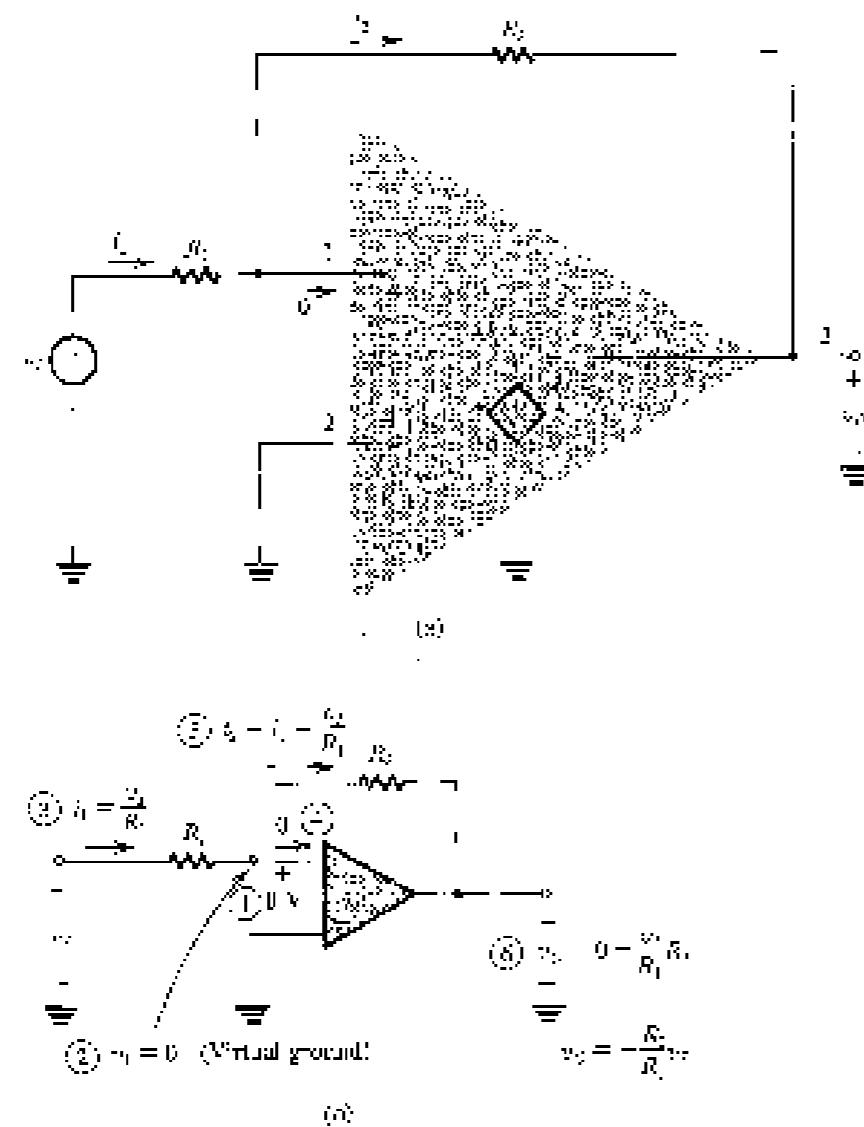


FIGURE 2.6 Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.

which is the required closed-loop gain. Figure 2.6(b) illustrates these steps and indicates by the circled numbers the order in which the analysis is performed.

We can see that the closed-loop gain is simply the ratio of the two resistances R_2 and R_1 . The minus sign means that the closed-loop amplifier provides signal inversion. Thus if $R_2/R_1 = 10$ and we apply at the input (v_1) a sine-wave signal of 1 V peak-to-peak, then the output (v_2) will be a sine wave of 10 V peak-to-peak and phase-shifted 180° with respect to the input sine wave. Because of the minus sign associated with the closed-loop gain, this configuration is called the **inverting configuration**.

The fact that the closed-loop gain depends entirely on external passive components (resistors R_1 and R_2) is very significant. It means that we can take the closed-loop gain as

constant as we want by selecting passive components of appropriate accuracy. It also means that the closed-loop gain is (ideally) independent of the open-loop gain. This is a dramatic illustration of negative feedback. We started out with an op-amp having very large gain A , and through applying negative feedback we have obtained a closed-loop gain R_2/R_1 that is much smaller than A but is stable and predictable. That is, we are trading gain for accuracy.

2.2.2 Effect of Finite Open-Loop Gain

The point just made are more clearly illustrated by deriving an expression for the closed-loop gain under the assumption that the op-amp open-loop gain is finite. Figure 2.7 shows the analysis. If we denote the current flowing in the voltage between the two input terminals of the op-amp will be i_1/A . Since the positive input terminal is grounded, the voltage at the negative input terminal must be $-v_1/A$. The current i_1 through R_1 can now be found from

$$i_1 = \frac{v_2 - (-v_1/A)}{R_1} = \frac{v_2 + v_1/A}{R_1}$$

The infinite input impedance of the op-amp causes the current i_1 to flow entirely through R_2 . The output voltage v_2 can thus be determined from

$$\begin{aligned} v_2 &= \frac{v_2}{A} + i_1 R_2 \\ &= -\frac{v_1}{A} + \left(\frac{v_2 + v_1/A}{R_1}\right) R_2 \end{aligned}$$

Collecting terms, the closed-loop gain G is found to

$$G = \frac{v_2}{v_1} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)A} \quad (2.5)$$

We note that as A approaches ∞ , G approaches the ideal value of $-R_2/R_1$. Also, from Fig. 2.7 we see that as A approaches ∞ , the voltage at the inverting input terminal approaches zero. This is the virtual-ground assumption we used in our dc analysis when the op-amp was assumed to be ideal. Finally, note that Eq. (2.5) in fact indicates the need to minimize the dependence of the closed-loop gain G on the value of the open-loop gain A , we should make

$$1 + \frac{R_2}{R_1} \ll A$$

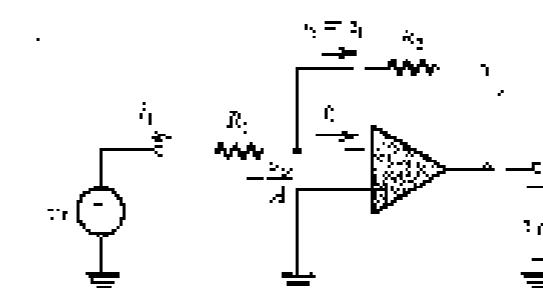


FIGURE 2.7 Analysis of the inverting configuration using the virtual-ground approximation.

Consider the inverting configuration with $R_1 = 1\text{ k}\Omega$ and $R_2 = 100\text{ k}\Omega$.

- Find the closed-loop gain for the cases $A = 10^3, 10^4, \text{ and } 10^5$. In each case determine the percentage error in the magnitude of G relative to the ideal value of R_2/R_1 (obtained with $A = \infty$). Also determine the voltage v_i that appears at the inverting input terminal when $v_o = 0.1\text{ V}$.
- If the open-loop gain A changes from 100,000 to 50,000 (i.e., drops by 50%), what is the corresponding percentage change in the magnitude of the closed-loop gain G ?

Solution

(a) Substituting the given values in Eq. (2.5), we obtain the values given in the following table where the percentage error ϵ is defined as

$$\epsilon = \frac{|A - (R_2/R_1)|}{(R_2/R_1)} \times 100$$

The values of v_i are obtained from $v_i = -v_o/A = Gv_o/A$ with $v_o = 0.1\text{ V}$

A	v_i	ϵ
10^3	-0.81	-0.1%
10^4	-0.001	-0.99%
10^5	-0.010	-0.10%

- (b) Using Eq. (2.5), we find that for $A = 50,000$, $G = 99.80$. Thus a -50% change in the open-loop gain results in a change of only -0.1% in the closed-loop gain!

2.2.3 Input and Output Resistances

Assuming an ideal op-amp with infinite open-loop gain, the input resistance of the closed-loop inverting amplifier of Fig. 2.5 is simply equal to R_1 . This can be seen from Fig. 2.6(b), where

$$R_i = \frac{v_i}{i_1} = \frac{R_1}{R_2/R_1} = R_1$$

Now recall that in Section 1.5 we learned that the amplifier input resistance forms a voltage divider with the resistance r_s of the source that feeds the amplifier. Thus, to avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. In the case of the inverting op-amp configuration we are studying, to make R_i high we should select a high value for R_1 . However, if the required gain R_2/R_1 is also high, then R_1 could become impractically large (e.g., greater than a few megohms). We may conclude that the inverting configuration suffers from a low input resistance. A solution to this problem is discussed in Example 2.7 below.

Since the output of the inverting configuration is taken at the terminals of the ideal voltage source ($v_{o1} = v_o$) (see Fig. 2.6), it follows that the output resistance of the closed-loop amplifier is zero.

Assuming the op-amp to be ideal, derive an expression for the closed-loop gain v_{o2}/v_i of the circuit shown in Fig. 2.8, use this circuit as a buffer with a gain of 100 and r_s input resistance of $1\text{ M}\Omega$. Assume that for practical reasons it is required not to use resistors greater than $1\text{ M}\Omega$. Compare your design with that based on the inverting configuration of Fig. 2.5.

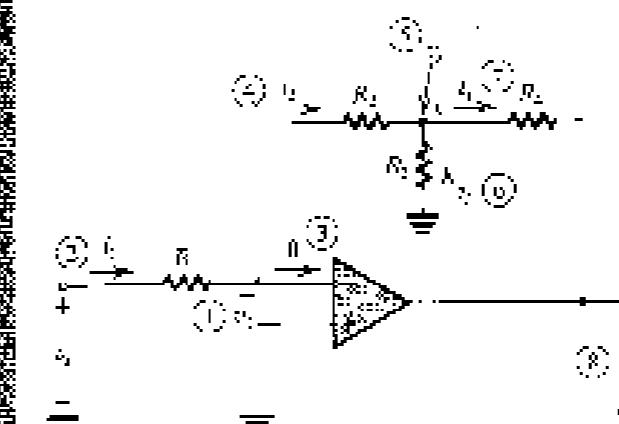


FIGURE 2.8 Circuit for Example 2.8. The circled numbers indicate the order of the steps in the analysis.

Solution

From your begin at the inverting input terminal of the op-amp, where the voltage is

$$v_i = \frac{-v_o}{A} = \frac{v_o}{A} = 0$$

Here we have assumed that the circuit is "swinging" and producing a finite output voltage v_o . Knowing v_i , we can determine the current i_1 as follows:

$$i_1 = \frac{v_i}{R_1} = \frac{0}{R_1} = \frac{v_o}{R_1} = \frac{i_2}{R_1}$$

Since zero current flows into the inverting input terminal, all of i_1 will flow through R_2 , and thus

$$i_2 = i_1 = \frac{v_o}{R_1}$$

Now we can determine the voltage at node 1:

$$v_{o1} = v_i + i_2 R_2 = 0 + \frac{v_o}{R_1} R_2 = -\frac{R_2}{R_1} v_o$$

This in turn enables us to find the current i_3 :

$$i_3 = \frac{v_o - v_{o1}}{R_3} = \frac{R_2}{R_1 R_3} v_o$$

Next, a node equation at node δ :

$$i = i_2 - i_1 = \frac{i_2}{R_1} + \frac{R_2}{R_1 R_2} i_1$$

Finally, we can determine v_o from

$$\begin{aligned} v_o &= v_2 - i_2 R_2 \\ &= -\frac{R_2}{R_1} i_1 + \left(\frac{R_2}{R_1} + \frac{R_3}{R_1 R_2} \right) R_4 \end{aligned}$$

Thus the voltage gain is given by

$$\frac{v_o}{v_1} = -\left[\frac{R_2}{R_1} \cdot \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1} \right) \right]$$

which can be written in the form

$$\frac{v_o}{v_1} = -\left[\frac{R_2}{R_1} \left(1 + \frac{R_1}{R_2} \right) \frac{R_4}{R_3} \right]$$

Now, since an input resistance of $1\text{ M}\Omega$ is required, we select $R_1 = 1\text{ M}\Omega$. Then, with the limits of using resistors no greater than $5\text{ M}\Omega$, the maximum value possible for the first factor in the gain expression is 1 and is obtained by selecting $R_2 = 1\text{ M}\Omega$. To obtain a gain of -100 , R_3 and R_4 must be selected so that the second factor in the gain expression is < 0 . If we select the maximum of power (i.e., this example) value of $1\text{ M}\Omega$ for R_3 , then the required value of R_4 can be calculated to be $10.2\text{ k}\Omega$. Thus this circuit utilizes three $1\text{-M}\Omega$ resistors and a $10.2\text{-k}\Omega$ resistor. In comparison, if the inverting op-amp which was used with $R_1 = 1\text{ M}\Omega$ we would have required a feedback resistor of $100\text{ M}\Omega$, an impractically large value!

Before leaving this example, it is insightful to inquire into the mechanism by which the circuit is able to realize a large voltage gain without using large resistances in the feedback path. Toward that end, observe that, because of the virtual ground at the inverting input terminal of the op-amp, R_2 and R_3 are in effect in parallel. Thus, by making R_1 lower than R_2 by, say, a factor k (i.e., $R_1 = R_2/k$ where $k > 1$), R_1 is forced to carry a current k times that of R_2 . Thus, while $i = i_2$, $i_1 = 0$, and $i = (1/k)i_2$, it is the current multiplication by a factor of $k = 10$ that enables a large voltage drop developed across R_2 and hence a large v_o without using a large value for R_2 . Notice also that the current through R_2 is independent of the value of R_3 . It follows that the circuit can be used as a current amplifier as shown in Fig. 2.9.

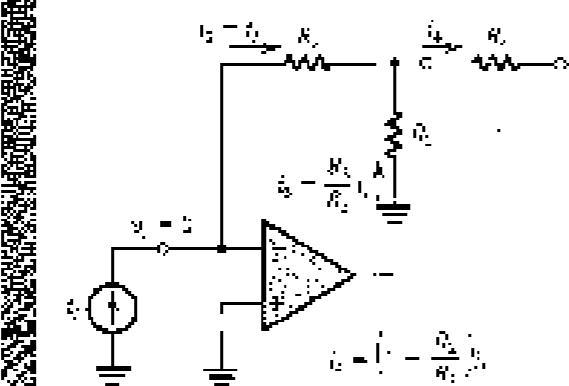


FIGURE 2.9 A current amplifier based on the circuit of Fig. 2.8.1 is using the values in its output is equal to R_1 . It has a voltage gain of $1 + R_2/R_1$, a low input resistance, and a high output resistance. The load (i_L), however, must be floating (i.e., neither of its terminals may be connected to ground).

EXERCISES

2.4. The inverting configuration of Fig. 2.8.1 is used with the following component values:

$R_1 = 10\text{ k}\Omega$; $R_2 = 1\text{ M}\Omega$

2.5. The circuit shown in Fig. 2.8.1 is used with the following component values:

$R_1 = 10\text{ k}\Omega$; $R_2 = 1\text{ M}\Omega$; $R_3 = 100\text{ k}\Omega$

2.6. Find the voltage gain of the inverting configuration of Fig. 2.8.1 if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.7. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.8. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.9. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.10. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.11. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

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2.49. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.50. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

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2.72. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

2.73. Find the output voltage if the input voltage is $v_1 = 10\text{ mV}$ and the output voltage is $v_o = 10\text{ V}$.

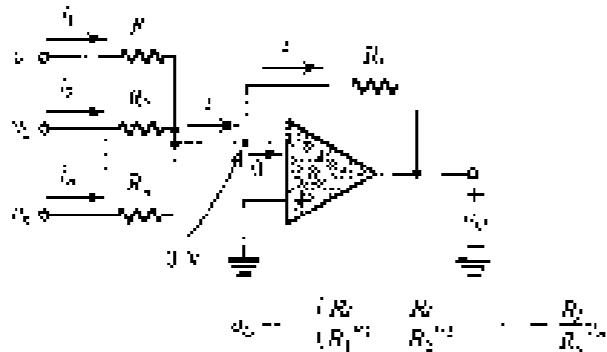


FIGURE 2.10 A weighted summer.

All these currents sum together to produce the current i_O at the op-amp output:

$$i_O = (i_1 - i_2) + \dots + i_n \quad (2.6)$$

will be forced to flow through R_2 (since no current flows into the input terminals of an ideal op-amp). The output voltage v_O may now be determined by another application of Ohm's law:

$$v_O = 0 - iR_2 = -iR_2$$

Thus,

$$v_O = \frac{iR_1v_1 + R_2v_2 + \dots + R_2v_n}{R_1 + R_2 + \dots + R_n} \quad (2.7)$$

That is, the output voltage is a weighted sum of the input signals v_1, v_2, \dots, v_n . This circuit is therefore called a weighted summer. Note that each summing coefficient may be independently adjusted by adjusting the corresponding "feed-in" resistor (R_1 to R_n). This also means that which ground-simulating circuit adjustment is a direct consequence of the virtual ground that exists at the inverting op-amp terminal. As the reader will soon come to appreciate, virtual grounds are extremely "flabby." The weighted summer of Fig. 2.10 has the constraint that all the summing coefficients are of the same sign. The need occasionally arises for summing signals with opposite signs. Such a function can be implemented using two op-amps as shown in Fig. 2.11. Assuming ideal op-amps, it can be easily shown that the output voltage is given by

$$v_O = v_1 \left(\frac{R_2/R_1}{R_2/R_1 + R_2/R_2} \right) + v_2 \left(\frac{R_2/R_2}{R_2/R_1 + R_2/R_2} \right) + v_3 \left(\frac{R_2/R_3}{R_2/R_1 + R_2/R_3} \right) \quad (2.8)$$

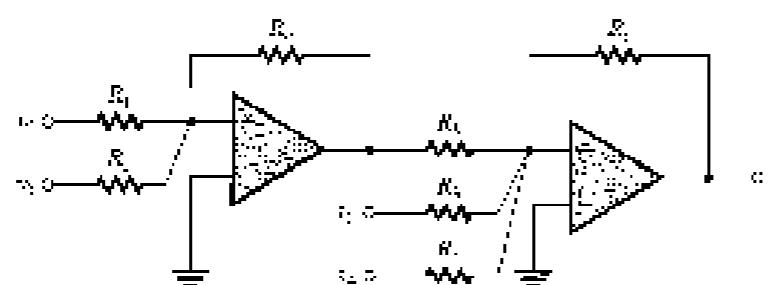


FIGURE 2.11 A weighted summer capable of implementing summing coefficients of both signs.

EXERCISES

- 2.1** Design a weighted summer circuit to fulfill the following requirements: the output voltage v_O and the input voltage v_1 are related by the equation $v_O = 2v_1 + 3v_2 + 5v_3 + 7v_4$, where v_1, v_2, v_3, v_4 are the input voltages. The output voltage v_O is to be fed back to the inverting input of the op-amp with a gain of -10 . Assume the op-amp has a unity-gain bandwidth of 10^6 Hz. Find the required values of the resistors R_1, R_2, R_3, R_4 and the feedback resistor R_f . (Ans. $R_1 = 10\text{k}\Omega, R_2 = 3\text{k}\Omega, R_3 = 5\text{k}\Omega, R_4 = 7\text{k}\Omega, R_f = 100\text{k}\Omega$)
- 2.2** Use the circuit of Fig. 2.11 to design a weighted summer that provides the output voltage $v_O = 2v_1 + 3v_2 + 5v_3 + 7v_4$. Assume the op-amps have a unity-gain bandwidth of 10^6 Hz. Find the required values of the resistors R_1, R_2, R_3, R_4 and the feedback resistor R_f . (Ans. A possible choice is $R_1 = 5\text{k}\Omega, R_2 = 15\text{k}\Omega, R_3 = 10\text{k}\Omega, R_4 = 25\text{k}\Omega, R_f = 100\text{k}\Omega$)

2.3 THE NONINVERTING CONFIGURATION

The second closed-loop configuration we shall study is shown in Fig. 2.12. Here the input signal v_1 is applied directly to the positive input terminal of the op-amp while one terminal of R_1 is connected to ground.

2.3.1 The Closed-Loop Gain

Analysis of the noninverting circuit to determine its closed-loop gain, (v_O/v_1) is illustrated in Fig. 2.13. Notice that the order of the steps in the analysis is indicated by circled numbers.

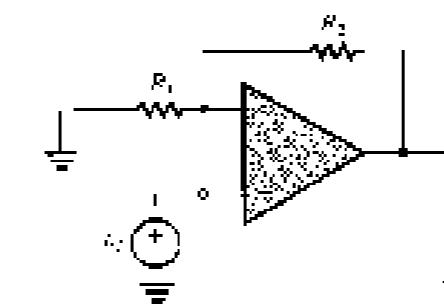


FIGURE 2.12 The noninverting configuration.

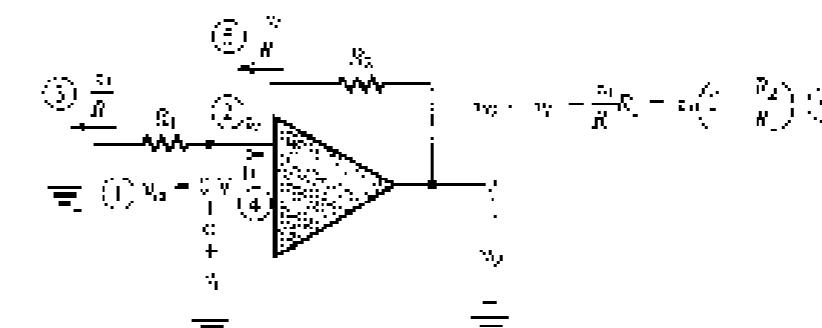


FIGURE 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

Assuming that the op-amp is ideal with infinite gain, a virtual short circuit exists between its two input terminals. Hence the difference input signal is

$$v_{d1} = \frac{v_2}{A} = 0 \quad \text{for } A = \infty$$

Hence the voltage at the inverting input terminal will be equal to that at the noninverting input terminal, which is the applied voltage v_1 . The current through R_2 can then be determined as v_1/R_2 . Because of the infinite input impedance of the op-amp, this current will flow through R_1 , as shown in Fig. 2.13. Note the output voltage can be determined from

$$v_0 = v_1 + \frac{v_1}{R_1} R_2$$

which yields

$$\frac{v_0}{v_1} = 1 + \frac{R_2}{R_1} \quad (2.9)$$

Further insight into the operation of the noninverting configuration can be obtained by considering the following: Since the current in the inverting input is zero, the circuit composed of R_1 and R_2 acts in effect as a voltage divider leading a fraction of the output voltage back to the inverting input terminal of the op-amp; that is,

$$v_{d2} = v_0 \left[\frac{R_1}{R_1 + R_2} \right] \quad (2.10)$$

Since the infinite open-loop gain and the resulting virtual short circuit between the two input terminals of the op-amp forces this voltage to be equal to the applied to the positive input terminal, that is

$$v_0 \left[\frac{R_1}{R_1 + R_2} \right] = v_1$$

which yields the gain expression given in Eq. (2.9).

This is an appropriate point to reflect further on the action of the negative feedback present in the noninverting circuit of Fig. 2.12. Let v_1 increase. Such a change in v_1 will cause v_{d2} to increase, and v_0 will correspondingly increase as a result of the high (ideally infinite) gain of the op-amp. However, a fraction of the increase in v_0 will be fed back to the inverting input terminal of the op-amp through the (R_1, R_2) voltage divider. The result of this feedback will be to counteract the increase in v_{d2} , driving v_{d2} back to zero, about a higher value of v_1 that corresponds to the increased value of v_0 . This degenerative action, or negative feedback gives rise to the alternative name degenerative feedback. Finally, note that the argument above applies equally well if v_1 decreases. A formal and detailed study of feedback is presented in Chapter 8.

2.3.2 Characteristics of the Noninverting Configuration

The gain of the noninverting configuration is positive—hence the name noninverting. The input impedance of this closed-loop amplifier is ideally infinite, since no current flows into the positive input terminal of the op-amp. The output of the noninverting amplifier is taken at the terminals of the ideal voltage source ($v_0 = v_1$; see the open-loop equivalent circuit in Fig. 2.4), thus the output resistance of the noninverting configuration is zero.

2.3.3 Effect of Finite Open-Loop Gain

As we have done for the inverting configuration, we now consider the effect of the finite op-amp open-loop gain A on the gain of the noninverting configuration. Assuming the op-amp

is ideal except for having a finite open-loop gain A , it can be shown that the closed-loop gain of the noninverting amplifier circuit of Fig. 2.12 is given by

$$\frac{v_0}{v_1} = \frac{1 + (R_2/R_1)}{1 + (R_2/R_1) - \frac{(R_2/R_1)}{A}} \quad (2.11)$$

Observe that the denominator is “deletion” in that for the case of the inverting configuration (Fig. 2.5), this is an coincidence; it is a result of having both the inverting and the noninverting configurations have the same feedback loop, which can be readily seen if the input signal source is chosen as v_1 . When calculated, the numerators, however, are different, for the inverter gives the ideal or nominal closed-loop gain $(-R_2/R_1)$ for the inverting configuration, and $1 + R_2/R_1$ for the noninverting configuration. Finally, we note (with reassurance) that the gain expression in Eq. (2.11) reduces to the ideal value for $A = \infty$. In fact, it approximates the ideal value for

$$A \gg 1 + \frac{R_2}{R_1} \quad (2.12)$$

This is the same condition as in the inverting configuration, except that here the quantity on the right-hand side is the nominal closed-loop gain.

2.3.4 The Voltage Follower

The property of high input impedance is a very desirable feature of the noninverting configuration. It enables using this circuit as a buffer amplifier to connect a source with a high impedance to a low-impedance load. We have discussed the need for buffer amplifiers in Section 1.5. In many applications the buffer amplifier is not required to provide any voltage gain; rather, it is used mainly as an impedance transformer or a power amplifier. In such cases we may make $R_2 = 0$ and $R_1 \rightarrow \infty$ to obtain the unity-gain amplifier shown in Fig. 2.14(a). This circuit is commonly referred to as a voltage follower, since the output “follows” the input. In the ideal case, $v_0 = v_1$, $R_{out} = 0$, and the circuit has the equivalent circuit shown in Fig. 2.14(b).

Since in the voltage-follower circuit the entire output is fed back to the inverting input, the circuit is said to have 100% negative feedback. The infinite gain of the op-amp then acts to make $v_d = 0$ and hence $v_0 = v_1$. Observe that the output is elegant in its simplicity!

Since the noninverting configuration has a gain greater than or equal to unity, depending on the source of A/R_1 , some prefer to call it a follower with gain.”

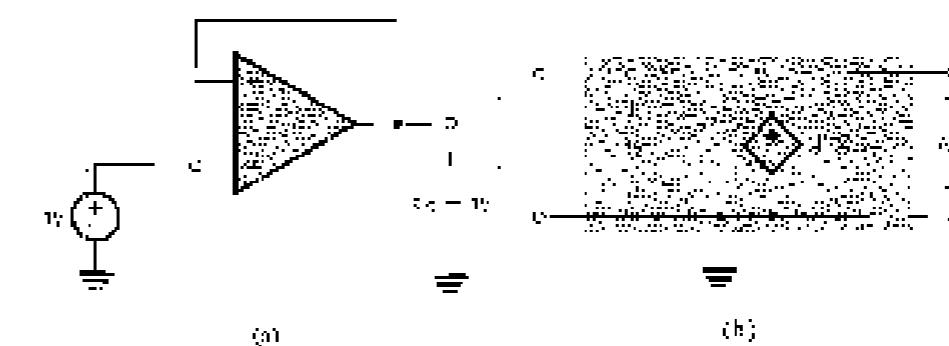
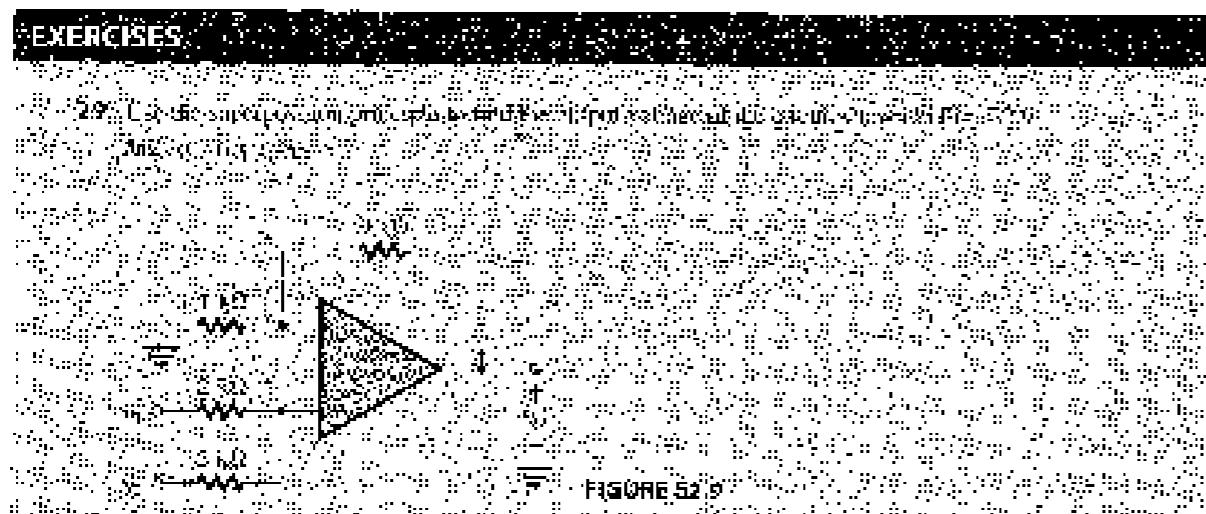


FIGURE 2.14 (a) The unity-gain buffer or follower amplifier; (b) its open-circuit model.



• FIGURE 5

Figure 10 shows the effect of the parameter α on the performance of the proposed scheme. The results show that the proposed scheme is robust to the variation of α .

12.11. The following are the steps to generate a generic QoS rule in the network using digital certificate of 11.12. The configuration is as follows:

2. In comparison to the design in the circuit of Fig. 1, 2 has full symmetry which makes the device more robust. The $L_1 = L_2$ and $A_1 = A_2$ make the performance insensitive to the variation of the inductor value. Each coil has 10 turns. The inductance of each coil is 1.1 nH. The bias voltage $V_B = 10$ mV. The current in each coil is the average current of the two coils, measured in the circuit.

In Fig. 12.13 find the values of α_1 , α_2 , α_3 , α_4 , and α_5 which satisfy the vector current equation $\chi_1 = \alpha_1 \chi_2 + \alpha_2 \chi_3 + \alpha_3 \chi_4 + \alpha_4 \chi_5 + \alpha_5 \chi_6$.

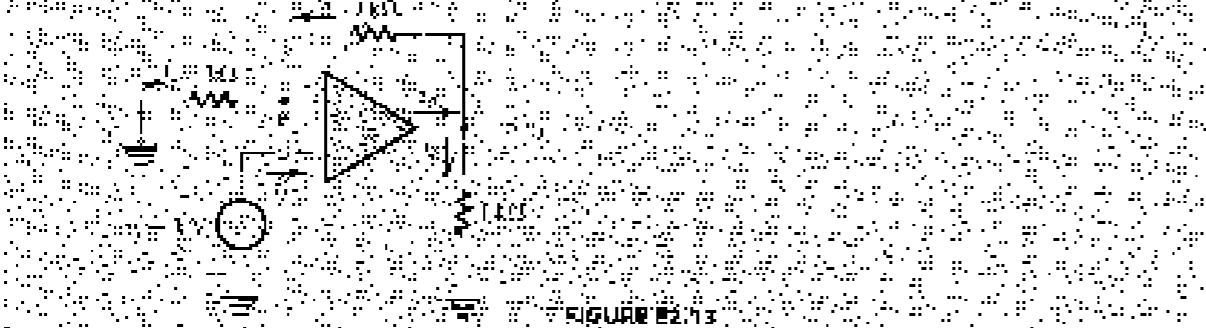


FIGURE E

74-5. *Leptodora* (*Leptodora*) *leptophylla* (L.) Schlecht. *L. lepto-* *phylla*. - A slender, erect, branched, yellowish-green, aquatic plant, 1-2 m. tall, with a basal tuft of long, narrow, linear leaves, and numerous smaller, opposite, linear, lanceolate leaves on the upper part of the stem. The flowers are numerous, small, yellowish, bell-shaped, and arranged in whorls around the stem. The fruit is a small, round, yellowish, pointed capsule.

2.4 DIFFERENCE AMPLIFIERS

Having studied the two basic configurations of op-amp circuits together with some of their direct applications, we are now ready to consider a somewhat more involved but very important application. Specifically, we shall study the use of op-amps to design differentiators or differential amplifiers.³ A difference amplifier is one that responds to the difference between the two signals applied at its inputs and thereby rejects signals that are common to the two inputs. The representation of signals in terms of their differential and common-mode components was given in Fig. 2.4. It is repeated here in Fig. 2.15 with slightly different symbols to serve as the input signals for the difference amplifiers we shall turn to next. Although ideally the difference amplifier will amplify only the differential-mode signal v_d and reject completely the common-mode input signal v_{cm} , practical circuits will have an output voltage v_o given by

$$v_0 = A_0 \alpha_0 + A_{-1} \beta_0 \quad (12.14)$$

where A_{d} denotes the amplifier differential gain and A_{cm} denotes its common-mode gain (already zero). The offload coefficient (*common-mode rejection ratio*) is measured as the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by a measure known as the common-mode rejection ratio (CMRR), defined as

$$CMRR = 20 \log_{10} \frac{|A_{av}|}{|A_{noise}|} \quad (2.14)$$

The need for difference amplifiers arises frequently in the design of electronic systems, especially those employed in the human brain. As a common example, consider a transducer providing a small (e.g., 1 mV) signal between its two output terminals while each of the two wires leading from the transducer terminals to the measuring instrument may have a large rate reference signal (e.g., 1 V) relative to the circuit ground. The instrument input end obviously needs a difference amplifier.

Before we proceed any further, we should address a question that the reader might have: The option is *far* more difficult than simple; why not just use an *objdump*? The answer is that, for very high (ideally infinite) γ , in which case *objdump* makes it impossible to use by itself.

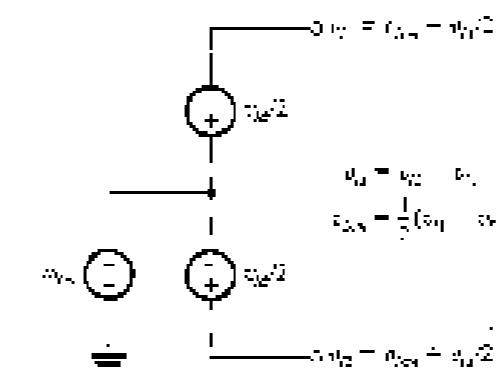


FIGURE 2.15 Representing the local spectral multi-technique amplitude in terms of three different scale components.

⁷The terms *affine space* and *affine coordinate system* usually used to describe something different than parallel types. For our purposes at this point the distinction is not sufficiently significant. We will be more precise next to the end of this section.

Rather, as we did before, we have to devise an appropriate feedback network to connect to the output to create a circuit whose closed-loop gain is finite, predictable, and stable.

2.4.1 A Single Op-Amp Difference Amplifier

Our first attempt at designing a difference amplifier is motivated by the observation that the gain of the noninverting amplifier configuration is positive ($1 + R_2/R_1$), while that of the inverting configuration is negative ($-R_2/R_1$). Combining the two configurations together is thus a step in the right direction—namely, getting the difference between two input signals. Of course, we have to make the two-gain magnitudes equal in order to reject common-mode signals. This, however, can be easily achieved by attenuating the positive input signal to reduce the gain of the positive path from $(1 + R_2/R_1)$ to (R_2/R_1) . The resulting circuit would then look like that shown in Fig. 2.16, where the attenuation in the positive input path is achieved by the voltage divider (R_3, R_4) . The voltage ratio of this voltage divider can be determined to be

$$\frac{R_4}{R_3 + R_4} = \frac{R_3}{R_3 + R_4} = \frac{R_3}{R_1}$$

which can be put in the form

$$\frac{R_4}{R_3 + R_4} = \frac{R_3}{R_2 + R_3}$$

This condition is satisfied by selecting

$$\frac{R_4}{R_3} = \frac{R_3}{R_2} \quad (2.15)$$

This completes our work. However, we have perhaps proceeded a little too fast! Let's step back and verify that the circuit in Fig. 2.16 with R_3 and R_4 selected according to Eq. (2.15) does in fact function as a difference amplifier. Specifically, we wish to determine the output voltage v_{o1} in terms of v_{i1} and v_{i2} . Toward that end, we observe that the circuit is linear, and thus we can use superposition.

To apply superposition, we first reduce v_{i2} to zero—that is, ground the terminal to which v_{i2} is applied—and then find the corresponding output voltage, which will be the voltage to v_{o1} . We denote this current voltage v_{o1} . Its value may be found from the circuit in Fig. 2.17(a), which we recognize as that of the inverting configuration. The existence of R_3 and R_4 does not affect the gain expression, since no current flows through either of them. Thus,

$$v_{o1} = -\frac{R_2}{R_1} v_{i1}$$

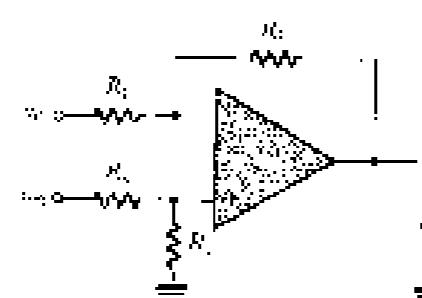


FIGURE 2.16 A difference amplifier.

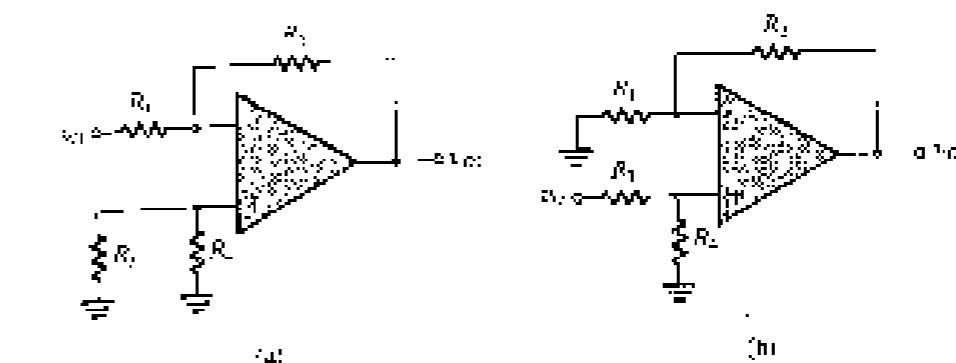


FIGURE 2.17 Application of superposition to the analysis of the circuit of Fig. 2.16.

Next we reduce v_{i1} to zero and evaluate the corresponding output voltage v_{o2} . The circuit will now take the form shown in Fig. 2.17(b), which we recognize as the noninverting configuration with an additional voltage divider made up of R_1 and R_2 , connected to the input v_{i2} . The output voltage v_{o2} is then given by

$$v_{o2} = v_{i2} \frac{R_1}{R_1 + R_2} \left[1 + \frac{R_2}{R_1} \right] = \frac{R_2}{R_1} v_{i2}$$

where we have utilized Eq. (2.15).

The superposition principle tells us that the output voltage v_o is equal to the sum of v_{o1} and v_{o2} . Thus we have

$$v_o = \frac{R_2}{R_1} (v_{i2} - v_{i1}) = \frac{R_2}{R_1} v_{i2} \quad (2.16)$$

Thus, as expected, the circuit acts as a difference amplifier with a differential gain A_o of

$$A_o = \frac{R_2}{R_1} \quad (2.17)$$

Of course this is predicated on the op-amp being ideal and furthermore on the selection of R_3 and R_4 such that their ratio matches that of R_1 and R_2 (Eq. 2.15). To make this matching requirement a little easier to satisfy, we usually select

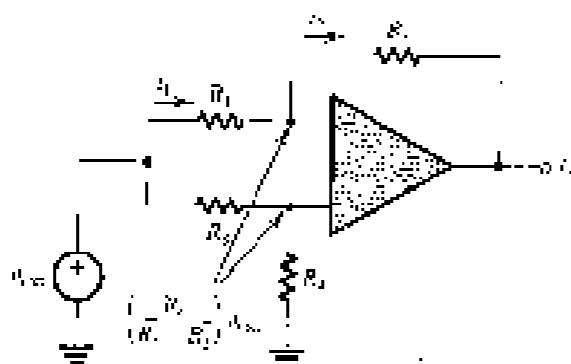
$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Let's next consider the circuit with only a common-mode signal applied to the input, as shown in Fig. 2.18. The figure also shows some of the analysis steps. Thus,

$$\begin{aligned} i_o &= \frac{1}{R_1} \left| v_{i1,CM} - R_1 \sqrt{R_2 R_4} v_{o1} \right| \\ &= v_{i1,CM} \frac{R_1}{R_1 + R_2 R_4} \end{aligned} \quad (2.18)$$

The output voltage can now be found from

$$v_o = \frac{R_2}{R_1 + R_2} v_{i1,CM} - i_o R_2$$

FIGURE 2.18 Analysis of the difference amplifier in its common-mode gain $A_{cm} = v_o/v_{in}$.

After applying $i_1 = i_2$ and for v_o from Eq. (2.18),

$$\begin{aligned} v_o &= \frac{R_4}{R_1 + R_2} v_{in} = \frac{R_2 \cdot R_3}{R_1 \cdot R_2 + R_3} v_{in} \\ &= \frac{R_3}{R_1 + R_2} \left(1 - \frac{R_1 \cdot R_2}{R_1 \cdot R_2 + R_3} \right) v_{in} \end{aligned}$$

Thus,

$$A_{cm} = \frac{v_o}{v_{in}} = \frac{R_3}{R_1 + R_2} \left(1 - \frac{R_1 \cdot R_2}{R_1 \cdot R_2 + R_3} \right) \quad (2.19)$$

For the design with the resistances selected according to Eq. (2.17), we obtain

$$A_{cm} = 0$$

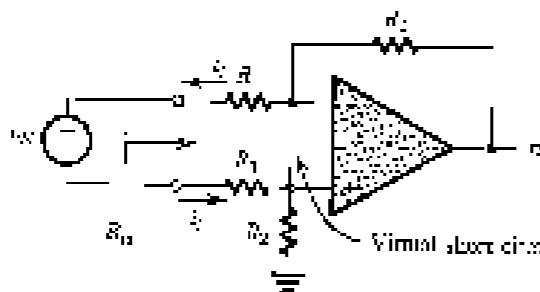
We expect $v_o = 0$. Note, however, that any mismatch in the resistance ratios can make A_{cm} nonzero, and hence CMRR finite.

In addition to rejecting common-mode signals, a CMRR amplifier is usually required to have a high input resistance. To find the input resistance between the two input terminals (i.e., the resistance seen by v_{in}), called the differential input resistance R_{di} , consider Fig. 2.19. Here we have assumed that the resistors are selected so that

$$R_1 = R_2 \quad \text{and} \quad R_3 = R_4$$

Now

$$R_{di} = \frac{R_1}{2}$$

FIGURE 2.19 Finding the differential resistance of the difference amplifier for the case $R_2 = R_1$ and $R_3 = R_4$.

Since the two input terminals of the op amp track each other in potential, we may write a loop equation and obtain

$$v_o = R_3 i_1 = 0 + R_3 i_2$$

Thus,

$$R_3 i_1 = 2 R_1 i_2 \quad (2.20)$$

Note that if the amplifier is required to have a large differential gain (R_3/R_1), then R_1 will necessarily will be relatively small, and the input resistance will be correspondingly low, a drawback of this circuit. Another drawback of the circuit is that it is not easy to view the differential gain of the amplifier. Both of these drawbacks are overcome in the instrumentation amplifier discussed next.

EXERCISES

- 2.18 Consider the difference amplifier circuit in Fig. 2.16 for the case of $V_{in} = 10\text{ mV}$ and $R_1 = R_2 = 1\text{k}\Omega$.
 (a) Find the value of the differential gain A_d . (b) Find the value of the common-mode gain A_{cm} and the input resistance R_{di} . (c) If the voltage noise of the source is $1\text{nV}/\sqrt{\text{Hz}}$, what will be within the noise at the output? (d) Find the CMRR of the circuit assuming a noise voltage of $1\text{nV}/\sqrt{\text{Hz}}$ and a noise current of $1\text{pA}/\sqrt{\text{Hz}}$. (e) If the noise voltage is $0.1\text{nV}/\sqrt{\text{Hz}}$ and the noise current is $0.1\text{pA}/\sqrt{\text{Hz}}$, what will be the noise at the output?
- 2.19 First solve for the resistances in Fig. 2.16 so that the circuit behaves as a difference amplifier with a differential resistance of $20\text{k}\Omega$ and a gain of 10.
 (a) $R_1 = R_2 = 1\text{k}\Omega$; $R_3 = R_4 = 10\text{k}\Omega$
 (b) $R_1 = R_2 = 1\text{k}\Omega$; $R_3 = R_4 = 100\text{k}\Omega$

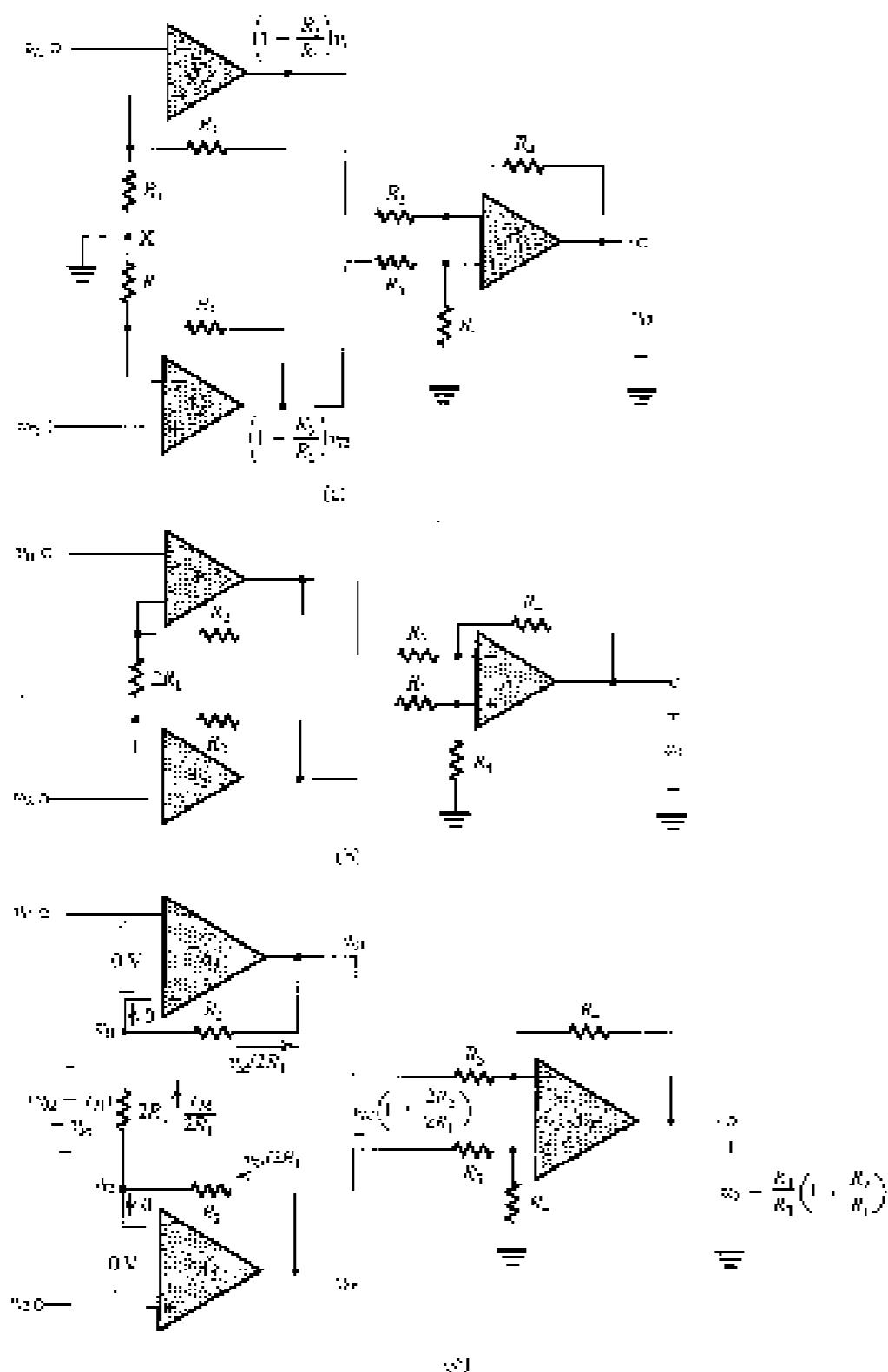
2.4.3 A Superior Circuit—The Instrumentation Amplifier

The low-input-resistance problem of the difference amplifier of Fig. 2.16 can be solved by buffering the two input terminals using voltage followers; that is, a voltage follower of the type in Fig. 2.14 is connected between each input terminal and the corresponding input terminal of the difference amplifier. However, if we are going to use two additional op amps, we should ask the question: Can we get more from them than just impedance buffering? An obvious answer would be that we should try to get some voltage gain. It is especially interesting that we can achieve this without compromising the high input resistance simply by using followers with gain rather than unity-gain followers. Achieving some or indeed the bulk of the required gain in this new first stage of the differential amplifier eases the burden on the difference amplifier in the second stage, leaving it to its main task of amplifying the differentiating function and common-mode rejection.

The resulting circuit is shown in Fig. 2.20(a). It consists of two stages. The first stage is formed by op amps A_1 and A_2 and their associated resistors, and the second stage is the buffer-amplifier difference amplifier formed by op amp A_3 and its four associated resistors. Observe that as we set out to do, each of A_1 and A_2 is connected in the noninverting configuration and thus receives a gain of $(1 + R_2/R_1)$. It follows that each of v_{o1} and v_{o2} is amplified by this factor, and the resulting amplifier signals appear at the outputs of A_1 and A_2 , respectively.

The difference amplifier in the second stage operates on the difference signal $(1 + R_4/R_3)v_{o2} - v_{o1} = (1 - R_2/R_1)v_o$, and provides at its output

$$v_o = \frac{R_3}{R_4} \left(1 + \frac{R_2}{R_1} \right) v_o$$



Observe that proper differential operation does not depend on the matching of the two resistors R_2 . Indeed, if one of the two is off-ditect value, say R_2' , the expression for A_2 becomes

$$A_2 = \frac{R_2}{R_1} \left(1 + \frac{R_2 + R_2'}{2R_1} \right) \quad (2.23)$$

Consider next what happens when the two input terminals are connected together to a common-mode input voltage v_{cm} . It is easy to see that an equal voltage appears at the negative input terminals of A_1 and A_2 , causing the current through $2R_1$ to be zero. Thus there will be no current flowing at the R_2 resistors, and the voltages at the output terminals of A_1 and A_2 will be equal to the input voltage v_{cm} . Thus the first stage no longer amplifies, and simply propagates v_{cm} to its two output terminals, where they are subtracted to produce a zero-common-mode output by A_3 . The difference amplifier in the second stage, however, now has a much improved situation at its input: The common-mode signal has been amplified by $(1 + R_2/R_1)$ while the common-mode voltage remained unchanged.

Finally, we observe from the expression in Eq. (2.23) that the gain can be varied by changing only one resistor, $2R_1$. We conclude that this is an excellent differential-amplifier circuit and is widely employed as an instrumentation amplifier; that is, as the input circuitry used in a variety of electronic instruments.

Design Exercise 2.20 Design the instrumentation amplifier circuit in Fig. 2.20(b) to provide a gain that can be varied over the range of 3 to 1000 utilizing a 100-kΩ variable resistance (a potentiometer, or "pot" for short).

Solution

It is usually preferable to obtain all the required gain in the first stage, leaving the second stage to perform the task of taking the difference between the outputs of the first stage and thereby selecting the common-mode signal. In other words, the second stage is usually designed for a gain of 1. Adopting this approach, we select all the second-stage resistors to be equal to a practically convenient value, say 10 kΩ. The problem then reduces to designing the first stage to realize a gain adjustable over the range of 3 to 1000. Implementing $2R_1$ as the series combination of a fixed resistor R_1 and the variable resistor R_2 , obtained using the 100-ohm (Fig. 2.21), we can write

$$1 + \frac{2R_2}{R_1 + R_2} = 2 \text{ to } 1000$$

Thus,

$$\frac{2R_2}{R_1} = 1000$$

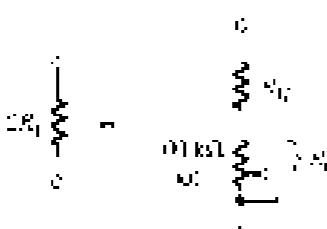


FIGURE 2.21 To make the gain of the circuit in Fig. 2.20(a) variable, $2R_1$ is implemented as the series combination of a fixed resistor R_1 and a variable resistor R_2 . Resistor R_1 is set to yield the maximum common-mode gain of 1000.

and

$$1 + \frac{2R_2}{R_1 + 100 \text{ k}\Omega} = 2$$

These two equations yield $R_1 = 100 \text{ k}\Omega$ and $R_2 = 50.000 \text{ k}\Omega$. Other practical values may be selected: for instance, $R_1 = 100 \text{ k}\Omega$ and $R_2 = 49.999 \text{ k}\Omega$ (both values are available as standard 1% tolerance metal-film resistors, see Appendix G) results in a gain covering approx. nearly the required range.

EXERCISES

- 2.17 Consider the instrumentation amplifier in Fig. 2.20(b) with a feedback voltage of $v_{fb} = -1000 v_{in}$, $R_1 = 0.5 \text{ k}\Omega$, and $R_2 = 10 \text{ k}\Omega$. Find the output voltage and bandwidth of the circuit. Assume $v_{cm} = 0$ and $v_{in} = 10 \text{ mV}$ peak-to-peak. (Ans.: $v_{out} = 10 \text{ V}$ peak-to-peak, $v_{fb} = -540.000 \text{ mV}$ peak-to-peak, $BW = 100 \text{ Hz}$)
- 2.18 A 1000-ohm potentiometer is used to vary the gain of the circuit in Fig. 2.20(b). If the output voltage is to remain constant at 10 V, find the required gain range of the circuit. (Ans.: $1000 \leq 1 + R_2/R_1 \leq 10000$, $R_1 = 10 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$)
- 2.19 A 1000-ohm potentiometer is used to vary the gain of the circuit in Fig. 2.20(b). If the output voltage is to remain constant at 10 V, find the required gain range of the circuit. (Ans.: $1000 \leq 1 + R_2/R_1 \leq 10000$, $R_1 = 10 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$)

2.5 EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH ON CIRCUIT PERFORMANCE

Above we defined the ideal op amp, and we presented a number of circuit applications of op amps. The analysis of these circuits assumed the op amps to be ideal. Although in many applications such an assumption is not a bad one, a circuit designer has to be thoroughly familiar with the characteristics of practical op amps and the effects of such characteristics on the performance of op-amp circuits. Only then will the designer be able to use the op amp intelligently, especially if the application at hand is not a straightforward one. The nonideal properties of op amps will, of course, limit the range of operation of the circuits analyzed in the previous examples.

In this and the two sections that follow, we consider some of the important nonideal properties of the op amp.³ We do this by treating one parameter at a time, beginning in this section with the most serious op-amp nonlinearities, i.e., finite gain and limited bandwidth.

2.5.1 Frequency Dependence of the Open-Loop Gain

The differential open-loop gain of an op amp is not infinite; rather, it is finite and decreases with frequency. Figure 2.22 shows a plot for A_v with the numbers typical of most commercially available general-purpose op amps (such as the 741-type op amp, which is available from many semiconductor manufacturers and whose internal circuit is studied in Chapter 9).

³ We should note that real op-amps have nonlinear effects addition to those discussed in this chapter. These include finite (nonzero) common-mode gain or, equivalently, common-mode CMRR, and finite input resistance and common-mode resistance. The effect of these, however, on the performance of most of the closed-loop circuits studied here is not very significant, and their study will be postponed to later chapters (in particular Chapters 3 and 5). Note, however, some of these nonideal characteristics will be modeled in Section 2.9 in the context of circuit simulation using SPICE.

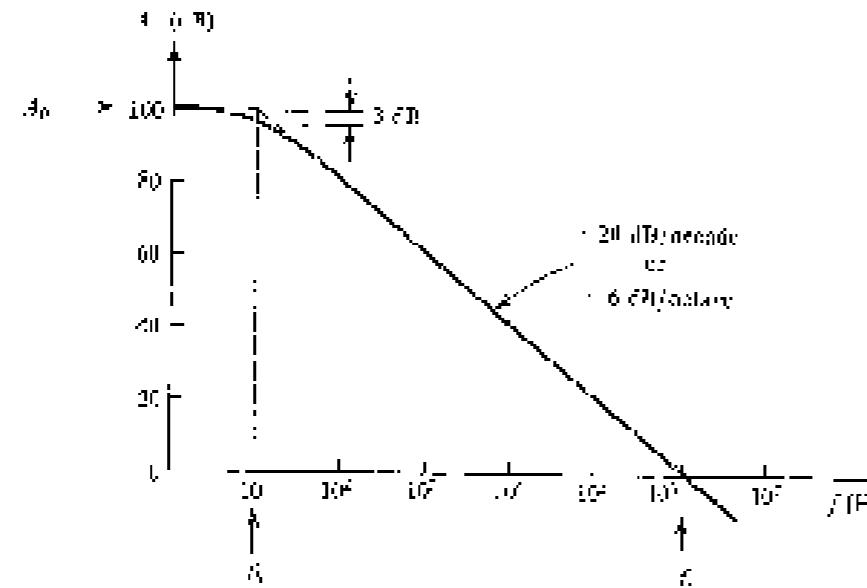


FIGURE 2.22 Open-loop gain for a typical general-purpose internally compensated op-amp.

Note that although the gain is quite high at dc and low frequencies, it starts to fall off at rather low frequency (10 Hz in our example). The uniform -20 dB/decade gain roll-off shown is typical of internally compensated op amps. These are units that have a network (usually a single capacitor) included within the same IC chip whose function is to cause the op-amp gain to have the single-pole roll-off (STC) low-pass response shown. This process of multiplying the open-loop gain is referred to as frequency compensation, and its purpose is to ensure that op-amp circuitry will be stable (as opposed to oscillatory). The subject of stability of op-amp circuits—*i.e.*, more generally, of feedback amplifiers—will be studied in Chapter 8.

By analogy to the response of low-pass Sallen-Key circuits (see Section 1.6 and, for more detail, Appendix D), the gain $A_o(f)$ of an internally compensated op-amp may be expressed as

$$A_o(f) = \frac{A_o}{1 + j\omega/\omega_b} \quad (2.24)$$

where the physical frequency $\omega = j\omega_b \cos \phi_{\omega}$,

$$A_o(f\omega) = \frac{A_o}{1 + j\omega/\omega_b}, \quad (2.25)$$

where ω_b denotes the *break* or *corner* frequency and ϕ_{ω} is the 3-dB frequency (corner frequency). For the example shown in Fig. 2.22, $A_o = 10^6$ and $\omega_b = 2\pi \times 10^4 \text{ rad/s}$. For low frequencies ($\omega \ll \omega_b$) (from 10 Hz to 10 kHz) Eq. (2.25) may be approximated by

$$A_o(f\omega) \approx \frac{A_o \omega_b}{j\omega} \quad (2.26)$$

Thus,

$$A_o(f\omega) \approx \frac{A_o \omega_b}{\omega} \quad (2.27)$$

From which it can be seen that the gain A_o reaches unity (0 dB) at a frequency denoted by ω_b and given by

$$\omega_b = A_o \omega_b \quad (2.28)$$

Substituting in Eq. (2.26) gives

$$A_o(f\omega) \approx \frac{\omega_b}{j\omega} \quad (2.29)$$

The frequency $f_b = \omega_b/2\pi$ is usually specified on the data sheets of commercially available op-amps and is known as the *unity-gain bandwidth*.⁴ Also, note that for $\omega \gg \omega_b$ the open-loop gain in Eq. (2.24) becomes

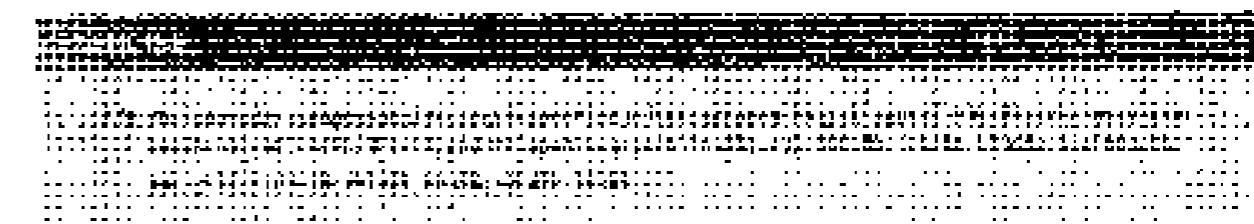
$$A_o(f) \approx \frac{\omega_b}{\omega} \quad (2.30)$$

The gain magnitude can be obtained from Eq. (2.29) as

$$|A_o(f\omega)| = \frac{\omega_b}{\omega} \cdot \frac{1}{j} \frac{1}{\omega} \quad (2.31)$$

Thus if ω_b is known (10^4 Hz in our example), one can easily determine the magnitude of the open-loop gain at a given frequency ω (with courage, observe that this relationship correlates with the Bode plot in Fig. 2.23). Specifically, for $\omega \gg f_b$, doubling ω (an octave increase) results in halving the gain (a 3-dB reduction). Similarly, increasing ω by a factor of 10 (a decade increase) results in reducing $|A_o|$ by a factor of 10 (30 dB).

As a matter of practical importance, we note that the product $\omega_b \phi_{\omega}$ (or the value of ϕ_{ω} between open-loop gain curves of the same type) is usually much smaller than that observed for ω_b and f_b . For this reason f_b is preferred as a specification parameter. Finally, it should be mentioned that an op-amp having this uniform -20-dB/decade (or equivalently -6 dB/octave) gain roll-off is said to have a *single-pole model*. Also, since this single pole dominates the amplifier frequency response, it is called a *dominant pole*. For more on poles (and zeros), the reader may wish to consult Appendix B.



2.5.2 Frequency Response of Closed-Loop Amplifiers

We next consider the effect of limited op-amp gain and bandwidth on the closed-loop transfer functions of the two basic configurations: the inverting circuit of Fig. 2.5 and the noninverting circuit of Fig. 2.12. The closed-loop gain of the inverting amplifier, assuming a finite op-amp open-loop gain A_o , was derived in Section 2.3 and given in Eq. (2.5), which we repeat here as

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A_o} \quad (2.32)$$

⁴Since $\omega_b = \omega_b \phi_{\omega}$, given a gain A_o and the 3-dB bandwidth f_b (where $f_b = \omega_b/2\pi$), it is also known as the *gain-bandwidth product (GB)*. The reader is cautioned, however, that in some amplifiers, the unity-gain frequency and the gain-bandwidth product are *not* equal.

Substituting for A from Eq. (2.24) gives

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{1}{A} + \frac{R_2}{R_1} + \frac{s}{a_1/(1 - R_2/R_1)}} \quad (2.35)$$

For $A_1 \gg 1 - R_2/R_1$, which is usually the case,

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{s}{a_1/(1 - R_2/R_1)}} \quad (2.36)$$

which is of the same form as that for a low-pass SIC network (see Table 1.2, page 51). Thus the inverting amplifier has an STC low-pass response with a dc gain of magnitude equal to R_2/R_1 . The closed-loop gain rolls off at a uniform -20 -dB/decade slope with a corner frequency (3-dB frequency) given by

$$a_1 \text{dB} = \frac{a_1}{1 + R_2/R_1} \quad (2.37)$$

Similarly, analysis of the noninverting amplifier of Fig. 2.12, assuming a finite open-loop gain A , yields the closed-loop transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.38)$$

Substituting for A from Eq. (2.24) and making the approximation $A_1 \gg 1 - R_2/R_1$ results in

$$\frac{V_o(s)}{V_i(s)} = \frac{1 + R_2/R_1}{1 + \frac{s}{a_1/(1 + R_2/R_1)}} \quad (2.39)$$

Thus the noninverting amplifier has an STC low-pass response with a dc gain of $(1 + R_2/R_1)$ and a 3-dB frequency given also by Eq. (2.37).



Consider an op amp with $A = 1\text{M}\mu\text{V}$. Find the 3-dB frequency of closed-loop responses with nominal gains of $+100$, $+10$, $+1$, -10 , -100 , and -1000 . Sketch the absolute frequency response for the amplifiers with closed-loop gains of ± 10 and ± 100 .

Solution

Using Eq. (2.37), we obtain the results given in the following table.

Closed-Loop Gain $= \pm 100$, ± 10 , ± 1 , ∓ 10 , ∓ 100 , ∓ 1000

$a_1 \text{dB}$	$f_{3\text{-dB}}$	$f_{3\text{-dB}}$
+100	990	10 kHz
+10	99	100 kHz
+1	9.9	1 MHz
-1	1	0.3 MHz
-10	0.1	9.9 GHz
-100	0.01	9.9 THz
-1000	0.001	990 Hz

Figure 2.23 shows the frequency response for the amplifier whose nominal dc gain is 0 (20 dB), and Fig. 2.24 shows the frequency response for the -10 (also 20 dB) case. An interesting observation follows from the table above: The unity-gain inverting amplifier has a 3-dB frequency of 0.2 as compared to 1 for the unity-gain noninverting amplifier (frequency for a voltage to current converter).

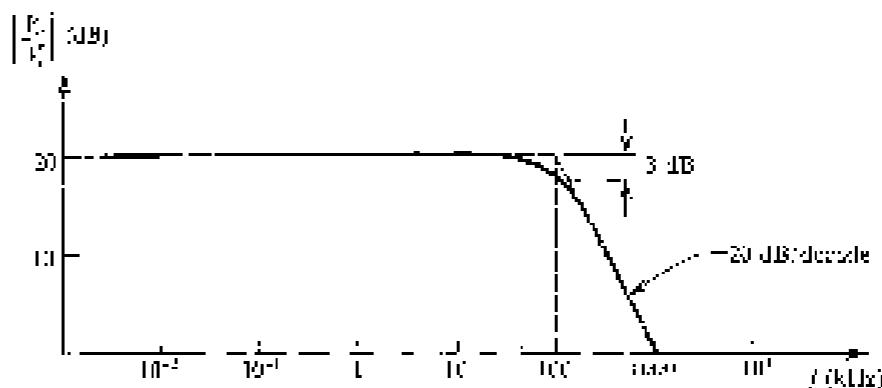


FIGURE 2.23 Frequency response of an inverter with a nominal gain of 4.1×10^3 .

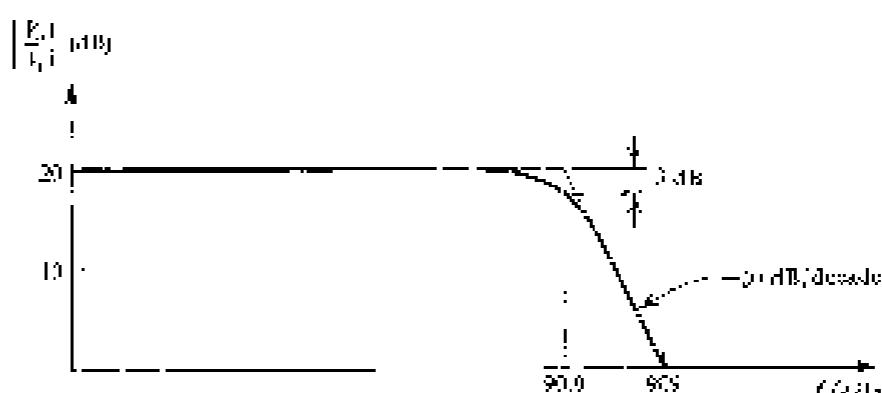


FIGURE 2.24 Frequency response of an inverter with a nominal gain of -10×10^3 .

The table in Example 2.4 above clearly illustrates the trade-off between gain and bandwidth. For a given op-amp, the lower the closed-loop gain required, the wider the bandwidth required. Indeed, the noninverting configuration exhibits a constant gain-bandwidth product equal to $1/A$ of the op-amp. An interpretation of these results in terms of feedback theory will be given in Chapter 8.

EXERCISES

- 1.15 An inverting configuration having a gain of 1000 with a unity-gain frequency of 100 Hz is required. If the available 3-dB frequency is limited to 10 kHz , what is the required closed-loop gain?
- 1.16 An inverting configuration having a gain of 1000 with a unity-gain frequency of 100 Hz is required. If the available closed-loop bandwidth is limited to 10 kHz , what is the required unity-gain frequency?
- 1.17 A unity-gain noninverting configuration having a 3-dB frequency of 100 Hz is required. If the available closed-loop bandwidth is limited to 10 kHz , what is the required unity-gain frequency?
- 1.18 A unity-gain noninverting configuration having a 3-dB frequency of 100 Hz is required. If the available closed-loop bandwidth is limited to 10 kHz , what is the required closed-loop gain?
- 1.19 A unity-gain inverting configuration having a 3-dB frequency of 100 Hz is required. If the available closed-loop bandwidth is limited to 10 kHz , what is the required closed-loop gain?
- 1.20 A unity-gain inverting configuration having a 3-dB frequency of 100 Hz is required. If the available closed-loop bandwidth is limited to 10 kHz , what is the required unity-gain frequency?

A 200-AV/V op-amp has a 316 dB gain-bandwidth product of unity. The closed-loop voltage gain is 100. Find the 3-dB frequency of the closed-loop circuit.

2.6 LARGE-SIGNAL OPERATION OF OP AMPS

In this section, we study the limitations on the performance of op-amp circuits when large output signals are present.

2.6.1 Output Voltage Saturation

Similar to all other amplifiers, op-amps operate linearly over a limited range of output voltages. Specifically, the op-amp output saturates in the manner shown in Fig. 2.12 with V_+ and V_- within 1 V of one of the positive and negative power supplies, respectively. Thus, an op-amp that is operating from ±15-V supplies will saturate when the output voltage reaches about +13 V in the positive direction and -13 V in the negative direction. For this particular op-amp the rated output voltage is said to be ± 3 V. To avoid clipping of the peaks of the output waveform and the resulting waveform distortion, the input signal must be kept correspondingly small.

2.6.2 Output Current Limits

Another limitation on the operation of op-amps is that their output current is limited to a specified maximum. For instance, the popular 741 op-amp is specified to have a maximum output current of ± 20 mA. Thus, in designing closed-loop circuits utilizing the 741, the designer has to ensure that under no condition will the op-amp be required to supply output currents in either direction, exceeding 20 mA. This, of course, includes both the current in the feedback circuit as well as the current supplied to a load resistor. If the circuit requires a larger current, the op-amp output voltage will saturate at the level corresponding to the maximum allowed output current.

Consider the noninverting amplifier circuit shown in Fig. 2.23. As shown, the circuit is designed for a constant gain $(1 + R_2/R_1) = 10$ V/V and is fed with a low-frequency sine-wave signal of peak voltage V_p and is connected to a load resistor R_L . The op-amp is specified to have output saturation voltages of ± 13 V and output current limits of ± 20 mA.

- For $V_p = 1$ V and $R_1 = 1$ k Ω , specify the signal resulting at the output of the amplifier.
- For $V_p = 1.5$ V and $R_1 = 1$ k Ω , specify the signal resulting at the output of the amplifier.
- For $R_1 = 1$ k Ω , what is the maximum value of V_p for which an undistorted sine-wave output is obtained?
- For $V_p = 1$ V, what is the lowest value of R_1 , at which an undistorted sine-wave output is obtained?

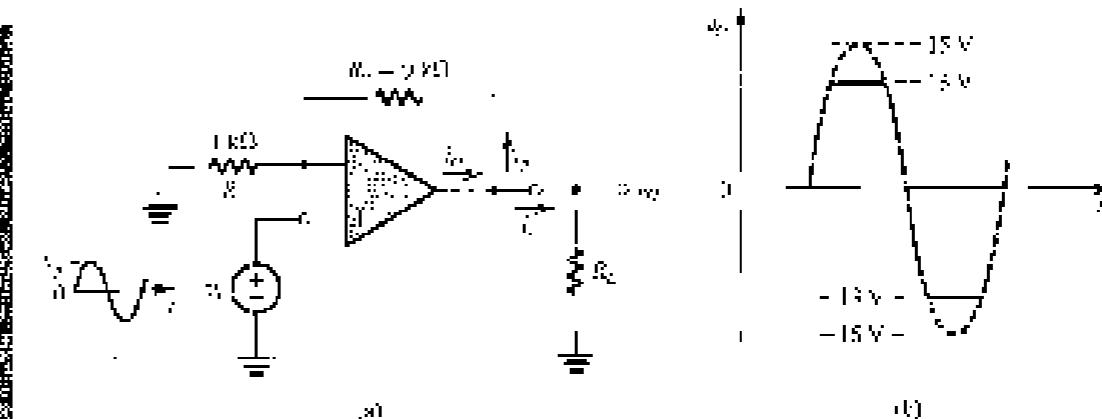


FIGURE 2.25 (a) A noninverting op-amp with a nominal gain of 10 V/V designed to operate in a linear region around 3-V output voltage and 10-mA output current. (b) When the input sine wave has a peak of 10 V, the output is clipped off at ± 13 V.

Solution

(a) For $V_p = 1$ V and $R_1 = 1$ k Ω , the output will be a sine wave with peak value of 10 V. This is lower than output saturation levels of ± 13 V, and thus the amplifier is not limited. (Let's say.) Also, when the output is at its peak (+10 V), the current in the load will be $10\text{ V}/1\text{k}\Omega = 10\text{ mA}$, and the current in the feedback network will be $10\text{ V}/(3 + 1)\text{k}\Omega = 2\text{ mA}$, or total op-amp output current of 12 mA, well under its limit of 20 mA.

(b) Now if V_p is increased to 1.5 V, ideally the output would be a sine wave of 15 V peak. The op-amp, however, will saturate at ± 13 V, thus clipping the sine wave output at those levels. Let's next check on the op-amp output current. At 13-V output and $R_1 = 1$ k Ω , $i_1 = 13\text{ mA}$ and $i_2 = 1.5\text{ mA}$; thus $i_o = 14.5\text{ mA}$, again under the 20-mA limit. Thus the output will be a sine wave with its peaks clipped off at ± 13 V, as shown in Fig. 2.25(b).

(c) For $R_1 = 1$ k Ω the maximum value of V_p for undistorted sine-wave output is 1.5 V. The output will be a 15-V peak-to-peak sine wave, and the op-amp output current at the peaks will be 14.5 mA.

(d) For $V_p = 1$ V and R_1 reduced, the lowest value possible for R_1 while the output is remains undistorted sine wave of 10-V peak can be found from

$$i_{out} = 20\text{ mA} = \frac{13\text{ V}}{R_{out}} = \frac{10\text{ V}}{(9\text{k}\Omega + 1\text{k}\Omega)}$$

which results in

$$R_{out} = 526\text{ }\Omega$$

2.6.3 Slew Rate

Another phenomenon that can cause nonlinear distortion when large output signals are present is that of slew-rate limiting. This refers to the fact that there is a specific maximum rate of change possible at the output of a real op-amp. This maximum is known as the slew rate (SR) of the op-amp and is defined as

$$SR = \frac{dv_o}{dt}_{max} \quad (2.38)$$

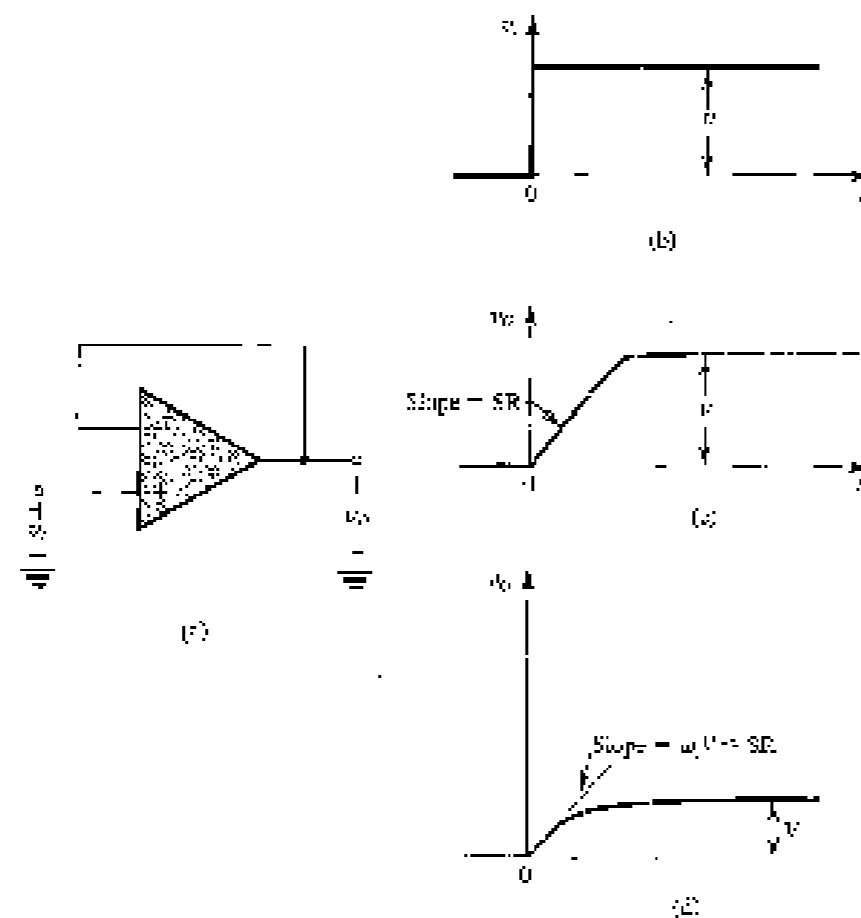


FIGURE 2.26 (a) Input step waveform; (b) Linearly rising output waveform obtained when the op-amp is slow-rate limited; (c) Exponentially rising output waveform obtained when \$V_i\$ is sufficiently small so that its initial slope (\$\omega_i V\$) is close to the required \$SR\$.

and is usually specified on the op-amp data sheet in units of $V/\mu s$. It follows that if the input signal applied to an op-amp circuit is such that it demands an output response that is faster than the specified value of SR, the op-amp will not comply. Rather, its output will change at the maximum possible rate, which is equal to its SR. As an example, consider an op-amp connected in the unity-gain voltage-follower configuration shown in Fig. 2.26(a), and let the input signal be the step voltage shown in Fig. 2.26(a). The output of the op-amp will not be able to rise instantaneously to the ideal value \$V\$; rather, the output will be far longer ramps of slope equal to SR, shown in Fig. 2.26(c). The amplifier is then said to be slow-rate limited.

In order to understand the origin of the slow-rate phenomenon, we need to know about the internal circuit of the op-amp, but we will do so in Chapter 3. For the time being, however, it is sufficient to know about the phenomena just to note that it is distinct from the finite op-amp bandwidth that limits the frequency response of the closed-loop amplifiers studied in the previous section. The limited bandwidth is a linear phenomenon and does not result in a change in the shape of no input sinusoid; that is, it does not lead to nonlinear distortion. The slow-rate limitation, on the other hand, can cause non-linear distortion to an

input sinusoidal signal when its frequency and amplitude are such that the corresponding ideal output would require \$v_o\$ to change at a rate greater than SR. This is the origin of another related op-amp specification, as full-power bandwidth, to be explained later.

Before leaving the example in Fig. 2.26, however, we should point out that if the step input voltage \$V\$ is sufficiently small, the output can be the exponentially rising ramp shown in Fig. 2.26(c). Such an output would be expected from the following. The only limitation on its dynamic performance is the finite gain-bandwidth. Specifically, the transfer-time constant of Eq. (2.14) can be found by substituting \$R_1 = \infty\$ and \$R_2 = 0\$ in Eq. (2.17) to obtain

$$\frac{V_o}{V_i} = \frac{1}{1 + \omega_i R_2}, \quad (2.39)$$

which is a low-pass RC response with a time constant \$1/\omega_i R_2\$. Its step response would have form (see Appendix D)

$$v_o(t) = V(1 - e^{-\omega_i t}), \quad (2.40)$$

The initial slope of this exponentially rising function is \$(\omega_i V)\$. Thus, as long as \$V\$ is sufficiently small, so that \$\omega_i V \leq SR\$, the output will be as in Fig. 2.26(c).

EXERCISE 2.24

- 2.24 An op-amp has a slow-rate limit of \$10^3 V/\mu s\$ and a bandwidth of \$10^3 Hz\$. It is connected in the unity-gain voltage-follower configuration. Find the largest transient input voltage \$V_i\$ for which the output voltage will still be sinusoidal (no distortion). For \$V_i = 10 mV\$, find the time constant of the exponential rise (or fall) of the output voltage if an input voltage \$10 \sin(10^3 t)\$ is applied, and the output voltage is measured \$10 \mu s\$ after the start of the transient.

2.6.4 Full-Power Bandwidth

Op-amp slow-rate limiting can cause nonlinear distortion. In sinusoidal waveforms, consider once more the unity-gain follower with a sine-wave input given by

$$v_i = V_{max} \sin(\omega_i t)$$

The rate of change of this waveform is given by

$$\frac{dv_i}{dt} = \omega_i V_{max} \cos(\omega_i t)$$

with a maximum value of \$\omega_i V\$. This maximum occurs at the zero crossings of the input sinusoid. Now if \$\omega_i V\$ exceeds the slow rate of the op-amp, the output waveform will be distorted in the manner shown in Fig. 2.27. Observe that the output cannot keep up with the large rate of change of the sinusoid at its zero crossings, and the output slew.

The op-amp data sheets usually specify a frequency \$f_0\$ called the full-power bandwidth. It is the frequency \$\omega\$ at which an input sinusoid with amplitude equal to the rated output voltage of the op-amp begins to show distortion due to slow-rate limiting. If we denote the rated output voltage \$V_{max}\$, then \$f_0\$ is related to SR as follows:

$$\omega_0 V_{max} = SR$$

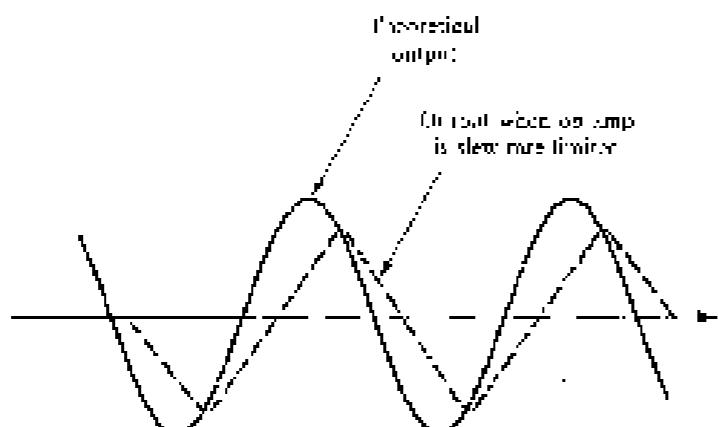


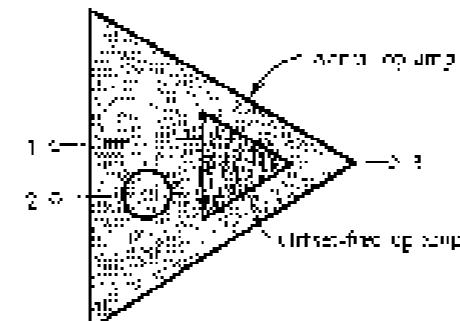
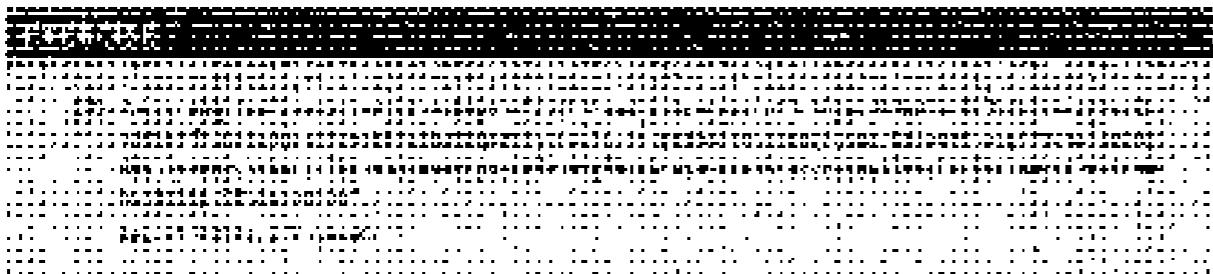
FIGURE 2.27 Effect of slew rate limiting on various sinusoidal waveforms.

Thus,

$$f_s = \frac{SR}{2\pi V_{os}} \quad (2.41)$$

It should be obvious that output amplitudes or frequencies smaller than V_{os} will show slew-rate distortion at frequencies higher than f_s . In fact, at a frequency of higher than f_s , the maximum amplitude of the distorted output sinusoid is given by

$$V_o = V_{os} \sqrt{\frac{\omega_s}{\omega}} \quad (2.42)$$

FIGURE 2.28 Circuit model for an op-amp with input offset voltage V_{os} .

The input offset voltage arises as a result of the unavoidable mismatches present in the input differential stage inside the op-amp. In later chapters we shall study this topic in detail. Here, however, our concern is to investigate the effect of V_{os} on the operation of closed-loop op-amp circuits. Toward that end, we note that general-purpose op-amps exhibit V_{os} in the range of $1-10\text{V}$ in 1mV . Also, the value of V_{os} depends on temperature. The op-amp data sheets usually specify typical and maximum values for V_{os} at room temperature as well as the temperature variation of V_{os} (usually in $\mu\text{V}/^{\circ}\text{C}$). They do not, however, specify the polarity of V_{os} because the component mismatch that gives rise to V_{os} are obviously not known in advance; different units of the same op-amp type may exhibit either a positive or a negative V_{os} .

To analyze the effect of V_{os} on the operation of op-amp circuits, we need a circuit model for the op-amp with input offset voltage. Such a model is shown in Fig. 2.28. It consists of a dc source of voltage V_{os} placed in series with the positive input lead of an offset-free op-amp. The justification for this model follows from the description above.

EXERCISE

- 2.2 Using the model of Fig. 2.28, sketch the transfer characteristic for a unity-gain follower with $V_{os} = 1\text{mV}$ and $V_{os} = 10\text{mV}$. Are these two models equivalent?

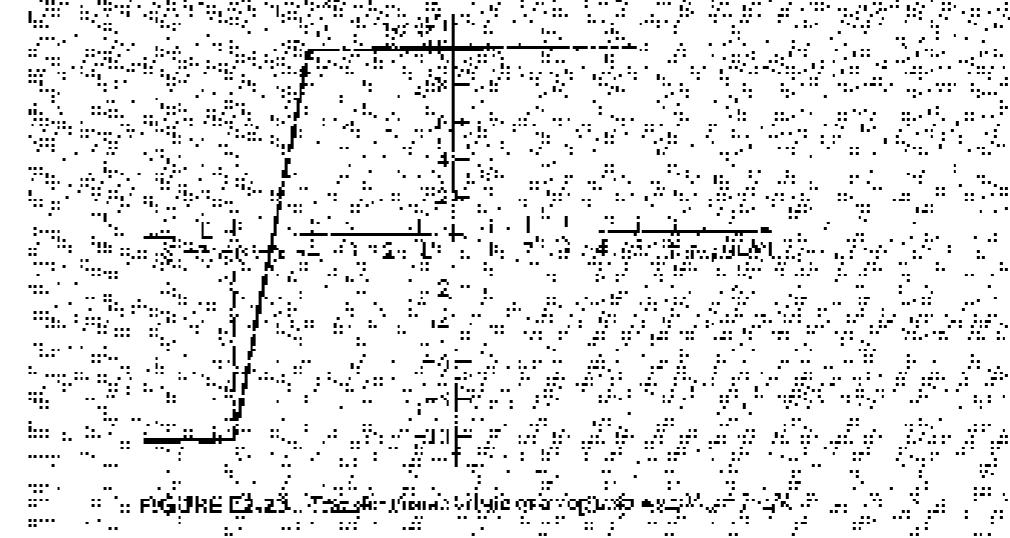


FIGURE 2.29 Transfer characteristic of an op-amp with input offset voltage.

2.7 DC IMPERFECTIONS

2.7.1 Offset Voltage

Because of op-amps are circuit-coupled devices with large gains so do they are prone to go problems. The first such problem is the dc offset voltage. To understand this problem consider the following noninvasive experiment. If the two input terminals of the op-amp are tied together and connected to ground, it will be found that a finite voltage exists at the out put. In fact, if the op-amp has a high dc gain, the output will be of either the positive or negative saturation level. The op-amp output can be brought back to its ideal value of 0 V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op-amp. This external source cancels out the net offset voltage of the op-amp. It follows that the input offset voltage (V_{os}) must be of equal magnitude and of opposite polarity to the voltage we applied externally.

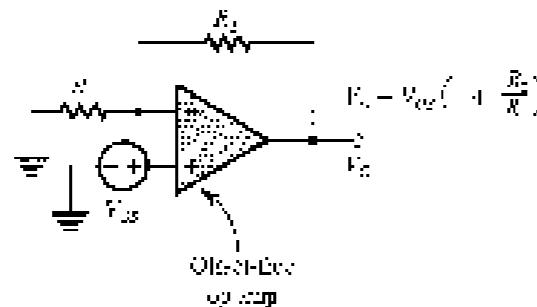


FIGURE 2.29 Evaluating the output dc voltage due to V_{be} in a closed-loop amplifier.

An analysis of op-amp circuits to determine the effect of the op-amp V_{be} on their performance is straightforward. The input voltage signal source is short-circuited and the op-amp is replaced with the model of Fig. 2.28. (Replacing the input signal source to simplify matters, is based on the principle of superposition.) Following this procedure we find that both the inverting and the noninverting-amplifier configurations result in the same circuit that shown in Fig. 2.29, from which the output dc voltage due to V_{be} is found to be

$$V_o = V_{be} \left(1 + \frac{R_2}{R_1} \right) \quad (2.49)$$

This output dc voltage can have a large magnitude. For instance, a noninverting amplifier with a closed-loop gain of 1000, when constructed from an op-amp with a 5-mV input offset voltage, will have a dc output voltage of 15 V < 5 V (depending on the polarity of V_{be}) rather than the dc value of 0 V. Now, when an input signal is applied to the amplifier, the corresponding signal output will be superimposed on the 5-V dc. Obviously then, the allowable signal swing at the output will be reduced. Even worse, if the signal to be amplified is dc, we would not know whether the output is due to V_{be} or to the signal!

Some op-amps are provided with two additional terminals to which a specified circuit can be connected to tried to zero the output dc voltage due to V_{be} . Figure 2.30 shows such an arrangement that is typically used with general-purpose op-amps. A potentiometer is

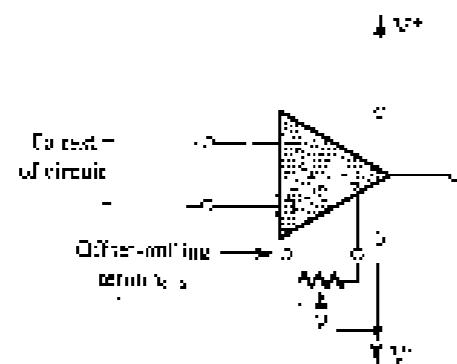


FIGURE 2.30 The output dc offset voltage V_{be} can be determined by connecting a potentiometer to the wiper of the potentiometer and connecting it to the negative supply of the op-amp.

connected between the offset-winding terminals with the wiper of the potentiometer connected to the op-amp negative supply. Moving the potentiometer wiper introduces an imbalance that augments the asymmetry present in the internal op-amp circuitry and that gives rise to V_{be} . We shall return to this point in the context of our study of the internal stability of op-amps in Chapter 9. It should be noted, however, that even though the dc output offset can be trimmed to zero, the problem remains of the variation (or drift) of V_{be} with temperature.

EXERCISE

- 2.26 Consider an inverting amplifier with a closed-loop gain of 1000 operating from a 12-V supply. If the input voltage is 10 mV with mean-square noise levels of 100 nV, what is the approximate dc output offset voltage? Assume the op-amp has a low-frequency open-loop gain of 100000, a unity-gain frequency of 10 Hz, and a corner frequency of 100 Hz. The output voltage is to be limited to ±10 V. Use the model of Fig. 2.28.

One way to overcome the dc offset problem is by capacitively coupling the op-amp. This, however, will be possible only in applications where the closed-loop amplifier is not required to amplify dc or very low frequency signals. Figure 2.31(a) shows a capacitively coupled amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. At a resistive equivalent circuit for determining the dc output voltage resulting from the nonzero input offset voltage V_{be} , will be that shown in Fig. 2.31(b). Thus V_{be} acts in effect as a unity-gain voltage follower, and the dc output voltage V_o will be equal to V_{be} rather than $V_{be}(1 + R_2/R_1)$, which is the case without the coupling capacitor. As long as input signals are concerned, the coupling capacitor C along together with R_1 an STC high-pass circuit with a corner frequency of $\omega_c = 1/\sqrt{CR_1}$. Thus the gain of the capacitive-coupled amplifier will fall off at the low-frequency end. From a magnitude of $(1 + R_2/R_1)$ at high frequencies and will be 3 dB down at ω_c .

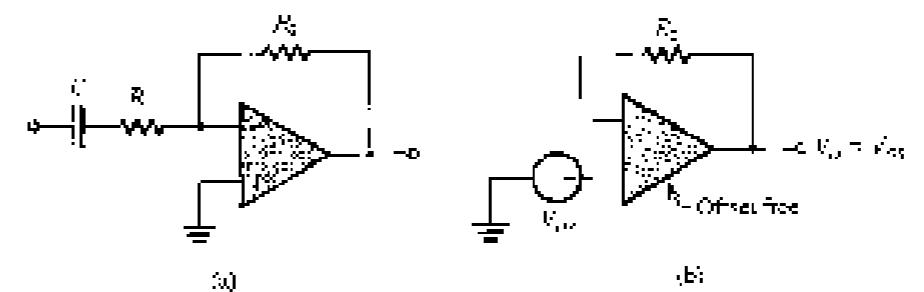


FIGURE 2.31 (a) A capacitive-coupled inverting amplifier, and (b) the equivalent circuit for the dc offset voltage V_{be} .

EXERCISE

- M23 Consider each of the two op-amp configurations shown in Fig. 2.31. In each case, determine the output voltage of the op-amp at different operating levels. Assume that the input bias currents are $I_{B1} = 1 \mu A$ and $I_{B2} = 2 \mu A$. Assume that the output voltage is limited to $V_{O\min} = -10 V$ and $V_{O\max} = +10 V$.
 a) The first configuration is a unity-gain follower. The output voltage is limited to $V_{O\min}$ at the negative input terminal. The output voltage is limited to $V_{O\max}$ at the positive input terminal.
 b) The second configuration is a noninverting amplifier with a gain of 2. The output voltage is limited to $V_{O\min}$ at the negative input terminal. The output voltage is limited to $V_{O\max}$ at the positive input terminal.

2.7.2 Input Bias and Offset Currents

The second dc problem experienced in op-amps is that it is rated in Fig. 2.32. In order for the op-amp to operate, its two input terminals have to be supplied with dc currents. Hence the input bias currents. In Fig. 2.32 these two currents are represented by two current sources, I_{B1} and I_{B2} , connected to the two input terminals. It should be emphasized that the input bias currents are independent of the fact that a real op-amp has finite though large input resistance (see Chapter 2). The op-amp manufacturer usually specifies the average value of I_{B1} and I_{B2} as well as their expected differences. The average value I_B is called the input bias current,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and the difference is called the input offset current and is given by

$$I_{OB} = |I_{B1} - I_{B2}|$$

Typical values for general-purpose op-amps that use bipolar transistors are $I_B = 100 \mu A$ and $I_{OB} = 10 \mu A$. Op-amps that utilize field-effect transistors in the input stage have much smaller input bias current (of the order of picampere).

We now wish to find the dc output voltage of the closed-loop amplifier due to the input bias currents. To do this we ground the signal source and obtain the circuit shown in

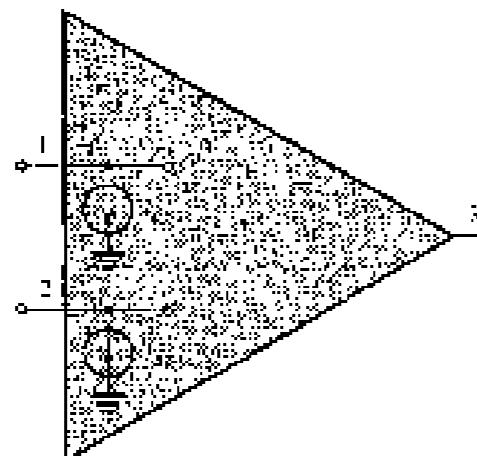


FIGURE 2.32 The op-amp input bias currents, represented by real current sources I_{B1} and I_{B2} .

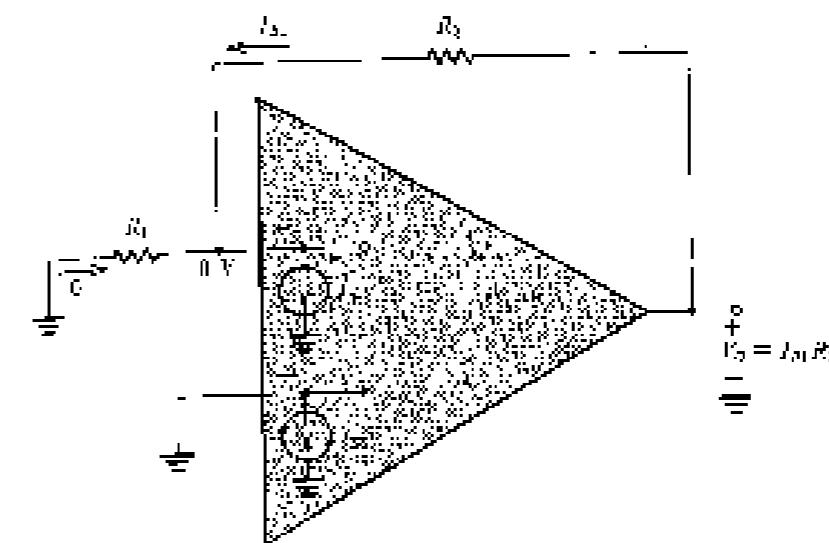


FIGURE 2.33 Analysis of a noninverting amplifier, taking into account the input bias currents.

Fig. 2.33 for both the inverting and noninverting configurations. As shown in Fig. 2.33, the output voltage is given by

$$V_O = I_B R_1 + I_B R_2 \quad (2.34)$$

This obviously places an upper limit on the value of R_2 , fortunately. However, a technique exists for reducing the value of the output dc voltage due to the input bias currents. This method consists of introducing a resistance R_3 in series with the noninverting input lead, as shown in Fig. 2.34. From a signal point of view, R_3 has a negligible effect (ideally no effect).

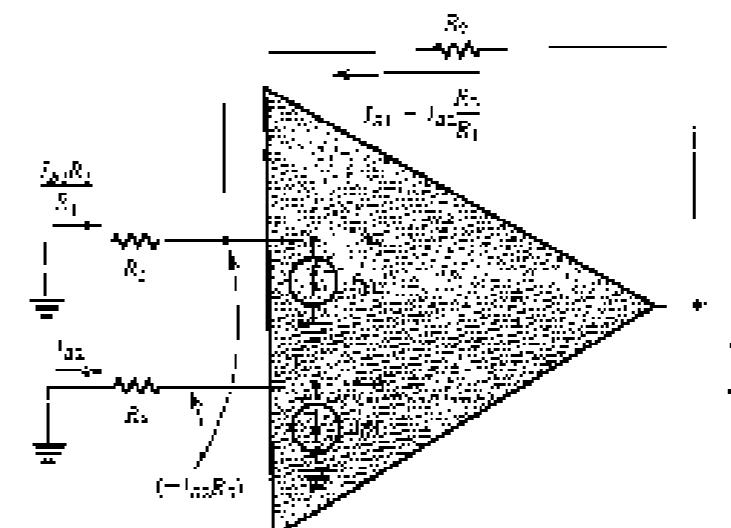


FIGURE 2.34 Reducing the value of the output dc voltage by introducing a resistor R_3 .

The appropriate value for R_3 can be determined by analyzing the circuit in Fig. 2.34, where analysis details are shown, and the output voltage is given by

$$V_o = -I_{\text{A}}R_1 + R_3(I_{\text{D}} - I_{\text{A}})S_1/R_1 \quad (2.45)$$

Consider first the case $I_{\text{D}} = I_{\text{A}} = I_0$, which results in

$$V_o = I_0[R_1 - R_3(1 + R_1/R_2)]$$

Thus we can reduce V_o to zero by selecting R_3 such that

$$R_3 = \frac{R_1}{1 + R_1/R_2} = \frac{R_1R_2}{R_1 + R_2} \quad (2.46)$$

That is, R_3 should be made equal to the parallel equivalent of R_1 and R_2 .

Having selected R_3 as above, let us evaluate the effect of a finite offset current I_{O} . Let $I_{\text{D}} = I_0 + I_{\text{O}}/2$ and $I_{\text{A}} = I_0 - I_{\text{O}}/2$, and substitute in Eq. (2.45). The result is

$$V_o = I_{\text{O}}R_2 \quad (2.47)$$

which is usually about an order of magnitude smaller than the value obtained without R_3 (Eq. 2.44). We conclude that to minimize the effect of the input bias currents one should place in the positive lead a resistance equal to the dc resistance seen by the inverting terminal. We should emphasize the word *dc* in the last statement; note that, if the amplifier is ac coupled, we should reflect $R_3 = R_{\text{D}}$, as shown in Fig. 2.35.

While we are on the subject of ac-coupled amplifiers, we should note that one must always provide a continuous dc path between each of the input terminals of the op-amp and ground. For this reason the ac-coupled noninverting amplifier of Fig. 2.36 will not work without the resistance R_2 to ground. Unfortunately, including R_2 lowers considerably the input resistance of the closed-loop amplifier.

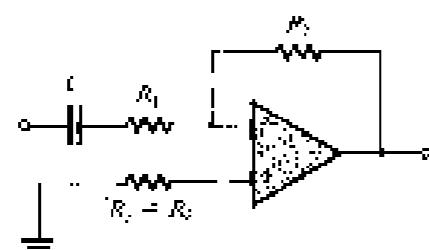


FIGURE 2.35 Invert ac-coupled amplifier circuit. The dc resistance seen by the inverting terminal will be R_3 ; hence R_3 is chosen equal to R_2 .

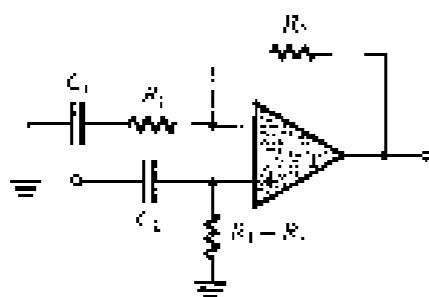


FIGURE 2.36 The need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will not work without resistor R_2 .

EXERCISE

- 2.20 A noninverting op-amp circuit has a negative feedback resistor $R_2 = 10 \text{ k}\Omega$ and $R_1 = 1 \text{ M}\Omega$. If the op-amp has an input bias current of 10 nA and an input offset voltage of 1 mV , find the output dc offset voltage. Neglect the feedback resistor R_2 for purposes of finding the positive input bias current in order to minimize the input offset voltage. What is the new value of V_o ? Ans. 0.1 V ; $9.9982 \times 10^{-10} \text{ A}$; 1 mV

2.8 INTEGRATORS AND DIFFERENTIATORS

In the op-amp circuit applications we have studied thus far, coupled resistors in the op-amp feedback path and in connecting the signal source to the circuit, that is, in the feed-in path. As a result circuit operation has been (ideally) independent of frequency. The only exception has been the use of coupling capacitors in order to minimize the effect of the dc bias currents in op-amps (e.g., the circuits in Figs. 2.31(p) and 2.36). By allowing the use of capacitors together with resistors in the feedback and feed-in paths of op-amp circuits, we open the door to a very wide range of useful and exciting applications of the op-amp. We begin our study of op-amp AC circuits in this section by considering two basic applications, namely signal integrators and differentiators.

2.8.1 The Inverting Configuration with General Impedances

To begin with, consider the inverting closed-loop configuration with impedances $Z_1(s)$ and $Z_2(s)$ replacing resistors R_1 and R_2 , respectively. The resulting circuit is shown in Fig. 2.37 and, for an ideal op-amp, has the closed-loop gain or, more appropriately, the closed-loop transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \quad (2.48)$$

As explained in Section 1.6, replacing s by $j\omega$ provides the transfer function for physical frequencies ω , that is, the transmission magnitude and phase for a sinusoidal input signal of frequency ω .

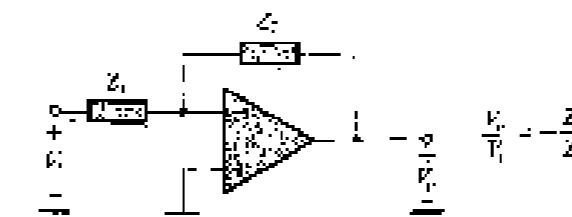


FIGURE 2.37 The inverting configuration with general impedances in the feedback and the feed-in paths.

Example 2.6

For the circuit in Fig. 2.38, derive an expression for the transfer function $V_o(s)/V_i(s)$. Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 34, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 10 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 k Ω . At what frequency does the magnitude of $V_o(s)/V_i(s)$ become unity? What is the phase angle at this frequency?

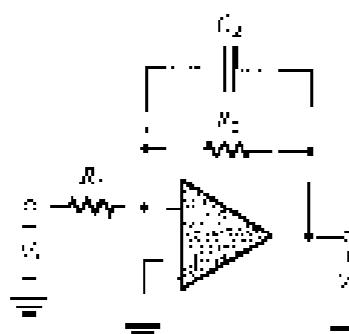


FIGURE 2.38 Circuit for Example 2.6.

Solution

To obtain the transfer function of the circuit in Fig. 2.38, we substitute in Eq. (2.18), $Z_1 = R_1$, and $Z_2 = R_2(1 + sC_2R_1)$. Since Z_2 is the parallel connection of two components, it is more convenient to work in terms of Z_2 . That is, we use the following alternative form of the transfer function:

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{Z_2(s)Z_1(s)}$$

and substitute $Z_1 = R_1$ and $Z_2(s) = 1/R_2 + sC_2R_1$ to obtain

$$\frac{V_o(s)}{V_i(s)} = \frac{s}{s + sC_2R_1}$$

This transfer function, as of Example 1.1, has a finite dc gain, at $s = 0$, $V_o/V_i = -R_2/R_1$, and one zero pole at infinite frequency. That is, it is the transfer function of a low-pass STC network and can be expressed in the standard form of Table 1.2 as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{sC_2R_1}{1 + sC_2R_1}$$

from which we find the dc gain, K , to be

$$K = -\frac{R_2}{R_1}$$

and the 3-dB frequency ω_0 as

$$\omega_0 = \frac{1}{C_2R_1}$$

We could have found all this from the circuit in Fig. 2.38 by inspection. Specifically, note that the inductor behaves as an open circuit at dc (unless the gain is unity $(-R_2/R_1)$). Further note, because there is a virtual ground at the inverting input terminal, the resistance seen by the capacitor is R_2 , and thus the time constant of the STC network is C_2R_2 .

Now to obtain a dc gain of 10 dB, that is, 10k, V/V, we select $R_2/R_1 = 10k$. For an input resistance of 1 k Ω , we select $R_1 = 1k$, and thus $R_2 = 10k$. Finally, for a 3-dB frequency $\omega_0 = 1$ kHz, we select C_2 to be

$$2\pi \times 1 \times 10^3 = \frac{1}{C_2 \times 10k \times 10^3}$$

which yields $C_2 = 1.59 \mu F$.

The circuit has gain and phase Bode plots of the standard form in Fig. 1.23. At the gain falls off at the rate of -20 dB/decade, it will reach 0 dB in one decade, that is, at $\omega = 10\omega_0 = 100$ Hz. As Fig. 1.23(b) indicates, at such a frequency which is much greater than ω_0 , the phase is approximately -90° . To this, however, we must add the 180° arising from the inverting nature of the amplifier (i.e., the negative sign in the transfer function expression). Thus at 100 Hz, the total phase shift will be -270° , or equivalently, 90° .

2.8.2 The Inverting Integrator

By placing a capacitor in the feedback path (i.e., in place of Z_2 in Fig. 2.37) and a resistor at the input (in place of Z_1), we obtain the circuit of Fig. 2.39(a). We shall now show that this circuit realizes the mathematical operation of integration. Let the input be a time-varying function $v_i(t)$. The virtual ground in the inverting op amp (i.e., it causes $v_i(t)$ to appear in effect across R_1) and thus the current $i_1(t)$ will be $v_i(t)/R_1$. This current flows through the capacitor C , causing charge to accumulate on C . If we assume that the circuit begins operation at time $t = 0$, then at an arbitrary time t the current $i_1(t)$ will have deposited on C a charge equal to $(v_i(t)/R_1)t$. Thus the capacitor voltage $v_c(t) = 0$ changes by $v_i(t)/R_1t$. If the initial voltage on C (at $t = 0$) is denoted V_C , then

$$v_c(t) = V_C + \frac{1}{C} \int_0^t i_1(t') dt'$$

Now the output voltage $v_o(t) = -v_c(t)$; thus,

$$v_o(t) = -\frac{1}{C} \int_0^t v_i(t') dt + V_C \quad (2.49)$$

Thus the circuit provides an output voltage that is proportional to the time-integral of the input, with V_C being the initial condition of integrator and CX the integrator time-constant. Note that, as expected, there is a negative sign attached to the output voltage, and thus this integrator circuit is said to be an inverting integrator. It is also known as a Miller integrator after early work in this area.

The operation of the integrator circuit can be described alternatively in the frequency domain by substituting $Z_1(s) = R$ and $Z_2(s) = 1/sC$ in Eq. (2.46) to obtain the transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR} \quad (2.50)$$

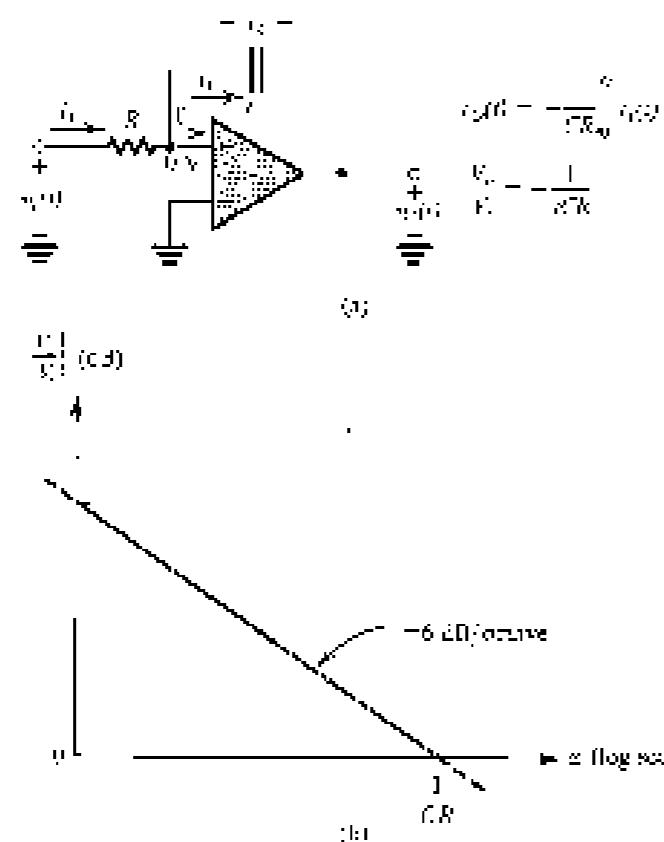


FIGURE 2.39 (a) The Miller compensated integrator. (b) Frequency response of the integrator.

For physical frequencies, $\omega = j\omega_0$ and

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega_0 CR} \quad (2.53)$$

Thus the integrator transfer function has one pole

$$\frac{V_o}{V_i} = \frac{1}{j\omega_0 CR} \quad (2.54)$$

and phase

$$\theta = -90^\circ \quad (2.55)$$

The Bode plot for the integrator magnitude response can be obtained by noting from Eq. (2.52) that as ω goes down 10 times (by an octave) the magnitude is halved (decreased by 6 dB). Thus the Bode plot is a straight line of slope -6 dB/octave (or, equivalently, -20 dB/decade). This line [shown in Fig. 2.39(b)] intercepts the 0-dB line at the frequency (i.e., makes $V_o/V_i = 1$), which from Eq. (2.52) is

$$\omega_0 = \frac{1}{CR} \quad (2.56)$$

The frequency ω_0 is known as the integrator frequency and is simply the inverse of the integrator time constant.

Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner frequency of ω_0 . Observe also that at $\omega = 0$, the magnitude of the integrator transfer function is infinite. This indicates that at $\omega = 0$ the op-amp is operating with an open loop. This should also be obvious from the integrator circuit itself. Reference to Fig. 2.39(a) shows that the feedback element is a capacitor, and thus at $\omega = 0$, where the capacitor behaves as an open circuit, there is no negative feedback! This is a very significant observation and one that indicates a source of problems with the integration circuit. At $\omega = 0$ the input signal, with frequency 0 to produce an infinite output. Of course, no infinite output voltage results in practice; rather, the output of the amplifier saturates at a voltage close to the supply positive or negative power supply (L_1 or L_2) depending on the polarity of the input dc signal.

It should be clear from this discussion that the integrator circuit will suffer deleterious effects from the presence of the op-amp input dc offset voltage and current. To see the effect on the input dc offset voltage V_{D2} , consider the integrator circuit in Fig. 2.40, where for simplicity we have short-circuited the input signal source. Analysis of the circuit is straightforward and is shown in Fig. 2.40. Assuming for simplicity that, at time $t = 0$ the voltage across the capacitor is zero, the output voltage as a function of time is given by

$$v_o = V_{D2} + \frac{V_{D2}}{CR} t \quad (2.57)$$

Thus v_o increases linearly with time until the op-amp saturates—clearly an unacceptable situation! As should be expected, the dc input offset current I_{D2} produces a similar problem. Figure 2.41 illustrates the situation. Observe that we have added a resistance R in the op-amp positive-input lead in order to keep the input bias current I_B from flowing through C .

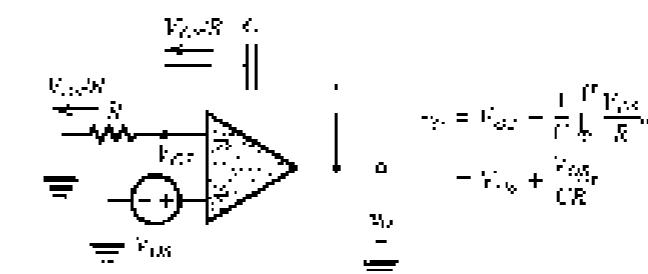
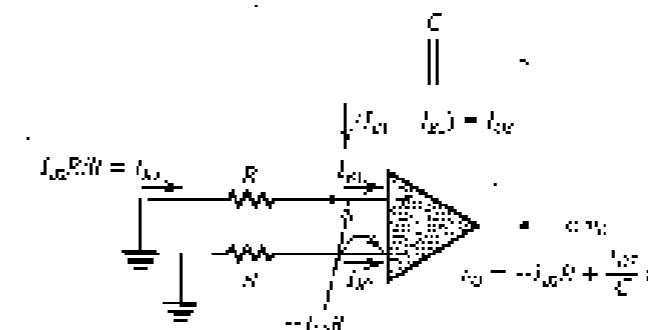
FIGURE 2.40 Miller compensation op-amp integrator circuit with a shorted input signal source. Note that with the output tied with V_{D2} , the output voltage linearly increases.

FIGURE 2.41 Effect of the op-amp input bias and other currents on the performance of the Miller integrator circuit.

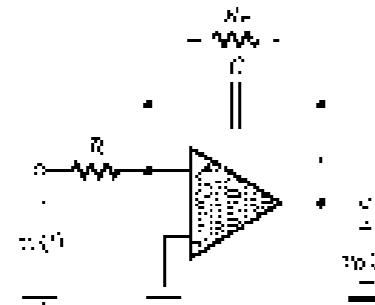


FIGURE 2.42 In Miller integrators, with negative feedback it is possible to provide negative feedback and hence finite gain.

Nevertheless, the offset current, I_{os} , will flow through C and cause v_o to ramp linearly with time until the op-amp saturates.

The dc problem of the integrator can be alleviated by connecting a resistor R_f across the integrator capacitor C , as shown in Fig. 2.43. Such a resistor provides a dc path through which the dc currents (V_{os}/R and I_{os}) can flow, with the result that v_o will now have a dc component $(V_{os}/R + R_f/R) + I_{os}R_f$ instead of rising directly. To keep the dc offset of the output small, one would select a low value for R_f . Unfortunately, however, the lower the value of R_f , the less ideal the integrator circuit becomes. This is because R_f causes the frequency of the integrator pole to move from its ideal location at $\omega = 0$ to one determined by the corner frequency of the SIC framework (R_f, C). Specifically, the integrator transfer function becomes:

$$\frac{V_o(s)}{V_i(s)} = \frac{R_f/R}{1 + sCR_f}$$

as opposed to the ideal function of $-1/sCR$. The lower the value we select for R_f , the higher the corner frequency $1/(CR_f)$ will be and the more nonideal the integrator becomes. Thus selecting a value for R_f presents the designer with a trade-off between dc performance and signal performance. The effect of R_f on integrator performance is investigated further in the Example 2.7. Before doing so, however, observe that R_f creates the negative feedback loop and also provides the integrator output with a finite dc gain of $-R_f/R$.

Example 2.6

Find the output produced by a Miller integrator in response to an input pulse of -1~V height and 1~ms width (Fig. 2.43(a)). Let $R = 10\text{ k}\Omega$ and $C = 10\text{ }\mu\text{F}$. If the integrator capacitor is supplied by a 1-mA resistor, how will the response be modified? (DC op-amp is assumed to saturate at $\pm 13\text{~V}$.)

Solution

In response to a $-1\text{-V}, 1\text{-ms}$ input pulse, the integrator output will be

$$v_o(t) = -\frac{1}{CR} \int_0^t 1 \, dt, \quad 0 \leq t \leq 1\text{ ms}$$

where we have assumed that the initial voltage on the integrator capacitor is 0. For $C = 10\text{ }\mu\text{F}$ and $R = 10\text{ k}\Omega$, $CR = 0.1\text{ ms}$, and

$$v_o(t) = -10t, \quad 0 \leq t \leq 1\text{ ms}$$

which is the linear ramp shown in Fig. 2.43(b). It reaches a magnitude of -10~V at $t = 1\text{~ms}$ and remains constant thereafter.

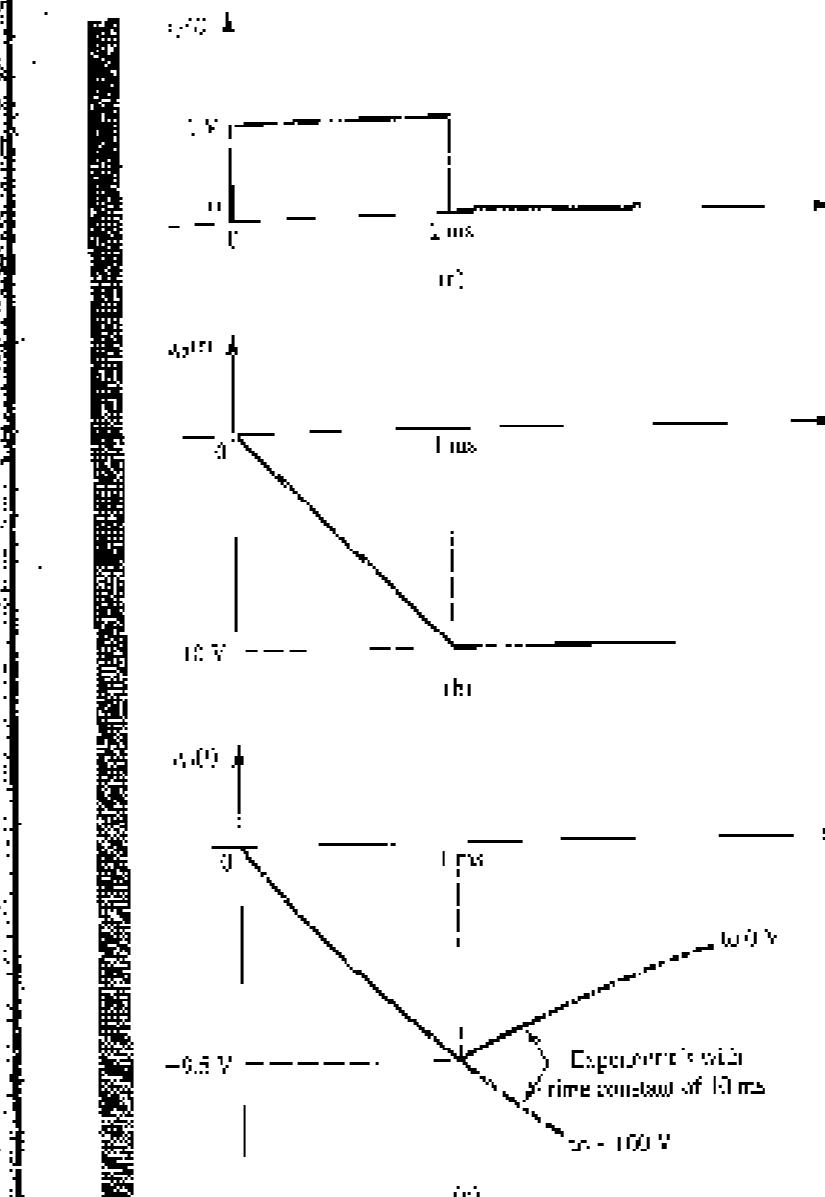


FIGURE 2.43 Waveforms for example 2.6: (a) Input pulse; (b) $0\text{-}1\text{-}0$ response of op-amp integrator; (c) $0\text{-}1\text{-}0$ response of op-amp integrator with resistor R_f connected across integrator capacitor.

That the output is a linear ramp should also be obvious from the fact that the 1-V input pulse produces a $1\text{~V}/(10\text{ k}\Omega \times 0.1\text{ ms})$ constant current through the capacitor. This current, in turn, $I = 0.1\text{ mA}$, supplies the capacitor with a charge i_C , and thus the capacitor voltage changes linearly as $i_C/(10\text{ }\mu\text{F})$, resulting in $v_o = -(1/10)\cdot i_C$. (It is worth remembering that charging a capacitor will always result in zero voltage across it.)

Now, consider the situation with resistor $R_f = 1\text{ M}\Omega$ connected across C . As before, the 1-V pulse will provide a constant current $I = 0.1\text{ mA}$. Now, however, the current is supplied to an

STC network composed of R_F in parallel with C . To find the output voltage, we use Eq. (1.29), which can be adapted to our case here as follows:

$$v_{o(t)} = v_{o(\infty)} + [v_{o(\infty)} - v_o] e^{-t/R_F C}$$

where $v_{o(\infty)}$ is the final value, obtained as

$$v_{o(\infty)} = -V_R = -1.1 \times 10^3 \times 1 \times 10^4 = -110 \text{ V}$$

and $v_{o(0)}$ is the initial value, which is zero. That is, the output will be an exponential decaying toward -110 V with a time constant $\tau = CR_F = 10 \times 10^3 \times 1 \times 10^4 = 10 \text{ ms}$.

$$v_o(t) = -110(1 - e^{-t/10}) \quad 0 \leq t \leq 1 \text{ ms}$$

Of course, the exponential will be truncated at the end of the pulse, that is, at $t = 1 \text{ ms}$, and the output will reach its value

$$v_o(1 \text{ ms}) = -110(1 - e^{-1/10}) = -9.5 \text{ V}$$

The output waveform is shown in Fig. 2.45(c), from which we see the including R_F causes the jump to be slightly rounded such that the output reaches only -9.5 V, 0.5 V short of the ideal value of -11 V. Furthermore, for $t > 1 \text{ ms}$, the capacitor discharges through R_F with the relatively long time-constant of 10 ms. Finally, we note that, up to saturation, specified to occur -15 V , has no effect on the operation of this circuit.

The preceding example gives an important application of integrators, namely, their use in providing rectangular waveforms in response to square-wave inputs. This application is explored in Exercise 2.27. Integrators have many other applications, including their use in the design of filters (Chapter 12).

2.8.3 The Op-Amp Differentiator

Interchanging the location of the capacitor and the resistor of the integrating circuit results in the circuit in Fig. 2.46(a), which performs the mathematical function of differentiation. To see how this comes about, let the input be the time-varying function $v_{i(t)}$, and note that the virtual ground in the inverting input terminal of the op-amp causes $v_{i(t)}$ to appear in effect across the capacitor C . Thus the current through C will be $C(v_{i(t)} - v_o)$, and this current flows through the feedback resistor R providing at the op-amp output a voltage $v_{o(t)}$:

$$v_{o(t)} = -CR \frac{dv_{i(t)}}{dt} \quad (2.56)$$

The frequency-domain transfer function of the differentiator circuit can be found by substituting in Eq. (2.56), $Z_1(s) = 1/sC$, and $Z_2(s) = R$ to obtain

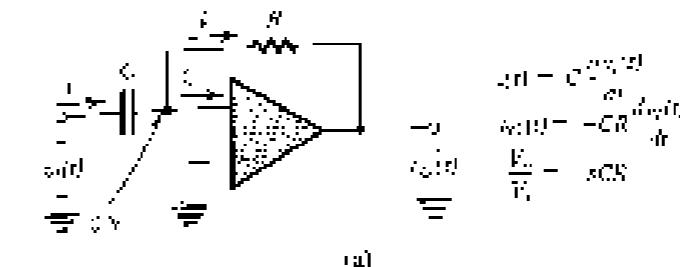
$$\frac{V_o(s)}{V_i(s)} = -sCR \quad (2.57)$$

which for physical frequencies $\omega = j\omega$ yields

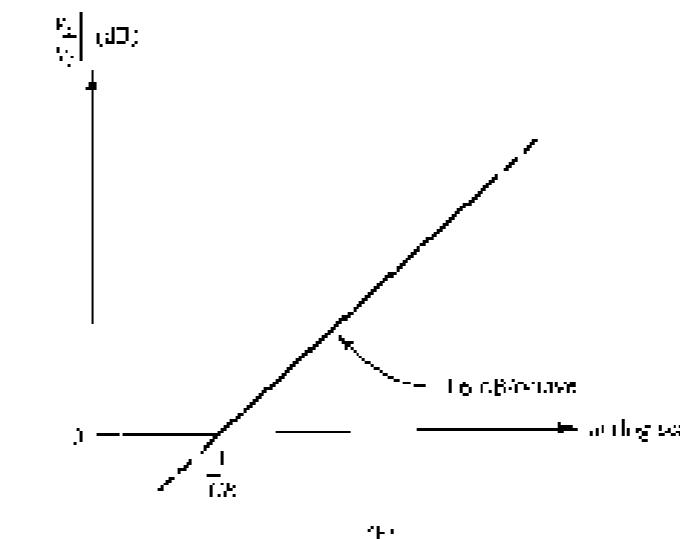
$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR \quad (2.58)$$

Thus the transfer function has magnitude

$$\frac{|V_o|}{|V_i|} = \omega CR \quad (2.59)$$



(a)



(b) Frequency response of a differentiator with a time-constant CR .

one phase

$$\omega = -90^\circ \quad (2.60)$$

The Bode plot of the magnitude response can be found from Eq. (2.59) by noting that the or negative increase in ω the magnitude doubles (increases by 6 dB). Thus the plot is simply a straight line of slope +6 dB/decade (or, equivalently, -20 dB/decade) intersecting the 0-dB line (where $|V_o|/|V_i| = 1$) at $\omega = 1/CR$, where CR is the differentiator time-constant, see Fig. 2.46(b).

The frequency response of the differentiator can be thought of as that of an STC high-pass filter with a corner frequency ω (in rad/s) (refer to Fig. 1.3-1). Finally, we should note that the very nature of a differentiator circuit causes it to be a "noisy differentiator." This is due to the spike in induced in the output every time there is a sharp change in $v_{i(t)}$; such a change could be an antenna-coupled electromagnetically ("picked-up") from adjacent signal sources. For this reason and because they suffer from stability problems (Chapter 8), differentiator circuits are generally avoided in practice. When the circuit of Fig. 2.46(a) is used, it is usually necessary to connect a small-value resistor in series with the capacitor. This modification, unfortunately, turns the circuit into a forced differentiator.

EXERCISES

- 2.27 Consider the unity-gain square-law op-amp model shown in Fig. 2.44. If the input voltage is 10 mV, calculate the output voltage. Assume that the internal circuit is ideal except for the square-law nonlinearity.
- 2.28 Design an op-amp circuit having a unity-gain bandwidth of 10 kHz and a gain of 100. What is the slew rate? Which op-amp model is appropriate?
- 2.29 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.30 Consider a Miller compensation with a load capacitor $C_L = 100 \text{ pF}$. The input voltage is 10 mV and the feedback voltage is -10 V . Assuming a load value of 10 M Ω , calculate the output voltage. Use the op-amp model given in Fig. 2.44 for the op-amp and assume that the open-loop gain is 1000. What is the critical frequency of the circuit? (See Fig. 2.10.)
- 2.31 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.32 Design an op-amp circuit with a unity-gain bandwidth of 100 Hz and a gain of 100. What is the slew rate? Which op-amp model is appropriate?
- 2.33 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.34 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.35 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.36 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.37 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.38 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.39 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.40 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.41 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.42 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.43 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.44 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.45 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.46 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.47 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.48 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.49 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.50 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.51 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.52 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
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- 2.58 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.59 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.60 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.61 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.62 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.63 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
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- 2.67 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.68 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.69 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.70 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.71 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.72 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.73 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.74 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.75 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.76 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.77 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.78 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.79 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.80 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.81 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.82 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.83 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.84 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.85 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.86 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.87 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.88 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.89 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.90 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.91 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.92 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.93 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.94 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.95 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.96 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.97 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.98 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.99 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?
- 2.100 (Op-amp C = 0) If $V_{in} = 100 \text{ mV}$, what is the output voltage?

2.9 THE SPICE OP-AMP MODEL AND SIMULATION EXAMPLES

As mentioned at the beginning of this chapter, the op-amp is not a single electronic device, such as the junction diode or the MOS transistor, both of which we shall study later on. Rather, it is a complex IC made up of a large number of discrete devices. Nevertheless, as we have seen in this chapter, the op-amp can be treated and indeed effectively used as a circuit component or a circuit building block without the user needing to know the details of its internal circuitry. The user, however, needs to know the electrical characteristics of the op-amps, such as its open-loop gain, its input resistance, its frequency crossover, etc. Furthermore, in designing circuits utilizing the op-amp, it is useful to be able to represent the op-amp with an equivalent circuit model. Indeed, we have already done this in this chapter, albeit with very simple equivalent circuit models suitable for hand analysis. Since we are now going to use computer simulation, the models we can be more complex to account as fully as possible for the op-amp's nonlinear performance.

Op-amp models that are based on their observed terminal characteristics are known as macromodels. These are to be distinguished from models that are obtained by modeling every device in the op-amp's actual internal circuit. The latter type of model can become very complex and unwieldy, especially if one attempts to use it in the simulation of a circuit that utilizes a large number of op-amps.

The goal of macromodeling of a circuit block (in our case here, the op-amp) is to achieve a very close approximation to the actual performance of the op-amp while using circuit model of significantly reduced complexity compared to the actual internal circuit. Advantages of

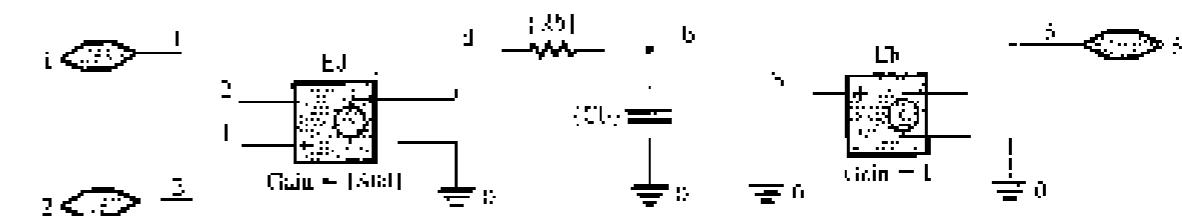


FIGURE 2.45 A SPICE macromodel for a model of the f_T of a unity-gain bandwidth of an op-amp.

using a macromodel include: A macromodel can be developed on the basis of data-sheet specification, without having to know the details of the internal circuitry of the op-amp. Moreover, macromodels allow the simulation of a circuit containing a number of op-amps to be performed much faster.

2.9.1 Linear Macromodel

The Capture schematic⁶ of a linear macromodel for an internally compensated op-amp with finite gain and bandwidth is shown in Fig. 2.46. In this equivalent circuit model, the gain constant A_{in} of the voltage-controlled voltage source V_1 corresponds to the differential gain of the op-amp model. Resistor R_1 and capacitor C_1 form an RLC filter with corner frequency

$$f_c = \frac{1}{2\pi R_1 C_1} \quad (2.61)$$

The low-pass response of the filter is used to model the frequency response of the internally compensated op-amp. The values of R_1 and C_1 used in the macromodel are chosen such that f_c corresponds to the 3-dB frequency of the op-amp being modeled. This is done by arbitrarily selecting a value for either R_1 or C_1 ; the selected value does not need to be a practical one and then using eq. (2.61) to compute the other value. In Fig. 2.46, the voltage-controlled voltage source V_1 with a gain constant of unity is used as a buffer to isolate the low-pass filter from the load of the op-amp output. Thus any even-order loading will not affect the frequency response of the filter and hence that of the op-amp.

The linear macromodel in Fig. 2.46 can be further expanded to account for other op-amp nonlinearities. For example, the emitter-coupled model in Fig. 2.60 can be used to model an internally compensated op-amp while accounting for the following op-amp nonlinearities:

1. Input Offset Voltage (V_{IO}): The dc voltage source V_{IO} models the op-amp input offset voltage.
2. Input Bias Current (I_{IB}) and Input Offset Current (I_{IO}): The dc current sources I_{IB} and I_{IO} model the input bias current at each input terminal of the op-amp, with

$$I_{IB} = I_B + \frac{I_{IO}}{2} \quad \text{and} \quad I_{IO} = I_B - \frac{I_{IO}}{2}$$

where I_B and I_{IO} are, respectively, the input bias current and the input offset current specified by the op-amp manufacturer.

⁶The reader is reminded that the Capture schematic is the component in SPICE simulation. All SPICE examples in this book can be found in the part 2.11 as well as on its website: www.electronics-tutorials.ws.

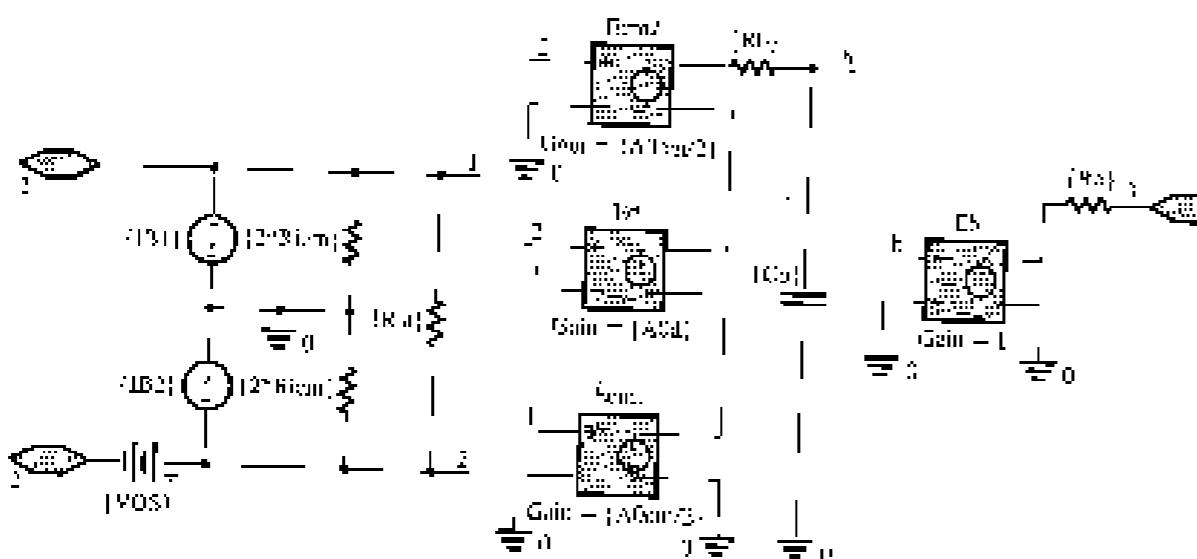


FIGURE 2.46 A comprehensive block-diagram model of an internally compensated op-amp.

3. Common-Mode Input Resistance (R_{inC}). If the two input terminals of an op-amp are tied together and its input resistance is measured, the result is the common-mode input resistance R_{inC} . In the block model of Fig. 2.46, we have split R_{inC} into two equal parts ($2R_{inC}$), each connected between one of the input terminals and ground.
4. Differential-Input Resistance (R_{inD}). The resistance seen between the two input terminals of an op-amp is the differential input resistance R_{inD} .
5. Differential Gain at DC (A_{vd}) and Common-Mode Rejection Ratio (CMRR). The output voltage of an op-amp at dc can be expressed as

$$V_o = A_{vd}(V_2 - V_1) + \frac{A_{vd}}{2}(V_1 - V_2)$$

where A_{vd} and A_{inC} are, respectively, the differential and common-mode gains of the op-amp at dc. For an op-amp with finite CMRR,

$$A_{vd} = A_{inC}/\text{CMRR} \quad (2.62)$$

where CMRR is expressed in dB (not in dB). Note that the CMRR value in Eq. (2.62) is that of the open-loop op-amp while the CMRR in Eq. (2.14) is that of a particular closed-loop op-amp. In the block model of Fig. 2.46, the voltage-controlled voltage sources E_{v1} and E_{v2} with gain constants of $A_{vd}/2$ account for the finite CMRR while source E_{in} models A_{inC} .

6. Unity-Gain Frequency (f_u). From Eq. (2.23), the 3-dB frequency f_u and the unity-gain frequency (or gain bandwidth product) f_T of an internally compensated op-amp with an STC frequency response are related through

$$f_u = \frac{f_T}{A_{vd}} \quad (2.63)$$

As in Fig. 2.45, the finite op-amp bandwidth is accounted for in the model of Fig. 2.46 by setting the corner frequency of the filter formed by resistor R_C and

capacitor C_1 (Eq. 2.61) to equal the 3-dB frequency of the op-amp (Eq. 2.62). It should be noted that here we are assuming that the differential gain and the common mode gain have the same frequency response (not always a valid assumption).

7. Output Resistance (R_o). The resistance seen in the output terminal of an op-amp is the output resistance R_o .

Performance of a Noninverting Amplifier

Consider an op-amp with a differential input resistance of $2 \text{ M}\Omega$, a common-mode input voltage of 12 mV , a dc gain of 1000 , and an output resistance of $70 \text{ }\Omega$. Assume the op-amp is internally compensated and has an STC frequency response with a gain bandwidth product of 1 MHz .

- (a) Create a schematic model for this op-amp in PSpice.

(b) Using the schematic, simulate the closed-loop noninverting amplifier in Fig. 2.12 with resistors $R_1 = 1 \text{ k}\Omega$ and $R_2 = 100 \text{ k}\Omega$ to find

- (i) its 3-dB bandwidth, f_u ,
- (ii) its output offset voltage, V_{os} ,
- (iii) its input resistance, R_{in} ,
- (iv) its output resistance, R_o ,
- (v) its open-loop response of the closed-loop amplifier, and measure its rise time, t_r . Verify that this time agrees with the 3-dB frequency determined above.

Solution

To model the op-amp in PSpice, we use the equivalent circuit in Fig. 2.46 but with $R_{in} = 2 \text{ M}\Omega$, $R_{inC} = 2 \text{ M}\Omega$ (open circuit), $V_{os} = 0$ (open circuit), $V_{th} = 12 \text{ mV}$, $A_{vd} = 10^6 \text{ V/V}$, $A_{inC} = 0$ (short-circuited), and $R_o = 70 \text{ }\Omega$. Furthermore, we set $C_1 = 1 \text{ }\mu\text{F}$ and $R_C = 15.915 \text{ k}\Omega$ to achieve a $f_u = 1 \text{ MHz}$.

To measure the 3-dB frequency of the closed-loop amplifier, we apply a 1-V ac voltage at its input, perform an ac analysis simulation in PSpice, and plot its output versus frequency. The output voltage, plotted in Fig. 2.47, corresponds to the gain of the amplifier because we chose an input voltage of 1 V. Thus, from Fig. 2.47, the closed-loop amplifier has a dc gain of $A_{vd} = 1000$ (V/V), and the frequency at which its gain drops by $\sqrt{2} = 70.7 \text{ V/V}$ is $f_u = 90 \text{ kHz}$, which agrees with Eq. (2.28).

The input resistance R_{in} corresponds to the resistance to the current drawn out of the 1-V ac voltage source used in the above ac-analysis simulation at 0.1 Hz. Theoretically, R_{in} is the actual signal input resistance at dc. However, ac analysis simulations must start at frequencies greater than zero, so we use 0.1 Hz to approximate the dc point. Accordingly, R_{in} is found to be $2 \text{ G}\Omega$.

To measure R_o , we short-circuit the amplifier input to ground, inject a 1-A ac current in the PSpice, and perform an ac-analysis simulation. R_o corresponds to the amplifier output voltage at 1-A dc, and is found to be $70 \text{ m}\Omega$. Although an ac voltage source could easily well have been used to measure the output resistance in this case, it is more precise to attach a current source rather than a voltage source between the output and ground. This is because an ac voltage source appears as an open circuit when the simulator computes the dc bias point of the circuit while an ac voltage source appears as a short circuit which can erroneously force the dc output voltage to zero. For similar reasons, an ac voltage source should be attached in series with the biasing dc voltage source for measuring the input resistance of an op-amp.

A quick look at R_{in} and R_o of the closed-loop amplifier reveals that their values have, respectively, increased and decreased by a factor of about 1000 relative to the corresponding

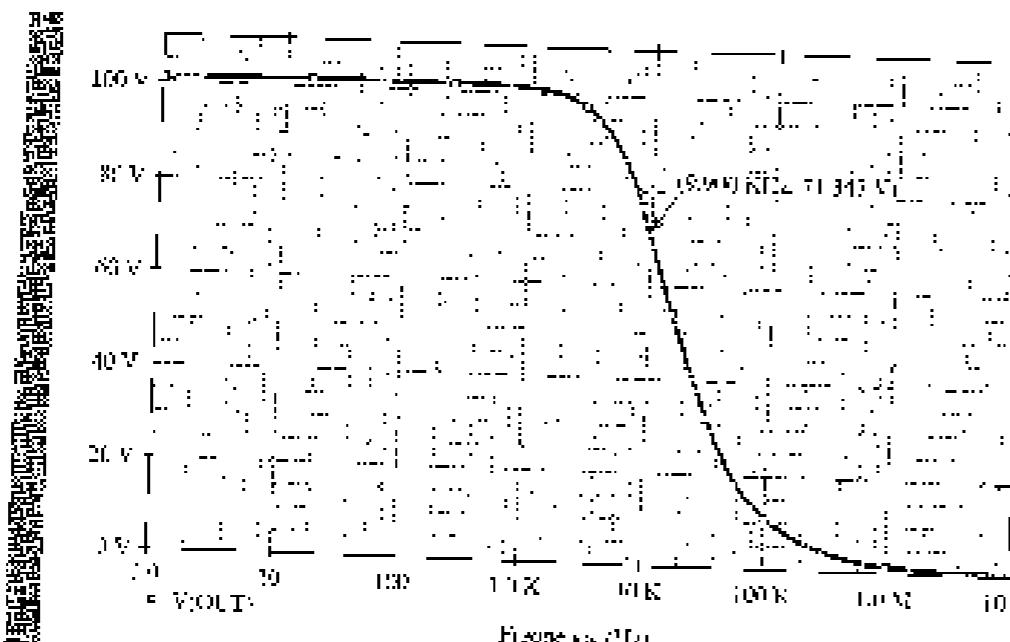


FIGURE 2.47 Frequency response of the closed-loop amplifier in Example 2.8.

resistance of the op-amp. Such a large input resistance and small output resistance are indeed desirable characteristics for a voltage amplifier. This improvement in the small-signal resistance of the closed-loop amplifier is a direct consequence of applying negative feedback (through resistors R_1 and R_2) around the open-loop op-amp. We will study negative feedback in Chapter 8, where we will also learn how the input-output gain (10000), this-way corresponds to the ratio of the open-loop non-invert gain (10^5) to the closed-loop amplifier gain (100).

From Figs. 2.37 and 2.38, the closed-loop amplifier has an SIC low-pass response given by

$$\frac{V_o(t)}{V_{in}(t)} = \frac{G_0}{1 + \frac{t}{2\pi f_{c0}}}$$

As described in Appendix D, the response of such an amplifier to an input step of height V_{in0} is given by

$$v_o(t) = V_{in0} (1 - e^{-t/\tau}) \quad (2.64)$$

where $V_{in0} = G_0 V_{out}$ is the final output voltage value (V_{out} is the voltage value toward which the output is heading) and $\tau = 1/(2\pi f_c)$ is the time constant of the amplifier. If we define $t_{0.9}$ and $t_{0.95}$ to be the time instances for the output waveform to rise to, respectively, 90% and 95% of V_{in0} , then from Eq. (2.64) $t_{0.9} = 0.1\tau$ and $t_{0.95} = 0.2\tau$. Therefore, the settling time of the amplifier

$$t_s = t_{0.95} - t_{0.9} = 0.2\tau = \frac{2.2}{2\pi f_{c0}}$$

Therefore, if $f_{c0} = 90$ Hz, then $t_s = 35.4 \mu s$. To simulate the step response of the closed-loop amplifier, we apply a step voltage of 10 mV, use a piecewise-linear (PWL) model (see Figure 2.48) for the op-amp, and perform a transient-analysis simulation, and measure the voltage at the output versus time. In our example, for an input voltage of 1 mV, we applied a 1-V step input, plotted the output waveform in Fig. 2.48, and measured t_s to be 37.4 μs .

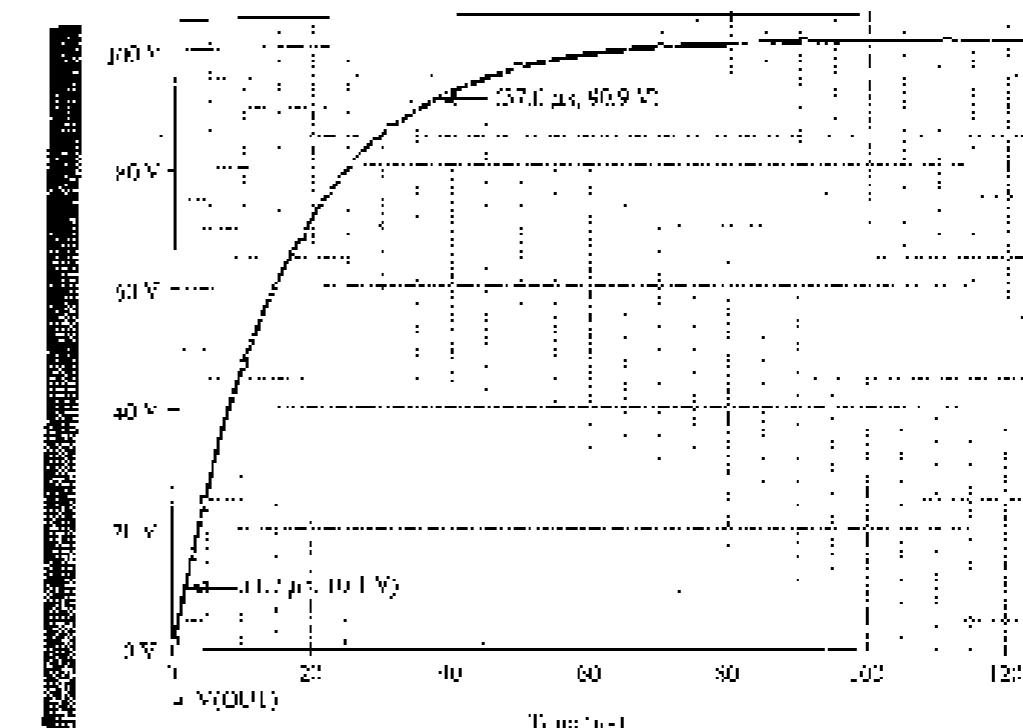


FIGURE 2.48 Step response of the closed-loop amplifier in Example 2.8.

The linear macromodels in Figs. 2.45 and 2.46 assume that the op-amp circuit is operating in its linear stage, and do not account for its nonlinear performance when large signals are present at the output. Therefore, nonlinear effects, such as output saturation and slew rate, are not modeled. This is why, in the step response of Fig. 2.48, we could see an output voltage of 100 V when we applied 1-V step input. However, CMOSamps are not capable of producing such large output voltages. Hence, a designer must be very careful when using these models.

It is important to point out that we also saw output voltages of 100 V or so in the ac analysis of Fig. 2.47, where for convenience we applied a 1-V ac input to measure the gain of the closed-loop amplifier. So, would we see such large output voltages if the op-amp macromodel accounted for nonlinear effects (particularly, output saturation)? The answer is yes, because in an ac analysis PSpice uses a linear model for nonlinear devices with the linear-model parameters evaluated at a bias point. We will have more to say about this in subsequent chapters. Here, however, we must keep in mind that the voltage magnitudes encountered in an ac analysis may not be realistic. What is of importance to the designer in this case are the voltage and current ratios (e.g., the output-to-input voltage ratio as a measure of voltage gain).

2.8.2 Nonlinear Macromodel

The linear macromodel in Fig. 2.46 can be further expanded to account for the op-amp non-linear performance. For example, the finite output voltage swing of the op-amp can be modeled by placing limits on the output voltage of the voltage-controlled voltage source G_0 . In PSpice this can be done using the FTABLINE component in the analog-behavioral-modelling (ABM) library and setting the output voltage limits in the look-up table of this component. Further details on how to build nonlinear macromodels for the op-amp can be found in the references on Spice simulation. In general, robust macromodels that account for the nonlinear effects in an IC are provided by the op-amp manufacturers. Most packages include such

manufacturers' for some of the popular op-amps and ICs in their libraries. For example, PSpice includes models for the *μA741*, the *LV111*, and the *LM324* op-amps.¹¹

Characteristics of the 741 Op-Amp

Consider the *μA741* op-amp whose model is available in PSpice. Use PSpice to plot the open-loop gain and hence determine A . Also, investigate the SR limit and the output saturation of this op-amp.

Solution

Figure 2.49 shows the Capture schematic used to simulate the frequency response of the *μA741* op-amp. The *μA741* part has seven terminals. Terminals 7 and 1 are, respectively, the positive and negative dc power-supply terminals of the op-amp. 741-type op-amps are typically operated from ±15-V power supplies; therefore we connected the dc voltage sources $V_{CC} = +15\text{ V}$ and $V_{EE} = -15\text{ V}$ to terminals 7 and 4, respectively. Terminals 2 and 3 of the *μA741* part correspond to the positive and negative input terminals, respectively, of the op-amp. In general, as outlined in Section 2.1.3, the op-amp input signals are expressed as

$$v_{in+} = V_{in+} + \frac{v_1}{2}$$

$$v_{in-} = V_{in-} - \frac{v_1}{2}$$

where v_{in+} and v_{in-} are the signals at, respectively, the positive- and negative-input terminals of the op-amp with V_{in} being the common-mode input signal (which sets the dc bias voltage at the op-amp input terminals) and v_1 being the differential input signal to be amplified. The dc voltage source V_{CM} in Fig. 2.49 is used to set the common-mode input voltage. Typically, V_{CM} is set to the average of the dc power-supply voltages V_{CC} and V_{EE} to maximize the available input signal swing. Hence, we set $V_{CM} = 0$. The voltage source V_1 in Fig. 2.49 is used to generate the differential input signal v_1 . This signal is applied differentially to the op-amp input terminals using the voltage-controlled voltage sources R_1 and R_2 whose gain constants are set to 0.5.

Terminals 5 and 6 of part *μA741* are the offset-nulling terminals of the op-amp (as depicted in Fig. 2.36). However, a check of the PSpice netlist of this part (by selecting Edit → PSpice Model), in the Capture menu, reveals that these terminals are floating; therefore the offset-nulling characteristic of the op-amp is not incorporated in the model.

To measure A of the op-amp, we set the voltage of source V_1 to be 1-V ac, perform an ac analysis simulation in PSpice, and plot the output voltage versus frequency as shown in Fig. 2.50. Accordingly, the frequency at which the op-amp voltage gain drops to 0 dB is $f_c = 0.9\text{ MHz}$ (which is close to the 1-MHz value reported in the data sheets for 741-type op-amps).

To determine the slew rate of the *μA741* op-amp, we connect the op-amp in a unity-gain configuration, as shown in Fig. 2.51, apply a large pulse signal at the input with very short rise and fall times to cause slew-rate limiting at the output, perform a transient-analysis simulation in PSpice, and plot the output voltage as shown in Fig. 2.52. The slope of the slew-rate limited output waveform corresponds to the slew-rate of the op-amp and is found to be $SR = 0.5\text{ V/μs}$ (which agrees with the value specified in the data sheets for 741-type op-amps).

¹¹ The OKAD 9.2 Live Edition of PSpice, which is available on the CD accompanying this book, includes these models in its evaluation (EVAL) library.

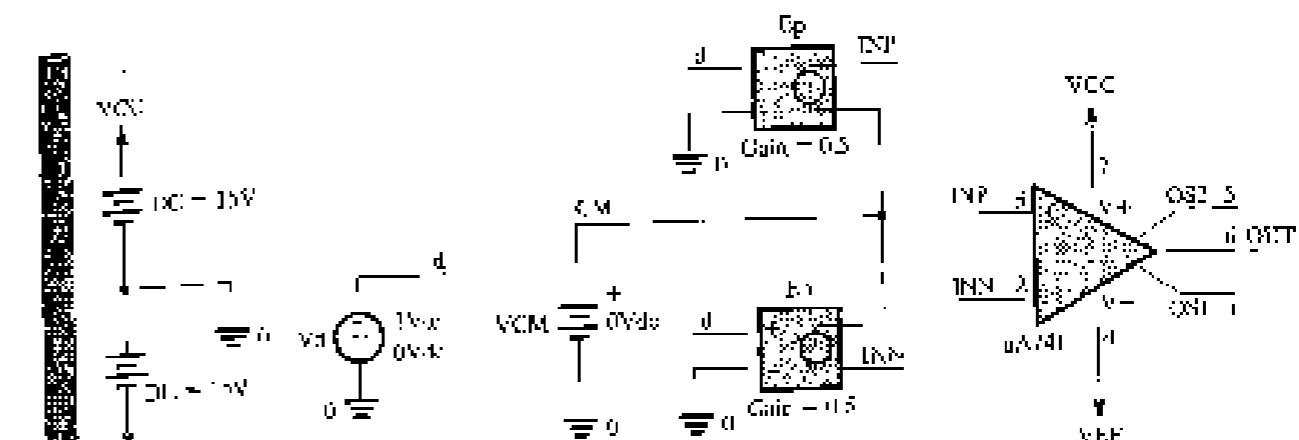


FIGURE 2.49 Simulating the frequency response of the *μA741* op-amp in Example 2.9.

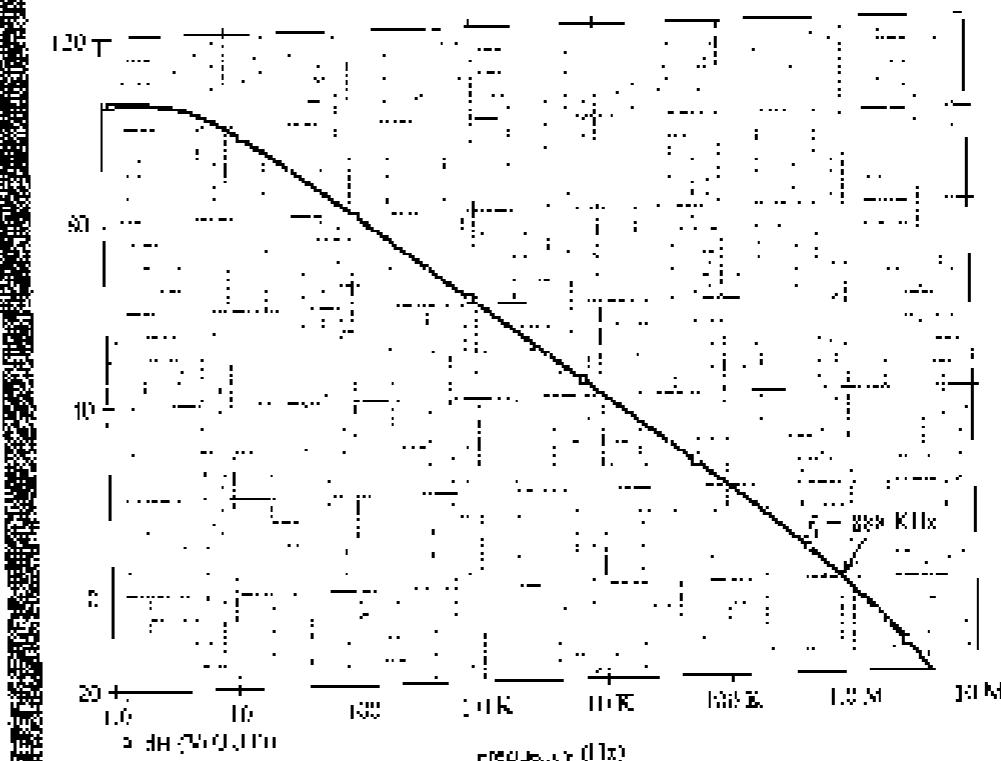


FIGURE 2.50 Frequency response of the *μA741* op-amp in Example 2.9.

To determine the maximum output voltage of the *μA741* op-amp, we set the dc voltage of the differential voltage source V_1 in Fig. 2.49 to a large value, say -1 V , and perform a bias-point simulation in PSpice. The corresponding dc output voltage is the positive output saturation voltage. We repeat the simulation with the dc differential input voltage set to $+1\text{ V}$ to find the negative output saturation voltage. Accordingly, we find that the *μA741* op-amp has a maximum output voltage $V_{OM} = +14.3\text{ V}$.

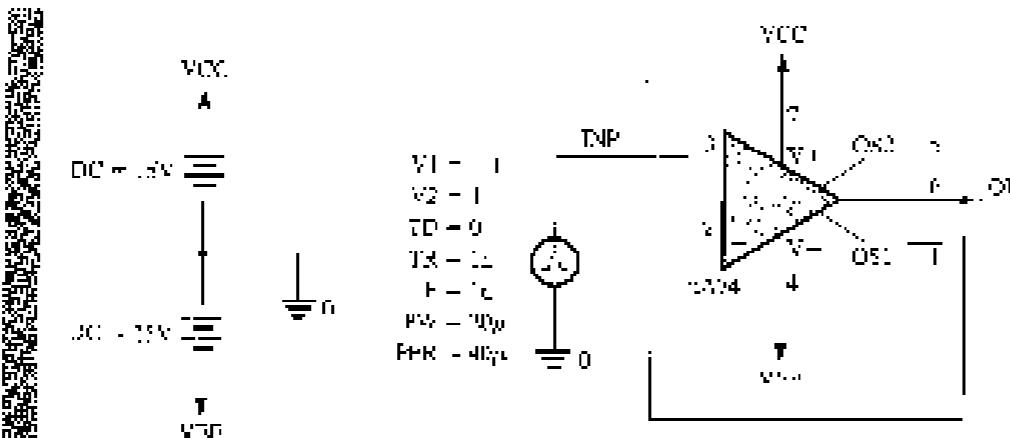


FIGURE 2.51 Circuit for determining the slew rate of the PA241 op-amp in Example 2.9.

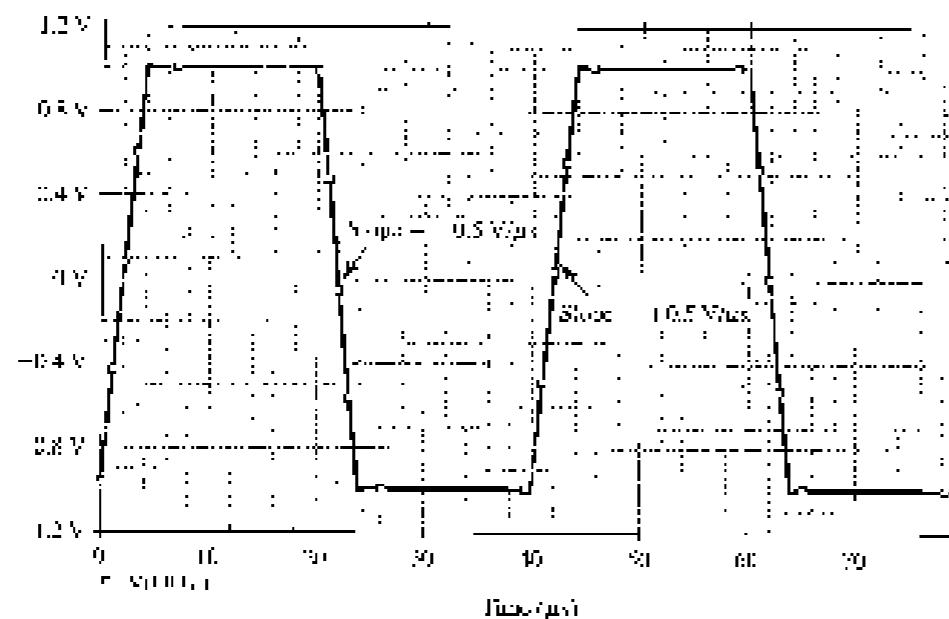


FIGURE 2.52 Step response of the PA241 op-amp connected in the non-inverting configuration shown in Fig. 2.51.

SUMMARY

- The IC op-amp is a versatile circuit building block. It is easy to apply, and the performance of op-amp circuits directly relates to standard integrated circuits.
- The non-inverting input (the inverting input is held at the negative feedback input terminal (2); the output terminal (3); the positive supply terminal (V_{CC}) is connected to the positive power supply, and the negative supply terminal (V_{DD}) is connected to the negative supply. The common terminal of the two supplies is the circuit ground.)
- The ideal op-amp responds only to the difference input signal. That is, $V_{o2} - V_{o1}$ provides at the output, between node 3 and ground, a signal $A(V_{o1} - V_{o2})$, where A , the

open-loop gain, is very large ($> 10^6$) and ideally infinite, so it contains no finite input resistance and a zero output resistance.

- Negative feedback is applied to an op-amp by connecting a resistor between its output terminal and its (inverting, negative) input terminal. Negative feedback reduces the voltage between the two input terminals to become $V_{o2} \approx V_{o1} \approx 0$ (that is, zero). Correspondingly, a signal short circuit is said to exist between the two input terminals. If the positive input terminal is connected to ground, a virtual ground appears at the negative input terminal.
- The two most important assumptions in the analysis of op-amp circuits, presuming negative feedback exists and the op-amps are ideal, are (1) the two input terminals carry the same voltage, sum-zero current flows into the op-amp input terminals, and (2) the output voltage is zero.
- With negative feedback applied and the dc bias closed, the closed-loop gain is almost entirely determined by external components. For the inverting configuration, $V_o/V_i = -R_2/R_1$, and for the non-inverting configuration, $V_o/V_i = 1 + R_2/R_1$.
- The non-inverting op-amp configuration features a very high input resistance. A special case is unity-gain feedback. Frequently employed as a buffer amplifier, it connects a high-resistance source to a low-resistance load.
- For most, internally compensated op-amps, the op-amp gain falls off with frequency at a rate of -20 dB/Decade , reaching unity gain at a frequency f_u (the unity-gain bandwidth). However, f_u is not known as the gain-bandwidth product of the op-amp ($= A_u f_u$), where A_u is the open-loop gain, and f_u is the 3-dB frequency of the open-loop gain. At any frequency $f < f_u$, the op-amp gain is $A = A_u f_u/f$.
- For both the inverting and non-inverting closed-loop configurations, the maximum rate of change of the output voltage dV_o/dt is called the slew rate. The slew rate, SR , is usually specified in V/ μs . Driven oscillating can result in nonlinear distortion of output signal waveforms.
- The full-power bandwidth, f_{HP} , is the maximum frequency at which an output sinusoid with an amplitude equal to the open-loop output voltage ($V_{o2,OL}$) can be produced without distortion: $f_{HP} = 38.2\pi V_{o2,OL}$.
- The input offset voltage, V_{IO} , is the magnitude of dc voltage that must be applied between the inverting input terminals, with appropriate polarity, to make the dc output voltage at the output to be zero.
- The effect of V_{IO} on performance can be evaluated by including it in the analysis of dc source E_{IO} in series with the op-amp positive input lead. For both the inverting and the non-inverting configurations, V_{IO} results in a dc offset voltage of the output of $V_{o2,OL} + E_{IO}/R_1$.
- Capacitively coupling an op-amp reduces the dc offset voltage at the output.
- The voltage-controlled voltage source (I_2) is the voltage at the input terminals of the op-amp, as well as the input bias current, I_B . In a closed-loop amplifier, I_2 is referred to as a dc offset voltage at the output of magnitude $I_2 R_2$. This voltage can be reduced to $I_2 R_2$ by connecting a resistance in series with the positive input terminal equal to the total input resistance seen by the negative input terminal. I_2 is the input offset current (that is, $I_2 = I_B + I_{o2}$).
- Connecting a large resistance in parallel with the capacitors of an op-amp having integrator prevents op-amp oscillation due to the effect of I_{o2} and I_{p1} .

PROBLEMS

SECTION 2.1: THE IDEAL OP AMP

- 2.1 What is the number of pins required for a single-chip four-op-amp IC package, one containing two op-amps? What is the number of pins required for a surface-mount quad op-amp package, one containing four op-amps?
- 2.2 The circuit of Fig. P2.2 uses an op-amp that is ideal except for having a finite gain A . Measurements indicate $V_o = 4.0\text{ V}$ when $V_i = 4.0\text{ V}$. What is the open-loop gain?
- 2.3 Measurement of a circuit incorporating what is thought to be an ideal op-amp shows the voltage at the op-amp output to be

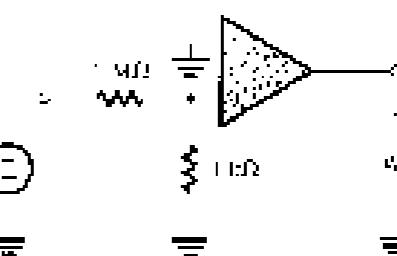


FIGURE P2.2

2.000 V and that of the negative input to be -1.000 V. For the output to be 0.500, what would you expect the voltage at the positive input to be? If the measured voltage of the positive input is -0.920 V, what is likely to be the actual gain of the amplifier?

2.4 A load of 1 k Ω is run on one output of an ideal op-amp (except for having a finite gain A). The results are tabulated below. Are the results consistent? If not, are they reasonable in view of the possibility of exponential error? What do they show? The output voltage of the op-amp can be expressed as

$$V_O = A_{vD} V_{IN} + A_{vC} V_{IN}$$

where A_{vD} is the differential gain (assumed to simply equal the test), and A_{vC} is the common-mode gain (assumed to be zero in the test). The op-amp's effectiveness in rejecting common-mode signals is measured by its CMRR, A_{vC}/A_{vD} :

$$\text{CMRR} = 20 \log_{10} \left| \frac{A_{vD}}{A_{vC}} \right|$$

Consider an op-amp whose internal structure is of the type shown in Fig. 2.3 except for a transistors ΔG_2 between the transistors of the two cascodes; that is,

$$G_{oD} = R_o + \frac{1}{2} \Delta G_o$$

$$G_{oC} = G_o + \frac{1}{2} \Delta G_o$$

Find expressions for A_{vD} , A_{vC} , and CMRR. If R_o is 10 M Ω and the two transistors are matched to within 0.1% of each other, calculate A_{vD} and CMRR.

SECTION 2.2: THE INVERTING CONFIGURATION

2.5 Assuming ideal op-amps, find the voltage gain v_o/v_i and input resistance R_i of each of the circuits in Fig. 2.8.

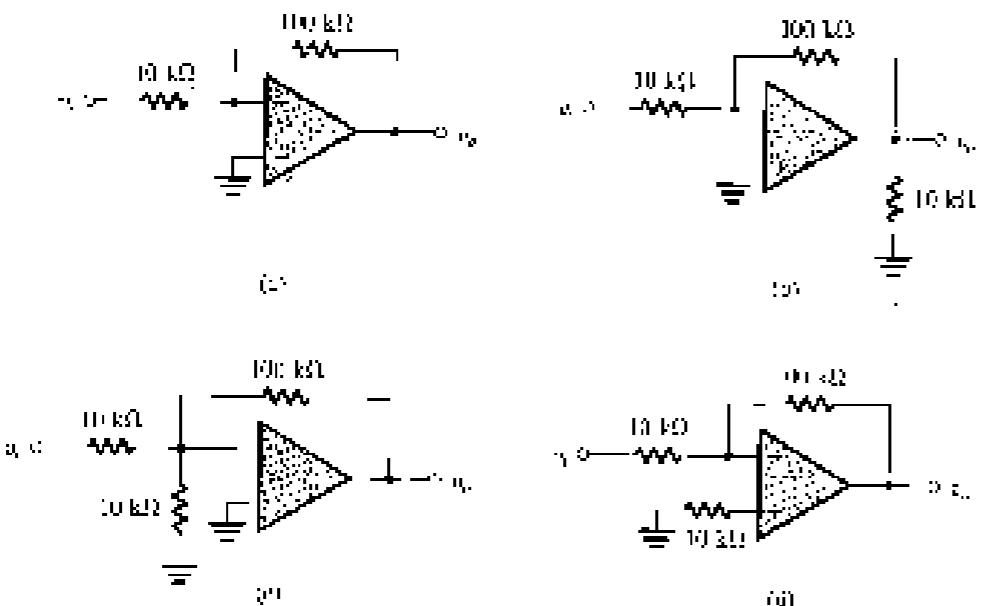


FIGURE P2.8

2.9 A particular inverting circuit uses an ideal op-amp and a 10-k Ω resistor. What closed-loop gain would you expect? If an input voltage of 1.500 V is applied to the input, what output result? If the 10-k Ω resistors are set to be "hot resistors," having values exactly 1% off the range ($+/- 0.05$) times the nominal value, what range of outputs would you expect to actually measure? (a) output precisely 5.00 V?

2.10 You are provided with an ideal op-amp and three 1-k Ω resistors. Using series and parallel resistor configurations, how many different inverting-amplifier circuit topologies are possible? What is the largest (most negative) available voltage gain? What is the smallest (most positive) available gain? What are the two resistances in these two cases?

2.11 For ideal op-amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

- (a) $R_1 = 10 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$
- (b) $R_1 = 10 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$
- (c) $R_1 = 10 \text{ k}\Omega$, $R_2 = 1 \text{ k}\Omega$
- (d) $R_1 = 100 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$
- (e) $R_1 = 100 \text{ k}\Omega$, $R_2 = 1 \text{ M}\Omega$

2.12 Using an ideal op-amp, what are the values of the resistors R_1 and R_2 to be used to design amplifiers with the closed-loop gains listed below? (a) you choose, use an east end 10-k Ω resistor and another target resistor

- (a) -1 V/V
- (b) -2 V/V
- (c) -0.5 V/V
- (d) -100 V/V

2.13 Design an inverting op-amp circuit for which the gain is -5 V/V and the load resistance is 120 k Ω .

2.14 Using the circuit of Fig. 2.5 and assuming an ideal op-amp, design an inverting amplifier with a gain of 29 dB having the largest possible load resistance under the constraint of having all the resistors in the circuit larger than 10 M Ω . What is the input resistance of your design?

2.15 An ideal op-amp connected as shown in Fig. 2.5 of the text with $R_1 = 10 \text{ k}\Omega$ and $R_2 = .001 \text{ k}\Omega$. A 50-mV sinusoidal wave signal with a bias of 1 V and 100 Hz is applied at the input. Sketch how it will affect the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

2.16 For the circuit in Fig. P2.16, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op-amp is greater than the current drawn from the input signal source, where does the additional current come from?

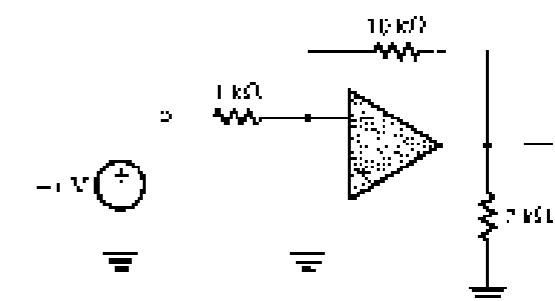


FIGURE P2.16

2.17 An inverting op-amp circuit is fabricated with two resistors R_1 and R_2 , using 1% tolerance (i.e., the value of each resistance can deviate from the nominal value by as much as 1%). What is the tolerance on the inverting closed-loop gain? Assume the op-amp to be ideal. If the nominal closed-loop gain is -100 V/V and $R_1 = 10 \text{ k}\Omega$, what is the range of gain values expected from such a circuit?

2.18 An ideal op-amp with 5.100 and 10.000 resistors is used to generate 15 V supply from a 10-V reference. Sketch the circuit. What are the voltages (in V) across the 5-k Ω resistor? (These resistors are cascaded 1% resistors—what are their values? see the range bounded by the nominal values.) (a) what are the limits of the output voltage produced? If the 10-V supply can also vary by 1%, what is the range of the output voltages that might be found?

2.19 An inverting op-amp circuit for which the required gain is -50 V/V cannot operate whose closed-loop gain is only -40 V/V. If the larger resistor used is 100 k Ω , to what must the smaller be reduced? Which resistor must a 2-k Ω resistor connected to the input be shunted to achieve this goal? (Note that a resistor R_2 is said to be shunted by resistor R_1 if R_2 is placed in parallel with R_1 .)

2.20 (a) Design an inverting op-amp with a closed-loop gain of -100 V/V and an input resistance of 10 k Ω .
(b) If the op-amp is known to have an open-loop gain of 1000 V/V, what do you expect the closed-loop gain of your circuit to be (assuming the resistors have precise values)?

(c) Give the value of a resistor you can place in parallel (shunt) with R_2 to restore the closed-loop gain to its nominal value. Use the closest standard 1% resistor value (see Appendix G).

2.21 An op-amp with an open-loop gain of 1000 V/V is used in the inverting configuration. If in this application the output voltage ranges from -10 V to +10 V, what is the maximum voltage by which the "virtual-ground node" departs from its ideal value?

2.22 The circuit in Fig. P2.22 is designed need to provide an output voltage v_o proportional to an input signal v_i such that the transresistance $R_t = v_o/v_i$, and the input resistance $R_i = R_1/R_2$ for the following cases:

- A is infinite.
- A is finite.

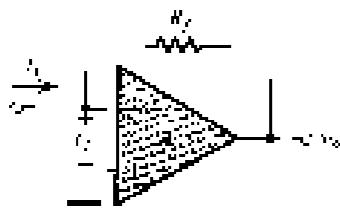


FIGURE P2.22

2.23 Derive an expression for the input resistance of the inverting amplifier of Fig. 2.5 taking into account the finite open-loop gains of the op-amp.

***2.24** For a inverting op-amp with open-loop gain A_{OL} and minimum closed-loop gain $A_{CL,MIN}$ find the minimum value of the pair (R_1, R_2) in series at R_1/R_2 for a gain range of 0.1%, 1%, and 10%. In each case, what value of resistance can be used to short R_1 (reduce the noise voltage)?

2.25 Figure P2.25 shows an op-amp that is used as a follower having a finite open-loop gain and is used as a driver or inverting amplifier where you have a normal input voltage v_i and $G = R_2/R_1$. To carry out the derivation due to the finite open-loop gain A_{OL} is shorted across R_1 . Show that perfect compensation is achieved when R_2 is selected according to

$$\frac{R_2}{R_1} = \frac{A_{OL}}{G + A_{OL}}$$

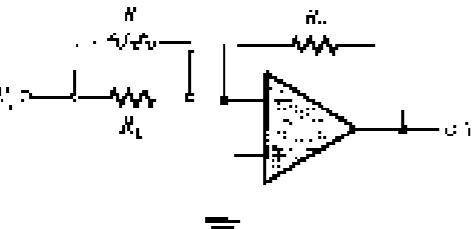


FIGURE P2.25

***2.26** Rearrange Eq. (2.5) to give the amplifier open-loop gain A required to realize a specific closed-loop gain ($G_{CL,MIN} = R_2/R_1$) with a specified gain error.

$$A = \frac{G - G_{CL,MIN}}{G_{CL,MIN} - 1}$$

For a closed-loop gain of 100 and a gain error of $\pm 10\%$, what is the minimum A required?

2.27 Using Eq. (2.5), determine the value of A for which the deviation of A by $\pm 10\%$ results in a reduction in $|G|$ by $(\pm 1)\%$. Find the value of A required for the case in which the nominal closed-loop gain is 100, $\epsilon = 50$, and $\epsilon_0 = 100$.

2.28 Consider the circuit in Fig. 2.8 with $R_1 = R_2 = R_4 = 1\text{ k}\Omega$, and assume the op-amp to be ideal. Find values for R_3 to attain the following gains:

- 0 V/V
- 100 V/V
- 2 V/V

2.29 An inverting op-amp circuit using an ideal op-amp must be designed to have $v_{out}/v_i = 1000\text{ V/V}$ in a range of no larger than $\pm 10\text{ mV}$.

(a) For the single two-resistor circuit, what input resistances would be used?

(b) If the circuit in Fig. 2.8 is used with no resistors of maximum value, what input resistance would be the maximum allowed value for R_3 ?

(c) If R_1 is varied in the range $100\text{ }\Omega$ to $1\text{ k}\Omega$, what is the corresponding change in R_2 and in v_{out} ?

2.30 The inverting circuit with the feedback in the feedback is redrawn in Fig. P2.30 in a way that emphasizes the observation that R_1 and R_2 in (2.5) are in parallel because the ideal op-amp forces a virtual ground at the inverting input terminal. Use this observation to derive an expression for the open-loop gain by first finding v_{o1}/v_{o2} and v_{o2}/v_i .

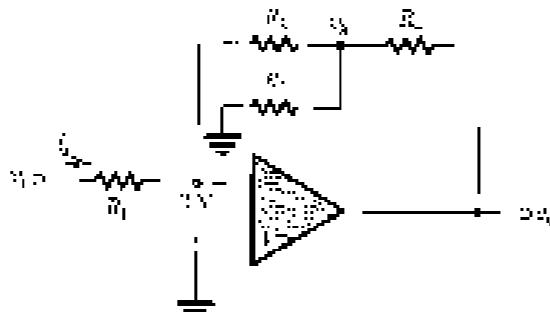


FIGURE P2.30

***2.31** The circuit in Fig. P2.4 can be considered an extension of the circuit in Fig. 2.8.

(a) Find the re-isources looking into nodes 1, R_1 ; node 2, R_2 ; node 3, R_3 ; and node 4, R_4 .

(b) Find the currents i_1, i_2, i_3 , and i_4 in terms of the input current i .

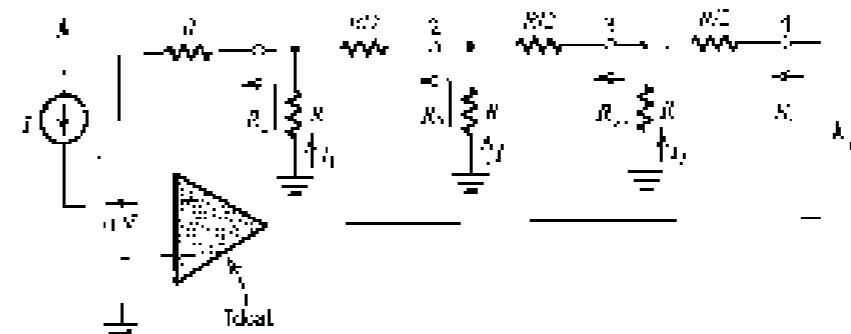


FIGURE P2.31

(c) Find the voltage amplitudes v_2, v_3, \dots, v_{14} (that is, $v_1, v_2, v_3, \dots, v_{14}$) in terms of v_i .

2.32 The circuit in Fig. P2.32 utilizes an ideal op-amp.

(a) If R_1, R_2 , i_1 , and v_{o1} :

(b) If v_{o1} is set to be lower than -15 V , for the maximum allowed value for R_2 :

(c) If R_1 is varied in the range $100\text{ }\Omega$ to $1\text{ k}\Omega$, what is the corresponding change in i_1 and in v_{o1} ?

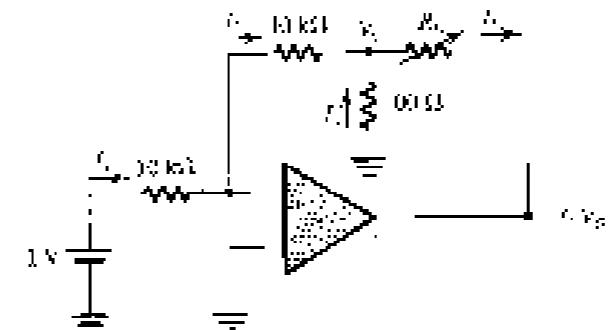


FIGURE P2.32

2.33 Assuming the op-amp to be ideal, it is required to design the circuit shown in Fig. P2.33 to implement a unity-gain buffer with gain $i_2/i_1 = 20\text{ A/A}$.

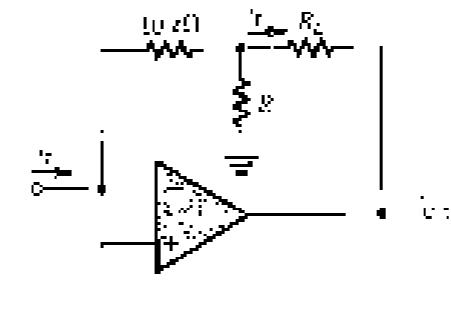


FIGURE P2.33

(d) Find the required value for R_3 .

(e) If $R_1 = 1\text{ k}\Omega$ and the open-loop voltage is an ideal number, how is v_{o1} in the range $\pm 12\text{ V}$? What range of i_2 is possible?

(f) What is the input resistance of the current amplifier? If the amplifier is fed with a current source I_1 of a current of 10 A and a source resistance of $411\text{ }\Omega$, find i_2 .

2.34 Figure P2.34 shows the unity-gain amplifier circuit of Fig. 2.8 redrawn to emphasize the fact that R_1 and R_2 can be thought of as a voltage divider connected across the output v_o and from which a fraction of the output voltage (that available at node A) is fed back through R_3 , assuming $R_3 \gg R_1$ and thus that the loading of the feedback network can be ignored, expressed as a function of v_o . Now express v_o as a function of v_i . Are they the same? If not, find the approximate relationship between v_o and v_i . Will appropriate manipulation compare it with the result obtained in Example 2.1. Show that the exact result can be obtained by noting that R_3 appears in series across R_1 and, thus, that the voltage is divided in proportion of R_1 and $(R_1 + R_3)$.

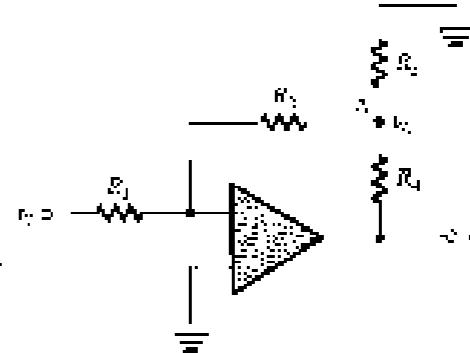


FIGURE P2.34

2.35 Design the circuit shown in Fig. P2.35 to have an input resistance of $100\text{ M}\Omega$ and a gain $i_2/i_1 = 100$ over the range $1\text{ V/V} \leq v_o \leq 10\text{ V/V}$ using the 1-dB pole junction R_2 . Write

voltage gain results when the potentiometer is set exactly at its mid-value?

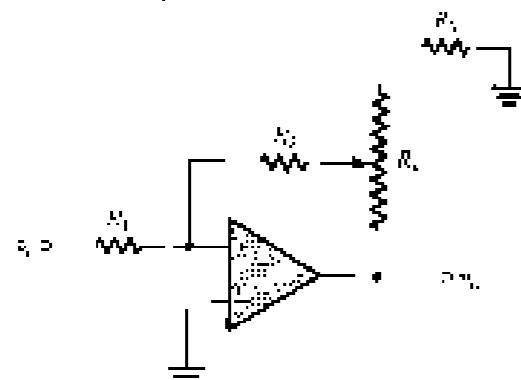


FIGURE P2.35

- P2.36** A strip-line summer circuit using an ideal op-amp has three inputs (each 100 kΩ resistors) and a feedback resistor of 10 kΩ. A signal v_1 is connected to one of the inputs while a signal v_2 is connected to the third. Express v_o in terms of v_1 and v_2 . If $v_1 = 5 \text{ V}$ and $v_2 = 1 \text{ V}$, what is v_o ?

- P2.37** Use an op-amp circuit to provide a output $v_o = v_1 + 2v_2 + 3v_3$. Use exclusively $10\text{-k}\Omega$ resistors for which the input current is 10 nA each. Input voltage sources are caused 0.1 mA for 1-V input signals.

- P2.38** Using the scheme illustrated in Fig. 2.10, design a summing circuit with inputs v_1 , v_2 , and v_3 whose output is $v_o = -2v_1 - 4v_2 - 8v_3$ using small resistors but no load less than $10\text{k}\Omega$.

- P2.39** An ideal op-amp is connected in a weighted summing configuration (Fig. 2.10). The feedback resistor is $10\text{k}\Omega$ and no 10-kΩ resistors are connected to the inverting input terminal of the op-amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

- $v_o = v_1 + 2v_2 - 5v_3$
- $v_o = -5v_1 - 8v_2 - 2v_3$
- $v_o = v_1 + 4v_2$
- $v_o = 6v_1$

In each case find the input resistance seen by each of the input voltage supplies v_1 , v_2 , v_3 , and v_o . Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is 0.5?

- P2.40** Give a circuit example with component values for a weighted summing junction that shifts the dc level of a sine wave signal by $10(0.1) \text{ V}$ (dc level to 0.1 V). Assume that in addition to the 0.1-V offset signal you have a reference voltage of 2 V available. Sketch the output signal waveform.

- D2.41** Use two ideal op-amps and resistors to implement the summing function

$$v_o = v_1 + 2v_2 - 3v_3 - 5v_4$$

- D2.42** In an instrumentation system, there is a need to take the difference between two signals, one of $v_1 = 3\sin(2\pi \times 60\text{Hz}) + 0.01 \sin(2\pi \times 1000\text{Hz})$ volts, and another of $v_2 = 3\sin(2\pi \times 60\text{Hz}) + 0.01 \sin(2\pi \times 1000\text{Hz})$ volts. Draw a circuit that finds the required difference using two op-amps and many 10-kΩ resistors. Since 1 is available to amplify the 100-Hz component in the process, arrange to provide an overall gain of $10 \rightarrow 10^2$. The op-amps available are ideal except that their output voltage swing is limited to $\pm 20 \text{ V}$.

- D2.43** Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $v_{1:0}v_{3:0}$, where v_0 , v_1 , v_2 , and v_3 take the values of 0 or 1, and it provides an analog output voltage v_o proportional to the value of the digital word. Each of the bits of the input word controls the corresponding numbered switch. For instance, if $v_1=1$ then switch 1 connects the 10-kΩ resistor to ground, while if $v_2=1$ the switch connects the 20-kΩ resistor to the 5-V power-supply line so that v_o is given by

$$v_o = \frac{R_f}{R_s} [2^0v_0 + 2^1v_1 + 2^2v_2 + 2^3v_3]$$

where R_s is in kΩ. Find the value of R_f so that v_o ranges from 0 to 12 volts.

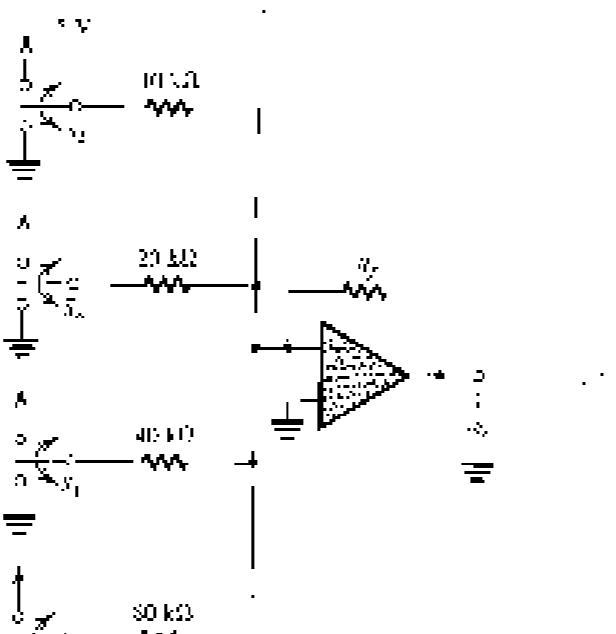


FIGURE P2.43

SECTION 2.3: THE NONINVERTING CONFIGURATION

- D2.44** Using analysis of loop gain, determine designs for the following closed-loop gain. Assume values of the gains (k_1 , k_2) should be unity. Where possible, use $10\text{-k}\Omega$ resistors and the smallest resistor in your design.

- 5 V/V
- +2 V/V
- 10 V/V
- +10.0 V/V

- D2.45** Design a circuit based on the topology of the noninverting amplifier to obtain a gain of $\pm 5 \text{ V/V}$, using only 10-kΩ resistors. Note that there are two possible fits. Which of these can be easily converted to have a gain of either $\pm 3 \text{ V/V}$ or $\pm 2.0 \text{ V/V}$ supply by short-circuiting a single 10-kΩ in each case?

- D2.46** Figure P2.46 shows a circuit for an analog voltmeter of very high input impedance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage V applied between the op-amp's noninverting terminal and ground. Assuming that the moving coil passes full-scale deflection when the current passing through it is 20 mA, and the value of R such that full-scale reading is obtained when V is 10 V, gives the meter resistance required to obtain the voltmeter calibration?

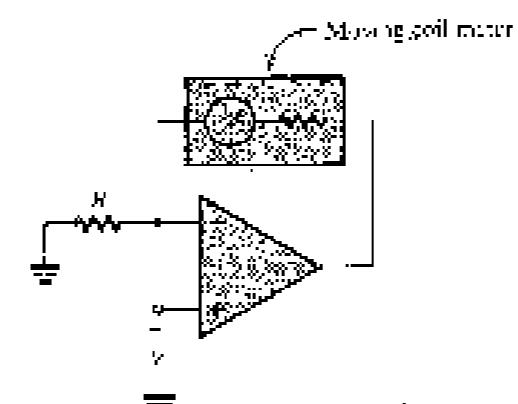


FIGURE P2.46

- D2.47** Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$\begin{aligned} v_o &= \frac{-R_f}{1+R_{f1}} v_1 + \frac{-R_f}{1+R_{f2}} v_2 + \cdots + \frac{-R_f}{1+R_{fn}} v_n \\ &= 1 + \frac{R_{f1}}{R_{f2}} \frac{v_1}{v_2} + \frac{R_{f2}}{R_{f3}} \frac{v_2}{v_3} + \cdots + \frac{R_{fn}}{R_{f1}} \frac{v_n}{v_1} \end{aligned}$$

where $R_{fi} = R_f / (R_{fi} + R_{oi})$ for $i = 1, 2, \dots, n$ and $R_{oi} = R_{oi} / (R_{fi} + R_{oi})$.

- E2.48** Design a circuit using an ideal op-amp whose output is $v_o = v_1 + 2v_2 - 3v_3 - 4v_4$. (Hint: Use a structure similar to that shown in general form in Fig. 2.45.)

- E2.49** Derive an expression for the voltage gain, v_o/v_i , of the circuit in Fig. P2.49.

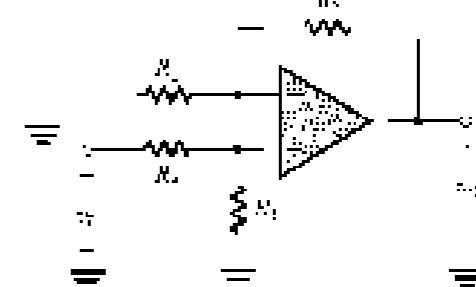


FIGURE P2.49

- E2.50** For the circuit in Fig. E2.50, use superposition to find v_o in terms of the input voltages v_1 and v_2 . Assume A is an ideal op-amp. For

$$v_1 = 10\sin(2\pi \times 60\text{Hz}) + 0.1\sin(2\pi \times 1000\text{Hz}) \text{ volts}$$

$$v_2 = 10\sin(2\pi \times 60\text{Hz}) + 0.1\sin(2\pi \times 10\text{kHz}) \text{ volts}$$

$$R_1 = R_2 = R_3 = R_4 = R_f = 10\text{k}\Omega$$

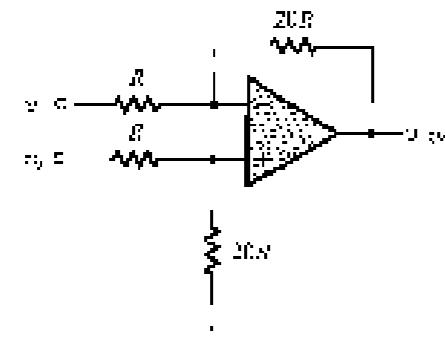


FIGURE P2.50

P2.51 The circuit shown in Fig. P2.51 has two $\pm 10\text{-k}\Omega$ potentiometers in its positive and negative noninverting configurations. Assume the op-amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range will be from 21 to 211 V/V. What should the resistor values be?

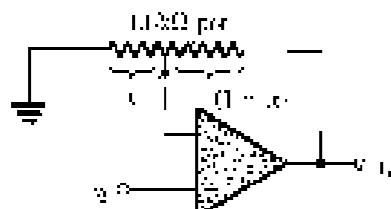


FIGURE P2.51

P2.52 Given the possibility of resistors of value 1 kΩ and 10 kΩ only, design a circuit based on the noninverting configuration to realize a gain of -13 V/V.

P2.53 It is required to connect a 10-V source with a source resistance of 100 kΩ to a 1-kΩ load. Find the voltage that will appear across the load:

- The source is connected directly to the load.
- A unity-gain op-amp buffer is inserted between the source and the load.

In each case find the load current and the current supplied by the source. What does the load current come from? Explain why?

P2.54 Derive an expression for the gain of the voltage follower of Fig. 2.13 assuming the op-amp to be ideal except for having a finite gain A . Calculate the value of the closed-loop gain for $A = 1000$, 100, and 10. In each case find the percentage error in gain magnitude from the nominal value of unity.

P2.55 Calculate the following ratios for the two amplifiers created using one ideal op-amp. Note that R_0 signifies input resistance and R_1 and R_2 are feedback-network resistors as indicated in the inverting and noninverting configurations:

Op-Amp	R_1 (kΩ)	R_2 (kΩ)	R_0 (kΩ)	R_{FB} (kΩ)
a	-0.5 kΩ	10 kΩ	100 kΩ	100 kΩ
b	-1 kΩ	-	100 kΩ	100 kΩ
c	-2 kΩ	-	100 kΩ	100 kΩ
d	1 kΩ	-	100 kΩ	100 kΩ
e	42 kΩ	-	100 kΩ	100 kΩ
f	+1.5 kΩ	-	100 kΩ	100 kΩ
g	0.5 kΩ	20 kΩ	100 kΩ	100 kΩ

P2.56 A noninverting op-amp circuit with an input offset of 10 mV uses an op-amp with open-loop gain of 50 V/V and a lowest common-mode voltage of 10 mV. Regardless of loop gain, what will happen if the input voltage V_1 is 10 mV? Assume the op-amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range will be from 21 to 211 V/V. What should the resistor values be?

P2.57 Using Eq. (2.11), show that if the reduction in the closed-loop gain G from its nominal value $G_V = 1 + R_2/R_1$ is to be kept less than 1% of G_V , then the open-loop gain of the op-amp must exceed G_V by at least a factor $F = (1.00/\epsilon)^{1/2} \approx 1.0116$. Find the required F for $\epsilon = 0.01$, 0.1, 1, and 10. Use these results to find the required minimum required open-loop gain to obtain closed-loop gain of ± 1 , 10, 10², 10³, and 10⁴ V/V.

P2.58 For each of the following combinations of op-amp open-loop gain A and common-mode closed-loop gain G_V , calculate the actual closed-loop gain G that is achieved. At 1-V, calculate the percentage by which $|G|$ falls short of the nominal gain magnitude G :

Op-Amp	G_V (V/V)	A (V/V)
a	-1	10
b	+1	10
c	-1	100
d	-10	10
e	-10	100
f	10	1000
g	1	2

P2.59 Figure P2.59 shows a circuit that provides an output voltage $v_o = \pm 10$ V, however, by turning the wiper of the 100-kΩ potentiometer R , the range over which v_o can be varied. If the potentiometer is a "104.0" device, find the change in v_o corresponding to each turn of the pot.

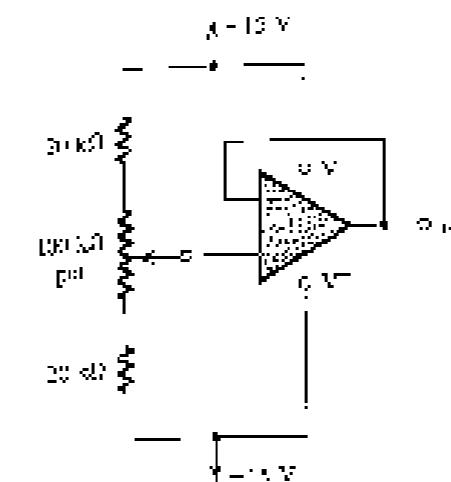


FIGURE P2.59

P2.63 Consider the difference amplifier of Fig. 2.18 with the two input terminals connected together as an in- π current-mode signal source. If $R_2/R_1 = R_4/R_3$, show that the input common-mode resistance is $(R_2 + R_4)/(R_1 + R_3)$.

P2.64 Consider the circuit of Fig. 2.18, and for each of the two ± 1 -V digital sources have a series resistance R . What conditions must apply in each of the two resistors R_1 and R_3 in order for the amplifier to function as a closed-difference amplifier?

P2.65 For the difference amplifier shown in Fig. 2.18, let all the resistors be 100 kΩ ± 1%. Find an expression for the resulting common-mode CMRR. Evaluate this for $\epsilon = 0.1$, 1, and 5. Also, evaluate the resulting CMRR in each case.

P2.66 For the difference amplifiers of Fig. 2.18, know that each resistor has a tolerance of ±10% (i.e., due to a 5% loss that $\epsilon = 0.001$); then the worst-case CMRR is given approximately by

$$\text{CMRR} = 20 \log \left[\frac{K+1}{1} \right]$$

where K is the nominal value of the ratio $(R_2/R_1) + (R_4/R_3)$. Calculate the value of ϵ such that CMRR for the amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op-amp is ideal and that 1% resistors are used.

P2.67 Design the difference amplifier circuit of Fig. 2.18 to realize a differential gain of 100, a differential input resistance of 20 kΩ, and a minimum CMRR of 80 dB. Assume the op-amp is ideal. Specify the component values and their required values (e.g., better than 1%).

P2.68 (a) Draw a ± 1 -V common-mode difference amplifier circuit shown in Fig. P2.68. The op-amp is specified to operate properly so long as the common-mode voltage of its positive and negative inputs lies in the range ± 2.5 V, what is the corresponding limitation on the range of the input common-mode signal v_{ci} ? This is known as the common-mode range of the difference amplifier.

(b) The circuit is modified by connecting a 10-kΩ resistor between node A and ground and another 10-kΩ resistor between node B and ground. What will now be the values of A_1 , A_{11} , and the input common-mode voltage?

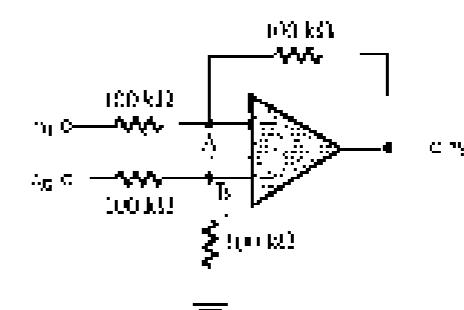


FIGURE P2.68

*2.69 To obtain a high-gain, high-input-resistance differential amplifier circuit (as shown in Fig. 2.16) one employs negative feedback in addition to the negative feedback provided by the resistor R_2 connected from the output to the negative input of the op-amp. Specifically, a voltage divider (R_3, R_4) connected across the output feeds a fraction β of the output, that is, a voltage βv_{out} , back to the positive input terminal of the op-amp through its bias node R_1 . Assume that R_3 and R_4 are much smaller than R_2 so that the current through R_2 is much lower than the current in the voltage divider, with the result that $\beta = R_3/(R_3 + R_4)$. Show that the differential gain is given by

$$A_d = \frac{v_o}{v_{in}} = -\frac{1}{\beta}$$

Design the circuit to obtain a differential gain of 10 kV/V and differential load resistors of 1.3 M Ω . Select values for R_1, R_2 , and R_3 such that $|R_3| + |R_4| \leq R_1/R_2$.

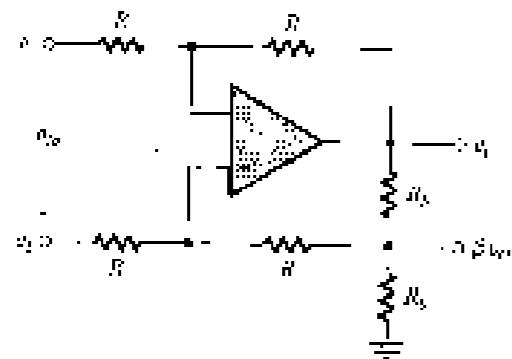


FIGURE P2.69

*2.70 Figure 22.10 shows a modified version of the E-gain circuit. The modified circuit includes a resistor R_{10} , which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_o}{v_{in}} = -\frac{R_2}{R_1} \frac{1 + R_{10}}{1 + R_{10}}$$

(a) The virtual short current of the op-amp input stages can flow through the R_{10} resistor to be $v_{in}/20 k\Omega$.

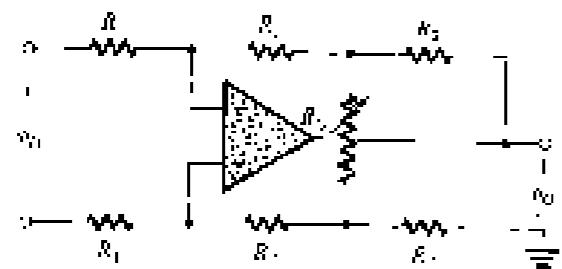


FIGURE P2.70

*2.71 The circuit shown in Fig. P2.71 is a preamplifier of a transimpedance common-emitter available IC, the JN4100, manufactured by Burr-Brown and known as a differential amplifying module. In view of its low input and parasitic noise-induced, overdriven, nonlinearities, this circuit can be configured for a variety of applications by the appropriate connection of terminals A, B, C, D, and G.

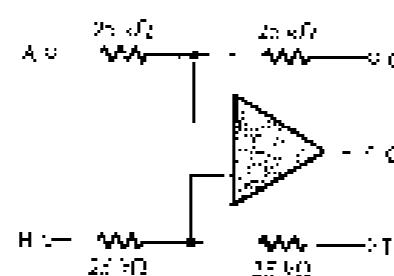


FIGURE P2.71

- (a) Show how the circuit can be used to implement a differential amplifier of unity gain.
 (b) Show how the circuit can be used to implement a differential amplifiers with gains:

- (i) 1 V/V
- (ii) 10 V/V
- (iii) 2 V/V
- (iv) 40 V/V

Avoid leaving a terminal open-circuited, for such a terminal may act as an antenna, picking up interference and noise through capacitive coupling. Rather, find a convenient way to connect such a terminal in a redundant way. When more than one closed-loop configuration is possible, comment on the relative merits of each, taking into account such considerations as dependence on component matching and load resistance.

2.72 Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of ± 15 V (DC) and a differential input signal of 100 mV peak-to-peak sine wave. Let $2\beta_1 = 14$ k Ω , $R_2 = 30$ k Ω , $R_3 = R_4 = 10$ k Ω . Find the voltage at every node in the circuit.

2.73 (a) Consider the instrumentation amplifier circuit of Fig. 2.20(a). If the op-amps are ideal except that their outputs are at ± 15 V, in the manner shown in Fig. 1.14, find the maximum allowed input common-mode signal for the case $R_1 = 100$ k Ω and $R_2 = 100$ k Ω .

(b) Repeat (a) for the circuit in Fig. 2.20(b), and comment on the difference between the two designs.

2.74 (a) Expressing v_o and v_{o2} in terms of differential and common-mode components, find v_{od} and v_{oc} in the circuit in Fig. 2.20(a) and hence find their common-mode component $v_{oc} = v_{od}$ and their common-mode component $v_{od} = (v_{od} + v_{oc})/2$. Now find the differential gain, i.e., the common-mode gain of

the first stage of this instrumentation amplifier and hence the CMRR.

(b) Repeat for the circuit in Fig. 2.20(b), and compare on the differences between the two circuits.

*2.75 Design an instrumentation amplifier of the type shown in Fig. 2.21(a). A designer proposes to make $R_1 = R_2 = 100$ k Ω , and $2\beta_1 = 10$ k Ω . For this component, what is the transconductance, common-mode gain, and CMRR result? If you like, use the worst-case values for loads in the estimation in which all resistors are specified at $\pm 10\%$ parts. Repeat the latter analysis for the case in which R_1 is reduced to 1 k Ω . What do you conclude about the importance of the relative drifts in gains of the first and second stages?

2.76 Design the instrumentation amplifier circuit of Fig. 2.21(b) to realize a differential gain variable in the range 1 to 100, using a 100-k Ω potentiometer as variable resistor. (Hint: Design the second stage for a gain of 1.)

2.77 The circuit shown in Fig. 2.77 is intended to supply a voltage to floating loads (these for which both terminals are ungrounded) while making greatest possible use of the available power supply.

- (a) Assuming ideal op-amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied to v_i . Also sketch v_o .
 (b) What is the value of v_o/v_i ?
 (c) Assuming that the op-amps operate from ± 15 -V power supplies, and further output voltage $v_o = 4$ V for the maximum value of v_i , calculate the DC currents between the two circuits.

2.78 The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters. That is, they supply the load impedance Z_L with a current proportional to v_i and independent of the value of Z_L . Show that this is indeed the case, and find for each circuit v_o as a function of v_i . Comment on the differences between the two circuits.

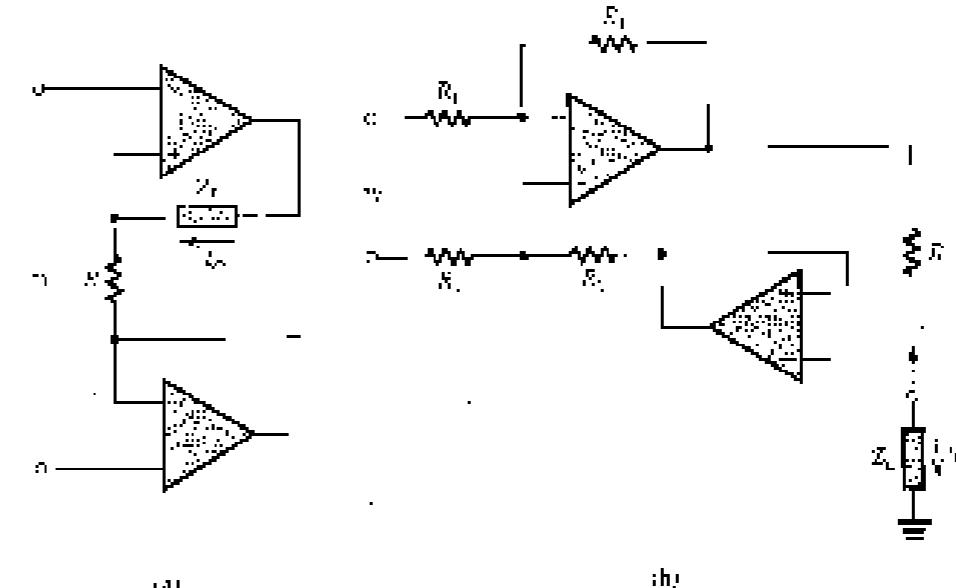


FIGURE P2.78

SECTION 2.5: EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH ON CIRCUIT PERFORMANCE

2.78 The data in the following table apply to internally compensated op amps. Fill in the blank entries.

	100 Hz	1 kHz
10 ³	10 ³	
10 ⁴	10 ⁴	
10 ⁵	10 ⁵	
10 ⁶	10 ⁶	
2 × 10 ⁶	10	

2.79 A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 80 dB; at 100 Hz, this shows it is 40 dB. Estimate ω_{OL} for the op amp. (Note: The step response of SIC low-pass networks is discussed in Appendix D.)

2.80 It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 10.0 mV is applied at the inverter input, the output is within 1% of its final value of 11 V in about 100 ms. What is ω_{OL} of the op amp? Note: The step response of SIC low-pass networks is discussed in Appendix D.)

2.81 Measurements of the open-loop gains of a compensated op amp intended for high-frequency operation indicate that the gain is $5.1 \times 10^3 \pm 0.1$ dB at $\omega = 10$ rad/s. Estimate the 3-dB frequency, the unity-gain frequency, and its dc gain.

2.82 Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3-dB and unity-gain frequencies?

- (a) -100 V/V at 10×10^3 Hz
- (b) -50 V/ μ V at 10 Hz
- (c) -150 V/V and 0.1 MHz
- (d) -100 V/V and 0.1 GHz
- (e) 25 V/mV and 25 MHz

2.83 An inverting amplifier with no gain, a -20 V/V output, an op amp having a dc gain of 10⁶ and a unity-gain frequency of 10³ Hz. What is the 3-dB frequency f_{3dB} of the closed-loop circuit? What is its gain at 0.1 f_{3dB} and at 10 f_{3dB} ?

2.84 A particular op amp, characterized by a gain bandwidth product of 20 MHz, is connected with a closed-loop gain of -100 V/V. If the 3-dB bandwidth requirement is 1000 times frequency does the closed-loop amplifier exhibit a 180° phase shift? A 90° phase shift?

2.85 Find the f_{3dB} required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:

- (a) -100 V/V; 100 kHz
- (b) -100 V/V; 10 kHz
- (c) -2 V/V; 1 MHz
- (d) -2 V/V; 10 MHz
- (e) -1000 V/V; 20 kHz
- (f) -1000 V/V; 1 MHz
- (g) -1 V/V; 1 MHz

2.86 A noninverting op amp circuit with a gain of 100 V/V is required to have a 3-dB frequency of 8 kHz. For a particular application, a bandwidth of 20 kHz is required. What is the highest gain available under these conditions?

2.87 Consider a unity-gain follower or inverting op amp with $f_0 = 1$ MHz. What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 10 times greater than the gain of the inverter? (Hint: In each case, the other input to the summer can be set to ground—a application of superposition.)

2.88 It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 10.0 mV is applied at the inverter input, the output is within 1% of its final value of 11 V in about 100 ms. What is ω_{OL} of the op amp? Note: The step response of SIC low-pass networks is discussed in Appendix D.)

2.89 This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single voltage amplifier with the same overall gain.

(a) Show that cascading two identical amplifier stages, each having a low-pass SIC frequency response with a 3-dB frequency f_{3dB} , results in an overall amplifier with a 3-dB frequency f_{3dB} .

(b) Show that cascading two identical amplifier stages, each having a low-pass SIC frequency response with a 3-dB frequency f_{3dB} , in an overall amplifier with a 3-dB frequency f_{3dB} .

$$f_{3dB} = \sqrt{2} - 1 f_c$$

(c) It is required to design a noninverting amplifier with a dc gain of -3 dB utilizing a single, internally compensated op amp with $f_0 = 1$ MHz. What is the 3-dB frequency obtained?

(d) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 V/V. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (c).

2.90 A designer, wanting to attain a stable gain of -100 V/V at 1 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her goal? Unfortunately, the new available amplifier has an f_0 of 50 MHz. How many additional stages will be needed in a cascade of identical noninverting stages to achieve her goal? What is the 3-dB frequency of each stage she can use? What is her overall 3-dB frequency?

2.91 Consider the use of an op amp with a unity-gain frequency f_c in the realization of:

- (a) an inverting amplifier with no gain, of magnitude K .
- (b) a noninverting amplifer with a dc gain of K .

In each case, the 3-dB frequency and the gain-bandwidth product ($GWP = Gain \times f_{3dB}$) are given in parentheses.

2.92 Consider an inverting amplifier with two inputs, V_1 and V_2 , such that $V_2 = -V + K$. Find the SIC 1-dB corner of each of the gain functions V_1/V and V_2/V in terms of the op amp's f_0 . Hint: In each case, the other input to the summer can be set to ground—a application of superposition.)

SECTION 2.6: LARGE-SIGNAL OPERATION OF OP AMPS

2.93 A particular op amp using ± 15 -V supplies operates linearly for input voltages in the range -12 V to $+12$ V. If used in an inverting amplifier configuration of gain $= -100$, what is the maximum value of the largest sine wave that can be applied at the input without clipping?

2.94 Consider an op amp connected in the inverting configuation with $V_+ = 0$ V, a load-drain gain of -100 V/V, and driving resistors of $1 \text{ k}\Omega$ and $100 \text{ }\mu\text{A}$. A load resistor R_L is connected from the output to ground, and a 3-dB frequency sawtooth signal of peak amplitude V_p is applied to the input. Let the op amp be ideal except that its output voltage saturates at ± 10 V, and its output current is limited to the range $\pm 0.1 \text{ mA}$.

(a) For $R_L = 1 \text{ k}\Omega$, what is the maximum possible value of V_p while maintaining output saturation?

(b) For $R_L = 10 \text{ k}\Omega$, $R_L = 100 \text{ }\mu\text{A}$,

(c) If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of V_p is allowed?

2.95 An op amp having a slew rate of 0.1 V/ μ s is to be used in the inverting configuration, with input pulse rise time from 0 to 2 V. What is the shortest pulse width that can be used while ensuring full amplitude output? For such a pulse, describe the current switching.

2.96 For operation with 10-V pulse inputs with the requirement that the sum of the rise and fall times should represent only 70% of the total width (or half an cycle), what is the maximum allowable duration for an op amp to switch pulse 1 μ s wide? (Note: The rise and fall times of a pulse signal are usually measured between the 10% and 90% height points.)

2.97 What is the highest frequency of a triangle wave of 20-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is 10 V/ μ s? For a sine wave of the same frequency, what is the maximum output dc component?

2.98 For an op amp having a slew rate of 0.1 V/ μ s, what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

2.99 In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op-amp finite bandwidth (f_0). Show that (SR), the output saturation (V_{sat}),

This problem can be solved by considering the case of an op amp with $f_0 = 2$ MHz, $SIL = 1$ V/ μ A, and $V_{sat} = \pm 10$ V in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine wave input with peak ampitude V_p .

(a) If $V_p = 0.5$ V, what is the maximum frequency before the output clips?

(b) If $V_p = 20$ mV, what is the maximum value of V_p before the output clips?

(c) If $V_p = 50$ mV, what is the total frequency range of operation?

(d) If $V_p = 2$ μ A, what is the peak input voltage?

SECTION 2.7: DC IMPERFECTIONS

2.100 An op amp wired in the inverting configuration, with the input grounded, having $R_1 = 100 \text{ k}\Omega$ and $R_2 = 1 \text{ k}\Omega$, has a supply voltage of ± 12 V. If the input bias current is known to be very small, find the input offset voltage.

2.101 A noninverting op amp that with a gain of 200 uses an op-amp offset input offset voltage of ± 2 mV. Find the output, when the input is 0.01 sin ωt volts.

2.102 A noninverting op amp with a closed-loop gain of 2000 is designed using an op amp having an input offset voltage of ± 2 mV and output saturation levels of ± 12 V. What is the maximum amplitude of the sine wave that can be applied to the input without the output clipping? If the amplifier is connected as shown in the manner indicated in Fig. 2.46, what would the negative input positive amplitude be?

2.103 An op amp connected in a closed-loop inverting configuration having a gain of 1000 V/V and using ± 15 -V rail-to-rail output resistors is connected with a input grounded to have a dc output voltage of -1.4 V. What is its input offset voltage? Prepare an offset-voltage source sketch resembling that in Fig. 2.28. Be careful of polarities.

2.104 A particular inverting amplifier with nominal gain of -100 V/V uses an imperfect op amp in conjunction with $100 \text{ }\mu\text{A}$ and $100 \text{ }\mu\text{A}$ resistors. The current voltage is found to be -9.31 V when connected with the ideal op-amp -9.06 V with the input grounded.

(a) What is the bias current of this amplifier? Is it what one would expect?

(b) Evaluate the value of the input offset voltage.

(c) A $10-\text{M}\Omega$ resistor is connected between the positive-input terminal and ground. With the input left floating (disconnected), the output voltage is measured to be -0.8 V. Determine the input offset current.

2.105 A noninverting op amp with a gain of 100 V/V using $100 \text{ }\mu\text{A}$ as the feedback resistor operates from ± 5 -V rails. For an amplifier offset voltage of 0 mV, but with a

bias current of $1\text{ }\mu\text{A}$ and an offset current of $0.1\text{ }\mu\text{A}$, what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents. What does the range of possible currents then become? A designer wishes to use this amp after gain $\times 1000$.
source. In order to compensate for the bias current in this case, what resistor would you use? And why?

P2.106 The circuit of Fig. P2.106 is used to create an uncomplicated non-inverting amplifier with a gain of 200 V/V using resistors no larger than $100\text{ k}\Omega$. What values of R_1 , R_2 , and R_3 should be used? Due to feedback due to C_1 at 100 Hz , and that due to C_2 at 10 Hz , what values of C_1 and C_2 are needed?

***P2.107** Consider the difference amplifier circ'd in Fig. 2.16, but $R_1 = R_3 = 10\text{ k}\Omega$ and $R_2 = R_4 = 1\text{ M}\Omega$. If the op-amp has $V_{OS} = 4\text{ mV}$, $I_b = 0.5\text{ }\mu\text{A}$, and $I_{BO} = 50\text{ pA}$, find the worst-case (largest) dc offset voltage at the output.

***P2.108** The circuit shown in Fig. P2.108 uses an op-amp because $\pm 20\text{ mV}$ offset. What is the output offset V_O (dc)? What does the output offset become with the input dc supplied through a capacitor? If, instead, the $-10\text{k}\Omega$ resistor is capacitively coupled to ground, what does the output offset become?

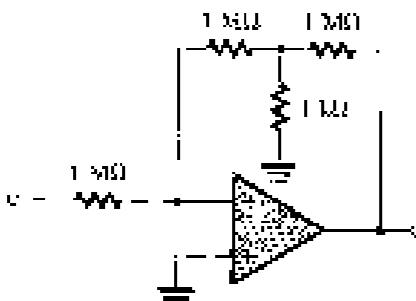


FIGURE P2.108

2.109 Using offset-nulling facilities provided for the op-amp, a closed-loop Miller with gain of $+1000$ is adjusted at 25°C to produce zero output with the input grounded. If the input offset voltage drift of the op-amp is specified to be $0.0\text{ }\mu\text{V}/^\circ\text{C}$, what output do you expect at 0°C and 75°C ? While nothing can be said separately about the polarity of the offset effect at either 0 or 75°C , what would you expect their relative polarities to be?

2.110 An op-amp is connected in a closed loop with gain $\times 100$ using a feedback resistor of $1\text{ M}\Omega$.

(a) If the bias current is $100\text{ }\mu\text{A}$, what output voltage results with the input grounded?

(b) If the input offset voltage is 1 mV and the input bias current is correct as in (a), what is the largest possible output that can be observed with the input grounded?

(c) If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting, exact offset voltage (plus an offset current of 0 pA)?

(d) With bias-current compensation as in (c) in place, what is the largest dc voltage at the output due to the combined effects of offset voltage and offset current?

***2.111** An op-amp is loaded the operation with a closed-loop gain of -10 V/V uses feedback resistors of $10\text{ k}\Omega$ and $1\text{ M}\Omega$ with a bias current compensation resistor R_3 . What should the value of R_3 be? With input grounded, the output dc voltage is found to be $+0.21\text{ V}$. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage can be as large as $\pm 1\text{ mV}$ of unknown polarity, what range of offset current is possible? What current is injected into, or extracted from, the negative node, and if R_3 would reduce the op-amp output voltage to zero? For two-level $\pm 1.5\text{ V}$ supplies, what resistor and supply voltage would you use?

SECTION 2.6: INTEGRATORS AND DIFFERENTIATORS

2.112 A Miller integrator incorporates an ideal op-amp, a resistor R of $10\text{ k}\Omega$ and a capacitor C of 10 nF . A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?

(b) At that frequency how does the phase of the output sine wave relate to that of the input?

(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?

(d) What is the phase relation between the input and output in this situation?

P2.113 Design a Miller integrator with a time constant of one second and an input resistance of $100\text{ k}\Omega$. For now assume $V_{OS} = 0$ with applied to the input at time 0 , at which moment $v_i = -1\text{ V}$. How long does it take the output to rise to 0.9994 V ?

2.114 An op-amp-based inverting integrator is measured at 1 kHz to have a voltage gain of -100 V/V . At what frequency is its gain reduced to -1 V/V ? What is the integrator time constant?

P2.115 Design a Miller integrator that has a unity-gain frequency of 1 rad/s and an input resistance of $100\text{ k}\Omega$. Sketch the output you would expect for the situation in which with input initially at 0 V , a 2-V , 2-ms pulse is applied to the input. Characterize the output. Just restate when a sine wave 2 V 1000 Hz is applied to the input?

P2.116 Design a Miller integrator whose input resistance is $20\text{ k}\Omega$ and unity-gain frequency is 10 kHz . What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor, which units (two digits) in dB. What is its value? What is the associated low- ω frequency? Sketch and label the output which results with (a) no dc stabilization but with the output initially at 0 V , and (b) the feedback resistor connected.

***2.117** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.117. Sketch and label the output waveform that results. Indicate what happens if the input levels are $\pm 2\text{ V}$, with the time constants the same (1 ms) but with the times increased, raised to 3 ms .

$v_i(\text{V})$

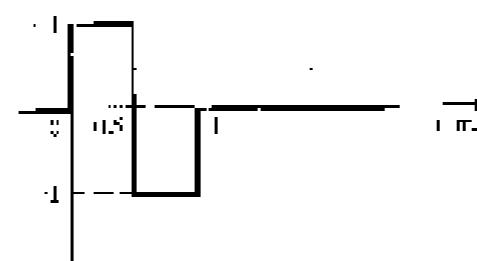


FIGURE P2.117

2.118 Consider an AT for integrator having a time constant of 1 ms , and whose capacitor is initially zero; when fed with a train of pulses of 10-ns duration and 1 V amplitude taken from 0 V (see Fig. P2.118). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V ?

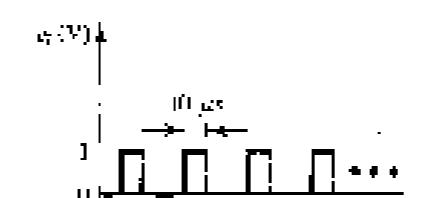


FIGURE P2.118

P2.119 Figure P2.119 shows a circuit that produces a low-pass Sinc function. Such a circuit is known as a first-order low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the half-power frequency

$\omega_0 = 1/(RC_1)$. Design the circuit to obtain an input resistance of $1\text{ M}\Omega$, a dc gain of 20 dB , and a 3-dB frequency of 1 kHz . At what frequency does the magnitude of the transfer function reduce to unity?

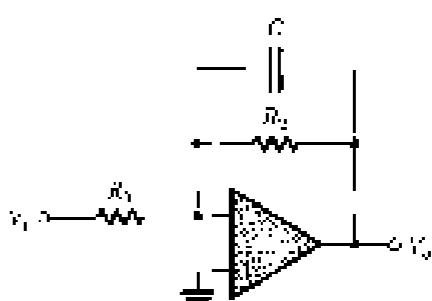


FIGURE P2.119

2.120 A Miller integrator with $R = 10\text{ k}\Omega$ and $C = 10\text{ nF}$ is implemented using an op-amp with $V_{OS} = 3\text{ mV}$, $I_b = 0.1\text{ }\mu\text{A}$, and $I_{BO} = 10\text{ nA}$. To provide a 20-dB gain, a $1\text{ M}\Omega$ resistor is connected across the capacitor.

(a) To compensate for the effect of I_b , a resistor is connected in series with the positive input terminal of the op-amp. What should its value be?

(b) With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

2.121 A differentiator utilizes an ideal op-amp, a $10\text{ k}\Omega$ resistor, and a 0.01-pF capacitor. What is the frequency at which its input and output sine wave signals have equal magnitude? What is the output signal for a 1 V peak-to-peak sine-wave input with frequency $\omega = 2\pi \times 10^3$?

2.122 An op-amp differentiator with 1 ms time constant is controlled by the rate-controlled sawtooth in Fig. P2.122. Assuming v_i to be zero initially, sketch and label v_o waveform.

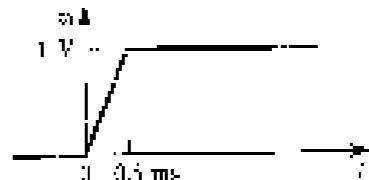


FIGURE P2.122

***2.123** An op-amp differentiator employing the circuit shown in Fig. 2.44(a), has $R = 10\text{ k}\Omega$ and $C = 0.1\text{ nF}$. When a triangle wave of 1-V peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of R is needed to force the output to have a 10-V peak amplitude? What is the 1-V rate-time when at 1 kHz is applied to

the original circuit, where output waveform is produced. What is its peak amplitude? Calculate this three ways: First, use the second formula in Fig. 2.1(b) directly; second, use the third formula in Fig. 2.1(b); third, use the maximum slopes of the input sine wave. In each case, establish a value for the peak output voltage and its duration.

2.124 Using an ideal op-amp, design a compensation circuit for which the time constant $\tau = 10^{-3}$ s, using a 10-pF capacitor. What are the corner and phase shift found for this circuit at zero-tail and 10-times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 10 V/V. What is the required 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

2.125 Figure P2.125 shows a circuit that performs the high-pass single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function, and show that the high-frequency gain is $(1 + R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/(C_1 R_1)$. Design the circuit to obtain a high-frequency input resistance of 10 k Ω , a high-frequency gain of 10 dB, and a 3-dB frequency of 100 Hz. At what frequency does the magnitude of the transfer function reduce to unity?



FIGURE P2.125

PROBLEM 2.126 Derive the transfer function of the circuit in Fig. P2.126 (for an ideal op-amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/\omega_0)^2][1 + j(\omega/\omega_0)]}$$

where $\omega_1 = 1/C_1 R_1$ and $\omega_0 = 1/C_2 R_2$. Assume ω_1 and the circuit is designed such that $\omega_2 > \omega_1$. Find approximate expressions for the transfer function in the following frequency regions:

- (a) $\omega \ll \omega_1$
- (b) $\omega_1 \ll \omega \ll \omega_2$
- (c) $\omega \gg \omega_2$

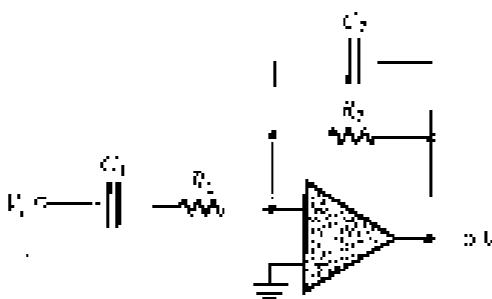


FIGURE P2.126

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain is flat at the low-frequency end, as the mirror of a high-pass SIC network, and at the high-frequency end as the inductor of a low-pass SIC network. Design the circuit to provide a gain of 40 dB in the "middle" frequency range, a low-frequency 3-dB point at 100 Hz, a high-frequency 3-dB point at 10 kHz, and an input resistance greater than or equal to 1 k Ω .

CHAPTER 3

Diodes

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INTRODUCTION

In the previous chapter we dealt almost entirely with linear circuit theory, nonlinearities such as that introduced by amplifier output saturation, were considered a problem to be solved by the circuit designer. However, there are many other signal processing functions that can be implemented only by nonlinear circuits. Examples include the generation of dc voltages from the ac power supply and the generation of signals of various waveforms (e.g., sinusoidal, square waves, pulses, etc.). Also, digital logic and memory circuits constitute a special class of nonlinear circuits.

The simplest and most fundamental nonlinear circuit element is the diode. Just like a resistor, the diode has two terminals but unlike the resistor, which has a linear (straight line) relationship between the current flowing through it and the voltage appearing across it, the diode has a nonlinear characteristic.

This chapter is concerned with the study of diodes. In order to understand the essence of the diode function, we begin with a fictitious element, the ideal diode. We then introduce the silicon junction diode, explain its terminal characteristics, and provide techniques for the analysis of diode circuits. The latter task involves the important subject of device modeling.

Our study of modeling the diode characteristics will lay the foundation for our study of modeling transistor operation in the next two chapters.

Of the many applications of diodes, their use in the design of rectifiers (which converts dc to dc) is the most common. Therefore we shall study rectifier circuits in some detail and briefly look at a number of other diode applications. Further advanced circuits that utilize diodes and other devices will be found throughout the book, but particularly in Chapter 13.

To understand the origin of the diode nonlinear characteristics, we can consider its physical operation. Our study of the physical operation of the pn junction and the basic concepts of semiconductor physics is intended to provide a foundation for understanding not only the characteristics of junction diodes but also those of the field-effect transistors, studied in the next chapter, and the bipolar junction transistor, studied in Chapter 5.

Although most of this chapter is concerned with the study of silicon pn-junction diodes, we briefly consider some specialized diode types, including the photodiode and the light-emitting diode. The chapter concludes with a description of the diode model utilized in the SPICE circuit-simulation program. We also present a design example that illustrates the use of SPICE simulation.

3.1 THE IDEAL DIODE

3.1.1 Current-Voltage Characteristic

The ideal diode may be considered the most familiar nonlinear circuit element. It is a two-terminal device having the circuit symbol of Fig. 3.1(a) and the *i*-*v* characteristic shown in Fig. 3.1(b). The terminal characteristic of the ideal diode can be interpreted as follows. If a

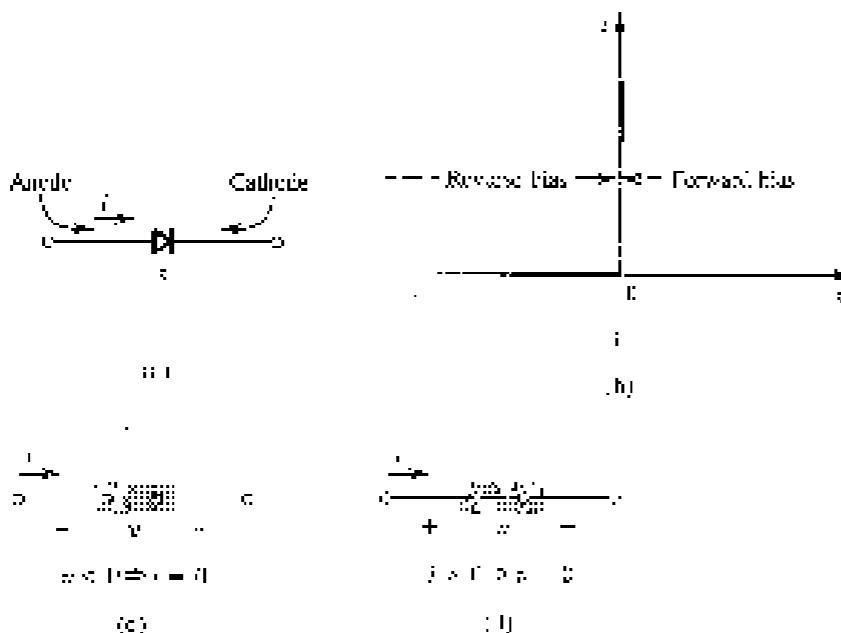


FIGURE 3.1 The ideal diode: (a) diode circuit symbol; (b) *i*-*v* characteristic; (c) equivalent circuit — the reverse direction; (d) equivalent circuit — the forward direction.

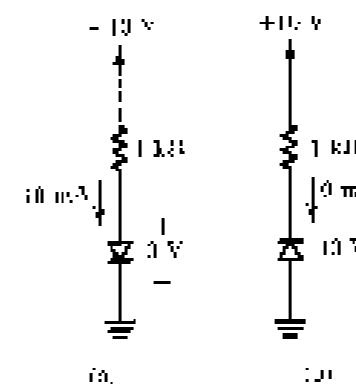


FIGURE 3.2 The two equivalent circuits of a diode: (a) reverse bias; (b) forward bias.

negative voltage (relative to the reference direction indicated in Fig. 3.1b) is applied to the diode, no current flows and the diode behaves as an open circuit (Fig. 3.1c). Diodes operated in this mode are said to be reverse biased, or operated in the reverse direction. An ideal diode has zero current when operated in the reverse direction and is said to be cut off, or simply off.

On the other hand, if a positive current (relative to the reference direction indicated in Fig. 3.1b) is applied to the ideal diode, zero voltage drop appears across the diode. In other words, the ideal diode behaves as a short circuit in the forward direction (Fig. 3.1d); it passes any current with zero voltage drop. A forward-biased diode is said to be turned on, or simply on.

From the above description it should be noted that the external circuit must be designed to limit the forward current through a conducting diode, and the reverse voltage across a cutoff diode, to predetermined values. Figure 3.2 shows two diode circuits that illustrate this point. In the circuit of Fig. 3.2(a) the diode is obviously conducting. Thus its voltage drop will be zero, and the current through it will be determined by the +10-V supply and the 1-kΩ resistor to 10 mA. The diode in the circuit of Fig. 3.2(b) is obviously cut off, and thus its current will be zero, which in turn means that the entire 10-V supply will appear as reverse bias across the diode.

The positive terminal of the diode is called the anode and the negative terminal the cathode, a carryover from the days of vacuum tube diodes. The *i*-*v* characteristic of the ideal diode (conducting in one direction and cut off in the other) should explain the choice of its arrow-like circuit symbol.

As should be evident from the preceding description, the *i*-*v* characteristic of the ideal diode is highly nonlinear; although it consists of two straight-line segments, they are ... so to one another. A nonlinear curve that consists of straight-line segments is said to be piecewise linear. If a device having a piecewise-linear characteristic is used in a particular application in such a way that the signal across its terminals swings along only one of the linear segments, then the device can be considered a linear circuit element as far as that particular circuit application is concerned. On the other hand, if signals swing past one of those break points in the characteristic, linear analysis is no longer possible.

3.1.2 A Simple Application: The Rectifier

A fundamental application of the diode, one that makes use of its severely nonlinear *i*-*v* curve, is the rectifier circuit shown in Fig. 3.3(a). The circuit consists of the series connection

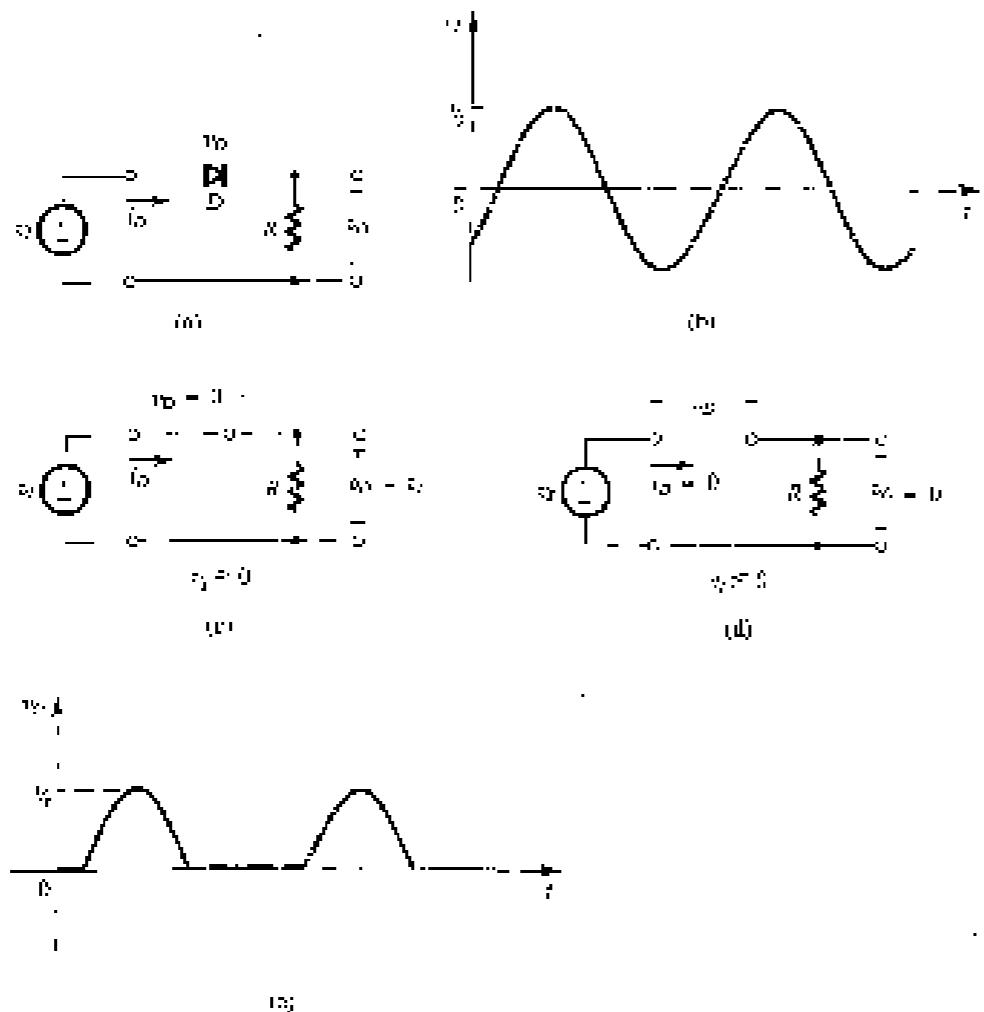


FIGURE 3.3 (a) Rectifier circuit. (b) Input waveform. (c) Equivalent circuit when $v_i > 0$. (d) Equivalent circuit when $v_i < 0$. (e) Output wave. [3.3]

at a diode \$D\$ and a resistor \$R\$. Let the input voltage \$v_i\$ be the sinusoid shown in Fig. 3.3(b), and assume the diode to be ideal. During the positive half-cycles of the input sinusoid, the positive \$v_i\$ will cause current to flow through the diode in its forward direction. It follows that the diode voltage \$v_D\$ will be very small—ideally zero. Thus the circuit will have the equivalent circuit shown in Fig. 3.3(c), and the output voltage \$v_o\$ will be equal to the input voltage \$v_i\$. On the other hand, during the negative half-cycles of \$v_i\$, the diode will not conduct. Thus the circuit will have the equivalent shown in Fig. 3.3(d), and \$v_O\$ will be zero. Thus the output voltage will have the waveform shown in Fig. 3.3(e). Note that while \$v_O\$ never reaches a polarity and has a zero average value, \$v_O\$ is unidirectional and has a finite average value or a dc component. Thus the circuit of Fig. 3.3(a) rectifies the signal and hence is called a rectifier. It can be used to generate dc from ac. We will study rectifier circuits in Section 3.5.

EXERCISES

1. For the circuit in Fig. 3.3, sketch the waveform of \$v_o\$.
2. For the circuit in Fig. 3.3, sketch the waveform of \$v_D\$.
3. In the circuit of Fig. 3.3, let \$v_i\$ have a peak value of \$10\text{ V}\$ and \$R = 1\text{ k}\Omega\$. Calculate the peak value of \$v_o\$.
4. In the circuit of Fig. 3.3, let \$v_i\$ have a peak value of \$10\text{ V}\$ and \$R = 1\text{ k}\Omega\$. Calculate the fraction of each cycle during which the diode conducts.
5. In the circuit of Fig. 3.3, let \$v_i\$ have a peak value of \$10\text{ V}\$ and \$R = 1\text{ k}\Omega\$. Calculate the maximum reverse-bias voltage that appears across the diode.

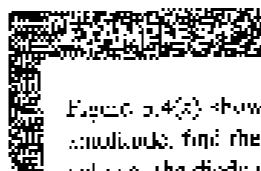


Figure 3.4(a) shows a circuit for charging a \$12\text{-V}\$ battery. Let \$v_i\$ be a sinusoid with \$21\text{-V}\$ peak amplitude. Find the fraction of each cycle during which the diode conducts. Also, find the peak value of the diode current and the maximum reverse-bias voltage that appears across the diode.

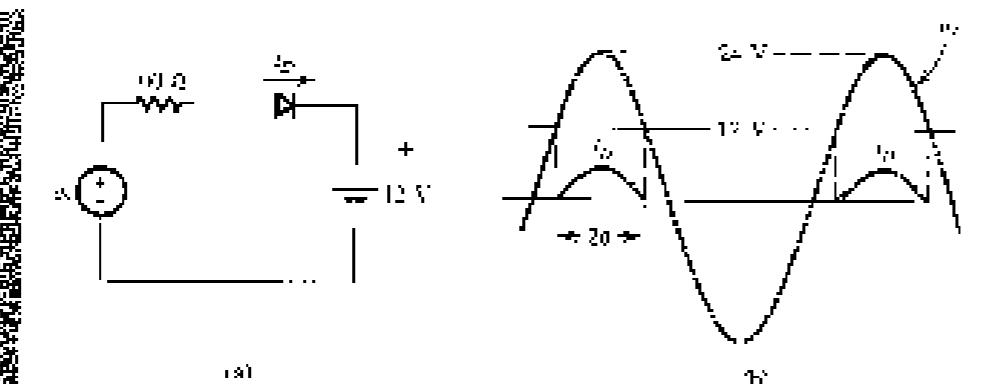


FIGURE 3.4 Circuit and waveform for Example 3.1.

Solution

The diode conducts when v_o exceeds 12 V, as shown in Fig. 3.4(b). The conduction angle is 2θ , where θ is given by

$$24 \cos \theta = 12$$

Thus $\theta = 60^\circ$ and the conduction angle is 120° , or one-third of a cycle.

The peak value of the diode current is given by

$$I_{D\text{pk}} = \frac{24 - 12}{100} = 0.12 \text{ A}$$

The maximum reverse voltage across the diode occurs when v_o is at its negative peak and is equal to $24 + 12 = 36 \text{ V}$.

3.1.3 Another Application: Diode Logic Gates

Diodes together with resistors can be used to implement digital logic functions. Figure 3.5 shows two diode logic gates. To see how these circuits function, consider a positive-logic system in which voltage values closest to 0 V correspond to logic 0 (or low) and voltage values

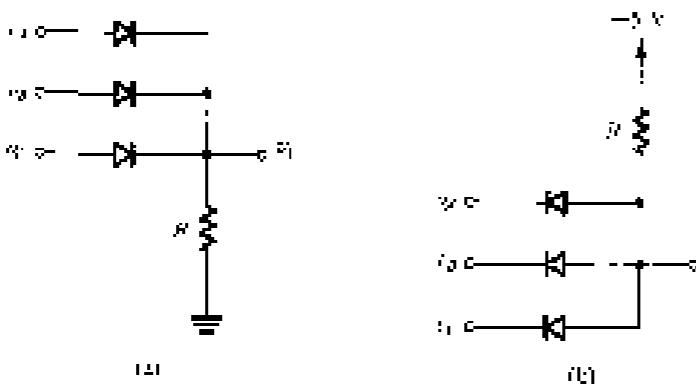


FIGURE 3.5 Diode logic gates: (a) OR gate; (b) AND gate (in a positive-logic system).

close to 15 V correspond to logic 1 (or high). The circuit in Fig. 3.5(a) has three inputs, v_1 , v_2 , and v_3 . It is easy to see that diodes connected to 15-V inputs will conduct, thus clamping the output v_o to a value equal to -5 V . This positive voltage at the output will keep the diodes whose inputs are low (around 0 V) cut off. Thus the output will be high if one or more of the inputs are high. The circuit therefore implements the logic OR function, which in Boolean notation is expressed as

$$Y = A + B + C$$

Similarly, the reader is encouraged to show that, using the same logic system mentioned above, the circuit of Fig. 3.5(b) implements the logic AND function,

$$Y = A \cdot B \cdot C$$

Assuming the diodes to be ideal, find the values of I and V in the circuits of Fig. 3.6.

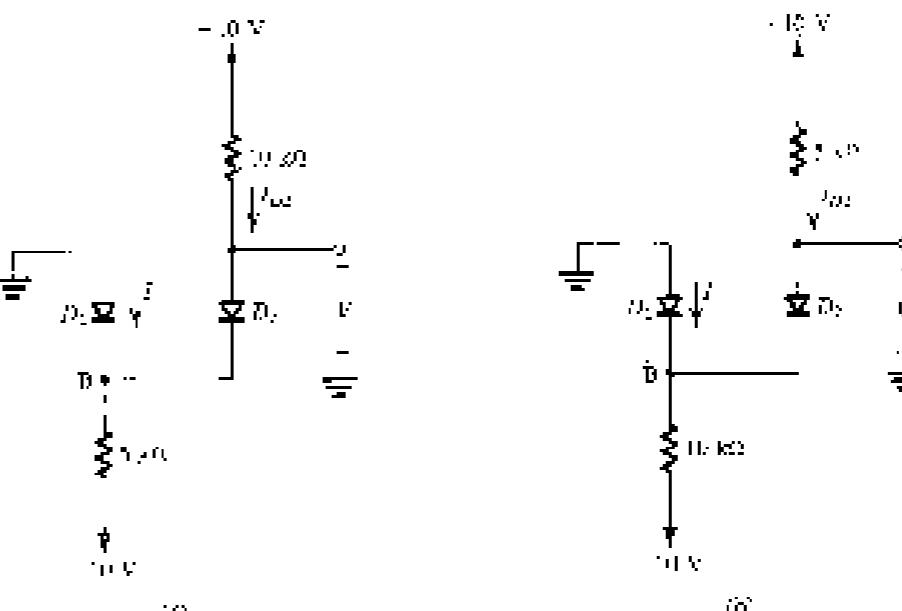


FIGURE 3.6 Circuits for Example 3.2.

Solution

In these circuits, it might not be obvious at first sight whether one, two, or both diodes are conducting. To tackle a case, we make a plausible assumption, proceed with the analysis, and then check our answer and go with a confirmed solution. For the circuit in Fig. 3.6(a), we shall assume that both diodes are conducting. It follows that $v_o = 0 \text{ mV} \approx 0$. The current through D_2 can now be determined from

$$I_{D2} = \frac{10 - 0}{10} = 1 \text{ mA}$$

Writing a node equation at B,

$$I - 1 = \frac{V - (-10)}{5}$$

Results in $I = 1$ mA. Thus D_1 is conducting as originally assumed, and the final result is $I = 1$ mA and $V = 3$ V.

For the circuit in Fig. 3.6(b), if we assume that both diodes are conducting, then $V_S = 0$ and $V = 0$. The current in D_2 is obtained from

$$I_{D_2} = \frac{10 - 0}{5} = 2 \text{ mA}$$

The voltage across R is

$$V - 2 = \frac{0 - 10}{20}$$

which yields $I = -1$ mA. Since this is not possible, nothing is wrong and our assumption is not correct. We start again, assuming that D_1 is off and D_2 is on. The current I_{D_2} is given by

$$I_{D_2} = \frac{10 - (-10)}{15} = 1.33 \text{ mA}$$

and the voltage across R is

$$V_S = -10 + 10 \times 1.33 = +3.3 \text{ V}$$

Thus D_1 is reverse biased as assumed, and the final result is $I = 0$ and $V = 3.3$ V.

EXERCISES

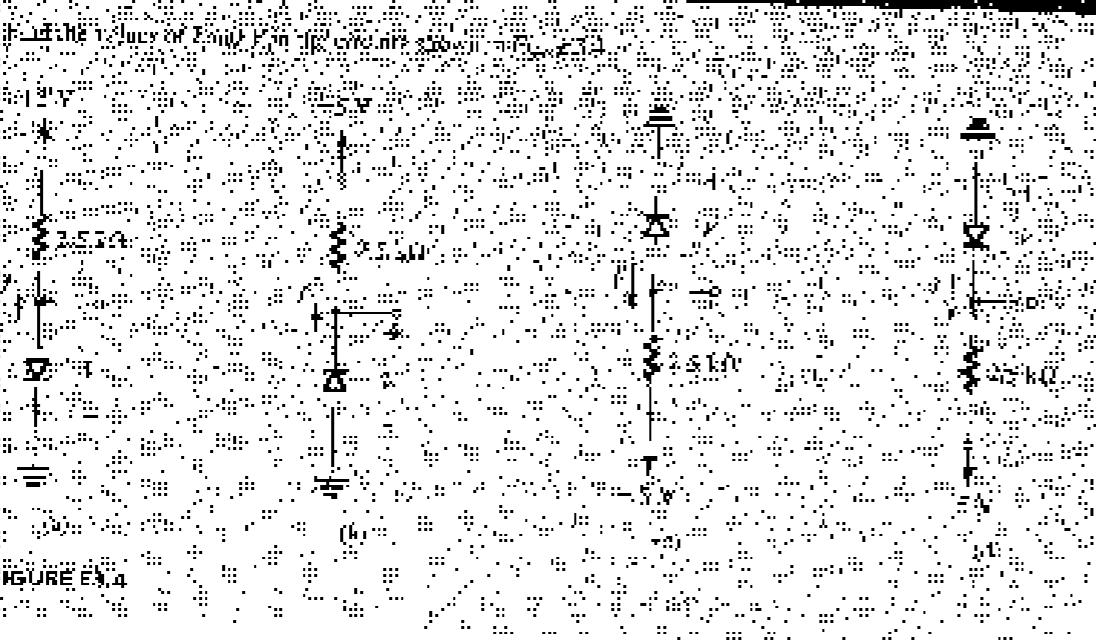


FIGURE E3.4

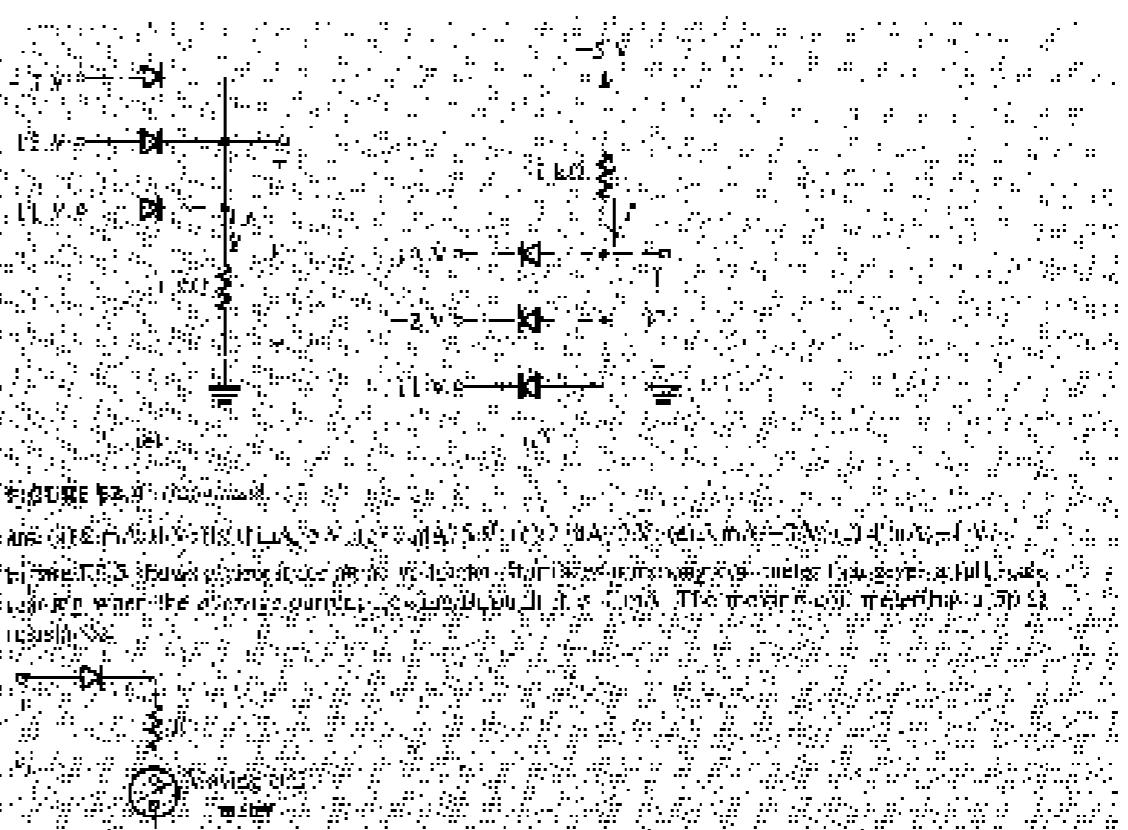


FIGURE E3.5

Find the value of R required in the rectifier circuit of Exercise E3.4, when the input voltage is 120 V peak-to-peak. Neglect the voltage drop of the zener diode.

3.2 TERMINAL CHARACTERISTICS OF JUNCTION DIODES

In this section we study the characteristic of real diodes, specifically, semiconducting junction diodes made of silicon. The physical processes that give rise to the diode terminal characteristics, and to the name "junction diode," will be studied in Section 3.7.

Figure 3.7 shows the $i-v$ characteristic of a silicon junction diode. The same characteristics are shown in Fig. 3.8 with some scales expanded and others compressed to reveal details. Note that the scale changes have been kept in the apparent discontinuity of the origin.

As indicated, the characteristic curve consists of three distinct regions:

1. The forward-bias region, determined by $v > 0$
2. The reverse-bias region, determined by $v < 0$
3. The breakdown region, determined by $v < -V_{BR}$

These three regions of operation are described in the following sections.

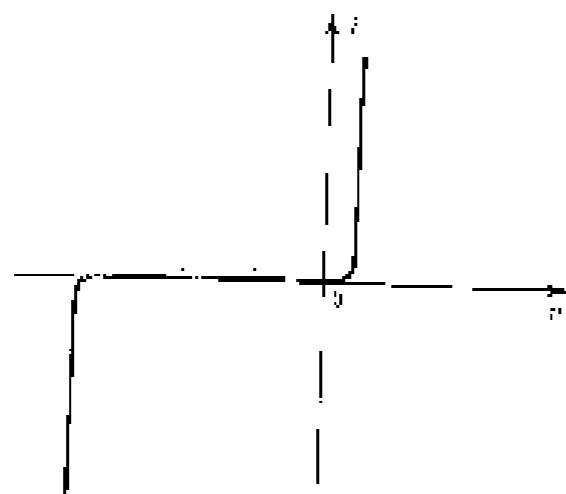


FIGURE 3.7 The voltage-current characteristic of a junction diode.

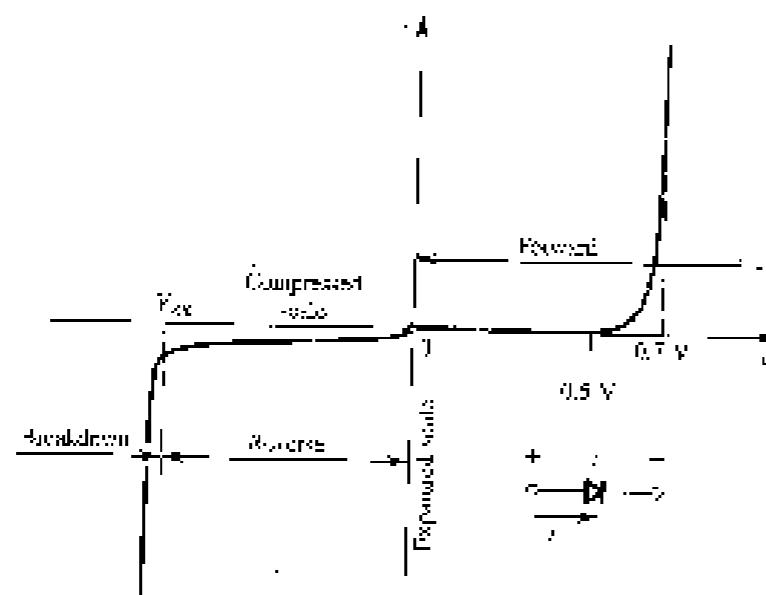


FIGURE 3.8 The diode characteristic with some values expanded and others compressed in a log-log plot.

3.2.1 The Forward-Bias Region

The forward-bias—or simply forward—region of operation is defined when the terminal voltage V is positive. In the forward region the i - V relationship is closely approximated by

$$i = I_S e^{V/V_T} \quad (3.1)$$

In this equation I_S is a constant for a given diode at a given temperature. A formula for I_S in terms of the diode's physical parameters and temperature will be given in Section 3.7. The current I_S is usually called the saturation current (for reasons that will become apparent shortly). Another name for I_S , and one that we will occasionally use, is the scale current. This name arises from the fact that I_S is directly proportional to the cross-sectional area of the diode. Thus doubling of the junction area results in a diode with double the value of I_S , and, as the diode equation indicates, double the value of current i for a given forward voltage V . For "small-signal" diodes, which are semiconductors intended for low-power applications, I_S is on the order of 10^{-15} A. The value of I_S is, however, a very strong function of temperature. As a rule of thumb, I_S doubles its value for every 5°C rise in temperature.

The voltage V_T in Eq. (3.1) is a constant called the thermal voltage and is given by

$$V_T = \frac{kT}{q} \quad (3.2)$$

where

k = Boltzmann's constant = 1.38×10^{-23} joule/degree kelvin

T = the absolute temperature in kelvins = $273 + \text{temperature in } ^\circ\text{C}$

q = the magnitude of electronic charge = 1.60×10^{-19} coulombs

At room temperature (20°C) the value of V_T is 25.8 mV. In rapid approximate circuit analysis we shall use $V_T = 25$ mV at room temperature.¹

In the diode equation the constant n has a value between 1 and 2, depending on the material and the physical structure of the diode. Diodes made using the standard integrated-circuit fabrication process exhibit $n = 1$ when operated under normal conditions.² Diodes available as discrete two-terminal components generally exhibit $n = 2$. In general, we shall assume $n = 1$ unless otherwise specified.

For appreciable current i in the forward direction, specifically for $i > I_S$, Eq. (3.1) can be approximated by the exponential relationship

$$i = I_S e^{V/V_T} \quad (3.3)$$

This relationship can be expressed alternatively in the logarithmic form

$$\sigma = \partial V_T / \partial \ln i \quad (3.4)$$

where \ln denotes the natural (base e) logarithm.

The exponential relationship of the current i to the voltage V holds over many decades of current (as span of as many as seven decades—that is, a factor of 10^7) can be found. This is quite a remarkable property of junction diodes, one that is also found in bipolar junction transistors and that has been exploited in many interesting applications.

Let us consider the forward i - V relationship in Eq. (3.3) and evaluate the current i , corresponding to a diode voltage V_F .

$$i = I_S e^{V_F/V_T}$$

¹ At slightly higher ambient temperatures (25°C or so) it is usually assumed, for electronic equipment operating within a cabinet, that this temperature, T , is 25.8 mV. Never, unless for these extreme simplicity and convenience purposes, would one use the more mathematically correct value of $V_T = 25$ mV throughout this book.

² In fact, commercial diodes are usually obtained by connecting a bipolar junction transistor ($h_{FE} > 1$) as a two-terminal device, as will be seen in Chapter 5.

Similarly, if the voltage is V_2 , the diode current I_2 will be

$$I_2 = I_1 e^{\frac{V_2 - V_1}{nV_T}}$$

These two equations can be combined to produce

$$\frac{I_2}{I_1} = e^{\frac{n(V_2 - V_1)}{V_T}}$$

which can be rewritten as

$$V_2 - V_1 = nV_T \ln \frac{I_2}{I_1}$$

or, in terms of base-10 logarithms,

$$V_2 - V_1 = 2.3nV_T \log \frac{I_2}{I_1} \quad (3.5)$$

This equation simply states that for a decade (factor of 10) change in current, the diode voltage drop changes by $2.3nV_T$, which is approximately 61 mV for $n = 1$ and 120 mV for $n = 2$. This also suggests that the diode $i-v$ relationship is more conveniently plotted on semilog paper. Using the vertical, linear axis for v and the horizontal, log axis for i , one obtains a straight line with a slope of 2.3 mV per decade of current. Finally, it should be mentioned that not knowing the exact value of n (which can be obtained from a simple experiment), circuit designers use the convenient approximate number of 0.1 V/decade for the slope of the diode logarithmic characteristic.

A glance at the $i-v$ characteristic in the forward region (Fig. 3.8) reveals that the current is negligibly small for v smaller than about 0.5 V. This value is usually referred to as the **cut-in voltage**. It should be emphasized, however, that this apparent threshold in the characteristic is simply a consequence of the exponential relationship. Another consequence of this relationship is the rapid increase of i . Thus, for a "fully conducting" diode, the voltage drop lies in a narrow range, approximately 0.5 V or 0.7 V. This gives rise to a simple "model" for the diode where it is assumed that a conducting diode has approximately a 0.7-V drop across it. Diodes with different current ratings (i.e., different areas and corresponding I_s) will exhibit the 0.7-V drop at different currents. For instance, a small-signal diode may be considered to have a 0.7-V drop at $i = 1 \text{ mA}$, while a higher-power diode may have a 0.7 V drop at $i = 1 \text{ A}$. We will study the topics of diode circuit analysis and diode models in the next section.

PROBLEM 3.5
A silicon diode with 1 mA current displays a forward voltage of 0.7 V at a current of 1 mA. Evaluate the junction scaling constant I_s at the event that n is either 1 or 2. What scaling curve would apply for a 1-A diode of the same manufacture that conducts 1 A at 0.7 V?

Solution

Since

$$i = I_s e^{\frac{v}{nV_T}}$$

then

$$I_s = i e^{-\frac{v}{nV_T}}$$

For the 1-mA diode

$$10^{-3} = 1 e^{-\frac{0.7}{n(290)}} \cdot 6.9 \times 10^{-16} \text{ A}, \text{ or about } 10^{-15} \text{ A}$$

$$10^{-3} = 1 e^{-\frac{0.7}{n(290)}} \cdot 8.3 \times 10^{-15} \text{ A}, \text{ or about } 10^{-14} \text{ A}$$

The diode conducting 1 A at 0.7 V corresponds to one thousand 1-mA diodes in parallel with a total junction area 1000 times greater. That I_s is also 1000 times greater, using 1 μA and 1 μA , respectively for $n = 1$ and $n = 2$.

From this example it should be apparent that the value of n used can be quite important.

Since both I_s and V_T are functions of temperature, the forward $i-v$ characteristic varies with temperature, as illustrated in Fig. 3.9. At a given constant diode current the voltage drop across the diode decreases by approximately 2 mV for every 1°C increase in temperature. The change in diode voltage with temperature has been exploited in the design of electronic thermometers.

PROBLEMS

- 3.6 Consider a diode with $n = 1.7$. Plot the characteristic curves for the temperatures 100°C, 200°C, and 300°C.
- 3.7 A silicon junction diode is at 25°C with a reverse current of 0.1 nA and a forward current of 10 mA.
- 3.8 Using the forward voltage drop as a function of temperature, find the value of I_s at 100°C.
- 3.9 Using the forward voltage drop as a function of temperature, find the value of I_s at 200°C.

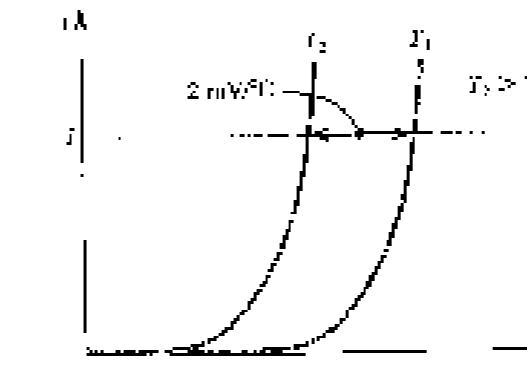


FIGURE 3.9 Illustrating the temperature dependence of the diode forward characteristic. At a given current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature.

3.2.2 The Reverse-Bias Region

The reverse-bias region of operation is entered when the diode voltage V_D is made negative. Equation (3.1) predicts that if V_D is negative and a few times larger than $k_T(25 \text{ mV})$, or negative, the exponential term becomes negligibly small compared to unity, and the diode current becomes

$$I_D = -I_0$$

That is, the current in the reverse direction is constant and equal to I_0 . This constancy is the reason behind the term *constant-current diode*.

Real diodes exhibit reverse currents that are much larger than I_0 , for instance, a small-signal diode whose I_0 is on the order of 10^{-11} A at 10^{-12} V could show a reverse current of the order of 1 nA. The reverse current also increases somewhat with the increase in magnitude of the reverse voltage. Note that because of the very small magnitude of the current, these details are not clearly evident on the diode $i-v$ characteristic of Fig. 3.8.

A large part of the reverse current is due to leakage effects. These leakage currents are proportional to the junction area, just as I_0 is. Their dependence on temperature, however, is different from that of I_0 . Thus, whereas I_0 doubles for every 5°C rise in temperature, the corresponding rule of thumb for the temperature dependence of the reverse current is that it doubles for every 10°C rise in temperature.

EXERCISE

3.6. A diode in the breakdown region has a reverse current of 10^{-10} A at -10 V . If the reverse current increases exponentially with voltage, what is the breakdown voltage?

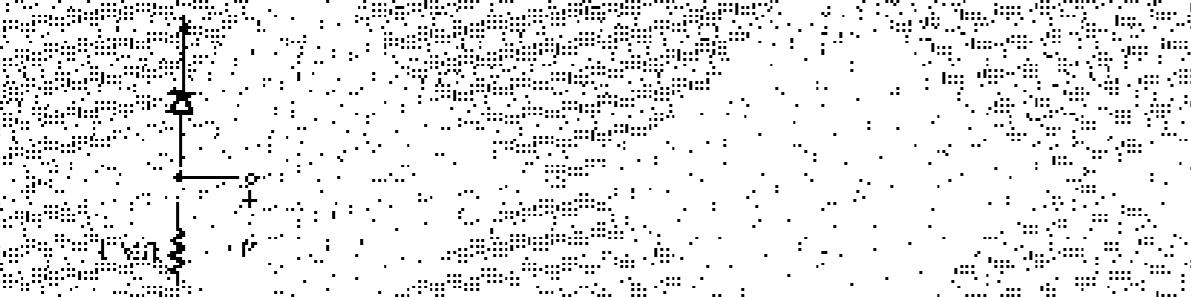


FIGURE 3.8 Diode $i-v$ characteristic. The exponential nature of the diode current is evident in the graph. The reverse current is constant for small negative voltages but increases exponentially as the reverse voltage increases.

3.2.3 The Breakdown Region

The third distinct region of diode operation is the breakdown region, which can be easily identified on the diode $i-v$ characteristic in Fig. 3.8. The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the breakdown voltage. This is the voltage at the "knee" of the $i-v$ curve in

Fig. 3.8 and is denoted V_{BR} , where the subscript B stands for *breakdown* (shortly, and K denotes knee).

As can be seen from Fig. 3.8, in the breakdown region the reverse current increases rapidly, with the associated increase in voltage being very small. Diode breakdown is normally not cumulative provided that the power dissipated in the diode is limited by external circuitry to a "safe" level. This safe value is normally specified on the device data sheets. It is therefore necessary to limit the reverse current in the breakdown region to a value commensurate with the permissible power dissipation.

The fact that the diode $i-v$ characteristic in breakdown is almost a vertical line is key to its use in voltage regulation. This subject will be studied in Section 7.5.

3.3 MODELING THE DIODE FORWARD CHARACTERISTIC

Having studied the diode terminal characteristics we are now ready to consider the analysis of circuits employing forward-conducting diodes. Figure 3.10 shows such a circuit. It consists of a dc source V_{DD} , a resistor R , and a diode. We wish to analyze this circuit to determine the diode voltage V_D and current I_D . Toward this end we consider developing a variety of models for the operation of the diode. We already know of two such models: the ideal-diode model and the exponential model. In the following discussion we shall assess the suitability of these two models in various analysis situations. Also, we shall develop an account of a number of other models. This material, besides being useful in the analysis and design of diode circuits, establishes a foundation for the modeling of transistor operation that we will study in the next two chapters.

3.3.1 The Exponential Model

The most accurate description of the diode operation in the forward region is provided by the exponential model. Unfortuneately, however, its severely nonlinear nature makes this model far most difficult to use. To illustrate, let's analyze the circuit in Fig. 3.10 using the exponential diode model.

Assuming that V_{DD} is greater than 0.5 V or so, the diode current will be much greater than I_0 , and we can represent the diode $i-v$ characteristic by the exponential relationship, resulting in

$$I_D = I_0 e^{V_D/V_T} \quad (3.6)$$

The other equation that governs circuit operation is obtained by writing a Kirchhoff loop equation, resulting in

$$I_D = \frac{V_{DD} - V_D}{R} \quad (3.7)$$

Assuming that the diode parameters I_0 and V_T are known, Eqs. (3.6) and (3.7) are two equations in the two unknown quantities I_D and V_D . Two alternate ways for obtaining the solution are graphical analysis and iterative analysis.

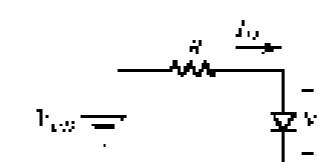


FIGURE 3.10 A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting.

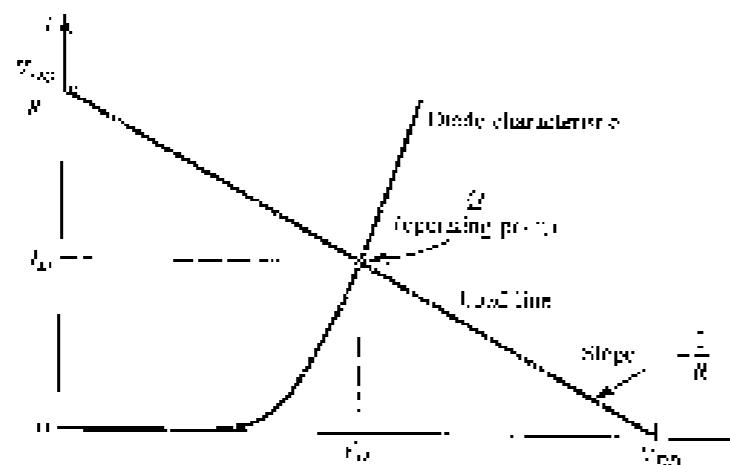


FIGURE 3.11 Graphical analysis of the circuit in Fig. 3.10 using the exponential diode model.

3.3.2 Graphical Analysis Using the Exponential Model

Graphical analysis is performed by plotting the relationships of Eqs. (3.6) and (3.7) on the i - v plane. The solution can thus be obtained as the coordinates of the point of intersection of the two graphs. A sketch of the graphical construction is shown in Fig. 3.11. The curve represents the exponential diode equation (Eq. 3.6), and the straight line represents Eq. (3.7). Such a straight line is known as the load line, a name that will become more meaningful in later chapters. The load line intersects the diode curve at point Q , which represents the operating point of the circuit. Its coordinates give the values of I_A and V_A .

Graphical analysis aids in the visualization of circuit operation. However, the effort involved in performing such an analysis, particularly in complex circuits, is too great to be justified in practice.

3.3.3 Iterative Analysis Using the Exponential Model

Equations (3.6) and (3.7) can be solved using a simple iterative procedure, as illustrated in the following example.

Example 3.10 Determine the current I_A and the node voltage V_A for the circuit in Fig. 3.10 with $V_{DD} = 5\text{ V}$ and $R = 1\text{ k}\Omega$. Assume IDE the diode has a current of 1 mA at a voltage of 0.7 V and that its voltage drops changes by 0.1 V for every decade change in current.

Solution

To begin the iteration, we assume that $V_A = 0.7\text{ V}$ and use Eq. (3.7) to determine the current:

$$I_A = \frac{V_{DD} - V_A}{R}$$

$$= \frac{5 - 0.7}{1} = 4.3\text{ mA}$$

3.3.4 Modeling the Diode Forward Characteristic

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We can use the diode equation to obtain a better estimate for V_A . This can be done by employing $I_2 \neq 0$, namely,

$$V_2 - V_1 = 2.3kT_2 \ln \left(\frac{I_2}{I_1} \right)$$

For our case, $2.3kT = 0.1\text{ V}$. Thus,

$$V_2 = V_1 + 0.1 \ln \left(\frac{I_2}{I_1} \right)$$

Substituting $V_1 = 0.7\text{ V}$, $I_1 = 1\text{ mA}$, and $I_2 = 4.3\text{ mA}$ results in $V_2 = 0.792\text{ V}$. Thus the results of the first iteration are $I_2 = 4.3\text{ mA}$ and $V_2 = 0.792\text{ V}$. The second iteration proceeds in a similar manner:

$$I_3 = \frac{5 - 0.792}{1} = 4.207\text{ mA}$$

$$V_3 = (0.792 + 0.1 \ln \left[\frac{I_3}{I_2} \right])$$

$$\approx 0.792\text{ V}$$

Thus the second iteration yields $I_3 = 4.207\text{ mA}$ and $V_3 = 0.792\text{ V}$. Since these values are not much different from the values obtained after the first iteration, no further iterations are necessary and the solution is $I_A = 4.207\text{ mA}$ and $V_A = 0.792\text{ V}$.

3.3.4 The Need for Rapid Analysis

The iterative analysis procedure utilized in the example above is simple and yields accurate results after two or three iterations. Nevertheless, there are situations in which the effort and time required are still greater than can be justified. Specifically, if one is doing a hand-and-paper design of a relatively complex circuit, rapid circuit analysis is a necessity. Through quick analysis, the designer is able to evaluate various possibilities before deciding on a suitable circuit design. To speed up the analysis process one can be content with less precise results. This, however, is seldom a problem, because the more accurate analysis can be postponed until a final or almost final design is obtained. Accurate analysis of the almost-final design can be performed with the aid of a computer circuit-analysis program such as SPICE (see Section 3.10). The results of such an analysis can then be used to further refine ("tune") the design.

To speed up the analysis process, we must find simpler models for the diode forward characteristics.

3.3.5 The Piecewise-Linear Model

The analysis can be greatly simplified if we can find linear relationships to describe the diode forward characteristics. An attempt in this direction is illustrated in Fig. 3.12, where the exponential curve is approximated by two straight lines, Line A with zero slope and line B with a slope of $1/kT_0$. It can be seen that for the particular case shown in Fig. 3.12, over the current range of 0.1 mA to 10 mA , the voltages predicted by the straight-line model shown differ from those predicted by the exponential model by less than 20 mV . Obviously the choice of these two straight lines is not unique; one can obtain a closer approximation by restricting the current range over which the approximation is required.

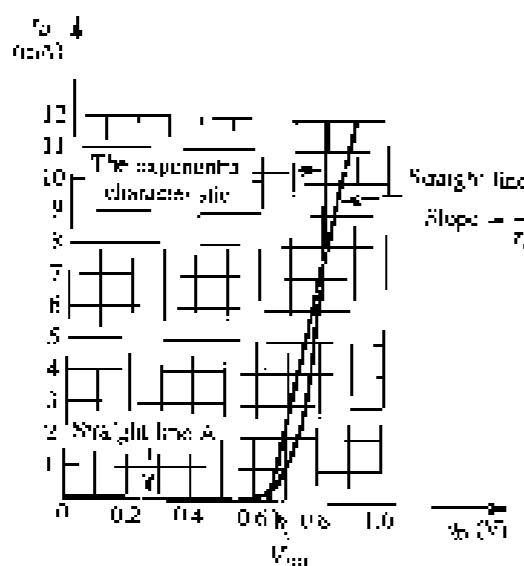


FIGURE 3.12 Approximating the diode forward characteristic with two straight lines—the piecewise-linear model.

The straight-line (or piecewise-linear) model of Fig. 3.12 can be described by

$$\begin{aligned} i_D &= 0, \quad v_D \leq V_{D0} \\ i_D &= (v_D - V_{D0})/r_D, \quad v_D > V_{D0} \end{aligned} \quad (3.8)$$

where V_{D0} is the intercept of line B on the voltage axis and r_D is the inverse of the slope of line B. For the particular example shown, $V_{D0} = 0.66$ V and $r_D = 20\Omega$.

The piecewise-linear model described by Eqs. (3.8) can be represented by the equivalent circuit shown in Fig. 3.13. Note that an ideal diode is included in this model to constrain i_D to flow in the forward direction only. This model is also known as the battery-plus-resistance model.

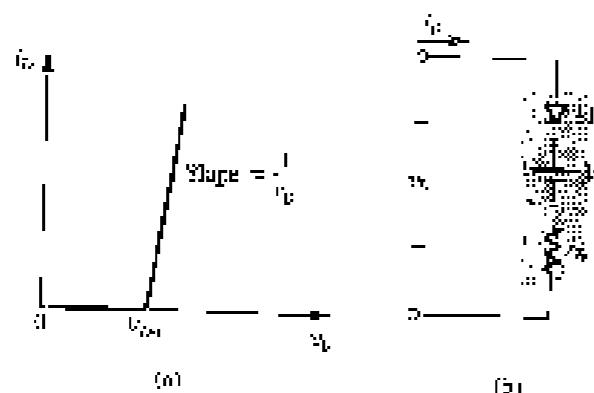


FIGURE 3.13 Piecewise-linear model of the diode forward characteristics and its equivalent circuit.

Repeat the problem in Example 3.4 utilizing the piecewise-linear model whose parameters are given in Fig. 3.12 ($V_{D0} = 0.66$ V, $r_D = 20\Omega$). Note that the characteristics depicted in this figure are those of the diode described in Example 3.4 (1 mA at 0.7 V and 0.1 V decade).

Solution

Replacing the diode in the circuit of Fig. 3.10 with the equivalent circuit model of Fig. 3.13 results in the circuit in Fig. 3.14, from which we can write for the current i_D ,

$$i_D = \frac{V_{DD} - V_D}{R + r_D}$$

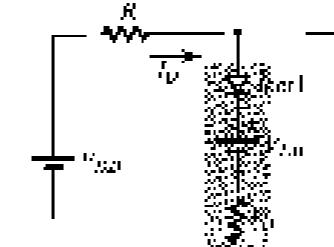


FIGURE 3.14 Equivalent of Fig. 3.10 with the diode replaced with the piecewise-linear model of Fig. 3.13.

where the model parameters V_{D0} and r_D are seen from Fig. 3.12 to be $V_{D0} = 0.66$ V and $r_D = 20\Omega$. Thus,

$$i_D = \frac{5 - 0.66}{1 + 0.02} = 4.26 \text{ mA}$$

The diode voltage V_D can now be computed:

$$\begin{aligned} V_D &= V_{DD} + i_D r_D \\ &= 5.00 + 4.26 \times 0.02 = 0.23 \text{ V} \end{aligned}$$

3.3.6 The Constant-Voltage-Drop Model

An even simpler model of the diode forward characteristics can be obtained if we use a vertical straight line to approximate the tailoring part of the exponential curve, as shown in Fig. 3.15. The resulting model simply says that a forward-conducting diode exhibits a **constant voltage drop**, V_D . The value of V_D is usually taken to be 0.7 V. Note that for the particular diode whose characteristics are depicted in Fig. 3.15, this model predicts the diode voltage to within 10.1 V over the current range of 0.1 mA to 10 mA. The constant-voltage-drop model can be represented by the equivalent circuit shown in Fig. 3.16.

The constant-voltage-drop model is the one most frequently employed in the initial phases of analysis and design. This is especially true if at these stages one does not have detailed information about the circle characteristics, which is often the case.

Finally, note that if we employ the constant-voltage-drop model to solve the problem in Examples 3.4 and 3.5, we obtain

$$V_D = 0.7 \text{ V}$$

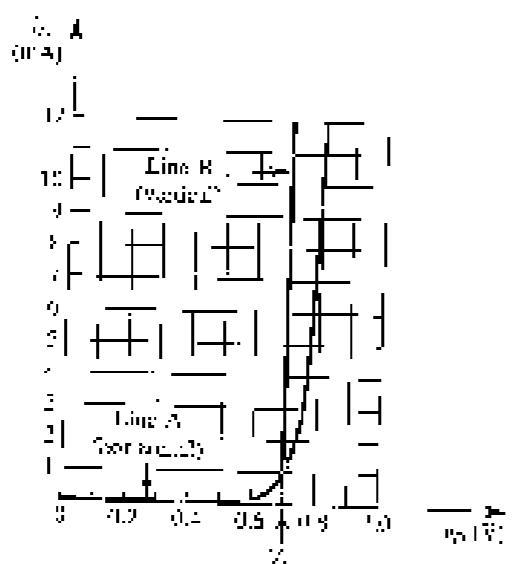


FIGURE 3.15 Development of the common voltage-loop mode of the Zener-Jordan-Hall test (14). A typical surge (line 10) is used to approach the resonance experimental. Observe that this surge mode voltage V_2 is within +1.1 V over the current range of $I = 2A$ to $10A$.

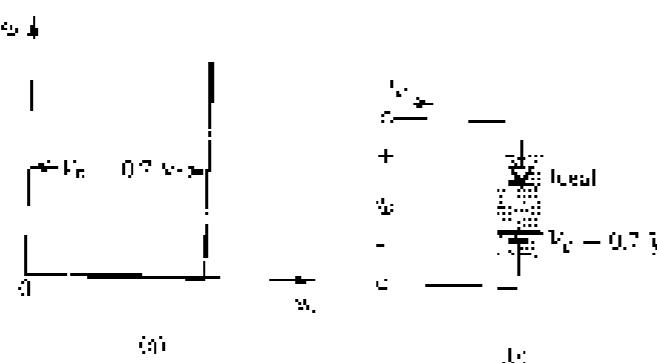


FIGURE 3.16 The transient voltage-drop model of the CBR forward characteristics and its equivalent circuit representation.

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$$I_{\text{av}} = \frac{V_{\text{av}} - 0.7}{R}$$

$$= \frac{3 - 0.7}{1} = 4.3 \text{ mA}$$

which are not too different from the values obtained before, with the same α elements.

3.3.7 The Ideal-Gas Model

In applications that involve voltage levels greater than the diode voltage drop (0.6 – 0.8 V), we may neglect the diode voltage drop altogether while calculating the diode current. The result is the ideal diode model, which we studied in Section 3.1. For the circuit in Examples 3.4 and 3.5 (e.g., Fig. 3.10 with $V_{DD} = 5$ V and $R = 1\text{ k}\Omega$), utilization of the ideal diode model would

$$V_0 = 0 \text{ V}$$

which for a very quick analysis would not be bad as a gross estimate. However, with almost no additional work, the 3-7-V-type model yields much more realistic results. We note, however, that the greatest utility of the ideal-diode model is in determining which diodes are on and which are off in a multidiode circuit, such as those considered in Section 3.1.

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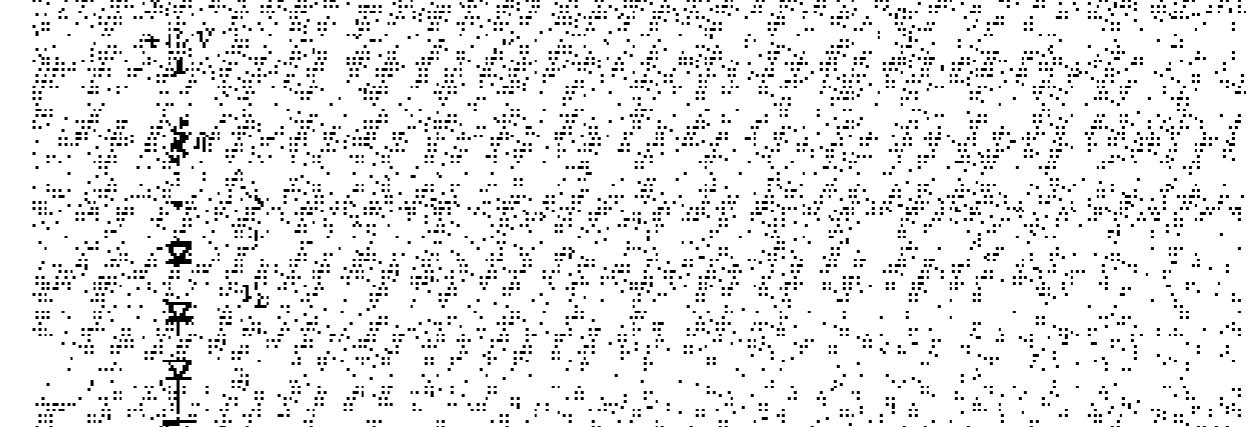


FIGURE 23.12 Repeating Exercise 23.1 using the 0.7-V-avg voltage to obtain better estimates of \bar{V} and \bar{V}^2 than those obtained by Exercise 23.1 using the ideal-T bridge result.

3.3.8 The Small-Signal Modes

There are applications in which a noise is desired to operate at a point on the forward $V-I$ characteristic and a small ac signal is superimposed on the dc quantities. For this situation, we find here to determine the dc operating point (V_0 and I_0) of the diode using one of the models discussed above. Most frequently, the 0.7V -drop model is utilized. Then, in

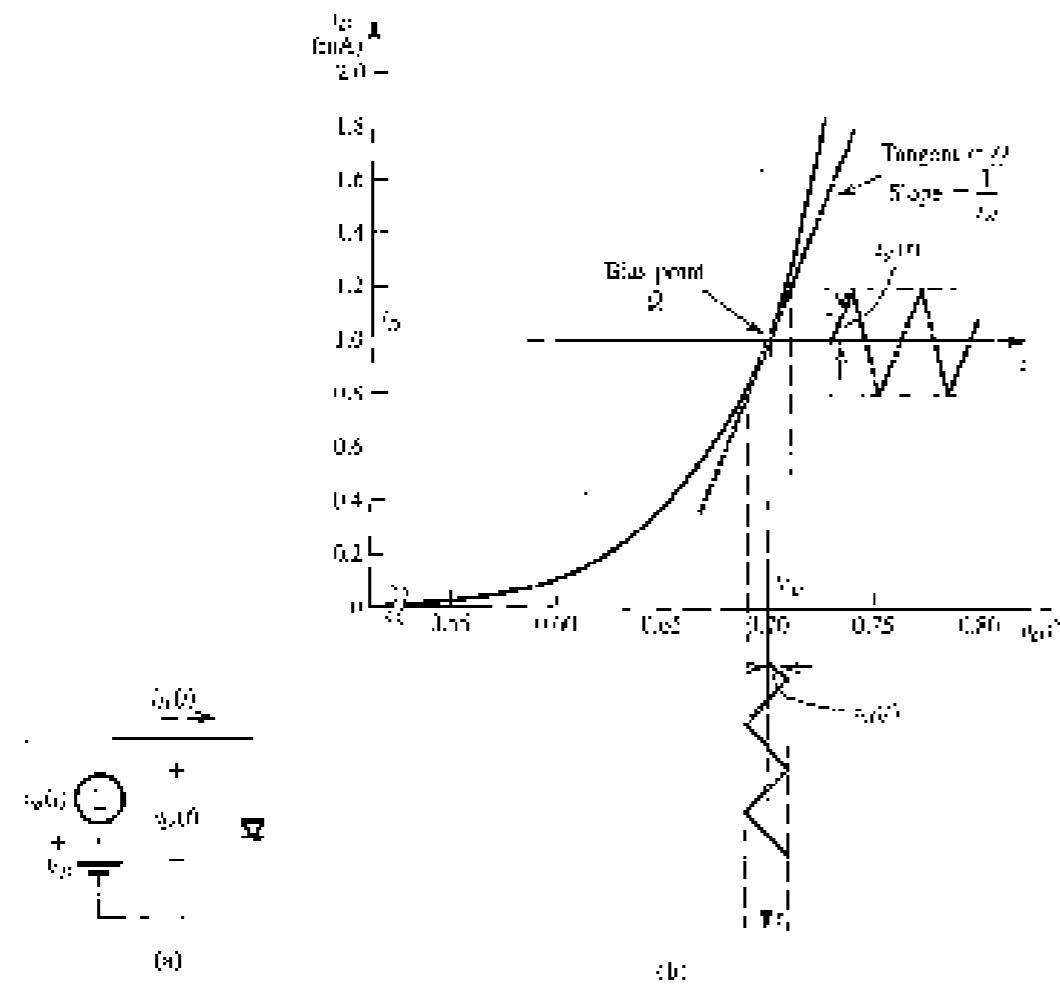


FIGURE 3.17 Development of the diode small-signal model. Note that the numerical values shown are for $n = 2$.

In ac signal operation around the dc bias point, the diode is best modeled by a resistance equal to the inverse of the slope n to the exponential $I-V$ characteristic of the bias point. The concept of treating a nonlinear device and restricting signal operation to a short, almost-linear segment of its characteristic around the bias point was introduced in Section 1.1 for the pentode model. In the following, we develop such a small-signal model for the junction diode and illustrate its application.

Consider the conceptual circuit in Fig. 3.17(b) and the corresponding graphical representation in Fig. 3.17(a). A dc voltage V_D , represented by a battery, is applied to the diode, and a time-varying signal $v_s(t)$, assumed (nearly) to have a triangular waveform, is superimposed on the dc voltage V_D . In the absence of the signal $v_s(t)$, the diode voltage is equal to V_D , and correspondingly, the diode will conduct a dc current I_D given by

$$I_D = I_S e^{\frac{V_D}{nV_T}} \quad (3.1)$$

When the signal $v_s(t)$ is applied, the total instantaneous diode voltage $v_d(t)$ will be given by

$$v_d(t) = V_D + v_s(t) \quad (3.10)$$

Correspondingly, the total instantaneous diode current $i_d(t)$ will be

$$i_d(t) = I_S e^{\frac{V_D + v_s(t)}{nV_T}} \quad (3.11)$$

Substituting for $v_s(t)$ from Eq. (3.10) gives

$$i_d(t) = I_S e^{\frac{V_D}{nV_T} + \frac{v_s(t)}{nV_T}} \quad (3.12)$$

which can be rewritten

$$i_d(t) = I_S e^{\frac{V_D}{nV_T}} e^{\frac{v_s(t)}{nV_T}} \quad (3.13)$$

Using Eq. (3.9) we obtain

$$i_d(t) = I_S e^{\frac{V_D}{nV_T}} \quad (3.14)$$

Now if the amplitude of the signal $v_s(t)$ is kept sufficiently small, such that

$$\frac{v_s(t)}{nV_T} \ll 1 \quad (3.15)$$

then we may expand the exponential of Eq. (3.13) in a series and truncate the series after the first two terms to obtain the approximate expression

$$i_d(t) \approx I_S \left[1 + \frac{v_s(t)}{nV_T} \right] \quad (3.16)$$

This is the small-signal approximation. It is valid for signals whose amplitudes are smaller than about 10 mV for the case $n = 2$ and 5 mV for $n = 1$ (see Sec. 3.1) and recall that $V_T = 25 \text{ mV}$.⁷

From Eq. (3.16) we have

$$i_d(t) = I_S + \frac{I_S}{nV_T} v_s(t) \quad (3.17)$$

Thus, superimposed on the dc current I_S , we have a signal current component directly proportional to the signal voltage $v_s(t)$. That is,

$$i_V = I_S + i_d \quad (3.18)$$

where

$$i_V = \frac{I_S}{nV_T} v_s(t) \quad (3.19)$$

The quantity relating the signal current i_V to the signal voltage $v_s(t)$ has the dimensions of conductance, or mhos (Ω^{-1}), and is called the diode small-signal conductance. The inverse of this parameter is the diode small-signal resistance, or incremental resistance, r_d :

$$r_d = \frac{nV_T}{I_S} \quad (3.20)$$

Note that the value of r_d is necessarily proportional to the bias current I_S .

⁷For $n = 2$, $nV_T/v_s(t) = 0.25 \text{ mV/mV}$. Thus the first term in the series expansion of the exponential, which is $(v_s(t)/nV_T)^2 = 0.025 \text{ mV}^2$, is below $\pm 10 \text{ mV}$ if all the significant digits are kept. A better approximation can be achieved by keeping $v_s(t)$ smaller. Also, note that, for $n = 1$, r_d is limited to, say, 5 mV.

Let us return to the graphical representation in Fig. 3.17(b). It is easy to see that using the small-signal approximation is equivalent to assuming that the signal amplitude is sufficiently small such that the successive swing path curve is linear to a short extent. Under this assumption, the slope of this segment, which is equal to the slope of the tangent to the i_v -curve at the operating point (I_0), is equal to the small-signal conductance. The reader is encouraged to prove that the slope of the i_v -curve at $I = I_0$ is equal to Y_D/v_F , which is $1/r_{DS}$; that is,

$$r_D = 1/\left[\frac{\partial i_v}{\partial v_D}\right]_{I=I_0} \quad (3.19)$$

From the preceding, we conclude that superimposed on the quantities V_D and I_0 that define the dc bias point, or quiescent point, of the diode will be the small-signal quantities $v_s(t)$ and $i_s(t)$, which are related by the diode small-signal resistance r_D evaluated at the bias point (Eq. 3.18). Thus the small-signal analysis can be performed separately from the dc bias analysis, a great convenience that results from the linearization of the diode characteristics inherent in the small-signal approximation. Specifically, after the dc analysis is performed, the small-signal equivalent circuit is obtained by eliminating all dc sources (i.e., short-circuiting dc voltage sources and open-circuiting dc current sources) and replacing the diode by its small-signal resistance. The following example should illustrate the application of the small-signal model.

Example 3.6 Consider the circuit shown in Fig. 3.18(a) for the case in which $R = 50\text{ k}\Omega$. The power-supply V^+ has a dc value of 10 V on which is superimposed a 60-Hz sinusoidal of 1 V peak amplitude. (This "signal" component of the power-supply voltage is an incorporation in the power-supply design. It is known as the power-supply ripple. More on this later.) Calculate both the dc voltage of the diode and the amplitude of the sinusoidal signal appearing across it. Assume the diode to have a 0.7-V drop, 1 mA current, and $a = 2$.

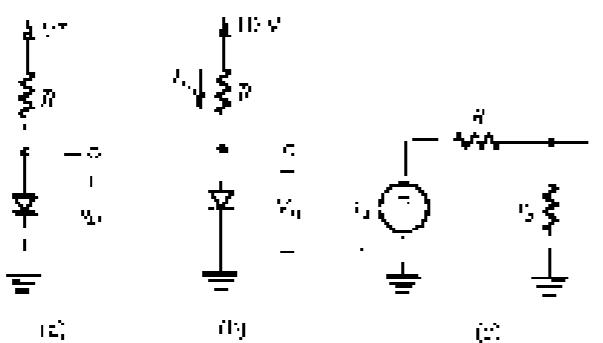


FIGURE 3.18 (a) Circuit for Example 3.6. (b) Circuit to calculate the dc operating point. (c) Small-signal equivalent circuit.

Solution

Considering dc quantities only, we assume $V_D \approx 0.7\text{ V}$ and calculate the diode current

$$i_D = \frac{10 - 0.7}{50} = 0.19\text{ mA}$$

Since this value is very close to 1 mA, the diode voltage will be very close to the assumed value of 0.7 V. At this operating point, the diode incremental resistance is

$$r_D = \frac{\partial V_D}{\partial I_D} = \frac{2 \times 25}{0.99} = 51.5\text{ }\Omega$$

The signal voltage across the diode can be found from the small-signal equivalent circuit in Fig. 3.18(c). Here v_s denotes the 60-Hz 1-V peak sinusoidal component of V_D , and v_a is the corresponding signal across the diode. Using the voltage-to-diode rule provides the peak amplitude of v_a as follows:

$$\begin{aligned} v_a (\text{peak}) &= \frac{R}{R + r_D} v_s \\ &= 1 \frac{0.0358}{51.5 + 0.0358} = 0.66\text{ mV} \end{aligned}$$

Finally, we note that since this value is quite small, use of the small-signal model of the diode is justified.

3.9 Use of the Diode Forward Drop in Voltage Regulation

A further application of the diode small-signal model is found in a popular diode application, namely the use of diodes to create a regulated voltage. A voltage regulator is a circuit whose purpose is to provide a constant dc voltage between its output terminals. The output voltage is required to remain as constant as possible in spite of (a) changes in the load current drawn from the regulator output terminals and (b) changes in the dc power-supply voltage that feeds the regulator circuit. Since the forward voltage drop of the diode remains almost constant at approximately 0.7 V while the current through it varies by relatively large amounts, a forward-biased diode can make a unique voltage constant. For instance, we have seen in Example 3.6 that while the 10-V dc supply voltage had a ripple of 2 V peak-to-peak ($\pm 10\%$ variation), the corresponding ripple in the diode voltage was only about 1.5 mV ($\pm 0.3\%$ variation). Regulated voltages greater than 0.7 V can be obtained by connecting a number of diodes in series. For example, the use of three forward-biased diodes in series provides a voltage of about 2.1 V. One such circuit is investigated in the following example, which utilizes the diode small-signal model to quantify the efficiency of the voltage regulator that is realized.

Example 3.7

Consider the circuit shown in Fig. 3.19. A string of three diodes is used to provide a constant voltage of about 2.1 V. We want to estimate the percent age change in this regulated voltage caused by (a) a $\pm 10\%$ change in the power-supply voltage and (b) connection to a $1\text{-m}\Omega$ load resistance. Assume $a = 2$.

Solution

With no load, the nominal value of the current in the diode string is given by

$$i = \frac{10 - 2.1}{1} = 7.9\text{ }\mu\text{A}$$

Thus each diode will have an incremental resistance of

$$r_D = \frac{\partial V_D}{\partial I_D}$$

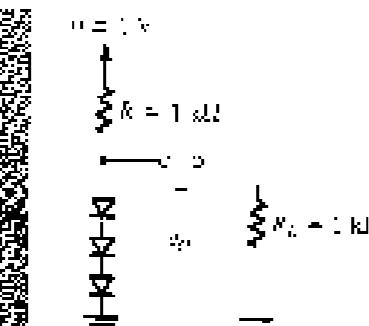


FIGURE 3.19 Circuit for Example 3.7.

Using $n = 2$ gives

$$r_s = \frac{25}{1.3} = 18.9 \Omega$$

The three diodes in series will have a total incremental resistance:

$$r = 3r_s = 56.7 \Omega$$

This resistance, along with the resistance R , forms a voltage divider whose ratio can be used to calculate the change in output voltage due to a $\pm 10\%$ rise ($\pm 1\text{V}$) change in supply voltage. Thus the peak-to-peak change in output voltage will be

$$\Delta v_o = 2 \cdot \frac{r}{R + r} = \frac{0.02 \cdot 56.7}{0.02 \cdot 56.7 + 1} = 17.1 \text{ mV}$$

That is, corresponding to the $\pm 1\text{V}$ $\pm 10\%$ change in supply voltage, the output voltage will change by $\pm 17.1 \text{ mV}$ or $\pm 0.9\%$. Since this implies a change of about 0.3 mV per diode, our use of the small-signal model is justified.

When a load resistance of $1 \text{ k}\Omega$ is connected across the diode string, it draws a current of approximately 2.1 mA . Thus the excess in the diodes decreases by 2.1 mV , resulting in a decrease in voltage across the diode string given by

$$\Delta v_o = -2.1 \times r = -2.1 \times 18.9 = -39.7 \text{ mV}$$

Since this implies that the voltage across each diode decreases by about 13.9 mV , the use of the small-signal model is not entirely justified. Nevertheless, a detailed calculation of the voltage change using the exponential model results in $\Delta v_o = -36.5 \text{ mV}$, which is not too different from the approximate value obtained using the incremental model.

EXERCISES

- 3.14 Find the value of the ideal small-signal resistance, r_s , for currents of 0.01 mA , 1 mA , and 10 mA . Assume $n = 1$.
- 3.15 $I_v = 25 \text{ mA}$; 25 mV ; 2.5Ω
- 3.16 Calculate the peak-to-peak change in output voltage due to a $\pm 10\%$ change in supply voltage ($\pm 10\text{V}$) for a $10 \text{ k}\Omega$ load, 5 mA (2.5 mA), and 50 mA (25 mA). Use $n = 1$ and $r_s = 2.5 \Omega$. In each case, (a) calculate Δv_o using the small-signal model and (b) using the exponential model.
- 3.17 $(a) -0.16, -0.25 \text{ mA}; (b) -0.23, -0.15, -0.05, -0.10, -0.02 \text{ mA}; (c) -0.24, -0.34, -0.40 \text{ mA}$

- 3.16 Please see the circuit of Fig. 3.16 under $V_o = 3 \text{ V}$ when $I_s = 0$ and V_o changes by $\pm 10\text{V}$ for 1 unit of load current. Find the value of r_s and the peak-to-peak exponential (not small-signal) change in output voltage for a diode with $n = 1$ and $r_s = 2.5 \Omega$.

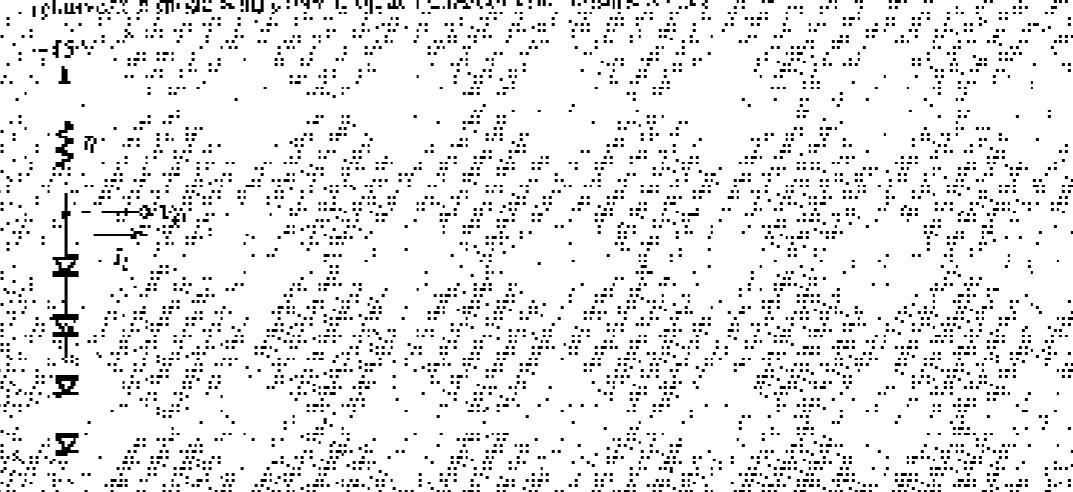


FIGURE 3.16

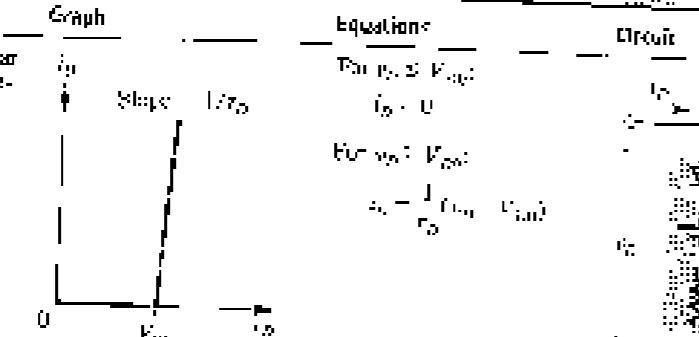
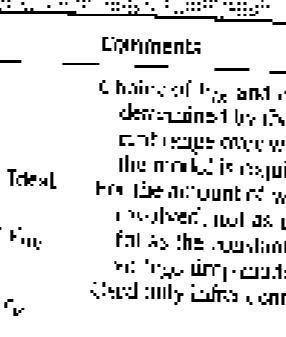
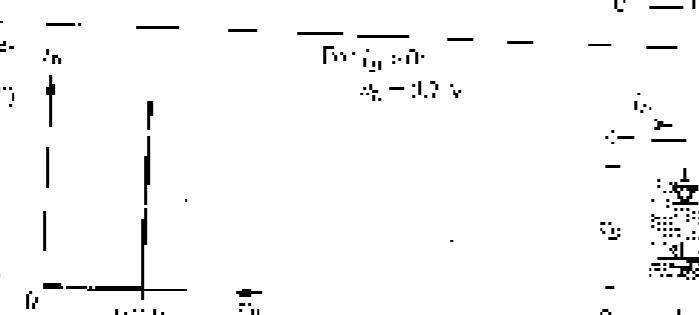
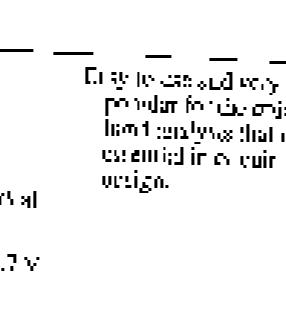
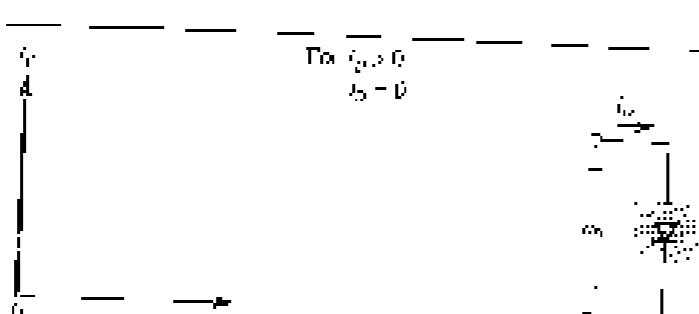
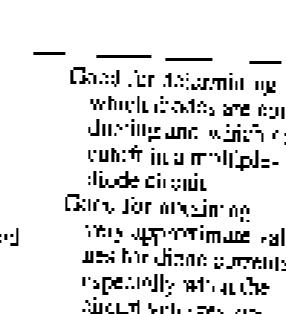
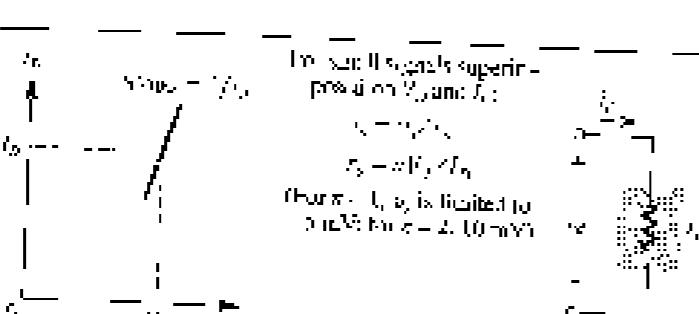
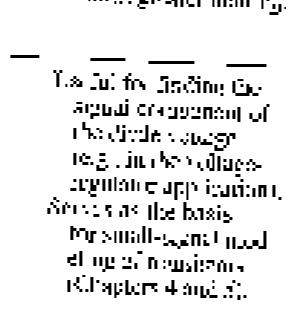
Ex. $R = 1 \text{ k}\Omega$; 0.14

3.3.10 Summary

As a summary of this important section on diode modeling, Table 3.1 lists the five diode models studied and provides pertinent comments regarding each. These comments are intended to aid in the selection of an appropriate model for a particular application. The question "which model?" is one that circuit designers face repeatedly, not just with diodes but with every circuit element. The truth is, finding an appropriate compromise between accuracy and speed of analysis. One's ability to select appropriate device models improves with practice and experience.

TABLE 3.1 Modeling the Diode Forward Characteristic

Model	Graph	Equations	Circuit	Comments
Exponential		$I_v = I_s e^{V_v/V_T}$ $V_T = 2.3 \text{ mV}$ for $n = 1$ $V_T = 2.3 \text{ mV} \log \left(\frac{I_v}{I_{s1}} \right)$ $V_{T2} = V_{T1} + 2.3 \text{ mV} \log \left(\frac{I_{v2}}{I_{s1}} \right)$ $2.3 n V_T = 83 \text{ mV}$ for $n = 1$ $2.3 n V_T = 120 \text{ mV}$ for $n = 2$		$I_v = 10^{-12} \text{ A} \rightarrow 10^{12} \text{ A}$ depending on junction area $V_T = 25 \text{ mV}$ $n = 1 \text{ to } 2$ Physically based and reasonably accurate model (useful when more analysis is needed)
Small-signal		$I_s = r_s V_v$		(Continued)
Incremental		$I_s = r_s V_v$		(Continued)

Model	Graph	Equations	Circuit	Comments
Diode in linear (series plus resistance)		For $V_d < V_{knee}$: $i_d = \frac{V_d}{R_s}$ For $V_d > V_{knee}$: $i_d = I_{sat} + \frac{V_d - V_{knee}}{R_s}$		Choice of R_s and i_{sat} is determined by the circuit requirements once which the model is required. For the amount of work involved, not as useful as the exponential model presented.
Constant-voltage- drop (≈ 0.7 V model*)		For $i_d > 0$: $V_d = 0.7$ V		Easy to use and very popular for the quick hand analysis that is common in circuit design.
Ideal diode		To $i_d > 0$: $i_d = \infty$		Used for determining which diodes are conducting and which are cut off in a multiple-diode circuit.
Small-signal		In small-signal superposition: $i_s = V_d / R_s$ $i_s = n I_d / I_s$ But $n \cdot I_d / I_s$ is limited to 0.125 for $n = 2$, 0.050 for $n = 1$.		Useful for finding the approximate values for diode currents, especially when the diode voltages are much greater than V_0 .

3.4 OPERATION IN THE REVERSE BREAKDOWN REGION—ZENER DIODES

The very steep i_v - v curve that the diode exhibits in the breakdown region (Fig. 3.8) and the diode's constant voltage drop after this indicates that diodes operating in the breakdown region can be used in the design of voltage regulators. From the previous section, the reader will recall that voltage regulators are circuits that provide constant dc output voltages in the face of changes in their load current and in the system power-supply voltage. This in fact turns out to be an important application of diodes operating in the reverse breakdown region, and special diodes are manufactured to operate specifically in the breakdown region. Such diodes are called **breakdown diodes** or, more commonly, **zener diodes**, after its early worker in the area.

Figure 3.20 shows the circuit symbol of the zener diode. In normal applications of zener diodes, current flows into the cathode, and the cathode is positive with respect to the anode. Thus $i_z \geq 0$ in Fig. 3.20 (any positive values).

3.4.1 Specifying and Modeling the Zener Diode

Figure 3.21 shows details of the diode's i_v - v characteristics in the breakdown region. We observe that the current is greater than the knee current I_{ZK} specified on the data sheet of



FIGURE 3.20 Circuit symbol for a zener diode.

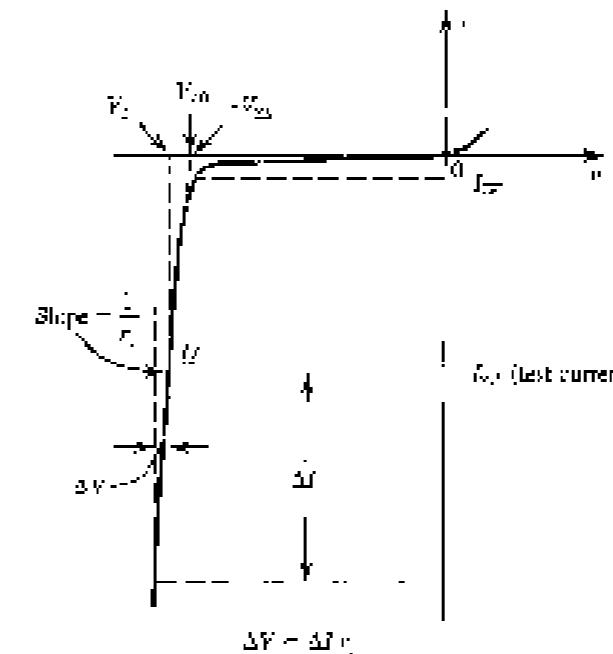


FIGURE 3.21 The diode's i_v - v characteristics with the breakdown region shown in some detail.

In a zener diode, the $I-V$ characteristic is almost a straight line. The manufacturer usually specifies the voltage across the zener diode V_2 at a specified test current, I_{ZT} . We have indicated these parameters in Fig. 3.21 as the coordinates of the point labeled Q . Thus a 6.8-V zener diode will exhibit a 6.8-V drop at a specified test current of, say, 10 μA . As the bias current through the zener deviates from I_{ZT} , the voltage across it will change, though only slightly. Figure 3.21 shows the corresponding current change ΔI for zener voltage changes by ΔV , which is related to ΔI by

$$\Delta V = r_z \Delta I$$

where r_z is the inverse of the slope of the almost-linear $I-V$ curve at point Q . Resistance r_z is the incremental resistance of the zener diode at operating point Q . It is also known as the dynamic resistance of the zener, and its value is specified on the device data sheet. Typically, r_z is in the range of a few ohms to a few tens of ohms. Obviously, the lower the value of r_z is, the more constant the zener voltage remains as its current varies and thus the more ideal its performance becomes in the design of voltage regulators. In this regard, we observe from Fig. 3.21 that while r_z remains low and almost constant over a wide range of current, its value increases considerably in the vicinity of the knee. Therefore, as a general design guideline, one should avoid operating the zener in this low-current region.

Zener diodes are fabricated with voltages V_2 in the range of a few volts to a few thousand volts. In addition to specifying V_2 for a particular current I_{ZT} , r_z , and I_{ZM} , the manufacturer also specifies the maximum power that the device can safely dissipate. Thus a 0.5-W, 6.8-V zener diode can operate safely at currents up to a maximum of about 70 μA .

The almost linear $I-V$ characteristic of the zener diode suggests that the device can be modeled as indicated in Fig. 3.22. Here V_{Z0} denotes the point at which the straight line of slope $1/r_z$ intersects the voltage axis [refer to Fig. 3.21]. Although V_{Z0} is shown to be slightly different from the zener voltage V_2 , in practice their values are almost equal. The equivalent circuit model of Fig. 3.22 can be analytically described by

$$V_Z = V_{Z0} + r_z I_Z \quad (3.20)$$

and it applies for $I_Z > I_{ZM}$ and, obviously, $V_Z > V_{Z0}$.

3.4.2 Use of the Zener as a Shunt Regulator

We now illustrate, by way of an example, the use of zener diodes in the design of shunt regulators, so named because the regulator circuit appears in parallel (shunt) with the load.

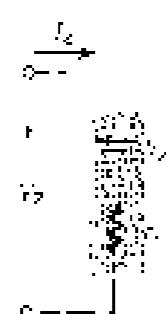


FIGURE 3.22 Model for the zener diode.

Example 3.2

The 6.8-V zener diode in the circuit of Fig. 3.23(a) is specified to have $V_2 = 6.8 \text{ V}$ at $I_Z = 5 \text{ mA}$. The 6.8-V zener diode in the circuit of Fig. 3.23(b) is specified to have $V_2 = 6.7 \text{ V}$ at $I_Z = 5 \text{ mA}$, $r_z = 0.5 \text{ k}\Omega$, and $I_{ZM} = 20 \text{ mA}$. The supply voltage V^+ is normally 10 V but can vary by $\pm 1 \text{ V}$.

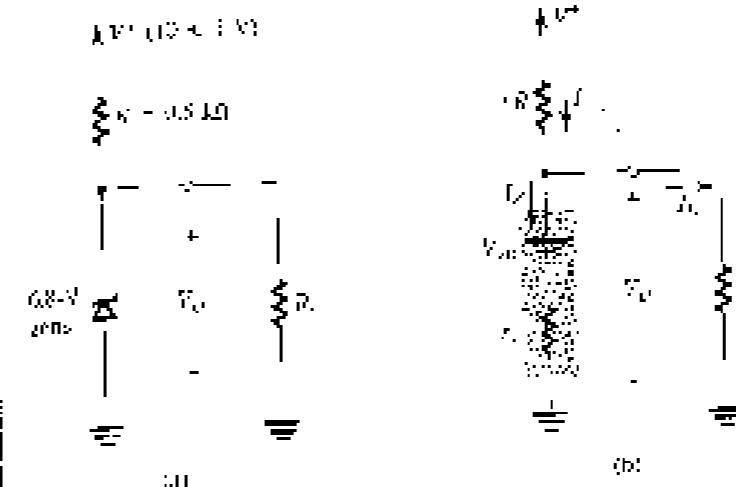


FIGURE 3.23 (see also Fig. 3.22). (a) The zener diode in a standard zener voltage regulator circuit. (b) The zener diode in a shunt regulator circuit.

- (a) Find V_0 with no load and with V^+ at its nominal value.
- (b) Find the change in V_0 resulting from the $\pm 1 \text{ V}$ change in V^+ . Note that $(\Delta V_0)/(\Delta V^+)$, usually expressed in millivolt/millivolt, is known as line regulation.
- (c) Find the change in V_0 resulting from connecting a load resistance R_L that draws a current $I_L = 1 \text{ mA}$, and hence find the load regulation $(\Delta V_0)/(\Delta I_L)$ in millivolt/milliampere.
- (d) Find the change in V_0 when $R_L = 2 \text{ k}\Omega$.
- (e) Find the value of V_0 when $R_L = 3.5 \text{ k}\Omega$.
- (f) What is the minimum value of R_L for which the diode will operate in the breakdown region?

Solution

First we must determine the value of the parameter V_{Z0} of the zener diode model by referring to Fig. 3.23(b). Since $V_2 = 6.8 \text{ V}$, $I_Z = 5 \text{ mA}$, and $r_z = 0.5 \text{ k}\Omega$ in Eq. (3.20) yields $V_{Z0} = 6.7 \text{ V}$, Figure 3.23(b) is equivalent to the circuit with the zener diode replaced with its model.

- (a) With no load connected, the current through the zener is given by

$$\begin{aligned} I_Z &= I = \frac{V - V_{Z0}}{R + r_z} \\ &= \frac{10 - 6.7}{0.5 + 0.02} = 6.35 \text{ mA} \end{aligned}$$

Thus,

$$\begin{aligned} V_0 &= V_{Z0} + I_Z r_z \\ &= 6.7 + 0.35 \times 0.02 = 6.73 \text{ V} \end{aligned}$$

(ii) For a $\pm 1\text{ V}$ change in V_1 , the change in output voltage can be found as

$$\Delta V_o = \Delta V \cdot \frac{R_1}{R+R_1} \\ = 1 \times \frac{20}{500 + 20} = +0.5\text{ mV}$$

Thus,

$$\text{Load regulation} = 30\text{ mV/V}$$

(iii) When a load resistance R_L that draws a load current $I_L = 1\text{ mA}$ is connected, the zener current will decrease by 1 mA . The corresponding change in zener voltage can be found from

$$\Delta V_o = r_z \Delta I_z \\ = 20 \times 1 = -20\text{ mV}$$

Thus the load regulation is

$$\text{Load regulation} = \frac{\Delta V_o}{\Delta I_L} = -20\text{ mV/mA}$$

(iv) When a load resistance of $2\text{ k}\Omega$ is connected, the load current will be approximately $6.8\text{ V}/2\text{ k}\Omega = 3.4\text{ mA}$. Thus the change in zener current will be $\Delta I_z = -3.4\text{ mA}$, and the corresponding change in zener voltage (output voltage) will thus be

$$\Delta V_o = r_z \Delta I_z \\ = 20 \times -3.4 = -68\text{ mV}$$

This calculation, however, is approximate, because it neglects the change in the current I . A more accurate estimate of ΔV_o can be obtained by analyzing the circuit in Fig. 3.23(b). The result of such an analysis is $\Delta V_o = -70\text{ mV}$.

(v) An R_L of $0.5\text{ k}\Omega$ would draw a load current of $6.8\text{ V}/0.5 = 13.6\text{ mA}$. This is not possible, because the current supplied through R is only 6.4 mA (for $V_1 = 10\text{ V}$). Therefore, the zener must be off. With this in mind, then V_o is determined by the voltage divider formed by R_1 and R (Fig. 3.23a),

$$V_o = V_1 \cdot \frac{R_1}{R+R_1} \\ = 10 \cdot \frac{0.5}{0.5 + 20} = 5\text{ V}$$

Since this voltage is lower than the breakdown voltage of the zener, the diode is indeed not operating in the breakdown region.

(vi) For the zener to be at the edge of the breakdown region, $I_z = I_S = 0.2\text{ mA}$ and $V_z = V_{zB} = 0.7\text{ V}$. At this point the forward current applied through R is $(V_1 - 0.7)/0.5 = 14.6\text{ mA}$, and thus the load current is $14.6 - 0.2 = 14.4\text{ mA}$. The corresponding value of R_L is

$$R_L = \frac{6.8}{14.4} = 0.48\text{ k}\Omega$$

3.4.3 Temperature Effects

The dependence of the zener voltage V_z on temperature is specified in terms of the temperature coefficient TC , or Imax as it is commonly known, which is usually expressed in mV/C .

The value of TC depends on the zener voltage, and for a given diode the TC varies with the operating current. Zener diodes whose V_z are lower than about 5 V exhibit a negative TC . On the other hand, zeners with higher voltages exhibit a positive TC . The TC of a zener diode with a V_z of about 5 V can be made zero by operating the diode at a specified current. Another evolutionarily used technique for obtaining a reference voltage with low temperature coefficient is to connect a zener diode with a positive temperature coefficient of about 2 mV/C in series with a forward-conducting diode. Since the forward-conducting diode has a voltage drop of -0.7 V and a TC of about -2 mV/C , the series combination will provide a voltage of $(V_T + 0.7)$ with a TC of about zero.

EXERCISES

- 3.17 A zener diode with a zener voltage of 10 V and a current of 10 mA is connected in series with a resistor R and a load $R_L = 10\text{ k}\Omega$. If the input voltage V_1 is varied from 10 V to 12 V , calculate the load regulation. Assume $r_z = 20\text{ mV}$ and $I_S = 0.1\text{ mA}$.
- 3.18 A zener diode with a zener voltage of 10 V and a current of 10 mA is connected in series with a resistor R and a load $R_L = 10\text{ k}\Omega$. If the input voltage V_1 is varied from 10 V to 12 V , calculate the load regulation. Assume $r_z = 20\text{ mV}$ and $I_S = 0.1\text{ mA}$.
- 3.19 A zener diode with a zener voltage of 10 V and a current of 10 mA is connected in series with a resistor R and a load $R_L = 10\text{ k}\Omega$. If the input voltage V_1 is varied from 10 V to 12 V , calculate the load regulation. Assume $r_z = 20\text{ mV}$ and $I_S = 0.1\text{ mA}$.
- 3.20 A zener diode with a zener voltage of 10 V and a current of 10 mA is connected in series with a resistor R and a load $R_L = 10\text{ k}\Omega$. If the input voltage V_1 is varied from 10 V to 12 V , calculate the load regulation. Assume $r_z = 20\text{ mV}$ and $I_S = 0.1\text{ mA}$.
- 3.21 A zener diode with a zener voltage of 10 V and a current of 10 mA is connected in series with a resistor R and a load $R_L = 10\text{ k}\Omega$. If the input voltage V_1 is varied from 10 V to 12 V , calculate the load regulation. Assume $r_z = 20\text{ mV}$ and $I_S = 0.1\text{ mA}$.

3.4.4 A Final Remark

Though simple and useful, zener diodes have lost a great deal of their popularity in recent years. They have been virtually replaced in voltage-regulation design by specially designed integrated circuits (ICs) that perform the voltage-regulation function much more effectively and with greater flexibility than zener diodes.

3.5 RECTIFIER CIRCUITS

One of the most important applications of diodes is in the design of rectifier circuits. A diode rectifier forms an essential building block of the dc power supplies required to power electronic equipment. A block diagram of such a power supply is shown in Fig. 3.24. As indicated, the power supply is fed from the 120-V (rms) 60-Hz ac line, and it delivers a dc voltage V_o (usually in the range of 5–20 V) to an electronic circuit represented by the *load* block. The dc voltage V_o is required to be as constant as possible in spite of variations in the ac line voltage and in the current drawn by the load.

The first block in a dc power supply is the **power transformer**. It consists of two separate coils wound around an iron core that magnetically couples the two windings. The primary winding, having N_1 turns, is connected to the 120-V ac supply, and the secondary winding, having N_2 turns, is connected to the circuit of the dc power supply. Thus an ac voltage v_s

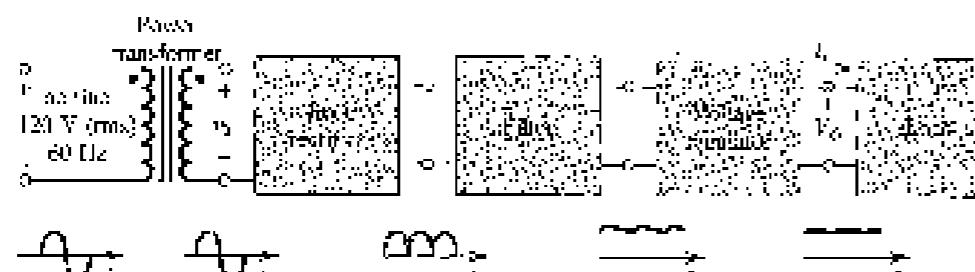


FIGURE 3.24 Block diagram of a rectifier power supply.

of $(120/N_2/N_1)V$ (rms) develops between the two terminals of the secondary winding. By selecting an appropriate turns ratio (N_2/N_1) for the transformer, the designer can step the line voltage down to the value required to yield the particular dc voltage output of the supply. For instance, a secondary voltage of 30 V rms may be appropriate for a dc output of 5 V. This can be achieved with a 15:1 turn ratio.

In addition to providing the appropriate sinusoidal amplitude for the dc power supply, the power transformer provides electrical isolation between the electronic equipment and the power line circuit. This isolator minimizes the risk of electric shock to the equipment user.

The diode rectifier converts the input sinusoidal waveform to a pulsed output, which can have the pulsating waveform indicated in Fig. 3.24. Although this waveform has a nonzero average or a dc component, its pulsating nature makes it unsuitable as a dc source for electronic circuits, hence the need for a filter. The variations in the magnitude of the rectifier output are considerably reduced by the filter block in Fig. 3.24. In the following sections we shall study a number of rectifier circuits and a simple implementation of the output filter.

The output of the rectifier filter, though much more constant than without the filter, still contains a time-dependent component, known as ripple. To reduce the ripple and to stabilize the magnitude of the dc output voltage of the supply against variations caused by changes in load current, a voltage regulator is employed. Such a regulator can be implemented using the zener diode regulation configuration studied in Section 3.4. Alternatively, and much more commonly at present, an integrated-circuit regulator can be used.

3.5.1 The Half-Wave Rectifier

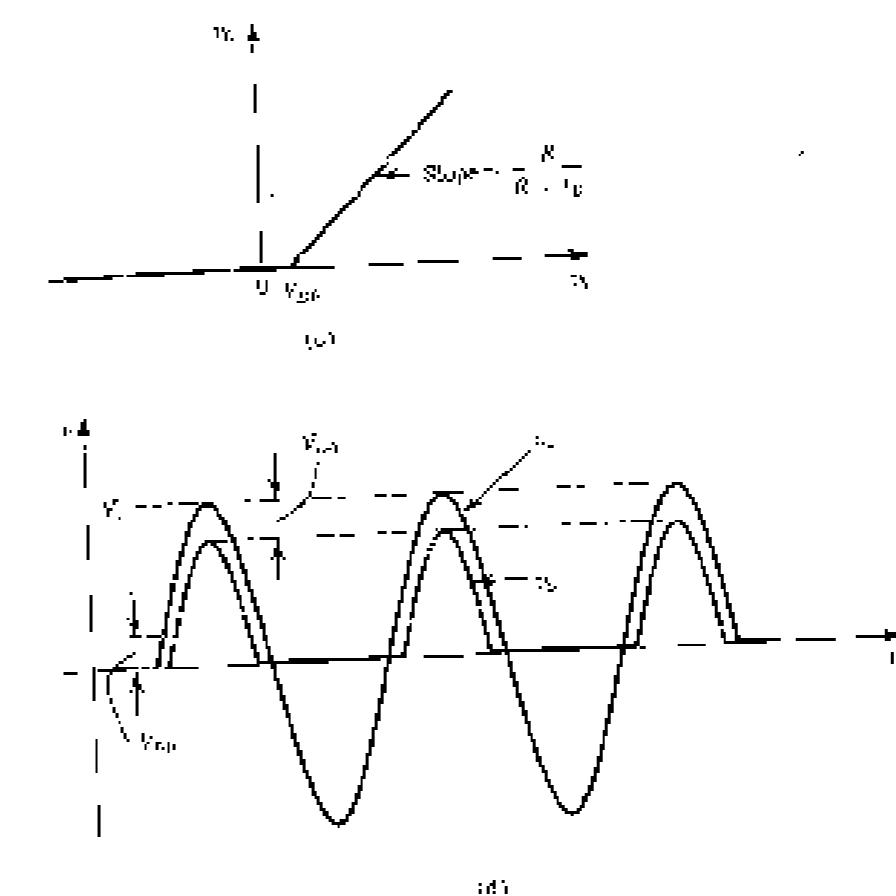
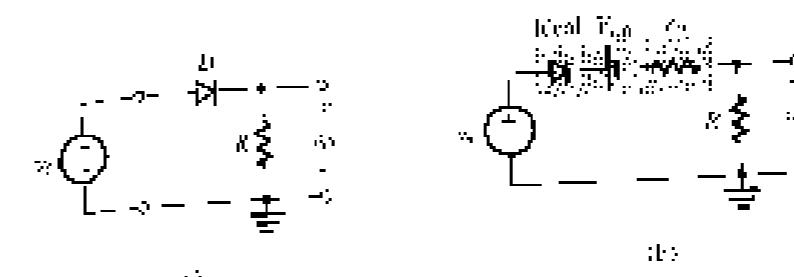
The half-wave rectifier utilizes alternate half-cycles of the input sinusoid. Figure 3.25(a) shows the circuit of a half-wave rectifier. This circuit was analyzed in Section 3.1 (see Fig. 3.3) assuming an ideal diode. Using the more realistic battery-plus-resistor diode model, we obtain the equivalent circuit shown in Fig. 3.25(b), from which we can write

$$v_D = 0, \quad v_S < V_{DS} \quad (3.21a)$$

$$v_D = \frac{R}{R + r_D} v_S - V_{DS} \frac{R}{R + r_D}, \quad v_S > V_{DS} \quad (3.21b)$$

The transfer characteristic represented by these equations is plotted in Fig. 3.25(c). In many applications, $r_D \gg R$ and the second equation can be simplified to

$$v_D \approx v_S - V_{DS} \quad (3.22)$$

FIGURE 3.25 (a) Half-wave rectifier. (b) Equivalent circuit of the half-wave rectifier with the diode represented with its battery-plus-resistor model. (c) Transfer characteristic of the circuit in (b). (d) Input and output waveforms assuming $V_{DS} = 5$ V.

where $V_{DS} = 0.7$ V or 0.8 V. Figure 3.25(d) shows the output voltage obtained when the input v_S is a sinusoid.

In selecting diodes for rectifier design, two important parameters must be specified: the forward current-handling capability (rating) of the diode, determined by the largest current the diode is expected to conduct, and the peak inverse voltage (PIV) that the diode must be able to withstand without breakdown, determined by the largest reverse voltage that is expected

to appear across the diode. In the rectifier circuit of Fig. 3.25(a), we observe that when $v_2 < 0$, negative bias is applied to the diode, and it will be cut off. It follows that the PIV is equal to the peak of v_2 .

$$\text{PIV} = V_p$$

It is usually prudent, however, to select a diode that has a reverse breakdown voltage at least 50% greater than the expected PIV.

Half-Wave Rectifier. Before leaving the half-wave rectifier, the reader should note two points. First, it is possible to use the diode exponential characteristic to determine the exact transfer characteristic of the rectifier (see Problem 3.73). However, the amount of work involved is usually too great to be justified in practice. Of course, such an analysis can be easily done using a computer circuit-analysis program such as SPICE (see Section 3.9).

Second, whether we analyze the circuit analytically or not, it should be obvious that this circuit does not function properly when the input signal is sinusoidal. For instance, this circuit cannot be used to rectify an input sinusoid of 100-mV amplitude. For such an application one resorts to a so-called precision rectifier, a circuit using diodes in conjunction with op amps. One such circuit is presented in Section 4.5.5.

EXERCISE

- 3.25 The half-wave rectifier shown in the accompanying diagram uses a center-tapped secondary winding. The diodes conduct during half cycles of the input voltage. The peak-to-peak output voltage is $V_o = 2V_p$. If the input voltage is given by $v_2 = V_p \sin(\omega t)$, determine the output voltage v_o and the current through the load resistor R . Assume that the diodes have a constant voltage drop V_d and a constant current-voltage characteristic.

3.5.2 The Full-Wave Rectifier

The full-wave rectifier utilizes both halves of the input waveform. To provide a unipolar output, i.e., inverse the negative halves of the sine wave, one possible implementation is shown in Fig. 3.26(a). Here the transformer secondary winding is center-tapped to provide two equal voltages of opposite polarity across the two halves of the secondary winding with the polarities indicated. Note that when the input line voltage (needing the primary) is positive, both of the voltages labeled v_2 will be positive. In this case, D_1 will conduct and D_2 will be reverse biased. The current through D_1 will flow through R and back to the center tap of the secondary. The circuit then behaves like a half-wave rectifier, and the current during the negative half-cycles when D_1 conducts will be identical to that produced by the half-wave rectifier.

Now, during the negative half-cycle of the v_2 line voltage, both of the voltages labeled v_2 will be negative. Thus, D_1 will be cut off while D_2 will conduct. The current conducted by D_2 will flow through R and back to the center tap. It follows that during the negative half-cycles while D_2 conducts, the circuit behaves again as a half-wave rectifier. The important point, however, is that the current through R always flows in the same direction, and thus v_o will be unipolar, as indicated in Fig. 3.26(c). The output waveform shown is obtained

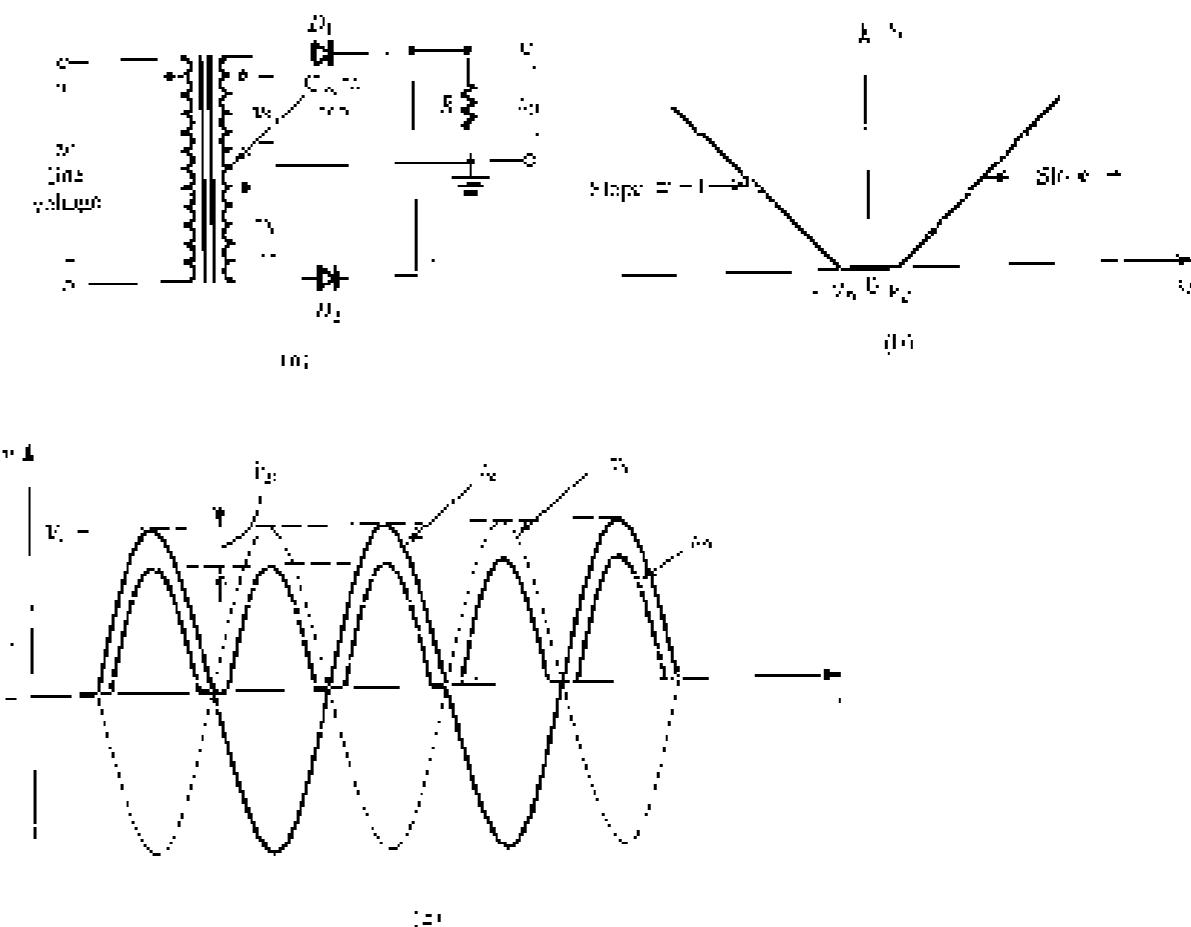


FIGURE 3.26 Full-wave rectifier utilizing a center-tapped secondary winding.
(a) circuit; (b) transfer characteristic assuming a constant-voltage drop model for the diodes (or input and output voltages).

by assuming that a conducting diode has a constant voltage drop V_d . Note the term "symmetric" of the full-wave rectifier takes the same shown in Fig. 3.26(b).

The full-wave rectifier obviously introduces a more "energetic" waveform than that produced by the half-wave rectifier. In almost all rectifier applications, one opt for a full-wave type of some kind.

To find the PIV of the diodes in the full-wave rectifier circuit, consider the situation depicted in the positive half-cycles. There D_1 is conducting, and D_2 is cut off. The voltage at the cathode of D_1 is v_2 , and that at its anode is $-v_2$. Thus, the reverse voltage across D_2 will be $(v_2 - v_2)$, which will reverse its maximum when v_2 is at its peak value of $(V + V_d)$, and v_2 is at its peak value of V_d , thus:

$$\text{PIV} = 2V_d + V_p$$

which is approximately twice that for less of the half-wave rectifier.

EXERCISE:

Determine the half-wave rectifier output voltage v_o during the positive half-cycle of the input voltage v_i if the peak value of the input voltage is $V_p = 2V_0$, the load resistance is $R = 10\ \Omega$, and the peak inverse voltage of the diodes is $V_{PIV} = 2V_0$. Assume the diodes are ideal.

3.5.3 The Bridge Rectifier

An alternative implementation of the full-wave rectifier is shown in Fig. 3.27(a). The circuit is known as the bridge rectifier because of its similarity of its configuration to that of the Wheatstone bridge. It does not require a center-tapped transformer, a distinct advantage over the full-wave rectifier circuit of Fig. 3.26. The bridge rectifier, however, requires four diodes as compared to two in the previous circuit. This is not much of a disadvantage, because diodes are inexpensive and one can buy a diode bridge in one package.

The bridge circuit operates as follows: During the positive half-cycles of the input voltage, v_i is positive, and that current is conducted through diode D_1 , resistor R , and

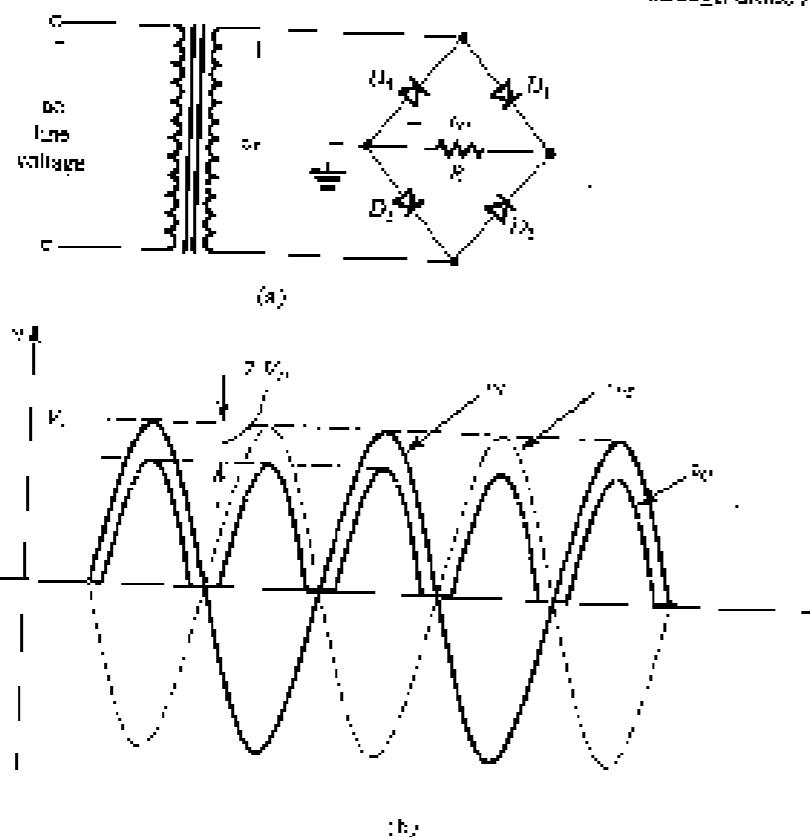


FIGURE 3.27 The bridge rectifier circuit; the input and output waveforms.

diode D_2 . Meanwhile, diodes D_1 and D_2 will be reverse biased. (Remember that there are two diodes in series in the conduction path, and thus v_o will be lower than v_i by two diode drops (compared to one drop in the circuit previously discussed).) This is somewhat of a disadvantage of the bridge rectifier.

Next, consider the situation during the negative half-cycles of the input voltage. The secondary voltage v_s will be negative, and thus $-v_s$ will be positive, forcing current through D_2 , R , and D_1 . Meanwhile, diodes D_1 and D_2 will be reverse biased. The important point to note, though, is that during both half-cycles, current flows through R in the same direction (from right to left), and thus v_o will always be positive, as indicated in Fig. 3.27(b).

To determine the peak inverse voltage (PIV) of each diode, consider the circuit during the positive half-cycles. The reverse voltage across D_1 can be determined from the loop formed by D_1 , R , and D_2 as

$$v_{D1}(\text{reverse}) = v_o + v_{D2}(\text{forward})$$

Thus the maximum value of v_{D1} occurs at the peak of v_i and is given by

$$\text{PIV} = V_s + 2V_D + V_B = V_s + V_D$$

Observe that here the PIV is about half the value for the full-wave rectifier with a center-tapped transformer. This is another advantage of the bridge rectifier.

Yet one more advantage of the bridge rectifier circuit, over that utilizing a center-tapped transformer is that only about half as many turns are required for the secondary winding of the transformer. Another way of looking at this point can be obtained by observing that each half of the secondary winding of the center-tapped transformer is utilized for only half the time. These advantages have made the bridge rectifier the most popular rectifier circuit configuration.

EXERCISE:

For the bridge rectifier of part (a) of Fig. 3.27, use the peak-value-load-diode model to show that the average value (v_{oav}) of the output voltage is $v_{oav} = (V_s - V_D)/R = 31\ \text{V}$, and that the peak-to-peak output voltage is $2(V_s - V_D)/R = 62\ \text{V}$. Find numerical values for the quantities in (a) and (b) and the PIV for the case in which v_i is a 12-V (rms) sinusoid, $R = 6.3\ \Omega$, and $V_D = 0.1\ \Omega$.

3.5.4 The Rectifier with a Filter Capacitor—The Peak Rectifier

The pulsating nature of the output voltage produced by the rectifier circuit discussed above makes it unsuitable as a dc supply for electronic circuits. A simple way to reduce the variation of the output voltage is to place a capacitor across the load resistor. It will be shown that this filter capacitor serves to reduce substantially the variations in the rectifier output voltage.

To see how the rectifier circuit with a filter capacitor works, consider first the simple circuit shown in Fig. 3.28. Let the input v_i be a sine wave with a peak value V_p , and assume the diode to be ideal. As v_i goes positive, the diode conducts and the capacitor is charged so that $v_o = v_i$. This situation continues until v_i reaches its peak value V_p . Beyond the peak, as v_i decreases the diode becomes reverse biased and the output voltage remains constant at the value V_p . In fact, theoretically speaking, the capacitor will retain its charge and hence its voltage indefinitely, because there is no way for the capacitor to discharge. Thus the circuit provides a dc voltage output equal to the peak of the input sine wave. This is a very encouraging result in view of our desire to produce a dc output.

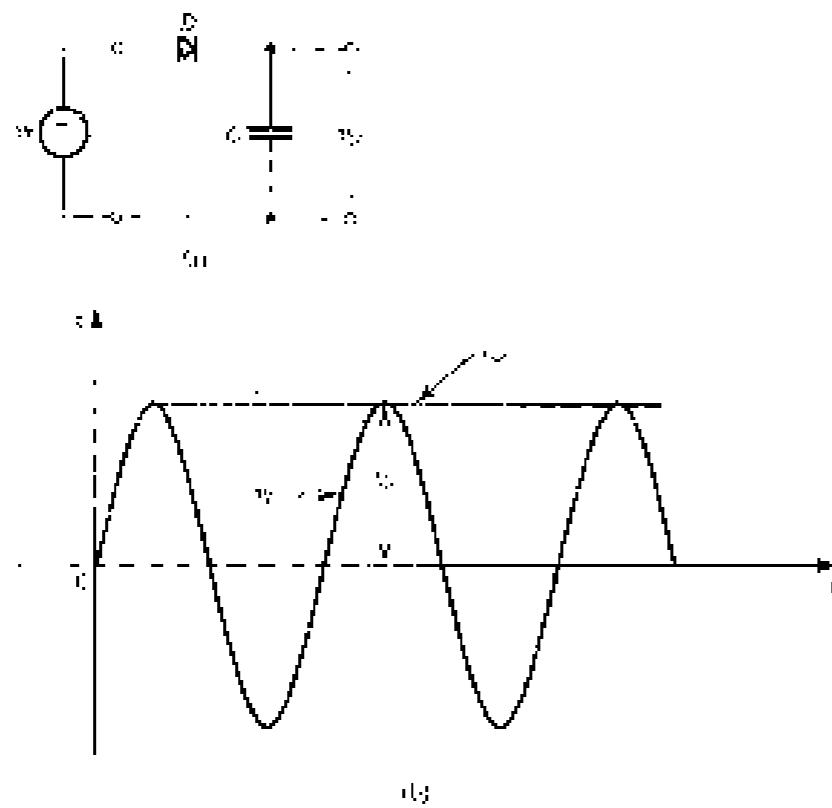


FIGURE 3.28 (a) A simple circuit used to illustrate the effect of a filter or peak rectifier and output voltage assuming an ideal diode. Notice that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a peak rectifier or peak detector.

Next, we consider the more practical situation where a load resistance R is connected across the capacitor C , as depicted in Fig. 3.29(a). However, we will continue to assume the diode to be ideal. As before, for a sinusoidal input, the capacitor charges to the peak of the input V_i . Then the diode cuts off, and the capacitor discharges through the load resistance R . The capacitor discharge will continue for almost the entire cycle, until the time at which it exceeds the saturation voltage. Then the diode turns on again and charges the capacitor up to the peak of v_o , and the process repeats itself. Observe that to keep the output voltage from decreasing too much during capacitor discharge, one selects a value for C so that the time constant CR is much greater than the discharge interval.

We are now ready to analyze the circuit in detail. Figure 3.29(b) shows the steady-state input and output voltage waveforms under the assumption that $CR \gg T$, where T is the period of the input sinusoid. The waveforms of the load current

$$i_L = i_d + i_C \quad (3.23)$$

and of the diode current (when it is conducting)

$$i_D = i_d + i_C \quad (3.24)$$

$$= C \frac{dv_o}{dt} - i_C \quad (3.25)$$

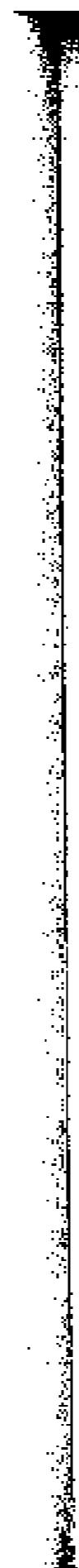


FIGURE 3.29 Voltage and current waveforms in the half-rectifier circuit with $CR \gg T$. The diode is assumed ideal.

are shown in Fig. 3.29(c). The following observations are in order:

1. The diode conducts for a brief interval, Δt_1 , near the peak of the input sinusoid and supplies the capacitor with charge equal to that lost during the much longer discharge interval. The latter is approximately equal to the period T .
2. Assuming an ideal diode, the diode conduction begins at time t_{d1} at which the input v_i equals the exponentially decaying output v_o . Conduction ceases at t shortly after the peak of v_o ; the exact value of t_2 can be determined by setting $i_d = 0$ in Eq. (3.25).

3. During the diode-off interval, the capacitor C discharges through R and thus v_2 decays exponentially with a time constant CR . The discharge interval begins just past the peak of v_2 . At the end of the discharge interval, which lasts for almost the entire period T , $v_{2p} = V_o - V_r$, where V_r is the peak-to-peak ripple voltage. When $CR \gg T$, the value of V_r is small.
4. When V_r is small, v_2 is a near constant and equal to the peak value of v_2 . Thus the output voltage is approximately equal to V_o . Similarly, the current i_2 is a near constant, and its dc component I_{2d} is given by

$$I_{2d} = \frac{V_o}{R} \quad (3.26)$$

If desired, a more accurate expression for the output dc voltage can be obtained by taking the average of the extreme values of v_{2p} :

$$V_{oA} = V_o - \frac{1}{2}V_r \quad (3.27)$$

With these observations in mind, we now derive expressions for V_r and for the average and peak values of the diode current. During the diode-off interval, v_2 can be expressed as

$$v_2 = V_o e^{-t/T_{RC}}$$

At the end of the discharge interval we have

$$V_r = V_o = V_o e^{-T_{RC}}$$

Now, since $CR \gg T$, we can use the approximation $e^{-T_{RC}} \approx 1 - T_{RC}/CR$ to obtain

$$V_r = V_o \frac{T}{CR} \quad (3.28)$$

We observe that to keep V_r small we must select a capacitance C so that $CR \gg T$. The ripple voltage V_r in Eq. (3.28) can be expressed in terms of the frequency $f = 1/T$ as

$$V_r = \frac{V_o}{fCR} \quad (3.28a)$$

Using Eq. (3.28a) we can express V_r by the alternate expression

$$V_r = \frac{I_d}{fC} \quad (3.28b)$$

Note that an alternative interpretation of the approximation made above is that the capacitor discharges by means of a constant current $I_d = V_o/R$. This approximation is valid as long as $V_r \ll V_o$.

Using Fig. 3.28(b) and assuming that diode conduction ceases almost at the peak of i_2 , we can determine the conducting interval Δt from

$$V_o \cos(\omega_d t) = V_o - V_r$$

where $\omega_d = 2\pi f = 2\pi/\tau$ is the angular frequency of i_2 . Since $\omega_d \Delta t$ is a small angle, we can employ the approximation $\cos(\omega_d \Delta t) \approx 1 - (\omega_d \Delta t)/2$ to obtain

$$\omega_d \Delta t \approx \sqrt{2}V_r/V_o \quad (3.29)$$

We note that when $V_r \ll V_o$, the conduction angle $\omega_d \Delta t$ will be small, as expected.

To determine the average diode current during conduction, i.e., we require the charge that the diode supplies to the capacitor:

$$Q_{2con} = I_{2d} \Delta t$$

where, from Eq. (3.24),

$$I_{2d} = I_{2p} - I_d$$

is the charge that the capacitor loses during the discharge interval.

$$Q_{2p} = CV_o$$

to obtain, using Eqs. (3.20) and (3.28a),

$$I_{2d} = I_d(1 + \pi\sqrt{2V_r/V_o}) \quad (3.30)$$

Observe that when $V_r \ll V_o$, the average diode current during conduction is much greater than the dc bias current. This is not surprising, since the diode conducts for a very short interval and must replenish the charge lost by the capacitor during the much longer interval in which it is discharged by I_d .

The peak value of the diode current, I_{2p} , can be determined by evaluating the expression in Eq. (3.25) at the onset of diode conduction. That is, at $t = t_1 = -\Delta t$ (where $t = 0$ is i_2 at the peak). Assuming that i_2 is almost constant at the value given by Eq. (3.28), we obtain

$$I_{2p} = I_d(1 - 2\pi\sqrt{2V_r/V_o}) \quad (3.31)$$

From Eqs. (3.30) and (3.31), we see that for $V_r \ll V_o$, $I_{2p} \approx 3I_{2d}$, which concludes with the fact that the waveform of i_2 is almost a right-angle triangle (see Fig. 3.29a).

PROBLEMS

Consider a peak rectified half-wave filtered having a peak value $V_o = 100$ V. Let the load resistance $R = 10$ ohms. Find the value of the capacitance C that will result in a peak-to-peak ripple of 2 V. Also, calculate the fraction of the cycle during which the diode is conducting and the average and peak values of the diode current.

Solution

From Eq. (3.28a) we obtain the value of C as

$$C = \frac{V_r}{V_o f R} = \frac{2}{2 \times 50 \times 10 \times 10} = 83.3 \mu F$$

The conduction angle $\omega_d \Delta t$ is found from Eq. (3.29) as

$$\omega_d \Delta t = \sqrt{2} \times 2/100 = 0.2 \text{ rad}$$

Thus the diode conducts for $(0.2/2\pi) \times 100 = 3.18\%$ of the cycle. The average diode current is obtained from Eq. (3.30), where $I_d = 100/10 = 10$ mA, as

$$I_{2d} = 10(1 + \pi\sqrt{2 \times 100/100}) = 32.1 \text{ mA}$$

The peak diode current is found using Eq. (3.31):

$$I_{2p} = 10(1 - 2\pi\sqrt{2 \times 100/100}) = 61.6 \text{ mA}$$

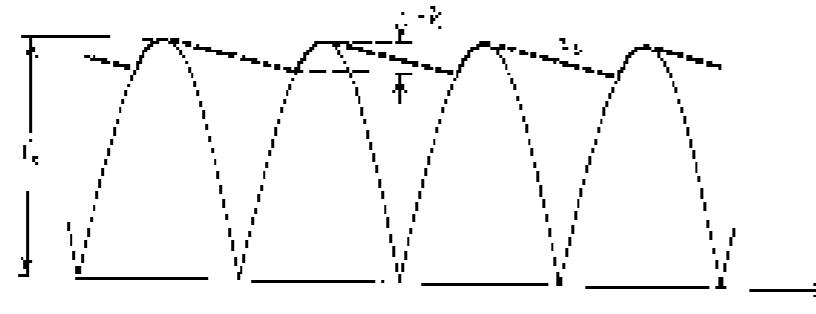


FIGURE 3.30 Waveforms in the full-wave peak rectifier.

The circuit of Fig. 3.29c, known as a half-wave peak rectifier, has the half-wave rectifier circuits of Figs. 3.26(a) and 3.27(a) can be converted to peak rectifiers by replacing a capacitor across the load resistor. As in the half-wave case, the output dc voltage will be almost equal to the peak value of the input sine wave (Fig. 3.30). The ripples frequency, however, will be twice that of the input. The peak-to-peak ripple voltage, for this case, can be derived using a procedure identical to that above but with the discharge period T replaced by $T/2$, resulting in

$$V_r = \frac{V_s}{2\sqrt{CR}} \quad (3.36)$$

While the diode conduction interval, Δt , will still be given by Eq. (3.50), the average and peak currents in each of the diodes will be given by

$$I_{av} = I_0(1 + \pi\sqrt{C/R}/2V_s) \quad (3.37)$$

$$I_{max} = I_0(1 + 2\pi\sqrt{C/R}/2V_s) \quad (3.38)$$

Comparing these expressions with the corresponding ones for the half-wave case, we note that for the same values of V_s , C , R , and V_d (and thus the same I_0), we need a capacitive load three times that required in the half-wave rectifier. Also, the current in each diode in the full-wave rectifier is approximately half that which flows in the diode of the half-wave circuit.

The analysis above assumed ideal circuits. The accuracy of the results can be improved by taking the diode voltage drop into account. This can be easily done by replacing the peak voltage V_s to which the capacitor charges with $(V_s - V_{d0})$ for the half-wave circuit and the full-wave circuit using a center-tapped transformer and with $(V_s - 2V_{d0})$ for the bridge rectifier case.

We conclude this section by noting that peak-rectifier circuits find application in signal-processing systems where it is required to detect the peak of an input signal. In such a case, the circuit is referred to as a peak detector. A particularly popular application of the peak detector is in the design of a demodulator for amplitude-modulated (AM) signals. We shall not discuss this application further here.

3.5.4 Other Rectifier Circuits with Diode Application One of the most common applications of the diode is in the half-wave rectifier circuit shown in Fig. 3.26(a). The output voltage is given by Eq. (3.26). If the diode is replaced by a zener diode, the output voltage will be constant at the zener voltage. This has important applications in power-supply design. The zener diode is also used in the design of precision rectifiers.

3.5.5 Precision Half-Wave Rectifier—The Super Diode⁴

The rectifier circuits studied thus far suffer from having one or two diode drops in the signal path. Thus, these circuits work well only when the signal to be rectified is much larger than the voltage drop of a conducting diode (0.7 V or so). In such a case, the details of the diode forward characteristics or the exact value of the diode voltage do not play a prominent role in determining circuit performance. This is indeed the case in the application of rectifier circuits in power-supply design. There are other applications, however, where the signal to be rectified is small (e.g., on the order of 100 mV or so) and thus clearly insufficient to turn on a diode. Also, in instrumentation applications, the need arises for rectifier circuits with very precise and predictable transfer characteristics. For these applications, a class of circuits has been developed utilizing op amps (Chapter 2) together with diodes to provide precision rectification. In the following discussion, we study one such circuit, leaving a more comprehensive study of op amp-based circuits to Chapter 12.

Figure 3.31(a) shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an op amp, with R being the rectifier load resistance. The op amp, of course, needs power supplies for its operation, but simplicity, V_{DD} and V_{SS} , are not shown in the circuit diagram. The circuit works as follows: If v_s goes positive, the output voltage v_o of the op amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op amp's output terminal and the negative input terminal.

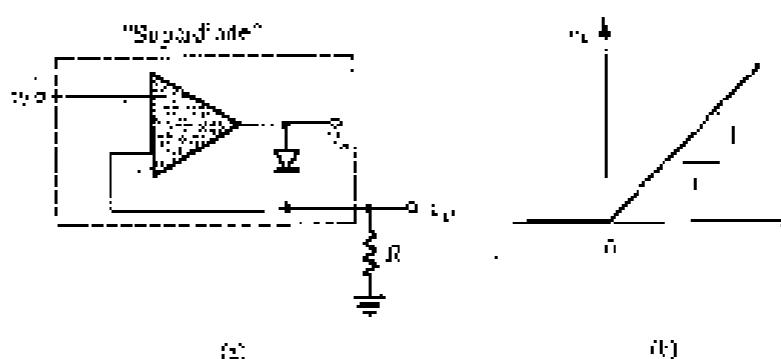


FIGURE 3.31 The "superdiode" precision half-wave rectifier and its almost-ideal transfer characteristic. $V_{DD} = 10$ V, $V_{SS} = 0$, and the diode symbol is the op-amp supply-side load curve, and the source is a current $I_0 = 1$ mA. Note that the op-amp power supply V_{DD} shows a low-side power supply.

⁴This section requires knowledge of operational amplifiers.

This negative feedback path will cause a virtual short circuit to appear between the two input terminals. Thus the voltage at the negative input terminal, which is also the output voltage v_o , will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage v_i .

$$v_o = v_i \quad (v_o > 0)$$

Note that the offset voltage (~ 0.6 V) exhibited in the simple full-wave rectifier circuit of Fig. 3.25 is no longer present. For the op-amp circuit to stay operational, v_i has to exceed only a negligibly small voltage equal to the diode drop divided by the op-amp's open-loop gain. In other words, the straight-line transfer characteristic v_o vs. v_i almost passes through the origin. This makes this circuit suitable for applications involving very small signals.

Consider now the case when v_i goes negative. The op-amp's output voltage v_o will tend to follow and go negative. This will reverse-bias the diode, and no current will flow through resistance R , causing v_o to remain equal to 0 V. Thus, for $v_i < 0$, $v_o = 0$. Since in this case the diode is off, the op-amp will be operating in an open-loop fashion, and its output will be at the negative saturation level.

The transfer characteristic of this circuit will be that shown in Fig. 3.31(B), which is almost identical to the ideal characteristic of a half-wave rectifier. The diode's diode characteristics have been almost completely masked by placing the diode in the negative feedback path of an op-amp. This is another dramatic application of negative feedback, a subject we will study formally in Chapter 8. The combination of diode and op-amp, shown in the device box in Fig. 3.31(n), is appropriately referred to as a "superdiode."

EXERCISES

- 3.21 Consider the operational amplifier circuit shown in Fig. 3.31(a), with $V_{DD} = 12$ V, $V_{SS} = -12$ V, and $V_T = 0.6$ V. Calculate the output voltage of the circuit if the input voltage is $v_i = 10$ mV. Assume that the op-amp has a load resistance of $2 k\Omega$ and a voltage gain of 10^4 . The diode has a diode voltage of 0.6 V, and the voltage step changes by 10^{-3} V per decade of current change. Assume that the diode current is $I_D = 10^{-10} \text{ A} / (0.6 \text{ V} / 10^{-3} \text{ V})^{1.3} / 10^4$. Hint: diode I_D decreases as v_o increases, and the transfer characteristic is a function of v_o .
- 3.22 For the circuit of Fig. 3.31(a), assume that $v_i = 10$ mV. Calculate the output voltage v_o if the diode current is $I_D = 10^{-10} \text{ A} / (0.6 \text{ V} / 10^{-3} \text{ V})^{1.3} / 10^4$. Hint: the diode current is $I_D = 10^{-10} \text{ A} / (0.6 \text{ V} / 10^{-3} \text{ V})^{1.3} / 10^4$.

3.6 LIMITING AND CLAMPING CIRCUITS

In this section, we shall present additional nonlinear circuit applications of diodes.

3.6.1 Limiter Circuits

Figure 3.32 shows the general transfer characteristic of a limiter circuit. As indicated, the circuit is a **clamper** if $L_+/K < L_-/K$; the former acts as a limiter circuit providing an output proportional to the input, $v_o = K v_i$. Although in general, K can be greater than 1, the circuits discussed in this section have $K \leq 1$ and are known as **soft** vs. **hard** limiters. (Examples of active limiters will be presented in Chapter 13.) If v_i exceeds the upper threshold (L_+/K), the output voltage is limited or clamped to the upper limiting level, L_+ . On the other hand, if v_i is reduced below the lower limiting threshold (L_-/K), the output voltage v_o is limited to the lower limiting level, L_- .

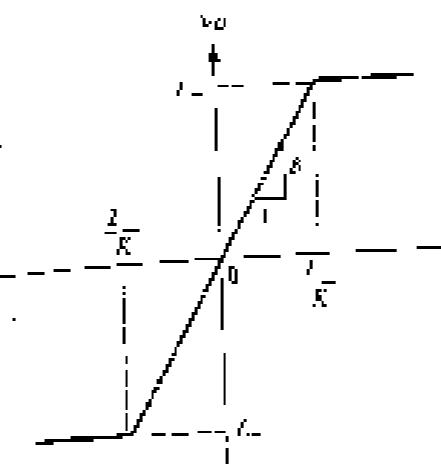


FIGURE 3.32 General transfer characteristic of a limiter circuit.

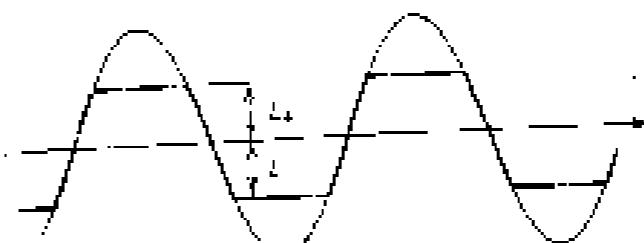


FIGURE 3.33 Applying a sine wave to a limiter circuit (just two periods).

The general transfer characteristic of Fig. 3.32 describes a **double limiter**, that is, a limiter that works on both the positive and negative portions of any waveform. Single limiter circuits exist. Finally, note that if an input wave form such as that shown in Fig. 3.33 enters a double limiter, its two peaks will be clipped off. Limiters therefore are often referred to as **clippers**.

The transfer characteristic depicted in Fig. 3.32 is described as a **hard limiter**. Hard limiting is characterized by immediate transitions between the linear regions and the saturation regions and is *steps* greater than zero in the saturation regions, as illustrated in Fig. 3.34. Depending on the application, either hard or soft limiting may be preferred.

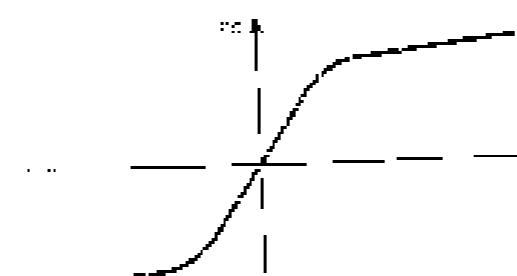


FIGURE 3.34 Soft limiter.

Limiters find application in a variety of signal-processing systems. One of their simplest applications is in limiting the voltage between the two input terminals of an op amp to a value lower than the breakdown voltage of the transistors that make up the input stage of the op-amp circuit. We will have more to say on this and other limiter applications at the end of this book.

Diodes can be combined with resistors to provide simple realizations of the limiter function. A number of examples are depicted in Fig. 3.35. In each case of the figure both the circuit and its transfer characteristic are given. The transistor characteristics are obtained using the constant-voltage-droop ($V_0 = 0.7$ V) diode model but assuming a smooth transition between the linear and saturation regions of the transfer characteristics. Better approximations for the transfer characteristics can be obtained using the piecewise-linear diode model. If this is done, the saturating region of the characteristic acquires a slight slope (due to the effect of V_0).

The circuit in Fig. 3.35(a) is that of the half-wave rectifier except that here the outputs are taken across the diode. For $v_i < 0.5$ V, the diode is cut off, no current flows, and the voltage

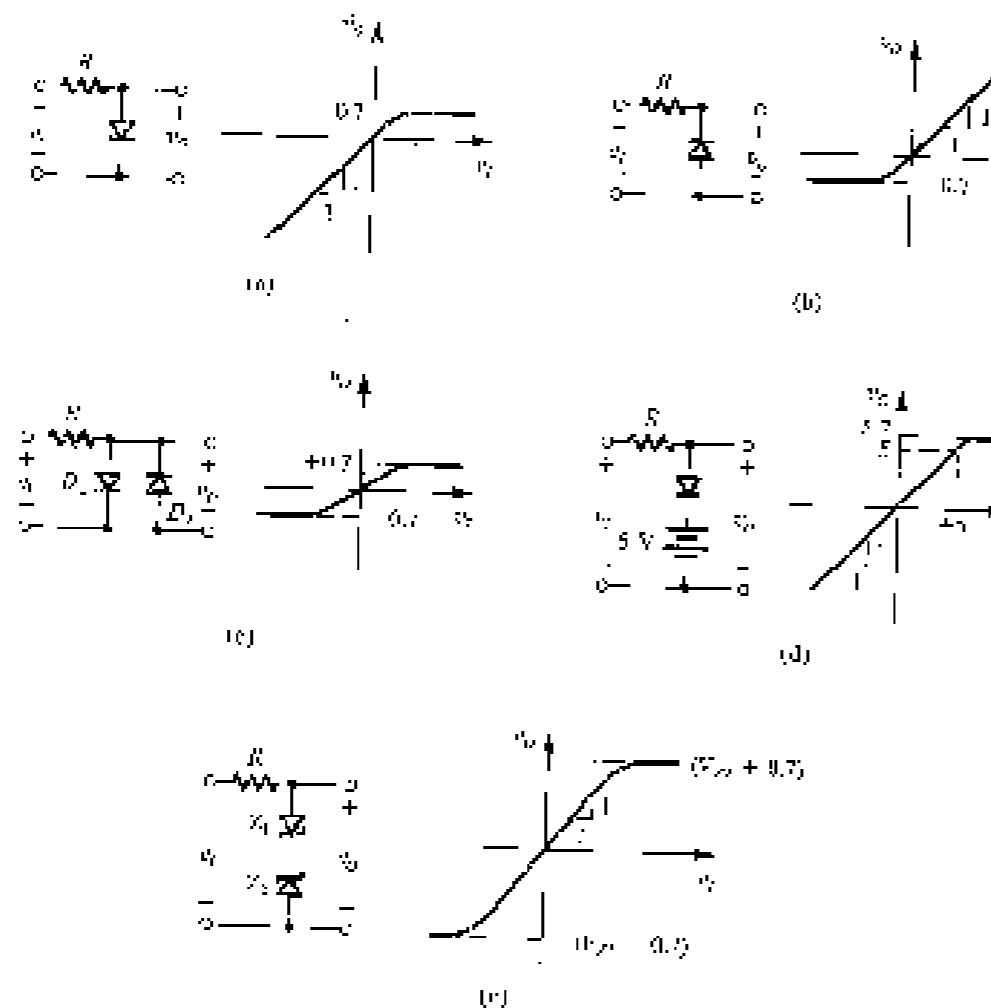


FIGURE 3.35 A variety of basic limiting circuits.

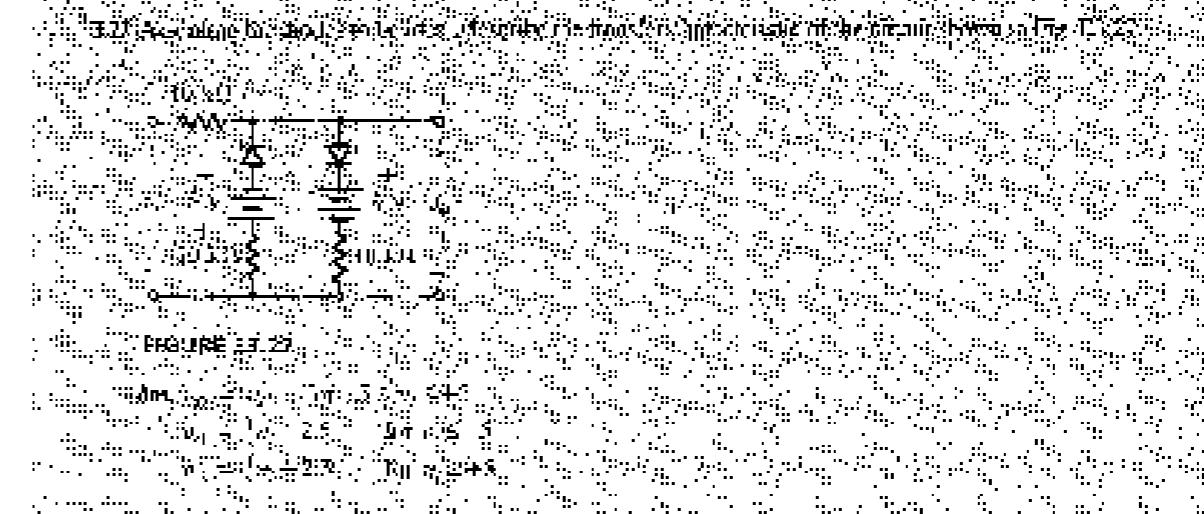
drop across it is zero; thus $v_o = v_i$. As v_i exceeds 0.5 V, the diode turns on, eventually limiting v_o up to the diode drop (0.7 V). The circuit of Fig. 3.35(a) is similar to that in Fig. 3.35(b) except that the diode is reversed.

Diode limiting can be implemented by placing two diodes of opposite polarity in parallel, as shown in Fig. 3.35(c). Here the linear region of the characteristic is obtained for $-0.5 \leq v_i < 0.5$ V. For this range of v_i , both diodes are off and $v_o = v_i$. As v_i exceeds 0.5 V, D_1 turns on and eventually limits v_o to 0.7 V. Similarly, as v_i goes more negative than -0.5 V, D_2 turns on and eventually limits v_o to -0.7 V.

The thresholds and saturation levels of diode limiters can be controlled by using strings of diodes either by connecting a dc voltage in series with the diode(s). The latter idea is illustrated in Fig. 3.35(d). Finally, rather than strings of diodes, we may use two zener diodes in series, as shown in Fig. 3.35(e). In this circuit, cutting occurs in the positive direction at a voltage of $V_Z + 0.7$, where 0.7 V represents the voltage drop across zener diode D_2 when conducting in the forward direction. The negative form of Z_2 acts as a zener, while Z_1 conducts in the forward direction. It should be mentioned that pairs of zener diodes connected in series are available commercially for applications of this type under the name double-zener zener.

More flexible limiter circuits are possible if op amps are combined with diodes and resistors. Examples of such circuits are discussed in Chapter 14.

EXERCISE



3.6.2 The Clamped Capacitor or DC Restorer

If in the basic zener limiter circuit the output is taken across the diode, rather than across the capacitor, an interesting circuit with important applications results. The circuit, called a dc restorer, is shown in Fig. 3.36 fed with a square wave. Because of the polarity in which the diode is connected, the capacitor will charge to a voltage v_C with the polarity indicated in Fig. 3.36 and equal to the magnitude of the most negative peak of the input signal. Subsequently, the diode turns off and the capacitor retains its voltage indefinitely. If, for instance, the input square wave has the arbitrary levels -6 V and +1 V, then v_C will be equal to 6 V.

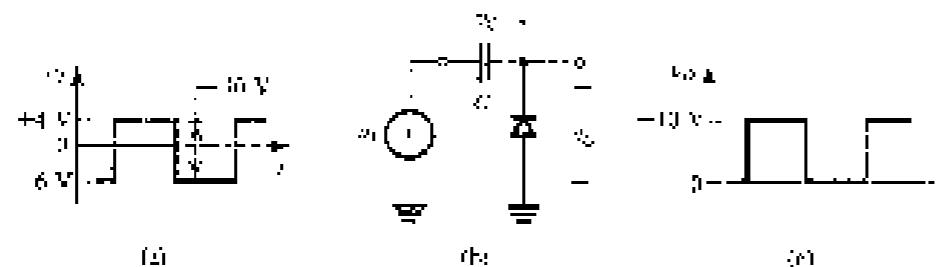


FIGURE 3.36 The clamped capacitor circuit with a square wave input and no load.

Now, since the output voltage \$v_o\$ is given by

$$v_o = v_i - v_d$$

it follows that the output waveform will be identical to that of the input, except that it is shifted upward by \$v_d\$ volts. In our example the output will thus be a square wave with levels of 6 V and -10 V.

Another way of visualizing the operation of the circuit in Fig. 3.36 is to note that because the diode is connected across the output with the polarity shown, it prevents the output voltage from going below 0 V by conducting and charging up the capacitor, thus causing the output to rise to 0 V, but this connection will not constrain the positive excursion of \$v_o\$. The output waveform will therefore have its lowest peak clamped at 0 V, which is why the circuit is called a clamped capacitor. It should be obvious that reversing the diode polarity will provide an output waveform whose highest peak is clamped to 0 V. In either case, the output waveform will have a finite average value or dc component. This dc component is easily attributed to the average value of the input waveform. As an application, consider a pulse signal being transmitted through a capacitive-coupled or re-coupled system. The capacitive coupling will cause the pulse train to lose whatever dc component it originally had. Passing the resulting pulse wave train to a clamping circuit provides it with a well-determined dc component, a process known as de restoration. This is why the circuit is also called a dc restorer.

Restoration is useful because the dc component or average value of a pulse waveform is an effective measure of its duty cycle.² The duty cycle of a pulse waveform can be modulated (i.e., a process called pulsedwidth modulation) and made to carry information. In such a system, detection or demodulation could be achieved simply by feeding the received pulse waveform to a detector and then using a simple \$RC\$ low-pass filter to separate the average of the output waveform from the superimposed pulses.

When a load resistance \$R\$ is connected across the diode in a clamping circuit as shown in Fig. 3.37, the situation changes significantly. While the output is above ground, a result current must flow in \$R\$. Since at this time the diode is off, this current obviously comes from the capacitor, thus causing the capacitor to discharge and the output voltage to fall. This is shown in Fig. 3.37 for a square-wave input. During the interval \$t_0\$ to \$t_1\$, the output voltage falls exponentially with time constant \$CR\$. At \$t_1\$ the input decreases by \$V_1\$ volts, and the output attempts to follow. This causes the diode to conduct heavily and to quickly charge the capacitor. At the end of the interval \$t_1\$ to \$t_2\$, the output voltage would normally be a few tenths of a volt negative (e.g., -0.5 V). Then, as the input rises by \$V_2\$ volts (at \$t_2\$), the output follows, and the cycle repeats itself. In the steady state the charge lost by the capacitor during

²The duty cycle of a pulse waveform is the proportion of each cycle occupied by the pulse. In other words, it is the pulse width expressed as a fraction of the pulse period.

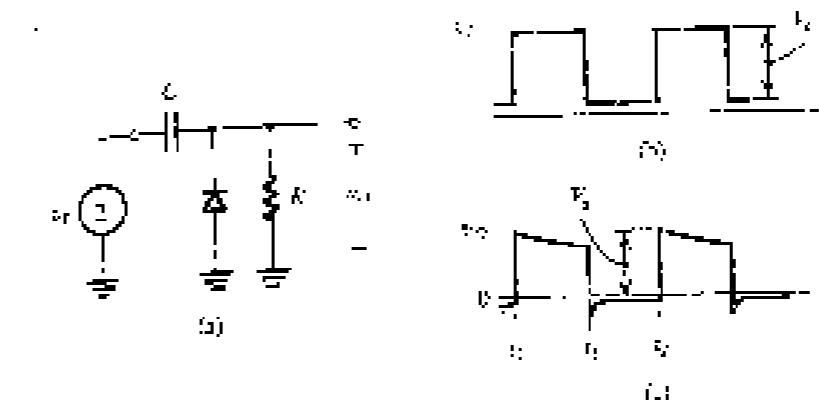


FIGURE 3.37 The clamped capacitor with a load resistor \$R\$.

the interval \$t_0\$ to \$t_1\$ is recovered during the interval \$t_1\$ to \$t_2\$. This charge equilibrium enables us to calculate the average diode current as well as the details of the output waveform.

3.6.3 The Voltage Doubler

Figure 3.38(a) shows a circuit composed of two sections in cascade: a clapper formed by \$D_1\$ and \$D_2\$, and a peak rectifier formed by \$D_3\$ and \$C_1\$. When excited by a sinusoid of amplitude \$V_0\$, the clapping section provides the voltage waveform shown, assuming ideal diodes. In \$V_p\$, the clapping section, provides the voltage waveform shown, assuming ideal diodes. In Fig. 3.38(b), note that while the positive peaks are charged to 0 V, the negative peak

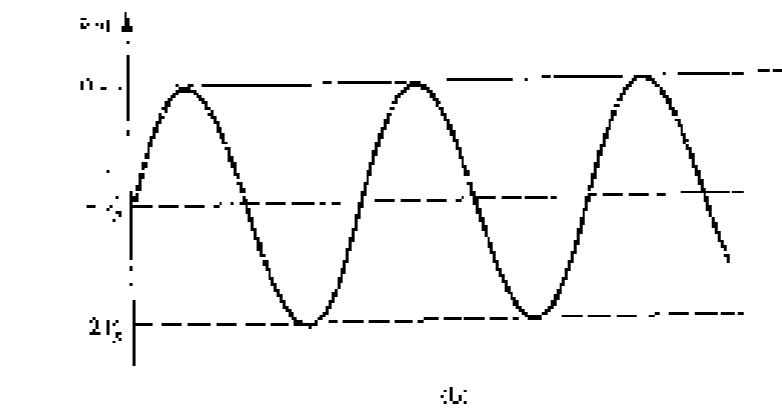
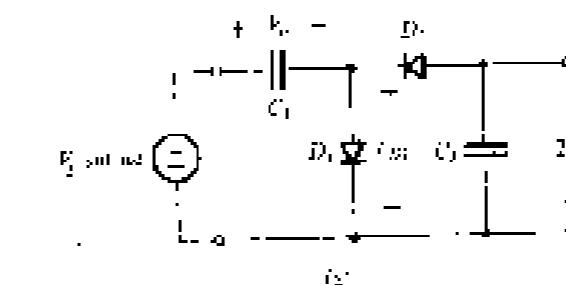


FIGURE 3.38 Voltage-doubler circuit. (b) waveform of the voltage across \$C_1\$.

reaches $-2V$. In response to this waveform, the peak-detector section provides across capacitor C_2 a negative dc voltage of magnitude $2V_p$. Because the output voltage is double the input peak, the circuit is known as a voltage doubler. The technique can be extended to provide output dc voltages that are higher multiples of V_p .

EXERCISE

Suppose the circuit of Fig. 3.36 is referenced to ground, with the dc component of V_s being zero. If the peak-to-peak value of V_s is 10 mV , determine the peak-to-peak value of V_o .

3.7 PHYSICAL OPERATION OF DIODES

Having studied the terminal characteristics and circuit applications of junction diodes, we will now briefly consider the physical processes that give rise to the observed terminal characteristics. The following treatment of device physics is somewhat simplified; nevertheless, it should provide sufficient background for a fuller understanding of diodes and for understanding the operation of transistors in the following two chapters.

3.7.1 Basic Semiconductor Concepts

The pn junction. The semiconductor diode is basically a pn junction, as shown in Fig. 3.39. As indicated, the pn junction consists of p -type semiconductor material (e.g., silicon) brought into close contact with n -type semiconductor material (also silicon). In actual practice, both the p and n regions are part of the same silicon crystal; that is, the pn junction is formed within a single silicon crystal by creating regions of different "doping" (p and n regions). Appendix A provides a brief description of the process employed in the fabrication of pn junctions. As indicated in Fig. 3.39, external wire connections to the p and n regions (i.e., diode terminals) are made through metal (interconnect) contacts.

In addition to being essentially a diode, the pn junction is the basic element of bipolar junction transistors (BJTs) and plays no insignificant role in the operation of field-effect transistors (FETs). Thus an understanding of the physical operation of pn junctions is important to the understanding of the operation and terminal characteristics both of diodes and transistors.

Intrinsic Silicon. Although silicon or germanium can be used to manufacture most semiconductor devices—indeed, earlier diodes and transistors were made of germanium—but today's

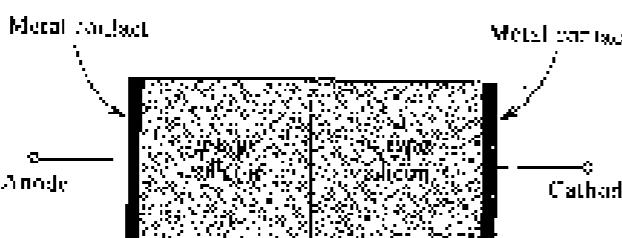


FIGURE 3.39 Simplified physical structure of the junction diode. Terminal geometries are given in Appendix A.3.

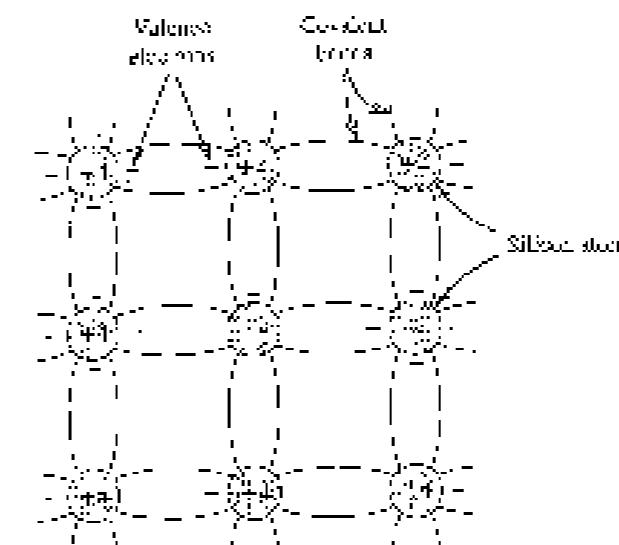


FIGURE 3.40 Two-dimensional representation of the silicon crystal. Atoms represent the valence electrons of silicon, and $+1q$ is a positive charge of $-1q$, which is neutralized by the charge of 2e from valence electrons. Observe how the coupling between is formed by sharing of the valence electrons. At 0 K, all bonds are intact so no free electrons are available for conduction.

integrated-circuit technology is based almost entirely on silicon. For this reason, we will deal mostly with silicon devices throughout this book.¹⁰

A crystal of pure or intrinsic silicon has a regular lattice structure where the atoms are held in their positions by bonds, called covalent bonds, formed by the four valence electrons associated with each silicon atom. Figure 3.40 shows a two-dimensional representation of such a structure. Observe that each atom shares each of its four valence electrons with a neighboring atom, with each pair of electrons forming a covalent bond. At sufficiently low temperatures, all covalent bonds are intact and no (or very few) free electrons are available to conduct electric current. However, at room temperature, some of the bonds are broken by thermal ionization and some electrons are freed. As shown in Fig. 3.41, when a covalent bond is broken, an electron leaves its parent atom, thus a positive charge, equal to the magnitude of the electron charge, is left with the parent atom. An electron from a neighboring atom may be attracted to the positive charge, leaving its parent atom. This action fills up the "hole" that existed in the parent atom but creates a new hole in the other atom. This process may repeat itself, with the result that we effectively have a positively charged carrier, or hole, moving through the silicon crystal structure and being available to conduct electric current. The charge of a hole is equal in magnitude to the charge of an electron.

Thermal ionization results in free electrons and holes in equal numbers and hence equal concentrations. These free electrons and holes move randomly through the silicon crystal structure, and in the process, some electrons may fill some of the holes. This process, called recombination, results in the disappearance of free electrons and holes. The recombination rate is proportional to the number of free electrons and holes, which, in turn, is determined by

¹⁰ An exception is the subject of gallium arsenide (GaAs) structures, which though not covered in this edition of the book, is studied in more detail in the additional material on the text website and on the CD accompanying the text.

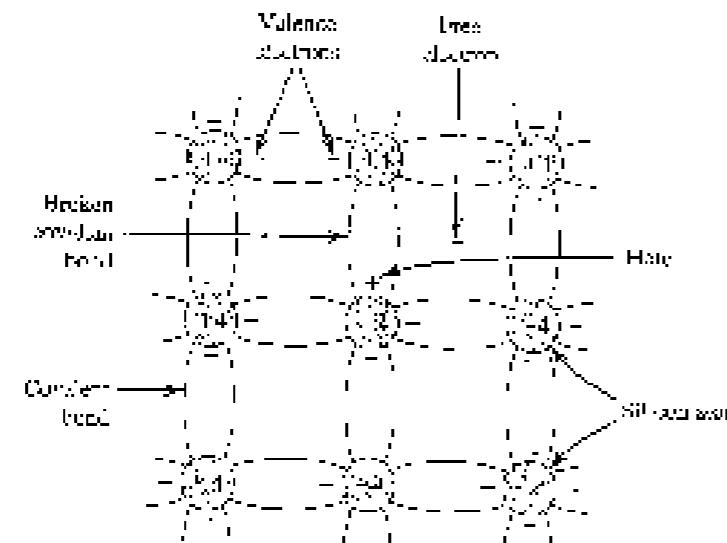


FIGURE 3.41 At room temperature, some of the covalent bonds are broken by thermal ionization. Each broken bond gives rise to one electron and one hole, each of which may be available for current conduction.

The ionization rate, the ionization rate is a linear function of temperature. In thermal equilibrium, the recombination rate is equal to the ionization or thermal-generation rate, and one can calculate the concentrations of free electrons n , which is equal to the concentration of holes p ,

$$n = p = n_i$$

where n_i denotes the equilibrium of free electrons or holes in intrinsic silicon at a given temperature. Study of semiconductor physics shows that at an absolute temperature T (in kelvin), the intrinsic concentration n_i , i.e., the number of free electrons and holes per cubic centimeter, can be found from

$$n_i^2 = B T^3 e^{-E_g/2kT} \quad (3.36)$$

where B is a material-dependent parameter = 5.4×10^3 for silicon, E_g is a parameter known as the bandgap energy = 1.12 electron-volts (eV) for silicon, and k is Boltzmann's constant = 8.63×10^{-5} eV/K. Although we shall not make use of the bandgap energy in this chapter (or introductory exposition), it is interesting to note that E_g represents the minimum energy required to break a covalent bond and thus generate an electron-hole pair. Substitution in Eq. (3.36) of the parameter values given shows that the intrinsic silicon at room temperature ($T = 300\text{ K}$), $n_i = 1.5 \times 10^{10}$ carriers/cm³. To place this number in perspective, we note that the silicon crystal has about 5×10^{22} atoms/cm³. Thus, at room temperature, only one of every billion atoms is ionized!

Finally, it should be mentioned that the reason that silicon is called a semiconductor is that its conductivity, which is determined by the number of charge carriers available to conduct electric current, is between that of conductors (e.g., metals) and that of insulators (e.g., glass).

Diffusion and Drift There are two mechanisms by which holes and electrons move through a silicon crystal—diffusion and drift. Diffusion is associated with random motion due to thermal statistics. In a piece of silicon with uniform concentrations of free electrons

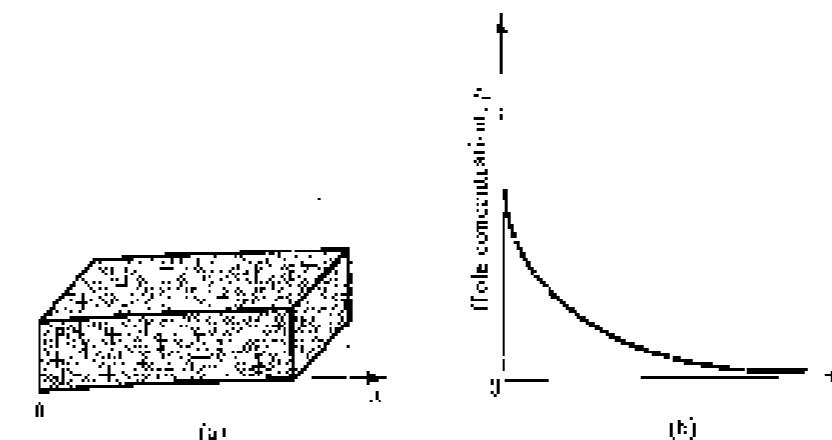


FIGURE 3.42 (a) Bar of silicon in which the hole concentration profile shown in (b) has been established along the x -axis by some unspecified mechanism.

and gives the random motion does not result in a net flow of charge (i.e., current). On the other hand, if by some mechanism the concentration of, say, free electrons is made higher in one part of the piece of silicon than in another, then electrons will diffuse from the region of high concentration to the region of low concentration. This diffusion process gives us a net flow of charge, or diffused current. As an example, consider the bar of silicon shown in Fig. 3.42(a), in which the hole concentration profile shown in Fig. 3.42(b) has been established along the x -axis by some unspecified mechanism. The existence of such a concentration profile results in a hole diffusion current I_h in the x direction, with the magnitude of the current at any point being proportional to the slope of the carrier-trace curve (or the concentration gradient) at that point,

$$I_h = -q D_h \frac{dn}{dx} \quad (3.37)$$

where I_h is the current density (i.e., the current per unit area of the plane perpendicular to the x axis in A/cm²), q is the magnitude of electron charge = 1.6×10^{-19} C, and D_h is a constant called the diffusion constant or diffusivity of holes. Note that the gradient (dn/dx) is negative, resulting in a positive current in the x direction, as should be expected. In the case of electron diffusion resulting from an electron concentration gradient, a similar relationship applies, giving the electron-current density

$$I_e = +q D_e \frac{dp}{dx} \quad (3.38)$$

where D_e is the diffusivity of electrons. Observe that a negative (dp/dx) gives rise to a negative current & result of the convention that the positive direction of current is taken to be that of the flow of positive charge (and opposite to that of the flow of negative charge). For holes and electrons diffusing in intrinsic silicon, typical values for the diffusion constants are $D_h = 12\text{ cm}^2/\text{s}$ and $D_e = 34\text{ cm}^2/\text{s}$.

The other mechanism for carrier transport in semiconductors is drift. Carrier drift occurs when an electric field is applied across a piece of silicon. Free electrons and holes are accelerated by the electric field and acquire a velocity component (superimposed on the velocity of their thermal motion) called drift velocity. If the electric field strength is denoted

E in V/m , the positively charged holes will drift in the direction of E and acquire a velocity $v_{h,i}$ in a crystal given by

$$v_{h,i} = \mu_h E \quad (3.40a)$$

where μ_h is a constant called the mobility of holes which has the units of $\text{cm}^2/\text{V}\cdot\text{s}$. For intrinsic silicon, μ_h is typically $480 \text{ cm}^2/\text{V}\cdot\text{s}$. The negatively charged electrons will drift in a direction opposite to that of the electric field, and their velocity is given by a relationship similar to that in Eq. (3.39), except that μ_h is replaced by μ_e , the electron mobility. In intrinsic silicon, μ_e is typically $1480 \text{ cm}^2/\text{V}\cdot\text{s}$, about 2.5 times greater than the hole mobility.

Consider now a silicon crystal having a hole density p_0 and a free electron density n_0 subjected to an electric field E . The holes will drift in the same direction as E , that is, in the x direction, with a velocity $v_{h,i}E$. Thus we have a positive charge of density qp_0 (electron-hole pairs) moving in the x direction with velocity $v_{h,i}E$ (current). It follows that in 1 second, a charge of qp_0EA (coulombs) will cross a plane of area A (cm^2) perpendicular to the x -axis. This is the current component caused by hole drift. Dividing by the area A gives the current density

$$J_{h,i} = qp_0 \mu_h E \quad (3.40a)$$

The free electrons will drift in the direction opposite to that of E . Thus we have a charge of density $(-np_0)$ moving in the negative x direction, and thus it has a negative velocity $(-\mu_e E)$. The result is a positive current component with a density given by

$$J_{e,i} = -qn \mu_e E \quad (3.40b)$$

The total drift current density is obtained by combining Eqs. (3.40a) and (3.40b),

$$J_{drift} = q(p\mu_h - n\mu_e)E \quad (3.40c)$$

It should be noted that this is a form of Ohm's law, with the resistivity ρ in units of $\Omega\cdot\text{cm}$, given by

$$\rho = 1/(q(p\mu_h - n\mu_e)) \quad (3.41)$$

Finally, it is worth mentioning that a similar relationship, known as the Einstein relationship, exists between the carrier diffusivity and mobility:

$$\frac{D_s}{D_n} = \frac{\mu_s}{\mu_n} = V_T \quad (3.42)$$

where V_T is the thermal voltage that we have encountered before, in the mobility relationship (see Eq. 3.11). Recall that at room temperature, $V_T \approx 25 \text{ mV}$. The reader can easily check the validity of Eq. (3.42) by substituting the typical values given above for intrinsic silicon.

Doped Semiconductors The intrinsic silicon crystal described above has equal concentrations of free electrons and holes generated by thermal ionization. These concentrations, denoted n_0 , are strongly dependent on temperature. Doped semiconductors are materials in which carriers of one kind (electrons or holes) predominate. Doped silicon in which the majority of charge carriers are the negatively charged electrons is called *n-type*, while silicon doped so that the majority of charge carriers are the positively charged holes is called *p-type*.

Doping of a silicon crystal to turn it into n-type or p-type is achieved by introducing a small number of impurity atoms. For instance, introducing impurity atoms of a pentavalent element such as phosphorus results in n-type silicon, because the phosphorus atoms that replace some of the silicon atoms in the crystal structure have five valence electrons, four of

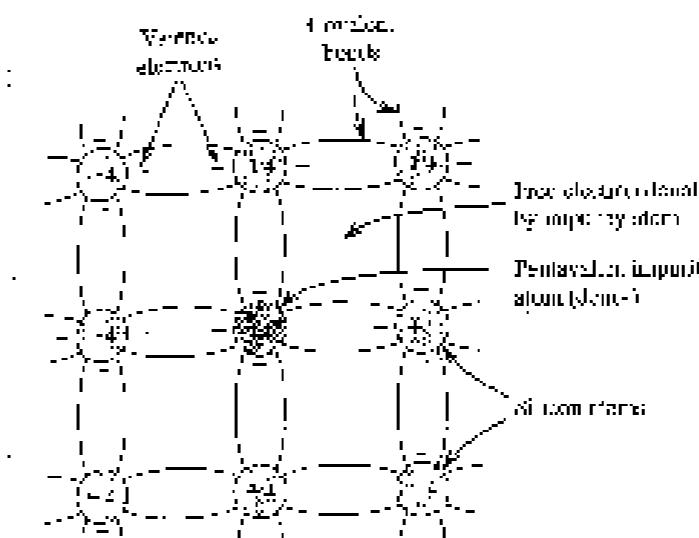


FIGURE 3.48 A silicon crystal doped with a pentavalent element. Each dopant atom donates 1 electron and is also called a donor. The doped semiconductor is an n-type.

which form bonds with the neighboring silicon atoms while the fifth becomes a free electron (Fig. 3.48). Thus each phosphorus atom donates a free electron to the silicon crystal, and the phosphorus impurity is called a donor. It should be clear enough that no holes are generated by this process; hence the majority of charge carriers in the phosphorus-doped silicon will be electrons. In fact, if the concentration of donor atoms (phosphorus) is N_d , in thermal equilibrium the concentration of free electrons in the n-type silicon, n_{eq} , will be

$$n_{eq} = N_d \quad (3.43)$$

where the additional subscript 0 denotes thermal equilibrium. From semiconductor physics, it turns out that in thermal equilibrium the product of electron and hole concentrations remains constant; that is,

$$n_{eq}p_{eq} = n_i^2 \quad (3.44)$$

Thus the concentration of holes, p_{eq} , that are generated by thermal ionization will be

$$p_{eq} = \frac{n_i^2}{N_d} \quad (3.45)$$

Since n_i is a function of temperature (Eq. 3.36), it follows that the concentration of the minority holes will be a function of temperature whereas that of the majority electrons is independent of temperature.

To produce a p-type semiconductor, silicon has to be doped with a trivalent impurity such as boron. Each of the impurity boron atoms accepts one electron from the silicon crystal, so that they may form covalent bonds in the lattice structure. Thus, as shown in Fig. 3.44, each atom gives rise to a hole, and the concentration of the majority holes in p-type silicon under thermal equilibrium is approximately equal to the concentration N_A of the acceptor (boron) impurity.

$$p_{eq} = N_A \quad (3.46)$$

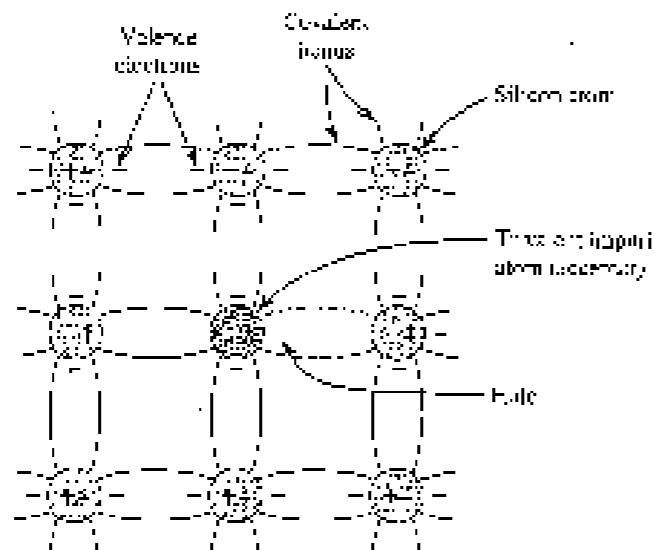


FIGURE 3.44 A silicon crystal diode with a tri-layer impurity. Each acceptor atom gives rise to one hole and one semiconductor hole carrier.

In this p -type silicon, the concentration of the minority electrons, which are generated by thermal ionization, can be calculated using the fact that the product of carrier concentrations remains constant; thus,

$$n_p n_i = \frac{N_1^2}{N_2} \quad (3.75)$$

It should be emphasized that a piece of n -type or p -type silicon is electrically neutral; the majority free carriers (electrons in n -type silicon, and holes in p -type silicon) are neutralized by bound charges associated with the impurity atoms.

EXERCISES

- 3.29. Calculate the diffusion current density J_D at $x = 10^{-5}$ m if the diffusion rate of holes in silicon is 10^{-10} m²/s and the hole concentration in the p region is 10^{16} cm⁻³. Assume that the hole concentration in the n region is 10^{10} cm⁻³.
- 3.30. Calculate the diffusion current density J_D at $x = 10^{-5}$ m if the diffusion rate of holes in silicon is 10^{-10} m²/s and the hole concentration in the p region is 10^{16} cm⁻³. Assume that the hole concentration in the n region is 10^{10} cm⁻³. The diffusion coefficient of holes in silicon is 10^{-15} m²/s.
- 3.31. Consider a silicon diode with a p -type material having a hole concentration of 10^{16} cm⁻³ and a n -type material having an electron concentration of 10^{16} cm⁻³. The diffusion coefficient of holes in silicon is 10^{-15} m²/s. If the diffusion current density is 10^{-10} A/m², calculate the diffusion length L_D .
- 3.32. Consider a silicon diode with a p -type material having a hole concentration of 10^{16} cm⁻³ and a n -type material having an electron concentration of 10^{16} cm⁻³. The diffusion coefficient of holes in silicon is 10^{-15} m²/s. If the diffusion current density is 10^{-10} A/m², calculate the diffusion length L_D .

3.7.2 The $p-n$ Junction Under Open-Circuit Conditions

Figure 3.45 shows a $p-n$ junction under open-circuit conditions—that is, the external terminals are all open. The "+" signs in the p -type material denote the majority holes. The charge-

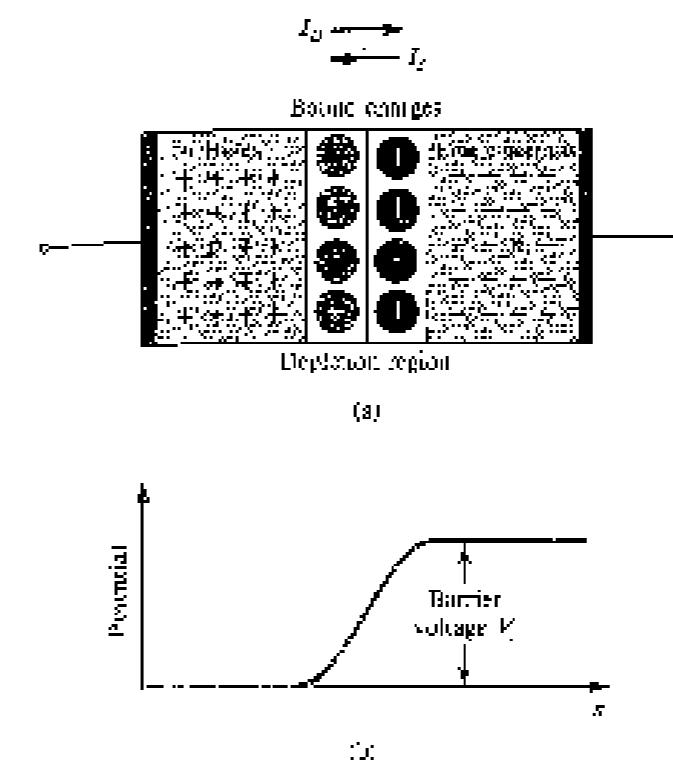


FIGURE 3.45 (a) The $p-n$ junction diode at open-circuit voltage. (b) The potential distribution along x , which is perpendicular to the junction.

of these holes is neutralized by an equal amount of bound negative charge associated with the acceptor atoms. For simplicity, these bound charges are not shown in the diagram. Also not shown are the minority electrons generated in the p -type material by thermal ionization.

In the n -type material the majority electrons are indicated by "+" signs. Here also, the bound negative charge, which neutralizes the charge of the majority electrons, is not shown. In order to keep the diagram simple, the n -type material also contains minority holes generated by thermal ionization that are not shown in the diagram.

The Diffusion Current J_D . Because the concentration of holes is high in the p region and low in the n region, holes diffuse across the junction from the p side to the n side; similarly, electrons diffuse across the junction from the n side to the p side. These two current components add together to form the diffusion current J_D , whose direction is from the p side to the n side, as indicated in Fig. 3.45.

The Depiction Region. The holes that diffuse across the junction into the n region quickly recombine with some of the majority electrons present there and thus disappear from the space. This recombination process results in the disappearance of some free electrons from the n -type material. Thus some of the bound positive charge will no longer be neutralized by free electrons, and this charge is said to have been uncovered. Since recombination takes place close to the junction, there will be a region close to the junction that is depleted of free electrons and contains an excess bound positive charge, as indicated in Fig. 3.45.

The electrons that diffuse across the junction into the p region quickly combine with some of the majority holes there, and thus disappear from the source. This results in a slight disappearance of some majority holes, causing some of the bound negative charge to be uncovered (i.e., no longer neutralized by holes). Thus, in the n material close to the junction, there will be a region depleted of holes and containing uncovered bound negative charge, as indicated in Fig. 3.45.

From the above it follows that a carrier-depletion region will exist on both sides of the junction, with the n side of this region positively charged and the p side negatively charged. The carrier-depletion region—*i.e.*, simply, depletion region—is also called the space-charge region. The charges on both sides of the depletion region cause an electric field to be established across the region; hence a potential difference results across the depletion region, with the n side at a positive voltage relative to the p side, as shown in Fig. 3.45(b). Thus the resulting electric field opposes the diffusion of holes into the n region and electrons into the p region. In fact, the voltage drop across the depletion region acts as a barrier that has to be overcome for holes to diffuse into the n region and electrons to diffuse into the p region. The larger the barrier voltage, the smaller the number of carriers that will be able to overcome the barrier and hence the lower the magnitude of diffusion current. Thus the diffusion current I_d depends strongly on the voltage drop V_0 across the depletion region.

The Drift Current I_s and Equilibrium In addition to the current component I_d , due to the drift-diffusion effect, a component due to minority-carrier drift exists across the junction. Specifically, some of the thermally generated holes in the n material diffuse through the n material to the edge of the depletion region. There, they experience the electric field in the depletion region, which sweeps them across that region, to the p side. Similarly, some of the minority thermally generated electrons in the p material diffuse to the edge of the depletion region and get swept by the electric field in the depletion region across that region into the n side. These two current components—electrons moved by drift from p to n and holes moved by drift from n to p —add together to form the drift current I_s , whose direction is from the n side to the p side of the junction, as indicated in Fig. 3.45. Since the current I_s is caused by thermally generated minority carriers, its value is strongly dependent on temperature. However, it is independent of the value of the depletion-layer voltage V_0 .

Under open-circuit conditions (Fig. 3.45) no external circuit exists; thus the two opposite currents across the junction should be equal in magnitude:

$$I_d = I_s$$

This equilibrium condition is maintained by the barrier voltage V_0 . Thus, if for some reason I_d exceeds I_s , then more bound charge will be uncovered on both sides of the junction, the depletion layer will widen, and the voltage across it (V_0) will increase. This in turn causes I_d to decrease until equilibrium is achieved with $I_d = I_s$. On the other hand, if I_s exceeds I_d , then the amount of uncovered charge will decrease, the depletion layer will narrow, and the voltage across it (V_0) will decrease. This causes I_d to increase until equilibrium is achieved with $I_d = I_s$.

The Junction Built-in Voltage With no external voltage applied, the voltage V_0 across the junction can be shown to be given by

$$V_0 = k_T \ln \left(\frac{N_n N_p}{n^2} \right) \quad (3.48)$$

where N_n and N_p are the doping concentrations of the n side and p side of the junction, respectively. Thus V_0 depends both on doping concentrations and on temperature. It is

known as the junction built-in voltage. Typically, for silicon at room temperature, V_0 is in the range of 0.6 V to 0.8 V.

When the pn junction terminals are left open-circuited, the voltage measured between them will be zero. That is, the voltage V_0 across the depletion region does not appear between the device terminals. This is because of the contact voltages existing at the metal-semiconductor junctions of the diode terminals, which counter and exactly balance the barrier voltage. If this were not the case, we would have been able to draw energy from the isolated pn junction, which would clearly violate the principle of conservation of energy.

Width of the Depletion Region From the above, it should be apparent that the depletion region exists in both the n and p materials and that equal amounts of charge exist on both sides. However, since usually the doping levels are not equal in the n and p materials, one can reason that the width of the depletion region will not be the same on the two sides. Rather, in order to uncover the same amount of charge, the depletion layer will extend deeper into the more lightly doped material. Specifically, if we denote the width of the depletion region in the p side by x_p and in the n side by x_n , this charge-equality condition can be stated as

$$q x_p A N_p = q x_n A N_n$$

where A is the cross-sectional area of the junction. This equation can be rearranged to yield

$$\frac{x_p}{x_n} = \frac{N_n}{N_p} \quad (3.49)$$

In actual practice, it is usual that one side of the junction is much more heavily doped than the other, with the result that the depletion region exists almost entirely on one side (the lightly doped side). Finally, in device physics, the width of the depletion region of an open-circuited junction is given by

$$W_{depl} = x_p + x_n = \sqrt{\frac{2q}{\epsilon_s} \left(\frac{1}{N_n} + \frac{1}{N_p} \right)} V_0 \quad (3.50)$$

where ϵ_s is the electrical permittivity of silicon = $11.7 \epsilon_0 = 1.14 \times 10^{-11}$ F/m. Typically, W_{depl} is in the range of 0.1 μm to 1 μm .

EXERCISE

3.7.1. If the junction voltage $V_0 = 0.6$ V, the depletion-layer width is $W_{depl} = 0.1$ μm , and the carrier density is $N = 10^{15}$ cm $^{-3}$, calculate the carrier density in the depletion region and the depletion-layer width for the structure in Exercise 3.7.1. (Ans.: $N_p = 3.5 \times 10^{15}$ cm $^{-3}$, $W_{depl} = 0.05$ μm .)

3.7.2. The Junction Under Reverse-Bias Conditions

The behavior of the pn junction in the reverse direction is most easily explained on a microscopic scale if we consider exciting the junction with a constant-current source (rather than with a voltage source), as shown in Fig. 3.46. The current source I is obviously in the reverse direction. For the time being let the magnitude of I be less than I_b ; if I is greater than I_b , breakdown will occur, as explained in Section 3.7.4.

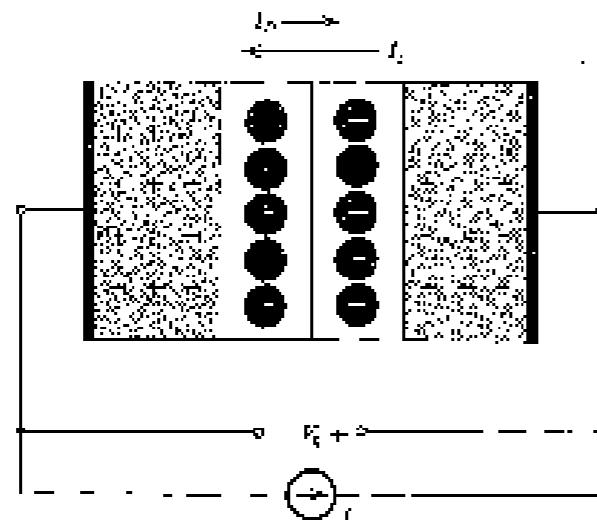


FIGURE 3.46 The diode excited by a constant current source in its reverse direction. To avoid breakdown, V_b is less than V_0 . Note that the depletion layer width W_0 increases as voltage increases; V_p , which appears between the terminals, is the reverse voltage.

The current I_0 will be carried by electrons flowing in the external circuit from the n material to the p material (i.e., in the direction opposite to that of I_0). This will cause electrons to leave the n material and holes to leave the p material. The free electrons leaving the n material cause the unoccupied positive bound charge to increase. Similarly, the holes leaving the p material result in an increase in the unoccupied negative bound charge. Thus the reverse current I_0 will result in an increase in the width of, and the charge stored in, the depletion layer. This in turn will result in a higher voltage across the depletion region—that is, a greater barrier voltage V_b —which causes the diffusion current I_d to decrease. The drift current I_0 , being independent of the barrier voltage, will remain constant. Finally, equilibrium (steady state) will be reached when

$$I_d = I_0 = I$$

In equilibrium, the increase in depletion-layer voltage above the value of the built-in voltage V_0 will appear as an external voltage V_p that can be measured between the diode terminals, with V_p being positive with respect to p . This voltage is denoted V_p in Fig. 3.48.

We can now consider exciting the pn junction by a reverse voltage V_p , where V_p is less than the breakdown voltage V_{Bd} . (Refer to Fig. 3.8 for the definition of V_{Bd} .) When the voltage V_p is first applied, a reverse current flows in the external circuit from p to n . This current causes the increase in width and charge of the depletion layer. Eventually, the voltage across the depletion layer will increase by the magnitude of the external voltage V_p , at which time an equilibrium is reached with the external reverse current I_0 equal to $(I_d - I_p)$. Note, however, that initially, the external current can be much greater than I_0 . The purpose of this initial transient is to charge the depletion layer and increase the voltage across it by V_p volts. Eventually, when a steady state is reached, I_0 will be negligibly small, and the reverse current will be nearly equal to I_p .

The Depletion Capacitance From the above we observe the analogy between the depletion layer of a pn junction and a capacitor. As the voltage across the pn junction changes,

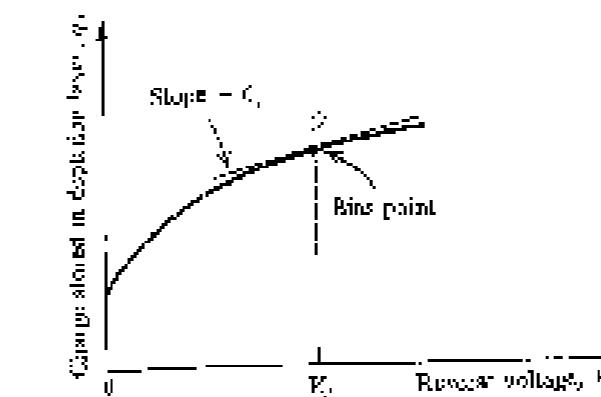


FIGURE 3.47 The charge stored in the reverse side of the depletion layer as a function of the reverse voltage V_p .

the charge stored in the depletion layer changes according to Fig. 3.47 above. A sketch of the typical charge-versus-extrinsic voltage characteristic of a pn junction. Note that only the portion of the curve in the reverse-voltage region is shown.

An expression for the depletion-layer stored charge q_0 can be derived by finding the charge stored on either side of the junction (which charges are, of course, equal), using the relation, we write

$$q_0 = \sigma A = q N_{Dn} A$$

where A is the cross-sectional area of the junction (in a plane perpendicular to the page). Next we use Eq. (3.40) to express σ in terms of the depletion-layer width W_{dp} to obtain

$$q_0 = \sigma \frac{N_D N_A}{N_n N_p} AW_{dp}, \quad (3.51)$$

where W_{dp} can be found from Eq. (3.50) by replacing V_0 by the total voltage across the depletion region, $(V_0 + V_p)$:

$$W_{dp} = \sqrt{\frac{2q}{\epsilon} \left(\frac{1}{N_n} + \frac{1}{N_p} \right) (V_0 + V_p)} \quad (3.52)$$

Combining Eqs. (3.51) and (3.52) yields the expression for the nonlinear $q_0 - V_p$ relationship depicted in Fig. 3.47. This relationship obviously does not represent a linear capacitor. However, a linear-capacitance approximation can be used if the device is biased and the signal swing around the bias point is small, as illustrated in Fig. 3.47. This is the technique utilized in Section 3.3 to obtain linear amplification from an amplifier having a non-linear transfer characteristic and in Section 3.5 to obtain a small-signal model for the diode in the forward-bias region. Under this small-signal approximation, the depletion capacitance (also called the junction capacitance) is simply the slope of the $q_0 - V_p$ curve at the bias point q_0 ,

$$C_d = \frac{\partial q_0}{\partial V_p} \Big|_{V_p=0} \quad (3.53)$$

We can easily evaluate the derivative and find C_s . Alternatively, we can treat the depletion layer as a parallel-plate capacitor and obtain an identical expression for C_s using the familiar formula

$$C_s = \frac{\epsilon A}{W_{dp}} \quad (3.54)$$

where W_{dp} is given in Eq. (3.52). The resulting expression for C_s can be written in the non-dimensional form

$$C_s = \frac{C_{s0}}{1 + \frac{V_S}{V_0}} \quad (3.55)$$

where C_{s0} is the value of C_s obtained for zero applied voltage.

$$C_{s0} = A \sqrt{\frac{\epsilon_{Si}}{2} \left(\frac{N_A N_D}{N_A + N_D} \right)} \quad (3.56)$$

The preceding analysis and the expression for C_s apply to junctions in which the minority concentration is made to change abruptly at the junction boundary. A more general formula for C_s is:

$$C_s = \frac{C_{s0}}{\left(1 + \frac{V_S}{V_0} \right)^m} \quad (3.57)$$

where m is a constant whose value depends on the tensor in which the concentration changes from the p to the n side of the junction. It is called the grading coefficient, and its value ranges from 3 to 1.

To recap, as a reverse-bias voltage is applied to a pn junction, a transient occurs during which the depletion capacitance is charged to the new bias voltage. After the transient ends, the steady-state reverse current is simply equal to $I_b = I_0$. Usually I_0 is very small when the diode is reverse biased, and the reverse current is approximately equal to I_0 . This, however, is only a theoretical model that does not apply very well. In actual fact, currents as high as few nanampères (10^{-9} A) flow in the reverse direction in devices for which I_0 is on the order of 10^{-16} A. This large difference is due to leakage and other effects. Furthermore, the reverse current is dependent to a certain extent on the magnitude of the reverse voltage, contrary to the theory (at model) which states that $I = I_0$ independent of the value of the reverse voltage applied. Nevertheless, because of the very low currents involved, one is usually not interested in the details of the diode $I-V$ characteristic in the reverse direction.

EXERCISE

- 3.9 The $n-p-n$ structure has a thickness of $10 \mu\text{m}$, a carrier density of 10^{16} cm^{-3} , and a diffusion coefficient of $10^{-16} \text{ cm}^2/\text{s}$. The depletion width is $1 \mu\text{m}$ at $V_S = 0$. Find the reverse current at $V_S = -10 \text{ V}$.

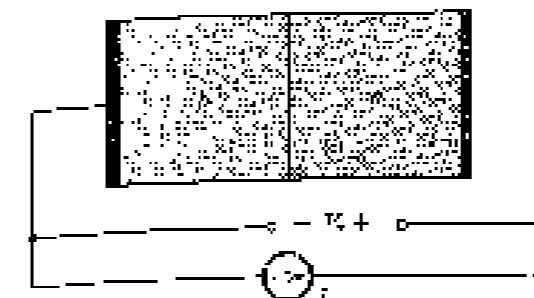


FIGURE 3.49: The pn junction with a depletion region width W_{dp} , where $I > I_0$. The non-dimensional steady-state reverse bias voltage V_S and the polarity indicated develops a positive junction.

3.7.4 The pn Junction in the Breakdown Region

In considering diode operation in the reverse-bias region in Section 3.7.3, it was assumed that the reverse-current source I (Fig. 3.48) was smaller than I_0 , or, equivalently, that the reverse voltage V_S was smaller than the breakdown voltage V_{BD} . Refer to Fig. 3.8 for the definition of V_{BD} . We now wish to consider the breakdown mechanisms in pn junctions and explain the reasons behind the almost-vertical line representing the $I-V$ relationship in the breakdown region. For this purpose, let the pn junction be excited by a current source that causes a constant current I greater than I_0 to flow in the reverse direction, as shown in Fig. 3.49. This current source will move holes from the p material through the external circuit⁷ into the n material and electrons from the n material through the external circuit into the p material. This action results in more and more of the bound charge being uncovered, hence the depletion layer widens until the barrier voltage rises. This voltage rise causes the diffusion current to decrease; eventually it will be reduced to below zero. Nevertheless, this is not sufficient to reach a steady state, since I is greater than I_0 . Therefore the process leading to the widening of the depletion layer continues until a sufficiently high junction voltage develops ... which point a new mechanism sets in to supply the charge carriers needed to support the current I . As will be now explained, this mechanism for supplying reverse current in excess of I_0 can take one of two forms depending on the pn junction material, structure, and so on.

The two possible breakdown mechanisms are the zener effect and the avalanche effect. If a pn junction breaks down with a breakdown voltage $V_S < 5 \text{ V}$, the breakdown mechanism is usually the zener effect. Avalanche breakdown occurs when V_S is greater than approximately 5 V . For junctions that break down between 5 V and 7 V , the breakdown mechanism can be either the zener or the avalanche effect or a combination of the two.

Zener breakdown occurs when the electric field in the depletion layer increases to the point where it can break covalent bonds and generate electron-hole pairs. The electrons generated in this way will be swept by the electric field into the p side and the holes into the n side. Thus these electrons and holes constitute a reverse current across the junction that helps support the external current I . Once the zener effect starts, a large number of carriers can be generated, with a negligible increase in the junction voltage. Thus the reverse current I , i.e., the breakdown region, will be determined by the external circuit, while the reverse voltage appearing between the diode terminals will remain close to the rated breakdown voltage V_S .

The other breakdown mechanism is avalanche breakdown, which occurs when the minority carriers that cross the depletion region under the influence of the electric field gain

⁷ The current in the external circuit will, of course, be carried out only by electrons.

sufficient kinetic energy to be able to break covalent bonds in atoms with which they come into contact. The carriers liberated by this process may have sufficiently high energy to be able to cause other carriers to be liberated in a similar ionizing collision. This process results in the formation of an avalanche, with the result that many carriers are created that are able to support any value of reverse current as determined by the external circuit, with a negligible change in the voltage drop across the junction.

As mentioned before, pn junction breakdown is not a destructive process, provided that the maximum specified power dissipation is not exceeded. This maximum power-dissipation rating is often employed as a maximum value for the reverse current.

3.7.5 The pn Junction Under Forward-Bias Conditions

We next consider operation of the pn junction in the forward-biased region. Again, it is easier to explain physical operation if we excite the junction by a constant-current source supplying a current I_0 in the forward direction, as shown in Fig. 3.49. This causes majority carriers to be supplied to both sides of the junction by the external circuit, holes to the p material and electrons to the n material. These majority carriers will neutralize some of the uncovered bound charges, causing less charge to be stored in the depleting layer. Thus the depletion-layer thickness and the barrier voltage reduces. The reduction in barrier voltage enables more holes to cross the barrier from the p material into the n material, and more electrons from the n side to cross into the p side. Thus the diffusion current I_d increases until equilibrium is achieved with $I_d = I_0$, the externally supplied forward current.

Let us now examine closely the current flow across the forward-biased pn junction in the steady state. The barrier voltage is now lower than V_0 , so at a point V that appears between the diode terminals as a forward voltage drop (i.e., the voltage of the diode will be more positive than the cathode by V volts). Owing to the decrease in the barrier voltage or, alternatively, because of the forward voltage drop V , holes are injected across the junction from the p region and electrons are injected across the junction into the n region. The holes injected into the n region will cause the minority-carrier concentration there, p_n , to exceed the thermal equilibrium value, p_{n0} . The excess concentration ($p_n - p_{n0}$) will be highest near the edge of

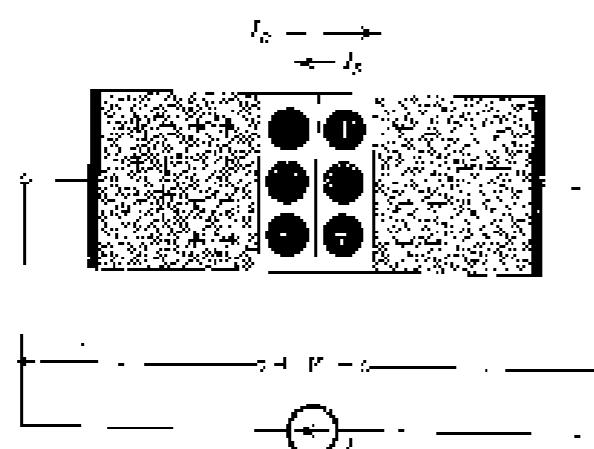


FIGURE 3.49 The pn junction excited by a constant current source supplying a current I_0 in the forward direction. The depletion-layer thickness and the barrier voltage decreases as V value, which appears as an applied voltage in the forward direction.

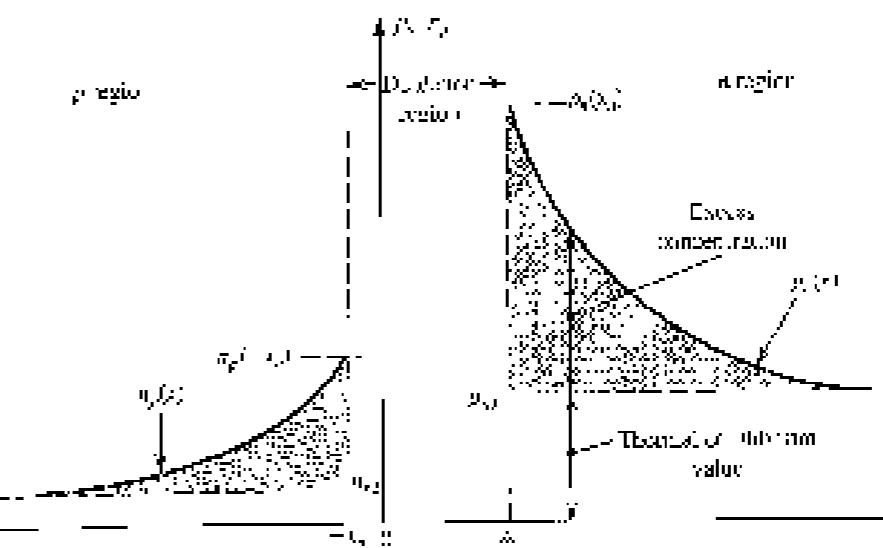


FIGURE 3.50 Minority-carrier distribution in a forward-biased pn junction. It is assumed that the p side is more heavily doped than the n region, $N_p > N_n$.

the depletion layer and will decrease exponentially as one moves away from the junction, eventually reaching zero. Figure 3.50 shows such a minority-carrier distribution.

In the steady state the concentration profile of excess minority carriers remains constant, and indeed it is such a distribution that gives rise to the increase of diffusion current I_d above the value I_0 . This is because the distribution shown causes injected minority holes to diffuse away from the junction into the n region and disappear by recombination. To maintain equilibrium at equal carrier ratios of electrons will have to be supplied by the external circuit, thus replenishing the electron supply in the n material.

Similar statements can be made about the minority electrons in the p material. The diffusion current I_p is, of course, the sum of the electron and hole components:

The Current-Voltage Relationship We now show how the diode $i-v$ relationship of Eq. (3.1) arises. Toward that end, we consider in some detail the current component caused by the holes injected across the junction into the n region. An important result from semiconductor physics relates the concentration of minority carriers at the edge of the depletion region, denoted by $p_n(x)$ in Fig. 3.50, to the forward voltage V ,

$$p_n(x) = p_{n0} e^{-\frac{qV}{kT}} \quad (3.58)$$

This is known as the law of the junction; its proof is usually found in textbooks dealing with device physics.

The distribution of excess hole concentration in the n region, shown in Fig. 3.50, is an exponentially decaying function of distance and can be expressed as

$$p_n(x) = p_{n0} + [p_n(x) - p_{n0}] e^{-\frac{qV}{kT}} \quad (3.59)$$

where I_p is a constant that determines the x -slope of the exponential decay. It is called the diffusion length of holes in the n -type silicon. The smaller the value of I_p , the faster the injected holes will recombine with majority electrons, resulting in a steeper decay of minority carrier

concentration. In fact, t_p is related to another semiconductor parameter known as the excess-minority-carrier lifetime, τ_p . It is the average time it takes for a hole injected into the n region to recombine with a majority electron. The relationship is

$$t_p = \sqrt{D_p \tau_p} \quad (3.60)$$

where, as mentioned before, D_p is the diffusion coefficient for holes in the n type material. Typical values for t_p are 1 to 100 μm , and the corresponding values of τ_p are in the range of 1 to 10,000 μs .

The holes diffusing in the n region will give rise to a hole current whose density can be evaluated using Eqs. (3.37) and (3.59) with p/p_0 obtained from Eq. (3.55).

$$J_p = q \frac{D_p}{L_p} p_{n0} (e^{v/v_0} - 1) e^{-x/t_p} \quad (3.61)$$

Observe that J_p is zero at the edge of the depletion region ($x = x_0$) and decays exponentially with distance. The decay is, of course, due to the recombination with the majority electrons. In the steady state, the majority carriers will have to be replenished, and this electrons will be supplied from the external circuit to the n region at a rate that will keep the concentration at the value it has at $x = x_0$. Thus the current density due to hole injection is given by

$$J_p = q \frac{D_p}{L_p} p_{n0} e^{v/v_0} - 1 \quad (3.61)$$

A similar analysis can be performed for the electrons injected across the junction into the p region resulting in the electron-current component J_n :

$$J_n = q \frac{D_n}{L_n} n_{p0} (e^{v/v_0} - 1) \quad (3.62)$$

where L_n is the diffusion length of electrons in the p region. Since J_n and J_p are in the same direction, they can be added and multiplied by the junction cross-sectional area to obtain the total current I as

$$I = J_p \left(\frac{q D_p p_{n0}}{L_p} + \frac{q D_n n_{p0}}{L_n} \right) (e^{v/v_0} - 1)$$

Substituting for $p_{n0} = n^2/N_1$ and for $n_{p0} = n^2/N_2$, we can express I as the form

$$I = A q n_0^2 \left(\frac{D_p}{N_1 N_2} + \frac{D_n}{N_2 N_1} \right) (e^{v/v_0} - 1) \quad (3.63)$$

We recognize this as the diode equation where the saturation current I_s is given by

$$I_s = A q n_0^2 \left(\frac{D_p}{L_p N_2} + \frac{D_n}{L_n N_1} \right) \quad (3.64)$$

Observe that, as expected, I_s is directly proportional to the junction area A . Furthermore, I_s is proportional to n_0^2 , which is a strong function of temperature (Fig. 3.36). Also, note that the exponential in Eq. (3.63) does not include the constant c_0 as a "fix-up" parameter that is included to account for carrier-gain effects.

Diffusion Capacitance. Even the description of the operation of the pn junction in the forward region, we note that in the steady state a certain amount of excess minority-carrier charge is stored in each of the p and n bulk regions. If the terminal voltage changes, this charge

will have to change before a new steady state is achieved. This charge storage phenomenon gives rise to another capacitive effect, distinctly different from that due to charge storage in the depletion region.

To calculate the excess minority-carrier stored charge, refer to Fig. 3.50. The excess hole charge stored in the n region can be found from the shaded area under the exponential as follows:

$$\begin{aligned} Q_p &= Aq \times \text{shaded area under the } p_n(x) \text{ exponential} \\ &= Aq \times [p_n(x_0) - p_n(0)] L_p \end{aligned}$$

Substituting for $p_n(x)$ from Eq. (3.58) and using Eq. (3.61) enables us to express Q_p as

$$Q_p = \frac{L_p^2}{\tau_p} I_s \quad (3.65)$$

where $I_s = A q J_s$ is the hole component of the current across the junction. Now, using Eq. (3.60), we can substitute for $L_p^2/D_p = t_p$, the hole lifetime, to obtain

$$Q_p = \tau_p I_s \quad (3.65)$$

This alternative relationship says that the stored excess hole charge is proportional to both the hole current component and the hole lifetime. A similar relationship can be developed for the electron charge stored in the p region,

$$Q_n = \tau_n I_s \quad (3.66)$$

where τ_n is the electron lifetime in the p region. The total excess minority-carrier charge can be obtained by adding together Q_p and Q_n :

$$Q = \tau_n I_s + \tau_p I_s \quad (3.67)$$

This charge can be expressed in terms of the diode current $I = I_s + I_d$ as

$$Q = \tau_s I \quad (3.68)$$

where τ_s is called the mean transit time of the space. Obviously, τ_s is related to τ_n and τ_p . Furthermore, in most practical devices, one side of the junction is much more heavily doped than the other. For instance, if $N_A \gg N_D$, one can show that $\tau_p \gg \tau_n$, $I_s \ll I_D$, $Q_p \gg Q_n$, $Q = Q_p$, and thus $\tau_s \approx \tau_p$. This case is illustrated in Exercise 3.74 on page 208.

For small changes around I_s this point, we can define the small-signal diffusion capacitance C_d as

$$C_d = \frac{\partial Q}{\partial V}$$

and can show that

$$C_d = \left(\frac{\tau_s}{V_s} \right)^{1/2} \quad (3.69)$$

where I is the diode current at the bias voltage. Note that C_d is directly proportional to the diode current I and is thus negligibly small when the diode is reverse biased. Also, note that to keep C_d small, the transit time τ_s must be made small, an important requirement for diodes intended for high-speed or high-frequency operation.

EXERCISE

3.34 A diode has a carrier concentration in the N_A layer of $N_A = 10^{17} \text{ cm}^{-3}$, $n_i = 3 \times 10^{10} \text{ cm}^{-3}$, and a carrier concentration in the P_A layer of $N_P = 10^{15} \text{ cm}^{-3}$. A reverse bias voltage $V_{DR} = -10 \text{ V}$ is applied across the junction. Calculate (a) the forward-bias voltage V_F at which the diffusion current equals the junction leakage current, (b) the junction leakage current, and (c) the total junction capacitance. Assume that the depletion width is constant at $W_D = 10 \mu\text{m}$ and that the carrier mobility in the P_A layer is $\mu_P = 75 \text{ cm}^2/\text{V}\cdot\text{s}$.

Junction Capacitance. The depletion-layer or junction capacitance under forward-bias conditions can be found by replacing V_F with $-V$ in Eq. (3.57). It turns out, however, that the accuracy of this relationship in the forward-bias region is rather poor. As an alternative, circuit designers use the following rule of thumb:

$$C_J \approx 2C_0 \quad (3.20)$$

3.7.6 Summary

For easy reference, Table 3.2 provides a listing of the important relationships that describe the physical operation of an junction.

TABLE 3.2 Summary of Important Equations for an Junction Diode
For Intrinsic Si at $T = 300 \text{ K}$ and $N_A = N_P = 10^{17} \text{ cm}^{-3}$

Quantity	Relationship	Values of Constants and Parameters For Intrinsic Si at $T = 300 \text{ K}$
Carrier concentration in reverse-biased region (cm^{-3})	$n_i^2 = BT^3 e^{-V/T}$	$B = 3.4 \times 10^9 \text{ A} \cdot \text{cm}^2 \cdot \text{V}^{-1} \cdot \text{K}^{-3}$ $D_N = 1.12 \text{ cm}^2/\text{s}$ $k = 8.62 \times 10^{-3} \text{ eV/K}$ $n_i = 3 \times 10^{10} \text{ cm}^{-3}$
Diffusion current density (A/cm^2)	$I_D = -qN_A \frac{dn}{dx}$ $I_D = qN_A \frac{dx}{dx}$	$N_A = 3.0 \times 10^{17} \text{ cm}^{-3}$ $D_N = 12 \text{ cm}^2/\text{s}$ $D_P = 34 \text{ cm}^2/\text{s}$
Drift current density (A/cm^2)	$I_{D,drift} = n(p/n_A + n/p_A)\phi$	$\mu_n = 480 \text{ cm}^2/\text{V}\cdot\text{s}$ $\mu_p = 1.140 \times 10^2 \text{ cm}^2/\text{V}\cdot\text{s}$
Resistivity ($\Omega \cdot \text{cm}$)	$\rho = 1.2 \times 10^4 (n_A + n_P)$	ρ_n and ρ_p decrease with an increase in doping concentration
Relationship between mobility and resistivity	$\frac{\rho_n}{\mu_n} = \frac{\rho_p}{\mu_p} = \rho_m$	$V_T = kT/q$ $\approx 25.8 \text{ mV}$
Carrier concentration at very small x (cm^{-3})	$n_{(x=0)} = n_i$ $n_{(x=0)} = n_i^2/N_A$	

Quantity	Relationship	Values of Constants and Parameters For Intrinsic Si at $T = 300 \text{ K}$
Carrier concentration in a type II region (cm^{-3})	$n_{(x=0)} = N_A$ $n_{(x=0)} = n_i^2/N_A$	
Forward-biased voltage (V)	$V_0 = V_{F,0} \left(\frac{n_{(x=0)}}{N_A} \right)^{1/m}$	
Width of depletion region (nm)	$x_0 = \frac{N_A}{N_A + N_D}$ $W_{DN} = x_0 - x_D$ $= \frac{2kT}{e} \left[\frac{1}{N_D} + \frac{1}{N_A} \right]^{1/2} x_0 + x_D$	$x_0 = 11.78 \text{ nm}$ $W_{DN} = 5.854 \times 10^{-10} \text{ nm}$
Charge stored in depletion layer (electron)	$Q_D = q \frac{N_A}{N_A + N_D} 4 W_{DN}$	
Depletion capacitance (F)	$C_J = \frac{q}{W_{DN}} C_0 = \frac{q}{W_{DN}} C_0 $ $C_J = C_0 \left(\frac{N_A}{N_A + N_D} \right)^{1/m}$ $C_J = 2C_0 \quad (\text{for Brown's law})$	$m = \frac{1}{2} \text{ or } \frac{1}{3}$
Forward current (A)	$I = I_D + I_S$ $I_S = 4q \left(\frac{N_A}{L_A N_D} \right)^{1/m} + 1$ $I_S = Aq \left(\frac{N_A}{L_A N_D} \right)^{1/m} + 1$	
Saturated current (A)	$I_S = 4q \left(\frac{D_N}{L_A N_D} \right)^{1/m} + 1$	
Mean free path ($\text{cm} \cdot \text{ns}$)	$\tau_p = L_p^2/D_p \quad \tau_n = L_n^2/D_n$	$L_p, L_n = 1 \text{ nm} \rightarrow 100 \text{ fm}$ $\tau_p, \tau_n = 1 \text{ ns} \rightarrow 10^4 \text{ fm}$
Minority-carrier concentration (cm^{-3})	$Q_n = \tau_n J_n \quad Q_p = \tau_p J_p$	
Diffusion capacitance (F)	$C_d = \frac{q N_A}{k T \tau_p}$	

3.8 SPECIAL DIODE TYPES^a

In this section, we'll take briefly some important special types of diodes.

^a This section can be skipped without loss of continuity.

3.8.1 The Schottky-Barrier Diode (SBD)

The Schottky-barrier diode (SBD) is formed by bringing metal into contact with a moderately doped n -type semiconductor material. The resulting metal-semiconductor junction behaves like a diode, conducting current in one direction (from the metal anode to the n region, conductive electrode) and acting as an open circuit in the other, and is known as the Schottky-barrier diode or simply the Schottky diode. In fact, the current-voltage characteristic of the SBD is remarkably similar to that of a $p-n$ -junction diode, with two important exceptions:

1. In the SBD, current is conducted by majority carriers (electrons). Thus the SBD does not exhibit the minority-carrier charge-storage effect found in forward-biased $p-n$ junctions. As a result, Schottky diodes can be switched from on to off, and vice versa, much faster than is possible with $p-n$ -junction diodes.
2. The forward voltage drop of a conducting SBD is lower than that of a $p-n$ junction diode. For example, an SBD made of silicon exhibits a forward voltage drop of 0.3 V to 0.5 V, compared to the 0.6 V to 0.8 V found in silicon $p-n$ -junction diodes. SBDs can also be made of gallium arsenide (GaAs) and, in fact, play an important role in the design of GaAs circuits.⁷ Gallium arsenide SBDs exhibit forward voltage drops of about 0.7 V.

Apart from GaAs circuits, Schottky diodes find application in the design of a special form of bipolar transistor logic circuits, known as Schottky-TTL, where TTL stands for transistor-transistor logic.

Before leaving the subject of Schottky-barrier diodes, it is important to note that not every metal-semiconductor contact is a diode. In fact, metals commonly deposited on the semiconductor surface in order to make terminals for the semiconductor devices and to connect different devices on an integrated circuit chip. Such metal-semiconductor contacts are known as **ohmic contacts** to distinguish them from the rectifying contacts that result in SBDs. Ohmic contacts are usually made by depositing metal on very heavily doped (and thus low-resistivity) semiconductor regions.

3.8.2 Varactors

Earlier, we learned that reverse-biased $p-n$ junctions exhibit a charge-storage effect that is modeled with the depletion-layer or junction capacitance C_j . As Eq. (3.2.1) indicates, C_j is a function of the reverse bias voltage V_r . This dependence turns out to be useful in a number of applications, such as the automatic tuning of radio receivers. Special diodes are therefore fabricated to be used as voltage-variable capacitors known as varactors. These diodes are optimized to make the capacitance a strong function of voltage by arranging that the grading coefficient a is large.⁸

3.8.3 Photodiodes

If a reverse-biased $p-n$ junction is illuminated—that is, exposed to incident light—the photons impinging the junction cause covalent bonds to break, and thus electron-hole pairs are generated in the depletion layer. The electric field in the depletion region then sweeps the liberated electrons to the n side and the holes to the p side, giving rise to a reverse current across the junction. This current, known as photocurrent, is proportional to the intensity of

⁷The CD acronym means the test and measure device with current material or GaAs topics.

the incident light. Such a diode, called a photodiode, can be used to convert light signals into electrical signals.

Photodiodes are usually fabricated using a compound semiconductor⁹ such as gallium arsenide. The photodiode is an important component of a growing family of circuits known as **optoelectronics** or **photronics**. As the name implies, such circuits utilize an optimization of electronics and optics for signal processing, storage, and transmission. Usually, electronics is the preferred means for signal processing, whereas optics is most suited for transmission and storage. Examples include fiber-optic transmission of telephone and television signals and the use of optical storage in CD-ROM computer disks. Optical transmission provides very wide bandwidths and low signal attenuation. Optical storage allows vast amounts of data to be stored reliably in a small space.

Finally, we should note that without reverse bias, the illuminated photodiode functions as a solar cell. Usually fabricated from low-cost silicon, a solar cell converts light to electrical energy.

3.8.4 Light-Emitting Diodes (LEDs)

The light-emitting diode (LED) performs the inverse of the function of the photodiode; it converts a forward current into light. The reader will recall that in a forward-biased $p-n$ junction, minority carriers are injected across the junction and diffuse into the p and n regions. The diffusing minority carriers then recombine with the majority carriers. Such recombination can be made to give rise to light emission. This can be done by fabricating the $p-n$ junction using a semiconductor of the type known as direct-bandgap materials. Gallium arsenide belongs to this group and can thus be used to fabricate light-emitting diodes.

The light emitted by an LED is proportional to the number of recombinations that take place, which in turn is proportional to the forward current in the diode.

LEDs are very popular devices. They find application in the design of numerous types of displays, including the displays of laboratory instruments such as digital voltmeters. They can be made to produce light in a variety of colors. Furthermore, LEDs can be designed so as to produce coherent light with a very narrow bandwidth. The resulting device is a laser diode. Laser diodes find application in optical communication systems and in CD players, among other things.

Combining an LED with a photodiode in the same package results in a device known as an optoisolator. The LED converts an electrical signal input to the optoisolator into light, which the photodiode detects and converts back to an electrical signal at the output of the optoisolator. Use of the optoisolator provides complete electrical isolation between the electrical circuit that is connected to the isolator's input and the circuit that is connected to its output. Such isolation can be useful in reducing the effect of electrical interference or signal transmission within a system, and has optoisolators are frequently employed in the design of digital systems. They can also be used in the design of medical instruments to reduce the risk of electrical shock to patients.

Note that the optoisolating between an LED and photodiode need not be accomplished inside a small package. Indeed, it can be implemented over a long distance using an optical fiber, as is done in fiber-optic communication links.

⁸ Whereas covalent semiconductors such as silicon use two elements from Group IV of the periodic table, a compound semiconductor uses a combination of elements from groups III and V (V/VI) and VI. For example, GaAs is formed of gallium (group III) and arsenic (group V), and is thus known as a III-V compound.

3.9 THE SPICE DIODE MODEL AND SIMULATION EXAMPLES

We conclude this chapter with a description of the model that SPICE uses for the diode. We will also illustrate the use of SPICE in the design of a dc power supply.

3.9.1 The Diode Model

To the designer, the value of simulation results is a direct function of the quality of the models used for the devices. The more faithfully the model represents the various characteristics of the device, the more accurately the simulation results will describe the operation of an actual fabricated circuit. In other words, to see the effect of various imperfections in device operation on circuit performance, these imperfections must be included in the device model used by the circuit simulator. These comments about device modeling obviously apply to all devices, and not just to diodes.

The large-signal SPICE model for the diode is shown in Fig. 3.51. The static behavior is modeled by the exponential $v_i - i$ relationship. The dynamic behavior is represented by the nonlinear capacitor C_{di} , which is the sum of the diffusion capacitance C_d and the junction capacitance C_j . The series resistance R_s represents the total resistance of the p and n regions on each side of the junction. The value of this parasitic resistance is usually very low, but it is typically in the range of a few ohms for small-signal diodes. For small-signal analysis, SPICE uses the diode incremental resistance r_i and the incremental values of C_d and C_j .

Table 3.3 provides a partial listing of the diode model parameters used by SPICE, all of which should be familiar to the reader. But, having a good device model solves only half of the modeling problem; the other half is to determine appropriate values for the model parameters. This is by no means an easy task. The values of the model parameters are determined using a combination of characterization of the device fabrication process and specific measurements performed on the actual manufactured devices. Semiconductor manufacturers expend a great deal of money to extract the values of the model parameters for their devices. For discrete diodes, the values of the SPICE diode parameters can be determined from the diode data sheets, supplemented if needed by key measurements. Circuit simulators (such as PSpice) include in their libraries the model parameters of some of the popular off-the-shelf components. For instance, in Example 3.10, we will use the commercially available 1N4448肖特基二极管 whose SPICE model parameters are available in PSpice.

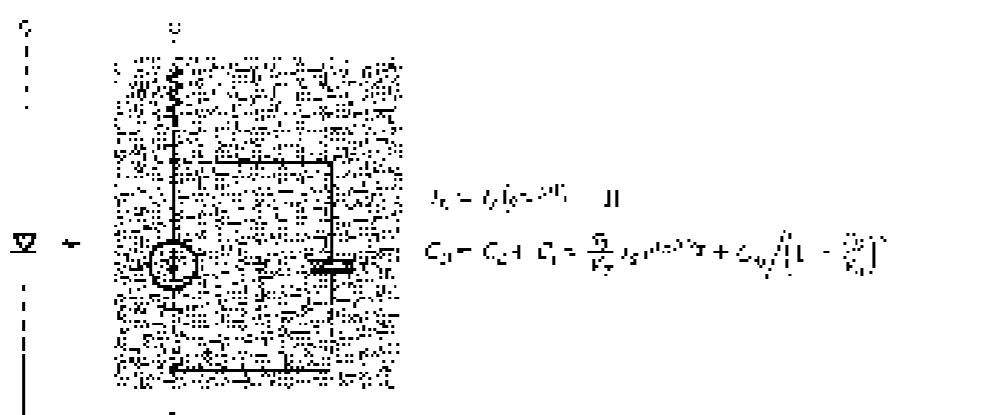


FIGURE 3.51 The SPICE diode model.

TABLE 3.3 Parameters of the SPICE Diode Model (Partial Listing)

SPICE Parameter	Book Symbol	Description	Units
I_0	I_0	Saturation current	A
N	N	Diode ideality coefficient	
R_S	R_s	Series resistance	Ω
V_J	V_j	Built-in potential	V
CJO	C_{j0}	Zero-bias depletion (junction) capacitance	F
Cd	$-$	Diffusion capacitance	
M	m	Transistor ratio	
TF	τ_T	Turn-on voltage	V
IV	V_{on}	Breakdown voltage	V
IR	I_{0s}	Reverse current, $> V_{on}$	A

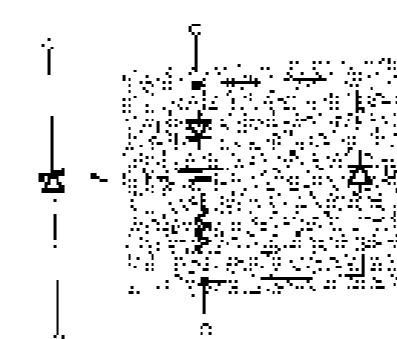


FIGURE 3.52 Equivalent circuit model used to simulate the breakdown in SPICE. Diode D_1 is ideal and can be approximated in SPICE by using a very small value for N (say $n=0.01$).

3.9.2 The Zener Diode Model

The diode model above does not adequately describe the operation of the diode in the breakdown region. Hence, it does not provide a satisfactory model of zener diodes. However, the equivalent-circuit model shown in Fig. 3.52 can be used to simulate a zener diode in SPICE. Diode D_1 is an ideal diode which can be approximated in SPICE by using a very small value for n (say $n=0.01$). Diode D_2 is a regular diode that models the breakdown bias region in the zener (for most applications, the parameter n D_2 is of little consequence).

DESIGN OF A DC POWER SUPPLY

In this example, we will design a dc power supply using the test-circuit schematic capture shown in Fig. 3.53. This circuit consists of a full-wave diode rectifier, a 10 mΩ buckling-oscillator, and a 100 μF filter capacitor.

* The reader is reminded that the Capture schematic and the corresponding PSpice simulation file of this SPICE example in this chapter can be found on the text's CD, as well as on the website (www.eeas.syr.edu/~tmcneely/). In these schematics (as shown in Fig. 3.53), we use variable parameters (V_{IN} , V_{ZEN} , R_L , etc.). In these schematics (as shown in Fig. 3.53), we use variable parameters (V_{IN} , V_{ZEN} , R_L , etc.). This allows one to investigate the effect of changing the values of the various circuit components. This allows one to investigate the effect of changing the component values by simply changing the corresponding parameter values.

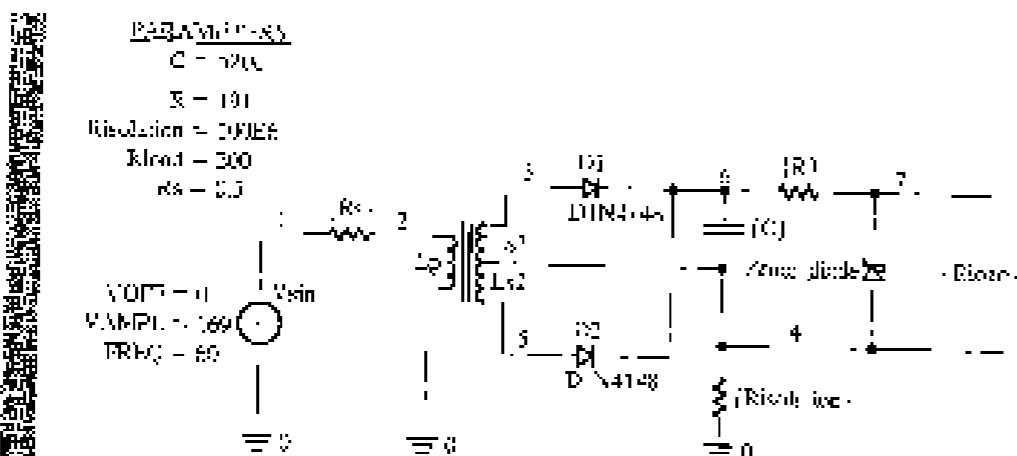


FIGURE 3.53 Layered schematic of Ex 3.Y.4. (lower supply in Example 3)

connected, and a zero voltage regulation. The only jolt-buzzing component is R_{center} , the 10M Ω resistor between the secondary winding of the transformer and ground. This resistor is included to provide dc continuity and thus "keep SPK's happy"; it has little effect on AC operation.

Let it be required that the power supply in Fig. 3.53 provide a minimum dc voltage of 5 V and be able to supply a load current, $I_{L_{\text{min}}}$, as large as 25 mA; that is, $K_{L_{\text{max}}} = 200$. The power supply is fed from a 120-V (rms) AC-DC line. Note that in the PS section (Fig. 3.54), we use a single-diode voltage source with a 169-V peak amplitude to represent the 120-V rms supply (as 120-V rms = 169-V peak). Assuming the availability of a 1-V zener diode having $i_z = 10 \mu\text{A}$ at $v_z = 20$ mV, find $V_{D_{\text{min}}} = 4.9$ V, and then the required minimum current through the zener diode is $I_{z_{\text{min}}} = 5 \mu\text{A}$.

An approximate first circuit design can be obtained as follows: The 120-V AC supply is stepped down to provide 12.5-V (peak) voltage across each of the secondary windings using a 14:1 turns ratio for the center-tapped transformer. The value of 12.5 V is a reasonable compromise between the need to allow for sufficient voltage (above the 5-V range) to operate the rectifier and the regulator, while keeping the PIV ratings of the diodes reasonably low. To determine a value for G , we can use the following expression:

$$R = \frac{F_{\text{exp}} - F_{\text{exp}}}{F_{\text{exp}} + f_{\text{exp}}} \times f_{\text{exp}}$$

where an estimate for V_{ZT1} , the minimum DC voltage across the capacitor, can be obtained by subtracting a diode drop (say, 0.8 V) from 12 V and allowing for a supply voltage across the capacitor of, say, $V = 0.5$ V. Thus, $V_{\text{ZT1}} = 10.7$ V. Furthermore, we note that $I_{\text{ZT1}} = 27 \mu\text{A}$ and $I_{\text{ZT2}} = 5 \mu\text{A}$ and that $V_{\text{Z2}} = 1.9$ V and $r = 16 \Omega$. The result is that $R = 191 \Omega$.

Next, we determine C using a rederivation of Eq. (5.25) with b_2X replaced by the current through the 191-Q resistor. This can be done by noting that the voltage across C varies from 10.7 to -11.2 V, and thus has an average value of 0.05 V. Furthermore, the desired voltage across the corner is 5 V. The result is $C = 500 \text{ pF}$.

Now, with an approximate design in mind, we can proceed with the SPICE simulation. For the power diode, we use the model of Fig. 3.52 and assume $V_{DSS} = 10$ V, $I_{SD} = 10$ A, $R_{DS(on)} = 0.05$ Ω , $C_{SS} = 10 \mu\text{F}$, and $C_{DS} = 1 \mu\text{F}$.

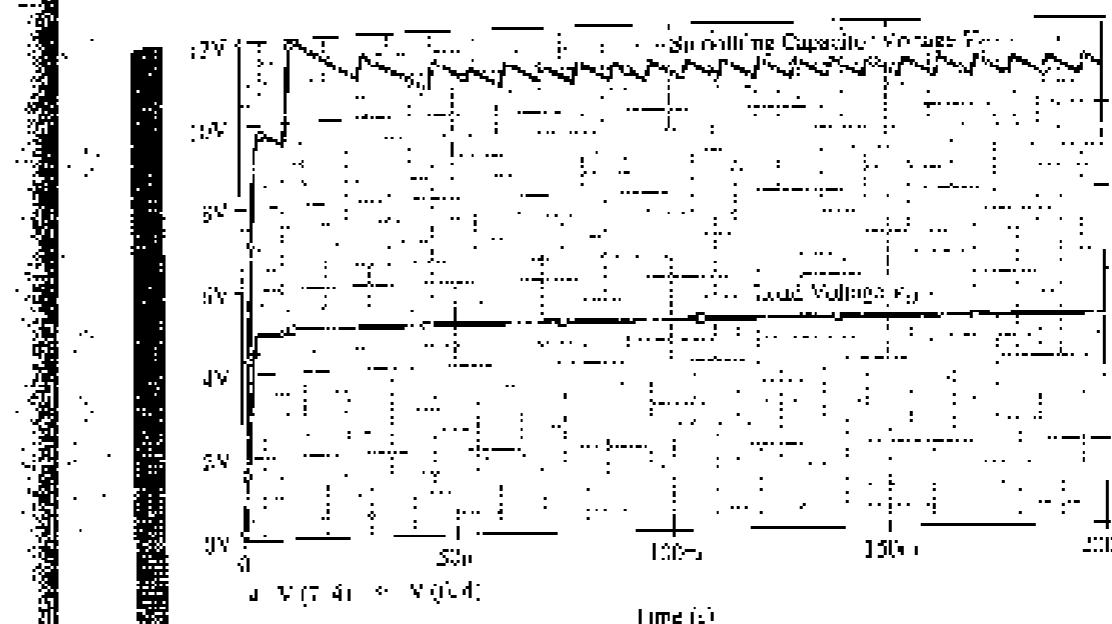


FIGURE 3.54 The voltage v_{C_1} across the coupling capacitor, in C , and the voltage v_{R_L} across the load resistor, in V , for the 5-V power supply of Example 3.13.

and $\alpha = 0.1$, while D_0 has $I_0 = 100 \text{ pA}$ and $\eta = 1.7$. For the soft-fair diode, we use the exact numerically available [0.41483]pc¹² (with $I_0 = 3.682 \text{ nA}$, $\alpha = 1.826$, $K_0 = 0.566$, $Q_0 = 1.57 \text{ V}$, $C_0 = 1.57 \text{ fF}$, $\eta = 0.333$, $\beta = 1.72$, $V_0 = 100 \text{ V}$, $I_{\text{sat}} = 100 \text{ pA}$).

In 2 stages, we perform a numerical analysis and plot the waveforms of both the voltage v_2 across the inverting input to G, and the voltage v_{out} across the load resistor R_{load} . The simulation results for $R_{\text{load}} = 200 \Omega$ ($I_{\text{load}} = 23 \text{ mA}$) are presented in Fig. 3.54. Observe that v_2 has an average of 10.35 V and a ripple of 10.21 V. Thus, $V_s = 10.42 \text{ V}$, which is close to the 10.5-V value that we would expect from the census value of C. The output voltage v_{out} is very close to the required 5 V, with v_{out} varying between 4.957 V and 4.977 V for a ripple of only 20 μV . The variations of v_2 with R_{load} is summarized in Fig. 3.55 for $R_{\text{load}} = 50 \Omega, 100 \Omega, 200 \Omega$, and 150Ω . Accordingly, v_2 remains closest to the nominal value of 5 V for R_{load} as low as 200Ω ($I_{\text{load}} = 23 \text{ mA}$). For $R_{\text{load}} = 150 \Omega$ (yielding only $I_{\text{load}} = 33 \text{ mA}$, greater than the maximum designed value), we see a significant jump in v_2 (from around 4.5 V), as well as a large increase in the ripple voltage at the output (to about 100 μV). This may compromise the zipper regulation as we have suggested. If v_{out} were to be in fact off, then

We conclude that the design meets the specifications, and we can stop here. Alternatively, we may continue fine-tuning the design using *Iteration* of *Space* to help with the task. For instance, we could evaluate what happens if we use a lower value of C , and so on. We can also investigate other properties of the present design, for instance, the maximum number of thoughts and ideas we can work with, or how many ideas we can have in this the time specified by the deadline.

¹² The 1841-1860 data is contained in the evaluation (EV A) of Primary oil-service (OrCa) v. 2.1. The following table is a subset of the EVB document as of this date.

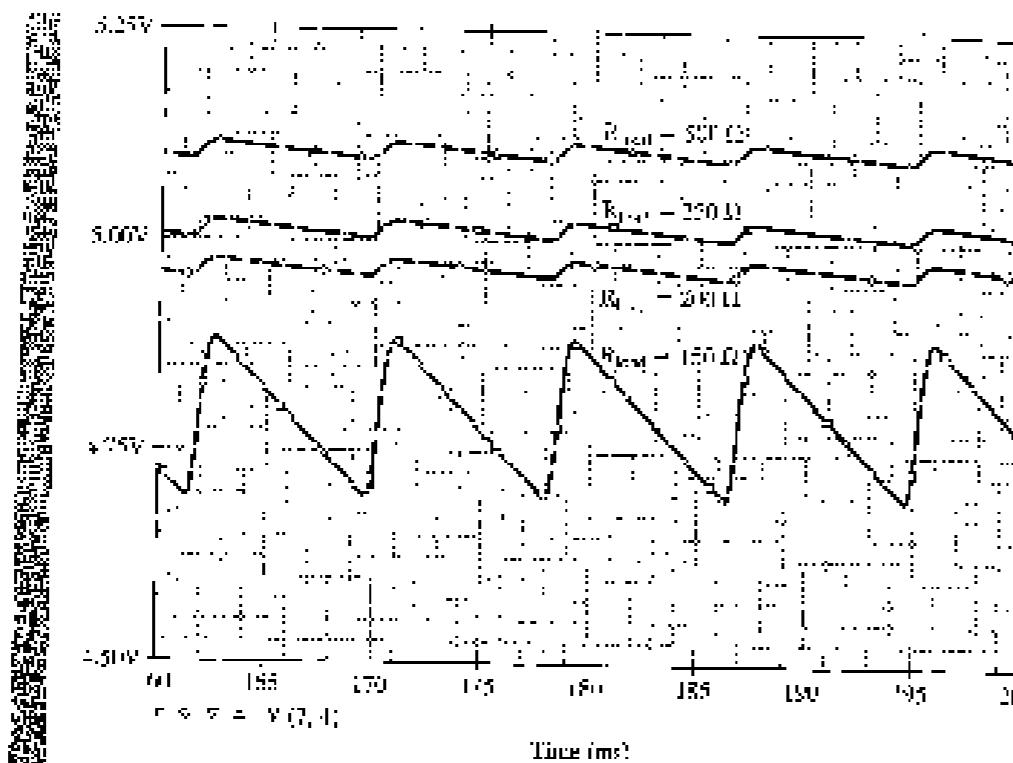


FIGURE 3-53 The output voltage waveform from the 5-V power supply in Example 3-17 for various load resistances: $R_{\text{load}} = 900 \Omega$, 250Ω , 200Ω , and 150Ω . The voltage regulation is lost as a result of a change of 13% .

RECIPE

Fig. 3B. Low PSPs, as interpreted by the method of the variance difference, shown in Fig. 3A. Specifically, plots of variance difference of the voltage V_1 and V_2 , which are filtered with a 100-1000 Hz bandpass, versus the time constant τ of the low-pass filter. The variance difference is $V_1^2 - V_2^2 = 0.5(V_1 + V_2)(V_1 - V_2)$, where $V_1 = 10 \text{ mV} \cdot \text{sec}^{-1}$ and $V_2 = 100 \text{ mV} \cdot \text{sec}^{-1}$.

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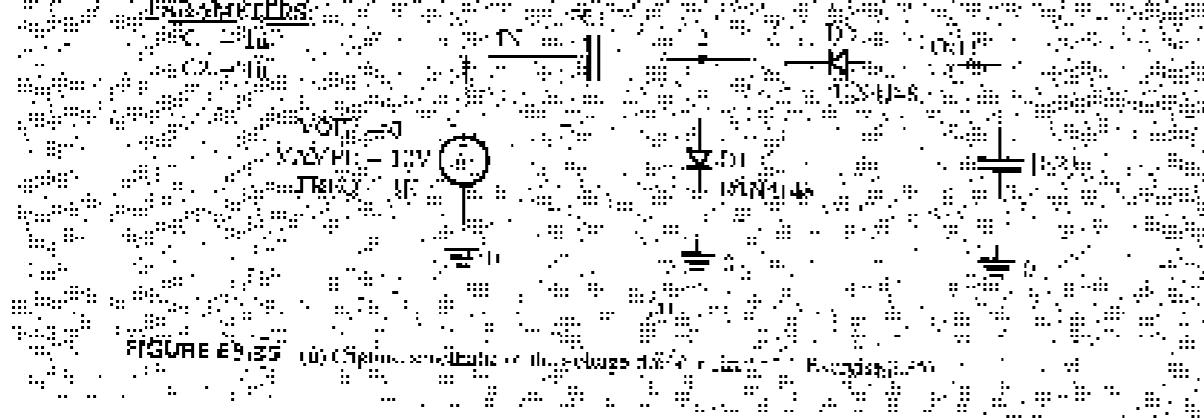


FIGURE 29-137 (b) Schematic of the charge diffusion boundary.

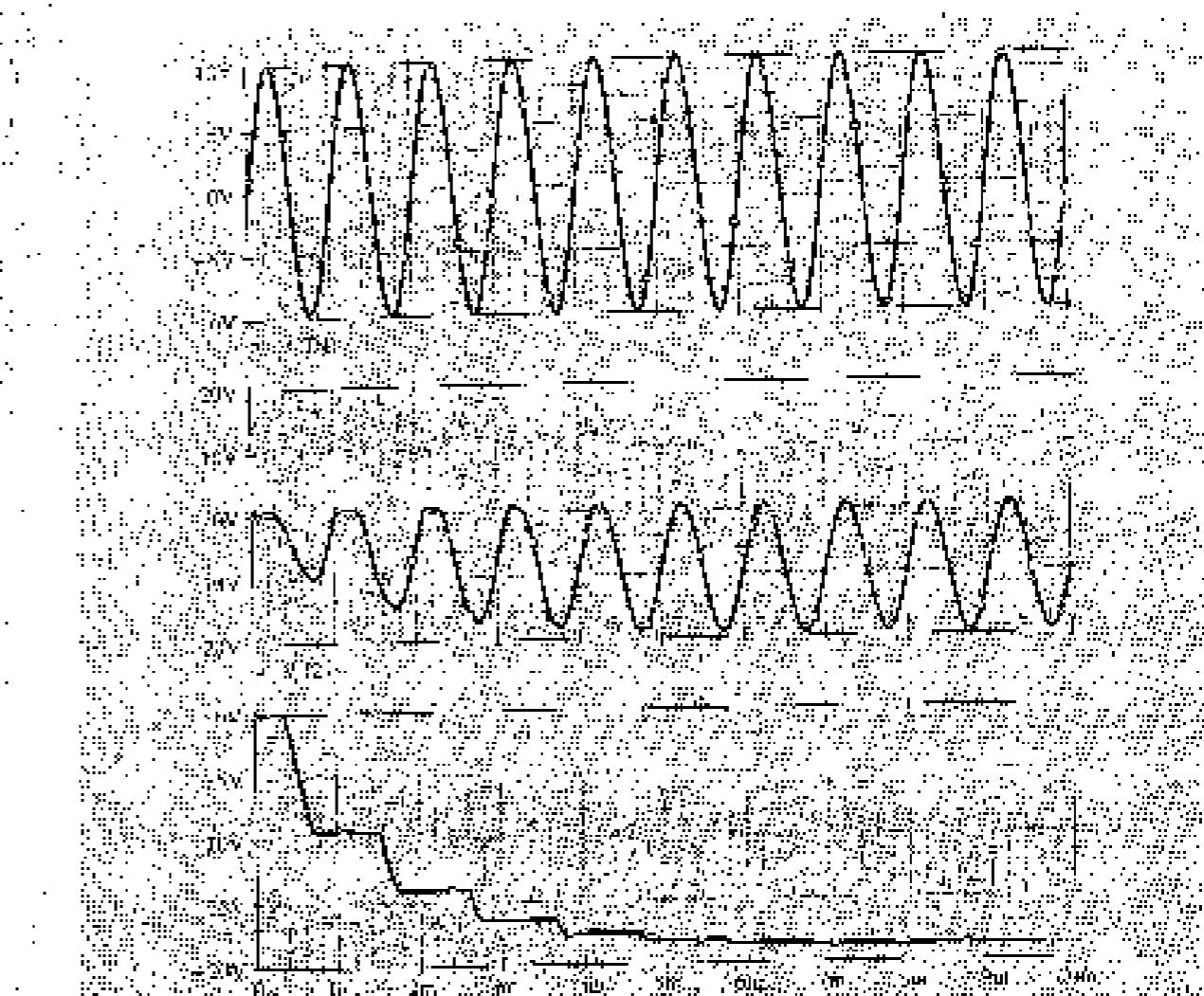


FIGURE 3. Estimated 10-year risk of death due to stroke in the Framingham study. The top panel displays the cumulative risk of stroke for men and women by age and sex. The bottom panel displays the estimated 10-year risk of stroke for men and women by age and sex.

SUMMARY

- In the forward direction, the N_{GD} diode conducts *no* current because the external circuit will be experiencing a zero voltage drop. The N_{GD} diode does not conduct in the reverse direction; the applied voltage appears as a reverse bias across the diode.
 - The unidirectional current flow property makes the diode useful in the **Geometric rectifier** circuits.
 - The low-current conduction of physical silicon diodes is summarized by the relationship $I = I_0 e^{V_D/2kT}$.

276 CHAPTER 3 DIODES

- 3.1** A silicon diode conducts a negligible current until the forward voltage is at least 0.5 V. Then the current increases rapidly, with the voltage drop decreasing by about 1 mV for each 10-fold increase of the value of α for every decade of current increase.
- 3.2** In the reverse direction, a silicon diode conducts a current in the range of $(10^{-9} \text{ A})^{\alpha}$. This current is much greater than J_0 and increases with the magnitude of reverse voltage.
- 3.3** Beyond a certain value of reverse voltage (that depends on the diode), breakdown occurs, and current increases rapidly with a small corresponding increase in voltage.
- 3.4** Diodes designed to operate in the breakdown region are called zener diodes. They are employed in the design of voltage regulators whose function is to provide a constant dc voltage that varies little with variations in power-supply voltage (indicated in V_{DD}).
- 3.5** A hierarchy of diode models is given, with the selection of an appropriate model dictated by the application.
- 3.6** In many applications, a conducting diode is modeled as having a constant voltage of 1.4 V, usually approximately 0.7 V.
- 3.7** A diode biased to operate in a dc current I_0 has a small-signal resistance $r_s = -V_{DS}/I_0$.
- 3.8** The silicon junction diode is basically a $p-n$ junction. Such a junction is represented as a single silicon crystal.

PROBLEMS

SECTION 3.1: THE IDEAL DIODE

- 3.1** An AA flashlight cell, whose Thévenin equivalent is a voltage source of 1.5 V and a resistance of 1 k Ω , is connected to the terminals of an ideal diode. Describe two possible directions that result. What are the diode current and the diode voltage when (a) the connection is between the diode cathode and the positive terminal of the battery and (b) the anode and the positive terminal are connected?

- 3.2** For the circuit shown in Fig. P3.2 using ideal diodes, find the values of the labeled voltages and currents.

- 3.3** For the circuits shown in Fig. P3.3 using ideal diodes, find the values of the labeled voltages and currents.

- 3.4** In each of the ideal diode circuits shown in Fig. P3.4, let v_s be a 1-kHz, 10-V peak sine wave. Neglect the capacitor resulting at v_o . What are its positive and negative peak values?

- 3.5** The circuit shown in Fig. P3.5 is a model for a hydrogen lamp. Here v_s is a 0-V peak sine wave, D_1 and D_2 are ideal diodes, I_b is a 200-mA current source, and B is a 9.5-V battery. Sketch and label the waveform of the voltage current i_b . What is its peak value? What is its average value? If the peak value

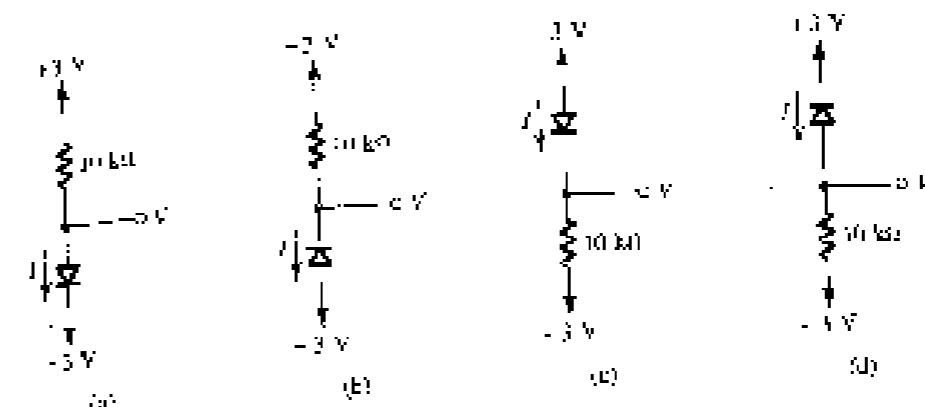


FIGURE P3.2

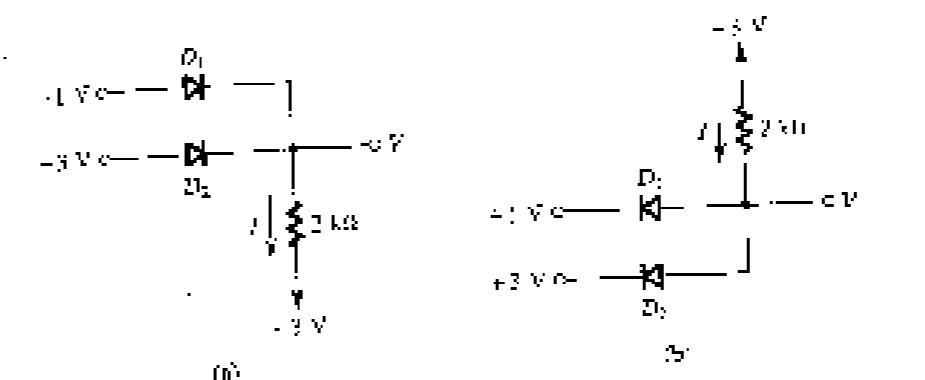


FIGURE P3.3

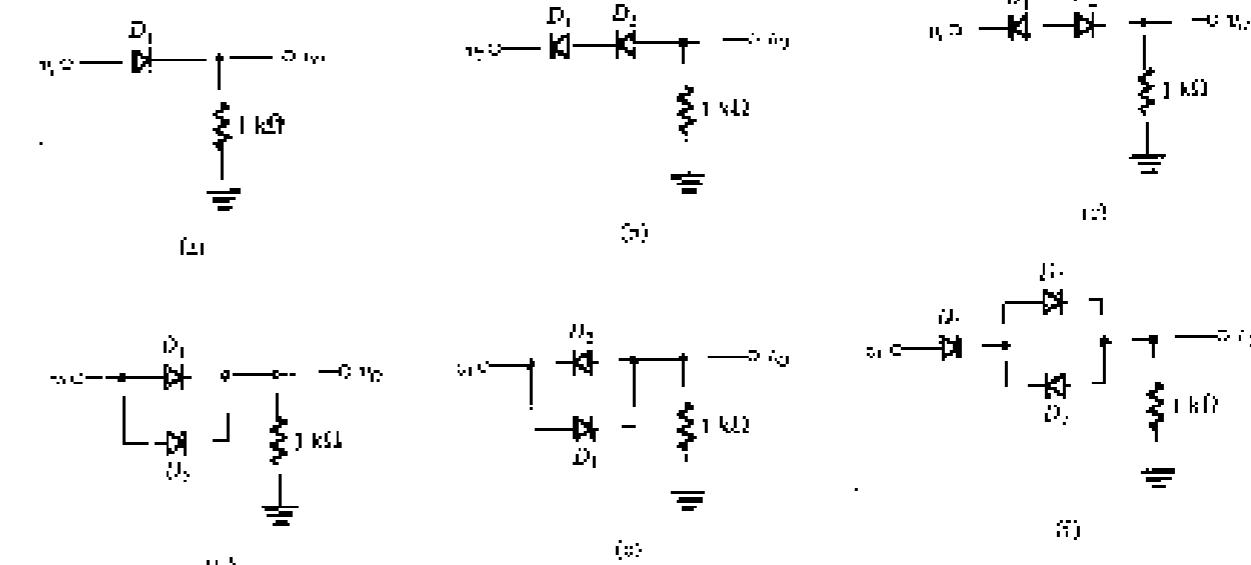


FIGURE P3.4 (Continued)

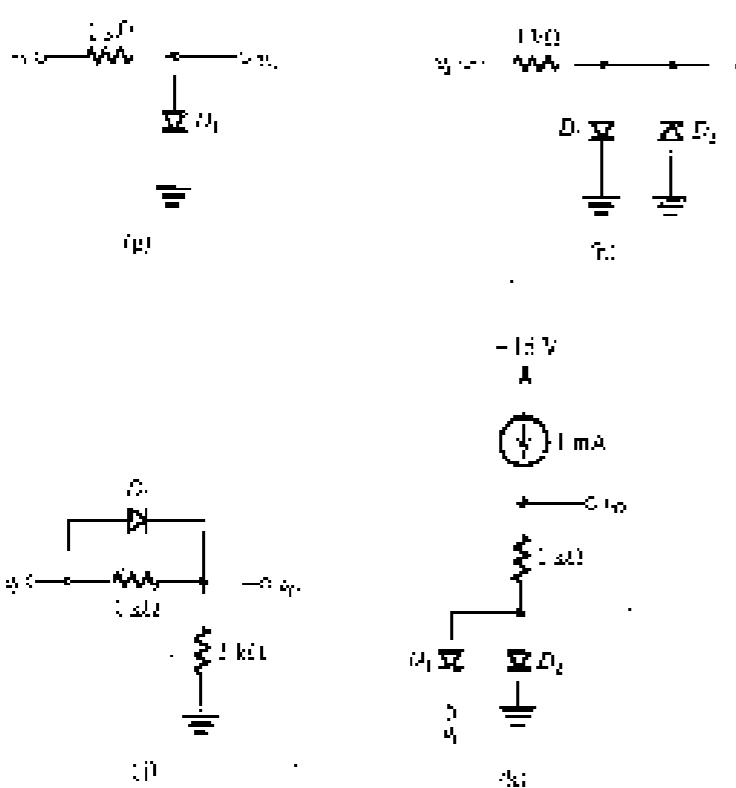


FIGURE P3.4 Diode Circuits.

is also reduced by 10%, what do the peak and average values of i_D become?

To denote the high value and 10% lower value, prepare a table with four columns including all possible input combinations and the resulting values of X and Y . What logic function is $X \oplus Y$? What logic function is $X \cdot Y$? If A has an value of 1 and B has a value of 0, what are the values of X and Y ?

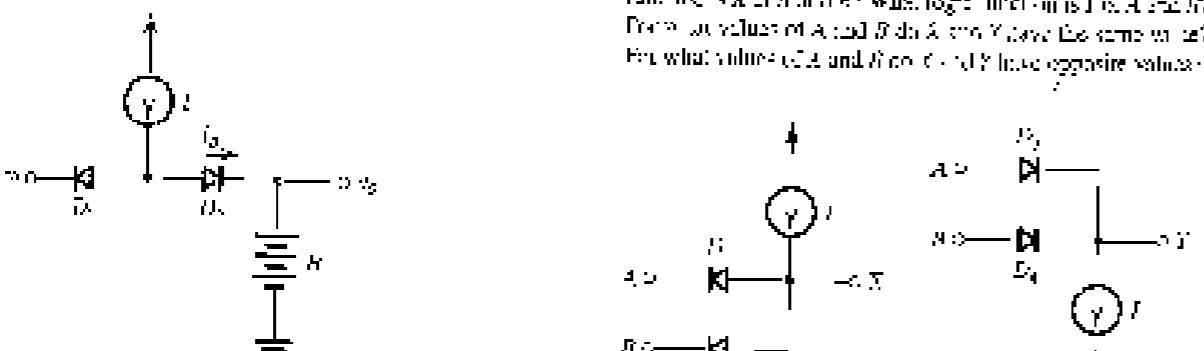
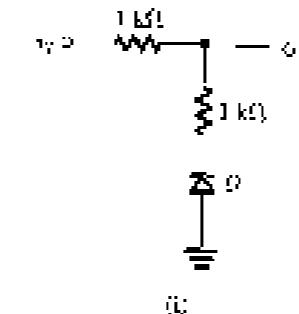


FIGURE P3.5

3.6 The circuit shown in Fig. P3.6 can function as logic even if your voltages are not at high or low. Using "1"

FIGURE P3.6



3.7 Give the logic gate of Fig. 3.6, assume ideal diodes, no input voltage levels of 5V and 15V. Find suitable values for R_1 and R_2 so that the peak-to-peak excursion of the input signal source does not exceed 0.1 mA.

3.8 Repeat Problem 3.7 for the logic gate of Fig. 3.6(b).

3.9 Assuming that the diodes in the circuits of Fig. P3.9 are ideal, find the values of the labeled voltages and currents.

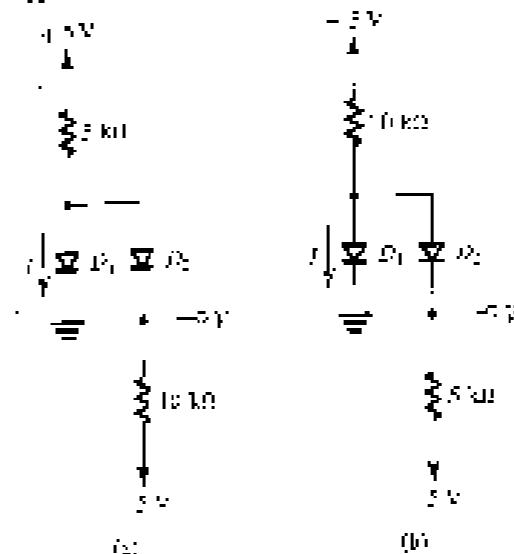


FIGURE P3.9

3.10 Assuming that the diodes in the circuits of Fig. P3.10 are ideal, utilize Thevenin's theorem to simplify the circuits and find the values of the labeled currents and voltages.

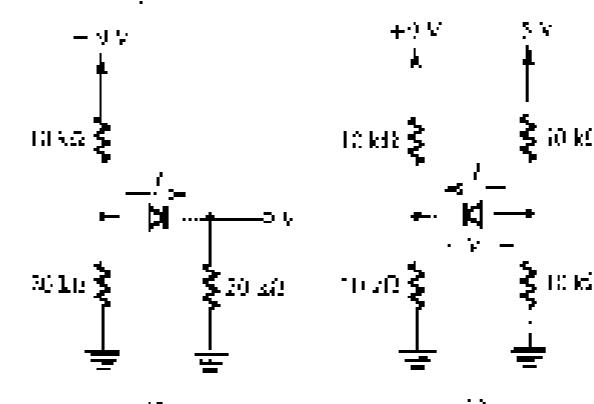


FIGURE P3.10

3.11 To the rectifier circuit of Fig. 3.1(a), let the input sine wave have 170-V rms value and assume the diodes to be ideal. Select suitable values for R so that the peak diode current does not exceed 50 mA. What is the greatest reverse voltage that will appear across the diodes?

3.12 Consider the circuit of Fig. 3.6(b) in the event that the input source has a source resistance R_s . For example, $R_s = 1\text{k}\Omega$ assuming the diode to be real, sketch and clearly label the transfer characteristic v_o versus v_i .

3.13 A square wave of 6-V peak-to-peak amplitude and zero average is applied to a circuit consisting of Fig. 3.6(a) and one 10kΩ resistor. What is the peak output voltage? What is the average output voltage that results? What is the peak diode current? What is the average diode current? What is the maximum reverse voltage across the diode?

3.14 Repeat Problem 3.3 for the situation in which the average voltage of the square wave is 2 V while its peak-to-peak voltage remains at 6 V.

*3.15 Design a half-wave rectifying circuit, assuming that in Fig. 3.1, load resistor R is such that current flows to the 12-V battery 20% of the time and has an average value of 100 mA. What peak-to-peak sine-wave voltage is required? What peak current is required? What peak diode current? What peak reverse voltage does the diode endure? If no values can be specified for every component in the circuit, the peak-to-peak voltage only is mentioned, what design would you choose to guarantee the no reverse biasing current? What fraction of the cycle does diode current flow? What is the average diode current? What is the peak diode current? What peak reverse voltage does the diode endure?

3.16 The circuit of Fig. P3.16 can be used in a switching system using one wire plus a common ground return. At any moment, the input has one of three values: +5 V, 0 V, -5 V. What is the state of the bridge for each input value? Note that the bridge can be located anywhere, such that there may be several of each type of connection, all in one world.

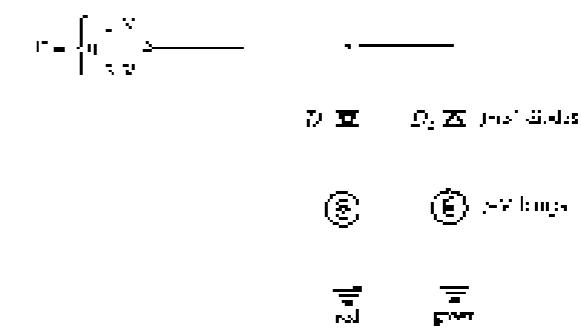


FIGURE P3.16

SECTION 3.2: TERMINAL CHARACTERISTICS OF JUNCTION DIODES

3.17 Calculate the value of the forward voltage, V_F , at -40°C, 0°C, +40°C, and +150°C. At what temperature is V_F exactly 25 mV?

3.18 At what forward voltage does a diode for which $n = 2$ conduct a current equal to 1000? To tens of I_0 , where current flows in the same diode when its forward voltage is 0.7 V?

3.19 A diode for which the forward voltage drop is 0.7 V at 1.0 mA and for which $n = 1$ is operated at 0.5 V. What is the value of the current?

3.20 A particular diode, for which $n = 1$, is found to conduct 2 mA with a junction voltage of 0.7 V. What is its saturation current I_0 ? What current will flow in this diode if the junction voltage is reduced to 0.1 V? To 0.5 V? To 0.9 V? What change in junction voltage will increase the diode current by a factor of 10?

3.21 The following measurements are taken on particular junction diodes to which V is the terminal voltage and I is the diode current. For each diode, estimate values of I_0 and n from an voltage at 1% of the measured current for $n = 1$ and for $n = 2$. Use $R_s = 2\Omega$ in your computations.

- $V = 0.700\text{ V}$ at $I = 1.00\text{ mA}$
- $V = 0.650\text{ V}$ at $I = 1.00\text{ mA}$
- $V = 0.600\text{ V}$ at $I = 10\text{ }\mu\text{A}$
- $V = 0.500\text{ V}$ at $I = 10\text{ }\mu\text{A}$

3.22 Listed below are the results of measurements done on several different junction diodes. For each diode, the data provided on the diode curve, 1, the corresponding diode voltage V_F , and the diode voltage at a current $I/10$. In each case, estimate I_0 , n , and the diode voltage at 100.

- 10 mA, 700 mV, 100 mV
- 1.0 mA, 700 mV, 100 mV
- 10 A, 800 mV, 100 mV
- 1 mA, 700 mV, 580 mV
- 10 μA , 700 mV, 640 mV

3.23 The circuit in Fig. P3.24 utilizes three identical diodes having $n = 1$ and $I_0 = 10^{-14}\text{ A}$. Find the value of the current I required to obtain a diode voltage $V_D = 2\text{ V}$. If a current of 1 mA is drawn away from the output terminal by a load, what is the change in output voltage?

3.24 A junction diode is operated in a circuit in which it is supplied with a constant current I . What is the effect on the forward voltage of the diode if an identical diode is connected in parallel? Assume $n = 1$.

3.25 In the circuit shown in Fig. P3.25, both diodes have $n = 1$, but D_1 has 10 times the A (area) of D_2 . What value

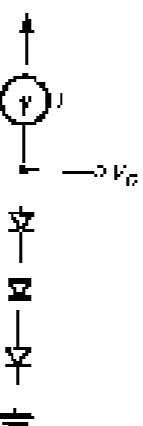


FIGURE P3.23

(a) V results? To obtain a value for V of 100 mV, what current I is needed?

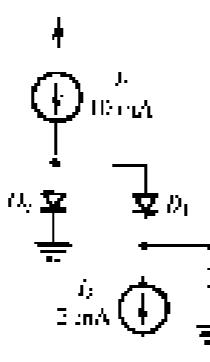


FIGURE P3.25

3.26 Using the circuit shown in Fig. P3.26, each diode is identical, conducting 10 mA at 0.7 V and 100 mA at 0.8 V. Find the value of R for which $V = 80\text{ mV}$.

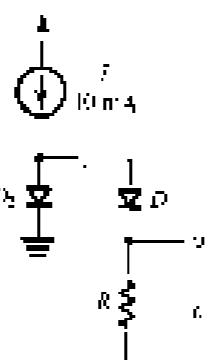


FIGURE P3.26

3.27 Several diodes having a range of sizes, but all with $n = 1$, are measured at various temperatures and their forward currents are noted below. For each, estimate the diode voltage at 1 mA and 25°C.

- 100 mV at $10\text{ }\mu\text{A}$ and 0°C
- 200 mV at 1 A and -50°C
- 250 mV at $100\text{ }\mu\text{A}$ and 100°C
- 350 mV at 10 mA and -50°C
- 500 mV at 100 mA and 100°C

3.28 In the circuit shown in Fig. P3.28, D_1 is a large-area肖特基 diode whose reverse voltage is high and independent of applied voltage, while D_2 is a much smaller, low-current diode for which $n = 1$. At an ambient temperature of 20°C , resistor R_1 is adjusted to make $V_{D1} = V_F = 320\text{ mV}$. Subsequent measurement indicates that R_1 is 750 Ω . What do you expect the voltages V_{D2} and V_F to become at 0°C and at 100°C ?

SECTION 3.3: MODELING THE DIODE FORWARD CHARACTERISTIC

3.32 Consider the graphical analysis of the diode circuit of Fig. 3.10 with $V_{DD} = 1\text{ V}$, $R = 1\text{ k}\Omega$, and a diode having $n = 0.7$ and $I_0 = 1$. Calculate a small number of points on the diode characteristic in the vicinity of where you expect the load line to intersect it, and use a graphical process to refine your estimate of diode current. What value of diode current and voltage do you find? Analytically, find the voltage corresponding to your estimate of current. By how much does it differ from the graphically estimated value?

3.33 Use the iteration-analysis procedure to determine the diode current and voltage in the circuit of Fig. 3.10 for $V_{DD} = 1\text{ V}$, $R = 1\text{ k}\Omega$, and a diode having $I_0 = 10^{-15}\text{ A}$ and $n = 1$.

3.34 A "1-A diode" (i.e., one that has $V_F = 0.7\text{ V}$ at $I_D = 1\text{ A}$) is connected in series with a 2 Ω resistor to a 1.0-V supply.

(a) Provide a rough estimate of the diode current you would expect.

(b) If the diode is characterized by $n = 2$, estimate the diode current more closely using iterative analysis.

3.35 A collection of diodes with area A that shown in Fig. 3.10 are listed below. For each diode used, the measured junction current I_0 at junction voltage $V_F = 0$ is provided, along with the change of junction voltage ΔV measured when the current is increased 10-fold. For each diode, consider the use of a large diode to establish a so-called relatively constant voltage. A power diode, for which the nominal current at 0.8 V is 10 A, is available. Furthermore, the designer has reason to believe that $n = 2$. For the available

current source, which can go from 0.5 mA to 1.5 mA, what junction voltage might be expected? What additional voltage change might be expected for a temperature variation of $+125^\circ\text{C}$?

3.36 As an alternative to the idea suggested in Problem 3.20, the designer employs a second op-amp to produce a relatively constant small voltage from a variable current supply. It relies on the ability to make quite accurate copies of any small current that is available (using a process called current mirroring). The designer proposes to use the idea of using two diodes in differential fashion, with the same current, and to measure their junction-voltage difference. Two types of diodes are available for a forward voltage around 200 mV, one conducts 0.1 mA while the other conducts 1 A. Now, for identical currents in the range of 0.5 mA to 1.5 mA supplied to each, what range of voltage differences result? What is the effect of a temperature change of 125°C on this arrangement? Assume $n = 1$.

SECTION 3.4: MODELING THE DIODE REVERSE CHARACTERISTIC

3.37 Consider the graphical analysis of the diode circuit of Fig. 3.10 with $V_{DD} = 1\text{ V}$, $R = 1\text{ k}\Omega$, and a diode having $n = 0.7$ and $I_0 = 1$. Calculate a small number of points on the diode characteristic in the vicinity of where you expect the load line to intersect it, and use a graphical process to refine your estimate of diode current. What value of diode current and voltage do you find? Analytically, find the voltage corresponding to your estimate of current. By how much does it differ from the graphically estimated value?

3.38 Use the iteration-analysis procedure to determine the diode current and voltage in the circuit of Fig. 3.10 for $V_{DD} = 1\text{ V}$, $R = 1\text{ k}\Omega$, and a diode having $I_0 = 10^{-15}\text{ A}$ and $n = 1$.

3.39 When a 1.5-A current is applied to a particular diode, it is found that the junction voltage immediately becomes 200 mV. Likewise, as the power being dissipated in the diode raises its temperature, it is found that the voltage decreases and eventually reaches 180 mV. What is the apparent rise in junction temperature? What is the power dissipated in the diode at this state? What is the temperature rise per watt of power dissipation? (This is called the thermal α coefficient.)

3.40 A designer of an instrument that must operate over a wide supply-voltage range, noting that a diode's junction-voltage drop is relatively independent of junction current, considers the use of a large diode to establish a so-called relatively constant voltage. A power diode, for which the nominal current at 0.8 V is 10 A, is available. Furthermore, the designer has reason to believe that $n = 2$. For the available

or them, and often make your life easier at circuit design much easier and faster!

	V_{DSS} (V)	I_{SD} (mA)	β_D (mV)	γ_D (mV)
1	0.05	1.0	1.0	100
2	0.1	1.0	1.0	100
3	0.2	1.0	1.0	100
4	0.3	1.0	1.0	100
5	0.4	1.0	1.0	100
6	0.5	1.0	1.0	100
7	0.6	1.0	1.0	100
8	0.7	1.0	1.0	100
9	0.8	1.0	1.0	100
10	0.9	1.0	1.0	100

3.3.34 Assuming the availability of diodes for which $\alpha = 2.0$, $V_A = -1$ mA, and $\kappa = 1$, design a circuit to limit the total diode current to 10 mA, in series with a 10-V source, to a maximum of 10-V power supply. The voltage across the string of diodes is to be 1.0 V.

3.3.35 Find the V -parameters of a piecewise-linear model for a diode, in which $v_1 = 0.7$ V at $i_1 = 1$ mA and $\kappa = 2$. The model is to fit exactly at 1 mA and 10 mA. Calculate the error in mW/mV in predicting v_2 using the piecewise linear model at $i_2 = 0.5$ mA and 4 mA.

3.3.36 Using a copy of the diode curve presented in Fig. 3.12, approximate the diode characteristic using a straight line that exactly matches the diode characteristics at both 1 mA and 10 mA. What is the slope? What is v_2 if $V_{DD} = 10$ V?

3.3.37 On a copy of the diode characteristics presented in Fig. 3.12, draw a load line corresponding to an output circuit consisting of a 10-V voltage source and a 1 kΩ resistor. What are the values of diode drop and load current you estimate using

- (a) the total diode characteristics?
- (b) the two-segment model shown?

3.3.38 For the circuit illustrated below, find v_{D1} and v_{D2} . On sketches of the bakery-piece-resistor model for which the straight line intersects the diode exponential characteristic at $i_1 = 1$ mA and $10 \times$ the specified diode current

- (a) $V_D = 0.7$ V if $i_1 = 1$ mA and $\kappa = 1$
- (b) $V_D = 0.7$ V if $i_1 = 1$ A and $\kappa = 1$
- (c) $V_D = 0.7$ V if $i_1 = 10 \mu$ A and $\kappa = 1$

3.3.39 A diode whose characteristic curve is shown in Fig. 3.13 is to be operated at 10 mA. What will it likely be a suitable voltage-controlled-current appropriate small-signal cap model?

3.3.40 A diode operates in a series circuit with $V = 1$ V. A designer, considering using a constant voltage model, is

uncertain whether to use 0.7 V or 0.6 V for V_D . For what value of V is the difference in the calculated values of α (not only 1%)? For $V = 2$ V, say, $R = 1$ kΩ, what two currents would result from the use of the two values of V_D ? What is their percentage difference?

3.3.41 A designer has a relatively large number of diodes, for which a current of 20 mA flows at 0.7 V and the 10-A diode approximation is relatively good. Using a 10-A current source, the designer wishes to obtain a reference voltage of 1.02 V. Suggest a combination of series and parallel diodes that will do the job as well as possible. How many diodes are needed? What voltage is actually achieved?

3.3.42 Consider the half-wave rectifier circuit of Fig. 3.7(a), with $R = 1$ kΩ and the diode having the characteristics and the equivalent-circuit model shown in Fig. 3.13 ($V_D = 0.65$ V, $\alpha = 0.02$). Apply the test-circuit analysis to the diode-coupled model for the diode, and then find the output voltage, v_o , as a function of v_i . Sketch the transfer characteristic v_o versus v_i for $0 \leq v_i \leq 10$ V. For v_i being a sinusoid with 10-V peak amplitude, sketch v_o (labelled v_{o1}) versus v_i .

3.3.43 Solve the problem in Example 3.2 using the constant-voltage-drop ($V_D = 0.7$ V) diode model.

3.3.44 For the circuit shown in Fig. 3.12, using the constant-voltage-drop ($V_D = 0.7$ V) diode model, find the voltages and currents in the circuit.

3.3.45 For the circuit shown in Fig. P3.5, using the constant-voltage-drop ($V_D = 0.7$ V) diode model, find the voltages and currents in the circuit.

3.3.46 For the circuit in Fig. P3.6, using Thévenin's theorem to simplify the circuit and find the values of the labeled currents and voltages. Assume that nonlinear diodes can be represented by the constant-voltage-drop model ($V_D = 0.7$ V).

3.3.47 Repeat Problem 3.11, representing the diode by its constant-voltage-drop ($V_D = 0.7$ V; more). How different is the resulting design?

3.3.48 Repeat the problem in Example 3.1, assuming that the diode has 10 times the area of the device whose characteristic and piecewise-linear model are employed in Fig. 3.12. Represent the diode by the piecewise-linear model ($\alpha = 0.65$; $\beta_D = 1$).

3.3.49 The small-signal model is said to be valid for voltage variations of about 0.1 mV. To what percentage current change

does this correspond for a diode with negative resistance?

- (a) 0.1%
- (b) 0.2%

For each case, what is the minimum allowable voltage signal for each case, so that the current change is to be limited to 0.05%?

3.3.50 In a particular circuit application, ten "20-mA" diodes" (a 20-mA diode is a diode that provides a 0.7 V drop when a current through it is 20 mA) are connected in parallel, operating at a total current of 0.1 A. For the diodes closely matched, at 0.1 A of current, there is no drift. What is the overvoltage if all current flows in one? What is the overvoltage if the specifying small-signal resistance of each diode and of the circuit is 10 mΩ? Compare this with the incremental resistance of a single diode connected at 0.1 A. If each of the 20-mA of a single diode is connected with a 0.2 Ω associated with the diode, has a series resistor of 0.2 Ω associated with the wire bonds in the junction, what is the equivalent resistance of the 10 pairs of connected diodes? What connection resistances are the single diode need to be very low (10^{-3} Ω)? This is why the parallel connection of 10 diodes is often preferred to advantage.

3.3.51 In the circuit shown in Fig. P3.54, i_1 is a DC current of 1 mA, v_i is a 1-V sinusoidal signal. Capacitors C_1 and C_2 are very large, their function is to couple the signal to and from the circuit but block the DC current from flowing into the signal source or the load (not shown). Use the diode as a digital model to show the AC component of the output voltage.

$$v_o = \frac{a_1 v_i}{V_D + V_T + R_s}$$

If $a_1 = 10$ mV, $i_1 = 1$ mA, for $V_D = 0.7$ V, $i_1 = 1$ mA, and $R_s = 1$ kΩ and $\kappa = 2$. At what value of i_1 does v_o become one-half of a_1 ? Note that this current functions as a signal attenuator with the diode as an active controller by the value of the diode current?

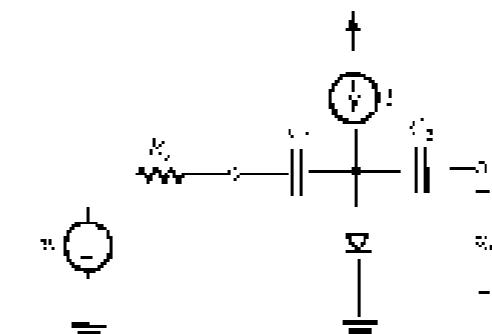


FIGURE P3.54

3.3.52 In the circuit of Fig. P3.51, if $R_s = 0.2\Omega$, the diode is a 1 mA diode ($i_1 = 1$ mA), it exhibits a voltage drop of 0.7 V and a current of 1 mA, $i_1 = 1$. For small input signals, what value of current i_2 is needed for $v_o/v_i = 0.50$? If $i_2 = 0.01$, $i_1 = 0.01$? In each case, what is the largest input signal that can be used while ensuring that the signal component of the diode current is limited to 10% of its DC current? What might happen otherwise?

3.3.53 In the capacitor-coupled oscillator circuit shown in Fig. P3.50, i_1 is a DC current that varies linearly from 0 mA to 1 mA. D_1 and D_2 are diodes with $\kappa = 2$ and C_1 and C_2 are large coupling capacitors. For very small input signals, find the values of the ratio v_o/v_i for $i_1 = 0$ mA.

- (a) 0.01
- (b) 0.02
- (c) 0.04
- (d) 0.1
- (e) 0.01
- (f) 0.02
- (g) 0.04
- (h) 0.1

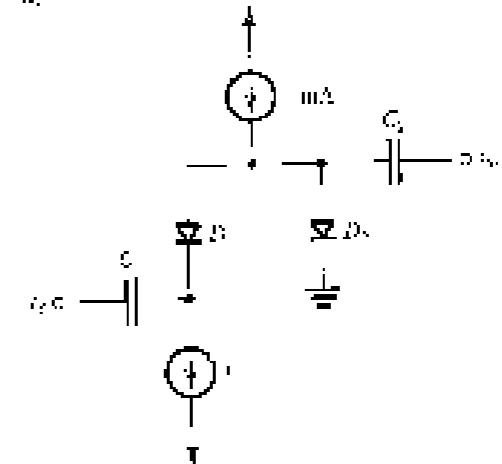


FIGURE P3.53

For the current in each diode in excess of 10 μA, what is the largest input signal for which the diode current is not more than 10% of its DC value?

3.3.54 In the circuit shown in Fig. P3.54, diodes D_1 through D_4 are identical. Each has $\kappa = 1$ and C is a 1-pF capacitor that exhibits a voltage drop of 0.7 V at 1 mA current. Find the values of the four input signals v_1 , v_2 , v_3 , and v_4 for various values of v_o if the small-signal transmission v_o/v_i for various values of v_i is 0.05, 1 mA, 10 mA, 100 mA, 1 mA, and 10 mA.

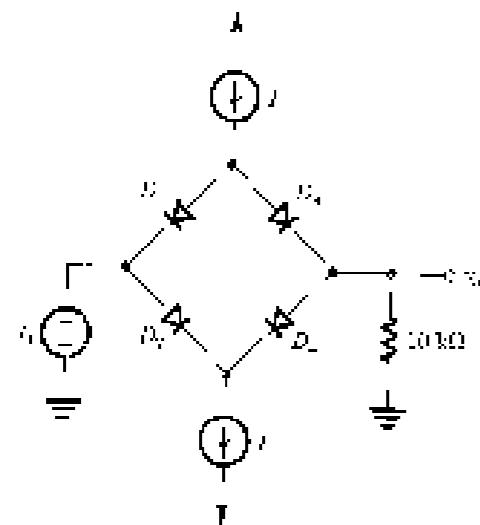


FIGURE P3.59

- (a) For a forward-biased zener diode, what is the largest signal voltage magnitude that can support while the corresponding signal current I_{ZS} is limited to 1% of the dc bias current? Now, for the circuit in Fig. P3.59, if a 20-mV peak input, what is the smallest value of R_L for which the diode currents remain within ±1% of their dc values?
 (b) If $I_{ZS} = 1 \text{ mA}$, what is the largest possible output signal for which the diode currents remain by at most 1% of their dc values? What is the corresponding peak input?

- *P3.58 In the circuit shown in Fig. P3.58, I_{ZS} is dc current and i_s is a sinusoidal signal with small amplitude (less than 0.1 V) and a frequency of 100 kHz. Representing the zener by its small-signal resistance r_Z , which is a function of V_Z , sketch the circuit for calculating the sinusoidal output voltage V_o , and thus find the phase shift between V_o and V_s . Plot the value of V_o that will provide a phase shift of -45°, and find the range of phase shift achieved as V_s is varied over the range of 0 to 20 times the zener voltage. Assume $n = 1$.

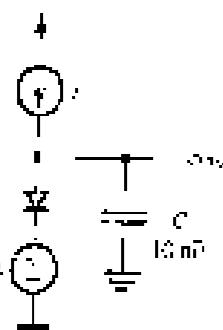


FIGURE P3.58

*P3.59 Consider the voltage-regulating circuit shown in Fig. P3.59. The value of K is selected to obtain an output voltage V_o across the load resistor of 0.7 V.

- (a) Use the diode small-signal model to show that the change in output voltage corresponding to a change of 1 V in V^+ is

$$\frac{\Delta V_o}{\Delta V^+} = \frac{K V_Z}{V^+ + K V_Z + 0.7}$$

This quantity is known as the line regulation and is usually expressed in mV/V.

- (b) Generalize the expression above for the case of two diodes connected in series and K adjusted so that the voltage across each diode is 0.7 V (and $V_o = 0.7 \text{ V}$).
 (c) Calculate the value of line regulation for the case $V^+ = 10 \text{ V}$ (assuming $V_Z = 5.6 \text{ V}$ and $K = 100$) ($\Delta V_o = ?$). Use $n = 1$.



FIGURE P3.59

- *P3.60 Consider the voltage-regulating circuit shown in Fig. P3.60 under the condition that a load current I_L is drawn from the output terminal.

- (a) If the value of R_L is sufficiently small so that the corresponding change in regulator output voltage ΔV_o is small enough to justify using the diode small-signal model, show that

$$\frac{\Delta V_o}{I_L} = -r_Z(R_R)$$

This quantity is known as the load regulation and is usually expressed in mV/mA.

- (b) If the value of R_L is selected such that across the voltage V_Z across the diodes is 0.7 V and the load current I_L is 50, show that the expression derived in (a) becomes

$$\frac{\Delta V_o}{I_L} = \frac{n V_Z}{I_L} \frac{V^+ - 0.7}{0.7 + n V_Z}$$

- Select the lowest possible value for I_L ; the results in a load regulation of 5 mV/mA. Assume $n = 2$, $V^+ = 10 \text{ V}$, and $V_Z = 0.7 \text{ V}$. What value of R_L is required? What is the supply current I_S of the diode required?

- (c) Use the line expression derived in (b) for the case of one diode connected in series and K adjusted so that $V_o = 0.7 \text{ V}$ when $I_L = 0$.

- (d) Design a zener voltage regulator to supply 1.2 V over 150 mA load. The two diodes specified have a 0.7 V drop at current of 10 mA and $n = 1$. The load needs to be connected to a 5-V supply through a resistor R . Supply the value for R . What is the output voltage with the load connected? What is the maximum rating of the power supply when the load is disconnected? What would happen if the load resistance is reduced to 100 Ω? To 75.427 Ω to 70.427 Ω?

- *P3.62 A voltage regulator consisting of two diodes in series fed with a constant-current source is used as a replacement for a single zener-diode cell (series of equal voltage 1.2 V). The regulator load current varies from 2 mA to 7 mA. Constant-current supplies of 5 mA, 10 mA, and 15 mA are available. Which would you choose, and why? What change in output voltage would result when the load current varies over its full range? Assume that the diodes have $n = 1$.

- *P3.63 A particular design of a voltage regulator is shown in Fig. P3.63. Diodes D_1 and D_2 are 1.0 mA units; that is, exclusive voltage drop of 1 V at current of 1.0 mA. Load $R_L = 1$.

- (a) What is the regulator current in reg. V_o with an 180-Ω load, estimated?

- (b) Find V_o with no load.

- (c) With the load removed, to what value can the 5-V supply be lowered while maintaining the loaded output voltage within 0.1 V of its normal value?

- (d) What does the loaded output voltage become when the 5-V supply is raised by the same amount as the drop found in (c)?

- (e) For the two values of charges explored in (c) and (d), by how many percentage does the current in D_2 change? At what percentage change of supply voltage would D_2 cease to conduct?

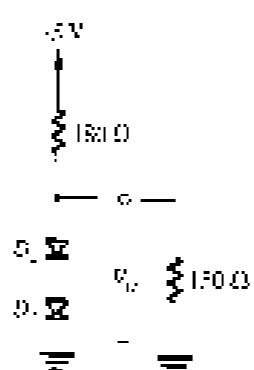


FIGURE P3.63

SECTION 3.4: OPERATION IN THE REVERSE BREAKDOWN REGION—ZENER DIODES

- P3.64 Partial specifications of a silicon $n-p-n$ zener diode are provided below. Identify the missing parameter and estimate its value. Note from Fig. 3.23 that $V_{BR} = V_Z$.

- (a) $V_Z = 10.0 \text{ V}$, $I_{ZS} = 80 \text{ nA}$, and $I_Z = 50 \text{ mA}$

- (b) $I_Z = 10 \text{ mA}$, $V_Z = 9.1 \text{ V}$, and $r_Z = 0.1 \Omega$

- (c) $r_Z = 2 \Omega$, $V_Z = 6.8 \text{ V}$, and $V_{BR} = 0.8 \text{ V}$

- (d) $r_Z = 4 \Omega$, $I_{ZS} = 10 \text{ nA}$, and $V_{BR} = 12.2 \text{ V}$

- (e) $I_{ZS} = 200 \text{ nA}$, $V_Z = 7.5 \text{ V}$, and $r_Z = 0.5 \Omega$

Assuming that the power rating of a breakdown diode is proportional to about twice the specified zener current (I_{ZS}), what is the power rating of each of the diodes described above?

- P3.65 A designer requires a shunt regulator of approximately 20 V. Two kinds of zener diodes are available: $p-n-p$ devices with $n = 10.0$ and $n = 4$ devices with $n = 50.0$. For the most negative values possible, find the load regulation. In this calculation neglect the effect of the regulator resistance R .

- P3.66 A shunt regulator utilizing a zener diode with an internal resistance of 1.0 Ω is fed through an 82-Ω resistor. If the raw supply changes by 1.3 V, what is the corresponding change in the regulated output voltage?

- P3.67 A 4.91-V zener diode exhibits its nominal voltage at a current of 28 mA. At this current, the more normal resistance is specified as 0.2 Ω. Find V_o of the zener diode, given the zener voltage at an output current of 4 mA at 100 mA.

- P3.68 Design a 7.5-V zener-regulator circuit using a 3.5-V zener specified at 10 mA. The zener has an internal resistance $r_Z = 10 \text{ } \Omega$ and a current of 0.5 mA. The regulator operates at a 10-V supply and has a 1.0 mA load. What is the value of R_{ZD} have chosen? What is the regulator output voltage when the supply is 10% higher or lower? What is the output voltage when the supply is 10% higher or the load is removed? What is the smallest possible load resistor that can be used while the zener operates at a current no lower than the knee current, while the supply is 10% low?

- *P3.69 Provide two designs of shunt regulators of 10-V for 1N3235 zener diodes, which is specified as follows: $V_Z = 6.8 \text{ V}$ and $I_{ZS} = 5.22$ for $I_Z = 2.1 \text{ mA}$, and $r_Z = 0.25 \text{ m} \Omega$ nearer the knee, $r_Z = 10 \text{ } \Omega$. For both designs, the supply voltage is nominally 10 V and varies by ±1 V. For the first design, assume that the availability of a low-current zener is not a problem, and thus operate the diode at 20 mA. For the second design, assume that the current from the raw supply is limited, and therefore you are forced to operate the diode at 0.35 mA. For the first pair of these initial designs, assume no load. For each design, find the value of R and the line regulation.

- P3.70** A zener diode regulator employs a 9.1-V zener diode for $-V_{ZD} = 9.1$ V and $I_Z = 0.1$ A, with $r_z = 30 \Omega$ and $I_{SD} = 0.3$ mA. The available supply voltage of 15 V can vary as much as 10%. If V_o is a diode, what is the value of R_L ? For a nominal load resistance $R_L = 1\text{ k}\Omega$ and a zener current of 10 mA, what current must flow in the zapping cells at R^2 ? For the nominal value of supply voltage, calculate a value for resistor R_1 specified to one digit. Assume that V_o provides an average output voltage of 9.1 V. What is the percentage change in the supply voltage, when variation in output voltage is $\pm 2\%$? If the zener current is reduced by 50%, what increase in V_o results? What is the shunt series load resistance that can be tolerated while maintaining regulation when the supply voltage is varied? What is the lowest peak-to-average voltage ratio? Calculate values for the maximum voltage and for the load regulation for this circuit, if using the numerical results obtained in this problem.

- P3.71** It is required to design a zener diode regulator to provide a regulated voltage of about 10 V. The available 10-V zener diode type 1N4740 is specified to have a 10-V drop across its terminals at 30 mA. At this current, $r_z = 7 \Omega$. The first-supply available load current value of 20 V has a tolerance of $\pm 5\%$. The regulator is required to supply a load current of 10 A to 20 mA. Design for a minimum zener current of 2 mA. (a) $R_o = ?$

(b) Calculate the required value of R_1 .

- (c) For the line regulation, what is the change in V_o expressed as a percentage, corresponding to the $\pm 5\%$ change in V_s ?

(d) Find the load regulation. By what percentage does V_o change from no load to the full-load condition?

- (e) What is the maximum current that the zener in your design is required to conduct? What is the zener power dissipation under this condition?

SECTION 3.5: RECTIFIER CIRCUITS

- P3.72** Consider the half-wave rectifier circuit of Fig. 3.25(a) using a zener diode reversed. Let V_o be a sinusoid with 15-V peak amplitude, and let $R = 1\text{ k}\Omega$. Use the constant-voltage-zener model with $V_z = 0.7$ V.

(a) Sketch the transient characteristics.

(b) Sketch the wave form of v_o .

(c) Find the average value of v_o .

(d) Find the peak current in the zener.

(e) Find the PIV of the zener.

- P3.73** Using the exponential diode characteristic, show that for $v_o > v_z$, the $i_o = -I_{SD}(1 - e^{-v_o/R})$ in Fig. 3.25(a) has the following characteristics:

$$i_o = v_o - v_z \quad \text{and} \quad i_o = -I_{SD}(1 - e^{-v_o/R})$$

where v_o and v_z are in volts and R is in kilohms.

- P3.74** Consider a half-wave rectifier circuit with a triangular-wave input of 5 V, with a peak amplitude and zero average sum with $R = 1\text{ k}\Omega$. Assume that the diode can be represented by the piecewise-linear model with $V_{zD} = 0.65$ V and $I_{SD} = 20$ mA. Find the average value of v_o .

- P3.75** For a full-wave rectifier circuit with $N = 1\text{ k}\Omega$, utilizing a diode with one-half V_o drop in 0.7 V at a current of 1 mA and exhibiting a 0.1-V change per decade of current, determine the value of the input voltage in the ac-tetra converter speed range for $v_s = 0.1$ V, 0.5 V, 1 V, 2 V, 5 V, and 10 V. Plot the resulting transfer characteristics.

- P3.76** A half-wave rectifier circuit with a 1-kΩ load operates from a 120-V rms 60-Hz household supply through a 10-to-1 step-down transformer. It uses a silicon diode that can be modeled to have a 0.7-V drop for any current. What is the peak voltage of the rectified output? For what fraction of the cycle does the diode conduct? What is the rectified output voltage? What is the average current in the load?

- P3.77** A full-wave bridge rectifier circuit with a 1-kΩ load operates from a 120-V rms 60-Hz household supply through a 10-to-1 step-down transformer having a complex secondary winding. It uses four diodes, each of which can be modeled to have a 0.7-V drop for any current. What is the peak value of the modified voltage of the 120-V load? For what fraction of a cycle does each diode conduct? What is the average current in the load?

- P3.78** A full-wave bridge rectifier circuit with a 1-kΩ load operates from a 120-V rms 60-Hz household supply through a 10-to-1 step-down transformer having a complex secondary winding. It uses four diodes, each of which can be modeled to have a 0.7-V drop for any current. What is the peak value of the modified voltage of the 120-V load? For what fraction of a cycle does each diode conduct? What is the average current across the load? What is the average current through the load?

- P3.79** It is required to design a full-wave rectifier circuit using the circuit of Fig. 3.26 to provide an average output voltage of:

(a) 12 V

(b) 100 V

In each case find the required turns ratio of the transformer. Assume that a conducting diode has a voltage drop of 0.7 V. The ac-line voltage is 120 V rms.

- P3.80** Repeat Problem 3.79 for the bridge rectifier circuit of Fig. 3.27.

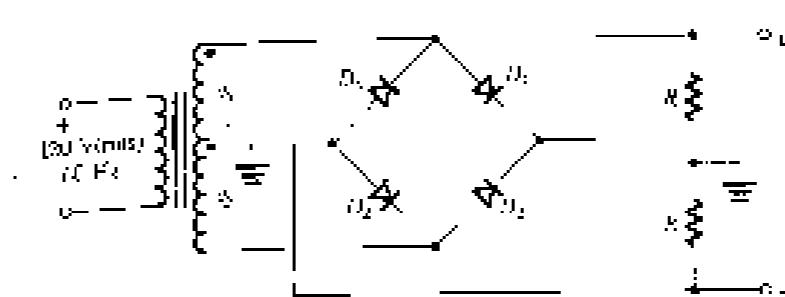


FIGURE P3.82

- P3.81** Consider the full-wave rectifier in Fig. 3.26 with a transformer in which it is calculated that the voltage across the entire secondary windings is 21 V rms. If the input ac-line voltage (120 V rms) is increased by as much as 10%, and the rectified PIV of the diodes is remembered to use a factor of safety in your design:

- (a) Find the maximum reverse voltage that will appear across the diodes, and specify the PIV rating of the diodes.
- (b) Calculate the average current through the diode during conduction.
- (c) Calculate the peak diode current.

- P3.82** Repeat Problem 3.81 for the case in which the designer opts for a full-wave circuit using a center-tapped transformer.

- P3.83** Repeat Problem 3.86 for the case in which the designer uses the half-wave bridge rectifier circuit.

- P3.84** Consider the rectifier circuit of Problem 3.67 with a capacitor chosen to produce a peak-to-ripple voltage ratio of 10% of the peak output and 100% of the peak output at each case:
- What is the peak-to-ripple voltage ratio?
 - What fraction of the cycle does the diode conduct?
 - What is the average diode current?
 - What is the peak diode current?

- P3.85** Repeat Problem 3.83 for the results in Problem 3.77.

- P3.86** It is required to design a peak-to-peak rectifier to deliver a dc power supply that provides an average dc output voltage of 15 V and a maximum of $\pm 1\%$ ripple is allowed. The rectifier loads a load of 100 Ω. The rectifier is fed from the ac voltage (120 V rms, 60 Hz) through a transformer. The diodes available have 0.7-V drop per diode conduction. If the designer opts for the half-wave rectifier:

- Specify the voltage that must appear across the transformer secondary.
- Find the required value of the filter capacitor.

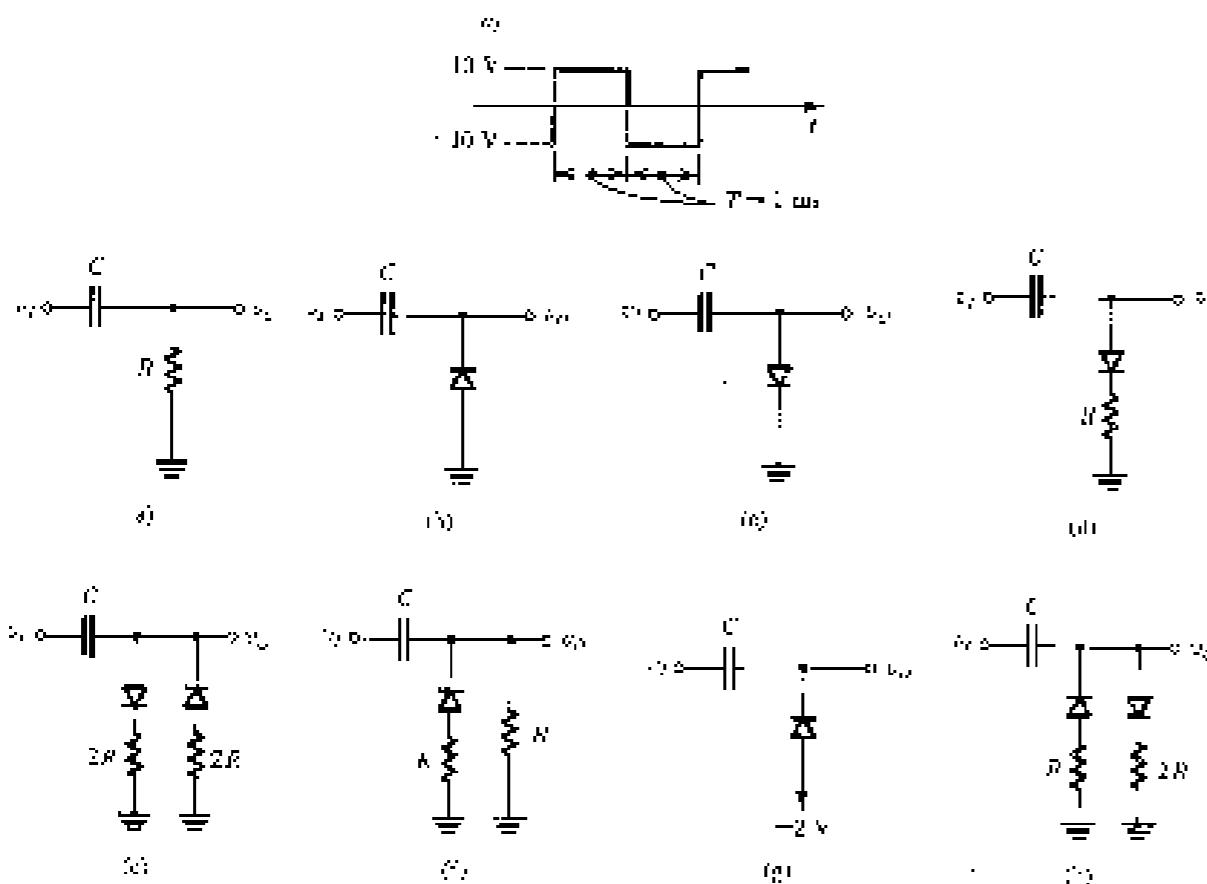


FIGURE P3.105

SECTION 3.7: PHYSICAL OPERATION OF DIODES

Note: If in the following problems the need arises for the values of particular parameters or physical constants that are not stated, refer to Table 3.1.

3.106 Find values of the intrinsic carrier concentration N_i in silicon at 300 K, 100 K, 200 K, 1000 K, and 1250 K. At each temperature, what fraction of the atoms is ionized? Recall that a silicon crystal has approximately 5×10^{22} atoms/cm³.

3.107 A young designer, aiming to develop integrated circuitizing conducting paths within an integrated circuit, examines the end-to-end resistance of a connecting bar 10 μm long, 0.5 μm wide, and 1 μm thick made of various materials. The designer considers:

- (a) aluminum
- (b) n -type silicon with $N_d = 10^{16} \text{ cm}^{-3}$
- (c) p -doped silicon with $N_d = 10^{16} \text{ cm}^{-3}$
- (d) n -doped silicon with $N_d = 10^{18} \text{ cm}^{-3}$
- (e) aluminum with resistivity of 1.5 $\mu\Omega \cdot \text{cm}$

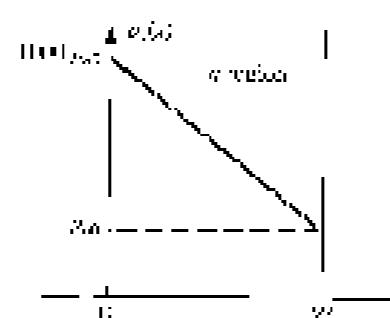


FIGURE P3.108

Find the resistance in each case. For aluminum, use the data in Table 3.2. For n -type silicon, assume $\mu_n = 2.3\mu_0 = 200 \text{ cm}^2/\text{V}\cdot\text{s}$. (Recall that $J = D_s E/A$.)

3.108 Electrons are being steadily injected into a region of n -type silicon (connected to the anode) of a device. The details of the device are important for this problem. In the steady state, the excess-hole concentration profile shown in Fig. P3.109 is established in the n -type silicon region. Here "excess" means

carrier excesses due to concentration N_d . If $N_d = 10^{16} \text{ cm}^{-3}$, $n_0 = 3.5 \times 10^{10} \text{ cm}^{-3}$, and $W = 5 \mu\text{m}$, and the carrier n is constant throughout the n -region,

3.109 Calculate the electron and hole drift velocities through a $10\text{-}\mu\text{m}$ layer of intrinsic silicon across which a voltage of 3 V is impressed. Let $\mu_e = 159 \text{ cm}^2/\text{V}\cdot\text{s}$ and $\mu_h = 480 \text{ cm}^2/\text{V}\cdot\text{s}$.

3.110 Find the current flow in a 5 μm bar of silicon having a $5\text{-}\mu\text{m} \times 5\text{-}\mu\text{m}$ cross-section and having free-electron and hole densities of 10^{16} cm^{-3} and 10^{15} cm^{-3} , respectively, with 1 V applied end-to-end. The $\mu_e = 1200 \text{ cm}^2/\text{V}\cdot\text{s}$ and $\mu_h = 500 \text{ cm}^2/\text{V}\cdot\text{s}$.

3.111 In a 20 μm long bar of donor-doped silicon, what carrier concentration is needed to realize a current density of $1 \text{ mA}/\text{cm}^2$ in response to an applied voltage of 1 V? (Assume $\mu_n = 1000 \text{ cm}^2/\text{V}\cdot\text{s}$.) Although the carrier n varies, change with volume concentration N_d (see the table associated with Problem 3.105), as a first approximation you may assume μ_n to be constant and use the value for intrinsic silicon, $100 \text{ cm}^2/\text{V}\cdot\text{s}$.

3.112 In a phosphorous-doped silicon layer with impurity concentration of 10^{16} cm^{-3} , find the hole and electron concentrations at 25°C if $n_0 = 125 \text{ cm}^{-3}$.

3.113 Both the carrier mobility and diffusion coefficient decrease as the doping concentration of silicon is increased. The following table provides a few data points for μ_n and D_s versus N_d concentration. Use the Peierls relationship to obtain the corresponding values for μ_p and D_p .

Concen-	μ_n (cm ² /V·s)	D_s (cm ² /s)	μ_p (cm ² /V·s)	D_p (cm ² /s)
10 ¹⁶	1300	450	10 ¹⁶	10 ¹⁶
10 ¹⁷	100	400	10 ¹⁷	10 ¹⁷
10 ¹⁸	10	200	10 ¹⁸	10 ¹⁸
10 ¹⁹	300	100	10 ¹⁹	10 ¹⁹

constant value of the p -type regions when the junction is reverse-biased with $V_b = 5 \text{ V}$. At this value of reverse bias, calculate the magnitude of the charge stored on either side of the junction. Assume the A_{min} at $x = 0$ is $400 \mu\text{m}^2$. Also, calculate C_s .

3.115 Estimate the total charge stored in a 0.1- μm depletion layer on one side of a $10\text{-}\mu\text{m} \times 10\text{-}\mu\text{m}$ junction, by neglecting concentration on that side of the junction ($N_d = 10^{16} \text{ cm}^{-3}$).

3.117 Combine Eqs. (3.52) and (3.53) to find q_s in terms of V_b . Differentiate this expression to find an expression for the junction capacitance C_s . Show that the expression you obtained is the same as the C_s it contained using Eq. (3.34) in conjunction with Eq. (3.52).

3.118 For a p-n junction in which $L_{\text{dr}} = 0.6 \mu\text{m}$, $V = 0.75 \text{ V}$, and $n_0 = 10^3$, find the capacitance at reverse-bias voltages of 1 V and 10 V.

3.119 An avalanche-diode operating code, for which the forward voltage is 12 V, has a rated power dissipation of 0.25 W. With continuous operating current will there be dissipation at half the maximum voltage? If breakdown occurs for only 0.1 s every 20 ms, what average breakdown current is allowed?

3.120 In a forward-biased p-n junction show that the ratio of the current component due to hole-injection across the junction to the component due to electron injection is given by

$$\frac{I_h}{I_e} = \frac{D_p}{D_n} \frac{k_B T}{N_d N_p}$$

Evaluate this ratio for the case $N_d = 10^{16} \text{ cm}^{-3}$, $N_p = 10^{15} \text{ cm}^{-3}$, $L_{\text{dr}} = 5 \mu\text{m}$, $L_{\text{sh}} = 0.5 \mu\text{m}$, $D_p = 10 \text{ cm}^2/\text{s}$, $D_n = 25 \text{ cm}^2/\text{s}$, and hence find I_h and I_e for the case $V = 0.75 \text{ V}$, the diode operating in a forward current $I = 1 \text{ mA}$.

3.121 A p-n diode is one in which the doping concentration in the n -region is 100 times greater than that in the p -region. In such a diode, the forward current is mostly due to hole-injection across the junction. Show that

$$I = I_0 = A_0 q^2 \frac{D_p}{L_{\text{dr}} N_p} (e^{qV/kT} - 1)$$

for the special case in which $N_d = 5 \times 10^{16} \text{ cm}^{-3}$, $N_p = 10^{15} \text{ cm}^{-3}$, $q = 1.6 \times 10^{-19} \text{ C}$, and $k = 10^{-23} \text{ J/K}$. Find I , assuming V obtained when $I = 0.2 \text{ mA}$. Assume operation at 200 K, where $n_0 = 1.5 \times 10^{10} \text{ cm}^{-3}$. Also, calculate the excess minority-carrier charge and the value of the diffusion capacitance $C_s = 0.1 \mu\text{F}/\text{cm}^2$.

***3.122** A short-base diode is one whose net widths of the p and n regions are much smaller than L_{dr} and L_{sh} , respectively. As a result, the excess minority carriers distributed in each

which is a straight-line relation from the exponential form in Eq. 3.50.

- (2) For the drift-base diode, choose a diode corresponding to Fig. 3.50 and assume, as in Fig. 3.51, that $N_A > N_D$. Following a derivation similar to that given on page 206–205, show that if we add the p and n regions to become N_A and N_D , then

$$I = A_0 \mu_0 \left[\frac{D_A}{(W_1 + x_1) D_D} + \frac{D_D}{(W_2 - x_2) D_A} \right] (e^{V_{DS}/V_T} - 1)$$

and

$$V_{DS} = \frac{1}{2} \frac{(W_1 + x_1)^2}{D_A} I_D$$

$$= \frac{1}{2} \frac{(W_1 + x_1)^2}{D_D} I_D \quad \text{for } W_1 \gg x_1$$

(3) Also, assuming $V = V_{DS}$, show that

$$C_D = \frac{\pi^2}{3} L$$

$$C_D = \frac{1}{2} \frac{W_1^2}{D_D}$$

- (4) If a design requires that C_D be 8 pF at $I = 1$ mA, what should V_{DS} be? Assume $D_A = 10 \text{ cm}^2/\text{A}$.

MOS Field-Effect Transistors (MOSFETs)

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INTRODUCTION

Having studied the junction diode, which is the most basic two-terminal semiconductor device, we now turn our attention to three-terminal semiconductor devices. Three-terminal devices are far more useful than two-terminal ones because they can be used in a multitude of applications, ranging from signal amplification to digital logic and memory. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way a three-terminal device can be used to realize a controlled source, which as we have learned in Chapter 3 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the three-terminal to change from zero to a large value, thus allowing the device to act as a switch. As we also

taught in Chapter 1, the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

There are two major types of four-terminal semiconductor device: the metal-oxide-semiconductor field-effect transistor (MOSFET), which is studied in this chapter, and the bipolar junction transistor (BJT), which we shall study in Chapter 5. Although each of the two transistor types offers unique features and areas of application, the MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are typically fabricated on a single silicon chip.

Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple (see Appendix A). Also, their operation requires comparatively little power. Furthermore, circuit designers have found ingenious ways to implement digital and analog functions utilizing MOSFETs almost exclusively (i.e., with very few or no resistors). All of these properties have made it possible to pack large numbers of MOSFETs (or BJT equivalents) on a single IC chip to implement very sophisticated, very large-scale integrated (VLSI) circuits such as those for memory and microprocessors. Analog circuits such as amplifiers and filters are also implemented in MOS technology, albeit in smaller less-dense chips. Also, both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

The objective of this chapter is to develop in the reader a high degree of familiarity with the MOSFET: its physical structure and operation, terminal characteristics, circuit models, and basic circuit applications, both as an amplifier and a digital logic inverter. Although discrete MOS transistors exist, the material studied in this chapter will enable the reader to design discrete MOS circuits. Our study of the MOSFET is strongly influenced by the fact that most of its applications are in integrated-circuit design. The design of IC analog and digital MOS circuits occupies a large portion of the remainder of this book.

4.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

The enhancement-type MOSFET is the most widely used field-effect transistor. In this section, we shall study its structure and physical operation. This will lead to the current-voltage characteristics of the device, studied in the next section.

4.1.1 Device Structure

Figure 4.1 shows the physical structure of the n-channel enhancement-type MOSFET. The meaning of the terms "enhancement" and "n-channel" will become apparent shortly. The transistor is fabricated on a p-type substrate, which is a single-crystal silicon wafer that provides physical support for the device and for the entire circuit in the case of an integrated circuit. Two heavily doped n-type regions, indicated in the figure as the "Source¹" and the "Drain region," are created in the substrate. A thin layer of silicon dioxide (SiO_2) of thickness t_2 (typically 2–50 nm)², which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made in the source region, the drain region, and the substrate, also known as the

¹ The term n-type denotes heavily doped n-type silicon. Conversely, p-type is used to denote lightly doped n-type silicon. Similar notation applies for p-type silicon.

² A nanometer (nm) is 10^{-9} m or 0.001 μm. A micrometer (μm) is 10^{-6} m. Sometimes the oxide thickness is expressed in angstroms. An angstrom (Å) is 10^{-10} m, or 10^{-8} nm.

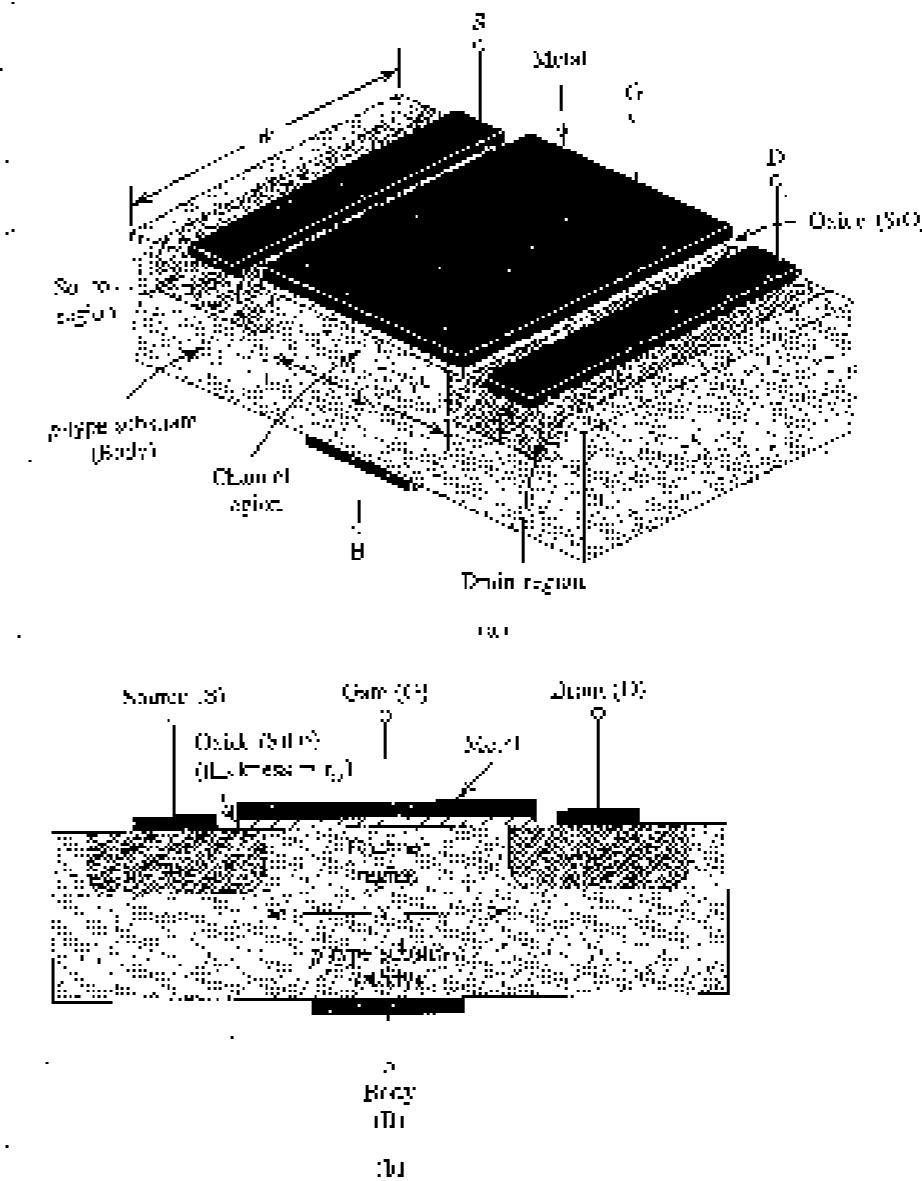


FIGURE 4.1 Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically, $t_1 = 0.1$ to 1 μm, $t_2 = 0.1$ to 100 nm, and the thickness of the oxide layer (t_3) is in the range of 2 to 50 nm.

body.¹ Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

At this point it should be clear that the name of the device (metal-oxide-semiconductor FET) is derived from its physical structure. The name, however, has become a generic one and is

¹ In Fig. 4.1, the contact to the body is shown on the bottom of the device, which is proved to be later in explanation a phenomena known as the "body effect." It is important to note, however, that in actual ICs, a contact to the body is made at a location on the top of the device.

used also for HEMTs that do not use metal for the gate electrode. In fact, most modern MOSFETs are fabricated using a process known as *electron-gate technology*, in which a certain type of silicon, called polysilicon, is used to form the gate electrode (see Appendix A). Our description of MOSFET operation and characteristics applies irrespective of the type of gate electrode.

Another name for the MOSFET is the *insulated-gate FET* or *IGFET*. This name also arises from the physical structure of the device, in particular the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the drain terminal to be extremely small (of the order of 10^{-14} A).

Observe that the substrate connection is made with the source and drain regions. In normal operation these pn junctions are kept reverse-biased at all times. Since the drain will be at a positive voltage relative to the source, the two pn junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. We shall assume this to be the case in the following description of MOSFET operation. Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D). It will be shown that a voltage applied to the gate creates current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled "channel region." Note that this region has a length L and a width W , two important parameters of the MOSFET. Typically, L is in the range of 0.1 μm to 5 μm , and W is in the range of 0.2 μm to 100 μm . Finally, note that the MOSFET is a symmetrical device; thus its source and drain can be interchanged with no change in device characteristics.

4.1.2 Operation with No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the pn junction between the n⁺ drain region and the p-type substrate, and the other diode is formed by the pn junction between the p-type substrate and the n⁺ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied, i.e., the path between drain and source has a very high resistance (of the order of 10^4 Ω).

4.1.3 Creating a Channel for Current Flow

Consider now the situation depicted in Fig. 4.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS} . The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "increased" because the mobile holes have been pushed downward into the substrate.

As well, the positive gate voltage attracts electrons from the n⁺ source and drain regions, where they are in abundance, into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, a region is in effect created, connecting the source and drain regions, as indicated in Fig. 4.2. Now, if a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The induced n region thus forms a channel for current flow from drain to source and is appropriately called an *inversion layer*. Correspondingly, the MOSFET of Fig. 4.2 is called an *n-channel MOSFET*, or, alternatively, an *NMOS transistor*. Note that an n-channel MOSFET is formed in a p-type substrate. The channel is created by *inverting* the substrate materials from p-type to n-type. Hence the induced channel is also called an *inversion layer*.

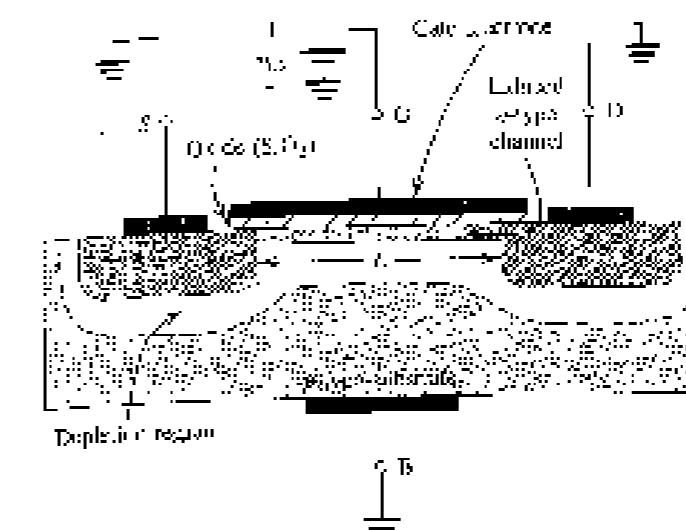


FIGURE 4.2 The n-channel-type NMOS transistor with a positive voltage applied to the gate. A depletion region is at the end of the substrate near the gate.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted V_T . Obviously, V_T for an n-channel FET is positive. The value of V_T is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0 V.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field has developed in the vertical direction. It is this field that carries the amount of charge in the channel, and thus it determines the channel conductivity and, ultimately, the current that will flow through the channel when a voltage v_{DS} is applied.

4.1.4 Applying a Small V_{DS}

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source, as shown in Fig. 4.3. We first consider the case where v_{DS} is small (e.g., 50 mV or so). The voltage v_{DS} causes a current to flow through the induced n channel. Current is carried by free electrons, moving from source to drain (hence the name source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_{DS} , will be from drain to source, as indicated in Fig. 4.3. The magnitude of i_{DS} depends on the density of electrons in the channel, which, in turn, depends on the magnitude of v_{GS} . Specifically, for $v_{GS} = V_T$, the channel is just induced and the current conducted is still negligibly small. As v_{GS} exceeds V_T , more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a decrease in resistance, or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the excess gate voltage ($v_{GS} - V_T$). Then

^a Some texts use V_T to denote the threshold voltage. We use V_T to avoid confusion w/ the junction voltage V_J .

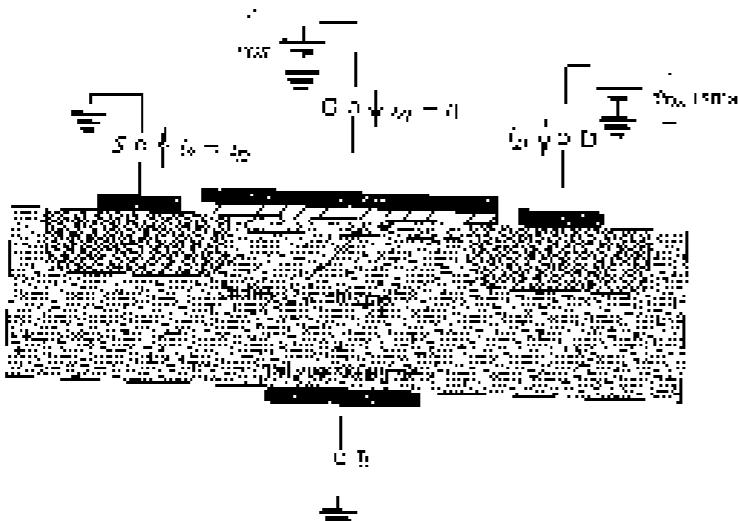


FIGURE 4.3 An NMOS transistor with $V_{DS} > V_g$ and with $V_{GS} = 0$ applied. The drain-to-source resistance is determined by V_{DS} . Specifically, the channel conductance is proportional to $V_{DS} - V_g$, and thus i_D is proportional to V_{DS} ($\propto V_{DS}$). Note that the depletion region is not shown (the short circuit).

known as the effective voltage or the overdrive voltage. It follows that the current i_D will be proportional to $(V_{GS} - V_g)$ and, of course, to the voltage V_{DS} (but rather V_g to V_{DS}).

Figure 4.4 shows a sketch of i_D versus V_{DS} for various values of V_{GS} . We observe that the MOSFET is operating as a linear resistance whose value is controlled by V_{GS} . The resistance is infinite for $V_{GS} \leq V_g$ and its value decreases as V_{GS} exceeds V_g .

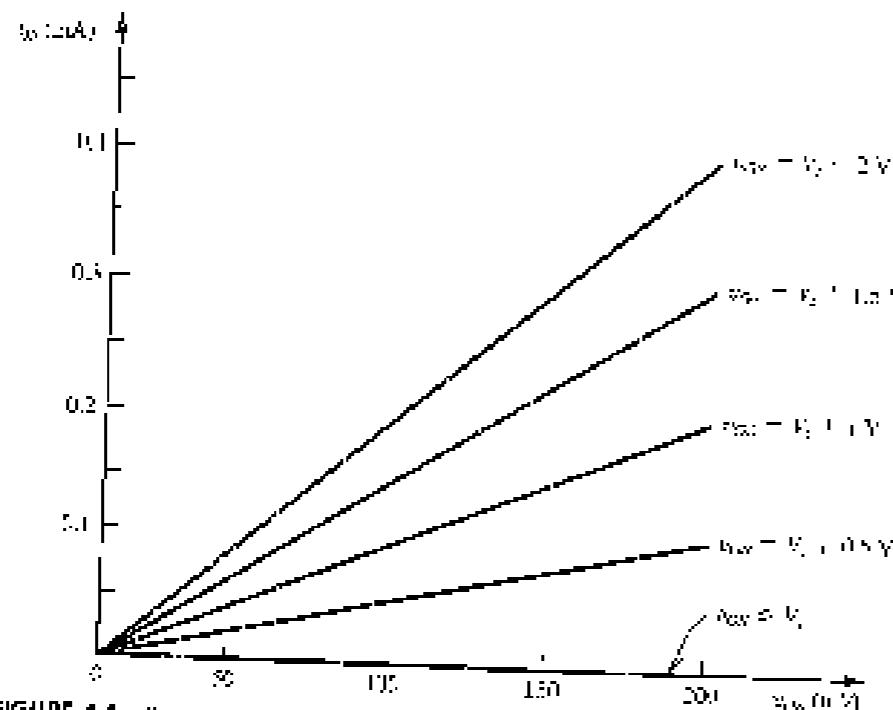


FIGURE 4.4 The i_D - V_{DS} characteristics of the MOSFET in Fig. 4.2 when the voltage V_{GS} between gate and source V_{GS} is kept small. The device operates as a linear resistance whose value is controlled by V_{GS} .

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing V_{GS} above the threshold voltage V_g enhances the channel hence the source-enhancement-mode operation and enhancement-type MOSFET. Finally, we note that the current that leaves the source terminal (i_D) is equal to the current that enters the drain terminal (i_D), and the gate current ($i_G = 0$).

EXERCISE

- 4.1 Given the circuit diagram of the NMOS device in Fig. 4.3, find the drain-to-source voltage V_{DS} when the drain current i_D is 1 mA. Assume the drain-to-source resistance is constant at 10Ω .
- 4.2 Given the circuit diagram of the NMOS device in Fig. 4.3, draw the output characteristic curve under the condition that $V_{GS} = 0.5$ V.
- 4.3 Given the circuit diagram of the NMOS device in Fig. 4.3, draw the output characteristic curve under the condition that $V_{GS} = 1$ V.

4.1.5 Operation as V_{GS} Is Increased

We next consider the situation as V_{GS} is increased. For this purpose let V_{GS} be held constant at a value greater than V_g . Refer to Fig. 4.5, and note that V_{GS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to V_{GS} . Thus the voltage between the gate and points along the channel decreases from V_{GS} at the source end to $V_g = V_{GS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth, neither the channel will take the tapered form shown in Fig. 4.3, being deepest at the source end and shallower at the drain end. As V_{GS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the i_D - V_{DS} curve does not continue as a straight line but bends as shown in Fig. 4.6. Eventually, when V_{GS} is increased to the value that reduces the voltage between gate and

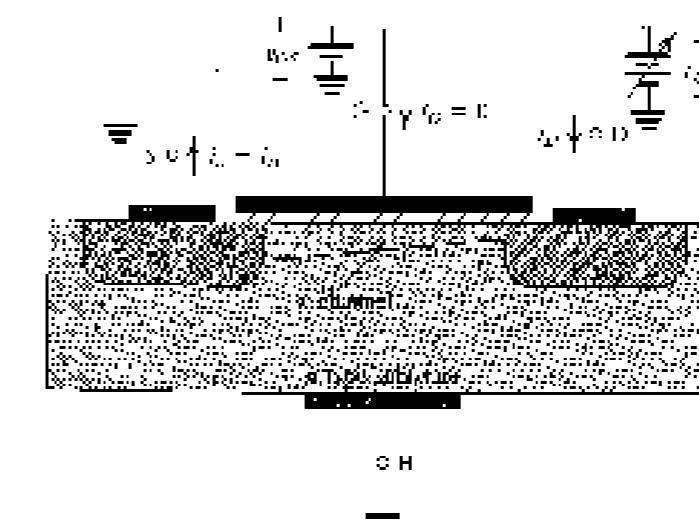


FIGURE 4.5 Operation of the enhancement NMOS transistor as V_{GS} is increased. The induced channel窮enes a tapered shape, and its resistance increases as V_{GS} is increased. Here, V_g is held constant at 0.5 V.

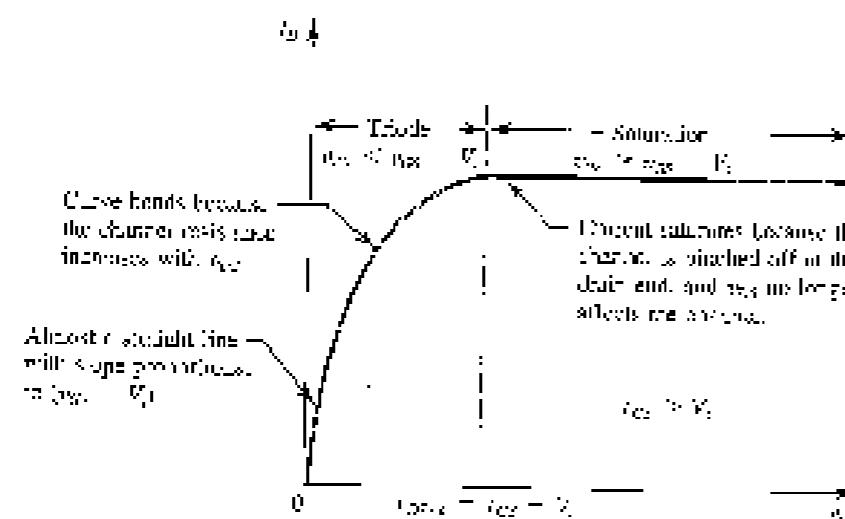


FIGURE 4.6 The drain current I_D versus the drain-to-source voltage V_{DS} for an enhancement-type NMOS transistor operating in the $V_{DS} > V_T$ region.

changed at the drain end to V_T , that is, $v_{DS} = V_D - v_{DS} = V_D - V_T$; or $v_{DS} = v_{DS} - V_T$. The drain end depth at the drain end decreases to almost zero, and the channel is said to be pinched off. Increasing v_{DS} beyond this value has little effect. Theoretically, no effect on the channel slope, and the current through the channel remains constant at the value reached for $v_{DS} = V_T$. The drain current thus saturates at this value, and the MOSFET is said to have entered the saturation region of operation. The voltage v_{DS} at which saturation occurs is denoted $v_{DS(on)}$.

$$v_{DS(on)} = v_{DS} - V_T \quad (4.1)$$

Obviously, for every value of $v_{DS} > V_T$, there is a corresponding value of $v_{DS(on)}$. The device operates in the saturation region $|I_D| > |I_{DS(on)}|$. The region of the I_D-v_{DS} characteristic obtained for $v_{DS} < v_{DS(on)}$ is called the triode region, a carryover from the days of vacuum-tube devices whose operation is FET resembles.

To help further in visualizing the effect of v_{DS} , we show in Fig. 4.7 sketches of the channel as v_{DS} is increased while v_{GS} is kept constant. Theoretically, any increase in v_{DS} above

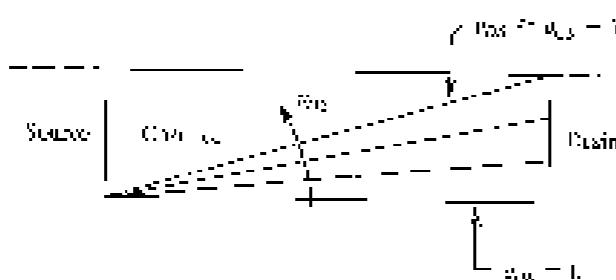


FIGURE 4.7 An increase in v_{DS} causes the channel to require a tapered shape. Eventually, as v_{DS} reaches V_T , the channel is pinched off at the drain end. In practice, $v_{DS} > V_T$ and $v_{DS} = V_T$ has little effect on the drain current.

v_{DS} , which is equal to $v_{DS} - V_T$, has no effect on the channel shape and simply appears across the depletion region surrounding the channel and the drain region.

4.1.6 Derivation of the I_D-v_{DS} Relationship

The description of physical operation presented above can be used to derive an expression for the relationship depicted in Fig. 4.6. Toward that end, assume that a voltage v_{GS} is applied between gate and source with $v_{GS} > V_T$ to induce a channel. Also, assume that a voltage v_{DS} is applied between drain and source. Thus, we shall consider operation in the triode region, for which the channel must be conductive and v_{DS} must be greater than V_T ; equivalently, $v_{DS} > v_{DS} - V_T$. In this case the channel will have the tapered shape shown in Fig. 4.8.

The reader will recall that in the MOSFET the gate and the channel region form a parallel plate capacitor for which the oxide layer serves as a dielectric. If the capacitance per unit area is denoted C_ox and the thickness of the oxide layer is t_{ox} , then

$$C_{ox} = \frac{C_ox}{t_{ox}} \quad (4.2)$$

where ϵ_{ox} is the permittivity of the silicon oxide,

$$\epsilon_{ox} = 3.0 \epsilon_0 = 3.0 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

The oxide thickness t_{ox} is determined by the process technology used to fabricate the MOSFET. As an example, for $t_{ox} = 10 \text{ nm}$, $C_{ox} = 2.45 \times 10^{-3} \text{ F/m}^2$, or $3.45 \text{ fF}/\mu\text{m}^2$ as it is usually expressed.

Now refer to Fig. 4.8 and consider the infinitesimal strip of the gate of distance x from the source. The capacitance of this strip is $C_x \text{ F/m}$. To find the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the effective voltage

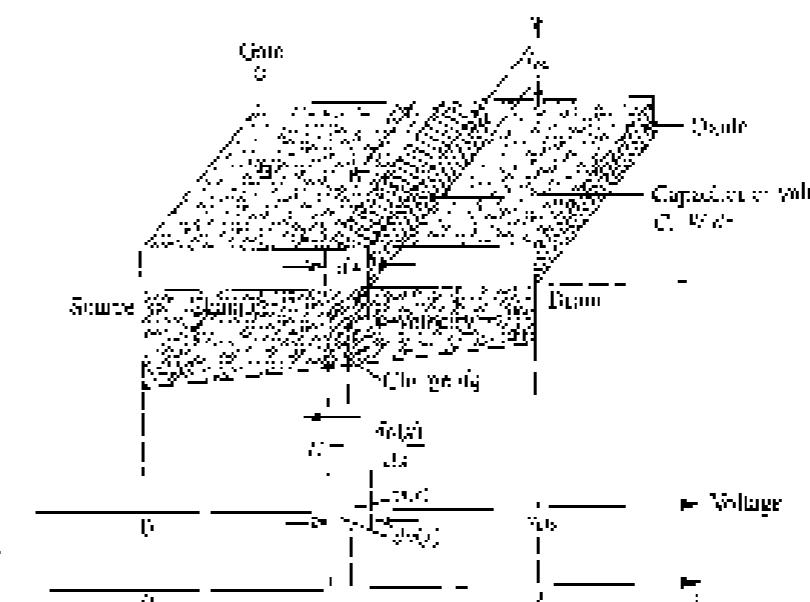


FIGURE 4.8 Derivation of the I_D-v_{DS} characteristic of the NMOS transistor.

between the gate and the channel at point x , where the effective voltage $v(x)$ is the voltage due to the induced gate voltage and is thus $[v_{GS} - v(x) - V_0]$ where v_{GS} is the voltage on the channel at point 0. It follows that the electron charge dv in the infinitesimal portion of the channel at position x

$$dv = -C_{ox} W dx [v_{GS} - v(x) - V_0] \quad (4.3)$$

where the leading negative sign accounts for the fact that dv is a negative charge.

The voltage $v(x)$ produces an electric field along the channel in the negative x direction. At position x this field can be expressed as

$$E(x) = -\frac{dv(x)}{dx}$$

The electric field $E(x)$ causes the electron charge dv to drift toward the drain with a velocity $v_s(x)dv$.

$$\frac{dv}{dt} = -\mu_e E(x) = \mu_e \frac{dv(x)}{dx} \quad (4.4)$$

where μ_e is the mobility of electrons in the channel (channel carrier mobility). It is a physical parameter whose value depends on the fabrication process technology. The resulting drift current i can be obtained as follows:

$$\begin{aligned} i &= \frac{di}{dt} \\ &= \frac{d(i dv)}{dx} \\ &= \frac{d^2i}{dx^2} \end{aligned}$$

Substituting for the charge per-unit-length dv/dx from Eq. (4.3), and for the electron drift velocity d^2i/dx^2 from Eq. (4.4), results in

$$i = -\mu_e C_{ox} W [v_{GS} - v(x) - V_0] \frac{d^2i}{dx^2}$$

Although evaluated at a particular point in the channel, the current i must be constant of all points along the channel. This i must be equal to the source-to-drain current. Since we are interested in the drain-to-source current i_D , we can find it as

$$i_D = i = \mu_e C_{ox} W [v_{GS} - v(x) - V_0] \frac{d^2i}{dx^2}$$

which can be rearranged in the form

$$i_D dx = \mu_e C_{ox} W [v_{GS} - V_0 - v(x)] dv(x)$$

Integrating both sides of this equation from $x = 0$ to $x = L$ and, correspondingly, for $v(x) = 0$ to $v(L) = v_{DS}$ gives

$$i_D = \left(\mu_e C_{ox} \right)^2 \frac{W}{L} \left[(v_{GS} - V_0) v_{DS} + \frac{1}{2} v_{DS}^2 \right] \quad (4.5)$$

This is the expression for the i_D - v_{DS} characteristic in the triode region. The value of the current at the edge of the triode region, or equivalently, at the beginning of the saturation region can be obtained by substituting $v_{DS} = V_0$ resulting in

$$i_D = \frac{1}{2} (\mu_e C_{ox})^2 \frac{W}{L} (v_{GS} - V_0)^2 \quad (4.6)$$

This is the expression for the i_D - v_{GS} characteristic in the saturation region; it simply gives the saturation value of i_D corresponding to the given v_{GS} . Recall that in saturation i_D remains constant for a given v_{GS} as v_{DS} is varied.

In the expressions in Eqs. (4.5) and (4.6), $\mu_e C_{ox}$ is a constant determined by the process technology used to fabricate the n-channel MOSFET. It is known as the process transconductance parameter. For $L = 1$ we shall see shortly, it determines the value of the MOSFET drain-to-source conductance g_D , and has the dimensions of A/V^2 :

$$g_D = \mu_e C_{ox} \quad (4.7)$$

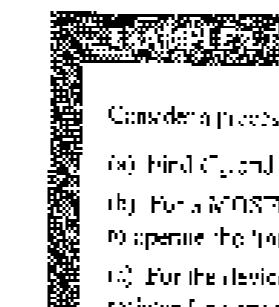
Of course, the i_D - v_{GS} expressions in Eqs. (4.5) and (4.6) can be written in terms of V_0 as follows:

$$i_D = \left(\mu_e \frac{W}{L} \right)^2 (v_{GS} - V_0) v_{DS} - \frac{1}{2} v_{DS}^2 \quad (\text{Triode region}) \quad (4.5a)$$

$$i_D = \frac{1}{2} \left(\mu_e \frac{W}{L} \right)^2 (v_{GS} - V_0)^2 \quad (\text{Saturation region}) \quad (4.6a)$$

In this book we will use the forms with $(\mu_e C_{ox})$ and with V_0 interchangeably.

From Eqs. (4.5) and (4.6) we see that the drain current is proportional to the ratio of the channel width W to the channel length L , known as the aspect ratio a , of the MOSFET. The values of W and L can be selected by the circuit designer to obtain the desired i_D - v_{GS} characteristics. For a given fabrication process, however, there is a minimum channel length, L_{min} . In fact, the minimum channel length L_{min} is possible with a given fabrication process and is being continually reduced as technology advances. For instance, at the time of this writing (2006) the state-of-the-art in MOS technology is a 0.13- μm process, meaning that for this process the minimum channel length possible is 0.13 μm . There also is a minimum value for the channel width W . For instance, for the 0.13- μm process just mentioned, W_{min} is 0.15 μm . Finally, we should note that the oxide thickness t_o scales down with L_{min} . Thus, for a 1.5- μm technology, t_o is 25 nm, but the 0.13- μm technology mentioned above has $t_o = 2$ nm.



Consider a process technology for which $L_{min} = 0.1 \mu\text{m}$, $t_o = 2$ nm, $\mu_e = 50 \text{ cm}^2/\text{V}\cdot\text{s}$, and $V_t = 0.7 \text{ V}$.

- Find C_{ox} and V_0 .
- For a MOSFET with $W/L = 8 \mu\text{m}/0.8 \mu\text{m}$, calculate the values of V_{GS} and V_{DSsat} needed to operate the transistor in the saturation region with a current $i_D = 100 \mu\text{A}$.
- For the device in (b), find the value of V_{GS} required to cause the device to operate at a 1000Ω resistance for very small i_D .

Solution

$$(a) \quad C_{ox} = \frac{V_{GS} - V_{th}}{I_{DS}} \cdot \frac{1.45 \times 10^{-10}}{8 \times 10^4} = 4.32 \times 10^{-10} \text{ F/cm}^2$$

$$= 4.32 \text{ aF}/\mu\text{m}^2$$

$$R_s = \mu_n C_{ox} = 450 \text{ cm}^2/\text{V}\cdot\text{s} \times 4.32 \times 10^{-10} \text{ F/cm}^2$$

$$= 450 \times 10^6 \text{ Ohm/V} \times 4.32 \times 10^{-10} \text{ F/cm}^2$$

$$= 1.94 \times 10^{-3} (\text{MV})$$

$$= 1.94 \mu\text{A/V}^2$$

(b) For operation in the saturation region,

$$I_D = \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_{th})^2$$

Thus,

$$100 = \frac{1}{2} \times 1.94 \times 10^{-3} (V_{GS} - 0.7)^2$$

which results in

$$V_{GS} = 0.7 \pm 0.32 \text{ V}$$

or

$$V_{GS} = 1.02 \text{ V}$$

and

$$V_{DSat} = V_{GS} - V_t = 0.32 \text{ V}$$

(c) For the NMOSFET in the triode region with v_{ds} very small,

$$I_D = \mu_n \frac{W}{L} (V_{GS} - V_t) v_{ds}$$

from which the drain-to-source resistance r_{ds} can be found as

$$r_{ds} = \frac{v_{ds}}{I_D}$$

$$= \frac{1}{\mu_n \frac{W}{L} (V_{GS} - V_t)}$$

Thus

$$1000 = \frac{1}{450 \times 10^6 \times 10 (V_{GS} - 0.7)}$$

which yields

$$V_{GS} - 0.7 = 0.52 \text{ V}$$

Thus

$$V_{GS} = 1.02 \text{ V}$$

EXERCISES

4.2 For a U.S.-style process technology, in which $L = 1.5 \text{ micrometers}$, $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$, $V_{th} = 0.7 \text{ V}$, k_1 and k_2 are $0.2 \text{ m}^2/\text{V}^2$ and $0.1 \text{ m}^2/\text{V}^2$, respectively, find the value of I_D for $V_{GS} = 1.5 \text{ V}$.

4.3 For the NMOSFET in operation in the triode region, assume that an n-channel JFET with $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$ is saturated with a drain-to-source voltage $V_{DS} = 10 \text{ V}$, and that its drain-to-source resistance is 10Ω . If the drain current is $I_D = 100 \text{ mA}$, determine V_{GS} and V_{DS} .

4.4 For the NMOSFET in operation in the triode region, assume that an n-channel JFET with $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$ is saturated with a drain-to-source voltage $V_{DS} = 10 \text{ V}$, and that its drain-to-source resistance is 10Ω . If the drain current is $I_D = 100 \text{ mA}$, determine V_{GS} and V_{DS} .

4.5 For the NMOSFET in operation in the triode region, assume that an n-channel JFET with $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$ is saturated with a drain-to-source voltage $V_{DS} = 10 \text{ V}$, and that its drain-to-source resistance is 10Ω . If the drain current is $I_D = 100 \text{ mA}$, determine V_{GS} and V_{DS} .

4.6 For the NMOSFET in operation in the triode region, assume that an n-channel JFET with $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$ is saturated with a drain-to-source voltage $V_{DS} = 10 \text{ V}$, and that its drain-to-source resistance is 10Ω . If the drain current is $I_D = 100 \text{ mA}$, determine V_{GS} and V_{DS} .

4.7 For the NMOSFET in operation in the triode region, assume that an n-channel JFET with $\mu_n = 350 \text{ cm}^2/\text{V}\cdot\text{s}$ is saturated with a drain-to-source voltage $V_{DS} = 10 \text{ V}$, and that its drain-to-source resistance is 10Ω . If the drain current is $I_D = 100 \text{ mA}$, determine V_{GS} and V_{DS} .

4.1.7 The p-Channel MOSFET

A p-channel enhancement-type MOSFET (PMOS for short), fabricated on an n-type substrate with p-regions for the drain and source, has holes as charge carriers. The device operates in the same manner as the n-channel device except that v_{ds} and v_{gs} are negative and the threshold voltage V_t is negative. Also, the current i_d enters the source terminal and leaves through the drain terminal.

PMOS technology originally dominated MOS technology, however, because NMOS devices can be made smaller and thus operate faster. But because NMOS historically required lower supply voltages than PMOS, NMOS technology has virtually replaced PMOS. Nevertheless, it is important to be familiar with the PMOS transistor for two reasons: PMOS devices are still available for discrete-device design, and more importantly, both PMOS and NMOS transistors are utilized in complementary MOS or CMOS circuits, which is currently the dominant MOS technology.

4.1.8 Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit-device possibilities. Indeed, at the present time CMOS is the most widely used of all the IC technologies. This statement applies to both analog and digital circuits. CMOS technology has virtually replaced integrated circuits based on NMOS transistors alone. Furthermore, at the time of this writing (2003), CMOS technology has taken over many applications that just a few years ago were possible only with bipolar devices. Throughout this book, we will study many CMOS circuit techniques.

Figure 4.3 shows a cross-section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n-region, known as an n-well. The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connection traces to the p-type body and to the n-well. The latter connection serves as the body terminal for the PMOS transistor.

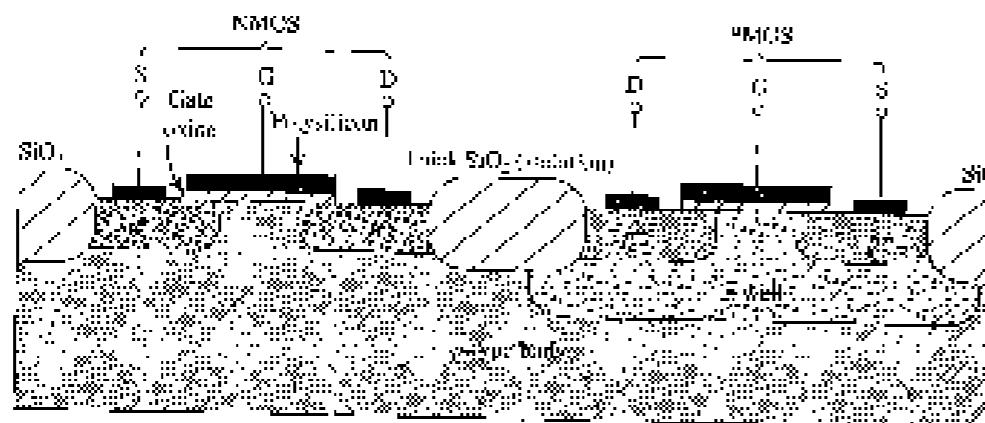


FIGURE 4.9 Cross-section of a CMOS inverter circuit. Note that the NMOS transistor is biased in a depletion-type regime, known as an n-well. Another arrangement is also possible in which a p-type body is used and the device is contained in a p-well. Not shown are the connections made to the p-type body and to the n-well. The letter L refers to the body terminal for the enhanced device.

4.1.8 Operating the MOS Transistor in the Subthreshold Region

The above description of the n-channel MOSFET operation implies that for $V_{GS} < V_t$, no current flows and the device is cut off. This is not entirely true, for it has been found that for values of V_{GS} smaller than but close to V_t , a small drain current flows. In this subthreshold region of operation, the drain current is exponentially related to V_{GS} , much like the $I-V$ relationship of a diode, as will be shown in the next chapter.

Although in most applications the MOS transistor is operated with $V_{GS} > V_t$, there are special, but a growing number of, applications that make use of subthreshold operation. In this book, we will not consider subthreshold operation any further and refer the reader to the references listed in Appendix E.

4.2 CURRENT-VOLTAGE CHARACTERISTICS

Building on the physical foundation established in the previous section for the operation of the enhancement-mode MOS transistor, we present in this section its complete current-voltage characteristics. These characteristics can be measured at dc or at low frequencies and thus are called static characteristics. The dynamic effects that limit the operation of the MOSFET at high frequencies and high switching speeds will be discussed in Section 4.8.

4.2.1 Circuit Symbol

Figure 4.10(a) shows the circuit symbol for the n-channel enhancement-type MOSFET. Observe that the spacing between the two vertical lines that represent the gate and the channel indicates the fact that the gate electrode is insulated from the body of the device. The polarity of the p-type substrate (body) and the n channel is indicated by the arrowhead on the line representing the body (B). This arrowhead also indicates the polarity of the transistor, namely, that it is an n-channel device.

Although the MOSFET is a symmetrical device, it is often useful in circuit design to designate one terminal as the source and the other as the drain (without having to write S and D beside the terminals). This objective is achieved in the modified circuit symbol shown in Fig. 4.10(b). Here an arrowhead is placed on the source terminal, thus distinguishing it from

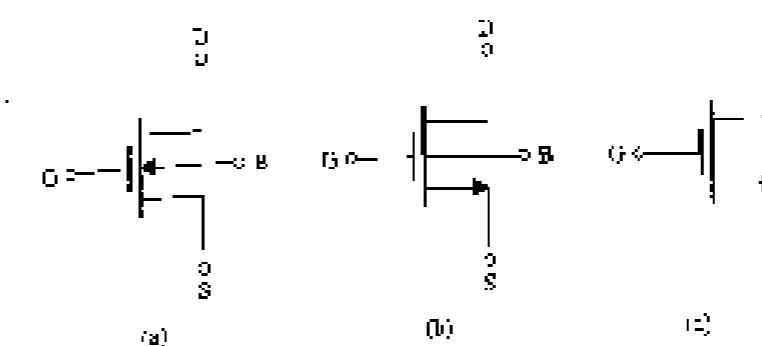


FIGURE 4.10 (a) Circuit symbol for the n-channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain, and a double dot to indicate device polarity (i.e., n channel). (c) Simplified symbol to be used when the source is connected to the body terminal when the effect of the body on circuit operation is unimportant.

the drain terminal. The arrowhead points in the normal direction of current flow and thus indicates the polarity of the device (i.e., n channel). Observe that in the modified symbol, there is no need to show the arrowhead on the body line. Although the circuit symbol of Fig. 4.10(b) clearly distinguishes the source from the drain, in practice it is the polarity of the voltage impressed across the device that determines source and drain; the drain is always positive relative to the source in an n-channel FET.

In applications where the source is connected to the body of the device, a further simplification of the circuit symbol is possible, as indicated in Fig. 4.10(c). This symbol is also used in applications where the effect of the body on circuit operation is not important, as will be seen later.

4.2.2 The i_D-V_{DS} Characteristics

Figure 4.11(a) shows an n-channel enhancement-type MOSFET with voltages V_{GS} and V_{DS} applied and with the normal directions of current flow indicated. This conceptual circuit can be used to measure the i_D-V_{DS} characteristics, which are a family of curves, each measured at a constant V_{GS} . From the study of physical operation in the previous section, we expect each of the i_D-V_{DS} curves to have the shape shown in Fig. 4.6. This is indeed the case, as is evident from Fig. 4.11(b), which shows a typical set of i_D-V_{DS} characteristics. A thorough understanding of the MOSFET terminal characteristics is essential for the reader who intends to design MOS circuits.

The characteristic curves in Fig. 4.11(a) indicate that there are three distinct regions of operation: the cutoff region, the triode region, and the saturation region. The saturation region is used if the FET is to operate as an amplifier. For operation as a switch, the cutoff and triode regions are utilized. The device is cut off when $V_{GS} < V_t$. To operate the MOSFET in the triode region we must first induce a channel:

$$V_{GS} \geq V_t \quad (\text{Induced channel}) \quad (4.8)$$

and then keep V_{GS} small enough so that the channel remains conductive. This is achieved by ensuring that the gate-to-drain voltage is

$$V_{GD} > V_i \quad (\text{Continuous channel}) \quad (4.9)$$

This condition can be stated explicitly in terms of V_{GS} by writing $V_{GS} = V_{GS} - V_{GD} = V_{GS} - V_i$. Therefore,

$$V_{GS} = V_{GS} - V_i > V_t$$

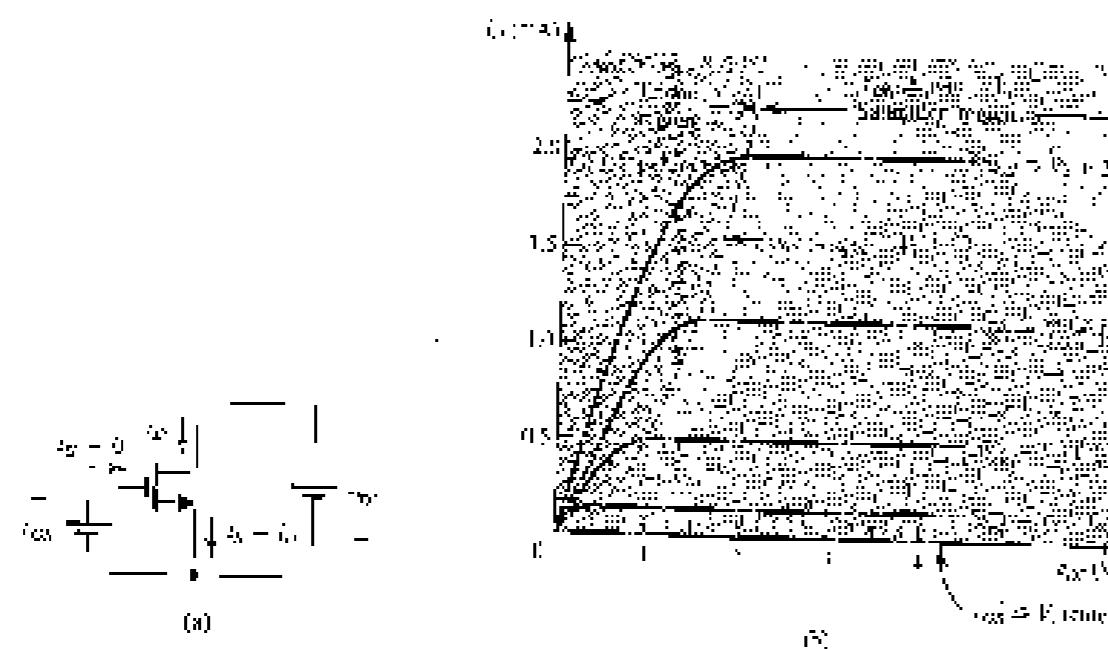


FIGURE 4.11 (a) A circuit diagram showing a MOSFET with V_{GS} and V_{DS} applied and with the current direction shown, as indicated. (b) The I_D - V_{DS} characteristics for a device with $K'_n (W/L) = 1.0 \text{ mA/V}^2$.

which can be rearranged to yield

$$V_{GS} \leq V_{DS} + V_t \quad (\text{Conduction channel}) \quad (4.10)$$

Either Eq. (4.9) or Eq. (4.10) can be used to ascertain triode-region operation. In words, the n-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t and the drain voltage is lower than the gate voltage by at least V_{DS} .

In the triode region, the I_D - V_{DS} characteristics can be described by the relationship of Eq. (4.5), which we repeat here:

$$I_D = K'_n \frac{W}{L} (V_{GS} - V_t) v_{DS} - \frac{1}{2} \frac{W}{L} C_{ox} v_{DS}^2 \quad (4.11)$$

where $K'_n = \mu_n C_{ox}$ is the process transconductance parameter; its value is determined by the fabrication technology. If v_{DS} is sufficiently small so that we can neglect the $\frac{1}{2} \frac{W}{L} C_{ox} v_{DS}^2$ term in Eq. (4.11), we obtain for the I_D - v_{DS} characteristics near the origin the relationship

$$I_D = K'_n \frac{W}{L} (V_{GS} - V_t) v_{DS} \quad (4.12)$$

This linear relationship represents the operation of the MOSFET transistor as a linear resistance r_{ds} whose value is controlled by v_{GS} . Specifically, for v_{GS} set to a value $V_{GS, \text{sat}}$ is given by

$$v_{GS, \text{sat}} = \left. \frac{V_{GS}}{I_D} \right|_{\text{saturation}} = \left[K'_n \frac{W}{L} (V_{GS} - V_t) \right]^{-1} \quad (4.13)$$

We discussed this region of operation in the previous section (refer to Fig. 4.4). It is also useful to express r_{ds} in terms of the gate-to-source overdrive voltage,

$$V_{OV} = V_{GS} - V_t \quad (4.14)$$

$$I_D = \frac{1}{2} K'_n \frac{W}{L} v_{DS}^2 \quad (4.15)$$

Finally, we urge the reader to show that the approximation involved in writing Eq. (4.12) is based on the assumption that $v_{DS} \ll V_{DS}$.

To operate the MOSFET in the saturation region, a condition must be imposed,

$$v_{DS} \geq V_t \quad (\text{Saturation channel}) \quad (4.16)$$

and pinched off at the drain end by raising v_{DS} to a value that results in the gate-to-drain voltage falling below V_t ,

$$v_{DS} \leq V_t \quad (\text{Pinched-off channel}) \quad (4.17)$$

This condition can be expressed explicitly in terms of v_{GS} as

$$v_{GS} \geq v_{DS} - V_t \quad (\text{Pinched-off channel}) \quad (4.18)$$

In words, the enhanced-voltage-type MOSFET operates in the saturation region when v_{GS} is greater than V_t and the drain voltage does not fall below the pinched-off voltage by more than V_t .

The boundary between the triode region and the saturation region is characterized by

$$v_{GS} = v_{DS} - V_t \quad (\text{Boundary}) \quad (4.19)$$

Substituting this value of v_{GS} into Eq. (4.11) gives the saturation value of the current as

$$I_D = \frac{1}{2} K'_n \frac{W}{L} (V_{DS} - V_t)^2 \quad (4.20)$$

Thus, in saturation the MOSFET provides a drain current whose value is independent of the drain voltage v_{DS} , and is determined by the gate voltage v_{GS} according to the square-law relationship in Eq. (4.20), a sketch of which is given in Fig. 4.12. Since the drain current is independent of the drain voltage, the saturated MOSFET behaves as an ideal current source whose value is controlled by v_{GS} according to the nonlinear relationship in Eq. (4.20). Figure 4.13 shows a circuit representation of this view of MOSFET operation in the saturation region. Note that this is a large-signal equivalent-circuit model.

Referring back to the I_D - v_{DS} characteristics in Fig. 4.11(b), we note that the boundary between the triode and the saturation regions is shown as a broken-line curve. Since this curve is characterized by $v_{GS} = v_{DS} - V_t$, its equation can be found by substituting for $v_{GS} = V_t$ by v_{DS} in either the triode-region equation (Eq. 4.11) or the saturation-region equation (Eq. 4.20). The result is

$$v_{DS} = \frac{1}{2} K'_n \frac{W}{L} v_{GS}^2 \quad (4.21)$$

It should be noted that the characteristics depicted in Figs. 4.1, 4.11, and 4.12 are for a MOSFET with $K'_n (W/L) = 1.0 \text{ mA/V}^2$ and $V_t = 1 \text{ V}$.

Finally, the chart in Fig. 4.11 shows the relative levels of the terminal voltages of the enhancement-type NMOS transistor for operation both in the triode region and the saturation region.

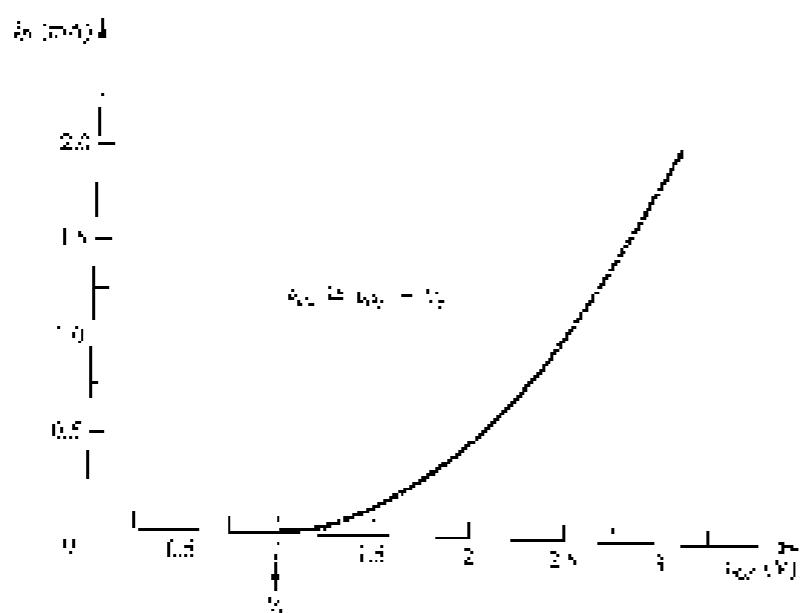


FIGURE 4.12 Transfer characteristic of a n-channel type NMOS transistor operating in the saturation region ($V_G = 1$ V).

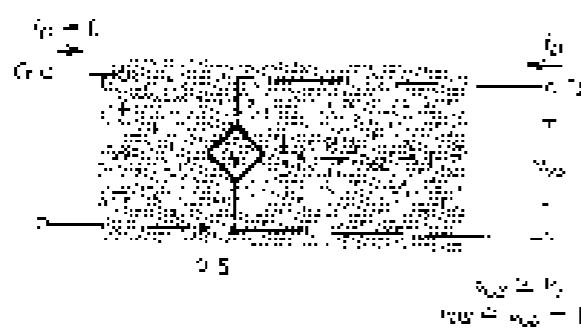


FIGURE 4.13 Large-signal equivalent circuit model of an n-channel MOSFET operating in the saturation region.

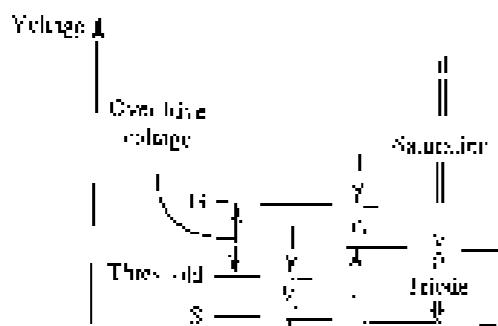


FIGURE 4.14 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

- PROBLEMS**
- 4.1 An enhancement-type NMOS transistor with $L = 1 \mu\text{m}$ is said to exhibit pinchoff with $V_{DS} \approx 0.5$ V at $V_G = 0$ V. If the drain current is $I_D = 10^{-12}$ A at $V_G = 0$ V, find the drain-to-source voltage at which the drain current is $I_D = 10^{-11}$ A.
 - 4.2 If the n-MOS device in Exercise 4.1 has $L = 1 \mu\text{m}$, $V = 10$ cm, and $\lambda = 1$ cm, find the value of drain current for which the drain-to-source voltage is 10^{-11} A. (Hint: Use Eq. (4.4) and Eq. (4.13).)
 - 4.3 Calculate drain-to-source voltage for which drain current is 10^{-12} A when $V_G = 0$ V. The drain-to-gate voltage is -1.5 V and $V = 10$ cm. Also, $\lambda = 1$ cm, the width of the drain is $10 \mu\text{m}$, and the resistance r_d for small signals is 50Ω . (Hint: Use Eq. (4.13) and Eq. (4.17).)
 - 4.4 A p-channel enhancement-type NMOS transistor has $L = 1 \mu\text{m}$, $V = 10$ cm, and $\lambda = 1$ cm. The drain current is $I_D = 10^{-12}$ A at $V_G = 0$ V. Find the drain-to-source voltage at which the drain current is $I_D = 10^{-11}$ A. (Hint: Use Eq. (4.4) and Eq. (4.13).)
 - 4.5 An enhancement-type NMOS transistor with $L = 1 \mu\text{m}$ is said to exhibit pinchoff with $V_{DS} \approx 0.5$ V at $V_G = 0$ V. If the drain current is $I_D = 10^{-12}$ A at $V_G = 0$ V, find the drain-to-source voltage at which the drain current is $I_D = 10^{-11}$ A. (Hint: Use Eq. (4.4) and Eq. (4.13).)

4.2.2 Drain Output Resistance in Saturation

Equation (4.12) and the corresponding large-signal equivalent circuit in Fig. 4.13 indicate that, in saturation, v_d is independent of v_{ds} . Thus a change Δv_{ds} in the drain-to-source voltage causes a zero change in v_d , which implies that the incremental resistance looking into the drain of a saturated MOSFET is infinite. This, however, is an idealization based on the premise that once the channel is pinched off at the drain end, further increases in v_{ds} have no effect on the channel's shape. But, in practice, increasing v_{ds} beyond v_{dsat} does affect the channel somewhat. Specifically, as v_{ds} is increased, the channel pinch-off point is moved slightly away from the drain toward the source. This is illustrated in Fig. 4.15, from which we note that the voltage across the channel remains constant at $v_{ds} = V_s - v_{sg}$, and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. Note, however, that (with depletion-layer widening) the channel length is in effect reduced, from L to $L - \Delta L$, a phenomenon known as channel-length modulation. Now, since v_d is inversely proportional to the channel length (Eq. 4.20), v_d increases with v_{ds} .

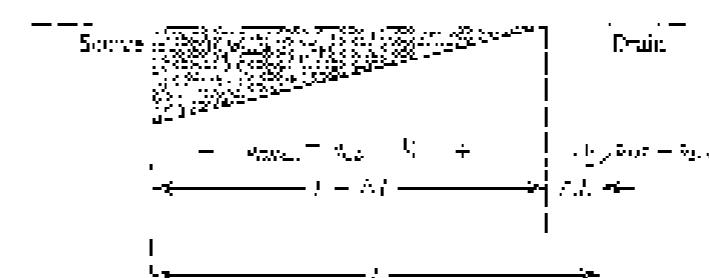


FIGURE 4.15 Increasing v_{ds} beyond v_{dsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the drain-to-gate channel length by ΔL .

To account for the dependence of k_0 on V_{DS} in saturation, we replace I_D in Eq. (4.20) with $I_D + \Delta I_D$ to obtain

$$\begin{aligned} i_D &= \frac{1}{2} k_0 \frac{W}{L} (V_{DS} - V_T)^2 \\ &= \frac{1}{2} k_0' \frac{W}{L} (1 + (\Delta I_D/I_D)) (V_{DS} - V_T)^2 \\ &\approx \frac{1}{2} k_0' \frac{W}{L} \left(1 + \frac{\Delta I_D}{I_D}\right) (V_{DS} - V_T)^2 \end{aligned}$$

where we have assumed that $(\Delta I_D/I_D) \ll 1$. Now, if we assume that ΔI_D is proportional to V_{DS} ,

$$\Delta I_D = \lambda V_{DS}$$

where λ' is a process technology parameter with the dimensions of $\mu\text{A}/\text{V}$, we obtain for i_D

$$i_D = \frac{1}{2} k_0' \frac{W}{L} \left(1 + \frac{\lambda'}{I_D} V_{DS}\right) (V_{DS} - V_T)^2$$

Usually, λ'/L is denoted λ .

$$\lambda = \frac{\lambda'}{L}$$

It follows that λ is a process-technology parameter with the dimensions of V^{-1} and that, for a given process, λ is inversely proportional to the length selected for the channel. In terms of λ , the expression for i_D becomes

$$i_D = \frac{1}{2} k_0' \frac{W}{L} (V_{DS} - V_T)^2 (1 + \lambda V_{DS}) \quad (4.22)$$

A typical set of i_D - v_{DS} characteristics showing the effect of channel-length modulation is displayed in Fig. 4.16. The observed linear dependence of i_D on v_{DS} in the saturation region is represented in Eq. (4.22) by the term $(1 + \lambda V_{DS})$. From Fig. 4.16 we observe that when the straight-line i_D - v_{DS} characteristics are extrapolated they intersect the v_{DS} -axis at the point $v_{DS} = V_T$, where V_T is a threshold voltage. Equation (4.22), however, indicates that $i_D = 0$

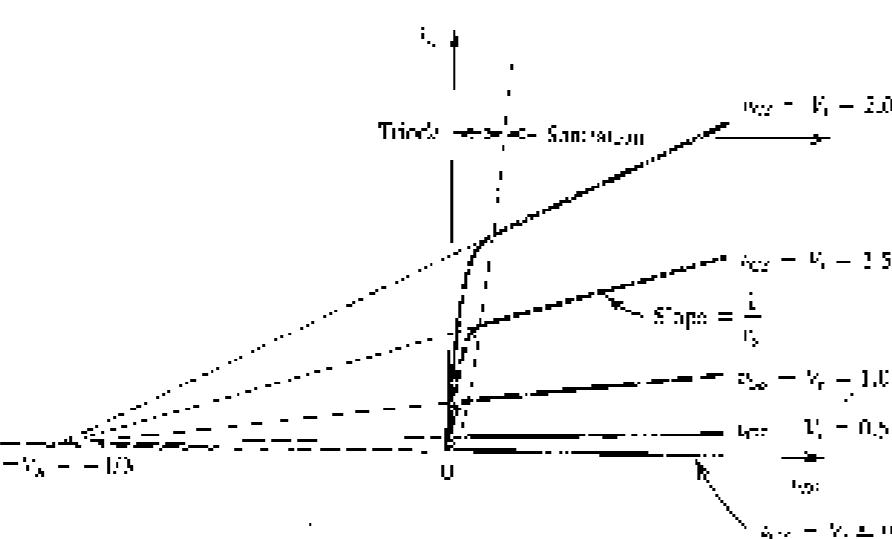


FIGURE 4.16 Effect of v_{DG} on i_D in the saturation region. The MOSFET parameter k_0 depends on the process technology and, for a given process, is proportional to the channel length L .

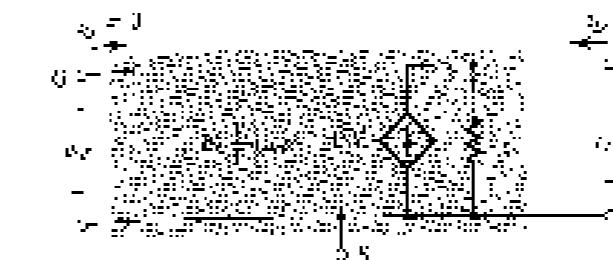


FIGURE 4.17 Transistor equivalent circuit model of the enhanced NMOSFET in saturation, incorporating the output resistance r_D . The output resistance model, or the dependence of r_D on i_D , will be given by Eq. (4.23).

at $v_{DS} = -V_T$. It follows that

$$V_T = \frac{1}{\lambda}$$

and thus V_T is a process-technology parameter with the dimensions of V . For a given process, V_T is proportional to the channel length L , but the designer selects for a MOSFET. Just as in the case of λ , we can isolate the dependence of V_T on L by expressing it as

$$V_T = V'_T L$$

where V'_T is a purely process-technology dependent with the dimensions of $\text{V}/\mu\text{m}$. Typically, V'_T falls in the range of 5 $\text{V}/\mu\text{m}$ to 50 $\text{V}/\mu\text{m}$. The voltage V_T is usually referred to as the Early voltage, after J.M. Early, who discovered a similar phenomenon for the BJT (Chapter 5).

Equation (4.22) indicates that when channel-length modulation is taken into account, the saturation values of i_D depend on v_{DS} ; thus, for a given v_{DS} , a change Δi_D in the drain current i_D follows from the output resistance of the current source representing i_D in saturation is no longer infinite. Defining the output resistance r_D as

$$r_D = \frac{1}{\frac{\partial i_D}{\partial v_{DS}}}_{i_D = \text{constant}} \quad (4.23)$$

and using Eq. (4.22) results in

$$r_D = \frac{k_0' W}{2} \left[\frac{V_{DS} - V_T}{L} \right]^2 \quad (4.24)$$

which can be written as

$$r_D = \frac{1}{\lambda I_D} \quad (4.25)$$

or, equivalently,

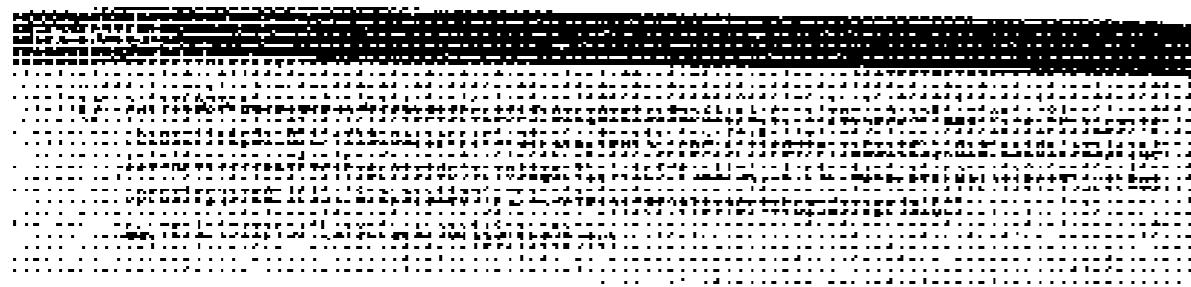
$$r_D = \frac{V_T}{I_D} \quad (4.26)$$

where I_D is the drain current without channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_0' \frac{W}{L} (V_{DS} - V_T)^2$$

Thus the output resistance is a inversely proportional to the drain current. Finally, we show in Fig. 4.17 the large-signal equivalent circuit model incorporating r_D .

² In this book we use r_o to denote the output resistance in saturation, and r_{DS} to denote the drain-to-source resistance in the triode regime. In a small-signal

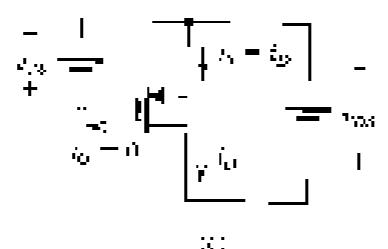
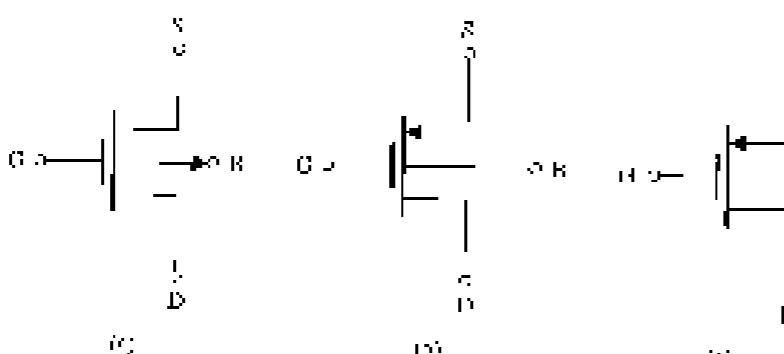


4.2.4 Characteristics of the p-Channel MOSFET

The circuit symbol for the p-channel enhancement-type MOSFET is shown in Fig. 4.18(a). Figure 4.18(b) shows a modified circuit symbol in which an arrowhead pointing *out* on the source terminal. For the case where the source is connected to the substrate, the simplified symbol of Fig. 4.18(c) is usually used. The voltage and current polarities for normal operation are indicated in Fig. 4.18(d). Recall that for the p-channel device the drain bias voltage, V_D , is negative. To induce a channel we apply a gate voltage that is more negative than V_A .

$$V_{GS} < V_A \quad (\text{Induced channel})$$

4.2.4



4.18(c)

FIGURE 4.18 (a) Circuit symbol for the p-channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead. (c) Simplified circuit symbol for the case where the source is connected to the body. (d) The MOSFET with voltage applied and the direction of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

or equivalently,

$$v_{GS} > |V_A|$$

and applying a drain voltage that is more negative than the source voltage (i.e., v_{DS} is negative or equivalently, v_{DS} is positive). The current i_D flows out of the drain terminal, as indicated in the figure. To operate in the triode region, v_{DS} must satisfy

$$v_{DS} > v_{DSs} - V_A \quad (\text{Triode region}) \quad (4.28)$$

that is, the drain voltage must be higher than the gate voltage by at least $|V_A|$. The current i_D is given by the same equation as for NMOS, Eq. (4.14), except by replacing k_n with k_p :

$$i_D = \mu_p \frac{W}{L} (v_{GS} - V_A) v_{DS} - \frac{1}{2} k_p v_{DS}^2 \quad (4.29)$$

where v_{GS} , V_A , and v_{DS} are negative and the transconductance parameter k_p is given by

$$k_p = \mu_p C_{ox} \quad (4.30)$$

where μ_p is the mobility of holes in the induced p channel. Typically, $\mu_p = 0.25$ to 0.35, and is process technology dependent.

To operate in saturation, v_{GS} must satisfy the relationship

$$v_{GS} < v_{GSs} - V_A \quad (\text{Pinched-off channel}) \quad (4.31)$$

that is, the drain voltage must be lower than gate voltage + $|V_A|$. The current i_D is given by the same equation used in NMOS, Eq. (4.22), again with k_n replaced with k_p :

$$i_D = \frac{1}{2} k_p \frac{W}{L} (v_{GS} - V_A)^2 (1 + \alpha v_{DS}) \quad (4.32)$$

where v_{GS} , V_A , k_p , and α are all negative. We should note, however, that in evaluating α , using Eqs. (4.24) through (4.26), the magnitudes of k_p and V_A should be used.

To recall, to turn a PMOS transistor on, the gate voltage has to be made lower than that of the source by at least $|V_A|$. To operate in the triode region, the drain voltage has to exceed that of the gate by at least $|V_A|$; otherwise, the PMOS operates in saturation.

Finally, the chart in Fig. 4.19 provides a pictorial representation of these operating conditions.

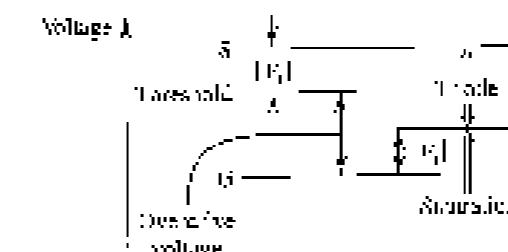


FIGURE 4.19 The plot of levels of the terminal voltages at the enhanced-type PMOS transistor for operation in the triode region and in the saturated region.

EXERCISE

4.1.25. In the circuit shown in Fig. 4.2.10, calculate the drain current I_D assuming the body of the p-channel device has a carrier concentration N_A equal to 10^{16} cm^{-3} . Assume the carrier mobility μ is constant at $0.02 \text{ cm}^2/\text{V}\cdot\text{s}$, and the threshold voltage V_{T0} is -0.75 V . The drain-to-source voltage is $V_D = 0.5 \text{ V}$, and the gate-to-source voltage is $V_G = -0.5 \text{ V}$. If $A = 0.01 \text{ m}^2$, find the drain current corresponding to the operating voltage determined in (b). Hint: For $V_D > 0$, the drain voltage is $V_D - I_D R_D$.

(b) Calculate the value of the applied drain voltage if $I_D = 10^{-10} \text{ A}$. Compare it to the value obtained in (a).

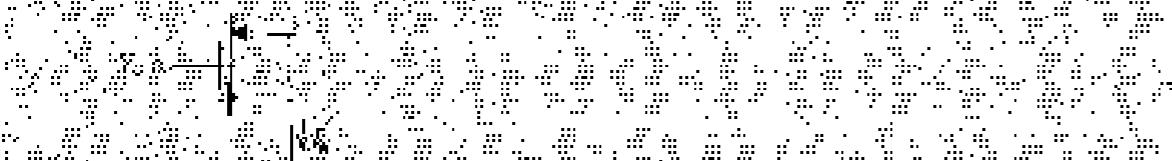


FIGURE E4.1.25.

Ans: (a) $V_D = 0.5 \text{ V}$; (b) $V_D = 0.5 \text{ V} + 10^{-10} \text{ A} \times 10 \Omega = 0.5 \text{ V} + 10^{-9} \text{ V} = 0.51 \text{ V}$
 $I_D = 10^{-10} \text{ A} \times 10 \Omega = 10^{-9} \text{ A}$ (0.01 m², $\mu = 0.02 \text{ cm}^2/\text{V}\cdot\text{s}$)

4.2.5 The Role of the Substrate—The Body Effect

In many applications the source terminal is connected to the substrate (or body) terminal B , which results in the pn junction between the substrate and the induced channel (see Fig. 4.5) having a constant zero (avalanche) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to worsen the on condition for all the substrate-to-drain junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse bias voltage between source and body (V_{SB}) in a n -channel device will have an effect on device operation. To appreciate this fact, consider an NMOS transistor and let the substrate be made negative relative to the source. The reverse bias voltage will widen the depletion region (refer to Fig. 4.2). This in turn reduces the channel depth. To return the channel to its former state, V_{GS} has to be increased.

The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_T . Specifically, it has been shown that increasing the reverse substrate bias voltage V_{SB} results in an increase in V_T , according to the relationship

$$V_T = V_{T0} + \gamma \sqrt{(2\phi_F + V_{SB}) - \sqrt{2\phi_F}} \quad (4.2.2)$$

where V_{T0} is the threshold voltage for $V_{SB} = 0$; γ is a physical parameter with C_V typically 0.6 V^{-1} ; ϕ_F is a fixed-dimensionless parameter given by

$$\phi_F = \frac{\sqrt{2qN_A}C_V}{C_{ox}} \quad (4.2.3)$$

where q is the electron charge ($1.6 \times 10^{-19} \text{ C}$), N_A is the doping concentration of the p-type substrate, and C_V is the permittivity of silicon ($11.7\varepsilon_0 = 11.7 \times 8.854 \times 10^{-12} = 1.04 \times 10^{-12} \text{ F/m}$). The parameter γ has the dimension of $\text{V}^{1/2}$ and is typically $0.4 \text{ V}^{1/2}$. Finally, note that Eq. (4.2.3) applies equally well for p-channel devices with V_{GS} replaced by the reverse bias of the substrate, V_{SB} (or alternatively, replace V_{DS} by $|V_{DS}|$) and note that γ is negative. In evaluating γ , N_A must be replaced with N_D , the doping concentration of the n-well in which the PMOS is located. For p-channel devices, C_V is typically 0.73 V^{-1} , and γ is typically $-0.5 \text{ V}^{1/2}$.

Equation (4.2.3) indicates that an additional change in V_{GS} gives rise to no incremental change in V_T , which in turn results in an incremental change in i_D , even though V_{GS} might have been kept constant. It follows that the body voltage controls i_D ; thus the body acts as another gate for the MOSFET, a phenomenon known as the body effect. Here we note that the parameter γ is known as the body-effect parameter. The body effect can cause considerable degradation in circuit performance, as will be shown in Chapter 8.

EXERCISE

4.1.26. Calculate the drain current I_D for the circuit shown in Fig. 4.2.10, assuming the body of the p-channel device has a carrier concentration $N_A = 10^{16} \text{ cm}^{-3}$ and $V_{T0} = -0.75 \text{ V}$. The drain-to-source voltage is $V_D = 0.5 \text{ V}$, and the gate-to-source voltage is $V_G = -0.5 \text{ V}$. If $A = 0.01 \text{ m}^2$, find the drain current corresponding to the operating voltage determined in (b). Hint: For $V_D > 0$, the drain voltage is $V_D - I_D R_D$.

4.2.6 Temperature Effects

Both V_T and A are temperature sensitive. The magnitude of V_T decreases by about 2 mV for every 1°C rise in temperature. This decrease in $|V_T|$ gives rise to a corresponding increase in drain current as temperature is increased. However, because A decreases with temperature and its effect is dominant, the overall observed effect of a temperature increase is a decrease in drain current. This very interesting result is put to use in applying the MOSFET in power circuits (Chapter 14).

4.2.7 Breakdown and Input Protection

As the voltage on the drain is increased, a value is reached at which the pn junction between the drain region and substrate suffers avalanche breakdown (see Section 3.7.4). This breakdown usually occurs at voltages of 20 V to 100 V and results in a somewhat rapid increase in current, known as a weak avalanche.

Another breakdown effect occurs at lower voltages (about 20 V in modern devices) is called punch-through. It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Punch-through does not result in permanent damage to the device.

Yet another kind of breakdown occurs when the gate-to-source voltage exceeds about 20 V . This is the breakdown of the gate oxide and results in permanent damage to the device. Although 20 V may seem high, it must be remembered that the MOSFET has a very high input resistance, and a very small input capacitance, and thus small amounts of static charge accumulating on the gate capacitor can drive its breakdown voltage to be exceeded.

To prevent the accumulation of static charge on the gate capacitor of a MOSFET, protection diodes are usually included at the input terminals of MOS integrated circuits. The protection mechanism is briefly treated of damping diodes.

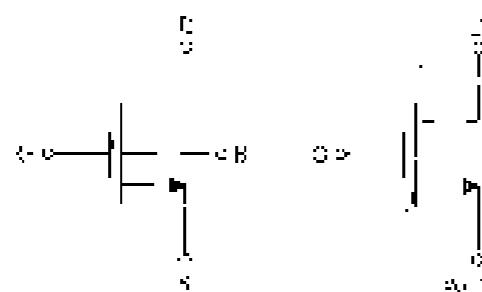
4.2.8 Summary

For easy reference we present in Table 4.1 a summary of the current-voltage relationships for enhancement-type MOSFETs.

TABLE 4.1 Summary of the Current-Voltage Characteristics

NMOS Transistor

Symbols:



Overdrive voltage:

$$v_{GS} = v_G - V_t$$

$$v_{DS} = V_D + v_D$$

Operation in the triode region:

a) Conditions:

$$(1) v_{GS} \geq V_t \Leftrightarrow v_{GS} \geq 0$$

$$(2) v_{DS} \geq V_D \Leftrightarrow v_{DS} \geq v_D - V_D \Leftrightarrow v_{DS} \geq v_D$$

b) Current expression:

$$i_D = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) v_{DS} \left(1 + \frac{v_D}{V_D} \right)$$

$$\text{or } i_D = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) v_{DS}$$

$$i_D = \frac{W}{L} \left[\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) \right] v_{DS}$$

Operation in the saturation region:

a) Conditions:

$$(1) v_{GS} \geq V_t \Leftrightarrow v_{GS} \geq 0$$

$$(2) v_{DS} \leq V_D \Leftrightarrow v_{DS} \leq v_D - V_D \Leftrightarrow v_{DS} \leq v_D$$

b) Current expression:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 (1 + \beta v_{DS})$$

a) Large-signal equivalent circuit model:



$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 \left(1 + \frac{v_D}{V_D} \right) = I_D$$

where

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

Threshold voltage:

$$V_t = V_F + \sqrt{2 \cdot 2 \cdot 10^{-12}} = (V_F + \sqrt{2 \cdot 10^{-12}})$$

Process parameters:

$$C_{ox} = \epsilon / t_{ox} = 10^{-10} \text{ F/m}^2$$

$$k_F = n_s A_{ox} = 10^{12} \text{ m}^{-2}$$

$$V_F = (V_T)^2 / k_F = 10^{-12} \text{ V}^2$$

$$\lambda = (1/k_F) = 10^{-12} \text{ m}^2$$

$$\gamma = \sqrt{2 \cdot 10^{-12}} / C_{ox} = 10^{-12} \text{ V}^{-1/2}$$

Constants:

$$e = 8.85 \times 10^{-12} \text{ F/m}$$

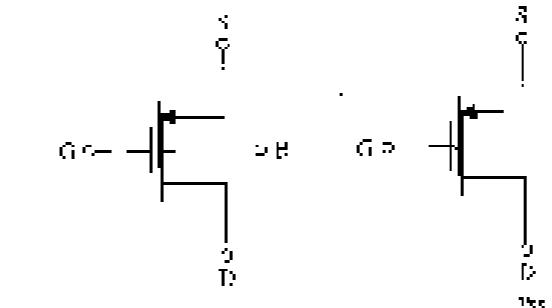
$$n_s = 2.0 \times 10^{15} \times 10^{-12} \text{ cm}^{-2}$$

$$V_T = 1.4 \times 10^{-12} \text{ V}$$

$$\theta = 1.012 \times 10^{-12} \text{ C}$$

PMOS Transistor

Symbols:



Overdrive voltage:

$$v_{GS} = v_G - V_t$$

$$v_{DS} = |V_D + v_D|$$

(continued)

TABLE 4.1 (Continued)

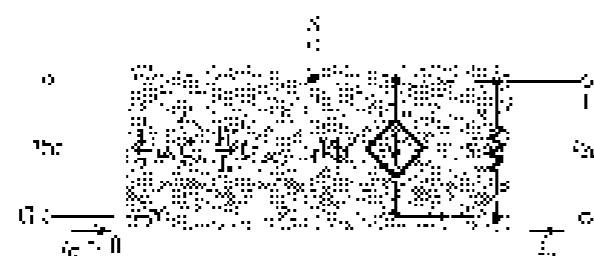
- 4.1 Characteristics:**
- Static relationships as for NMOS transistors except:
- Replace μ_n , N_A , and V_{t0} with μ_p , N_A , and V_{t0} , respectively.
- V_s , V_D , V_G , k , and β are negative.
- Conditions for operation in the triode region:

 - (1) $v_{GS} < V_t \Rightarrow v_{DS} > 0 \Leftrightarrow v_{DS} > |V_s|$
 - (2) $v_{DS} > |V_s| \Rightarrow v_{GS} > v_{DS} - V_t \Rightarrow v_{GS} \leq |v_{DS}|$

- Conditions for operation in the saturation region:

 - (1) $v_{GS} < V_t \Rightarrow v_{DS} \leq 0 \Leftrightarrow v_{DS} \geq |V_s|$
 - (2) $v_{GS} \leq V_t \Rightarrow v_{GS} \leq v_{DS} - V_s \Rightarrow v_{DS} \geq v_{GS} + V_s$

- Large-signal equivalent circuit model:



$$I_D = \left[4 \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \right]^{1/2} = \frac{I_D}{I_D}$$

where

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

4.3 MOSFET CIRCUITS AT DC

Having studied the current-voltage characteristics of MOSFETs, we now consider circuits in which only voltages and currents are of concern. Specifically, we shall present a series of design and analysis examples of MOSFET circuits at dc. The objective is to instill in the reader familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.

In the following examples, to keep matters simple and thus focus attention on the essence of MOSFET circuit operation, we will generally neglect channel-length modulation, that is, we will assume $k = 0$. We will find it convenient to work in terms of the excessdrive voltage $V_{GS} = V_{GS} - V_t$. Recall that for NMOS, V_s and V_{DS} are positive while, for PMOS, V_s and V_{DS} are negative. For PMOS the reader may prefer to write $V_{GS} = V_{GS} - V_{t0} = V_s - |V_{GS}|$.

FIGURE 4.20

Design the circuit in Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistors have $V_t = 0.5$ V, $\mu_p C_{ox} = 100 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $W = 32 \mu\text{m}$. Neglect the channel-length modulation effect (i.e., assume that $k = 0$).

**FIGURE 4.20** Circuit for Example 4.2.

Solution

Since $V_D = 0.5$ V is greater than V_t , this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of I_D to determine the required value of V_{GS} :

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

Substituting $V_{DS} = V_s = V_{GS} - V_t = 0.4$ mA, $I_D = 0.4$ mA, $\mu_p C_{ox} = 100 \mu\text{A/V}^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{GS}^2$$

which results in

$$V_{GS} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_s + V_{GD} = 0.5 + 0.5 = 1.0 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.0 V, and the required value of R_G can be determined from

$$\begin{aligned} R_G &= \frac{V_s - V_{GS}}{I_D} \\ &= \frac{-1.0 - (-0.5)}{0.4} = 1.25 \text{ k}\Omega \end{aligned}$$

To establish a dc voltage of 0.5 V at the drain, we must select R_D as follows:

$$\begin{aligned} R_D &= \frac{V_{DS} - V_D}{I_D} \\ &= \frac{0.5 - 0.5}{0.4} = 5 \text{ k}\Omega \end{aligned}$$

EXERCISE

- 4.10 Redesign the circuit of Fig. 4.20 for the following cases: $V_g = +5\text{ V}$, $V_s = -5\text{ V}$, $V_d = 0\text{ V}$, $k_s^2 = 100\text{ }\mu\text{A/V}^2$, $\lambda = 0.5\text{ mA/V}^2$, $I_{DQ} = 0.5\text{ mA}$, $V_t = -0.1\text{ V}$, $\mu_s C_{ox} = 200\text{ }\mu\text{A/V}^2$, $L = 0.8\text{ }\mu\text{m}$, and $W = 4\text{ }\mu\text{m}$. Neglect the channel-length modulation factor (*i.e.*, assume $\lambda = 0$).

Design the circuit in Fig. 4.21 to obtain a current I_D of $80\text{ }\mu\text{A}$. Find the value required for R , and find the dc voltage V_D . Let the NMOS transistor have $V_t = 0.5\text{ V}$, $\mu_s C_{ox} = 200\text{ }\mu\text{A/V}^2$, $L = 0.8\text{ }\mu\text{m}$, and $W = 4\text{ }\mu\text{m}$. Neglect the channel-length modulation factor (*i.e.*, assume $\lambda = 0$).

$$V_{DD} = -5\text{ V}$$

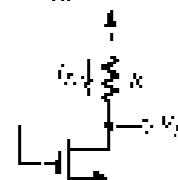


FIGURE 4.21 Circuit for Example 4.3

Solution

Since $V_{GS} > 0$, $V_s = V_t$, and the FET is operating in the saturation region. Thus,

$$\begin{aligned} I_D &= \frac{1}{2} \mu_s C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \\ &= \frac{1}{2} \mu_s C_{ox} \frac{W}{L} V_{DS}^2 \end{aligned}$$

From which we obtain V_{DS}

$$\begin{aligned} V_{DS} &= \sqrt{\frac{2I_D}{\mu_s C_{ox} (W/L)}} \\ &= \sqrt{\frac{2 \times 80}{200 \times (4 \times 0.8)}} = 0.4\text{ V} \end{aligned}$$

Thus,

$$V_{DD} = V_s + V_{DS} = 0.5 + 0.4 = 1\text{ V}$$

and the drain voltage will be

$$V_D = V_s = -5\text{ V}$$

The required value of R can be found as follows:

$$\begin{aligned} R &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{1 + 5}{0.080} = 25\text{ k}\Omega \end{aligned}$$

EXERCISE

- 4.11 Redesign the circuit in Example 4.3 to double the value of I_D , from three times the V_t . Other parameters for the NMOS transistor are the same as in Example 4.3. Find V_D and V_{DS} .
- 4.12 Consider the circuit of Fig. 4.22, which is a common-emitter configuration. What is the output voltage V_{out} for the specified condition? Then, calculate the output voltage V_{out} for the condition that $V_D = 0$. Assume that $V_t = 0.5\text{ V}$, $V_{DD} = 10\text{ V}$, and $V_{SS} = 0$.

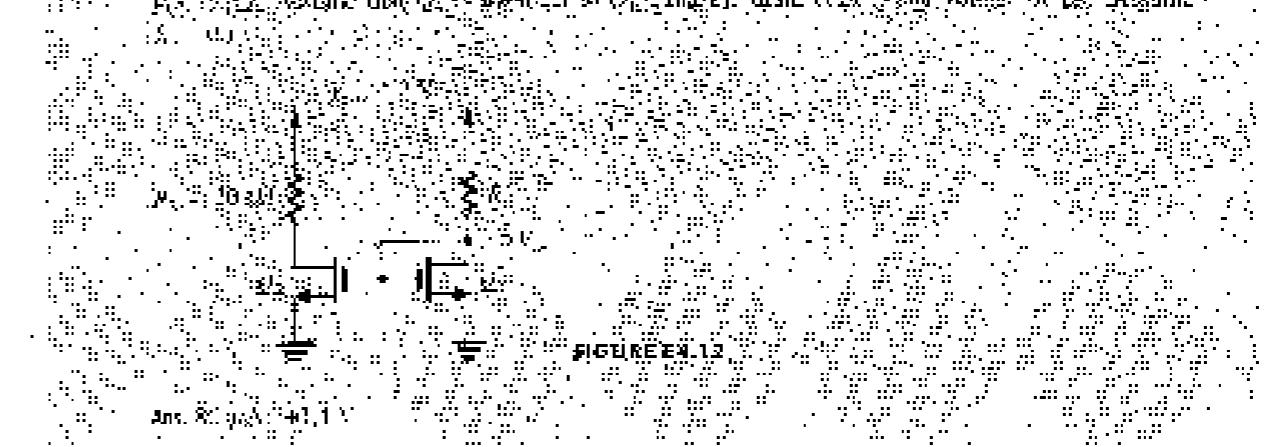


FIGURE 4.22

$$\text{Ans. } V_{out} = 4.1\text{ V}$$

EXERCISE

- Design the circuit in Fig. 4.22 to establish a drain voltage of 0.1 V . What is the effective resistance between drain and source at this operating point? (*i.e.*, $V_t = 1\text{ V}$ and $\mu_s W/L = 1\text{ mA/V}^2$).

$$V_{DD} = 1.5\text{ V}$$

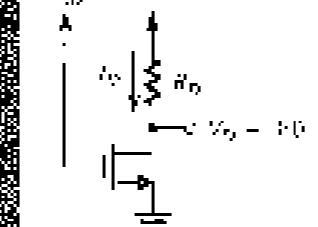


FIGURE 4.22 Common-emitter circuit for Exercise 4.12

Solution

Since the drain voltage is lesser than the gate voltage by 4.9 V and $V_t = 1\text{ V}$, the NMOSFET is operating in the triode region. Thus the current I_D is given by

$$\begin{aligned} I_D &= \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ I_D &= 1 \times \left(5 - 1 \right) \times 0.1 - \frac{1}{2} \times 0.01 \\ &\approx 0.395\text{ mA} \end{aligned}$$

The required value for R_s can be found as follows:

$$\begin{aligned} R_s &= \frac{V_{DS} - V_D}{I_D} \\ &= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega \end{aligned}$$

In a practical discrete-circuit design problem one selects the closest standard value available for, say, 12 k Ω —in this case, 12 k Ω ; see Appendix G. Since the transistor is operating in the triode region, we should note the effective drain-to-source resistance can be determined as follows:

$$\begin{aligned} r_{DS} &= \frac{V_{DS}}{I_D} \\ &= \frac{0.1}{0.395} = 0.25 \text{ k}\Omega \end{aligned}$$

EXERCISE

- 4.13 Use the circuit of Fig. 4.29(a) to determine the drain current and the drain-to-source voltage for the NMOS transistor.

Ans. 0.2 mA, 0.89 V

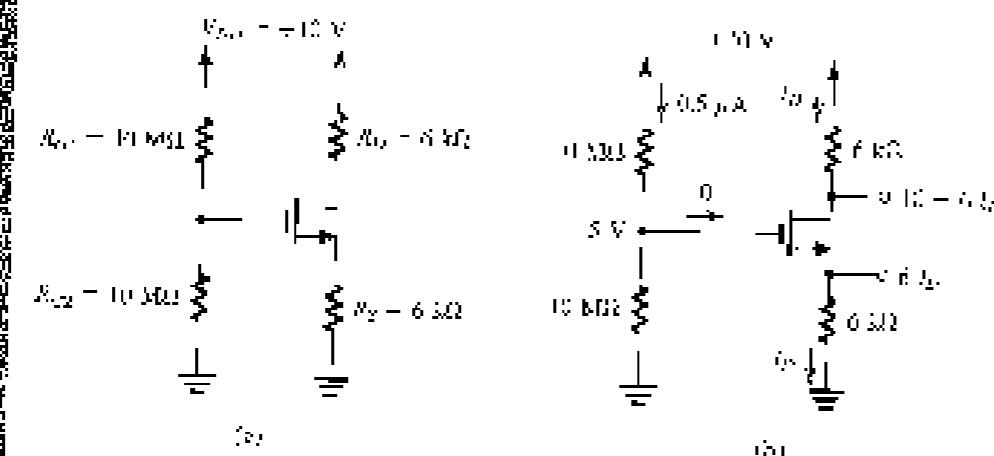


FIGURE 4.29 (a) Circuit for use in Ex. 4.13. The circuit will prove useful in analyzing the circuit in Fig. 4.29(b).

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10 M Ω resistors,

$$V_G = V_{DD} \frac{R_{S2}}{R_{S1} + R_{S2}} = 12 \times \frac{10}{10 + 10} = 6 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We will assume saturation-region operation, solve the problem, and then check the validity of our assumption. Previously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 4.29(b). Since the voltage at the gate is 6 V and the voltage at the source is $I_D(0.2) \times 6 \text{ k}\Omega = 6 I_D$, we have

$$V_{GS} = 6 - 6 I_D$$

Thus I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_T)^2 \\ &= \frac{1}{2} \times 1 \times 10^{-14} (6 - 6 I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D :

$$18 I_D^2 - 25 I_D + 3 = 0$$

This equation yields two values for I_D : 0.89 mA and 0.3 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$, which is greater than the gate voltage and thus not in physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$\begin{aligned} I_D &= 0.3 \text{ mA} \\ V_G &= 6 - 1.8 \text{ V} \\ V_{GS} &= 6 - 1.8 = 4.2 \text{ V} \\ V_D &= 12 - 6 \times 0.3 = 10.2 \text{ V} \end{aligned}$$

Since $V_D > V_G - V_T$, the transistor is operating in saturation, as initially assumed.

EXERCISE

- 4.14 The circuit of Fig. 4.29(b), what is the largest value that R_{S2} can have while the transistor remains in the saturation region?
- Ans. 12.5 k Ω
- 4.15 Redesign the circuit of Fig. 4.29(b) so that the total voltage drop across the two resistors R_{S1} and R_{S2} is 1.5 V. Assume $V_{DD} = 12 \text{ V}$, $V_T = 1 \text{ V}$, and $k_n = 1 \text{ mA/V}^2$. The drain-to-source voltage V_{DS} is to be 5 V. The drain current I_D is to be 0.5 mA. Formulate the equations for R_{S1} and R_{S2} .

Design the circuit of Fig. 4.24 so that the transistor operates in saturation with $I_D = 0.5 \text{ mA}$ and $V_{DS} = -3 \text{ V}$. If the enhancement-type PMOS transistor have $V_t = 1 \text{ V}$ and $k_p(W/L) = 1 \text{ mA/V}^2$, assume $\lambda = 0$. What is the largest value that R_{SD} can have while maintaining saturation-region operation?

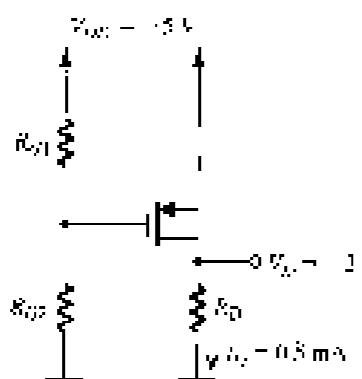


FIGURE 4.24 Circuit for Example 4.6.

Solution

Since the NMOSFET is to be in saturation, we can write

$$\begin{aligned} I_D &= \frac{1}{2} k_p \frac{W}{L} (V_{GS} - V_t)^2 \\ &= \frac{1}{2} k_p \frac{W}{L} V_{GS}^2 \end{aligned}$$

Substituting $I_D = 0.5 \text{ mA}$ and $k_p(W/L) = 1 \text{ mA/V}^2$ and recalling that for a PMOS transistor $V_{GS} \approx V_{DS}$, we obtain

$$V_{GS} = 1 \text{ V}$$

and

$$V_{DS} = V_g - V_{GS} = -1 - 1 = -2 \text{ V}$$

Since the source is at -3 V , the gate voltage must be no less than -3 V . This can be achieved by the appropriate selection of the values of R_{GS} and R_{SD} . A suitable solution is $R_{GS} = 1.2 \text{ M}\Omega$ and $R_{SD} = 3 \text{ M}\Omega$.

The value of R_S can now be found:

$$R_S = \frac{V_{GS}}{I_D} = \frac{1}{0.5} = 2 \text{ k}\Omega$$

Since saturation operation will be maintained up to the point that V_{GS} exceeds V_t by $\sqrt{2}$, that is, until

$$V_{GS} = 1 + 1 = 2 \text{ V}$$

This value of V_{GS} is obtained with R_S given by

$$R_S = \frac{4}{0.5} = 8 \text{ k}\Omega$$

EXAMPLE 4.7

The NMOS and PMOS transistors in the circuit of Fig. 4.25(a) are matched with $k_p(W/L_1) = 1 \text{ mA/V}^2$ and $V_t = -1 \text{ V}$. Assume $\lambda = 0$ for both devices and the drain currents I_{Q1} and I_{Q2} , as well as the voltage v_g , for $v_g = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

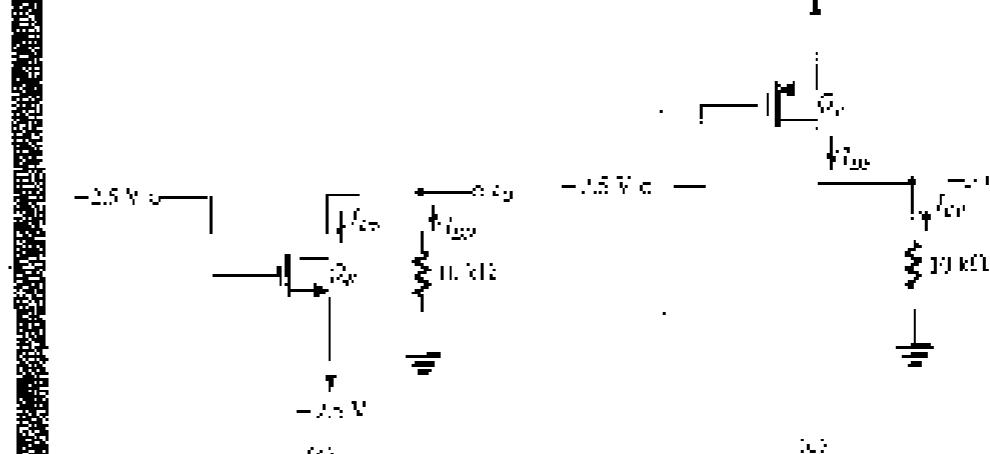
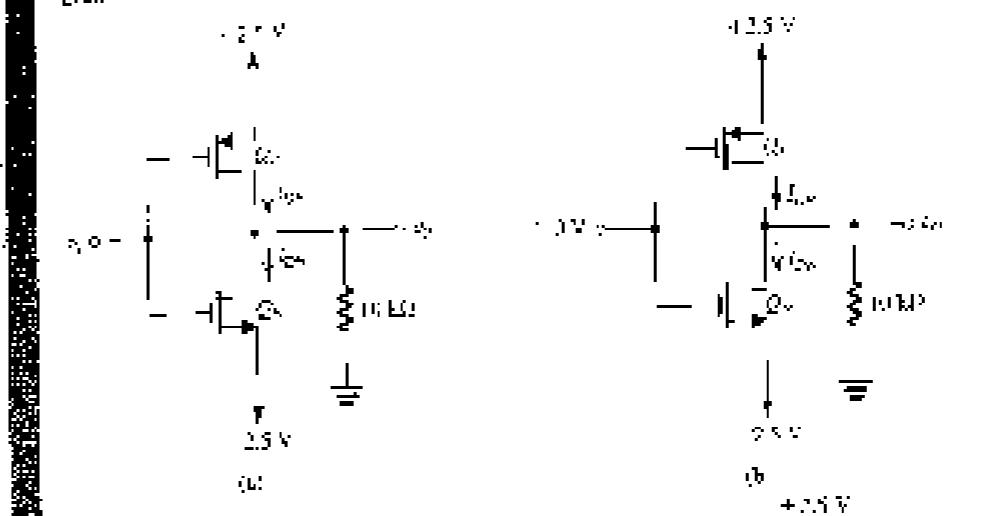


FIGURE 4.25 Circuits for Example 4.7.

Solution

Figure 4.25(b) shows the circuit for the case $v_g = 0 \text{ V}$. We note that since Q_1 and Q_2 are perfectly matched and are operating in saturation, $|V_{DS}|(2.5 \text{ V})$, the circuit is symmetrical, which implies that $v_g = 0 \text{ V}$. Thus both Q_1 and Q_2 are operating with $|V_{GS}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$\begin{aligned} I_{Q1} &= I_{Q2} = \left(\frac{V_{DD}}{2} \times 1.2\right)^2 \\ &= 1.125 \text{ mA} \end{aligned}$$

Next, we consider the circuit with $v_g = +2.5 \text{ V}$. Transistor Q_2 will have a V_{GS} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 4.25(c). We note that v_g will be

negative, and thus v_{ds} will be greater than V_s , causing Q_2 to operate in the triode region. For simplicity we shall assume that v_{ds} is small and nonzero:

$$\begin{aligned} I_{DS} &= V_D(4R_D + 1)(V_{DS} - V_A)V_{GS} \\ &= (12.5 - (-2.5)) \cdot 2(I_{DS} - (-2.5)) \end{aligned}$$

From the circuit diagram shown in Fig. 4.25(c), we can also write

$$I_{DS}(mA) = \frac{0 - v_D}{10(3k\Omega)}$$

These two equations can be solved simultaneously to yield

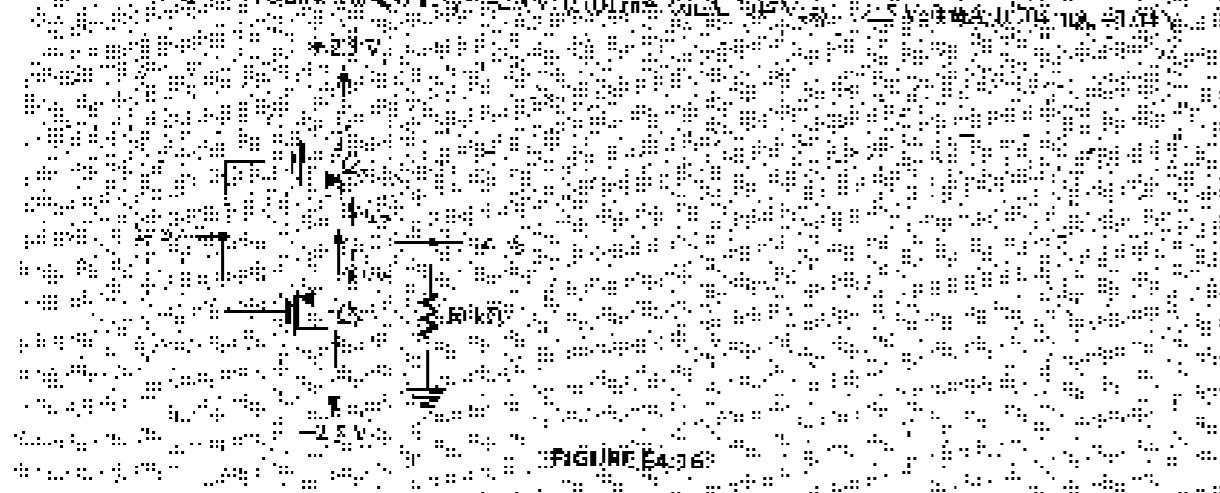
$$I_{DS} = 0.244 \mu A \quad v_D = -2.44 V$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06 V$, which is small as assumed.

Finally, the situation for the case $v_i < -2.5 V$ [Fig. 4.25(d)] will be the exact complement of the case $v_i = -2.5 V$. Transistor Q_1 will be off. Thus $I_{DS} = 0$. Q_2 will be operating in the triode region with $I_{DS} = 0.44 \mu A$ and $v_D = -2.44 V$.

EXERCISE

- 4.16 For NMOS and PMOS common-source circuits like that in Fig. 4.16, the required input voltage v_i (from v_{DD}) is $v_i = 1.5 V$ for saturation, $v_i = 0.5 V$ for breakdown, and $v_i = -1.5 V$ for breakdown. For $v_i = -2.5 V$ and $-2.6 V$, determine the drain current I_{DS} and the drain-to-source voltage v_D for each case. Assume $R_D = 10 k\Omega$, $R_S = 10 k\Omega$, $R_G = 100 k\Omega$, $V_{DD} = 5 V$, $V_A = 0.5 V$, and $k_n = 0.01 \mu A/V^2$.



4.4 THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

In this section we begin our study of the use of MOSFETs in the design of amplifier circuits.⁶ The basis for this important MOSFET application is that when operated in the saturation region, the MOSFET acts as a voltage-controlled current source. Changes in the gate-to-source voltage

⁶ An introduction to amplifiers from an electrical engineer's point of view was presented in Chapter 1 (Sections 1.4 and 1.5), and it would be helpful for readers who are familiar with basic amplifier techniques to review some of this material before proceeding with the study of MOS amplifiers.

will give rise to changes in the drain current I_D . Thus the saturated MOSFET can be used to implement a voltage-controlled current source (see Section 1.5). However, since we are interested in linear amplification—that is, in amplifiers whose output signal (in this case, the drain current I_D) is linearly related to their input signal (in this case, the gate-to-source voltage v_{GS})—we will have to find a way around the highly nonlinear (saturation) relationship of I_D to v_{GS} .

The technique we will utilize to obtain linear amplification from a fundamentally non-linear device is that of biasing the MOSFET to operate at a certain appropriate V_{GS} and v_{DS} corresponding to I_D , and then superimposing the voltage signal to be amplified, v_{GS} , on the dc bias voltage V_{GS} . By keeping the signal v_{GS} "small," the resulting change in drain current I_D can be made proportional to v_{GS} . This technique was introduced in a general way in Section 1.4 and was applied in the case of the diode in Section 1.3.8. However, before considering the small-signal operation of the MOSFET amplifier, we will look at the "big picture". We will study the total or large-signal operation of a MOSFET amplifier. We will do this by deriving the voltage transfer characteristic of a commonly used MOSFET amplifier circuit. From the voltage transfer characteristic we will be able to clearly see the region over which the amplifier can be biased to operate as a small-signal amplifier as well as those regions where it can be operated as a switch (i.e., being either fully "on" or fully "off"). MOS switches find application in both analog and digital circuits.

4.4.1 Large-Signal Operation—The Transfer Characteristic

Figure 4.26(a) shows the basic structure (skeleton) of the most commonly used MOSFET amplifier, the common-source (CS) circuit. The name common-source is given because

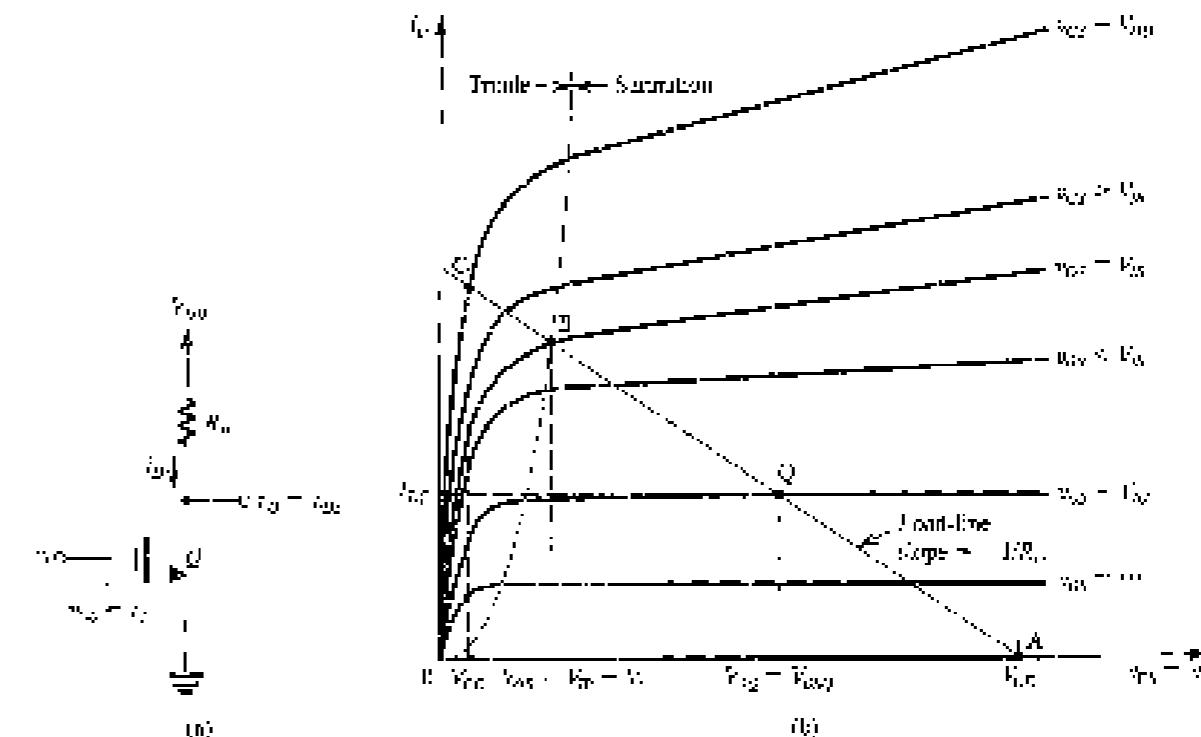


FIGURE 4.26 (a) Basic structure of the common-source amplifier. (b) Required circuit to determine the static characteristics of the amplifier in (a).

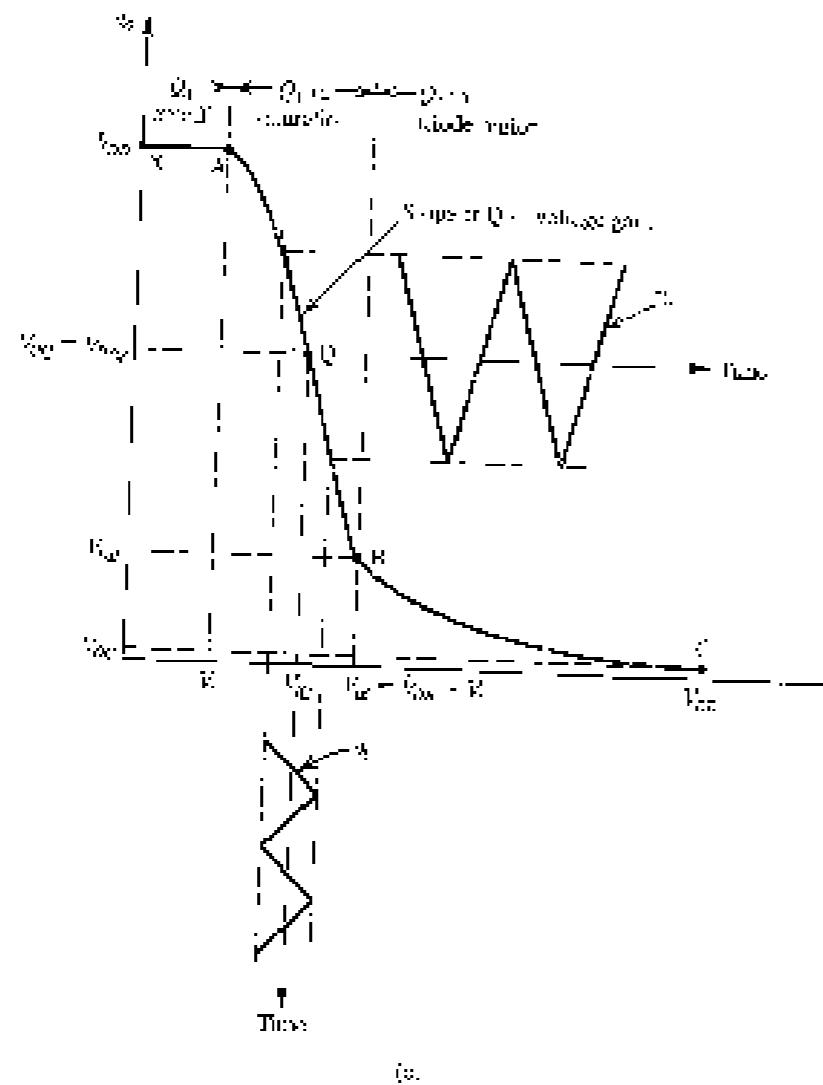


FIGURE 4.26 (Continued) (c) Transfer characteristic showing operation in amplification mode at point Q.

circuit arises because when the circuit is viewed as a two-port network, the ground-to-source terminal is connected to both the input port, between gate and source, and the output port, between drain and source. Note that although the basic control action of the MOSFET is that changes in v_g (base, changes in v_{Dg}) cause changes in i_D (gate-to-drain currents), we are using a resistor R_D to obtain an output voltage v_D .

$$v_D = v_{DD} - R_D i_D \quad (4.35)$$

In this way, the transconductance amplifier is converted into a voltage amplifier. Mindly, note that of course a dc power supply is needed to turn the MOSFET on and to supply the necessary power for its operation.

We wish to analyze the circuit of Fig. 4.26(a) to determine its output voltage v_o for various values of its input voltage v_i , that is, to determine the voltage transfer characteristic.

As in Fig. 4.26(a), we will assume v_i to be in the range of 0 to V_{DD} . To obtain greater insight into the operation of the circuit, we will derive its transfer characteristic in two ways, graphically and analytically.

4.4.2 Graphical Derivation of the Transfer Characteristic

The operation in the common-source circuit is governed by the MOSFET's i_D-v_{Dg} characteristics and by the relationship between v_i and v_{Dg} imposed by connecting the drain to the power supply V_{DD} via resistor R_D , namely

$$v_{Dg} = V_{DD} - R_D i_D \quad (4.36)$$

or equivalently,

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{Dg} \quad (4.37)$$

Figure 4.26(b) shows a sketch of the MOSFET's i_D-v_{Dg} characteristic curves superimposed on which is a straight line representing the i_D-v_{Dg} relationship of Eq. (4.37). Observe that the straight line intersects the v_{Dg} axis at V_{DD} (since from Eq. (4.36) $v_{Dg} = V_{DD}$ at $i_D = 0$) and has a slope of $-1/R_D$. Since R_D is usually thought of as the load resistor of the amplifier (i.e., the resistor across which the amplifier provides its output voltage), the straight line in Fig. 4.26(b) is known as the load line.

The graphical construction of Fig. 4.26(a) can now be used to determine v_o (equal to v_{Dg}) for each given value of v_i (as $v_i \rightarrow v_D$). Specifically, for any given value of v_i , we locate the corresponding i_D-v_{Dg} curve and find v_o from the point of intersection of this curve with the load line.

Qualitatively, the circuit works as follows: Since $v_{Dg} = v_D$, we see that for $v_i < V_D$, the transistor will be cut off, i_D will be zero, and $v_D = v_{DD} - V_D$. Operation will be at the point labeled A. As v_i exceeds V_D , the transistor turns on, i_D increases, and v_D decreases. Since v_D will initially be high, the transistor will be operating in the saturation region. This corresponds to points along the segment of the load line from A to B. We have identified a particular point in this region of operation and labeled it C. This is obtained for $v_D = V_{DD}$, that is, the coordinates $(v_D, v_{Dg}) = (V_{DD}, V_{DD})$.

Saturation-region operation continues until v_D decreases to the point that it is below a v_D (V_D) volt. At this point, $v_{Dg} = v_{DD} - V_D$, and the MOSFET enters its triode region of operation. This is indicated in Fig. 4.26(b) by point B, which is at the intersection of the load line and the broken-line curve that defines the boundary between the saturation and the triode regions. Point B is defined by

$$V_{DD} = V_{DD} - V_D$$

For $v_i > V_{DD}$, the transistor is driven deeper into the triode region. Note that because the characteristic curves in the triode region are bunched together, the output voltage decreases slowly towards zero. Here we have identified a particular operating point D, obtained for $v_i = V_{DD}$. The corresponding output voltage V_{DD} will usually be very small. This point, by point decomposition of the transfer characteristic, results in the truncated curve shown in Fig. 4.26(c). Observe that we have delineated six distinct segments, each corresponding to one of the three regions of operation of MOSFET Q. We have also labeled the crucial points of the transfer curve in correspondence with the points in Fig. 4.26(b).

4.4.3 Operation as a Switch

When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve. Specifically, the device is turned off by keeping $v_g < v_t$, resulting in operation near where on the segment XA with $v_d = V_{DD}$. The switch is turned on by applying a voltage close to V_{DD} , resulting in operation close to point C with v_g very small (at C, $v_g = V_{DD}$). As this situation we observe from the transfer curve of Fig. 4.20(e), one of the four presented in Section 1.7 for the digital logic inverter. Indeed, the增强型 source MOSFET can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close to V_{DD} . More elaborate MOS logic inverters are studied in Section 4.10.

4.4.4 Operation as a Linear Amplifier

To operate the MOSFET as an amplifier we make use of the saturation-linear segment of the transfer curve. The device is biased at a point located somewhere close to the middle of the curve: point Q is a good example of an appropriate bias point. The dc bias point is also called the quiescent point, which is the reason for labeling it Q. The voltage signal to be amplified is then superimposed on the dc voltage v_g , as shown in Fig. 4.26(c). By keeping α sufficiently small to restrict operation to an almost linear segment of the transfer curve, the resulting output voltage v_{ds} will be proportional to v_s . That is, the amplifier will be very nearly linear, and v_o will have the same waveform as v_s , except that it will be larger by a factor equal to the voltage gain of the amplifier at Q, A_v , where

$$A_v = \left. \frac{dv_o}{dv_s} \right|_{v_g = V_g} \quad (4.38)$$

Thus the voltage gain is equal to the slope of the transfer curve at the bias point Q. Observe that the slope is negative, and thus the basic CS amplifier is "inverting." This should be also evident from the waveforms of v_s and v_o shown in Fig. 4.26(c). It should be obvious that if the amplitude of the input signal v_s is increased, the output signal will become distorted since operation will no longer be restricted to an almost linear segment of the transfer curve.

We shall return to the small-signal operation of the MOSFET in Section 4.6. For the time being, however, we wish to make an important observation about selecting an appropriate location for the bias point Q. Since the output signal will be superimposed on the dc voltage in the drain (V_{DD}) or V_{DSQ} , it is important that V_{DSQ} be of such value to allow for the required output signal swing. That is, V_{DSQ} should be lower than V_{DD} by a sufficient amount and higher than V_{DD} by a sufficient amount to allow for the required positive and negative output signal swing, respectively. If V_{DSQ} is too close to V_{DD} , the positive peaks of the output signal might "but" into V_{DD} and would be clipped off, because the MOSFET would turn off for part of the cycle. We speak of this situation as the circuit not having sufficient "headroom." Similarly, if V_{DSQ} is too close to the boundary of the triode region, the MOSFET would enter the triode region for the part of the cycle near the negative peaks, resulting in a distorted output signal. We speak of this situation as the circuit not having sufficient "tailroom." Finally, it is important to note that although we made our comments on the selection of bias-point location in the context of a given transfer curve, the circuit designer also has to decide on a value for R_{DS} , which of course determines the transfer curve. It is therefore more appropriate when considering the location of the bias point Q to do so with reference to the i_D-v_{DS} plane. This point is further illustrated by the sketch in Fig. 4.27.

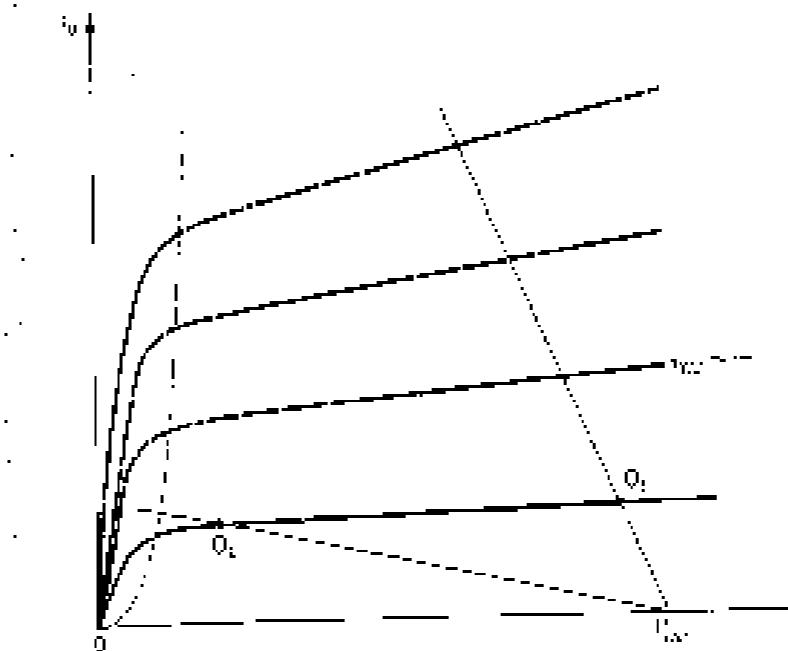


FIGURE 4.27 Two-level linear corresponding bias points P vs point Q. Note one leads sufficient room to the positive-swing swing (close to V_{DD}) while point Q is too close to the boundary of the triode region, the right to follow for sufficient negative signal swing.

4.4.5 Analytical Expressions for the Transfer Characteristic

The i_v -relationships that describe the MOSFET operation in the three regions—cutoff, saturation, and triode—can be easily used to derive analytical expressions for the three segments of the transfer characteristic in Fig. 4.26(a).

The Cutoff-Region Segment, XA: Here, $v_g < v_t$ and $v_d = V_{DD}$.

The Saturation-Region Segment, AQB: Here, $v_g > v_t$ and $v_d \approx v_g = V_g$. Neglecting channel length modulation and substituting for i_D from

$$i_D = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_g - V_t)^2$$

gives

$$v_o = V_{DD} - R_{DS} i_D \quad (4.39)$$

$$v_o = V_{DD} - \frac{1}{2} R_{DS} C_{ox} \frac{W}{L} (v_g - V_t)^2$$

We can use this relationship to derive an expression for the incremental voltage gain A_v at a bias point Q at which $v_g = V_g$ is obtained:

$$A_v = \left. \frac{dv_o}{dv_s} \right|_{v_g = V_g}$$

Thus,

$$A_v = -R_o \mu_s C_{ox} \frac{W}{L} (V_{ds} - V_t) \quad (4.40)$$

Observe that the voltage gain is proportional to the values of R_o , the transconductance parameter $\mu_s = \mu_s C_{ox}$, the transistor aspect ratio W/L , and the overdrive voltage at the bias point: $V_{ds} - V_t = V_{ds}$.

Another simple and very useful expression for the voltage gain can be obtained by substituting $v_2 = V_{ds}$ and $v_0 = V_{ds0}$ in Eq. (4.39), utilizing Eq. (4.40), and substituting $V_{ds} = V_t + V_{os}$. The result is

$$A_v = \frac{2(V_{ds0} - V_{ds})}{V_{os}} = \frac{2V_{os}}{V_{os}} \quad (4.41)$$

where V_{os} is the dc voltage across the drain resistor R_o , that is, $V_{os} = V_{ds0} - V_{ds}$.

The end point of the saturation-region segment is characterized by

$$V_{os0} = V_{ds} - V_t \quad (4.42)$$

Thus its coordinates can be determined by substituting $v_0 = V_{os0}$ and $v_2 = V_t$ in Eq. (4.39) and solving the resulting equation simultaneously with Eq. (4.42).

The Triode-Region Segment, BC Here, $v_0 > V_t$, thus $v_0 \leq v_2 = V_t$. Substituting for i_d by the triode-region expression

$$i_d = \mu_s C_{ox} \frac{W}{L} [(v_2 - V_t)v_0 - \frac{1}{2}v_0^2]$$

into

$$v_0 = V_{ds0} - R_o i_d$$

gives

$$v_0 = V_{ds0} - R_o \mu_s C_{ox} \frac{W}{L} [v_2 - V_t] v_0 - \frac{1}{2}v_0^2$$

The portion of this segment for which v_0 is small is given approximately by

$$v_0 \approx V_{ds0} - R_o \mu_s C_{ox} \frac{W}{L} (v_2 - V_t) v_0$$

which reduces to

$$v_0 = V_{ds0} \left[1 + R_o \mu_s C_{ox} \frac{W}{L} (v_2 - V_t) \right] \quad (4.43)$$

We can use the expression for r_{ds} , the drain-to-source resistance near the origin of the i_d - v_{ds} plane (Eq. 4.15),

$$r_{ds} = 1 / \left[\mu_s C_{ox} \frac{W}{L} (v_2 - V_t) \right]$$

together with Eq. (4.43) to obtain

$$v_0 = V_{ds0} \frac{r_{ds}}{r_{ds} + R_o} \quad (4.44)$$

which makes intuitive sense. For small v_0 , the MOSFET operates as a resistance r_{ds} (whose value is determined by v_2), which forms with R_o a voltage divider across V_{ds0} . Usually, $r_{ds} \ll R_o$, and Eq. 4.44 reduces to

$$v_0 \approx V_{ds0} \frac{r_{ds}}{R_o} \quad (4.45)$$

To make the above analysis more concrete we consider a numerical example. Specifically, consider the CS circuit of Fig. 4.26(a) for the case $k_A' (W/L) = 1 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, $R_o = 10 \text{ k}\Omega$, and $V_{ds0} = 10 \text{ V}$.

Solution

First, we determine the coordinates of important points on the transfer curve.

(a) Point X:

$$v_1 = 0 \text{ V}, \quad v_2 = 10 \text{ V}$$

(b) Point A:

$$v_1 = 1 \text{ V}, \quad v_2 = 10 \text{ V}$$

(c) Point B: Substituting

$$\begin{aligned} v_1 &= V_{ds} = V_{os0} - V_t \\ &= V_{os} + 1 \end{aligned}$$

and $v_2 = V_{os}$ in Eq. (4.39) results in

$$9V_{os}^2 + V_{os} - 10 = 0$$

which has two roots, only one of which makes physical sense, namely,

$$V_{os} = 1 \text{ V}$$

Correspondingly,

$$V_t + 1 + 1 = 2 \text{ V}$$

(d) Point C: From Eq. (4.43) we find

$$V_{os} = -\frac{10}{1 + 9 \times 1 \times (10 - 1)} = 0.091 \text{ V}$$

which is very small, justifying our use of the approximate expression in Eq. (4.43).

Next, we let the amplifier to operate at an appropriate point on the saturation-region segment. Since this segment extends from $v_0 = 1 \text{ V}$ to 3 V , we choose to operate at $V_{os} = 4 \text{ V}$. This point allows for reversible signals swing in both directions and provides a higher voltage gain than the middle of the range (i.e., at $V_{os} = 5.5 \text{ V}$). To operate at an intermediate voltage

$V_s + V_b$, the drain current could be

$$I_D = \frac{V_{DS} - V_{DS2}}{R_D} = \frac{10 - 4}{8} = 0.750 \text{ mA}$$

We can find the required operating voltage V_{GS} from

$$I_D = \frac{1}{2} C_L V_{GS}^2$$

$$V_{GS} = \sqrt{\frac{2 \times 0.750}{C_L}} = 0.86 \text{ V}$$

Thus, we can operate the MOSFET at a drain-to-source voltage

$$V_{DS2} = V_s + V_{GS} = 1.816 \text{ V}$$

The voltage gain of the amplifier at this bias point can be found from Eq. (4.40) as

$$\begin{aligned} A_v &= -18 \times 1 \times (1.816 - 1) \\ &= -14.7 \text{ V/V} \end{aligned}$$

To gain insight into the operation of the amplifier we apply an input signal v_i of, say, 100 mV peak-to-peak amplitude, of, say, triangular waveform. Figure 4.28(a) shows such a signal superimposed on the bias voltage $V_{GS2} = 1.816 \text{ V}$. As shown, v_{GS} varies linearly between 1.741 V and 1.891 V around the bias value of 1.816 V. Correspondingly, i_D will be

$$\text{At } v_{GS} = 1.741 \text{ V, } i_D = \frac{1}{2} \times 1 \times (1.741 - 1)^2 = 0.275 \text{ mA}$$

$$\text{At } v_{GS} = 1.816 \text{ V, } i_D = \frac{1}{2} \times 1 \times (1.816 - 1)^2 = 0.351 \text{ mA}$$

$$\text{At } v_{GS} = 1.891 \text{ V, } i_D = \frac{1}{2} \times 1 \times (1.891 - 1)^2 = 0.397 \text{ mA}$$

Note that the negative excursion in i_D is $(0.351 - 0.275) = 0.076 \text{ mA}$ while the positive excursion is $(0.397 - 0.351) = 0.046 \text{ mA}$, which are slightly different, indicating that the region of the i_D - v_{GS} curve for, equivalently, of the v_i - v_o curve is not perfectly linear, as should be expected. The output voltage will vary around the bias value $V_{DS2} = 4 \text{ V}$ and will have the following extrema:

$$\text{At } v_{GS} = 1.741 \text{ V, } v_o = 0.275 \text{ mA, and } v_o = 10 - 0.275 \times 18 = 5.05 \text{ V}$$

$$\text{At } v_{GS} = 1.891 \text{ V, } i_D = 0.397 \text{ mA, and } v_o = 10 - 0.397 \times 18 = 2.85 \text{ V}$$

Thus, while the positive excursion is 1.15 V, the negative excursion is slightly larger at 2.2 V, again a result of the nonlinear transfer characteristic. The nonlinear distortion of v_o can be reduced by reducing the amplitude of the input signal.

Further insight into the operation of this amplifier can be gained by considering its graphical analysis shown in Fig. 4.28(b). Observe that as v_{GS} varies, because of i_D , the instantaneous operating point moves along the load line, being at the intersection of the load line and the i_D - v_{GS} curve corresponding to the instantaneous value of v_{GS} .

We note that by biasing the transistor at a quiescent point, in the middle of the saturation region, we ensure that the instantaneous operating point always remains in the saturation region, and thus nonlinear distortion is minimized. Finally, we note that in this example we extend our calculations to three decimal digits. Simply to illustrate the concepts involved in practice, this degree of precision is not justified for approximate numerical analysis.

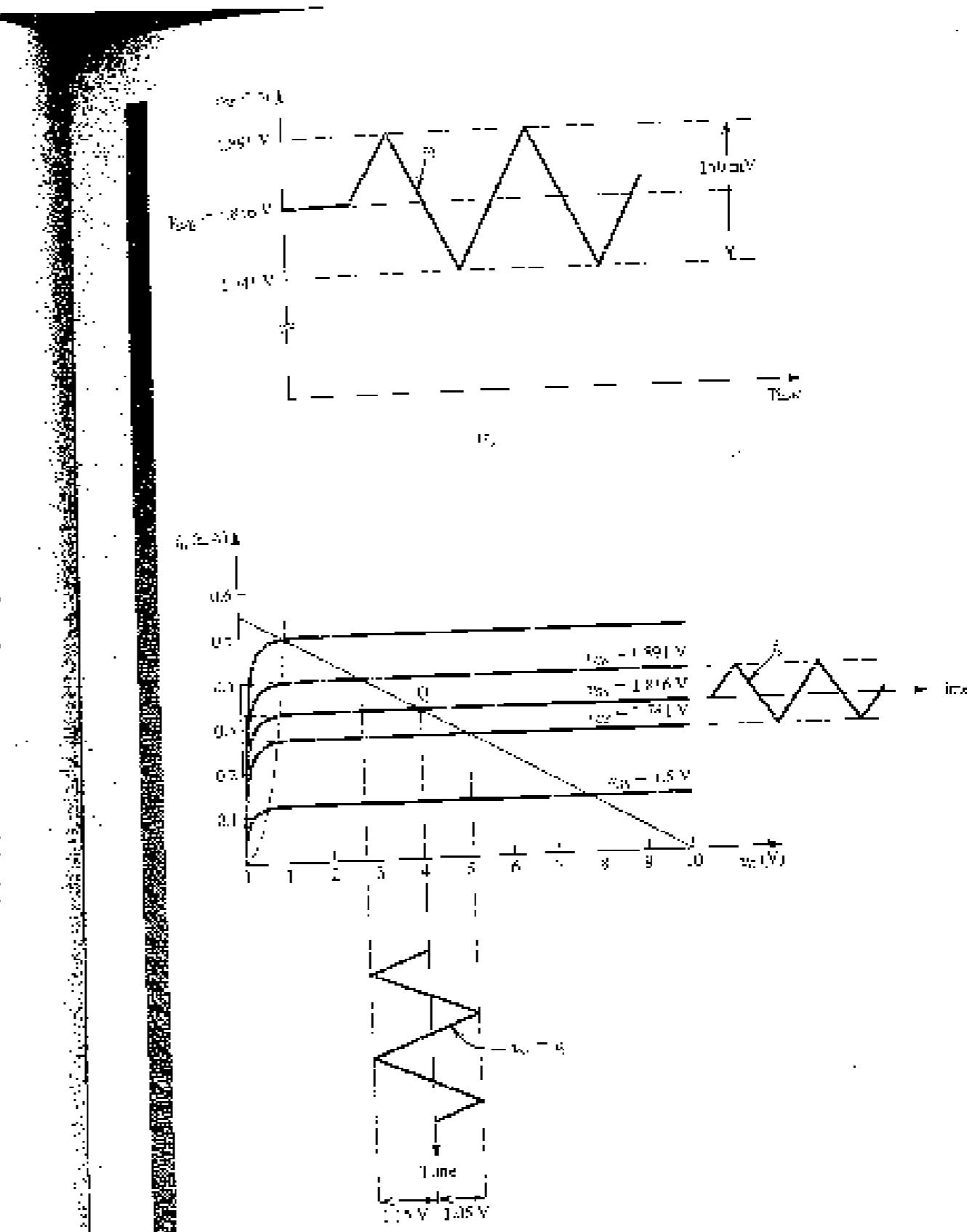


FIGURE 4.28 Example 4.8.

4.4.6 A Final Remark on Biasing

In the above example, the MOSFET was assumed to be biased at a constant bias of 13.6 V. Although it is possible to generate a constant bias voltage using an appropriate voltage divider network across the power supply V_{DD} or across another reference voltage that may be available in the system, fixing the value of V_{GS} is not a good biasing technique. In the next section we will explain why this is so and present superior biasing schemes.

EXERCISES

- 4.47 Take the circuit given in Fig. 4.37 and assume that the drain current is to be controlled by V_{GS} (not the gate bias V_{GSS}) and V_{GS} is the dependent variable. The dependent variable will be controlled by a voltage-controlled voltage source with its input voltage being the output of the input signal. Disregarding load, can we still obtain the same drain current? If so, how? Repeat this for the case of V_{GSS} fixed and the drain current dependent upon V_{GS} . In this case, what is the maximum gain that can be obtained? What is the operating point and what is the corresponding drain-to-source voltage? What will happen when the input voltage varies? Will this differ significantly from the MOSFET example 4.46?
- Ans. (in) 316 V_{G2}, 3.4 V, 1 V; (b) 3.4 V, 13.6 V, 13.6 V
- 4.48 Design the voltage-controlled-current source in Fig. 4.37 based on the expression to verify the drain current found in Example 4.46. Assume that the drain current is to be controlled by V_{GS} and that the drain-to-source voltage is to be controlled by V_{GSS} .

4.5 BIASING IN MOS AMPLIFIER CIRCUITS

As mentioned in the previous section, an essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or biasing. An appropriate dc operating point or bias point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region, our expected input signal levels.

4.5.1 Biasing by Fixing V_{GS}

The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D . This voltage value can be derived from the power-supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage V_{GS} may be generated, this is not a good approach to biasing a MOSFET. To understand the reason, let's consider a typical fault

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{k}{T} (V_{GS} - V_T)^2$$

and note that the values of the threshold voltage V_T , the oxide capacitance C_{ox} , and (to a lesser extent) the transistor aspect ratio $\mu_n C_{ox}$ vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spread in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated circuits, especially among devices that operate on different wafers and switch between different batches or wafers. Furthermore, both V_{GS} and I_D depend on temperature, with the result that if we fix the value of V_{GS} , the drain current I_D becomes very much temperature dependent.

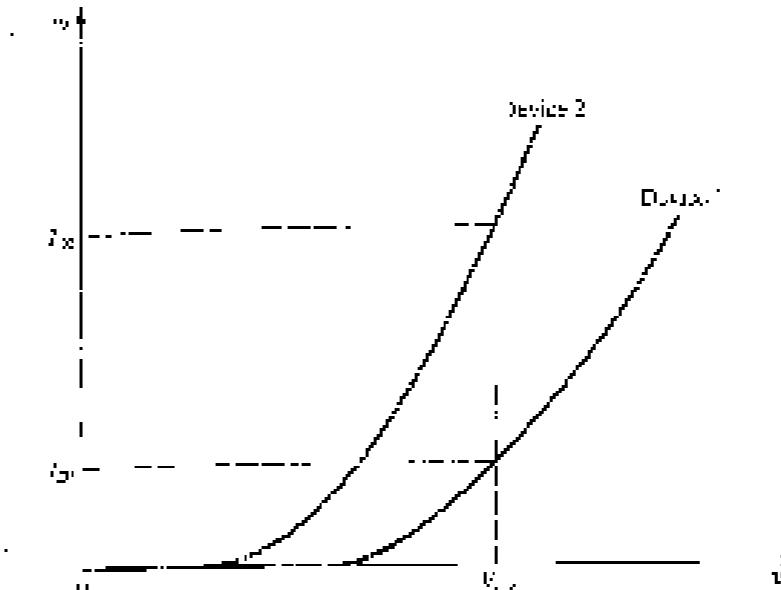


FIGURE 4.29 The word "bias" (constant V_{GS}) can result in a loss of stability if the value of I_D varies due to variations in the drain-to-source voltage.

To emphasize the point that biasing by fixing V_{GS} is not a good technique, we show in Fig. 4.29 two device characteristic curves representing extreme values in a batch of MOSFETs of the same type. Observe that, for the fixed value of V_{GS} , the resultant spread in the values of the drain current can be substantial.

4.5.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G , and connecting a resistance in the source lead, as shown in Fig. 4.30(a). For this circuit we can write

$$V_G = V_{GS} + R_s I_D \quad (4.40)$$

Now, if V_G is much greater than V_{GS} , I_D will be mostly determined by the value of V_G and R_s . However, even if V_G is not much larger than V_{GS} , resistor R_s provides negative feedback, which tends to stabilize the value of the bias current I_D . To see how this comes about, consider the case when I_D increases for whatever reason. Equation (4.40) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D , a change that is asymptotic but initially assumed. Thus the action of R_s works to keep I_D as constant as possible. The negative feedback action of R_s gives it the name degeneration resistance, a name that we will appreciate a bit better at a later point in this text.

Figure 4.30(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here we show the device characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit, namely, V_G , (4.40). The intersection of this straight line with the $I_{D,GS}$ characteristic curve provides the coordinates (I_D, V_{GS}) of the bias point. Observe that, compared to the case of fixed V_{GS} , here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_s are made larger (provided R_s is not too large that is less steep).

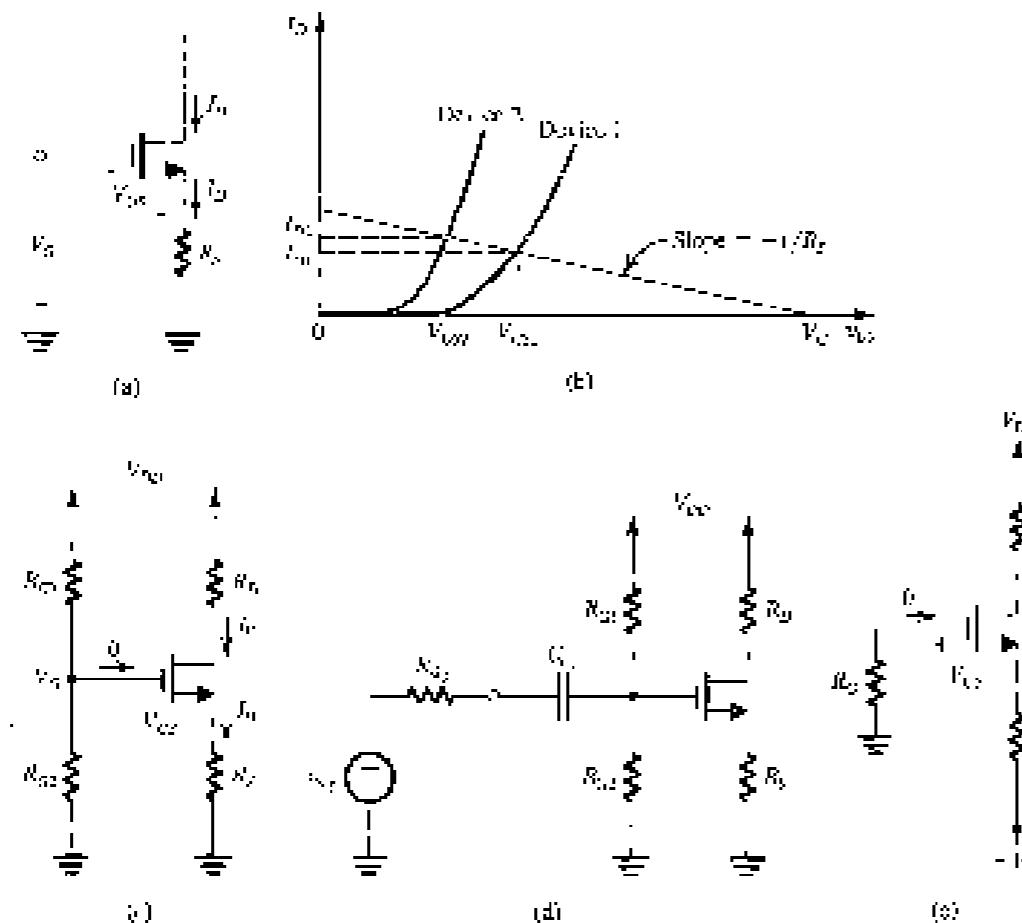


FIGURE 4.30 Biasing using a fixed voltage on the gate, V_{GS} , and a resistor in the source lead, R_s . (a) Load arrangement: by reducing $r_{ds,0}$ in Fig. 4.10, one can implement a load using a single-supply load coupling circuit as far to the right as using a capacitor C_L ; (b) practical implementation using two supplies.

Two possible practical discrete implementations of this basic scheme are shown in Fig. 4.30(c) and (e). The circuit in Fig. 4.30(c) utilizes one power-supply V_{DD} and derives V_T through a voltage divider (R_{V_T} , R_{DD}). Since $I_D = 0$, R_{G1} and R_{G2} can be selected to be very large (in the MΩ range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 4.30(d). Here capacitor C_{G1} blocks dc and thus allows us to couple the signal v_{IN} to the amplifier input without disturbing the MOSFET dc bias point. The value of C_{G1} should be selected sufficiently large so that it approximates a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers which are suitable only in discrete circuit design. In Section 4.7, finally, note that in the circuit of Fig. 4.30(c) resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 4.20(c) can be utilized. This circuit is an implementation of Eq. (4.16), with V_b replaced by V_{bb} . Resistor R_b establishes a dc ground for the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

It is required to design the circuit of Fig. 4.30(c) to establish a drain current $I_D = 0.5 \text{ mA}$. The FET is required to have $V_T = 1 \text{ V}$ and $k'_D W/L = 1 \text{ mA/V}^2$. For simplicity, neglect the MOSFET's output conductance (*i.e.*, assume $g_o = 0$). Use a power-supply $V_{DD} = 15 \text{ V}$. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another having the same $k'_D W/L$, but $V_T = 1.5 \text{ V}$.

Soluções

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_S in proportion to one-third of the power-supply voltage: $V_{DD} \approx 7$ drop across each of R_D , the Transistor (i.e., V_{BE}) and R_S . For $V_{DD} = 15$ V, this choice makes $V_{DSS} = -10$ V and $V_2 = -5$ V. Note, since $I_D \approx$ constant, the value of R_D and R_S is follows:

$$R_o = \frac{V_{DD} - V_L}{I_o} = \frac{15 - 12}{0.5} = 10 \text{ k}\Omega$$

$$R_1 + \frac{V_1}{R_2} = \frac{5}{0.5} = 10 \text{ k}\Omega$$

The required value of V_{C_1} can be determined by first calculating the load voltage V_D , from

$$T_{\psi} = \frac{1}{2}\nabla^2((\Psi/\epsilon_0)^2)$$

$$Q^S = \{x_1, x_2, \dots\}$$

which satisfies $V_{\text{out}} = 1/V_0$, and thus

$$V_{\text{DD}} = V_0 + V_{\text{off}} \approx -1 \pm 2 \text{ V}$$

Now, since $V_1 = +5$ V, V_C must be

4000, 5000, 7000, 10000, 15000

$$V_{\alpha} = V_1 + V_{\omega_3} = \beta + z = -1/\sqrt{2}$$

To establish the voltage at the gate we may select $R_{12} = 2\text{ k}\Omega$ and $R_{13} = 1\text{ M}\Omega$. The no-current bias voltage at the gate we may select $V_{G1} = 2\text{ V}$ and $V_{G2} = -10\text{ V}$. The no-current bias voltage at the drain (-10 V) will then form a positive signal swing of $+5\text{ V}$ (i.e., up to V_{D1}) and a negative signal swing of -4 V (i.e., down to $(V_D - V_2)$).

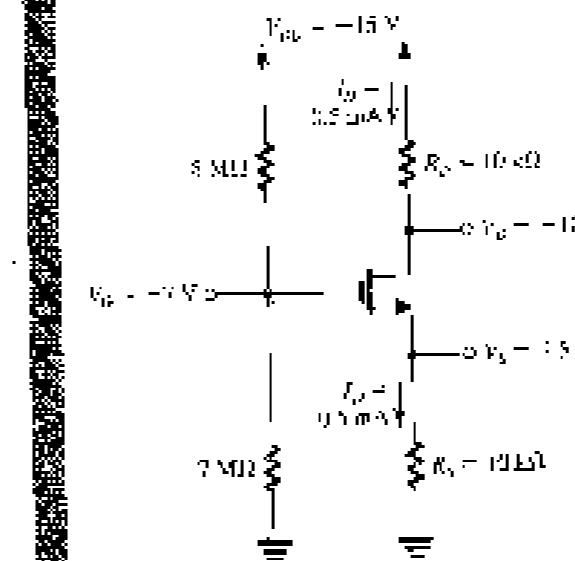


FIGURE 4.31 Circular Example 10

If the NMOS transistor is replaced with another having $V_t = -1.5$ V, the new value of I_D can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad (4.47)$$

$$\begin{aligned} V_G &= V_{DS} - I_D R_D \\ 7 &= V_{DS} + 1.5 I_D \end{aligned} \quad (4.48)$$

Solving Eqs. (4.47) and (4.48) together yields

$$I_D = 0.455 \text{ mA}$$

The change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\frac{-0.045}{0.5} \times 100 = -9\%$ change.

EXERCISES

Ex. 4.27- Consider the NMOSFET in Example 4.2 with $V_t = -1.5$ V and $k = 1$ mA/V². If the drain voltage is set at $V_{DS} = 10$ V, what is the drain current? If the drain voltage is increased to $V_{DS} = 12$ V, what is the drain current?

Ans. $I_D = 0.455 \text{ mA}$

Ex. 4.28- If the drain-to-gate voltage is increased from $V_{GS} = 7$ V to $V_{GS} = 8$ V, the drain current increases by 0.05 mA . Use the values given in Appendix A.2 and the resulting drain current to find the drain-to-source voltage V_{DS} if $R_D = 10$ k Ω , $V_t = -1.5$ V, $k = 1$ mA/V², and $I_D = 0.5$ mA. You may neglect the effect of drain-to-source voltage on the drain current.

4.5.3 Biasing Using a Drain-to-Gate Feedback Resistor

A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 4.32. Here the large feedback resistance R_F (usually 10^6 to 10^8 Ω) forces the dc voltage at the gate to be equal to that at the drain (because $I_D = 0$). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_F I_D$$

which can be rewritten in the form

$$V_{GS} = V_{DD} + R_F I_D \quad (4.49)$$

which is identical to Eq. (4.46), which describes the operation of the bias scheme discussed above (but in Fig. 4.30(a)). Thus, here too, if I_D for some reason changes, say decreases, then Eq. (4.49) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D , a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by R_F works to keep the value of I_D as constant as possible.

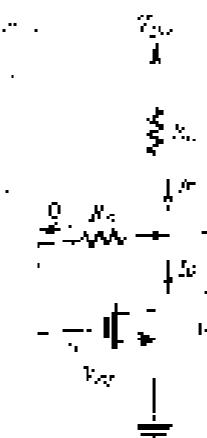


FIGURE 4.32 Biasing the MOSFET using a drain-to-gate feedback resistor, R_F .

The circuit of Fig. 4.32 can be utilized as a CS amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The generated output signal at the drain can be coupled to another part of the circuit again via a capacitor. We shall consider such a CS amplifier circuit in Section 4.6. There we will learn that this circuit has the drawback of a rather limited output voltage signal swing.

EXERCISE

Ex. 4.29- Consider the circuit in Fig. 4.32, utilizing a drain-to-gate resistance of $R_F = 10^8 \Omega$, a drain-to-source voltage of $V_{DS} = 10$ V, a drain current of $I_D = 0.5$ mA, and a drain-to-gate voltage of $V_{GS} = 7$ V. The drain-to-source voltage is to be varied from $V_{DS} = 6.25$ V down to $V_{DS} = 3.75$ V. Use the values obtained from Fig. 4.32 to calculate the corresponding drain current I_D and the drain-to-gate voltage V_{GS} for each value of V_{DS} . Plot the results on a graph of I_D versus V_{DS} .

4.5.4 Biasing Using a Constant-Current Source

The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 4.33(a) shows such an arrangement applied to a discrete MOSFET. Here R_D (usually in the M2 channel) establishes a dc ground at the gate and presents a large resistance to all input signal sources that can be capacitively coupled to the gate. Resistor R_1 establishes an appropriate dc voltage at the drain to allow for the required output signal swing while assuring that the transistor always remains in the saturation region.

A circuit for implementing the constant-current source I_1 is shown in Fig. 4.33(b). The heart of the circuit is transistor Q_1 , whose drain is shorted to its gate and bias is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2} \lambda' \sqrt{\frac{W}{L}} (V_{GS1} - V_A)^2 \quad (4.50)$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R . Since the gate currents are zero,

$$I_{D1} = I_{DS1} = \frac{V_{GS1} + V_{DS1} - V_A}{R} \quad (4.51)$$

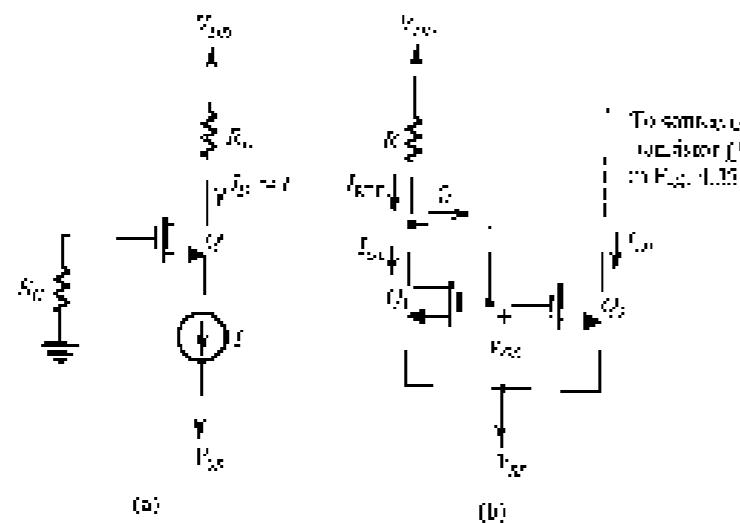


FIGURE 4.33 (a) Biasing the 3dOS-NET using a constant input shown in (b) and $\text{center}_\text{c} = 0.0$, $\text{constant}_\text{c} = 0.0001$ using the constant value.

Here the current through R is considered to be the reference current of the current source and is denoted I_{R2} . Given the parameter values of Q_1 and a desired value for I_{R2} , Eqs. (4.50) and (4.51) can be used to determine the value of R . Now consider transistor Q_3 ; it has the same $V_{DS(on)}$ as Q_1 ; thus if we assume that it's operating in saturation, its drain current, which is the desired current I_{R2} of the current source, will be

$$I = I_{\text{diff}} = \frac{1}{2} k_B \left(\frac{V'}{V} \right) (V_{\text{out}} - V_0)^2 \quad (4.5)$$

where we have used channel-length modulation. Equations (4.51) and (4.52) enable us to relate the current I to the reference current I_0 .

$$t = t_{\text{end}} \cdot \frac{(\Psi/L)}{(\Psi_0/L_0)}, \quad (4.5)$$

Thus V_1 is related to I_{Q_2} , by the ratio of the aspect ratios of P_1 and Q_2 . This circuit, known as a current mirror, is very popular in the design of IC MOS amplifiers and will be studied in greater detail in Chapter 6.

EXERCISE

On 27 May 1945, the first issue of the *Yiddish Journal* was published in New York City. It was founded by the *Yiddish Writers' Association*, which had been established in 1939. The journal was edited by Sholem Asch and published by the *Yiddish Writers' Association*. It was the first Yiddish newspaper in the United States.

4.5.5 & Final Remarks

The logic circuits discussed in this section are intended for discrete-circuit applications. The only exception is the current mirror circuit of Fig. 1.15(b) which, as mentioned above, is extensively used in IC design. Basic arrangements for IC MOS inverters will be studied in Chapter 6.

4.6 SMALL-SIGNAL OPERATION AND MODELS

In our study of the large-signal operation of the common-source MOSFET amplifier in Section 4.4 we learned how linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small. Having studied methods for biasing the MOSFET in the previous section, we now turn our attention to exploring small-signal operation in some detail. For this purpose we utilize the conventional common-source amplifier circuit shown in Fig. 4.34. Here the MOSFET is biased by applying a dc voltage V_{GS} & clearly beyond its threshold by more than i_1 (drain and well suited for our purposes). The input signal to be amplified, v_{in} , is shown superimposed on the drain voltage V_{DS} . The output voltage is taken at the drain.

4.6.1 The DC Bias Point

The peak bias current I_b can be found by setting the signal v_x to zero. When

$$f_{ij} = \frac{1}{2} \delta_i^j \left(V_{\text{max}} - V_{ij} \right)^2 \quad (1.22)$$

where we have neglected channel length modulation (i.e., we have assumed $\lambda = 0$). The derivative of the drug, X_0 , or simply X_0 (since X is unspecified), will be

$$Y_{\alpha\beta} \equiv Y_{\alpha\beta\gamma\delta} = \delta_{\alpha\beta}\delta_{\gamma\delta} \quad (4.55)$$

To ensure substation-feeding operation, we must have

$$V_1 \geq V_{\text{min}} = 1$$

Furthermore, since the total voltage at the drain will have a signal over positive supply voltage V_{DD} , V_D has to be sufficiently greater than $(V_{DD} - V_0)$ to allow for the required signal swing.

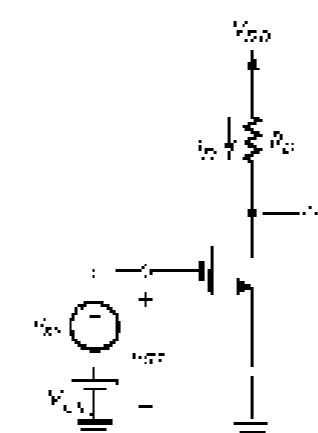


FIGURE 4.24 Overhead circuit realized as $S_1 \oplus S_2$ for operation of the 2010 USL 12-28 a small to small crossover.

4.6.2 The Signal Current in the Drain Terminal

Next consider the situation with the input signal v_{in} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{in} \quad (4.56)$$

resulting in a total instantaneous drain current i_D ,

$$\begin{aligned} i_D &= \frac{1}{2} k_s \frac{W}{L} (V_{GS} + v_{in} - V_0)^2 \\ &\quad + \frac{1}{2} k_s \frac{W}{L} (V_{GS} + V_0)^2 - k_s \frac{W}{L} (V_{GS} - V_0) v_{in} + \frac{1}{2} k_s \frac{W}{L} v_{in}^2 \end{aligned} \quad (4.57)$$

The first term on the right-hand side of Eq. (4.57) can be recognized as the dc bias current I_0 (Eq. 4.53). The second term represents a current component that is directly proportional to the input signal v_{in} . The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents nonlinear distortion. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2} k_s \frac{W}{L} v_{in}^2 \ll k_s \frac{W}{L} (V_{GS} - V_0) v_{in}$$

resulting in

$$v_{in} \ll 2(V_{GS} - V_0) \quad (4.58)$$

or, equivalently,

$$v_{in} \ll 2V_{OD} \quad (4.59)$$

where V_{OD} is the overdrive voltage at which the transistor is operating.

If small-signal condition is satisfied, we may neglect the last term in Eq. (4.57) and express i_D as

$$i_D = I_0 + i_s \quad (4.60)$$

where

$$i_s = k_s \frac{W}{L} (V_{GS} - V_0) v_{in}$$

The parameter that relates i_s and v_{in} is the MOSFET transconductance g_m ,

$$g_m = \frac{i_s}{v_{in}} = k_s \frac{W}{L} (V_{GS} - V_0) \quad (4.61)$$

or, in terms of the overdrive voltage V_{OD} ,

$$g_m = k_s \frac{W}{L} V_{OD} \quad (4.62)$$

Figure 4.35 presents a graphical interpretation of the small-signal operation of the enhancement MOSFET amplifier. Note that g_m is equal to the slope of the i_D-v_{GS} characteristic at the bias point.

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{V_{GS}=V_{GS0}, I_D=I_0} \quad (4.63)$$

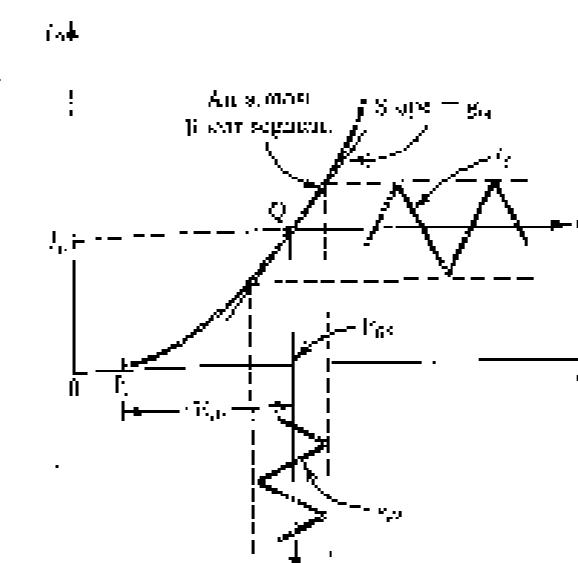


FIGURE 4.35 Small-signal operation of the enhancement MOSFET amplifier.

This is the formal definition of g_m , which can be shown to yield the expression given in Eqs. (4.61) and (4.62).

4.6.3 The Voltage Gain

Referring to the circuit of Fig. 4.31, we can express the total instantaneous drain voltage v_D as follows:

$$v_D = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_D = V_{DD} - R_D (I_0 + i_s)$$

which can be rewritten as

$$i_s = V_{DD} - R_D I_0$$

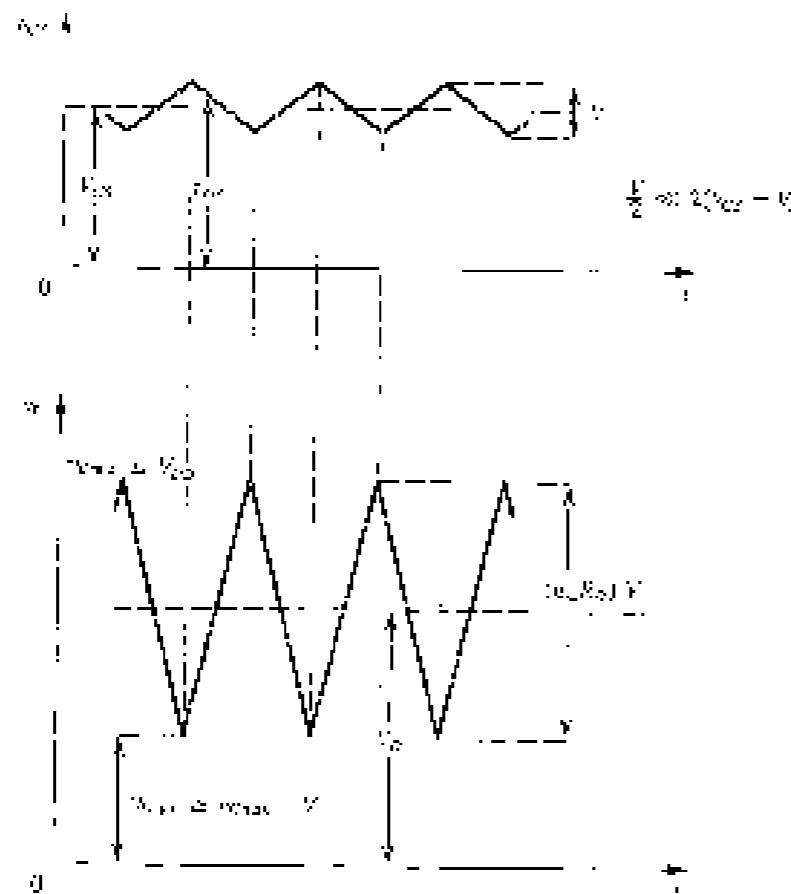
Thus, the signal component of the drain voltage is

$$v_s = -i_s R_D = -g_m v_{in} R_D \quad (4.64)$$

which indicates that the voltage gain is given by

$$A_v = \frac{v_s}{v_{in}} = -g_m R_D \quad (4.65)$$

The minus sign in Eq. (4.65) indicates that the output signal v_s is 180° out of phase with respect to the input signal v_{in} . This is illustrated in Fig. 4.36, which shows v_{in} and v_s . The input signal is assumed to have a triangular wave form with an amplitude much smaller than $2(V_{GS0} - V_0)$, the small-signal condition in Eq. (4.58), to ensure linear operation. For operation in the saturation region in all times, the minimum value of v_{in} should not fall below the corresponding value of v_{in} by more than V_0 . Also, the maximum value of v_{in} should be

FIGURE 4.36 Total instantaneous voltage v_D and gate-to-drain voltage v_{GS} in Fig. 4.32.

smaller than V_{GS1} ; otherwise the FET will enter the cut-off region and the peaks of the output signal waveform will be clipped off.

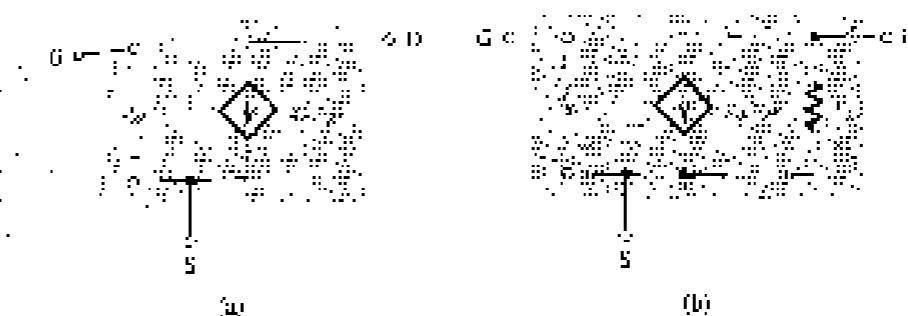
Finally, we note that by substituting for g_m from Eq. (4.61) the voltage gain expression in Eq. (4.67) becomes identical to that derived in Section 4.4—namely, Eq. (4.46).

4.6.4 Separating the DC Analysis and the Signal Analysis

From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current i_{D0} plus the signal component, the total drain voltage $v_D = V_D + v_d$, and so on. It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations. That is, once a steady-state operating point has been established and all dc variables calculated, we may then perform signal analysis ignoring dc quantities.

4.6.5 Small-Signal Equivalent-Circuit Models

From a signal point of view the FET behaves as a voltage-controlled current source. It accepts a signal v_{GS} between gate and source and provides a current $g_m v_{GS}$ at the drain terminal. The input resistance of this controlled source is very high—ideally, infinite. The output resistance—that is, the resistance looking in at the drain—is also high, and we have assumed

FIGURE 4.37 Small-signal models for the MOSFET: (a) neglecting the dependence of r_s on r_{ds} in saturation; (b) including the effect of channel-length modulation, modeled by variable resistance $r_s = |V_A|/I_{D0}$.

r_s to be infinite (i.e., r_{ds} is zero). Putting all of this together, we arrive at the circuit in Fig. 4.37(a), which represents the small-signal operation of the MOSFET and is thus a small-signal model or a small-signal equivalent circuit.

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model shown in Fig. 4.37(b). The rest of the circuit remains unchanged except that ideal constant dc voltage sources are replaced by short circuits. This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source. A similar argument applies to constant dc current sources. Equally, the signal current of an ideal constant dc current source will always be zero, and thus no ideal constant dc current source can be required by an open corner in the small-signal equivalent circuit of the amplifier. The circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

The most serious shortcoming of the small-signal model of Fig. 4.37(a) is that it assumes the drain current in saturation is independent of the drain voltage. From our study of the MOSFET characteristics in saturation, we know that the drain current does in fact depend on v_D in a linear manner. Such dependence was modeled by a finite resistance r_s between drain and source, whose value was given by Eq. (4.66) in Section 4.3.3, which we repeat here:

$$r_s = \frac{|V_A|}{I_{D0}} \quad (4.66)$$

where $|V_A| = 1/kL$ is a MOSFET parameter that either is specified or can be measured. It should be recalled that for a given process technology, $|V_A|$ is proportional to the MOSFET channel length. The current I_{D0} is the value of the dc drain current without the channel length included, as taken in account; that is,

$$I_{D0} = \frac{1}{2} k \frac{W}{L} V_{DS0}^2 \quad (4.67)$$

Typically, r_s is in the range of 10 MΩ to 100 MΩ. It follows that the accuracy of the small-signal model can be improved by including r_s in parallel with the controlled source, as shown in Fig. 4.37(b).

It is important to note that the small-signal model parameters r_s and r_{ds} depend on the dc bias point of the MOSFET.

Returning to the amplifier of Fig. 4.34, we find that replacing the MOSFET with a small-signal model of Fig. 4.37(b) results in the voltage gain expression

$$A_{\perp} = \frac{v_0}{\omega_0} = g_0 A(R_0)/r_0 \quad (4.6)$$

This is the State effect. resistance r_1 results in a reduction in the magnitude of the voltage gain.

Although the analysis above is performed on NMOS transistor, the results and equivalent circuit models of Fig. 4.37 apply equally well to PMOS devices, except for using $|V_{DS}|$, V_D , $|V_{GS}|$, and $|V_G|$ and replacing ζ with ξ .

4.6.5 The Transconductance g_m

We shall now take a closer look at the MOSFET transconductance given by Eq. (14.1), which we repeat here as

$$g_{\mu} = k_s^f (W/L) (V_{\mu e} - V_{\tau e}) - k_f^e (W/L) V_{\mu e}, \quad (4.64)$$

This relationship indicates that y_{g} is proportional to the process transconductance parameter, $\mu_n C_o$, and to the V_{DD} scale of the MOS transistors; hence to obtain relatively large output conductance the device must be short and wide. We also observe that for a given device, the transconductance is proportional to the overdrive voltage, $V_{\text{DD}} = V_{\text{DDH}} + V_{\text{DDL}}$, the amount by which the bias voltage V_{DD} exceeds the threshold voltage V_t . Note, however, that increasing y_{g} by biasing the device at a larger V_{DD} has the disadvantage of reducing the allowable voltage signal swing due to V_{DD} .

Another useful expression for ϵ_0 can be obtained by substituting $m_e(E_{\text{kin}} - V_0)$ in Eq. 11.69 by $(2J_0^2/\sqrt{\pi})(W_0^2 D_0)$ (from Eq. 11.53);

$$g_{\mu\nu} = \frac{e^2 k^2}{4\pi G} \sqrt{\eta} \sqrt{1 - \frac{2M}{r}} \delta_{\mu\nu}$$

The expression also shows that

- For a given MOSFET, β , is proportional to the square root of the drain current.
 - At a given bias current, i_d , is proportional to $\sqrt{V_{GS}}$.

In contrast, the transmission curve of the bipolar junction transistor (BJT) studied in Chapter 13 is proportional to the bias current and is independent of the physical size and geometry of the device.

To gain some insight into the values of g_m obtained in MCOS180's consider an inverting circuit device operating at $I_d = 0.5 \text{ mA}$ and having $V_{DD} = 2.5 \mu\text{V}$. Equation (4.36) shows that for $R/L = 1$, $g_m = 0.45 \text{ mS/V}$, whereas a device for which $R/L = 100$ has $g_m = 3.5 \text{ mS/V}$. Consider a BJT operating at a collector current of 0.5 mA , $V_c = 25 \text{ mV}$

Yet another useful expression for g_m in the MOSFET can be obtained by substituting Eq. (3.33) in Eq. (2.69) to get

$$\beta_{\alpha} = \frac{2I_{\alpha}}{V_{\alpha\beta}V_{\gamma\beta}} \approx \frac{2I_{\alpha}}{V_{\alpha\beta}} \quad (4.7)$$

In summary, there are three different relationships for determining y_s —Eqs. (2.69) (4.70), and (4.71)—and there are three design parameters—W/L, V_{DD} , and I_D , any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain operating voltage V_{DD} and at a particular current I_D . The required W/L ratio can then be found and the resulting y_s determined.



Figure 4 shows a discrete-coupling-source MOSFET amplifier with the drain-to-gate voltage V_{DS} being the output signal. The input signal v_i is coupled to the gate via a large capacitor, and feedback is using a resistor. The input signal v_i is coupled to the load resistance R_L via another large capacitor. The output signal at the drain is coupled to the load resistance R_L via a smaller capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistors has $I_D = 1.5 \text{ mA}$, $k = 0.25 \text{ mA/V}^2$, $L = 1 \mu\text{m}$, and $V_{DD} = 50 \text{ V}$. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the small frequencies of interest.

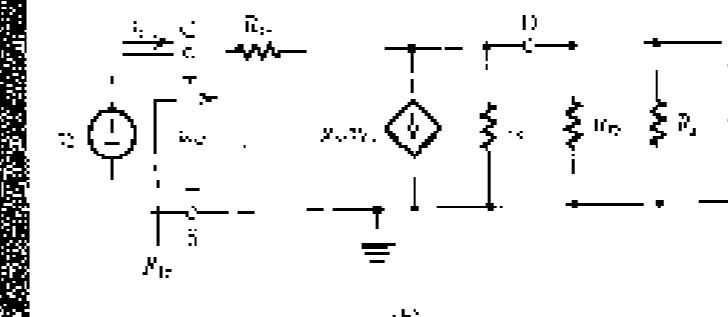
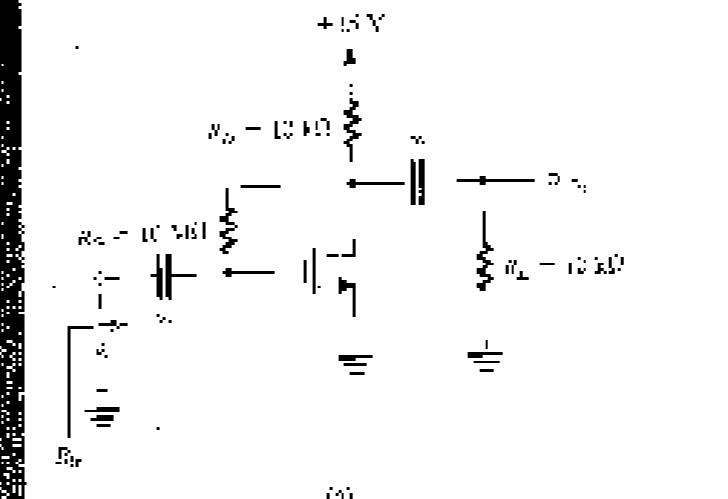


FIGURE 4.20 *Impact of 10% of annual budget on the number of new cases*

Solutions

וְלֹא תַּעֲשֶׂה כֵּן כִּי כֵן יָרַב בְּבָנֶיךָ

$$I_{\text{cr}} = \frac{1}{3} \times (0.28, V_{\text{cr}} = 1.5) \quad . \quad (4.72)$$

where, for simplicity, we have neglected the current length modulation effect. Since the total gate current is zero, there will be no dc voltage drop across R_G , i.e. $V_{GS} = V_g$, which, when substituted in Eq. (17), yields

$$L_0 = 94.6(V_{\odot} - 1.5)^2 \quad (4.73)$$

Also,

$$V_D = 15 - R_D i_D = 15 - 10 i_D \quad (4.74)$$

Solving Eqs. (4.73) and (4.74) together gives

$$I_D = 1.06 \text{ mA} \quad \text{and} \quad V_D = 4.4 \text{ V}$$

(Note that the other solution to the quadratic equation is not physically meaningful.)

The value of i_{DS} is given by

$$\begin{aligned} i_{DS} &= k \frac{W}{L} (V_{GS} - V_T) \\ &= 0.25(4.4 - 1.5) = 0.725 \mu\text{A/V} \end{aligned}$$

The output resistance r_o is given by

$$r_o = \frac{V_D}{I_D} = \frac{15}{1.06} = 13.8 \text{ k}\Omega$$

Figure 4.38(b) shows the small-signal equivalent circuit of the amplifier, where we observe that the coupling capacitors have been replaced with short circuits and the dc supply has been replaced with a short circuit to ground. Since R_S is very large ($10 \text{ M}\Omega$), the current through it can be neglected compared to that of the controlled source $\beta_0 v_{DS}$, enabling us to write for the output voltage

$$v_O = -\beta_0 v_{DS} (R_D / R_o r_o)$$

Since $v_{DS} = 0$, the voltage gain is

$$\begin{aligned} A_v &= \frac{v_O}{v_I} = -\beta_0 (R_D / R_o r_o) \\ &= -0.725(13.8)(10)(10^3) = -1.3 \text{ V/V} \end{aligned}$$

To calculate the input resistance r_{in} , we note that the input current i_I is given by

$$\begin{aligned} i_I &= i_{DS} + v_I / R_S \\ &= \frac{v_I}{R_S} \left[1 - \frac{v_I}{V_T} \right] \\ &= \frac{v_I}{R_S} (1 - 1/0.33) = \frac{4.3 v_I}{R_S} \end{aligned}$$

Thus,

$$r_{in} = \frac{v_I}{i_I} = \frac{R_S}{4.3} = \frac{10}{4.3} = 2.3 \text{ M}\Omega$$

The largest allowable input signal v_I is determined by the need to keep the MOSFET in saturation at all times. That is,

$$v_{GS} \geq V_T = V_T$$

Under this condition, with equality, at the point v_{DS} is maximum and v_{DS} is correspondingly minimum, we write

$$v_{DS,\text{max}} = v_{DS,\text{min}} = V_T$$

$$V_{DS} = A |i_I - v_{GS}| + V_T - V_T$$

$$4.4 = 2.3 i_I - 4.3 + V_T - 1.5$$

which results in

$$i_I = 0.54 \text{ V}$$

Note that in the negative direction, this input signal amplitude results in $v_{DS} = 4.4 - 0.54 = 4.06 \text{ V}$, which is larger than V_T , and thus the transistor remains conducting. Thus, as we have discussed, the limitation on input signal amplitude is posed by the upper-end considerations, and the maximum allowable input signal peak is 0.54 V .

4.6.7 The T Equivalent-Circuit Model

Through a suitable circuit transformation it is possible to develop an alternative equivalent-circuit model for the MOSFET. The development of such a model, known as the T model, is illustrated in Fig. 4.39. Figure 4.39(a) shows the equivalent circuit studied above without r_o . In Fig. 4.39(b) we have added a second drain current source in series with the original controlled source. This addition obviously does not change the terminal currents and is thus allowed. The newly created circuit node, labeled X, is joined to the gate terminal G in Fig. 4.39(c). Observe that the gate current does not change—that is, it remains equal to zero—and thus this connection does not alter the terminal characteristics. We now note that

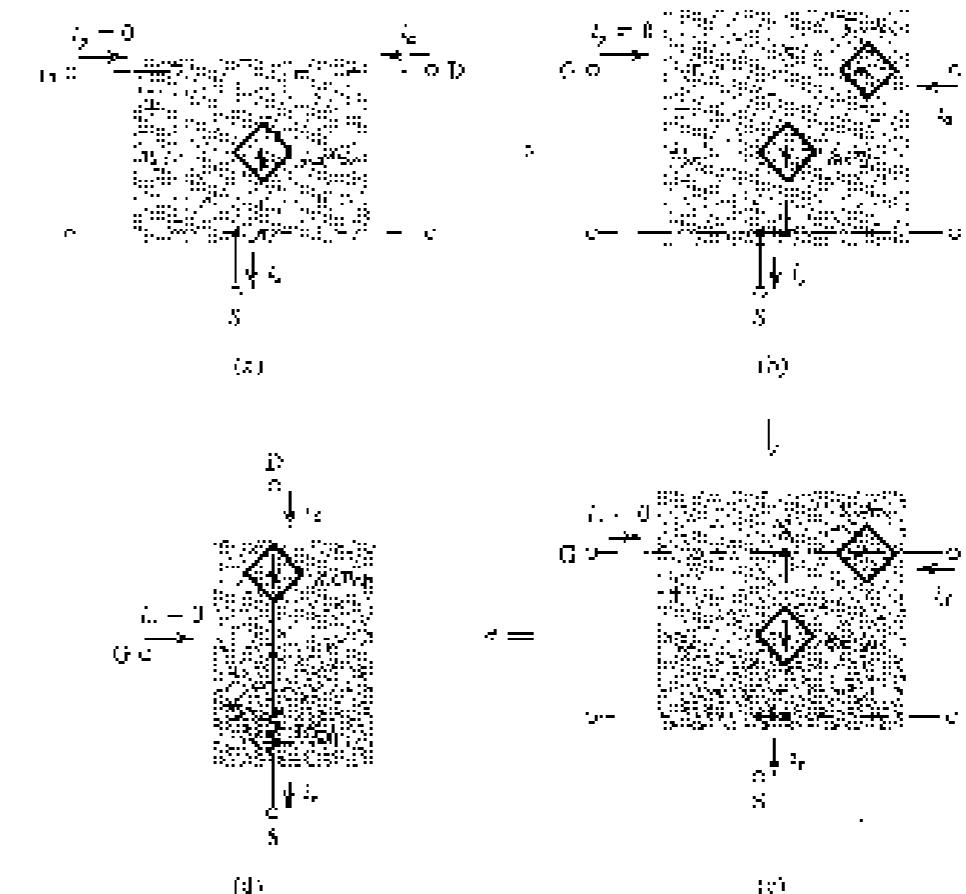


FIGURE 4.39 Development of the T equivalent-circuit model for the MOSFET. The impedance r_o has been omitted but can be added between D and S in the T model of (d).

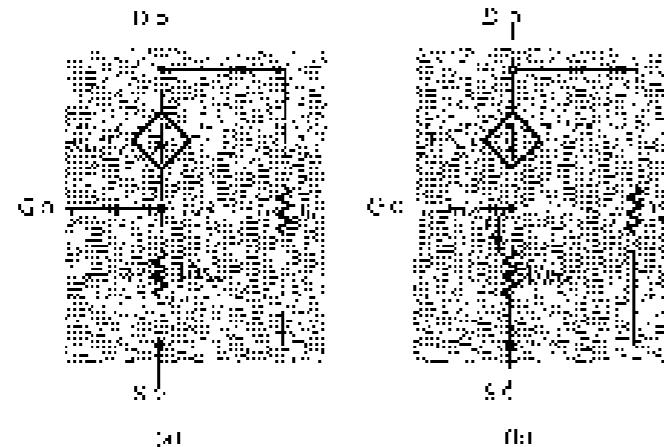


FIGURE 4.40 (a) The T model of the MOSFET augmented with the drain-source resistance r_s . (b) An equivalent representation of the T model.

We have a controlled current source $\beta(v_{DS}, v_g)$ connected across the control voltage v_g . We can recall the controlled source by a resistance as long as this resistance draws an equal current as the source. (See the source absorption theorem in Appendix C.) Thus the value of the resistance is $r_s/\beta(v_{DS}, v_g)$. This replacement is shown in Fig. 4.40(b), which depicts the alternative model. Observe that r_s is still zero, $r_s = \beta(v_{DS}, v_g)$, and $r_s = v_{DS}/\beta(v_{DS}, v_g) = \beta(v_{DS}, v_g)$, all the same as in the original model in Fig. 4.53(a).

The model of Fig. 4.40(b) shows that the resistance between gate and source looking into the source is $1/\beta(v_g)$. This observation, and the T model, prove useful in many applications. Note that the resistance between gate and source, looking into the gate, is infinite.

In developing the T model we did not include r_s . If desired, this can be done by incorporating it in the circuit of Fig. 4.39(d) as a resistance r_s between drain and source, as shown in Fig. 4.40(c). An alternative representation of the T model in which the voltage-controlled current source is replaced with a current-controlled current source is shown in Fig. 4.40(d).

Finally, we should note that in order to distinguish the model in Fig. 4.40(e) from the equivalent T model, the former is sometimes referred to as the hybrid- π model, a carryover from the bipolar transistor literature. The origin of this name will be explained in the next chapter.

4.6.8 Modeling the Body Effect

As mentioned in section 4.2, the body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most-negative power supply in the integrated circuit for n-channel devices and to the most-positive for p-channel devices). Thus the substrate (body) will be at signal ground, but since the source is not a signal voltage v_s , it develops between the body (B) and the source (S). In Section 4.2, it was mentioned that the substrate acts as a "second gate," a backgate for the MOSFET. Thus the signal v_s gives rise to a drain-current component, which we shall write as $\beta_{BS}v_s$, where β_{BS} is the body transconductance, defined as

$$\beta_{BS} = \frac{\partial I_D}{\partial V_{SB}} \Big|_{V_{GS}=V_{DS}=0} \quad (4.75)$$

Recalling that I_D depends on v_{DS} through the dependence of V_{DS} on v_{DS} , Eqs. (4.20), (4.33), and (4.61) can be used to obtain

$$\beta_{BS} = \beta_{DS} \quad (4.76)$$

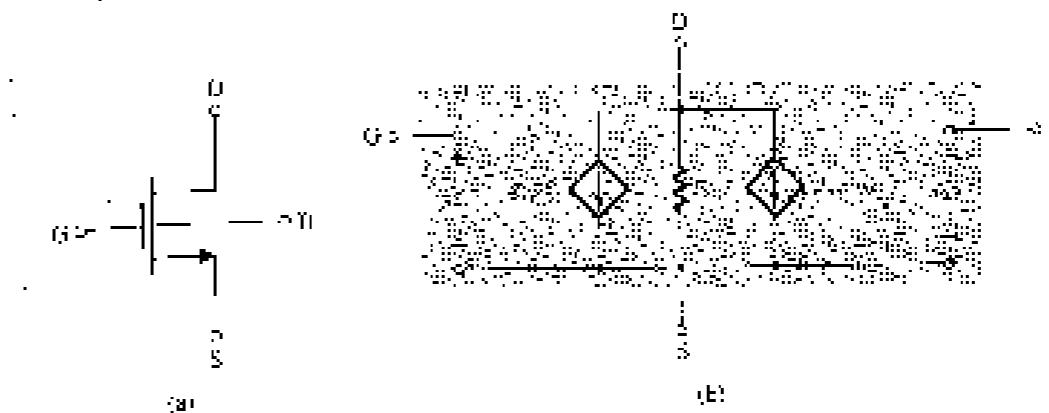


FIGURE 4.41 (a) Small-signal equivalent circuit of a MOSFET (b) which the source is not connected to ground.

where

$$\chi = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{2\beta_0^2 g_m + V_{DS}} \quad (4.77)$$

Typically the value of χ lies in the range 0.1 to 0.5.

Figure 4.41 shows the MOSFET model augmented to include the controlled source $\beta_{BS}v_s$ that models the body effect. This is the model to be used whenever the source is not connected to the substrate.

Finally, although the analysis above was performed on a NMOS transistor, the results and the equivalent circuit of Fig. 4.41 apply equally well to PMOS transistors, except for using [Fig. 4.41(b)] V_{DD} , V_{SS} , V_{GS} , V_{DS} , γ , and β and replacing β_0 with β_p .

4.6.9 Summary

We conclude this section by presenting in Table 4.2 a summary of the formulas for calculating the values of the small-signal MOSFET parameters. Observe that for g_m we have three different formulas, each providing the circuit designer with insight regarding design choices. We shall make frequent references to these in later sections and chapters.

TABLE 4.2 Small-Signal Equivalent-Circuit Models for the MOSFET

Small-Signal Parameters

NMOS Transistor:

a) Transconductance:

$$g_m = \beta_0 \frac{W}{L} V_{GS} = \frac{1}{2} \mu_n C_o \frac{W}{L} \frac{V_{GS}}{V_{DS}} = \frac{2I_D}{V_{DS}}$$

b) Output Conductance:

$$g_{os} = V_{DS}/I_D = 1/\beta_{DS}$$

c) Body Transconductance:

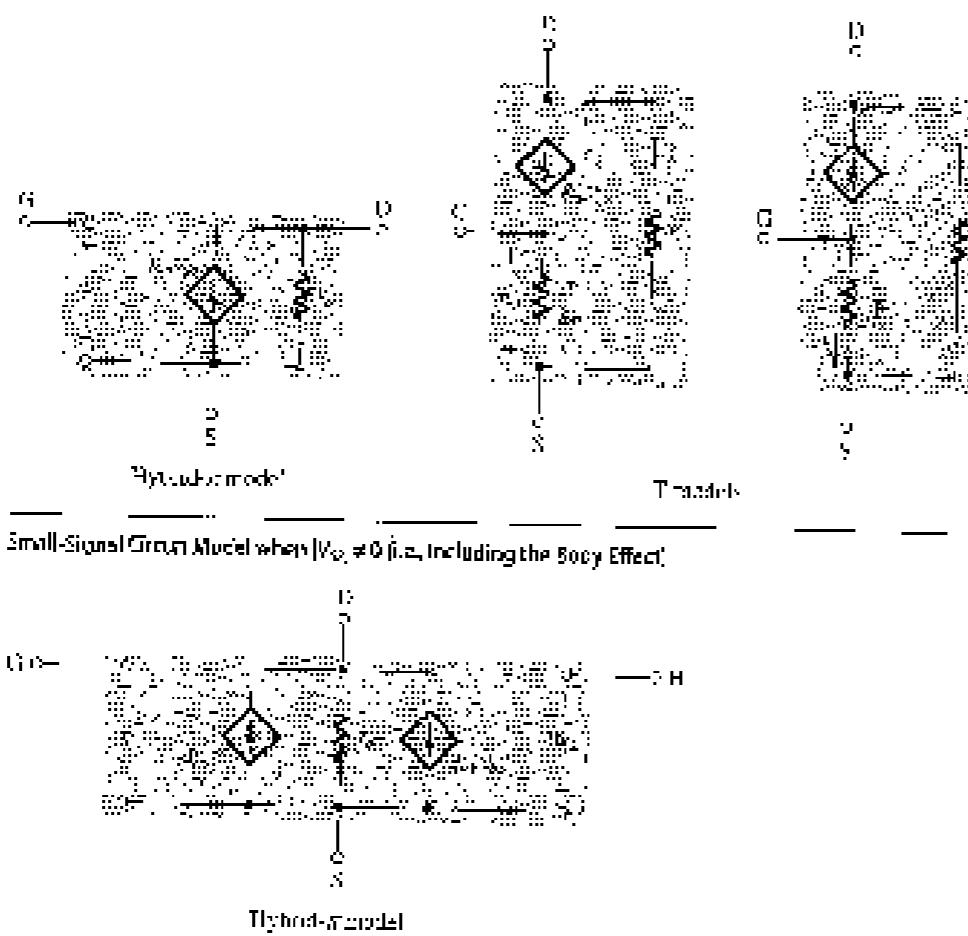
$$\beta_{BS} = \beta_{DS} = \frac{Y}{2\beta_0^2 g_m + V_{DS}} R_o$$

PMOS Transistor:

Same formulas as for NMOS except using [V_{DD} , V_{SS} , V_{GS} , V_{DS} , γ , and β] and replacing β_0 with β_p .

TABLE F-47. EQUATIONS

Small-Signal Equivalent Circuit Models when $V_{DD} = 0$ (i.e., No-Body Model)



EXERCISES

8.24 An NEMO6 transistive has $\mu(C_{ss}) = 0.1 \text{ pA/V}^2$, $k_0 = -4$, $V_t = 1 \text{ V}$, and $V_{DD} = 12 \text{ V}$. Find y_s and a_s when

- 4.26 by a different approach, by writing - *Decompose the state of the grid of a POMDP domain, to get white belief states*, translating so that the two sentences have logically equivalent sense. Explanations will be given in the next section.

19. *Leucosia* *leucostoma* (Fabricius) *leucostoma* (Fabricius)

- ¹⁴ See also M. S. Gitterman, "The Social Construction of Risk," *Journal of Risk Research*, 1998, 1, 1-18.

- 3.26. A PHEWIS cell with $V_{th} = -1$ V, $N_{eff} = 10^{13}$ cm $^{-2}$, and $Q_{cap} = 6 \times 10^{-10}$ C cm $^{-2}$ has $R_{load} = 100$ M Ω . Find I_{load} when the device is biased at $V_{bias} = -1.1$ V, with the value of r_{eff} at 10^{-10} cm 2 is 10^{-4} V $^{-1}$.

- 3.29 The following Table 3-2 is an expression for δ_{eff} in terms of δ_{eff} values which shall be in Chapter 6. This is an adjustment factor based on the statement of the problem. Below are the values.

- وهو ينبع من مفهوم العدالة الاجتماعية الذي يرى أن كل إنسان له حقوق متساوية لا يجوز إغفالها أو إهمالها.

- ANSWER - 215.11100000000002

4.7 SINGLE-STAGE MOS AMPLIFIERS

Having studied MOS amplifier biasing (Section 4.5) and the small-signal operation and models of the MOSFET amplifier (Section 4.6), we are now ready to consider the various configurations utilized in the design of MOS amplifiers. In this section we shall do this for the case of discrete MOS amplifiers, leaving the study of integrated-circuit (IC) MOS amplifiers to Chapter 6. Besides being useful in their own right, discrete MOS amplifiers are somewhat easier to understand than their IC counterparts for two main reasons: The separation between dc and signal quantities is more obvious in discrete circuits, and discrete circuits utilize resistors as circuit load levels. In contrast, as we shall see in Chapter 6, IC MOS amplifiers employ constant current sources as output loads, with these being implemented using additional MOSFETs and resulting in more complicated circuits. Thus the circuits studied in this section should provide us with both an introduction to the subject of MOS amplifier configurations and a solid base on which to continue our study of IC MOS amplifiers in Chapter 6.

Since in cascode circuits the MOSFET source is usually tied to the substrate, the body effect will be absent. Therefore in this section we shall not make the body effect take account. Also, in some circuits we will neglect v_b in order to keep the analysis simple and focus our attention at this early stage on the salient features of the amplifier configurations studied.

4.7.1 The Basic Structure

Figure 4.42 shows the basic circuit we shall utilize to implement the various configurations of discrete-circuit MOS amplifiers. Among the various schemes for biasing discrete MOS

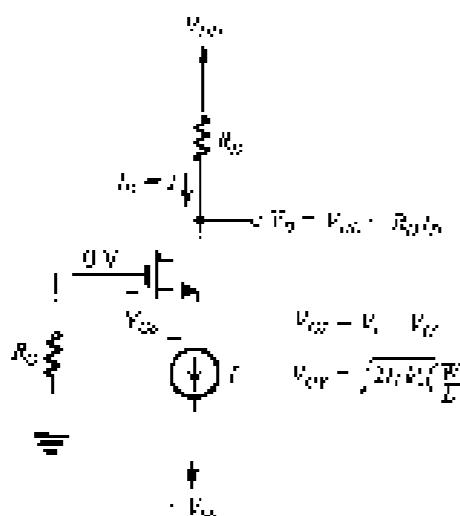


FIGURE 4.42 Basic structure of the circuit used to realize single-stage discrete-signal MOS amplifiers.

duplicators (Section 4.5) we have selected), for both its effectiveness and its simplicity. The one employing constant-current biasing, Figure 4.42 indicates the dc current and the dc voltages resulting of various nodes.

EXERCISE

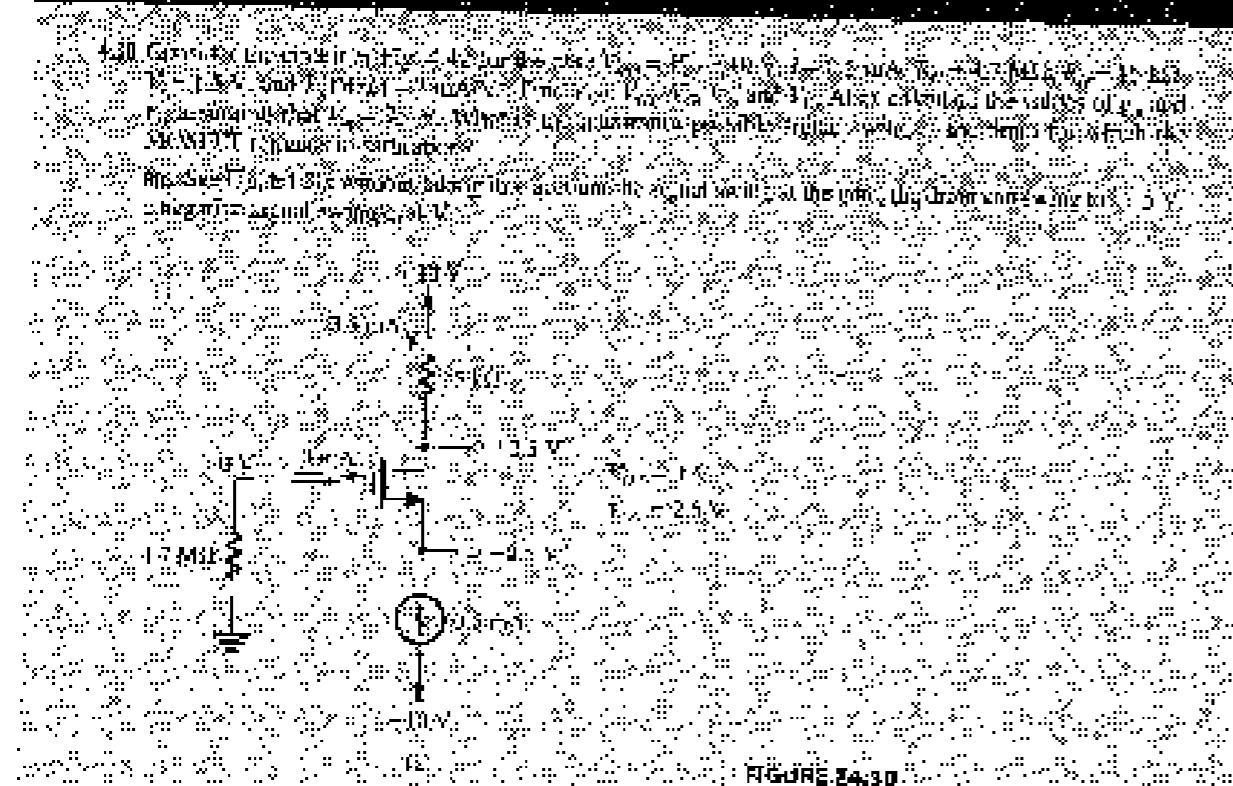


FIGURE 4.43

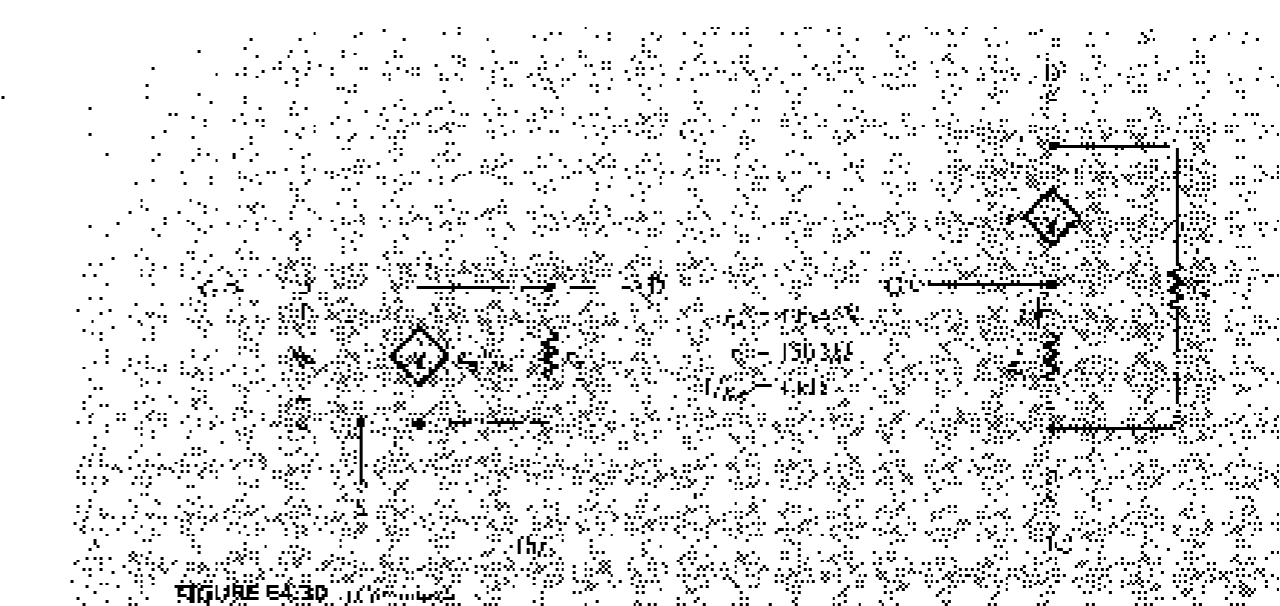


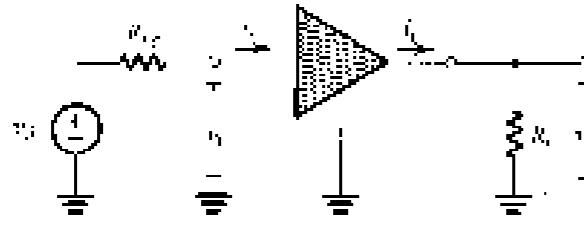
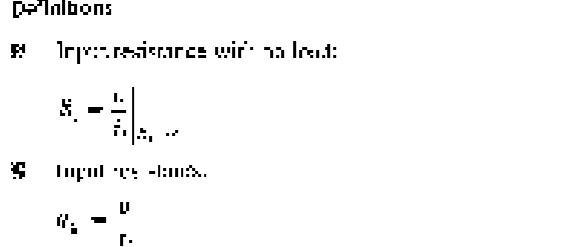
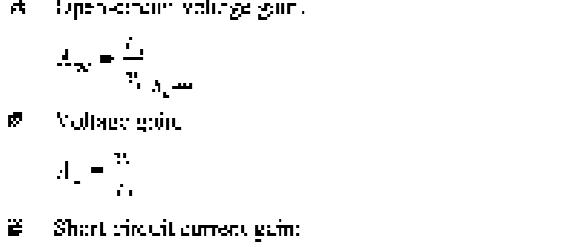
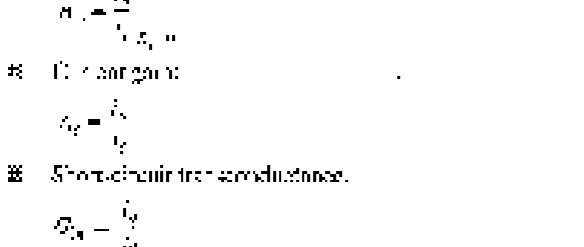
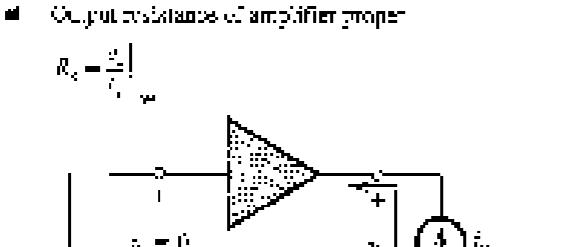
FIGURE 4.43(b)

4.7.2 Characterizing Amplifiers

As we begin our study of MOS amplifier circuits, it is important to know how to characterize the performance of amplifiers as circuit building blocks. An introduction to this subject was presented in Section 1.5. However, the material of Section 1.5 was limited to **unilateral** amplifiers. A number of the amplifier circuits we shall study in this book, though none in this chapter, are not unilateral; that is, they have internal feedback that may cause their input resistance to depend on the load resistance. Similarly, internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier. To accommodate **nonunilateral** amplifiers, we present, in Table 4.1, a general set of parameters and equivalent circuits that we will employ in characterizing and comparing transistors amplifiers. A number of remarks are in order:

- The amplifier is shown fed with a signal source having an open-circuit voltage v_{in} and an internal resistance R_{in} . These can be the parameters of an actual signal source or the Thévenin equivalence of the output circuit of another amplifier stage preceding the one under study in a cascade amplifier. Similarly, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.
- Parameters R_s , R_o , A_{in} , A_{out} , and G_m pertain to the **amplifier proper**; that is, they do not depend on the values of R_{in} and R_L . By contrast, R_{in} , R_{out} , A_{in} , A_{out} , G_m , and C_{in} may depend on one or both of R_{in} and R_L . Also, observe the relationships of related pairs of these parameters; for instance, $R_s = R_{in}|_{v_{in}=0}$ and $R_o = R_{out}|_{v_{in}=0}$.
- As mentioned above, for nonunilateral amplifiers, R_{in} may depend on R_L , and R_{out} may depend on R_{in} . Although none of the amplifiers studied in this chapter are of this type, we shall encounter nonunilateral MOSFET amplifiers in Chapter 6 and beyond. No such dependencies exist for unilateral amplifiers, for which $R_s = R_i$ and $R_{out} = R_o$.
- The **loading** of the amplifier on the signal source is determined by the input resistance R_s . The value of R_s determines the current i_s that the amplifier draws from the signal source. It also determines the proportion of the signal v_{in} that appears at the input of the amplifier proper (i.e., v_i).

TABLE 4.3 Characteristic Parameters of Amplifiers

Circuit	Definitions
	<p>R_i Input resistance with no load:</p> $R_i = \frac{V_g}{I_d} \Big _{R_L \rightarrow \infty}$
	<p>R_o Output resistance:</p> $R_{o\text{av}} = \frac{V_o}{I_d} \Big _{V_g = 0}$
	<p>A_v Open-circuit voltage gain:</p> $A_{v\text{oc}} = \frac{V_o}{V_g} \Big _{R_L \rightarrow \infty}$
	<p>G_v Voltage gain:</p> $A_v = \frac{V_o}{V_g}$
	<p>A_i Short-circuit current gain:</p> $A_i = \frac{I_o}{I_g} \Big _{R_L \rightarrow \infty}$ <p>G_i Current gain:</p> $G_i = \frac{I_o}{I_g}$ <p>G_{is} Short-circuit transconductance:</p> $G_{is} = \frac{I_o}{V_g} \Big _{R_L \rightarrow \infty}$ <p>R_o Output resistance of amplifier proper:</p> $R_o = \frac{V_o}{I_d} \Big _{V_g = 0}$

Equivalent Circuits**A****B****C****Relationships**

$$\frac{V_o}{V_{g\text{oc}}} = \frac{R_o}{R_o + R_{L\text{oc}}}$$

$$G_v = \frac{R_o}{R_o + R_{L\text{oc}}} A_{v\text{oc}} \frac{R_o}{R_o + R_{L\text{oc}}}$$

$$A_i = A_{v\text{oc}} \frac{R_o}{R_o + R_{L\text{oc}}}$$

$$G_{is} = \frac{R_o}{R_o + R_{L\text{oc}}} A_{v\text{oc}}$$

$$A_{v\text{oc}} = G_{is} R_o$$

$$G_{is} = G_{is} + \frac{R_o}{R_o + R_{L\text{oc}}}$$

5. When evaluating the gain A_v from the open-circuit value $A_{v\text{oc}}$, R_o is the output resistance to $V_{g\text{oc}}$. This is because $A_{v\text{oc}}$ is based on feeding the amplifier with an ideal voltage signal V_g . This should be evident from Equivalent Circuit A in Table 4.3. On the other hand, if we are evaluating the overall voltage gain G_v from its open-circuit value $G_{v\text{oc}}$, the output resistance is now $R_o + R_{L\text{oc}}$. This is because G_v is based on feeding the amplifier with V_g , which has an internal resistance $R_{L\text{oc}}$. This should be evident from Equivalent Circuit C in Table 4.3.

6. We urge the reader to carefully examine and reflect on the definitions and the relationships presented in Table 4.3. Example 4.1 should help in this regard.

A transistor amplifier is fed with a signal source having an open-circuit voltage $v_{in} = 10 \text{ mV}$ and an internal resistance R_{in} of $100 \text{ k}\Omega$. The voltage v_i at the amplifier input, and the output voltage v_o , are measured both without load and with a load resistance $R_L = 10 \text{ k}\Omega$ connected to the amplifier output. The measured results are as follows:

	v_i (mV)	v_o (mV)
With $R_L = 0$	0	10
With $R_L = 10 \text{ k}\Omega$	8	9.6

Find all the amplifier parameters.

Solution

First, we use the data obtained for $R_L = 0$ to determine

$$A_{in} = \frac{v_i}{v_{in}} = 10 \text{ mV/V}$$

and

$$G_{in} = \frac{R_i}{100} = 8 \text{ mV/V}$$

Now, since

$$G_{in} = \frac{R_i}{R_i + R_{in}} A_{in}$$

$$8 = \frac{R_i}{R_i + 100} \times 10$$

which gives

$$R_i = 900 \text{ k}\Omega$$

Next, we use the data obtained when $R_L = 10 \text{ k}\Omega$ is connected to the amplifier output to determine

$$A_{in} = \frac{v_i}{v_{in}} = 8.75 \text{ mV/V}$$

and

$$G_{in} = \frac{70}{10} = 7 \text{ mV/V}$$

The values of A_{in} and G_{in} can be used to determine R_{in} as follows:

$$A_{in} = A_{in} \frac{R_i}{R_i + R_{in}}$$

$$8.75 = 10 \frac{10}{10 + R_{in}}$$

which gives

$$R_{in} = 1.73 \text{ k}\Omega$$

Similarly, we use the values of G_{in} and G_{out} to determine R_{out} from

$$G_{out} = G_{out} \frac{R_o}{R_o + R_{out}}$$

$$7 = 8 \frac{10}{10 + R_{out}}$$

resulting in

$$R_{out} = 1.86 \text{ k}\Omega$$

The value of R_s can be determined from

$$\frac{R_s}{R_{in}} = \frac{R_i}{R_i + R_{in}}$$

Thus,

$$10 = \frac{R_i}{R_i + 900}$$

which yields

$$R_s = 400 \text{ k}\Omega$$

The short-circuit transconductance G_A can be found as follows:

$$G_A = \frac{A_{in}}{R_s} = \frac{10}{400} = 2 \text{ mA/V}$$

and the current gain A_v can be determined as follows:

$$A_v = \frac{v_o / R_L}{v_i / R_{in}} = \frac{v_o R_{in}}{v_i R_L}$$

$$= A_{in} \frac{R_{in}}{R_L} = 8.75 \times \frac{400}{10} = 350 \text{ A/A}$$

Finally, we determine the short-circuit current gain A_{in} as follows. From equivalent circuit A in Table 4.3, the short-circuit output current is

$$i_{os} = A_{in} v_i / R_L$$

Now, equating the two expressions for i_{os} and substituting for G_{in} , we

$$G_{in} = \frac{R_i}{R_i + R_{in}} A_{in}$$

and the value of

$$v_i = v_{in} \frac{R_{in} + R_{in} R_{in}}{R_{in} + R_{in} + R_{in}} A_{in}$$

results in

$$R_{in} |_{v_{in}=0} = R_{in} / \left[\left(1 + \frac{R_{in}}{R_i} \right) \cdot \frac{R_{in}}{R_{in} + R_{in}} \right] = 1.73 \text{ k}\Omega$$

We now can use

$$i_{os} = A_{in} k_b R_{in} |_{v_{in}=0} / R_L$$

to obtain

$$A_{in} = \frac{i_{os}}{k_b R_{in} |_{v_{in}=0} / R_L} = 1 \times 8.75 / (1.73 \times 10^3) = 572 \text{ A/A}$$

EXERCISE

- (A) In Example 4.11, R_{ds} is doubled. Find the values for R_s , C_s , and R_{out} . (b) Repeat for $V_{GS} = -0.5$ V, $I_D = 10$ mA, $R_{DS} = 100$ k Ω . (c) Repeat for both R_s and A_V doubled.

4.7.3 The Common-Source (CS) Amplifier

The common-source (CS) or grounded-source configuration is the most widely used of all MOSFET amplifiers circuits. A common-source amplifier realized using the circuit of Fig. 4.42 is shown in Fig. 4.43(a). Observe that to establish a signal ground, or true ground as it is sometimes called, at the source, we have connected a large capacitor, C_S , between the source and ground. This capacitor, usually in the μ F range, is required to provide a very small impedance (ideally, zero impedance; i.e., an effect short circuit) at all signal frequencies of interest. In this way, the signal current passes through C_S to ground and does bypasses the output resistance of current source I (and any other circuit component that might be connected to the MOSFET source). Hence, C_S is called a bypass capacitor. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 4.9. For our purposes here we shall assume that C_S is acting as a perfect short circuit and thus is establishing zero signal voltage at the MOSFET source.

In order not to disturb the dc bias current and voltages, the signal to be amplified, shown as voltage source v_{sd} with an internal resistance R_{sd} , is connected to the gate through a large capacitor C_{gs} . Capacitor C_{gs} , known as a coupling capacitor, is required to act as a perfect short circuit at all signal frequencies of interest, while blocking dc. Here again, we note that as the signal frequency is lowered, the impedance of C_{gs} (i.e., $1/(j\omega C_{gs})$) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. This problem too will be considered in Section 4.9 when the dependence of the amplifier operation on frequency is studied. For our purposes here we shall assume C_{gs} is acting as a perfect short circuit as far as the signal is concerned. Before leaving C_{gs} , we should point out that in situations where the signal source can provide an appropriate dc path to ground, the gate can be connected directly to the signal source and both R_{sd} and C_{gs} can be dispensed with.

The voltage signal resulting at the drain is coupled to the load resistance R_L via another coupling capacitor C_{gd} . We shall assume that C_{gd} acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage is $v_o = v_d$. Note that R_L can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 5.)

To determine the terminal characteristics of the CS amplifier—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its small-signal model. The resulting circuit is shown in Fig. 4.43(b). At the outset we observe that the amplifier is unilateral. Therefore R_{in} does not depend on R_L , and thus $R_{in} \gg R_L$. Also, R_{out} will not depend on R_{sd} , and thus $R_{out} \gg R_L$. Analysis of this circuit is straightforward and proceeds in a step-by-step manner from the signal source to the amplifier load. At the input,

$$i_s = 0 \quad (4.78)$$

$$R_{in} = R_S \quad (4.79)$$

$$v_o = v_{sd} \frac{R_L}{R_S + R_{sd}} = v_{sd} \frac{R_L}{R_S + R_{in}} \quad (4.80)$$

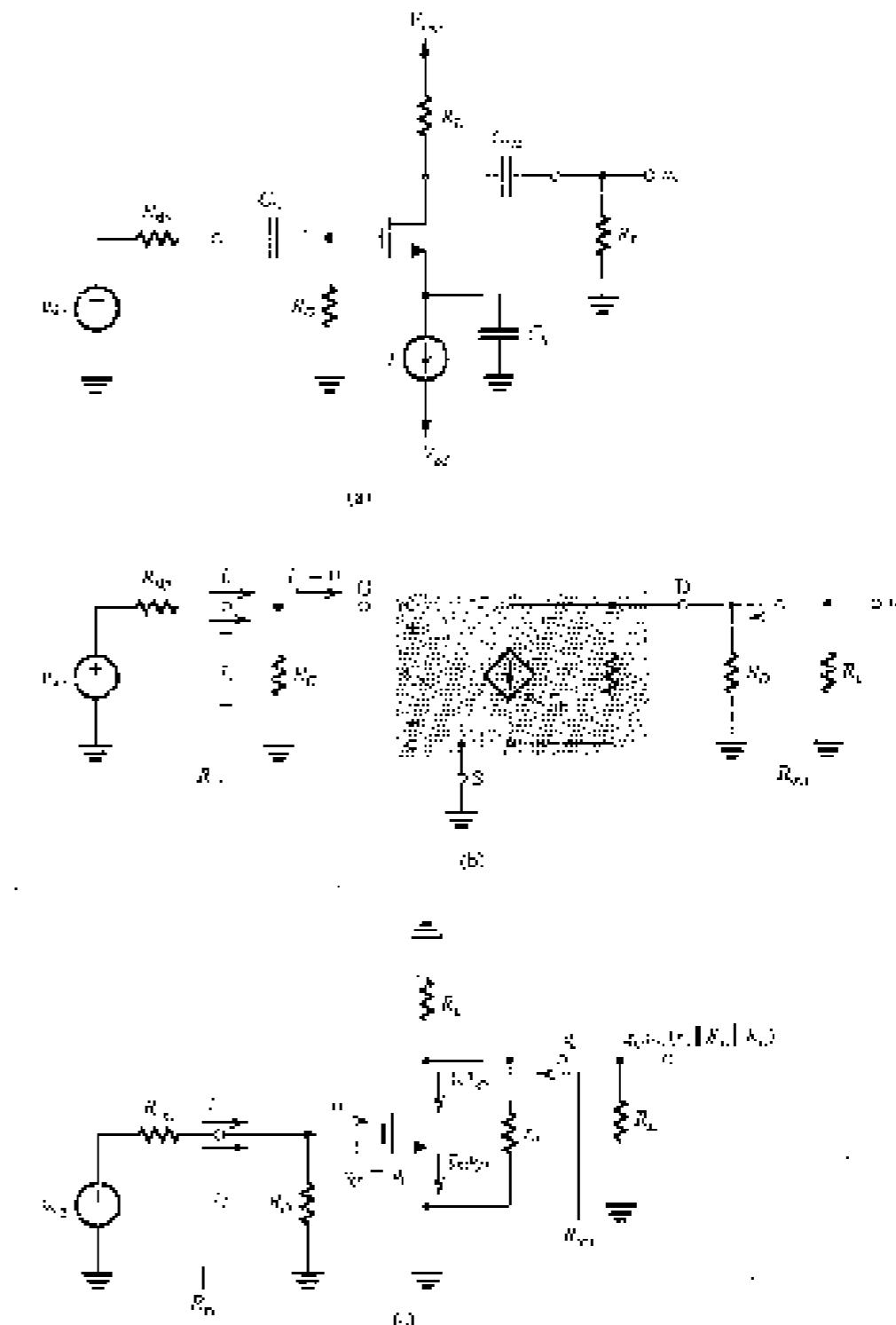


FIGURE 4.43 (a) Common-source amplifier based on the circuit of Fig. 4.42. (b) Small-signal model of the amplifier for low signal amplitudes so that signal analysis is performed directly on the amplifier circuit with the MOSFET model implicitly utilized.

Usually R_D is selected very large (e.g., in the 2MΩ range) with the result that in many applications $R_D \gg R_{DS}$ and

$$r_o \equiv r_{DS}$$

Now

$$r_{DS} = r_o$$

and

$$v_o = -g_m v_{DS}(r_o \parallel R_D \parallel R_L)$$

Thus the voltage gain A_{vo} is

$$A_{vo} = -g_m(r_o \parallel R_D \parallel R_L) \quad (4.80)$$

and the open-circuit voltage gain A_{oc} is

$$A_{oc} = -g_m(r_o + R_D) \quad (4.81)$$

The overall voltage gain from the signal-source to the load will be

$$\begin{aligned} G_v &= \frac{R_{DS}}{R_{DS} + R_{DS}} \\ &= -\frac{R_{DS}}{R_{DS} + R_{DS}} g_m(r_o + R_D + R_L) \end{aligned} \quad (4.82)$$

Finally, to determine the amplifier output resistance R_{out} , we set v_{DS} to 0; that is, we replace the signal generator v_{DS} with a short circuit and look back into the output terminal, as indicated in Fig. 4.43. The result can be found by inspection as

$$R_{out} = r_o \parallel R_L \quad (4.83)$$

As we have seen, including the output resistance r_o in the analysis of the CS amplifier is straightforward. Since r_o appears between drain and source, its effect appears in parallel with R_D . Since it is usually the case that $r_o \gg R_D$, the effect of r_o will be a slight decrease in the voltage gain and a decrease in R_{out} , the latter being a beneficial effect!

Although small-signal equivalent circuit models provide a systematic process for the analysis of any amplifier circuit, the effort involved in drawing the equivalent circuit is not always justified. That is, in simple situations and after a lot of practice, one can perform the small-signal analysis directly on the original circuit. In such a situation, the small-signal MOSFET model is employed implicitly rather than explicitly. In order to get the reader started in this direction, we show in Fig. 4.44(a) the small-signal analysis of the CS amplifier performed on a somewhat simplified version of the circuit. We urge the reader to examine this analysis and to compare it with the analysis using the equivalent circuit of Fig. 4.43(b).

EXERCISE

Consider a CS amplifier based on the circuit contained in Figure 4.40. Specifically, refer to the results of that analysis in Figure 4.40(c). Let $V_{GS} = 0.7$ V, $V_{DS} = 15$ V, and $R_D = 15$ kΩ with r_o taken into account. For the same input voltage pulse as in the previous problem, calculate v_{DS} with r_o taken into account. For the same input voltage pulse as in the previous problem, calculate v_{DS} without r_o taken into account. For the same input voltage pulse as in the previous problem, calculate v_{DS} with r_o neglected. Assume $k_n = 4.7$ MΩ, $A_{DS} = -145$ V/V, and $R_L = 15$ kΩ with r_o taken into account. Calculate the peak-to-peak output voltage v_{DS} for each case.

We conclude our study of the CS amplifier by noting that it has a very high input resistance, a moderately high voltage gain, and a relatively high output resistance.

4.7.4 The Common-Source Amplifier with a Source Resistance

It is often beneficial to insert a resistance R_S in the source lead of the common-source amplifier, as shown in Fig. 4.44(a). The corresponding small-signal equivalent circuit is shown in

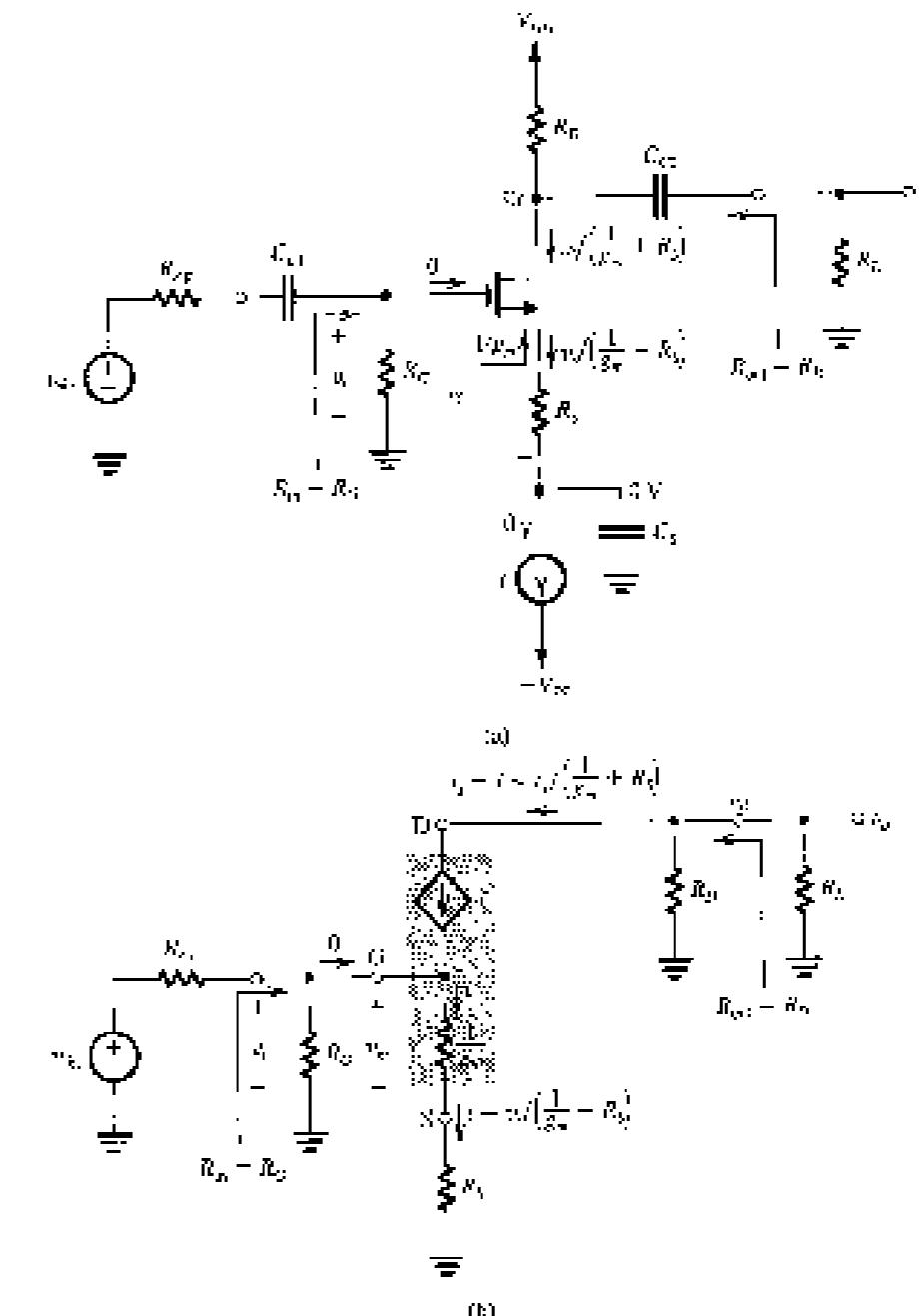


FIGURE 4.44 (a) Common-source amplifier with a resistance R_S in the source lead. (b) Small-signal equivalent circuit of (a), neglecting R_S .

Fig. 4.44(b) where we note that the trapezoid has been replaced by its T equivalent-circuit model. The T model is used in preference to the π model because it makes the analysis in this case somewhat simpler. In general, whenever a resistance is connected in the source lead, as for instance in the source-follower circuit we shall consider shortly, the T model is preferred. The source resistance then simply appears in series with the resistance $1/g_m$, which represents the resistance between source and gate, looking into the source.

It should be noted that we have not included r_o in the equivalent-circuit model. Including r_o would complicate the analysis considerably; r_o would connect the output node of the amplifier to the input side and this would make the amplifier noninverting. Fortunately, it turns out that the effect of r_o on the operation of this source-circuit amplifier is not important. This can be verified using SPICE simulation (Section 4.2). This is not the case, however, for the integrated-circuit version of the circuit where r_o plays a major role and must be taken into account in the analysis and design of the circuit which we shall do in Chapter 6.

From Fig. 4.44(b) we see that as in the case of the CS amplifier,

$$R_{in} = R_s + R_2 \quad (4.84)$$

and thus,

$$v_{in} = v_i - \frac{R_2}{g_m R_s + R_2} \quad (4.85)$$

Unlike the CS circuit, however, here v_{in} is only a fraction of v_i . It can be determined from the voltage divider composed of $1/g_m$ and R_2 that appears across the amplifier input as follows:

$$v_{in} = v_i \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_2} = v_i \frac{1}{1 + g_m R_2} \quad (4.86)$$

Thus we can use the value of R_2 to control the magnitude of the signal v_{in} and thus ensure that v_{in} does not become too large and cause unacceptable high nonlinear distortion. (Recall the constraint on v_{in} given by Eq. 4.59.) This is the first benefit of including resistor R_2 . Other benefits will be encountered in later sections and chapters. For instance, we will show by SPICE simulation in Section 4.2 that R_2 causes the useful bandwidth of the amplifier to be extended. The mechanism by which R_2 causes such improvements in amplifier performance is that of negative feedback. Unfortunately, the price paid for these improvements is reduction in voltage gain, as we shall now show.

The current i_d is equal to the current flowing in the source lead; thus

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_2} = \frac{A_{in} v_i}{1 + g_m R_2} \quad (4.87)$$

Thus including R_2 reduces i_d by the factor $(1 + g_m R_2)$, which is hardly surprising since this is the factor relating v_{in} to v_i and the MOSFET produces $i_d = g_m v_{in}$. Equation (4.87) indicates also that the effect of R_2 can be thought of as reducing the effective g_m by the factor $(1 + g_m R_2)$.

The output voltage can now be found from

$$\begin{aligned} v_o &= -i_d (R_D + R_L) \\ &= -\frac{g_m R_D + R_L}{1 + g_m R_2} A_{in} v_i \end{aligned}$$

thus the voltage gain is

$$A_{in} = -\frac{g_m (R_D + R_L)}{1 + g_m R_2} \quad (4.88)$$

and setting $R_L = \infty$ gives

$$A_{in} = -\frac{g_m R_D}{1 + g_m R_2} \quad (4.89)$$

The overall voltage gain G_v is

$$G_v = -\frac{R_D + R_L}{R_D + R_{in} + 1 + g_m R_2} \quad (4.90)$$

Comparing Eqs. (4.88), (4.89), and (4.90) with their counterparts without R_2 indicates that including R_2 results in a gain reduction by the factor $(1 + g_m R_2)$. In Chapter 8 we shall study negative feedback in some detail. There we will learn that this factor is called the amount of feedback and that it determines both the magnitude of performance improvements and, as a trade-off, the reduction in gain. At this point, we should recall that in Section 1.5 we saw that a resistor R_2 in the source lead improves stability; that is, R_2 reduces the variability in I_D . The action of R_2 that reduces the variability of I_D is exactly the same action we are employing here, R_2 in the circuit of Fig. 4.44 in reducing i_d , which is, after all, just a variation in I_D . Because of its action in reducing the gain, R_2 is called source degeneration resistance.

Another useful interpretation of the gain expression in Eq. (4.88) is that the gain reduction is simply the ratio of the total resistance in the drain, $(R_D + R_L)$, to the total resistance to the source, $(1 + g_m R_2 + R_2)$.

Finally, we wish to direct the reader's attention to the small-signal analysis that is performed and indicated directly on the circuit in Fig. 4.44(a). Again, with some practice, the reader should be able to dispense, in simple situations, with the extra work involved in drawing a complete equivalent-circuit model and use the MOSFET model implicitly. This also has the added advantage of providing greater insight regarding circuit operation and, furthermore, reduces the probability of making manipulation errors in circuit analysis.

EXERCISE

- 4.44.1. For each of the two configurations shown in Fig. 4.44, draw the small-signal equivalent circuit and determine the voltage gain G_v as a function of the drain load R_D , the source resistance R_2 , and the input voltage v_i . Assume that the drain voltage is constant at V_D and that the source voltage is zero. Assume that the MOSFET is operating in saturation. Neglect the effect of the drain load on the drain current.

4.55 The Common-Gate (CG) Amplifier

By connecting a signal source or the MOSFET gate terminal, a certain configuration, usually named common-gate (CG) or grounded-gate amplifier is obtained. The input signal is applied to the source, and the output is taken at the drain, with the gate forming a

common terminal between the input and output ports. Figure 4.45(a) shows a CGF configuration based on the circuit of Fig. 4.42. Observe that since both the drain and gate voltages at the source are to be zero, we have connected the gate directly to ground, thus eliminating resistor R_g . Also here, coupling capacitors C_{11} and C_{22} perform similar functions to those in the CS circuit.

The small-signal equivalent circuit model of the CGF amplifier is shown in Fig. 4.45(b). Since resistor R_{ds0} appears directly in series with the MOSFET source lead, we have selected the T model for the transisted CGF model; of course, can be used and yields identical

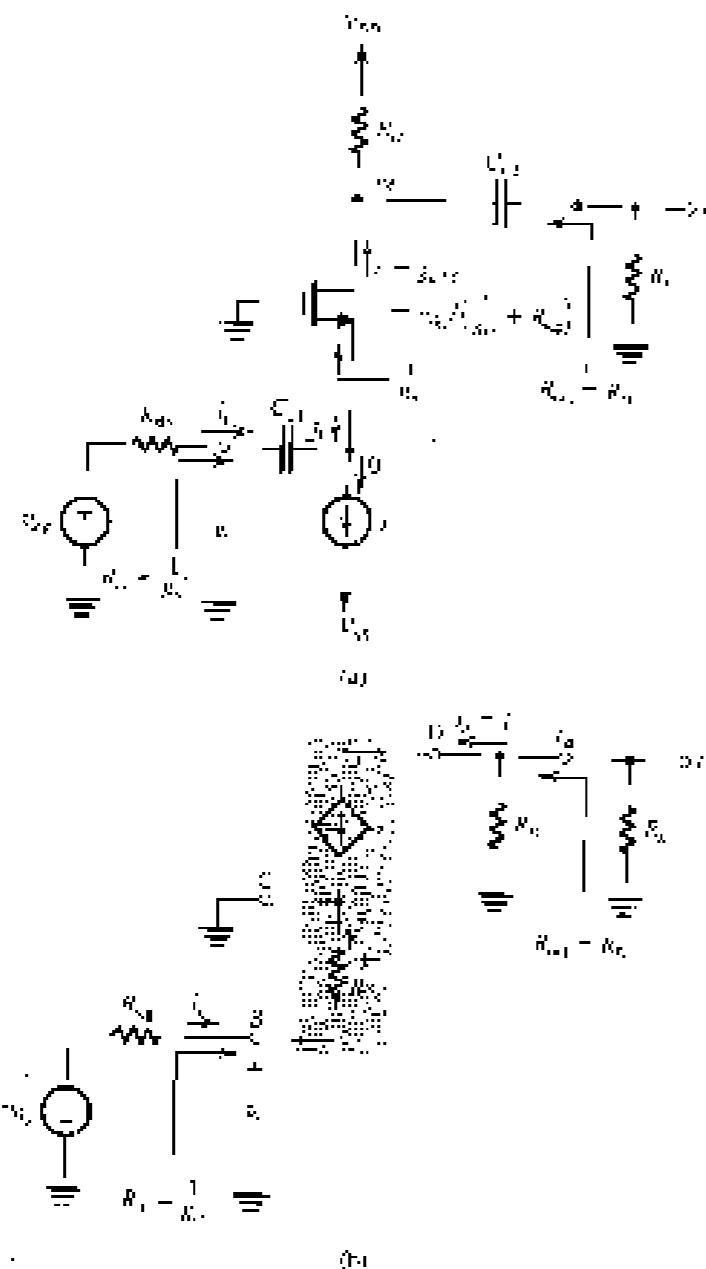


FIGURE 4.45 (a) A common-gate amplifier based on the circuit of Fig. 4.42. (b) A small-signal equivalent circuit of the amplifier in (a).

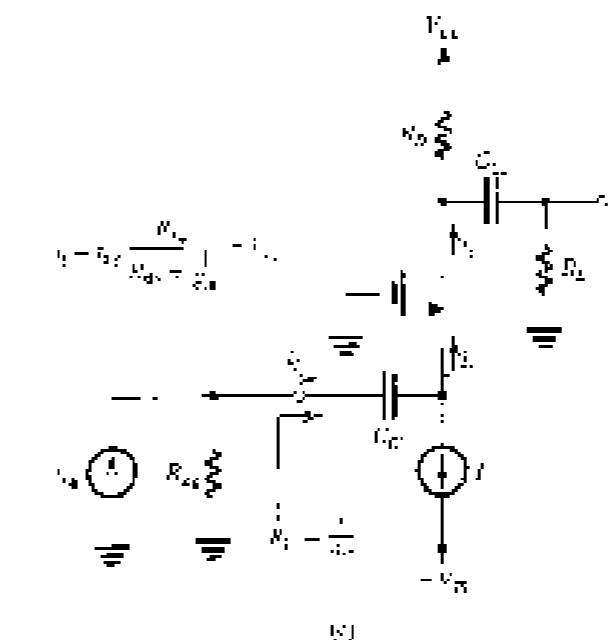


FIGURE 4.46 (a) The common-source amplifier with negative feedback.

result; however, the T model is more convenient in this case. Observe also that we have not included r_s . Including r_s here would complicate the analysis considerably, for it would appear between the output and input of the amplifier. We will consider the effect of r_s when we study the IC form of the CG amplifier in Chapter 6.

From inspection of the equivalent circuit model in Fig. 4.45(b) we see that the input resistance is

$$R_{in} = \frac{1}{g_m} \approx \frac{1}{g_m} \quad (4.91)$$

This should have been expected since we are looking in to the source terminal of the MOSFET and the gate is grounded.¹ Furthermore, since the circuit is unilateral, R_{in} is independent of R_d and R_s ($R_s = R_d$). Since g_m is of the order of 1 mA/V , the input resistance of the CG amplifier can be relatively low (of the order of $1 \text{ k}\Omega$) and certainly much lower than in the case of the CS amplifier. It follows that significant loss of signal strength can occur in connecting the signal to the input of the CG amplifier.

$$v_i = v_{in} \frac{R_s}{R_{in}} \frac{R_d}{R_{ds0}} \quad (4.92)$$

Thus,

$$\beta_i = \beta v_i = \frac{\beta v_{in}}{\frac{R_s}{R_{in}} \frac{R_d}{R_{ds0}}} = \frac{v_{in}}{1 + g_m R_{ds0}} \quad (4.93)$$

¹ As we will see in Chapter 6, when this is not the case, R_{in} depends on R_s and R_d and can be quite different from $1/g_m$.

from which we see that to keep the loss in signal strength small, the source resistance R_{sr} should be small.

$$R_{\text{sr}} \ll \frac{1}{g_m}$$

The current i_s is given by

$$i_s = \frac{v_i}{R_{\text{in}}} = \frac{v_{\text{in}}}{1/g_m} = g_m v_i$$

and the drain current i_d is

$$i_d = i_s + i_b = g_m v_i$$

Thus the output voltage can be found as

$$v_o = v_d = -i_d (R_2 \parallel R_3) = g_m (R_2 \parallel R_3) v_i$$

resulting in the voltage gain

$$A_v = g_m (R_2 \parallel R_3) \quad (4.94)$$

from which the open-circuit voltage gain can be found as

$$A_{\text{oc}} = g_m R_2 \quad (4.95)$$

The overall voltage gain can be obtained as follows:

$$G_v = \frac{R_3}{R_{\text{in}} + R_{\text{sr}}} A_{\text{oc}} = \frac{R_3}{1 + g_m R_{\text{sr}}} A_{\text{oc}} = \frac{A_{\text{oc}}}{1 + g_m R_{\text{sr}}} \quad (4.96a)$$

resulting in

$$G_v = \frac{g_m (R_2 \parallel R_3)}{1 + g_m R_{\text{sr}}} \quad (4.96b)$$

Finally, the output resistance is found by inspection to be

$$R_{\text{out}} = R_3 \approx R_2 \quad (4.97)$$

Comparing these expressions with those for the common-source amplifier we make the following observations:

1. Unlike the CS amplifier, which is inverting, the CG amplifier is noninverting. This, however, is seldom a significant consideration.
2. While the CS amplifier has a very high input resistance, the input resistance of the CG amplifier is low.
3. While the A_{oc} values of both CS and CG amplifiers are nearly identical, the overall voltage gain of the CG amplifier is smaller by the factor $1 + g_m R_{\text{sr}}$ (Eq. 4.96b), which is due to the low input resistance of the CG circuit.

The observations above do not show any particular advantage for the CG circuit; to explore this circuit further we take a closer look at its operation. Figure 4.45(c) shows the CG amplifier fed with a signal current-source i_{in} having an internal resistance R_{in} . This can, of course, be the Norton equivalent of the signal source used in Fig. 4.45(a). Now, using

$R_{\text{in}} = 1/g_m$ and the current-divider rule we can find the fraction of i_{in} that flows into the MOSFET source, i_s ,

$$i_s = i_{\text{in}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sr}}} = i_{\text{in}} \frac{R_{\text{in}}}{R_{\text{sr}} + \frac{1}{g_m}} \quad (4.98)$$

Normally, $R_{\text{sr}} \ll 1/g_m$, and

$$i_s \approx i_{\text{in}} \quad (4.98a)$$

Thus we see that the circuit presents a relatively low input resistance, $1/g_m$, to the input signal current source, resulting in very little signal-current attenuation at the input. The MOSFET then reproduces this current, in the drain, as well as a much higher output resistance. The circuit thus acts in effect as a unity-gain current amplifier or a current follower. This view of the operation of the common-gate amplifier has resulted in its most popular application, in a configuration known as the emITTER circuit, which we shall study in Chapter 6.

Another area of application of the CG amplifier makes use of its superior high-frequency performance, as compared to that of the CS stage (Section 4.6). We shall study wide-band amplifier circuits in Chapter 6. Here we should note that the low input-resistance of the CG amplifier can be an advantage in some very-high-frequency applications where the input signal connection can be thought of as a transmission line and the $1/g_m$ input resistance of the CG amplifier can be made to function as the termination resistance of the transmission line (see Problem 4.36).

EXERCISE

- 4.34 Consider a CG stage fed with the signal of Fig. 4.42(b). If the load is a short circuit, determine the output voltage v_o if $i_{\text{in}} = 10 \mu\text{A}$, $R_{\text{in}} = 10 \text{ k}\Omega$, $R_1 = 10 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_3 = 10 \text{ k}\Omega$, $R_{\text{sr}} = 10 \text{ M}\Omega$, $R_{\text{dr}} = 10 \text{ M}\Omega$, $V_{\text{DD}} = 10 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 10 \text{ V}$, $I_{\text{DS}} = 10 \text{ mA}$, $k_n = 10 \text{ mA/V}^2$, $\lambda = 0.05$, $V_t = 1 \text{ V}$, and $\beta_m = 100$.

4.7.6 The Common-Drain or Source-Follower Amplifier

The last single-stage MOSFET amplifier configuration we shall study is that obtained by establishing a signal ground at the drain and using it as a terminal common to the input port between gate and drain, and the output port between source and drain. By analogy to the CS and CG amplifier configurations, this circuit is called common-drain or grounded-drain amplifier. However, it is known more popularly as the source follower, for a reason that will become apparent shortly.

Figure 4.46(a) shows a common-drain amplifier based on the circuit of Fig. 4.42. Since here it is to function as a signal ground, there is no need for resistor R_{sr} , and it has therefore been eliminated. The input signal is coupled via capacitor C_{in} to the MOSFET gate, and the output signal at the MOSFET source is coupled via capacitor C_{out} to a load resistor R_L .

Since R_{in} is in effect connected in series with the source terminal of the transistor (current source i_{in} is an open circuit as far as signals are concerned), it is more convenient to use the MOSFET's T model. The resulting small-signal equivalent circuit of the common-drain

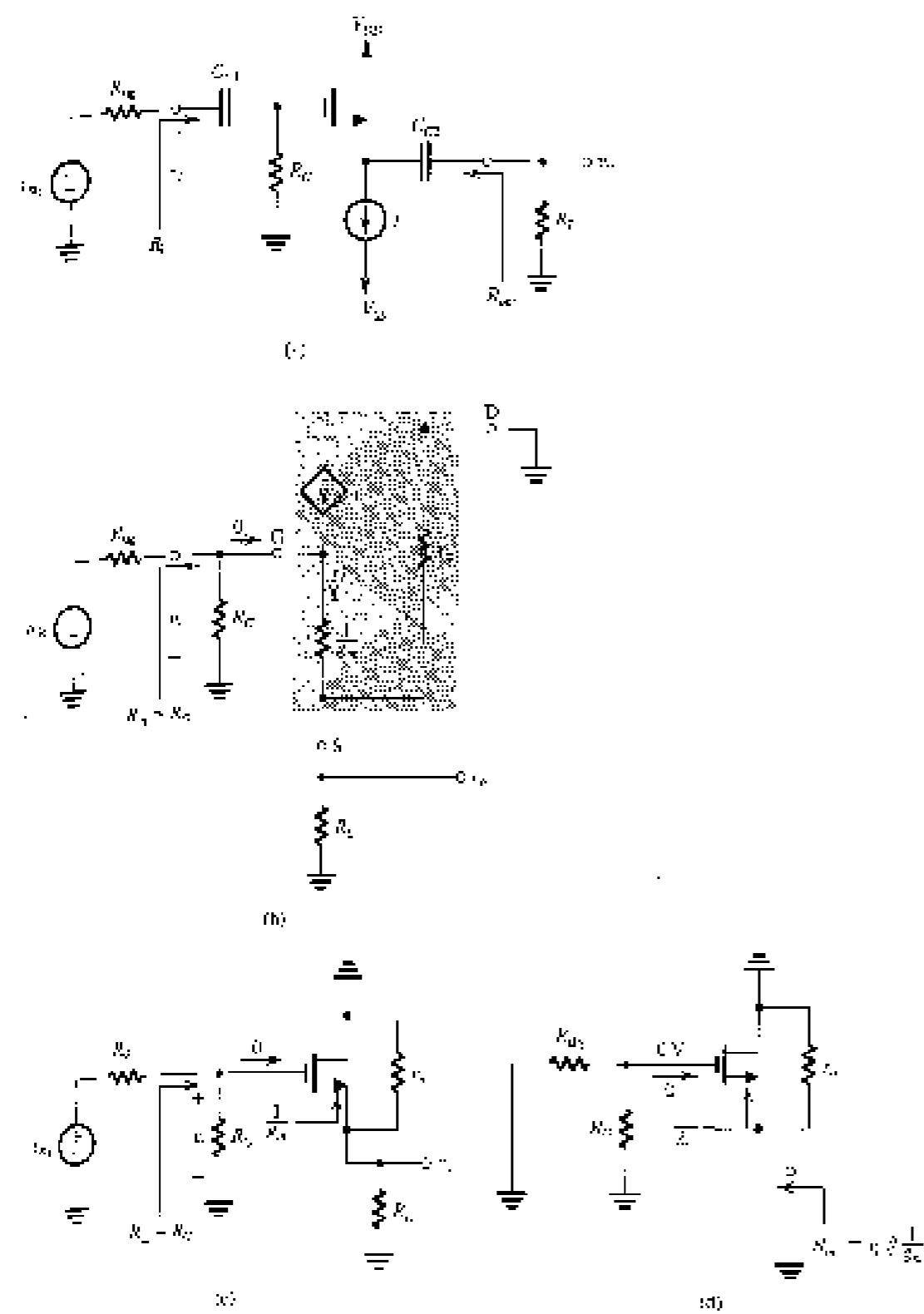


FIGURE 4.46 (a) A common drain or source-follower amplifier. (b) Small-signal equivalent-circuit model for small-signal analysis plotted directly on the circuit. (c) Current biasing circuit. (d) Input resistance R_{IN} of the source follower.

amplifier > above in Fig. 4.46(b), analysis of this circuit is straightforward and proceeds as follows: The output resistance R_{out} is given by

$$R_{out} = R_2 \quad (4.99)$$

Thus,

$$v_o = v_{in} \frac{R_1}{R_1 + R_{in}} = v_{in} \frac{R_1}{R_1 + R_{in}} \quad (4.100)$$

Usually R_1 is selected to be much larger than R_{in} , with the result that

$$v_o \approx v_{in}$$

To proceed with the analysis, it is important to note that r_s appears in effect in parallel with R_2 , with the result that between the gate and ground we have a resistance $(1/g_m)$ in series with $(R_2 \parallel r_s)$. The signal v_i appears across this total resistance. Thus we may use the voltage divider rule to determine v_g as

$$v_g = v_i \frac{R_1 \parallel r_s}{(R_1 \parallel r_s) + \frac{1}{g_m}} \quad (4.101)$$

From which the voltage gain A_v is obtained as

$$A_v = \frac{R_2 \parallel r_s}{(R_2 \parallel r_s) + \frac{1}{g_m}} \quad (4.102)$$

and the open-circuit voltage gain A_{oc} as

$$A_{oc} = \frac{r_s}{r_s + \frac{1}{g_m}} \quad (4.103)$$

Normally $r_s \gg 1/g_m$, causing the open-circuit voltage gain from gate to source, A_{oc} , in Eq. (4.103), to become nearly unity. Thus the voltage at the source follows that at the gate, giving the circuit its popular name of source follower. Also, in many discrete-circuit applications, $r_s \gg R_2$, which enables Eq. (4.102) to be approximated by

$$A_v \approx \frac{R_2}{R_2 + \frac{1}{g_m}} \quad (4.102a)$$

The overall voltage gain G can be found by combining Eqs. (4.100) and (4.102a), with the result that

$$G = \frac{R_2}{R_1 + R_{in}} \frac{R_1 \parallel r_s}{(R_1 \parallel r_s) + \frac{1}{g_m}} \quad (4.104)$$

which approaches unity for $R_1 \gg R_{in}$, $r_s \gg 1/g_m$, and $r_s \gg R_2$.

To emphasize the fact that it is usually easier to perform the small-signal analysis directly on the circuit diagram with the MOSFET small-signal model utilized only implicitly, we show such an analysis in Fig. 4.16(c). Once again, to separate the intrinsic action of the MOSFET from the early effect, we have extracted the output resistance r_o and shown it separately.

The circuit for determining the output resistance R_{out} is shown in Fig. 4.46(d). Because the gate voltage is now zero, looking back into the source we see between the source and ground a resistance $1/g_m$, or parallel with r_o ; thus,

$$R_{\text{out}} = \frac{1}{g_m} \parallel r_o \quad (4.105)$$

Normally, $r_o \gg 1/g_m$, reducing R_{out} to

$$R_{\text{out}} = \frac{1}{g_m} \quad (4.106)$$

which indicates that R_{out} will be moderately low.

We observe that although the source-follower circuit has a large amount of internal feedback (as we will find out in Chapter 8), its R_{out} is independent of R_s (and thus $R_s = R_{\text{in}}$) and its R_{out} is independent of R_{load} (and thus $R_{\text{load}} = R_{\text{out}}$). The reason for this, however, is the zero gate current.

In conclusion, the source follower features a very high input resistance, a relatively low output resistance, and a voltage gain that is less than but close to unity. It finds application in situations in which we need to connect a voltage-signal source that is providing a signal of reasonable magnitude but has a very high internal resistance to a much smaller load resistance—that is, as a unity-gain voltage buffer amplifier. The need for such amplifiers was discussed in Section 4.5. The source follower is also used as the output stage in a three-stage amplifier, where its function is to equate the overall amplifier with a low output resistance, thus enabling it to supply relatively large load currents without loss of gain (i.e., with little reduction of output signal level.) The design of output stages is studied in Chapter 14.

EXERCISE

- 4.8 Consider a simple full-wavelength channel, 45 nm long, with a drain-to-source voltage of $V_{DS} = -0.5$ V, a drain current of $I_D = 10$ mA, and a drain-to-source resistance of $R_{DS} = 10$ k Ω . The channel width is $W = 10$ μ m. The carrier mobility is $\mu_n = 1500$ cm 2 /V·s and $\mu_p = 400$ cm 2 /V·s. Neglecting the effect of drain-induced barrier lowering, find the drain-to-source voltage gain (A_{DS}) with the immittance method. (Ans.: $A_{DS} = 4.76$ at $V_{GS} = 1$ V; $A_{DS} = 0.047$ at $V_{GS} = -0.98$ V; $A_{DS} = 0.032$ at $V_{GS} = -1.02$ V; their absolute values are identical.)

4.7.7 Summary and Comparisons

For easy reference we present, in Table 4.4, a summary of the characteristics of the various configurations of discrete single-stage MOSFET amplifiers. In addition to the remarks already made throughout this section on the relative merits of the various configurations, the results displayed in Table 4.4 enable us to make the following concluding points:

1. The CS configuration is the best suited for obtaining the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single CS stage or a cascade of two or three CS stages can be used.
2. Including a resistor R_s in the source lead of the CS stage provides a number of improvements in its performance, as will be seen in later chapters, at the expense of reduced gain.

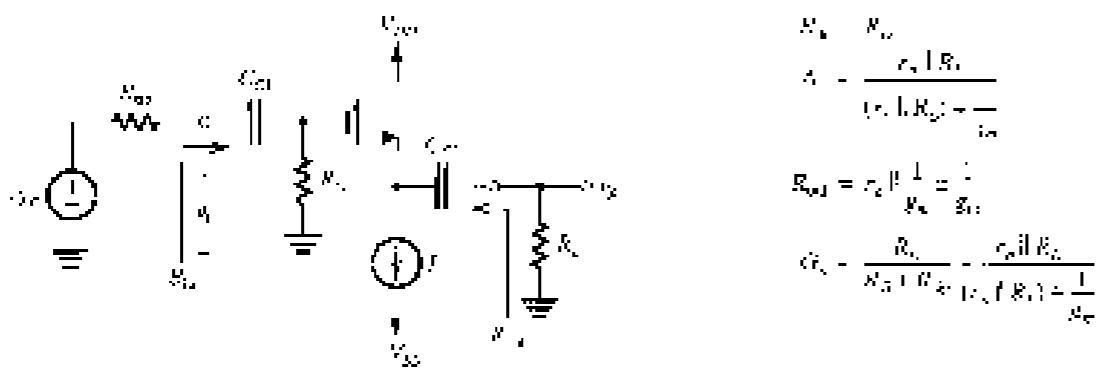
TABLE 4.4 Characteristics of Single-Stage Discrete MOSFET Amplifiers

Common-Source		V_{GS}	V_{DS}	V_{DS}
$k_h = R_s$				
$A_v = g_m (R_s \parallel R_L) / R_s$				
$R_{\text{out}} \approx r_o \parallel R_L$				
$G_o = -\frac{R_s}{R_s + R_{\text{out}}} (k_h + R_s) / R_s$				
Common-Source with Source Resistance		V_{GS}	V_{DS}	V_{DS}
Neglecting r_o :				
$R_s = R_s$				
$A_v = \frac{R_s \parallel R_s}{1 + g_m R_s} = \frac{g_m (R_s + R_s)}{1 + g_m R_s}$				
$R_{\text{out}} = R_s$				
$G_o = \frac{R_s}{R_s + R_{\text{out}}} \frac{g_m (R_s + R_s)}{1 + g_m R_s}$				
$r_o = \frac{1}{1 + g_m R_s}$				
Common-Gate		V_{GS}	V_{DS}	V_{DS}
Neglecting r_o :				
$R_s = \frac{1}{g_m}$				
$A_v = g_m (R_s \parallel R_s)$				
$R_{\text{out}} = R_s$				
$G_o = \frac{1}{1 + g_m R_s} - g_m (R_s + R_s)$				

(Continued)

TABLE 4.4 (Continued) Common-Drain or Source Follower

Common-Drain or Source Follower



$$\begin{aligned} R_{in} &= R_s \\ A_v &= \frac{r_o + R_L}{(r_o + R_L) + \frac{1}{g_m}} \\ R_{out} &= r_o \parallel \frac{1}{g_m} = \frac{1}{g_m} \\ G_v &= \frac{R_L}{R_s + R_L + r_o + \frac{1}{g_m}} = \frac{r_o + R_L}{r_o + R_L + \frac{1}{g_m}} \end{aligned}$$

3. The low input resistance of the CG amplifier makes it useful only in specific applications. These include voltage amplifiers that do not require a high input resistance and that take advantage of the excellent high-frequency performance of the CG configuration (see Chapter 6) and as a unity-gain current amplifier or current follower. This latter application gives rise to the most popular application of the common-gate configuration, the cascode amplifier (see Chapter 6).
4. The source follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multivoltage amplifier.

4.8 THE MOSFET INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

From our study of the physical operation of the MOSFET in Section 4.1, we know that the device has internal capacitances. In fact, we used one of these, the gate-to-channel capacitance, in our derivation of the MOSFET $i-v$ characteristics. We did, however, implicitly assume that the steady-state changes on these capacitances are acquired instantaneously. In other words, we did not account for the finite time required to charge and discharge the various internal capacitances. As a result, the device models we derived, such as the small-signal model, do not include any capacitances. The use of these models would predict constant amplifier gains independent of frequency. We know, however, that this is (unfortunately) not the case; in fact, the gain of every MOSFET amplifier falls off at some high frequency. Similarly, the MOSFET digital logic inverter exhibits a finite non-zero propagation delay. To be able to predict these results, the MOSFET model must be augmented by including internal capacitances. This is the subject of this section.

To visualize the physical origin of the various internal capacitances, the reader is referred to Fig. 4.1. There are basically two types of internal capacitances in the MOSFET:

1. The gate capacitive effect: The gate electrode (polysilicon) forms a parallel-plate capacitor with the channel, with the oxide layer serving as the capacitive dielectric. We discussed the gate (or oxide) capacitance in Section 4.1 and denoted its value per unit area as C_{ox} .

4.8 THE MOSFET INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

2. The source-finite and drain-finite depletion-layer capacitances: These are the capacitances of the reverse-biased pn junctions formed by the n+ source region (also called the source diffusion) and the p-type substrate, and by the n+ drain region (the drain diffusion) and the substrate. Evaluation of these capacitances will utilize the material studied in Chapter 3.

These two capacitive effects can be modeled by including capacitances in the MOSFET model between its four terminals, G, D, S, and D. There will be five capacitances in total, C_{ox} , C_{ds} , C_{gs} , C_{ds} , and C_{gd} , where the subscripts indicate the location of the capacitance in the model. In the following, we show how the values of the five model capacitances can be determined. We will do so by considering each of the two capacitive effects separately.

4.8.1 The Gate Capacitive Effect

The gate capacitive effect can be modeled by the three capacitances C_{ox} , C_{gs} , and C_{gd} . The values of these capacitances can be determined as follows:

1. When the MOSFET is operating in the triode region, at small v_{ds} , the channel will be of uniform depth. The gate-channel capacitance will be $WL C_{ox}$ and can be modeled by dividing it equally between the source and drain ends; thus,

$$C_{gs} = C_{gd} = \frac{1}{2} WL C_{ox} \quad (\text{triode region}) \quad (4.107)$$

This is obviously an approximation (as all modeling is), but works well for triode-region operation, even when v_{ds} is not small.

2. When the MOSFET operates in saturation, the channel has a tapered shape and is pinched off at or near the drain end. It can be shown that the gate-to-channel capacitance in this case is approximately $\frac{1}{2} WL C_{ox}$, and can be modeled by assigning this entire amount to C_{gs} and a zero amount to C_{gd} because the channel is pinched off at the drain; thus,

$$C_{gs} = \frac{1}{2} WL C_{ox} \quad (\text{saturation region}) \quad (4.108)$$

$$C_{gd} = 0 \quad (4.109)$$

3. When the MOSFET is cut off, the channel disappears, and thus $C_{gs} = C_{gd} = 0$. Once again, we can (after some rather complex reasoning) model the gate capacitive effect by assigning a capacitance $WL C_{ox}$ to the gate-only model capacitance; thus,

$$C_{gs} = C_{gd} = 0 \quad (\text{cutoff}) \quad (4.110)$$

$$C_{ox} = WL C_{ox} \quad (4.111)$$

4. There is an additional small capacitive component that should be added to C_{ox} and C_{gs} in all the preceding formulas. This is the capacitance that results from the fact that the source and drain diffusions extend slightly under the gate oxide (refer to Fig. 4.1). If the overlap length is denoted L_{ov} , we see that the overlap-capacitance component is

$$C_{ov} = WL_{ov} C_{ox} \quad (4.112)$$

Typically, $L_{ov} = 0.05$ to 0.1 μ m.

4.8.2 The Junction Capacitances

The depletion-layer capacitances of the two reverse-biased p-n junctions formed between each of the source and the drain diffusions and the body can be determined using the formula developed in Section 3.7.3 (Eq. 3.56). Thus, for the source diffusion, we have the source-body capacitance, C_{sb} ,

$$C_{sb} = \frac{C_{sb0}}{1 + \frac{V_{SB}}{V_0}} \quad (4.113)$$

where C_{sb0} is the value at $V_{SB} = 0$ (no-body-source bias), V_0 is the magnitude of the reverse bias voltage, and V_0 is the junction built-in voltage (0.6 V to 0.8 V). Similarly, for the drain, we have the drain-body capacitance C_{db} ,

$$C_{db} = \frac{C_{db0}}{1 + \frac{V_{DB}}{V_0}} \quad (4.114)$$

where C_{db0} is the capacitance value at very-reverse-bias voltage and V_0 is the magnitude of this reverse bias voltage. Note that we have assumed that for both junctions, the grading coefficient, $m = 3$.

It should be noted also that each of these junction capacitances includes a contribution arising from the bottom side of the diffusion and a component arising from the side walls of the diffusion. In this regard, observe that each diffusion has three side walls that are in contact with the substrate and thus contribute to the junction capacitance (the fourth wall is in contact with the channel). In more advanced MOSFET modeling, the two components of each of the junction capacitances are calculated separately.

The formulas for the junction capacitances in Eqs. (4.113) and (4.114) assume small-signal operation. These formulas, however, can be modified to obtain approximate average values for the capacitances when the transistor is operating under large-signal conditions such as in logic circuits. Finally, typical values for the various capacitances exhibited by an n-channel MOSFET in a relatively modern (0.5 μm) CMOS process are given in the following section.

EXERCISE

Consider a MOSFET with $L = 10 \mu\text{m}$, $W = 10 \mu\text{m}$, $V_T = 0.15 \text{ V}$, $V_{DS} = 0.5 \text{ V}$, $V_{GS} = 0.5 \text{ V}$, and $V_{SB} = -0.5 \text{ V}$. Calculate the four junction capacitances for this device. Assume $C_{sb0} = 100 \text{ fF}$ and $C_{db0} = 200 \text{ fF}$. Use Table 4.1 for the other junction capacitances.

4.8.3 The High-Frequency MOSFET Model

Figure 4.47(a) shows the small-signal model of the MOSFET, including the four source漏出的 C_{sb} , C_{db} , and C_{ds} . This model can be used to predict the high-frequency response of MOSFET amplifiers. It is, however, quite complex for transient analysis, and its use is

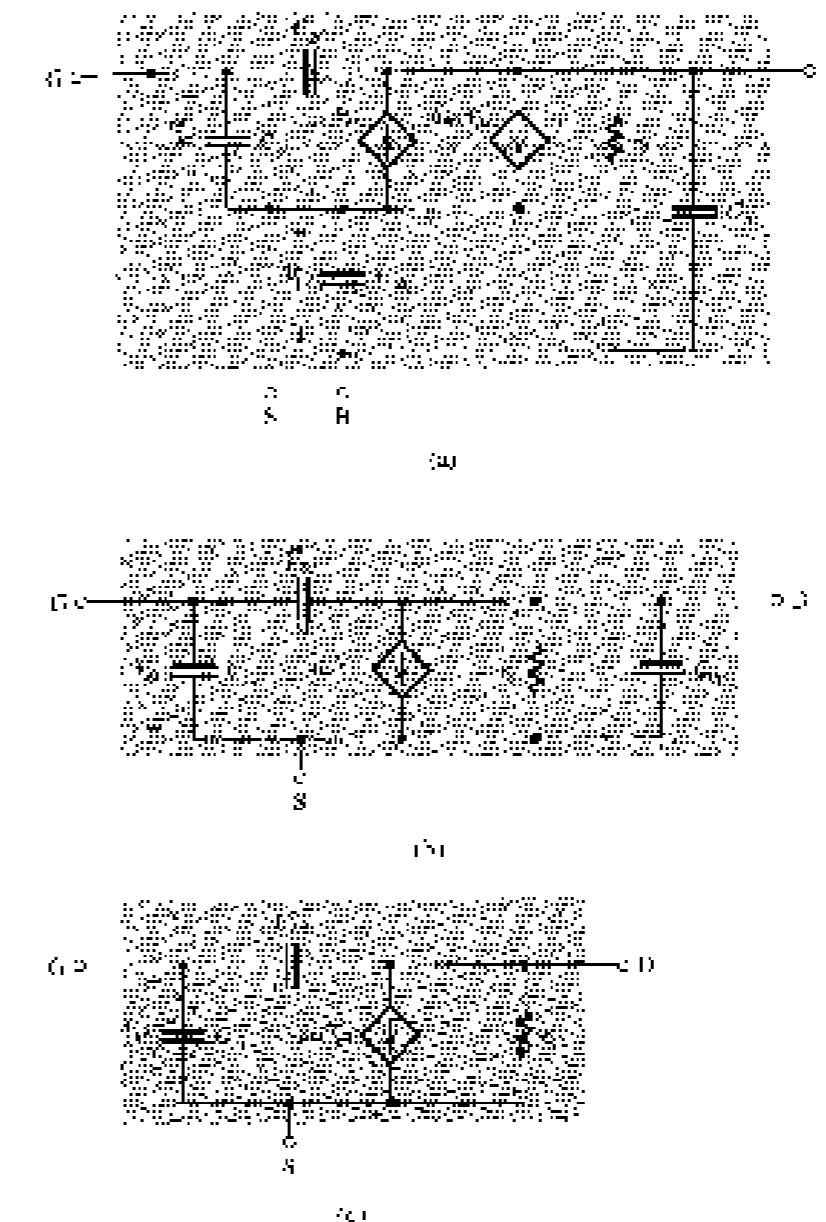
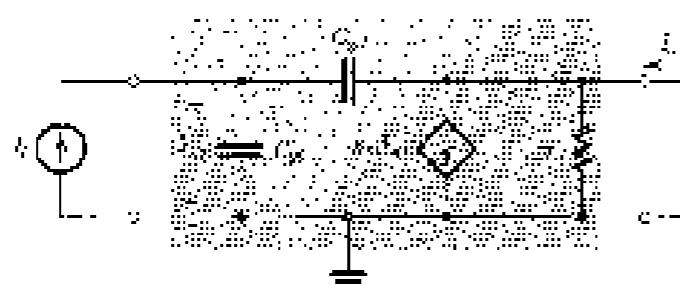


FIGURE 4.47 (a) High-frequency equivalent circuit model of the MOSFET; (b) the equivalent circuit for the case in which the source is connected to the substrate (body); (c) The equivalent circuit for $V_T < V_{SB}$, neglecting bodyinity analysis.

difficult to complete simulation using, for example, SPICE. Fortunately, for the case when the source is connected to the body, the model simplifies considerably, as shown in Fig. 4.47(b). In this model, C_{db} , although small, plays a significant role in determining the high-frequency response of amplifiers (Section 4.9) and thus must be kept in the model. Capacitor C_{db} , on the other hand, can usually be neglected, resulting in significant simplification of transient analysis. The resulting circuit is shown in Fig. 4.47(c).

FIGURE 4.48 Determining the short-circuit current gain $I_s > I_d$.

4.8.4 The MOSFET Unity-Gain Frequency (f_T)

A figure of merit for the high-frequency operation of the MOSFET as an amplifier is the unity-gain frequency, f_T . This is defined as the frequency at which the short-circuit current gain of the common-source configuration becomes unity. Figure 4.48 shows the MOSFET hybrid model with the source as the common terminal between the input and output ports. To determine the short-circuit current gain, the input is fed with a current source signal I_s and the output terminals are short-circuited.⁸ It is easy to see that the current in the short circuit is given by

$$I_s = g_m V_{gs} - \omega C_{gs} V_{ds}$$

Recalling that C_{gs} is small, at the frequencies of interest, the second term in this equation can be neglected,

$$I_s = g_m V_{gs} \quad (4.115)$$

From Fig. 4.48, we can express V_{gs} in terms of the input current I_s as

$$V_{gs} = I_s / (C_{gs} + C_{ds}) \quad (4.116)$$

Equations (4.115) and (4.116) can be combined to obtain the short-circuit current gain:

$$\frac{I_s}{I_d} = \frac{g_m}{g_m (C_{gs} + C_{ds})} \quad (4.117)$$

For physical frequencies $\omega = \omega_0$, it can be seen that the magnitude of the current gain decreases with the frequency.

$$\omega_0 = g_m / (C_{gs} + C_{ds})$$

Thus the unity-gain frequency $f_T = \omega_0 / 2\pi$ is

$$f_T = \frac{\omega_0}{2\pi(C_{gs} + C_{ds})} \quad (4.118)$$

Since f_T is proportional to g_m and inversely proportional to the FET internal capacitances, the higher the value of f_T , the more effective the FET becomes as an amplifier. Substituting for g_m using Eq. (4.106), we can express f_T in terms of the drain current I_D (see Problem 4.92).

⁸Note that since we are now dealing with quantitative circuits, in these notes the are fractions of frequency, or equivalently, i.e., square root values, we are using capital letters with lowercase subscripts for circuit symbols. This continues the symbol notation introduced in Chapter 1.

Alternatively, we can substitute for g_m from Eq. (4.69) to express f_T in terms of the overdrive voltage V_{OP} (see Problem 4.93). Both expressions yield additional insight into the high-frequency operation of the MOSFET.

Typically, f_T ranges from about 100 MHz for the older technologies (e.g., a 5-μm CMOS process) to many GHz for newer high-speed technologies (e.g., a 0.13-μm CMOS process).

TABLE 4.4	
Model	Small-signal model
Symbol	
Equation	$I_D = \frac{W}{L} \cdot \frac{V_{DS}}{2} \cdot \left(1 + \frac{V_{GS}}{V_{TH}} \right)^2$
Capacitances	$C_{GS} = \frac{W}{L} \cdot \frac{V_{DS}}{2} \cdot \frac{1}{1 + \frac{V_{GS}}{V_{TH}}} \cdot \frac{1}{C_{ox}}$ $C_{GD} = \frac{W}{L} \cdot \frac{V_{DS}}{2} \cdot \frac{1}{1 + \frac{V_{GS}}{V_{TH}}} \cdot \frac{1}{C_{ox}}$ $C_{DS} = \frac{W}{L} \cdot \frac{V_{DS}}{2} \cdot \frac{1}{1 + \frac{V_{GS}}{V_{TH}}} \cdot \frac{1}{C_{ox}}$
Frequency	$f_T = \frac{1}{2\pi(C_{GS} + C_{DS})}$

4.8.5 Summary

We conclude this section by presenting a summary in Table 4.5.

TABLE 4.5 The MOSFET High-Frequency Model

Model

Model Parameters

$$\begin{aligned}
 g_m &= \mu_n C_{ox} \frac{W}{L} V_{DS} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} I_D - \frac{2 I_D}{V_{DS}} & L_{eff} &= \frac{L_{real}}{1 + \frac{V_{DS}}{V_{TH}}} \\
 r_o &= Z_{DS} = \frac{V_{DS}}{2 \sqrt{\mu_n C_{ox} \frac{W}{L} I_D}} & C_{gd} &= \frac{C_{ox}}{1 + \frac{V_{DS}}{V_{TH}}} \\
 r_s &= V_{DS} I_D & C_{ds} &= \frac{C_{ox}}{1 + \frac{V_{DS}}{V_{TH}}} \\
 C_{gs} &= \frac{W}{L} V_{DS} C_{ox} + W I_D C_{ox} & f_T &= \frac{2 \pi}{2 \pi(C_{GS} + C_{DS})}
 \end{aligned}$$

4.9 FREQUENCY RESPONSE OF THE CS AMPLIFIER⁸

In this section we study the dependence of the gain of the MOSFET common-source amplifier of Fig. 4.49(a) on the frequency of the input signal. Before we begin, however, a note of terminology is in order: Since we will be dealing with voltages and currents that are functions of frequency or, more generally, the complex frequency variable ω , we will use superscript letters with lowercase subscripts to represent them (e.g., V_{in} , V_{out} , I_{in} , I_{out}).

4.9.1 The Three Frequency Bands

When the circuit of Fig. 4.49(a) was studied in Section 4.7.3, it was assumed that the coupling capacitors C_{in} and C_{out} and the bypass capacitor C_b were acting as perfect short circuits at all signal frequencies of interest. We also neglected the internal capacitances of the MOSFET, that is, C_{gs} and C_{gd} of the MOSFET high-frequency model shown in Fig. 4.7(c), were assumed to be sufficiently small to act as open circuits at all signal frequencies of interest. As a result of ignoring all capacitive effects, the gain expressions derived in Section 4.7.3 were independent of frequency. In reality, however, this situation applies over only a limited, though normally wide, band of frequencies. This is illustrated in Fig. 4.49(b), which shows a sketch of the magnitude of the overall voltage gain, G_v , of the CS amplifier versus frequency. We observe that the gain is almost constant over a wide frequency band, called the midband. The value of the midband gain A_0 corresponds to the overall voltage gain G_v that was derived in Section 4.7.2, namely,

$$A_0 = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_o}{R_{\text{in}} + R_{\text{ds}}} g_{\text{m}}(r_s \parallel R_{\text{in}} \parallel R_o) \quad (4.118)$$

Figure 4.49(b) shows that the gain falls off at signal frequencies below and above the midband. The gain fall-off in the low-frequency band is due to the fact that even though C_{in} , C_{out} , and C_b are large capacitors (in the nF range), as the signal frequency is reduced, their impedances increase, and they no longer behave as short circuits. On the other hand, the gain falls off in the high-frequency band as a result of C_{gs} and C_{gd} , which though very small for the pF or fraction of pF range of discrete devices are much lower for IC devices; their impedances at high frequencies decrease and thus can no longer be considered as open circuits. It is our objective in this section to study the mechanisms by which these two sets of capacitances affect the amplifier gain in the low-frequency and the high-frequency bands. In this way, we will be able to determine the frequencies f_L and f_H , which define the extent of the midband, as shown in Fig. 4.49(c).

The midband is obviously the useful frequency band of the amplifier. Usually, f_L and f_H are the frequencies at which the gain drops by 3 dB below its value at midband. The amplifier bandwidth or 3-dB bandwidth is defined as the difference between the lower (f_L) and the upper or higher (50% 3-dB) frequencies:

$$BW = f_H - f_L \quad (4.120)$$

and since, usually, $f_L \ll f_H$,

$$BW \approx f_H \quad (4.121)$$

⁸ We strongly urge the reader to review Section 4.7 before proceeding with the study of this section.

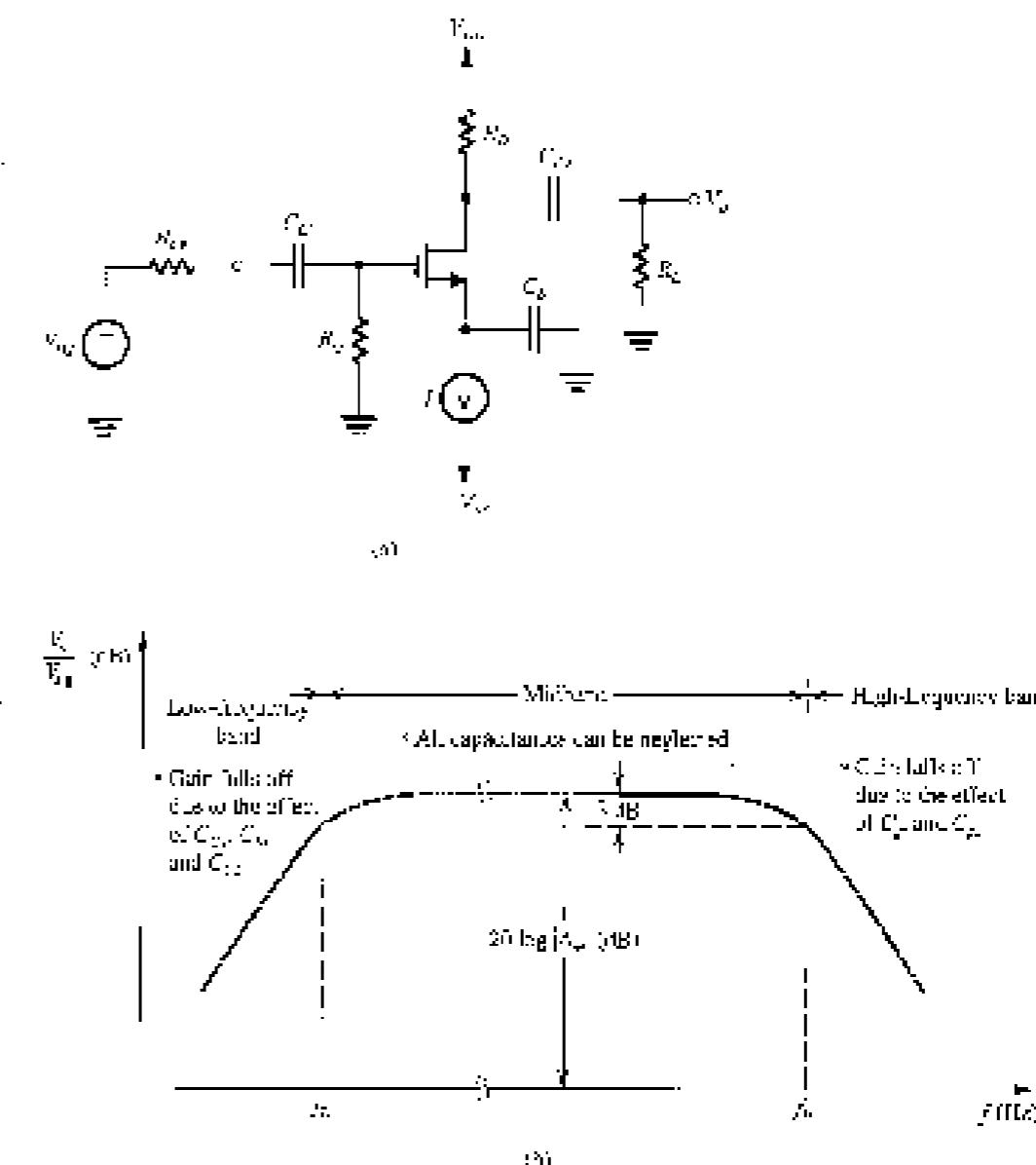


FIGURE 4.49 (a) Capacitively coupled common-source amplifier, (b) A sketch of the frequency response of the amplifier gain, (c) A graph of the three frequency bands of the amplifier.

A figure-of-merit for the amplifier is its **gain-bandwidth product**, which is defined as

$$GB = f_H \cdot BW \quad (4.122)$$

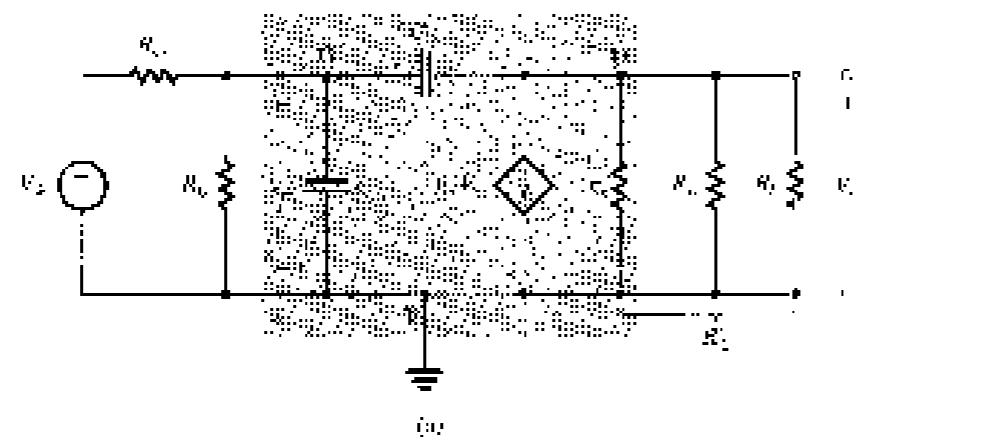
It will be shown at a later stage that in amplifier design it is usually possible to trade off gain for bandwidth. One way to accomplish this, for instance, is by adding a source degeneration resistance R_g , as we have done in Section 4.7.4.

4.8.2 The High-Frequency Response

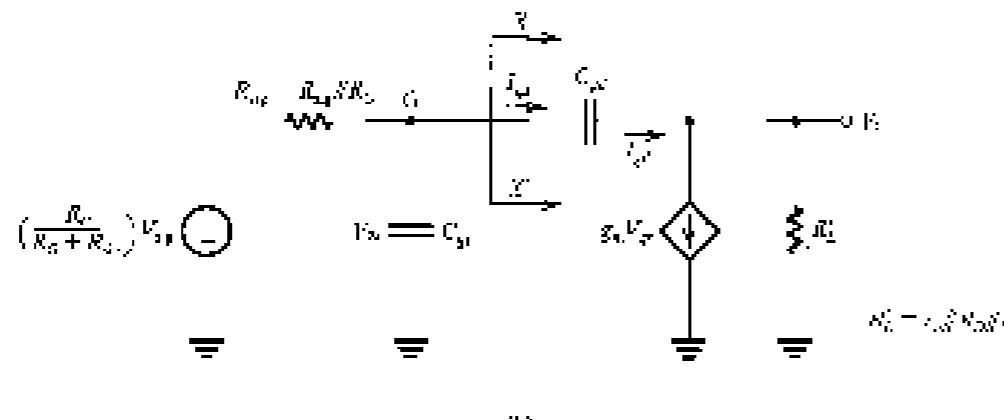
To determine the gain, or the transfer function, of the amplifier of Fig. 4.49(a) at high frequencies, and particularly the upper 3-dB frequency f_u , we replace the MOSFET with its high-frequency model of Fig. 4.47(c). At these frequencies, C_{gs} , C_{ds} , and C_{os} will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit shown in Fig. 4.50(a).

The equivalent circuit of Fig. 4.50(a) can be simplified by utilizing the Thévenin theorem at the input side and by combining the three parallel resistances at the output side. The resulting simplified circuit is shown in Fig. 4.50(b). This circuit can be further simplified if we can find a way to deal with the bypass capacitor C_{gs} that connects the output node to the input node. Toward this end, consider first the output node. It can be seen that the drain current is $(g_m V_{ds} - I_{ds})$, where $(g_m V_{ds})$ is the output current of the transistor and I_{ds} is the current supplied through the very small capacitance C_{gs} . At frequencies in the vicinity of f_u , which defines the edge of the midband, it is reasonable to assume that I_{ds} is still much smaller than $(g_m V_{ds})$, with the result that V_d can be given approximately by

$$V_d \approx (g_m V_{ds}) R_d = g_m R_d V_{ds} \quad (4.123)$$



(a)



(b)

FIGURE 4.50 Determining the high-frequency response of the CS amplifier: (a) equivalent circuit; (b) the circuit with a shunt load at the output.

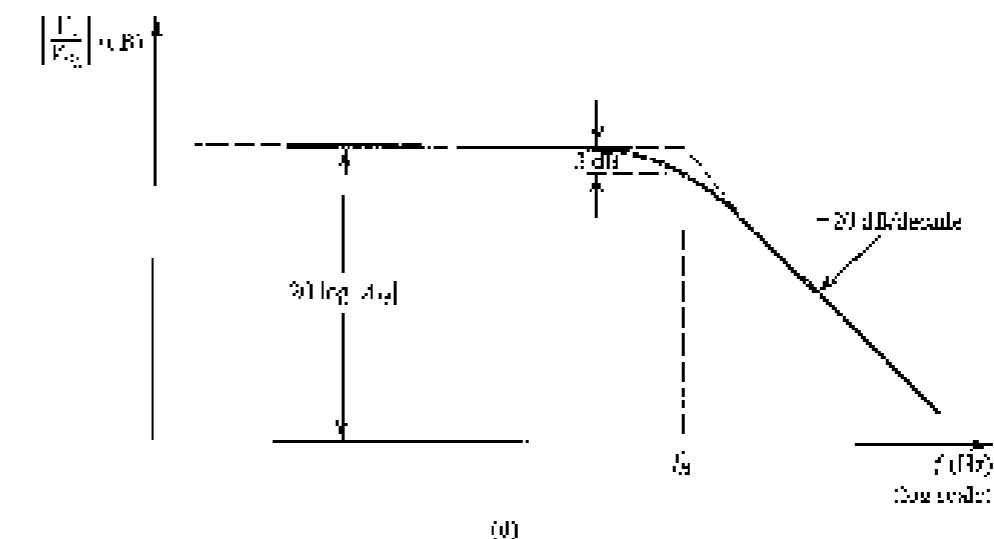
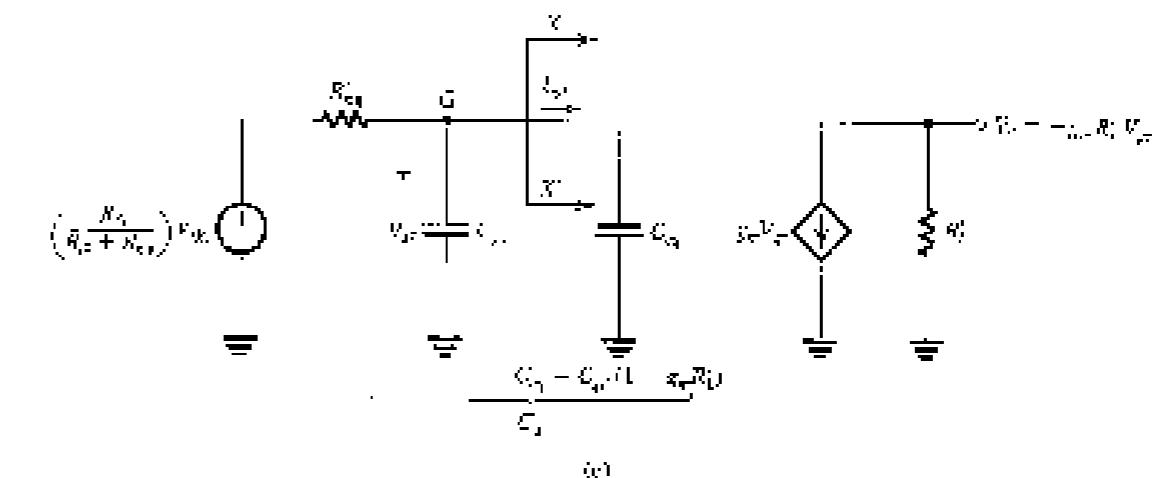


FIGURE 4.51 (a) Drawing of the equivalent circuit with C_{gs} replaced at the input side with the equivalent capacitance C_{eq} ; (b) the frequency response plot, which is that of a low-pass single time constant circuit.

where

$$R_d' = R_d \| R_2 \| R_1$$

Since $V_d = V_{ds}$, Eq. (4.123) indicates that the gain from gate to drain is $-g_m R_d'$, the same value as in the midband. The current I_{ds} can now be found as

$$\begin{aligned} I_{ds} &= s C_{gs} (V_{ds} - V_d) \\ &= s C_{gs} (V_{ds} - (-g_m R_d' V_{ds})) \\ &= s C_{gs} (1 + g_m R_d') V_{ds} \end{aligned}$$

Now, the left-hand side of the circuit in Fig. 4.50(b), at \mathcal{R}^* , knows of the existence of C_{ex} only through the current i_{ex} . Therefore, we can replace C_{ex} by an equivalent capacitance C_{eq} between the gate and ground as long as i_{ex} draws a current equal to i_{ex} . That is,

$$\omega L_{\text{eq}} i_{\text{ex}} = sC_{\text{eq}}(1 + g_m R'_v) V_{\text{ex}}$$

which results in

$$C_{\text{eq}} = C_{\text{ex}}(1 + g_m R'_v) \quad (4.124)$$

Using C_{eq} enables us to simplify the equivalent circuit at the input side to that shown in Fig. 4.50(c). We recognize the circuit of Fig. 4.50(c) as a single-pole-constant (STC) circuit of the low-pass type (Section 1.6 and Appendix D). Reference to Table 1.2 enables us to express the output voltage V_o in the STC circuit in the form

$$V_o = \frac{i}{\sqrt{R_v R_{\text{ex}}} \omega_0} \frac{V_{\text{ex}}}{1 + \frac{i}{\omega_0}} \quad (4.125)$$

where ω_0 is the corner frequency or the break frequency of the STC circuit.

$$\omega_0 = 1/C_{\text{eq}} R'_v \quad (4.126)$$

with

$$C_{\text{eq}} = C_{\text{ex}} - C_{\text{in}} = C_{\text{ex}} + C_{\text{ex}}(1 + g_m R'_v) \quad (4.127)$$

and

$$R'_v = R_{\text{ex}} + R_v \quad (4.128)$$

Combining Eqs. (4.123) and (4.125) results in the following expression for the high-frequency gain of the CS amplifier:

$$\frac{V_o}{V_{\text{ex}}} = -\left(\frac{R_v}{R_v + R_{\text{ex}}} \right)^2 \frac{A_H}{1 + \frac{i}{\omega_0}} \quad (4.129)$$

which can be expressed in the form

$$\frac{V_o}{V_{\text{ex}}} = \frac{A_H}{1 + \frac{i}{\omega_0}} \quad (4.130)$$

where the midband gain A_H is given by Eq. (4.1.9) and ω_0 is the upper 3-dB frequency:

$$\omega_0 = \omega_c = \frac{1}{C_{\text{eq}} R'_v} \quad (4.131)$$

and

$$\omega_c = \frac{g_m}{2\pi} + \frac{1}{2\pi C_{\text{eq}} R'_v} \quad (4.132)$$

We thus see that the high-frequency response will be that of a low-pass STC network with a 3-dB frequency f_0 determined by the time constant $C_{\text{eq}} R'_v$. Figure 4.50(d) gives a sketch of the magnitude of the high-frequency gain.

Before leaving this section we wish to make a number of observations:

1. The upper 3-dB frequency is determined by the interaction of $R'_v = R_v + R_{\text{ex}}$ and $C_{\text{eq}} = C_{\text{ex}}(1 + g_m R'_v)$. Since the bias resistance R_v is usually very large, it can be neglected, resulting in $R'_v = R_{\text{ex}}$, the resistance of the signal source. It follows that a large value of R_{ex} will cause f_0 to be lowered.
2. The total input capacitance C_{in} is usually dominated by C_{ex} , which in turn is made large by the multiplication effect due to C_{ex} itself. Thus, although C_{ex} is usually a very small capacitance, its effect on the high-frequency response can be very significant as a result of its multiplication by the factor $(1 + g_m R'_v)$, which is approximately equal to the midband gain of the amplifier.
3. The multiplication effect due to C_{ex} undergoes changes about because it is collected between two nodes whose voltages are related by a large negative gain ($-g_m R'_v$). This effect is known as the Miller effect, and $(1 + g_m R'_v)$ is known as the Miller multiplier. It is the Miller effect that causes the CS amplifier to have a large total input capacitance C_{in} and hence a low f_0 .
4. To extend the high-frequency response of a MOSFET amplifier, we have to find conditions in which the Miller effect is absent or at least reduced. We shall return to this subject at great length in Chapter 6.
5. The above analysis, resulting in an STC or a single-pole response, is a simplified one. Specifically, it is based on neglecting i_{ex} relative to $g_m R'_v$, an assumption that applies well at frequencies much lower than f_0 . A more exact analysis of the circuit in Fig. 4.50(a) will be carried out in Chapter 6. The results above, however, are more than sufficient for our current needs.

Example 4.10

Find the midband gain A_H and the upper 3-dB frequency f_0 of a CS amplifier fed with a signal source having an internal resistance $\mathcal{R}_v = 100 \text{ k}\Omega$. The amplifier has $R_v = 4.7 \text{ M}\Omega$, $R_t = 15 \text{ k}\Omega$, $\rho_s = 1 \text{ mV/V}$, $r_o = 150 \text{ M}\Omega$, $C_{\text{ex}} = 1 \text{ pF}$, and $C_{\text{in}} = 0.1 \text{ pF}$.

Solution

$$A_H = -\frac{R_t}{R_v + R_t} \approx \frac{R_t}{R_v}$$

Thus,

$$R'_v = r_s + R_t + R_v = 150 \parallel 15 \parallel 4.7 = 2.14 \text{ k}\Omega$$

$$g_m R'_v = 1 \times 2.14 = 2.14 \text{ V/V}$$

Thus,

$$A_H = -\frac{4.7}{4.7 + 0.1} \approx 0.99 \approx 1 \text{ V/V}$$

The equivalent capacitance, C_{eq} , is found as

$$C_{eq} = (1 - \bar{\pi}_A R) / C_A$$

$$= .1 + 7.47 \times 0.1 = 3.27 \text{ ;}$$

The next important step is to calculate the observed

$$G_{\mu} = G_{\nu}, \quad G_{\mu} = 1 - 2.26 = 1.26 \times$$

The *APC02-13* inventory (in Gt C) is:

$$k_B = \frac{1}{2\pi C_0(E_{\text{ref}} + E_F)}$$

$$= \frac{1}{3.9 \times 1.76 \times 10^{-12} (0.1 + 14.7) \times 10}$$

$$= 382 \text{ kJ/K}$$

EXERCISES

439 4.39. *Chlorophytum comosum* (L.) Willd. ex Willd. *var. comosum* (L.) Willd. *var. comosum* (L.) Willd. *var. comosum* (L.) Willd.

4.9.3 The Low-Frequency Response

To determine the low-frequency gain or transfer function of the common-source amplifier we show in Fig. 13.5.1(a) the circuit with the dc sources eliminated (current source I open-circuited and voltage source V_{DD} short-circuited). We can then carry the small-signal analysis directly on this circuit. However, we will ignore v_o . This is done in order to keep the analysis simple and thus focus attention on significant issues. The effect of v_o on the low-frequency operation of this amplifier is minor; as can be verified by a SPICE simulation (Section 13.2).

The analysis begins at the signal generator by finding the fraction of V_{12} that appears in the transistor base.

$$V_x = V_{x0} \frac{R_C}{R_S} \frac{1}{\sqrt{1 + R_L}}$$

which can be written in the alternative form

$$V_r = V_{cr} \frac{R_0}{R_C - R_{ik}} = \frac{2\pi}{\sqrt{(R_0 - R_{ik})}} \quad (1.15)$$

Thus we see that the expression for the signal transmission from signal generator to amplifier input has essentially frequency-dependent factor. From our study of frequency response

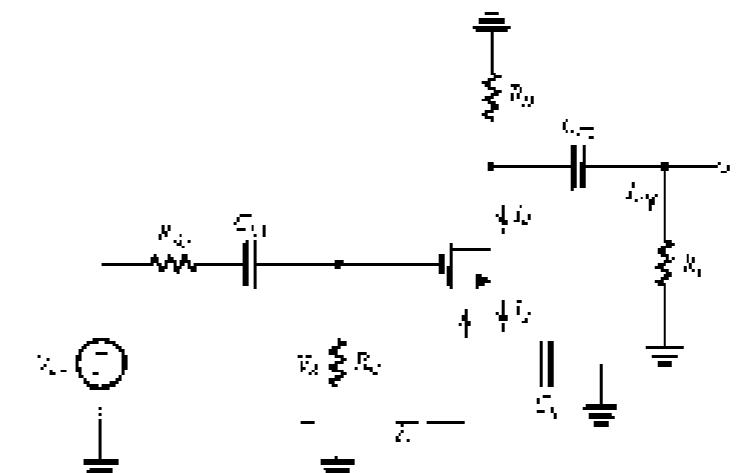


FIGURE 4.51 Analysis of the CX amplifier to determine its low-to-quiescent transfer function. For simplicity, $r_{\text{L}} = R_{\text{L}}$.

In Section 1.6 (see also Appendix D), we recognize this factor as the transfer function of an STC network of the high-pass type with a break or corner frequency $\omega_0 = 1/\sqrt{L_{\text{ext}}(R_C + R_{\text{ext}})}$. Thus the effect of the coupling capacitor C_{ext} is to introduce a high-pass STC response with a break frequency that we shall denote ω_0 .

$$n_{T_1} = n_1 - \frac{1}{C_{11}(R_1 + R_{11})} \quad (4.134)$$

Continuing with the analysis, we next determine the drain current I_D by dividing V_D by the total resistance in the source circuit which is $\left(\frac{1}{2}R_s + \left(\frac{1}{2}R_S\right)\right)$, to obtain

$$I_2 = \frac{F_2}{\gamma + \frac{1}{kC}}$$

which can be written with a license form

$$f_{ij} = p_{ij} V_{ij} \frac{\delta}{\delta + \frac{2m}{C}} \quad (4.125)$$

We observe that C_1 introduces a frequency-dependent factor, which is also of the STC type, i.e., pass band. Thus the same filter requires another break frequency.

$$\phi_{\text{eff}} = \frac{\phi_0}{C_0} \quad (4.126)$$

To complete the analysis, we find R_1 by first using the current-divider rule to determine the fraction of I_1 that flows through R_1 :

$$I_o = -I_a \frac{R_o}{R_{in} + \frac{1}{C_o} + R}$$

and then multiplying by R_2 to obtain

$$V_o = I_s R_2 = -I_s \frac{R_2 R_3}{R_3 + R_L} = -\frac{g_m V}{C_{GS}(R_3 + R_L)} \quad (4.137)$$

from which we see that C_{GS} introduces a third Sallen low-pass factor, giving the amplifier a third break frequency at

$$\omega_{p3} = \frac{1}{C_{GS}(R_3 + R_L)} \quad (4.138)$$

The overall low-frequency transfer function of the amplifier can be found by combining Eqs. (4.137), (4.138), and (4.137) and rewriting the break frequencies by their symbols from Eqs. (4.134), (4.136), and (4.138).

$$\frac{V_o}{V_{in}} = \frac{-g_m R_3}{(R_3 + R_{L3})} \left[g_m (R_3 + R_L) \left(\frac{s}{s + \omega_{p1}} \right) \left(\frac{s}{s + \omega_{p2}} \right) \left(\frac{s}{s + \omega_{p3}} \right) \right] \quad (4.139)$$

The low-frequency magnitude response can be obtained from Eq. (4.139) by replacing s by $j\omega$ and finding $|V_o/V_{in}|$. In many cases, however, one of the three break frequencies can be much higher than the other two, say by a factor greater than 10. In such a case, it is the high-frequency break point that will determine the lower 3-dB frequency, f_L , and we do not have to do any additional band analysis. For instance, because the expression for ω_{p3} includes ρ_m (Eq. 4.138), ω_{p3} is usually higher than ω_{p1} and ω_{p2} . If ω_{p3} is sufficiently separated from ω_{p1} and ω_{p2} , then

$$f_L = f_{p1}$$

which means that, in such a case, the bypass capacitor determines the low end of the midband. Figure 4.52 shows a sketch of the low-frequency gain of a CS amplifier in which the three break frequencies are sufficiently separated so that their effects appear distinct. Observe that at each break frequency, the slope of the asymptotes to the gain curve increases by 20 dB/decade. Readers familiar with poles and zeros will recognize f_L , f_{p2} , and f_{p3} as the frequencies of the three real low-frequency poles of the amplifier. We will use poles and zeros and related asymptotic approximation in Chapter 6 and beyond.

Before leaving this section, it is essential that the reader be able to quickly find the time-constant and hence the break frequency associated with each of the three capacitors. The procedure is simple:

1. Reduce V_{in} to zero.
2. Consider each capacitor separately, that is, assume that the other two capacitors are acting as perfect short circuits.
3. For each capacitor, find the total resistance seen between its terminals. This is the resistance that determines the time constant associated with this capacitor.

The reader is encouraged to apply this procedure to C_{GS} , C_S , and C_{L3} and thus see that Eqs. (4.134), (4.136), and (4.138) can be written by inspection.

Selecting Values for the Coupling and Bypass Capacitors We now address the design issue of selecting appropriate values for C_{GS} , C_S , and C_{L3} . The design objective is to place the lowest 3-dB frequency f_L at a specified value while minimizing the capacitor values.

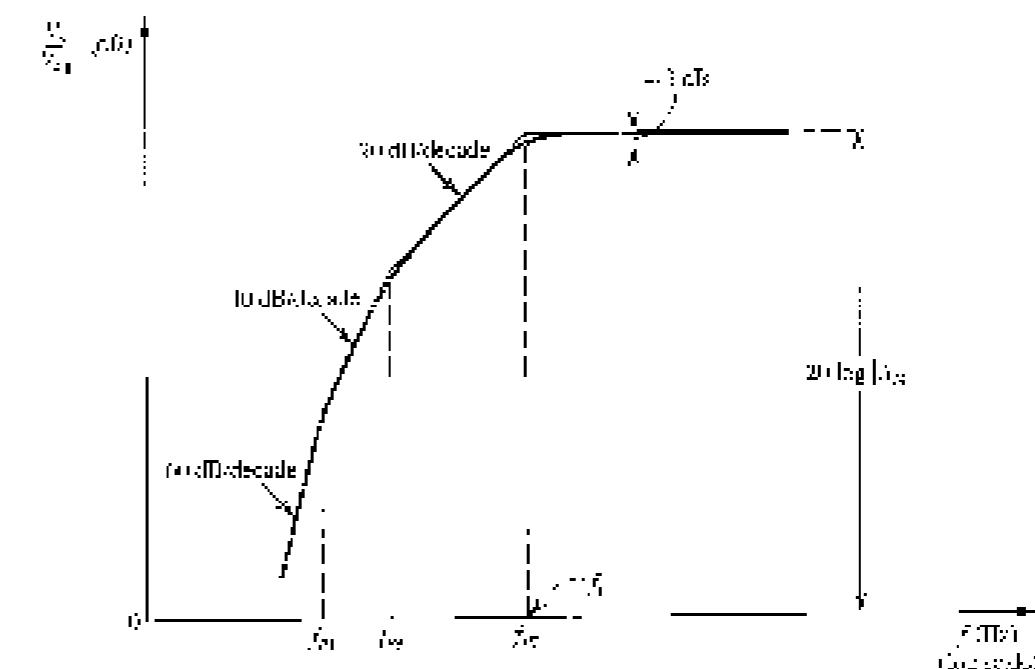


FIGURE 4.52 Sketch of the low-frequency magnitude response of a CS amplifier for which the three break frequencies are sufficiently separated for their effects to appear distinct.

Since as mentioned above C_S results in the highest of the three break frequencies, the total capacitance is minimized by selecting C_S so that its break frequency $f_{p2} = f_L$. We then decline on the location of the other two break frequencies, say 5 to 10 times lower than the frequency of the dominant one, f_{p2} . However, the values selected for f_L and f_{p3} should not be too low, for that would require larger values for C_{GS} and C_{L3} ; that may be necessary. The design procedure will be illustrated by an example.

Example 4.12

We wish to select appropriate values for the coupling capacitors C_{GS} and C_{L3} and the bypass capacitor C_S for the CS amplifier whose high-frequency response was analyzed in Example 4.12. The amplifier has $R_g = 4.7 \text{ k}\Omega$, $R_3 = R_L = 15 \text{ k}\Omega$, $R_{in} = 30 \text{ M}\Omega$, and $g_m = 1 \text{ mA/V}$. It is required to have f_L at 100 Hz and that the nearest break frequency be at least a decade lower.

Solution

We select C_S so that

$$f_{p2} = \frac{1}{2\pi C_S R_L} = f_L$$

thus

$$C_S = \frac{R_L}{2\pi f_L} = \frac{1 + 10^3}{2\pi \times 100} = 1.5 \mu\text{F}$$

Let $i_s = i_p = 10 \text{ mA}$, we obtain

$$10 = \frac{1}{2\pi C_{GS}(15 - 15) \times 10^3}$$

which yields

$$C_{GS} = 0.3 \text{ pF}$$

and

$$10 = \frac{1}{2\pi C_{DS}(15 - 15) \times 10^3}$$

which results in

$$C_{DS} = 0.3 \text{ pF}$$

EXERCISE

Given $V_{DD} = 5 \text{ V}$, $V_{SS} = -5 \text{ V}$, $i_s = 10 \text{ mA}$, $i_p = 10 \text{ mA}$, $C_{GS} = 0.3 \text{ pF}$, and $C_{DS} = 0.3 \text{ pF}$, calculate the output voltage v_o for the input voltage $v_i = 0.5 \text{ V}$. Assume that the drain-to-source voltage is zero.

4.9.4 A Final Remark

The frequency response of the other amplifier configurations will be studied in Chapter 6.

4.10 THE CMOS DIGITAL LOGIC INVERTER

Complementary MOS or CMOS logic circuits have been available as standard packages for use in conventional digital system design since the early 1970s. Such packages contain logic gates and other digital system building blocks with the number of gates per package ranging from a few (small-scale integrated orSSI) circuitry) to few tens (medium-scale integrated orMSI) circuitry).

In the late 1970s, as the era of large- and very-large-scale integration (LSI and VLSI) hundreds- to thousands-of-gates-per-chip began, circuits using only n -channel MOS transistors, known as NMOS, became the fabrication technology of choice. Indeed, early VLSI circuits, such as the early microprocessors, employed NMOS technology. Although at that time the design flexibility and other advantages that CMOS offers were known, the CMOS technology available then was too complex to produce such high-density VLSI chips economically. However, as advances in processing technology were made, this state of affairs changed rapidly. In fact, CMOS technology has now completely replaced NMOS at all levels of integration, in both analog and digital applications.

For any IC technology used in digital circuit design, the basic circuit element is the logic inverter.¹⁰ Once the operation and characteristics of the inverter circuit are thoroughly

¹⁰ A study of the digital logic inverter as a basic building block was presented in Section 4.1. A review of this material before proceeding with the actual section should prove helpful.

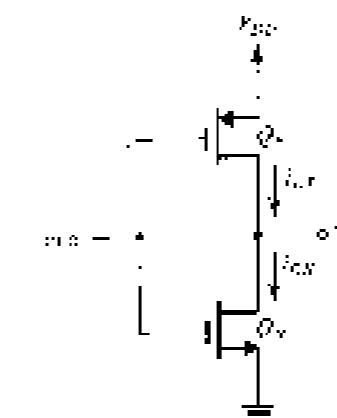


FIGURE 4.53 In CMOS inverter

understood, the results can be extended to the design of logic gates and other more complex circuits. In this section we provide such a study for the CMOS inverter. Our study of the CMOS inverter and logic circuits will continue in Chapter 10.

The basic CMOS inverter is shown in Fig. 4.53. It utilizes two matched enhancement-type MOSFETs, one (Q_1), with an n -channel and the other (Q_2), with a p -channel. The body of each device is connected to a source and thus no body effect arises. As will be seen shortly, the CMOS circuit realizes the conventional inverter logic implementation studied in Chapter 1 (Fig. 1.52), where a pair of switches are operated in a complementary fashion by the input voltage v_i .

4.10.1 Circuit Operation

We first consider the two extreme cases, when v_i is at logic 0 level, which is approximately 0 V , and when v_i is at logic 1 level, which is approximately V_{DD} volts. In both cases, for ease of exposition we shall consider the n -channel device Q_1 to be the driving transistor and the p -channel device Q_2 to be the load. However, since the circuit is completely symmetric, this assumption is obviously arbitrary, and the results would lead to identical results.

Figure 4.54 illustrates the case when $v_i = V_{DD}$, showing the $i_D - v_{DS}$ characteristic curve for Q_1 with $v_{GS} = V_{DD}$. (Note that $v_{GS} = v_i$ and $v_{DS} = v_o$.) Superimposed on the i_D -characteristic curve is the load curve, which is the i_D vs. v_{DS} curve of Q_2 for the case $v_{GS} = 0 \text{ V}$. Since $v_{GS} < |V_t|$, the load curve will be a horizontal straight line at almost zero current level. The operating point will be at the intersection of the two curves, whom we note that the output voltage is nearly zero (typically less than 10 mV) and the current through the two devices is also nearly zero. This means that the power dissipation in the circuit is very small (typically a fraction of a microwatt). Note, however, that although Q_1 is operating at nearly zero current and zero drain source voltage (i.e., near the origin of the $i_D - v_{DS}$ plane), its operating point is on a steep segment of the $i_D - v_{DS}$ characteristic curve. Thus Q_1 provides a low resistance path between the output terminal and ground, with the resistance obtained using Eq. (4.7) as

$$r_{DSV} = 1/\left[k_n' \left(\frac{W}{L}\right) (V_{DD} - V_{t1})\right] \quad (4.140)$$

Figure 4.54(c) shows the equivalent circuit of the inverter when the input is high. The circuit confirms that $v_o = V_{DD} \approx 0 \text{ V}$ and that the power dissipation at the inverter is zero.

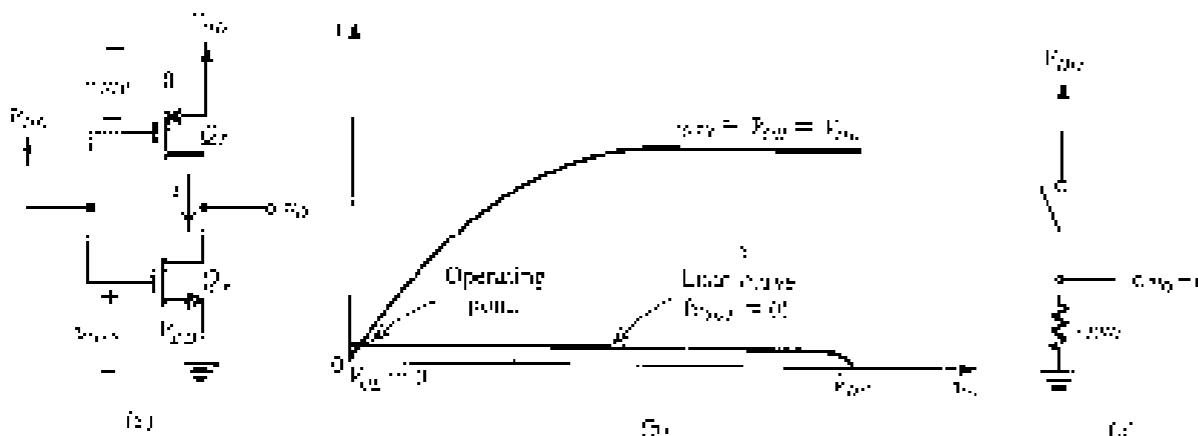


FIGURE 4.54 Operation of the CMOS inverter when v_i is high: (a) circuit with $v_i = V_{DD}$, logic 1 level; (b) graph of current to determine operating point; (c) equivalent circuit.

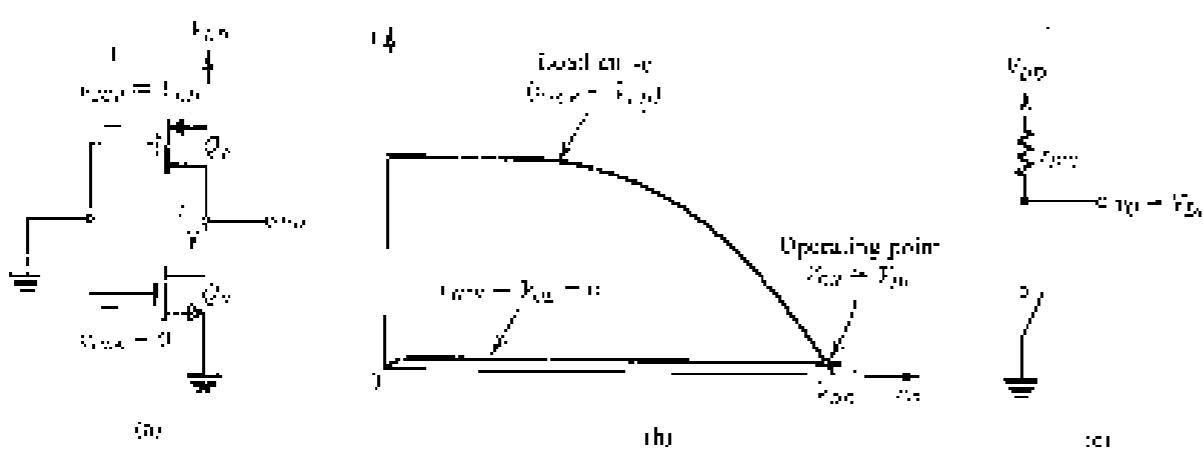


FIGURE 4.55 Operation of the CMOS inverter when v_i is low: (a) circuit with $v_i = 0$, logic 0 level; (b) graph of current to determine operating point.

The other extreme case, when $v_i = 0 \text{ V}$, is illustrated in Fig. 4.55. In this case (b), operating at $v_{GS1} = 0$, hence the i_D-v_{DS} -characteristic is a most horizontal straight line at zero current level. The load curve is the i_D-v_{DS} -characteristic of the p-channel device with $v_{GS2} = V_{DD}$. As shown, at the minimum point the output voltage is almost equal to V_{DD} (typically less than 10 mV below V_{DD}), and the current in the two devices is still nearly zero. Thus the power dissipation in the circuit is very small in both extreme cases.

Figure 4.56(a) shows the equivalent circuit of the inverter when the input is low. We see that Q_1 provides a low-resistance path between the output terminal and the dc supply V_{DD} , with the resistance given by

$$r_{DS1} = 1/\left[k_D \left(\frac{W}{L} \right)_D (V_{DD} - |V_T|) \right] \quad (4.14)$$

The equivalent circuit confirms that in this case $v_o = V_{DD} = V_{PO}$ and that the power dissipation in the inverter is zero.

It should be noted, however, that in spite of the fact that the quiescent current is zero, the load driving capability of the CMOS inverter is high. For instance, with the load circuit as in the circuit of Fig. 4.51, transistor Q_1 can sink a relatively large load current. This current can quickly discharge the load capacitance, as will be seen shortly. Because of its role in sinking load current and thus pulling the output voltage down toward ground, transistor Q_1 is known as the "pull-down" device. Similarly, with the input low, as in the circuit of Fig. 4.55, transistor Q_2 can source a relatively large load current. This current can quickly charge up a load capacitance, thus pulling the output voltage up toward V_{DD} . Hence, Q_2 is known as the "pull-up" device. The reader will recall that we used this terminology in connection with the conceptual inverter circuit of Fig. 1.52.

From the above, we conclude that the basic CMOS logic inverter behaves as an ideal inverter, in summary:

1. The output voltage levels are 0 and V_{DD} , and thus the signal swing is the maximum possible. This, coupled with the fact that the inverter can be designed to achieve a very uniform voltage-transfer characteristic, results in wide noise margins.
2. The static power dissipation in the inverter is very negligible. The dissipation due to leakage currents in both of its states (Recall that the static power dissipation is so small as to distinguish it from the dynamic power dissipation during the repeated switching of the inverter, as will be discussed shortly).
3. A low-resistance path exists between the output terminal and ground (in the low-output state) or V_{DD} (in the high-output state). These low-resistance paths ensure that the output voltage is 0 or V_{DD} , independent of the exact values of the k_D/k_A ratios or other device parameters. Furthermore, the low output resistance makes the inverter less sensitive to the effects of noise and other disturbances.
4. The active pull-up and pull-down devices provide the inverter with high load-driving capability in both directions. As will be seen, this speeds up the operation considerably.
5. The input resistance of the inverter is infinite because $i_G = 0$. Thus the inverter can drive an arbitrary large number of similar inverters with no loss in signal level. Of course, each additional inverter increases the load capacitance on the driving inverter and slows down the operation. Shortly, we will consider the inverter switching times.

4.10.2 The Voltage Transfer Characteristic

The complete voltage transfer characteristic (VTC) of the CMOS inverter can be obtained by repeating the graphical procedure used above in the two extreme cases, for all intermediate values of v_i . In the following, we will evaluate the critical points of the switching voltage transfer curve. For this we need the $i-v$ -relationships of Q_1 and Q_2 for v_i ,

$$i_{DS1} = k_D \left(\frac{W}{L} \right)_D \left(v_o - V_{DD} \right) v_o - \frac{1}{2} v_i^2 \quad \text{for } v_i \leq v_o - V_{DD} \quad (4.142)$$

and

$$i_{DS2} = \frac{1}{2} k_A \left(\frac{W}{L} \right)_A \left(v_o - V_{DD} \right)^2 \quad \text{for } v_i \geq v_o - V_{DD} \quad (4.143)$$

For Q_p ,

$$i_{Dp} = \frac{1}{2} k_s' \frac{W}{L} v_o (V_{DS} - v_o - V_{GS}) (V_{DS} - v_o) - \frac{1}{2} (V_{DS} - v_o)^2 \quad \text{for } v_o \geq v_t + |V_{GS}| \quad (4.141)$$

and

$$i_{Dp} = \frac{1}{2} k_s' \frac{W}{L} v_o (V_{DS} - v_o - |V_{GS}|)^2 \quad \text{for } v_o \leq v_t + |V_{GS}| \quad (4.142)$$

The CMOS inverter is usually designed to have $V_{DD} = V_{SS} = V_t$ and $k_s' W/L_{Qp} = k_s' W/L_{Qn}$. It should be noted that since μ_n is 0.5 to 0.8 times the value of μ_p , to make $k_s' W/L$ of the two devices equal, the width of the p -channel device is made two to three times that of the n -channel device. More specifically, the two devices are designed to have equal lengths, with widths related by

$$\frac{W_{Qp}}{W_{Qn}} = \frac{\mu_p}{\mu_n}$$

This will result in $k_s' W/L_{Qp} = k_s' W/L_{Qn}$, and the inverter will have a symmetric transfer characteristic and equal current driving capability in both directions (pull-up and pull-down).

With Q_n and Q_p matched, the CMOS inverter has the voltage transfer characteristic shown in Fig. 4.56. As indicated, the transfer characteristic has five distinct segments corresponding to different combinations of states of operation of Q_n and Q_p . The vertical

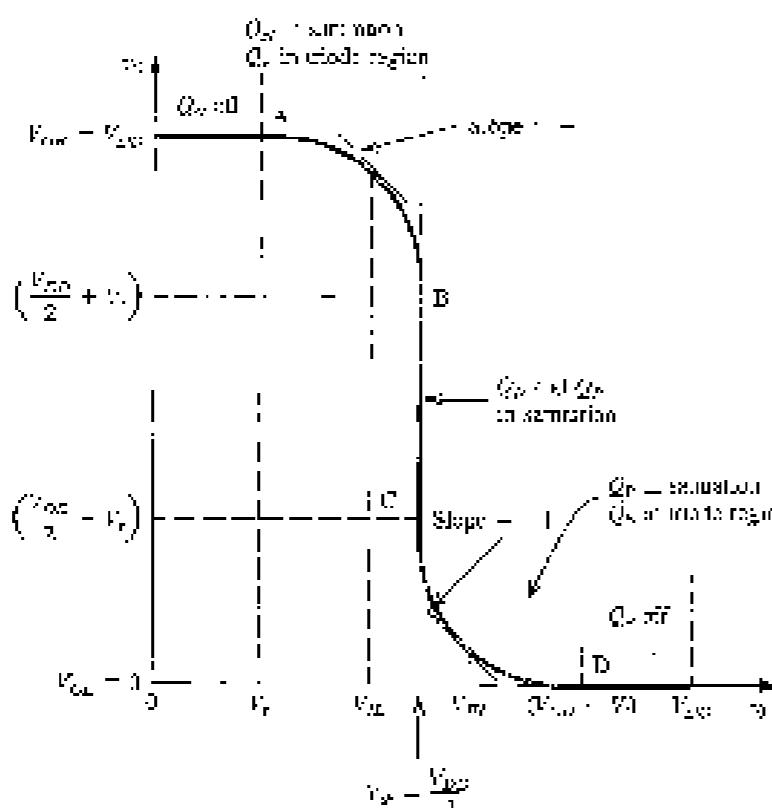


FIGURE 4.56 The voltage transfer characteristic of the CMOS inverter.

region at DC is obtained when both Q_n and Q_p are operating in the saturation region. Because we are neglecting the finite output resistance in saturation, the transfer gain in this region is infinite. From symmetry, this vertical segment occurs at $v_t = V_{DD}/2$ and is bounded by $v_o(B) = V_{DD}/2 - V_t$ and $v_o(C) = V_{DD}/2 + V_t$.

The reader will recall from Section 4.7 that in addition to V_{GS} and V_{DS} , two other points can be used to determine the basic margins of the inverter. These are the maximum permitted logic-0 or "low" level at the input, V_{IL} , and the minimum permitted logic-1 or "high" level at the output, V_{OL} . These are formally defined as the two points on the transfer curve at which the incremental gain is unity (i.e., the slope is $+1/V_t$).

To determine V_{IL} we note that Q_n is in the triode region, and thus its current is given by $i_{Dn} = 1/2 I_D$, while Q_p is in saturation and its current is given by Eq. (4.143). Equating i_{Dn} and i_{Dp} and assuming matched devices, gives

$$v_t - V_{GS} = \frac{1}{2} v_o^2 = \frac{1}{2} (V_{DD} - v_o)^2 \quad (4.143)$$

Differentiating both sides relative to v_o results in

$$(v_t - V_{GS}) \frac{dv_o}{dv_o} + v_o - v_t \frac{dv_o}{dv_o} = -(V_{DD} - v_o) \quad (4.144)$$

in which we substitute $v_t = V_{DD}$ and $dv_o/dv_o = 1$ to obtain

$$v_o = V_{DD} - \frac{V_{DD}}{2} \quad (4.145)$$

Substituting $v_t = V_{DD}$ and from Eq. (4.143) to Eq. (4.144) gives

$$V_{IL} = \frac{1}{2}(5V_{DD} - 2V_t) \quad (4.146)$$

V_{IL} can be determined in a manner similar to that used to find V_{OL} . Alternatively, we can use the symmetry relationship

$$V_{IL} = \frac{V_{DD} - V_{GS}}{2} + V_{IL}$$

together with V_{IL} from Eq. (4.146) to obtain

$$V_{IL} = \frac{1}{4}(V_{DD} + 2V_t) \quad (4.147)$$

The noise margins can now be determined as follows:

$$\begin{aligned} NM_{pi} &= V_{OL} - V_{GS} \\ &= V_{DD} - \frac{1}{2}(5V_{DD} - 2V_t) \\ &= \frac{1}{2}(3V_{DD} + 2V_t) \end{aligned} \quad (4.148)$$

$$\begin{aligned} NM_{po} &= V_{GS} - V_{OL} \\ &= \frac{1}{2}(3V_{DD} + 2V_t) - 0 \\ &= \frac{1}{2}(3V_{DD} + 2V_t) \end{aligned} \quad (4.149)$$

As expected, the symmetry of the voltage transfer characteristic results in equal noise margins. Of course, if Q_n and Q_p are not matched, the voltage transfer characteristic will no longer be symmetric, and the noise margins will not be equal (see Problem 4.67).

EXERCISES

- 4.41 Design a single-transistor MOSFET inverter with $V_{DD} = 10\text{ V}$, $L = 1\text{ }\mu\text{m}$, $k_n = 100\text{ A/V}^2/\text{D}_{\text{sat}}$, $k_p = 40\text{ A/V}^2/\text{D}_{\text{sat}}$, $V_{t,n} = -1\text{ V}$, and $V_{t,p} = 1\text{ V}$. Plot the output voltage versus time for a square-wave input.
- 4.42 Consider a CMOS inverter with $V_{DD} = 10\text{ V}$, $L = 1\text{ }\mu\text{m}$, $k_n = 100\text{ A/V}^2/\text{D}_{\text{sat}}$, $k_p = 40\text{ A/V}^2/\text{D}_{\text{sat}}$, $V_{t,n} = -1\text{ V}$, and $V_{t,p} = 1\text{ V}$. Plot the output voltage versus time for a square-wave input.
- 4.43 Design a single-transistor CMOS technology uses the minimum possible channel lengths ($L = 1\text{ }\mu\text{m}$, $k_n = 100\text{ A/V}^2/\text{D}_{\text{sat}}$, $k_p = 40\text{ A/V}^2/\text{D}_{\text{sat}}$, $V_{t,n} = -1\text{ V}$, and $V_{t,p} = 1\text{ V}$) to calculate the value of the output resistance of the inverter when $v_o = 5\text{ V}$.
- 4.44 Show that the threshold voltage of a CMOS inverter (set to 0) is given by
- $$V_{t,0} = \frac{V_{DD}}{2} + \frac{k_p}{k_n} V_{t,p} = \frac{V_{DD}}{2} + \frac{V_{t,p}}{V_{t,n}}$$

4.10.3 Dynamic Operation

As explained in Section 1.7, the speed of operation of a digital system (e.g., a computer) is determined by the propagation delay of the logic gates used to construct the system. Since the inverter is the basic logic gate of any digital IC technology, the propagation delay of the inverter is a fundamental parameter in characterizing the technology. In the following, we analyze the switching operation of the CMOS inverter to determine its propagation delay. Figure 4.57(a) shows the inverter with a capacitor C between the output node and ground. Here C represents the sum of the appropriate internal capacitances of the MOSFETs Q_1 and Q_2 , the capacitance of the interconnect wire between the inverter output node and the inputs of the other logic gates the inverter is driving, and the total input capacitance of these load (or fan-out) gates. We assume that the inverter is driven by the ideal pulse (zero rise and fall times) shown in Fig. 4.57(b). Since the circuit is symmetric (assuming standard MOSFETs), the rise and fall times of the output waveform should be equal. It is sufficient, therefore, to consider either the turn-on or the turn-off process. In the following, we consider the first.

Figure 4.57(c) shows the trajectory of the operating point obtained when the input pulse goes from $V_{DD} = 0$ to $V_{DD} = V_{DD}$ at time $t = 0$. Just prior to the leading edge of the input pulse (that is, at $t = 0^-$) the output voltage equals V_{DD} and capacitor C is charged to this voltage. At $t = 0$, v_o rises to V_{DD} , causing Q_1 to turn off immediately. From then on, the circuit is equivalent to that shown in Fig. 4.57(d) with the initial value of $v_o = V_{DD}$. Thus the operating point at $t = 0^+$ is point E, at which it can be seen that Q_2 will be in the saturation region and conducting a large current. As C discharges, the control of Q_2 remains constant until $v_o = V_{DD} - V$ (point F). During this portion of the discharge interval $t_{\text{dis}}(t)$ (where the subscript

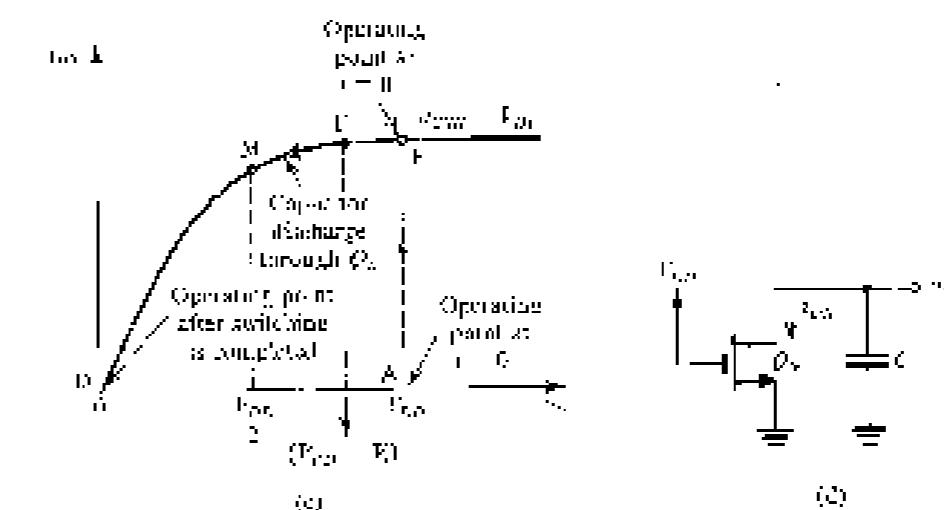
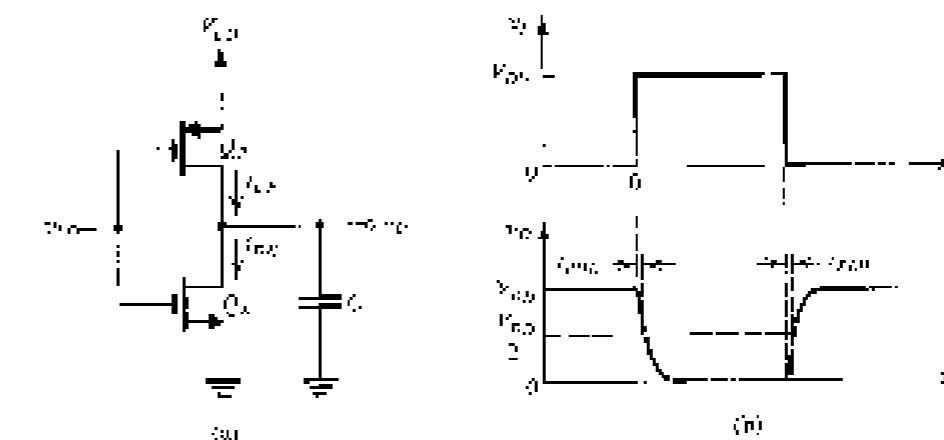


FIGURE 4.57 Dynamic operation of a cascoded body-loaded CMOS inverter: (a) with the input and output waveforms; (c) trajectory of the operating point as the input goes high and C discharges through Q_2 ; (d) equivalent circuit during the capacitive discharge.

EL indicates the turn-to-low output transition, we can write

$$\begin{aligned} t_{\text{dis}}(t) &= \frac{C(V_{DD} - (V_{DD} - V))}{\frac{1}{2} k_s' \left(\frac{W}{L}\right)_n (V_{DD} - V)^2} \\ &= \frac{CV}{\frac{1}{2} k_s' \left(\frac{W}{L}\right)_n (V_{DD} - V)^2} \end{aligned} \quad (4.152)$$

Beyond point F, transistor Q_2 operates in the triode region, and thus its current is given by Eq. 4.113. This portion of the discharge interval can be described by

$$i_{\text{dis}}(t) = -C \partial v_o / \partial t$$

Substituting in Eq. (4.142) and rearranging the differential equation, we obtain

$$\frac{k'_i(W/L)}{C} \frac{dV_D}{dt} = \frac{1}{(V_{DD} - V_i)} \frac{\frac{dV_D}{dt}}{\frac{1}{2(V_{DD} - V_i)} \frac{dV_D}{dt} - v_0} \quad (4.153)$$

To find the component of the delay time (t_{prop}) during which v_D decreases from $(V_{DD} - V_i)$ to the 50% point, $v_0 = V_{DD}/2$, we integrate both sides of Eq. (4.153). Denoting this component of delay time t_{prop} , we find that

$$\frac{k'_i(W/L)}{C} t_{prop} = \frac{1}{(V_{DD} - V_i)} \int_{v_0}^{(V_{DD} - V_i)/2} \frac{\frac{dV_D}{dt}}{\frac{1}{2(V_{DD} - V_i)} \frac{dV_D}{dt} - v_0} dt \quad (4.154)$$

Using the fact that

$$\int \frac{dx}{x^2} = \pi \left(1 - \frac{1}{x^2} \right)$$

enables us to evaluate the integral in Eq. (4.154) and it is obtained

$$t_{prop} = \frac{C}{k'_i(W/L)(V_{DD} - V_i)} \ln \left(\frac{3V_{DD} - 4V_i}{V_{DD}} \right) \quad (4.155)$$

The two components of t_{prop} in Eqs. (4.152) and (4.155) can be added to obtain

$$t_{prop} = \frac{2C}{k'_i(W/L)(V_{DD} - V_i)} \left[\frac{V_i}{V_{DD} - V_i} + \frac{1}{2} \ln \left(\frac{3V_{DD} - 4V_i}{V_{DD}} \right) \right] \quad (4.156)$$

For the usual case of $V_i \approx 0.2V_{DD}$, this expression reduces to

$$t_{prop} = \frac{1.6C}{k'_i(W/L)V_{DD}} \quad (4.157)$$

Similar analysis of the turn-off process yields an expression for t_{prop} identical to that in Eq. (4.157) except for $k'_i(W/L)_D$ replaced with $k'_i(W/L)_P$. The propagation delay is the average of t_{prop} and t_{off} . From Eq. (4.157), we note that to obtain lower propagation delays and hence faster operation, C should be minimized, a lighter process transconductance parameter k' should be utilized, the transistor W/L ratio should be increased, and the power-supply voltage V_{DD} should be increased. There are, of course, design trade-offs and physical limits involved in making choices for these parameter values. This subject, however, is too advanced for our present needs.

EXERCISES

- 4.45 For typical operation of a CMOS inverter, $V_{DD} = 10\text{V}$, $V_i = 0.2\text{V}$, $C = 10\text{fF}$, $k'_i(W/L) = 10\text{A/V}^2$, $k'_o(W/L) = 10\text{A/V}^2$, $R_L = 10\text{M}\Omega$, and $f = 10\text{MHz}$. Calculate the propagation time, t_{prop} , and the output rise and fall times, t_{rise} and t_{fall} .
- 4.46 For the CMOS inverter of Exercise 4.45, when is turned off? Assume typical operating conditions. Ans: 6 ns

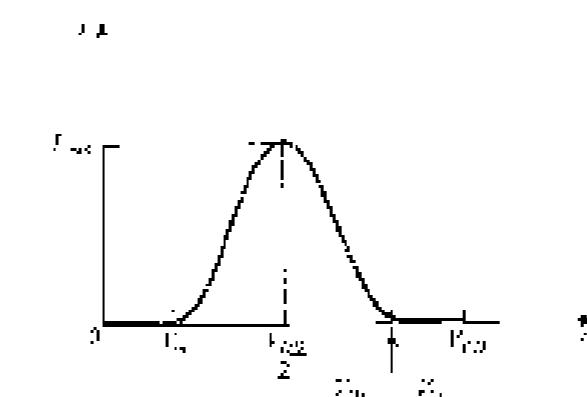


FIGURE 4.58 The current in the CMOS inverter increases the input voltage.

4.10.4 Current Flow and Power Dissipation

As the CMOS inverter is switched, current flows through the series connection of Q_X and Q_Y . Figure 4.58 shows the inverter current as a function of t . We note that the current peaks at the switching threshold, $V_{in} = v_i = v_o = V_{DD}/2$. This current gives rise to dynamic power dissipation in the CMOS inverter. However, a more significant component of dynamic power dissipation results from the current that flows in Q_X and Q_Y when the inverter is loaded by a capacitor C .

An expression for this latter component can be derived as follows. Consider once more the circuit in Fig. 4.57(a). At $t = 0$, $v_i = V_{DD}$, and the energy stored on the capacitor is $\frac{1}{2}CV_{DD}^2$. At $t = 0$, v_o goes high to V_{DD} , Q_Y turns off, and Q_X turns on. Transistor Q_X then discharges the capacitor, and at the end of the discharge interval, the capacitor voltage is reduced to zero. Thus during the discharge interval, energy of $\frac{1}{2}CV_{DD}^2$ is removed from C and dissipated in Q_X . Next consider the other half of the cycle when v_i goes low to zero. Transistor Q_Y turns on, and Q_X conducts and charges the capacitor. Let the instantaneous current supplied by Q_Y to C be denoted i . This current is, of course, equaling from the power supply V_{DD} . Thus the energy drawn from the supply during the charging period will be $iV_{DD}dt = V_{DD}Idt = V_{DD}Q$, where Q is the charge supplied to the capacitor; that is, $Q = CV_{DD}$. Thus the energy drawn from the supply during the charging interval is CV_{DD}^2 . At the end of the charging interval, the capacitor voltage will be V_{DD} , and thus the energy stored in it will be $\frac{1}{2}CV_{DD}^2$. It follows that during the charging interval, half of the energy drawn from the supply, CV_{DD}^2 , is dissipated in Q_Y .

From the above, we see that in every cycle, $\frac{1}{2}CV_{DD}^2$ of energy is dissipated in Q_X and $\frac{1}{2}CV_{DD}^2$ dissipated in Q_Y , for a total energy dissipation in the inverter of CV_{DD}^2 . Now, if the inverter is switched at the rate of f cycles per second, the dynamic power dissipation in it will be

$$P_d = fCV_{DD}^2 \quad (4.158)$$

Observe that the frequency of operation is related to the propagation delay: The lower the propagation delay, the higher the frequency at which the circuit can be operated and, according to Eq. (4.158), the higher the power dissipation in the circuit. A figure of merit or a quality measure of the particular circuit technology is the delay-power product (DfP).

$$DfP = f_{\text{prop}} \quad (4.159)$$

The delay-power product tends to be a constant for a particular digital circuit technology and can be used to compare different technologies. Obviously the lower the value of DP the more effective is the technology. The delay-power product has the units of joules, and is an effective measure of the energy dissipated per cycle of operation. This is for CMOS where much of the power dissipation is dynamic; we can take DP as simply Cf^2V^2 .

EXERCISES

- 444 Third-order nonlinearity in Raman scattering from single-walled carbon nanotubes, *J. Appl. Phys.*, Vol. 108, p. 013504

445 Effect of surface roughness on Faraday's law and Hall effect in single-walled carbon nanotubes, *Phys. Rev. B*, Vol. 77, p. 115426

446 Effect of surface roughness on the current-voltage characteristics of single-walled carbon nanotubes, *Phys. Rev. B*, Vol. 77, p. 115427

447 Effect of surface roughness on the conductance of single-walled carbon nanotubes, *Phys. Rev. B*, Vol. 77, p. 115428

448 Conductance of C60/Si/SiO₂ stack having two SiO₂ gates fabricated with 1.2-μm CMOS technology, *Int. J. Nanosci.*, Vol. 10, p. 111

449 Conductance of C60/Si/SiO₂ stack having two SiO₂ gates, *Int. J. Nanosci.*, Vol. 10, p. 112

4.10.5 Summary

In this section, we have provided an introduction to CMOS digital circuits. For convenient reference, Table 4.6 provides a summary of the important characteristics of the inverter. We shall return to this subject in Chapter 14, where a variety of CMOS logic circuits are studied.

4.11 THE DEPLETION-TYPE MOSFET

In this section we briefly discuss another type of MOSFET, the depletion-type MOSFET. Its structure is similar to that of the enhancement-type MOSFET with one important difference. The depletion MOSFET has a physically unjoined channel. Thus an n -channel depletion-type MOSFET has an n -type silicon region connecting the n^+ source and the n^+ drain regions at the top of the p -type substrate. Thus if a voltage V_{DS} is applied between drain and source, a current I_D flows for $V_{GS} = 0$. In other words, there is no need to induce a channel, unlike the case of the enhancement MOSFET.

The channel depth and hence its conductivity can be controlled by v_{ds} in exactly the same manner as in the enhancement-type device. Applying a positive v_{ds} enhances the channel by attracting more electrons into it. Here, however, we also can apply a negative v_{ds} , which causes electrons to be repelled from the channel, and thus the channel becomes shallower and its conductivity decreases. This negative v_{ds} is said to deplete the channel of its charge carriers, and this mode of operation (negative v_{ds}) is called depletion mode. As the magnitude of v_{ds} is increased in the negative direction, a value is reached at which the channel is completely depleted of charge carriers and is reduced to zero even though v_g

TABLE 4-6 Summary of Important Characteristics of the EML's Logic Insert

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- c. 30 percent low income working) (Fig. 124).

$$V_{DyA} = \sqrt{\left[\sum_{j=1}^J W_j \right] (V_{Dy} - V_{dy})}$$

- Which is the most popular language? (Fig. 4.3)

$$V_{D,n} = V \left[\sqrt{\frac{W}{\pi}} \left(\sum_{j=1}^{W-1} (V_{D,n} - V_0) \right) \right]$$

Gate Threshold Voltage

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$$V_{\beta} = \frac{\alpha(V_{\text{max}} - V_{\text{min}}) + V_{\text{min}}}{\beta + \epsilon}$$

20

$$r = \frac{V_0(W/L_0)}{\sqrt{W/L_0}}$$

Suscepting Current and Power Dissipation (Fig. 4.5)

$$I_{\text{pass}} = \frac{1}{2} k' \left(\frac{W}{d} \right) \left[\frac{V_{\text{eff}}}{n} - V_r \right]$$

$E_{\gamma} \approx 50$ GeV.

Noise Margin (Fig. 4.56)

For matched devices, that is, $\rho_1 \sqrt{\frac{P_{S1}}{L_{S1}}} = \rho_2 \sqrt{\frac{P_{S2}}{L_{S2}}}$

$$U_0 = U_{\text{imp},0}$$

$$V_{\pm} = \frac{1}{2}(\beta V_{\pm 2} + 2\gamma)$$

$$V_{\text{eff}} = \frac{1}{2} \Omega^2 V_{\text{ext}}(r) \sin^2(\theta)$$

$$\delta M_0 = \delta M_1 \approx \frac{1}{2} \delta V_{200} + \frac{1}{2} V$$

Evaluation Policy Fig. 5.5

$E_{\text{kin}} V = 0.2 V_{\text{RF}}$

$$I_{\text{max}} = \frac{1.6C}{S_1 W/L_1 V_s}$$

$$I_{\text{SUS}} \approx \frac{1.5C}{(C + k/L) \sqrt{V}}$$

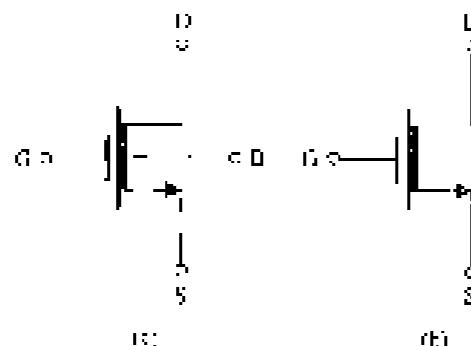


FIGURE 4.59 (a) Circuit symbol for the *n*-channel depletion-type MOSFET. (b) Simplified circuit symbol applicable for the case the substrate (B) is connected to the source (S).

may be still applied. This negative value of v_{GS} is the threshold voltage of the *n*-channel depletion-type MOSFET.

The description above suggests (correctly) that a depletion-type MOSFET can be operated in the enhancement mode by applying a positive v_{GS} and in the depletion mode by applying a negative v_{GS} . The i_D-v_{DS} characteristics are similar to those for the enhancement device except that V_t of the *n*-channel depletion device is negative.

Figure 4.59(b) shows the circuit symbol for the *n*-channel depletion-type MOSFET. This symbol differs from that of the enhancement-type device in only one respect: There is a shaded area next to the vertical line representing the channel, signifying that a physical channel exists. When the body (B) is connected to the source (S), the simplified symbol shown in Fig. 4.59(a) can be used.

The i_D-v_{DS} characteristics of a depletion-type *n*-channel MOSFET for which $V_t = -4$ V and $k'_n W/L = 2 \text{ mA/V}^2$ are described in Fig. 4.60(b). (These numbers are typical of discrete devices.) Although these characteristics do not show the dependence of i_D on v_{GS} in saturation, such dependence exists and is identical to the case of the enhancement-type device. Observe that because the threshold voltage V_t is negative, the depletion NMOS will operate in the triode region as long as the drain voltage does not exceed the gate voltage by more than $|V_t|$. For it to operate in saturation, the drain voltage must be greater than the gate voltage by at least $|V_t|$ volts. The case in Fig. 4.61 shows the relative levels of the terminal voltages of the depletion NMOS transistor for the two regions of operation.

Figure 4.60(c) shows the i_D-v_{GS} characteristics in saturation, indicating both the depletion and enhancement modes of operation.

The current-voltage characteristics of the depletion-type MOSFET are described by the equations identical to those for the enhancement device except that, for an *n*-channel depletion device, V_t is negative.

A special parameter for the depletion MOSFET is the value of drain current obtained in saturation with $v_{GS} = 0$. This is denoted i_{DS0} and is indicated in Fig. 4.60(b) and (c). It can be shown (p.

$$i_{DS0} = \frac{1}{2} k'_n \frac{W}{L} V_t^2 \quad (4.160)$$

Depletion-type MOSFETs can be fabricated on the same IC chip as enhancement-type devices, resulting in circuits with improved characteristics, as will be shown in a later chapter.

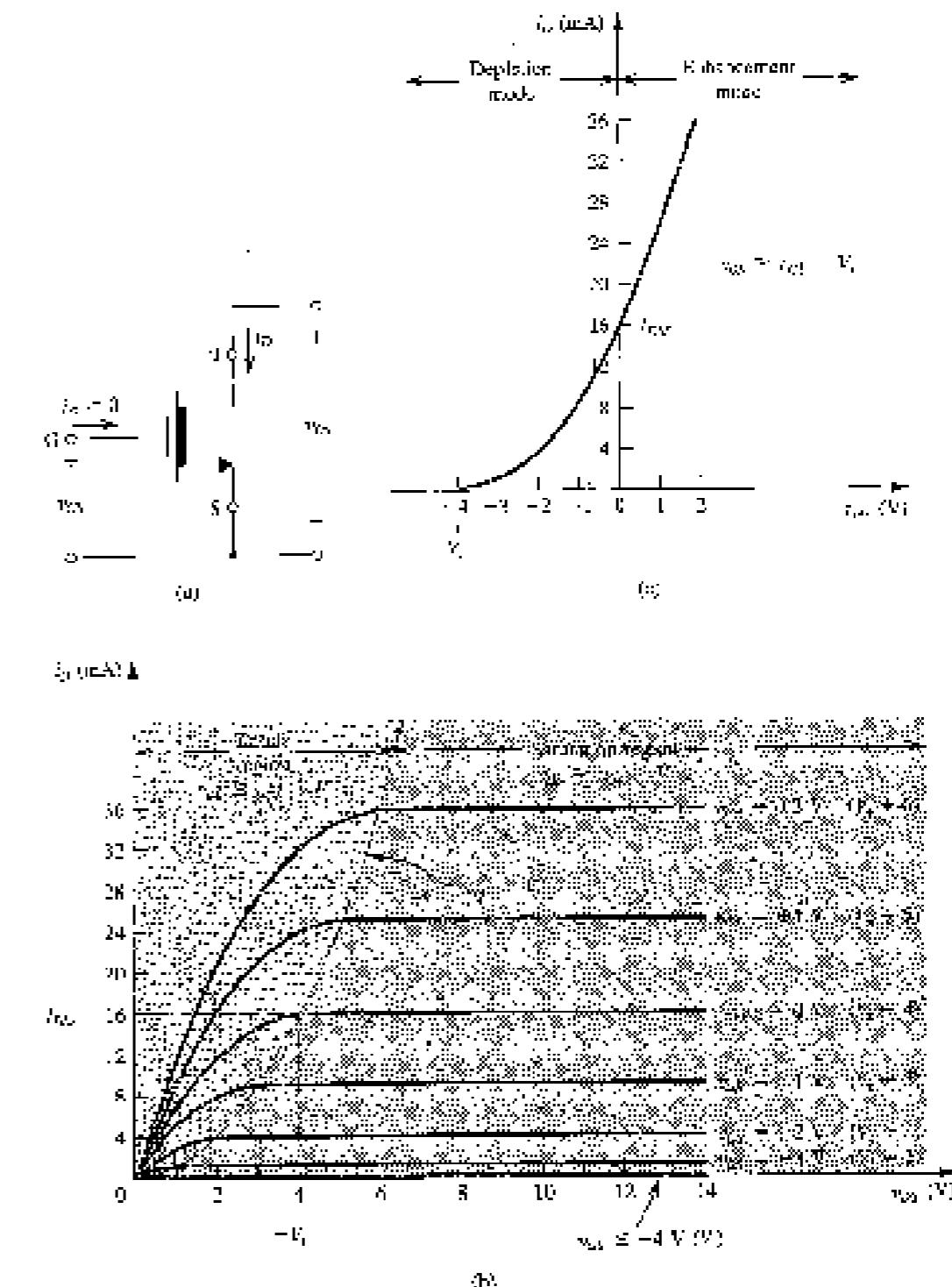


FIGURE 4.60 The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which $V_t = -4$ V and $k'_n (W/L) = 2 \text{ mA/V}^2$: (a) circuit with current and voltage polarities indicated; (b) drain i_D characteristics; (c) the i_D-v_{GS} characteristic in saturation.

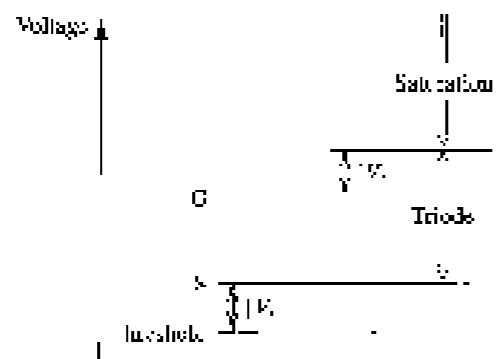


FIGURE 4.61 The drain-to-source voltage of a depletion-type NMOS transistor for operation in the triode and the saturation regions. The overshadowed region is the enhancement mode (V_{gs} is positive).

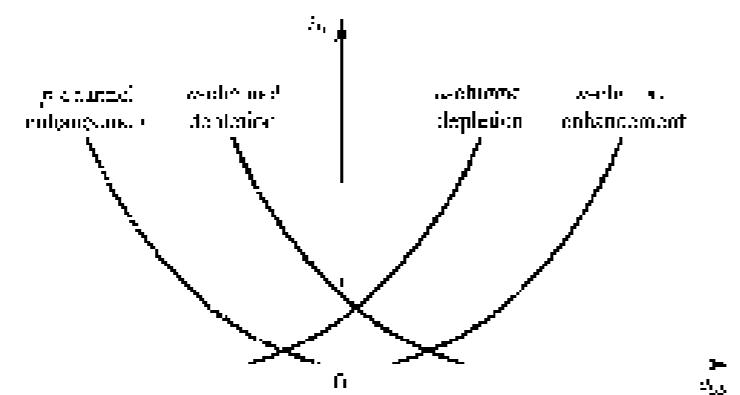


FIGURE 4.62 Sketches of the i_d - v_{ds} characteristics for MOSFETs of enhancement and depletion types, of both polarities (operating in saturation). Note that the characteristic curves intersect the v_{ds} axis at 0. Also note that for generality we have taken values of $|V_g|$ as shown for n-channel and p-channel devices.

In the above, we have discussed only *n*-channel depletion devices. Depletion PMOS transistors are available in discrete form and operate at a manner similar to their *n*-channel counterparts except that the polarities of all voltages (including V_g) are reversed. Also, in a *p*-channel device, i_d flows from source to drain, entering the source terminal and leaving by way of the drain terminal. As a summary, we show in Fig. 4.62 sketches of the i_d - v_{ds} characteristics of enhancement and depletion MOSFETs of both polarities (operating in saturation).

EXERCISES

- 4.6.1 A depletion-type NMOS transistor with $V_t = -3\text{ V}$, $k = 2\text{ mA/V}^2$, and $\lambda = 0.05\text{ mA/V}^2$ is required to operate in the saturated region with $V_{ds} = 1\text{ V}$. What is the required value of V_g ? (Ans: -5 V .)

- 4.6.2 The characteristics of a MOSFET in Fig. 4.61 are $k = 1\text{ mA/V}^2$ and $V_t = -2\text{ V}$. What is the value of V_{ds} (neglecting the effect of drain-to-gate voltage) if $i_d = 2\text{ mA}$? Find the voltage that will produce the zero-current condition.



FIGURE E4.51

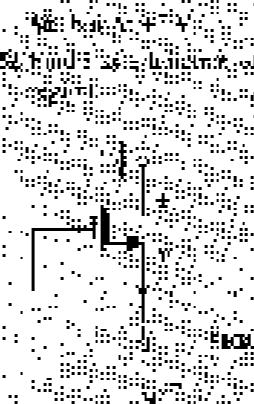


FIGURE E4.52

4.12 THE SPICE MOSFET MODEL AND SIMULATION EXAMPLE

We conclude this chapter with a discussion of the models that SPICE uses to simulate the MOSFET. We will also illustrate the use of SPICE in the simulation of the CS amplifier circuit.

4.12.1 MOSFET Models

To simulate the operation of a MOSFET circuit, a simulator requires a mathematical model to represent the characteristics of the MOSFET. The model we have derived in this chapter to represent the MOSFET is a simplified or first-order model. This model, called the square-law model because of the quadratic i - v relationship in saturation, works well for resistors with relatively long channels. However, for devices with short channels, especially submicron, dangerous, many physical effects that we have neglected come into play, with the result that the derived first-order model no longer accurately represents the actual operation of the MOSFET.

The simple square-law model is useful for understanding the basic operation of the MOSFET as a circuit element and is indeed used to obtain approximate pentodiode-pnpot circuit designs. However, more elaborate models, which account for short-channel effects, are required to predict the performance of integrated circuits with a certain degree of precision prior to fabrication. Such models have indeed been developed and continue to be refined to more accurately represent the higher-order effects in short-channel transistors through a mix of physical relationships and empirical data. Examples include the Berkley short-channel MOSFET model (BSIM) and the HKV model, popular in Europe. Currently, semiconductor manufacturers rely on such sophisticated models to accurately represent the fabricated process. These manufacturers select a MOSFET model and then extract the values for the corresponding model parameters using both their knowledge of the details of the fabrication process and extensive measurements on a variety of fabricated MOSFETs. A great deal of effort is expended on extracting the model parameter values. Such effort pays off in fabricating circuits exhibiting performance very close to that predicted by simulation, thus reducing the need for costly redesign.

Although it's beyond the scope of this book to delve into the subject of MOSFET modeling and short-channel effects, it is important that the reader be aware of the limitations of the square-law model and of the availability of more accurate but, unfortunately, more complex MOSFET models. In fact, the power of computer simulation is once again apparent when one has to use more complex model models in the analysis and design of integrated circuits.

SPICE-based simulators like PSpice provide the user with a choice of MOSFET models. The corresponding SPICE model parameters (which are user-specified by the semiconductor manufacturer) include a parameter, called LEVEL, which selects the MOSFET model to be used by the simulator. Although the value of this parameter is not always indicative of the accuracy nor of the complexity of the corresponding MOSFET model, LEVEL = 1 corresponds to the simplest first-order model (called the Shichman-Hodges model) which is based on the square-law MOSFET equations presented in this chapter. For simplicity, we will use this model to illustrate the description of the MOSFET model parameters in SPICE and to simulate the example circuit in PSpice. However, the reader is again reminded of the need to use a more sophisticated model than the level-1 model to accurately predict the circuit performance, especially the submicron transistors.

4.12.2 MOSFET Model Parameters

Table 4.7 provides a listing of some of the MOSFET model parameters used in the Level-1 model of SPICE. The reader should already be familiar with these parameters, except for a few, which are described next.

MOSFET Diode Parameters For the two reverse-biased diodes formed by each of the source and drain diffusion regions and the body (see Fig. 4.1) the saturation-current density is modeled in SPICE by the parameter JS. Furthermore, based on the parameters specified in Table 4.7, SPICE will calculate the depletion-layer (junction) capacitances discussed in Section 4.8.2 as

$$C_{DS} = \frac{C_J}{\left(1 + \frac{V_{DS}}{V_{TF}}\right)^n} AD \quad \frac{CJSW}{\left(1 + \frac{V_{DS}}{V_{TF}}\right)^{M_{SW}}} PD \quad (4.161)$$

$$C_{DS} = \frac{C_J}{\left(1 + \frac{V_{DS}}{V_{TF}}\right)^n} AS \quad \frac{CJSW}{\left(1 + \frac{V_{DS}}{V_{TF}}\right)^{M_{SW}}} PS \quad (4.162)$$

TABLE 4.7 Parameters of the SPICE-Level-1 MOSFET Model (Pspice Listing)

SPICE Parameter	Book Symbol	Description	Joints
Basic Model Parameters			
LEVEL		MOSFET model selection	
TOX	C_s	Gate-oxide thickness	μm
COX	C_g	Gate oxide capacitance, per unit area	F/m^2
HO	μ	Carrier mobility	$cm^2/V \cdot s$
KP	k'	Process transconductance parameter	A/V^2
LAMBDA	λ	Channel length modulation coefficient	V^{-1}
Threshold Voltage Parameters			
VTO	V_t	Zero-bias threshold voltage	V
GAMMA	γ	Body-effect parameter	V
NUD	N_d, N_a	Alloyed doping	cm^{-3}
PB	D_B	Surface inversion potential	V
MOSFET Diode Parameters			
JS		Ridge current at zero drain-current density	Am^2
TD		Zero-bias body-junction capacitance, per unit area over the drain/source region	F/m^2
SL		Grading coefficient, drain component	
CISW		Zero-bias body-drain capacitance, per unit length along the sidewall (per unit width of the drain/source region)	F/m
MJSW		Grading coefficient, drain sidewall component	
PR	η_0	Hot-electron build-up factor	V
MOSFET Dimension Parameters			
LD	L_s	Lateral dimension for the channel from the source/drain to P-well region	μm
WD		Side-wall Lateral L from the channel from the body along the wall	μm
MOS Gate-Capacitance Parameters			
CXAC		Gate-body overlap capacitor, per unit length	F/m
CDDO	C_{gD} /W	Gate-drain overlap capacitance, per unit channel width	F/m
CDCS	C_{gS} /W	Gate-source overlap capacitance, per unit channel width	F/m

where AD and AS are the areas while PD and PS are the perimeters of, respectively, the drain and source regions of the MOSFET. The first capacitance term in Eqs. (4.161) and (4.162) represents the depletion-layer (junction) capacitance over the bottom plate of the drain and source regions. The second capacitance term accounts for the depletion layer capacitance along the sidewall (periphery) of these regions. Both terms are expressed using the formula developed in Section 3.7.3 (Eq. 3.55). The values of AD, AS, PD, and PS must be specified by the user based on the dimensions of the device being used.

MOSFET Dimension and Gate-Capacitance Parameters In a fabricated MOSFET, the effective channel length L_{eff} is shorter than the nominal (or drawn) channel length L as specified by the designer, because the source and drain diffusing regions extend slightly

under the gate oxide during fabrication. Furthermore, the effective channel width W_{eff} of the MOSFET is shorter than the nominal or drawn channel width W because of the sideways diffusion into the channel from the body along the width. Based on the parameters specified in Table 4.7,

$$L_{\text{eff}} = L + 2L_D \quad (4.163)$$

$$W_{\text{eff}} = W - 2W_D \quad (4.164)$$

In a manner analogous to using L_{eff} to denote L_D , we will use the symbol W_{eff} to denote W_D . Consequently, as indicated in Section 4.5.1, the gate-source capacitance C_{gs} and the gate-body capacitance C_{gb} must be increased by an overlap exponent of, respectively,

$$C_{gs,\text{ov}} = W_{\text{eff}} C_{gs} \quad (4.165)$$

and

$$C_{gb,\text{ov}} = W_{\text{eff}} C_{gb} \quad (4.166)$$

Similarly, the gate-body capacitance C_{gb} must be increased by an overlap exponent of

$$C_{gb,\text{ov}} = L_{\text{eff}} C_{gb} \quad (4.167)$$

The reader may have observed that there is a built-in redundancy in specifying the MOSFET model parameters in SPICE. For example, the user may specify the values of λ_2 for a MOSFET or, alternatively, specify TOX and DQ and let SPICE compute λ_2 as TOX/DQ . Similarly, GAMMA can be directly specified, or the physical parameters that enable SPICE to determine it can be specified (e.g., NSUB). In any case, the user-specified values will always take precedence over (i.e., override) those values calculated by SPICE. As another example, note that the user has the option of either directly specifying the overlap capacitances CGBO , CGDO , and CXBO or letting SPICE compute them as $\text{CGBO} = \text{CDSO} - \text{LD}_1 \text{COX}$ and $\text{CGDO} = \text{CDSO} - \text{WD}_1 \text{COX}$.

Table 4.8 provides typical values for the Level 1 MOSFET model parameters of a modern 0.5- μm CMOS technology and, for comparison, those of an older (now obsolete) 5- μm CMOS technology. The corresponding values for the minimum channel length L_{min} , minimum channel width W_{min} , and the maximum supply voltage $V_{\text{DD}} = |V_{\text{DD}}|_{\text{max}}$ are as follows:

Technology	L	W	V_{DD}
5- μm CMOS	5 μm	12.5 μm	10 V
0.5- μm CMOS	0.5 μm	1.25 μm	2.3 V

Because of the shrinking size of modern CMOS technologies, the maximum supply voltage must be reduced to ensure that the MOSFET terminal voltages do not cause a breakdown of the oxide dielectric under the gate. The shrinking supply voltage is one of the most challenging design aspects of analog integrated circuits in advanced CMOS technologies. From Table 4.8, the reader may have observed some other trends in CMOS processes. For example, as L_{min} is reduced, the channel length modulation effect becomes more pronounced and, hence, the value of λ increases. This results in MOSFETs having smaller output resistance r_o and, therefore, smaller "intrinsic gains" (Chapter 6). Another example is the decrease in surface mobility μ in modern CMOS technologies and the corresponding increase in the ratio of μ_s/μ_b from 2.0

TABLE 4.8 Values of the Level 1 MOSFET Model Parameters for Two CMOS Technologies¹⁾

	3- μm CMOS Process		0.5- μm CMOS Process	
	NMOS	PMOS	NMOS	PMOS
EYBL	1	1	1	1
TOX	35e-9	35e-9	5.7e-9	6.4e-9
L _D	75	75	46	115
GAMMA	0.91	0.91	0.1	0.2
GAMMA	4	6.6	0.3	0.45
VTO	1	1	0.7	-0.8
PHB	0.7	0.65	0.3	0.75
ZD	0.7e-6	0.6e-6	0.05e-6	0.08e-6
IS	1e-6	1e-6	1.0e-6	5e-6
OJ	0.4e-3	0.18e-3	0.57e-3	0.92e-3
MT	0.1	0.5	0.5	0.4
CTSW	0.3e-9	0.6e-9	0.12e-9	0.11e-9
MLSW	0.5	0.5	0.4	0.35
PH	0.1	0.7	0.9	0.9
CGDO	5.2e-9	0.2e-9	0.048e-9	0.08e-9
CGBO	0.4e-9	0.1e-9	0.4e-9	0.35e-9
CXBO	0.4e-9	0.4e-9	0.1e-9	0.15e-9

¹⁾In Table 4.8, we have placed NMOS parameters to the right of their PMOS counterparts. Readers can find these pairs in the SPICE code block, which is available on the CD accompanying the book as well as online at www.soc.kit.edu/~spice/. The 3- μm CMOS pair is the 0.7- μm CMOS technology, called NMOSFET_07 and PMOSFET_07; similarly, the 5- μm CMOS pair is the 5- μm CMOS technology, as labelled NMOSFET_05 and PMOSFET_05, respectively. These two technologies are NMOS and PMOS, respectively, and NMOSFET and PMOSFET are used in conjunction with NMOSFET_05 and PMOSFET_05 to body connect to the source and drain MOSFETs, respectively, in a body-connected pair.

close to λ . The impact of λ and other factors on the design of integrated circuits in advanced CMOS technologies are discussed in Chapter 6 (see in particular Section 6.2).

When simulating a MOSFET circuit, the user needs to specify both the values of the model parameters and the dimensions of each MOSFET in the circuit being simulated. At least, the channel length L and width W must be specified. The areas AS and AS and the perimeters PS and PS need to be specified for SPICE to model the body-contact capacitances (otherwise, zero capacitances would be assumed). The exact values of these geometry parameters depend on the actual layout of the device (Appendix A). However, to estimate these dimensions, we will assume that a metal contact is to be made to each of the source and drain regions of the MOSFET. For this purpose, typically, these contact regions must be extended past the end of the channel (i.e., to the L -direction in Fig. 4.1) by at least $2.75L_{\text{min}}$. Thus, the minimum area and perimeter of a drain/source diffusion region with a contact are, respectively,

$$\text{AD} = \text{AS} = 2.75L_{\text{min}} W \quad (4.168)$$

and

$$\text{PD} = \text{PS} = 2 \times 2.75L_{\text{min}} W \quad (4.169)$$

Unless otherwise specified, we will use Eqs. (4.168) and (4.169) to estimate the dimensions of the drain/source regions in our examples.

Finally, we note that SPICE computes the values for the parameters of the MOSFET small-signal model based on the dc operating point (bias point). These are then used by SPICE to perform the small-signal analysis (the analysis).

THE CS AMPLIFIER

In this example, we will use PSpice to compute the frequency response of the CS amplifier whose circuit schematic is shown in Fig. 4.63.¹ Observe that the MOSFET has its source and body connected in series to cancel the body effect. We will assume a 0.5 μm CMOS technology for the MOSFET and use the SPICE level-1 model parameters listed in Table 4.8. We will also assume a source-degeneration resistance $R_{S1} = 10\text{ k}\Omega$, a load resistance $R_L = 50\text{ k}\Omega$, and bypass and coupling capacitors of $10\text{ }\mu\text{F}$. The targeted specifications for this CS amplifier are a midband gain $A_V = 10\text{ V/V}$ and a maximum power consumption $P = 1.5\text{ mW}$. As should always be the case with computer simulation, we will begin with an approximate pencil-and-paper design. We will then use PSpice to fine tune our design and investigate the performance of the final design. To this way, maximum advantage and insight can be obtained from simulation.

With a 3.3-V power supply, the drain current of the NMOSFET must be limited to $I_D = P/V_{DD} = 1.5\text{ mW}/3.3\text{ V} = 0.45\text{ mA}$ to avoid the power consumption specification. Choosing $V_{GS} = 0.3\text{ V}$ (typical value in low voltage designs) and $V_{DS} = V_{DD}/3$ (to achieve a large signal swing at the output), the MOSFET can now be sized as

$$\frac{W}{L} = \frac{I_D}{\frac{1}{2}K_nV_{GS}^2(1+AV_{DS})} = \frac{0.45 \times 10^{-3}}{\frac{1}{2}(170.1 \times 10^{-6})(0.3)^2(1+0.1(1.1))} \approx 53 \quad (4.76)$$

where $K_n = \mu_nC_{ox} = 170.1\text{ mA/V}^2$ (from Table 4.8). Here, L_{eff} rather than L is used to more correctly estimate I_D . The effect of using W/L rather than W is much less important because typically $W \ll L_{eff}$. Thus, choosing $L = 0.6\text{ }\mu\text{m}$ results in $L_{eff} = 1 - 2L_{eff} = 0.4\text{ }\mu\text{m}$ and $W = 33.2\text{ }\mu\text{m}$. Note that we chose L slightly larger than L_{eff} . This is a common practice in the design of analog ICs to minimize the effects of fabrication nonidealities on the actual value of L . As we will study in later chapters, this is particularly important when the circuit performance depends on the matching between the dimensions of ten or more MOSFETs (e.g., in the current-mirror circuits we will study in Chapter 5).

Next, R_L is calculated based on the desired voltage gain:

$$A_V^2 = g_m(R_L \parallel R_{SD}) = 10\text{ V/V} = R_L \approx 4.3\text{ k}\Omega \quad (4.77)$$

where $g_m = 3.0\text{ mA/V}$ and $r_o = 22.2\text{ k}\Omega$. Hence, the output bias voltage is $V_{DS} = V_{DD} - I_D R_D = 1.29\text{ V}$. An $R_S = (V_{DS} - V_{GS})/I_D = 63\text{ k}\Omega$ is needed to bias the MOSFET and $V_{GS} = V_{DD}/3$. Finally, resistors $R_{C1} = 2\text{ M}\Omega$ and $R_{C2} = 1.5\text{ M}\Omega$ are chosen to set the gate bias voltage at $V_{GS} = I_D R_S + V_{DD}/3 = 1.29\text{ V}$. Using large values for these gate resistors ensures that both their power consumption and the loading effect on the input signal source are negligible. Note that we neglected the body effect in the expression for V_{GS} to simplify our hand calculations.

We will now use PSpice to verify our design and investigate the performance of the CS amplifier. We begin by performing a bias-point simulation to verify that the MOSFET is properly

¹The reader is reminded that the Circuits schematics and the corresponding SPICE simulations for all SPICE examples in this book can be found on the text's CD as well as on its website (www.ee.wustl.edu/~chiu/). In these schematics (as shown in Fig. 4.63), we used variable port names to enter the values of the various circuit components (including the dimensions of the MOSFET). This will allow the reader to investigate the effect of changing component values by simply changing the corresponding variable values.

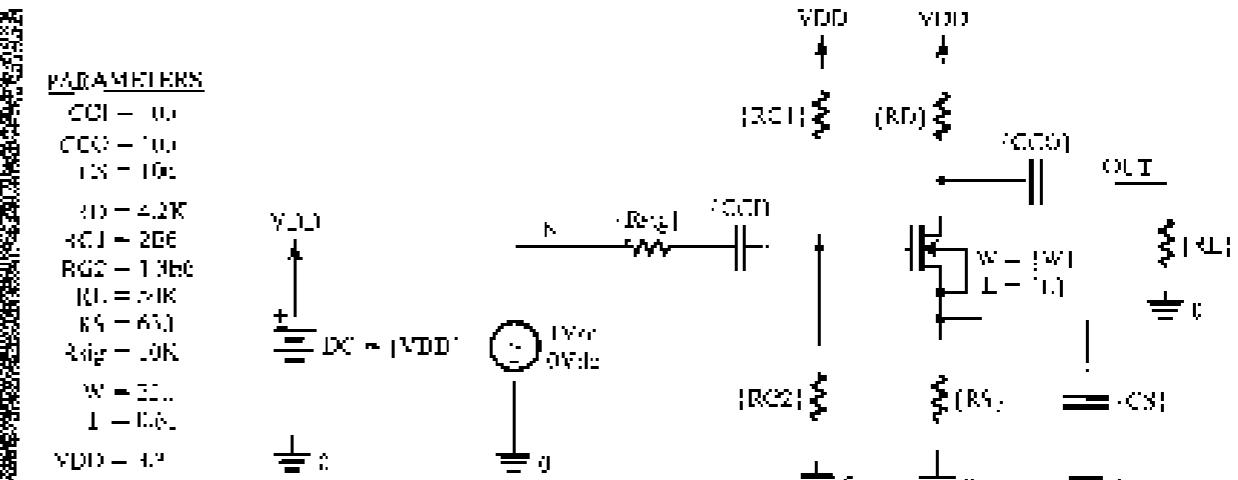


FIGURE 4.63 Capture schematic of the CS amplifier from Example 4.14.

biased in the saturation region and that the voltages and currents are within the design specifications. Based on this simulation, we will increase the value of R_S to 22.2 Ω to limit I_D to about 0.45 mA. Next to measure the ratio of $g_m A_V$, and the 3-dB frequencies f_L and f_H , we apply a 1-V ac voltage at the input, perform full ac-analysis simulation, and plot the output voltage magnitude (in dB) versus frequency as shown in Fig. 4.64. This corresponds to the magnitude response of the CS amplifier because we chose a 1-V rms input signal.² Accordingly, the midband gain is about 9.55 V/V and the 3-dB bandwidth is $BW = f_H - f_L = 123.1\text{ MHz}$. Figure 4.64 further shows that the gain begins to roll off at about 200 Hz but flattens out against about 10 Hz. This flattening in the gain at low frequencies is due to a real transresistor AV_{DS} ³ introduced in the transfer function of the amplifier by R_D together with C_D . This zero occurs at a frequency $f_T = 1/(2\pi R_D C_D) = 27.3\text{ Hz}$, which is typically between the break frequencies f_L and f_H defined in Section 4.9.3 (Fig. 4.52). So, let us now verify this phenomenon by simulating the CS amplifier with a $C_D = 0\text{ pF}$, removing C_D in order to move f_T to infinity and remove its effect. The corresponding log-frequency response is plotted also in Fig. 4.64. As expected, with $C_D = 0$, we do not observe any flattening in the low-frequency response of the amplifier, which now looks similar to that in Fig. 4.52. However, because the CS amplifier now includes a source resistance R_S , it has dropped by a factor of 2.6. This factor is approximately equal to $(1 + g_m R_S)$, as expected from our study of the CS amplifier with a source-degeneration resistance in Section 4.7.4. Note that the bandwidth BW is increased by approximately the same factor as the drop in $g_m A_V$. As we will learn in Chapter 6 when we study negative feedback, the source degeneration resistor R_S provides negative feedback, which allows us to trade off gain for wider bandwidth.

²The reader should not be confused about the use of a such a large-signal amplitude. Recall (see Eq. 4.29.1) that it is a small-signal AC simulation, SPICE runs first the small-signal equivalent circuit (at the bias point) and then analyzes this linear circuit. Such an analysis can, of course, be done with C_D as a real capacitor. However, a 1-V ac input is convenient because the resulting ac output corresponds to the voltage gain of the circuit.

³ Readers who have not yet studied AV_{DS} and r_o can either refer to Appendix E or skip these two sentences.

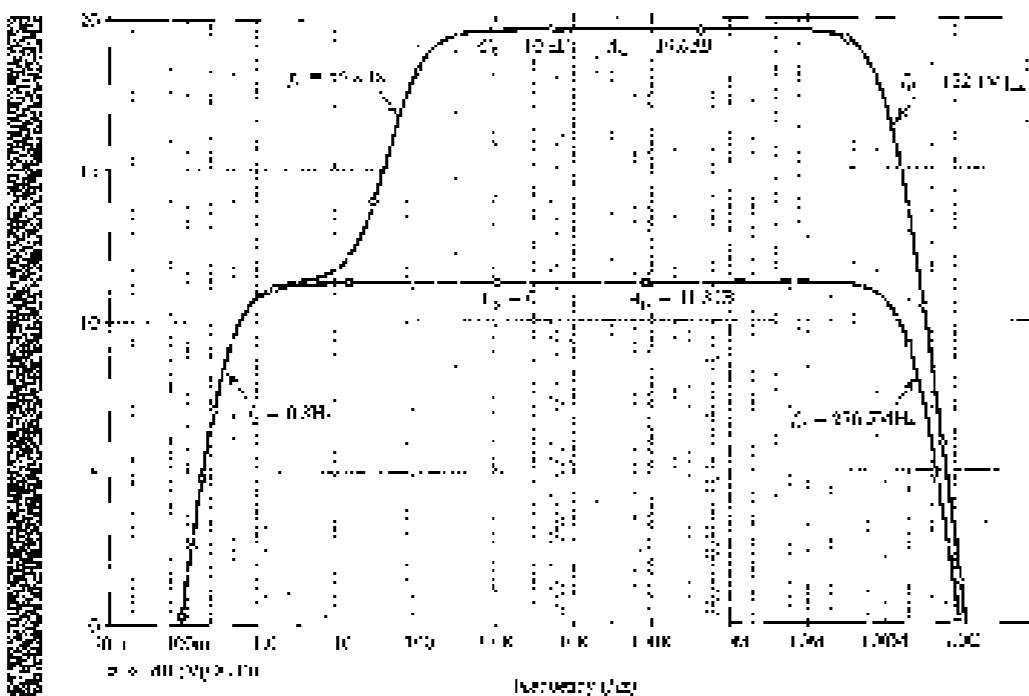


FIGURE 4.64 Frequency response of the CS amplifier (Example 4.6) with $C_3 = 10\text{ pF}$ and $C_2 = 0$ (i.e., grounded).

To conclude this example, we will demonstrate the improved bias stability achieved when a source degeneration R_s is used (see the discussion in Section 4.3.2). Specifically, we will change (in the MOSFET level-1 model of the NMOS/PNP) the value of the zero-threshold voltage parameter $V_{TH} \approx \pm 0.5\text{ V}$ and perform a two-point simulation in PSPice. Table 4.9 shows the corresponding variations in I_D and V_{DS} for the case of a load $R_L = 300\Omega$. For the case without source degeneration, we use an $R_s = 0$ in the schematic of Fig. 4.62. Furthermore, to obtain the same I_D and V_{DS} in both cases (for the nominal threshold voltage $V_{TH} = 0.7\text{ V}$), we use an $R_{DS} = 0.08\text{ M}\Omega$ to reduce V_{DS} to exceed $V_{DS} + V_{TH} = 1\text{ V}$. The corresponding variations in the bias point are shown in Table 4.9. Accordingly, we see that the source degeneration resistor makes the bias point of the CS amplifier less sensitive to changes in the threshold voltage. In fact, the reader can show from the values displayed in Table 4.9 that the variation in bias current ($\Delta I_D/I_D$) is reduced by approximately the same factor ($1 + g_m R_s$). However, unless a large bypass capacitor C_2 is used, this reduced sensitivity comes at the expense of a reduction in the midband gain (as we observed in the example when we simulated the frequency response of the CS amplifier with a $C_2 = 0$).

TABLE 4.9 Variation in the Bias Point with the MOSFET Threshold Voltage

V_{TH}	$R_s = 300\Omega$		$R_s = 0$	
	$I_D(\text{mA})$	$V_{DS}(\text{V})$	$I_D(\text{mA})$	$V_{DS}(\text{V})$
-0.6	0.36	0.962	—	—
-0.7	0.25	1.20	0.75	1.40
-0.8	0.16	1.57	0.21	2.40

SUMMARY

- The enhancement-type MOSFET is currently the most widely used semiconductor device [1] as the basis of CMOS technology, which is the most popular IC fabrication technology at this time. CMOS provides both n-channel (NMOS) and p-channel (PMOS) transistors, which increases design flexibility. The enhancement MOSFET channel length achievable with a given CMOS process is used to characterize the process. This figure has been continually reduced and is currently about 0.1 μm .
- The output voltage characteristics of the MOSFET are presented in Section 4.2 and are summarized in Table 4.1.
- Techniques for calculating MOSFET drain currents are illustrated in Section 4.3 via a number of examples.
- The large-signal operation of the basic cascode source (CS) cascode-loaded MOSFET is studied in Section 4.4. The voltage transfer characteristic is derived, both analytically and numerically, and is used to show the three regions of operation: cutoff, saturation, which are useful for the application of the MOSFET as a switch, or as a digital logic inverter; and saturation, which is the critical circuit performance. To obtain linear amplification, the transistor is biased to operate somewhere near the middle of the saturation region, and the signal is superimposed on the dc bias V_{DS} and V_{GS} , ≈ 1 . The small-signal gain is equal to the slope of the transfer characteristic at the bias point (see Fig. 4.30).
- A key step in the design of nonlinear amplifiers is to bias the transistor to operate at an appropriate point in the saturation region. A good bias design can result in the parameters of the bias point, I_D , V_{GS} , and V_{DS} , being predictable and stable, and do not vary by a large amount when the transistor is replaced by another or the same type. A variety of biasing methods suitable for discrete-circuit design are presented in Section 4.5.
- The single-signal operation of the MOSFET as well as its cut-off condition (represented in Section 4.6). A summary of the relationships for determining the values of MOSFET model parameters is provided in Table 4.9.
- Grounding one of the three terminals of the MOSFET results in a two-port network with the grounded terminal serving as a common terminal between the input and output ports. Accordingly, there are three basic MOSFET amplifier configurations: the CS configuration, which is the one which uses the enhancement MOSFET region, which has specific applications and is particularly useful as high-frequency and noise-current-drain source-multiplication switches employing a voltage buffer at the output stage of a multi-stage amplifier. Refer to the summary at the end of Section 4.7, and in particular to Table 4.10, which provides a summary and a comparison of the attributes of the various single-stage MOSFET amplifiers configurations.
- For the MOSFET high-frequency model and the formulae for determining the model parameters, refer to Table 4.5.
- The internal capacitance of the MOSFET cause the gain of VDS amplifiers to fall off at high frequencies. Also, the coupling and bypass capacitors can be used to discrete MOS amplifiers since the gain is low, but the low frequencies. The frequency band over which both sets of oscillations can be neglected, and hence over which the gain is constant, is known as the midband. The amplifier frequency response is characterized by the midband gain A_0 and the lower and upper 3-dB frequencies, f_L and f_H , respectively, and the bandwidth is $f_H - f_L$.
- Analysis of the frequency response of the cascode source amplifier (Section 4.9) shows that its high-frequency response is dominated by the interaction of the total input capacitance C_{in} and the effective resistance of the signal source, $R_{DS} r_{ds} = 1/2 + g_m R_{DS} C_{in}$. The input capacitance $C_{in} = C_{in} + (1 + g_m R_{DS} C_{in})$, which can be dominated by the second term. Thus, while C_{in} is small, its effect can be very significant because it is multiplied by a factor approximately equal to C_{in} divided r_{ds} , thus is the Miller effect.
- The CMOS digital logic gate provides a generalized implementation of the basic inversion function. Its characteristics are studied in Section 4.10 and summarized in Table 4.11.
- The depletion-type MOSFET has an unbalanced channel and thus can be operated in either the depletion or enhancement mode. It is characterized by the same equations as for the enhancement device except for having a negative V_t (positive V for depletion PMOS transistors).
- A useful technique for simulating for mixed-signal-pulse-circuit design, employing simplified device models, occupies considerable time using SPICE with some elaborate and hence more precise models is evident. For checking and fine-tuning the design before fabrication.
- Our study of MOSFET amplifiers continues in Chapter 6 and that of digital CMOS circuits in Chapter 10.

PROBLEMS

SECTION 4.1: DEVICE STRUCTURE AND PHYSICAL OPERATION

4.1 MOS technology is used to fabricate a capacitor, utilizing the gate metal line, ion and the substrate as the two electrodes. Find the area required per 1-pF plate capacitor for oxide thickness ranging from 0.5 to 1.5 μm . For a square plate of width of 10 μm , what maximum dimensions are needed?

4.2 A p-channel MOSFET having the same gate structure and channel length as the one shown in Fig. 4.1(b), but with $V_{t0} = V_{d0}$, characteristics are shown in Fig. 4.1(b). If V_d is doubled with respect to V_g , how much should the vertical axis be scaled? Is it appropriate to consider this change? Find the new constant of proportionality relating I_d and $(V_g - V_{t0})^2$. What is the range of drain-to-source voltage, V_d , corresponding to an overdrive voltage $V_{g0} - V_t$ ranging from 0.5 V to 2 V?

4.3 With the knowledge that $V_{t0} = 3$ μV , what must be the relative width (1-mosistor) and p-channel devices if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of 1.25 times magnitude?

4.4 An n-channel device has $V_{t0} = 50$ $\mu\text{A}/\text{V}^2$, $V_s = 0.8$ V, and $I_{d0} = 20$. The device is to operate as a switch for small I_{ds} , utilizing a control voltage V_{g0} in the range 0.5 V to 5 V. Find the switch's on-resistance, R_s , and closure voltage, V_c , obtained when $V_{g0} = 5$ V and $I_{d0} = 1$ mA. Recalling that $\mu_n = 0.1 \mu\text{m}$, what will L_D be for a p-channel device that provides the same performance as the n-channel device in this application?

4.5 An n-channel MOS device in a technology for which oxide thickness is 20 μm , mobility¹ and length is 1 μm , $K = 100 \mu\text{A}/\text{V}^2$, and $V_s = 0.8$ V operates in the triode region, with $I_{ds} = 1$ mA and $V_{g0} = 1.5$ V. Find the switch's on-resistance, R_s , and closure voltage, V_c , obtained when $V_{g0} = 5$ V and $I_{d0} = 1$ mA. Recalling that $\mu_n = 0.1 \mu\text{m}$, what will L_D be for a p-channel device that provides the same performance as the n-channel device in this application?

4.6 Consider a CMOS process for which $V_{t0} = 10$ μV , $I_{d0} = 15$ mA, $\mu_n = 500 \mu\text{A}/\text{V}^2$, and $V_s = 0.8$ V.

(a) Find C_{ox} and V_c .
 (b) For an NMOS transistor with $V_{g0} = 0.5$ and 0.8 gate voltage find the values of R_s , I_{ds} , and V_{ds0} needed to operate the transistor in the saturation region with a drain current of 0.5 mA. Required is a device of length of 5 μm . What value of L_D is suitable for design use?

4.7 Consider an n-channel MOSFET with $L_D = 20$ μm , $\mu_n = 650 \mu\text{A}/\text{V}^2$, $V_s = 0.8$ V, and $V_{t0} = 10$. Find the drain current

in the following cases:

- (a) $V_{g0} = 5$ V and $V_{d0} = 1$ V
- (b) $V_{g0} = 2$ V and $V_{d0} = 1.2$ V
- (c) $V_{g0} = 5$ V and $V_{d0} = 10$ V
- (d) $V_{g0} = V_{d0} = 2$ V

SECTION 4.2: CURRENT-VOLTAGE CHARACTERISTICS

4.8 Consider an NMOS transistor that is identical to except for having its L_D twice the length or twice V_{t0} . If V_{g0} , characteristics are shown in Fig. 4.1(b), should the vertical axis be scaled on the characteristics to correspond to the source electrode? If the transistor is operated in saturation with an overdrive voltage of 1.5 V, what are the resulting values?

4.9 Explain why the graph in Fig. 4.1(b) does not change as V_g is increased. Can you derive a more general, V_g -independent representation of the characteristics, as is done in Fig. 4.1?

4.10 For the transistor whose V_g , V_d characteristics are depicted in Fig. 4.2, sketch, without overdrive voltage $V_{g0} = V_g - V_t$, for $V_d > V_{ds0}$. Where is the saturation, on the graph (see Fig. 4.1), sketch, on the same diagram, the graph for a device that is identical except for having half the width.

4.11 An NMOS transistor having $V_s = 1$ V is operated in the triode region with $V_{g0} = V_t$. With $V_{ds} = 1.5$ V, it is found to have a drain current of 1 mA. What value of V_{ds0} is required at $V_{g0} = 1.5$ V? Find the corresponding resistance values obtained with a device having twice the value of L_D .

4.12 A p-channel enhancement MOSFET for which $V_s = 1$ V and $\mu_p = 0.1 \mu\text{m}^2/\text{V}\cdot\text{A}$ is to be operated in the saturation region. If I_{ds} is to be 0.2 mA, find the minimum required V_g . Repeat for $I_{ds} = 0.8$ mA.

4.13 A p-channel-channel-enhancement MOSFET is measured to have a drain current of 0.4 mA at $V_{g0} = V_t = 5$ V and $V_{ds} = 1$ mA at $V_{ds} = V_{ds0} = 5$ V. What are the values of K , V_{t0} , and V_s for this device?

4.14 For a particular IC fabrication process, the transconductance parameter $k'_t = 50 \mu\text{A}/\text{V}^2$, and $V_s = 1$ V. In an application in which $V_{g0} = V_{ds0} = 5$ V, a drain current of 0.5 mA is required of a device of length of 5 μm . What value of L_D is suitable for design use?

4.15 An NMOS transistor operating in the triode-resistance region with $V_{ds} = 1.5$ V is found to exceed 50 μA for $V_{g0} = 2$ V and 40 μA for $V_{g0} = 1$ V. What is the apparent value of threshold voltage V_t ? If $V_s = 50 \mu\text{A}/\text{V}^2$, what is the device R_s value? What current would you expect to flow with $V_{g0} = 4$ V and $V_{ds} = 0.15$ V? If the device is operated at $V_g = 4$ V, at

what value of V_d will the drain current of the MOSFET channel just reach given off and what is the corresponding drain current?

4.16 For an NMOS transistor, for which $V_s = 0.8$ V, operating with V_{g0} in the range of 1.5 V to 4 V, what is the largest value of V_{ds} for which the channel remains continuous?

4.17 An NMOS transistor, fabricated with $V_s = 100$ $\mu\text{A}/\text{V}^2$ and $V_t = 5$ μV in a technology for which $\mu_p = 50 \mu\text{A}/\text{V}^2$ and $V_s = 1$ V, is to be operated at very low values of V_{ds} in linear resistance. For this case, the drain voltage is varied from 1.5 V to 11 V, what range of resistance values can be obtained? What is the smallest V_{ds} if

- (a) the drain width is halved?
- (b) the device length is halved?
- (c) both the width and length are halved?

4.18 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "back-gate-controlled" resistor. Figure 4.18 shows such a device (circuit) from MOS technology of high precision. Show that

- (a) the relationship is given by

$$I = K \frac{V}{L} (V_g - V_t)^2$$

(b) the internal drain resistance r for a device biased to operate at $V_g = V_t + V_{ds0}$ is given by

$$r = \left(\frac{\partial I}{\partial V_{ds}} \right) = \left(\frac{K}{L} \right) \frac{V}{V_g - V_t}$$

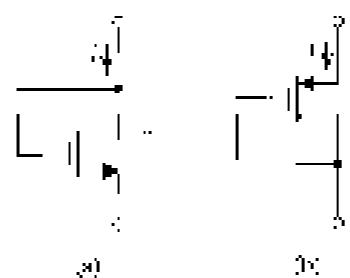


FIGURE 4.18

4.19 For a particular MOSFET operating in the saturation region, and a drain current of 1 mA is found to be 2 mA. For $V_{g0} = 1$ V and 1.2 mA, for $V_{ds} = 3$ V, what are values of V_t , V_{ds0} , and A respectively?

4.20 A particular MOSFET has $V_s = 50$ $\mu\text{A}/\text{V}^2$. For operation at 0.1 mA and 1 mA, what are the respective drain resistances? In each case, for a change in V_{ds} of 1 V, what percentage change in drain current would you expect?

4.21 In a typical IC design, which has standard channel length of 2 μm , an NMOS device with $300 \mu\text{A}/\text{V}^2$ operating at

0.5 μm is found to have an output resistance of 5.5 $\text{k}\Omega$, about $\frac{1}{2}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new drain-to-source voltage V_s for the modified device in the 10% increase in V_{ds} ?

4.22 For a particular n-channel MOS technology, in which the minimum channel length is 1 μm , the associated value of K is 0.02 $\mu\text{A}/\text{V}^2$. The particular device for which $V_s = 5 \mu\text{m}$ operates at $V_{ds} = 1$ V with drain current of 800 μA . At this bias, the drain current becomes 12 μA if V_{ds} is raised to 5 V. What percentage change does this represent? What can be done to reduce the resistance by a factor of 20?

4.23 An NMOS transistor is fabricated in a 0.8- μm process having $V_s = 130 \mu\text{A}/\text{V}^2$ and $V_t = 20$ μV of channel length $L_D = 1.6 \mu\text{m}$ ($L_D = 1.9 = 15 \mu\text{m}$, that V_s and L_D are to be increased by very low values of V_{ds} in linear resistance. For this case, the drain voltage is varied from 1.5 V to 11 V, what range of resistance values can be obtained? What is the smallest V_{ds} if

4.24 Complete the missing entries in the following table, which describes characteristics of similarly biased NMOS transistors.

MOS	V_s	V_t	I_{d0}	V_{ds0}	R_s	V_{ds}
A (V)	50	30	—	—	—	—
B (mA)	—	—	3	—	—	—
C (mA)	50	100	100	—	—	—

4.25 An NMOS transistor with $V_s = 0.01 \text{ V}^{-1}$ is operating at a drain current $I_{ds} = 1 \text{ mA}$. If the channel length is doubled, find the new values of V_s , V_t , I_{d0} , and V_{ds0} for each of the following reasons:

- (a) V_s and V_{ds0} are fixed
- (b) V_s and V_t are fixed

4.26 An n-channel MOS transistor has $45/900 \mu\text{A}/\text{V}^2$, $V_s = -1.5 \text{ V}$, and $V_t = -1002 \text{ mV}$. The gate is connected to ground and the source to +2 V. Find the drain current for $V_g = 14$ V, 1.5%, 0 V, and -5 V.

4.27 A d-channel transistor for which $V_s = 1$ V and $|V_t| = 50 \text{ V}$ operates in saturation with $I_{dsq} = 2 \text{ V}$, $V_{dsq} = -2 \text{ V}$, and $I_{ds} = 1 \text{ mA}$. The drain operating voltage V_{ds} for values between V_t and V_s is given by $V_{ds} = V_t + V_s - V_{ds}$.

4.28 In a technology for which the gate-oxide thickness is 20 μm , and the value of K , for which $= 0.5 \text{ V}^{1/2}$, if the doping level is quadrupled for the gate oxide thickness is increased to 100 μm , what does V_s become? If V_s is kept constant at $0.5 \text{ V}^{1/2}$, what value must the doping level be changed?

4.39 In a particular application, an n-channel MOSFET operates with V_{DS} in the range 6 V to 1 V. If V_T is nominally 1.6 V, $\mu_C V_A = 200 \mu A/V^2$, $L = L_0 = 0.8 \mu m$, $W_0 = 8 \mu m$, and $\lambda = 0$, if the gate-to-drain thickness is increased by a factor of 4, what does the threshold voltage become?

4.40 A p-channel transistor operates in saturation with its source voltage 3 V lower than its substrate. For $\gamma = 0.5 V^{1/2}$, $2A = 0.25 \mu A$, and $V_{DS} = -10 V$, $\lambda = 0$,

(a) Using the expression for I_D in saturation and replacing the channel length modulation coefficient by zero, deduce an expression for I_D per unit of area, in $\mu A/\mu m^2$: $I_D = (\mu_C V_A)^{1/2} 2A$ [in μA] is the per-unit change in V_D per $1^\circ C$ ($\gamma V_A / \lambda_0 V^2 T$] the temperature coefficient of V_T is $-50^\circ C/\mu V^2$, and V_{DS} and V_S]

(b) I_D decreases by 2 mA for every $1^\circ C$ rise in temperature. Given the temperature coefficient of V_A , find results in I_D decreasing by 0.25% when the NMOS transistor with $V_T = 1 V$ is operated at $V_{DS} = 5 V$.

4.41 Various NMOS and PMOS transistors (one each) in saturation, as shown in the table at the bottom of the page. For each transistor, find the value of $\mu_C V_A$ and V_T that apply and complete the table, with V in volts, R in μA , and $\mu_C V_A R$ in $\mu A/V^2$.

4.42 All the transistors in the circuits shown in Fig. P4.35 have the same values of $|V_T|$, K , W/L , and λ . Moreover, λ is negligibly small. Q1 operates in saturation at $V_D = 7$ and $V_{DS} = V_{GS} = 1 V$. Find the voltages V_1 , V_2 , V_3 , and V_4 if $V_T = 1 V$ and $I = 7 \mu A$. How does K affect V_1 ? To be maximized I stays with each drain connection while minimizing saturation? What is the largest resistor that can be placed in series with each gate? If the circuit requires a minimum of 2 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each NMOSFET source while ensuring saturated mode operation of each transistor at $I_D = I$? In the latter limiting situation, what do V_1 , V_2 , V_3 , and V_4 become?

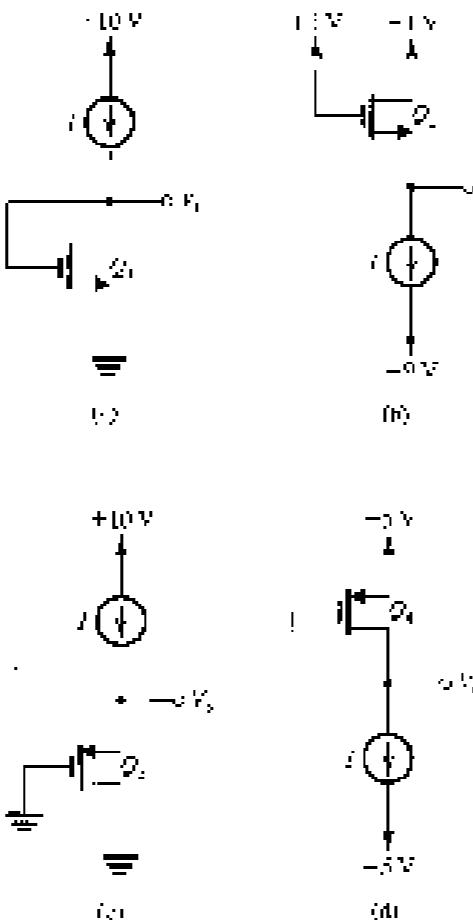


FIGURE P4.35

SECTION 4.3: MOSFET CIRCUITS AT DC

4.43 Design the circuit of Fig. 4.20 to establish a drain current of 1 mA and a drain voltage of 10 V. The MOSFET has $V_T = 1 V$, $\mu_C V_A = 100 \mu A/V^2$, $L = 2 \mu m$, and $W = 100 \mu m$.

Case	Transistor	V_{GS}	V_{DS}	V_{GS}	Type	Mode	V_{GS}	V_{DS}
a	1	0	2	5	NMOS	saturation	0.5 V	10 V
	1	0	4	5				
b	2	5	3	-1.5	PMOS	saturation	-0.5 V	10 V
	2	5	2	-0.5				
c	3	5	3	4	NMOS	saturation	0.5 V	10 V
	3	5	2	0				
d	4	-2	0	0	PMOS	saturation	-0.5 V	10 V
	4	-1	0	1				

4.45 Consider the circuit of Fig. P4.12. For ϕ and ϕ_2 have $V_T = 0.6 V$, $\mu_C V_A = 200 \mu A/V^2$, $L = L_0 = 0.8 \mu m$, $W_0 = 8 \mu m$, and $\lambda = 0$,

(a) Find the value of K required to establish a drain current of $0.2 \mu A$ in Q_1 .

(b) Find R_1 and a new value for R_2 so that Q_2 operates in the saturation region with a current of $0.5 \mu A$ and a drain voltage of $1 V$.

4.46 The PMOS transistor in the circuit of Fig. P4.36 has $V_T = 0.1 V$, $\mu_C V_A = 60 \mu A/V^2$, $L = 1.5 \mu m$, and $\lambda = 0$. Find the values required for R and R_1 in order to establish a drain current of $11.5 \mu A$ and a drain voltage $V_D = 2.5 V$.

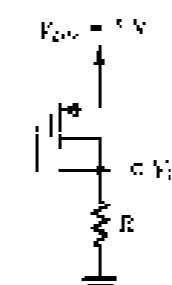


FIGURE P4.36

Find the required values of K with the value of O_1 , O_2 , and O_3 to obtain the voltage and current values indicated.

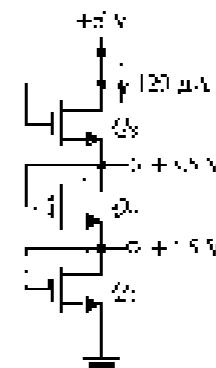


FIGURE P4.37

4.47 Consider the circuit of Fig. 4.23(a). In Example 4.5 it was found that when $V_T = 1 V$ and $V_D(VGS) = 1 mV/V^2$, the drain current of Q_1 and drain voltage of Q_2 is $1.5 V$. If the transistor is replaced with another having $V_T = 2 V$ and $V_D(VGS) = 2 mV/V^2$, find the new values of I_D and V_D . Comment on how relevant (or irrelevant) the circuit is to changes in device parameters.

4.48 Using an enhancement-type PMOS transistor with $V_T = 1.5 V$, $\mu_C V_A = 1 \text{ mA/V}^2$, and $A = 3$, design a circuit that resembles the in Fig. 4.23(a). Using a 10-V supply design for a pair of logic at 1-V and sum current of $0.5 \mu A$, and a drain voltage of $4 V$. Find the values of R_1 and R_2 .

4.49 In the NMOS circuit in Fig. P4.41 has $V_T = 1 V$, $\lambda = 100 \mu A/V^2$, and $\lambda = 0$. Find the required values of R_1 and R_2 so that when $\phi = V_{DD} = 45 V$, $i_1 = 30 \mu A$, and $i_2 = 30 \mu A$.

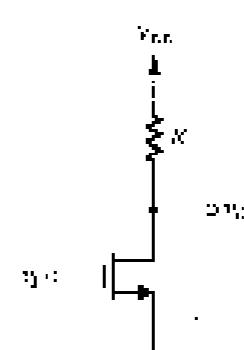


FIGURE P4.41

4.50 The NMOS transistors in the circuit of Fig. P4.39 have $V_T = 1 V$, $\mu_C V_A = 120 \mu A/V^2$, $\lambda = 0$, and $L = L_0 = 1 \mu m$.

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4.42 In the circuit shown in Fig. P4.42, transistors are characterized by $V_T = 1\text{ V}$, $k'(WL) = 1\text{ mA/V}^2$, and $\lambda = 0$.

- Find the labeled voltages V_1 if $V_{DD} = V_S$.
- In each of the circuits, suppose a current source will be replaced by the transistor with a load current equal to that of I_D . Assume $\lambda = 0$. While using resistors specified in the tables provided in Appendix G, find the new values of V_1 or V_2 .

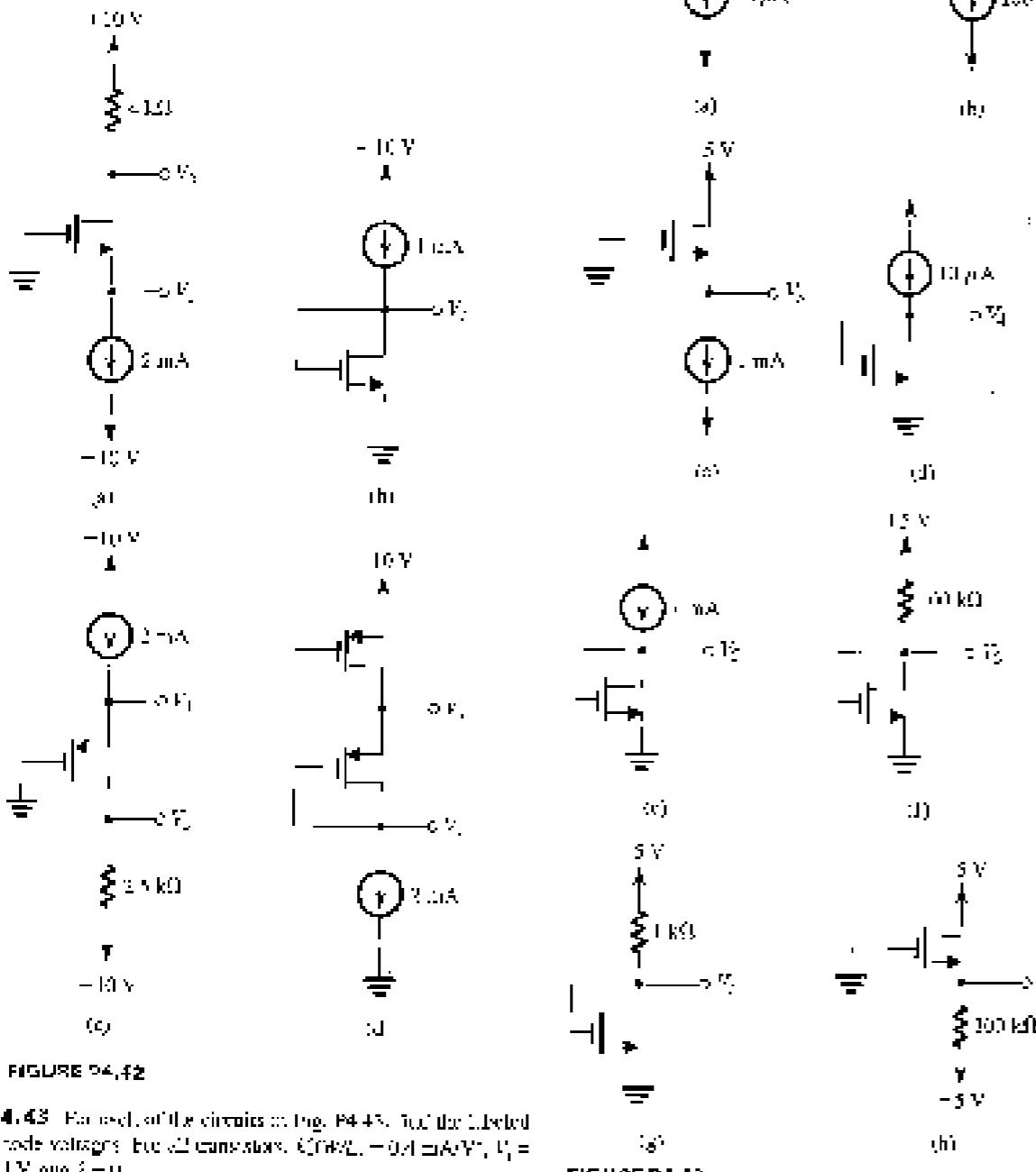


FIGURE P4.42

4.43 For each of the circuits in Fig. P4.43, find the labeled node voltages for all transistors. $C_{ox}/L = 0.1\text{ fF}/\mu\text{m}$, $V_T = 1\text{ V}$, and $\lambda = 0$.

FIGURE P4.43

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4.44 For each of the circuits shown in Fig. P4.44, find the labeled node voltages. The NMOS transistors have $V_T = 1\text{ V}$ and $k'(WL) = 2\text{ mA/V}^2$. Assume $\lambda = 0$.

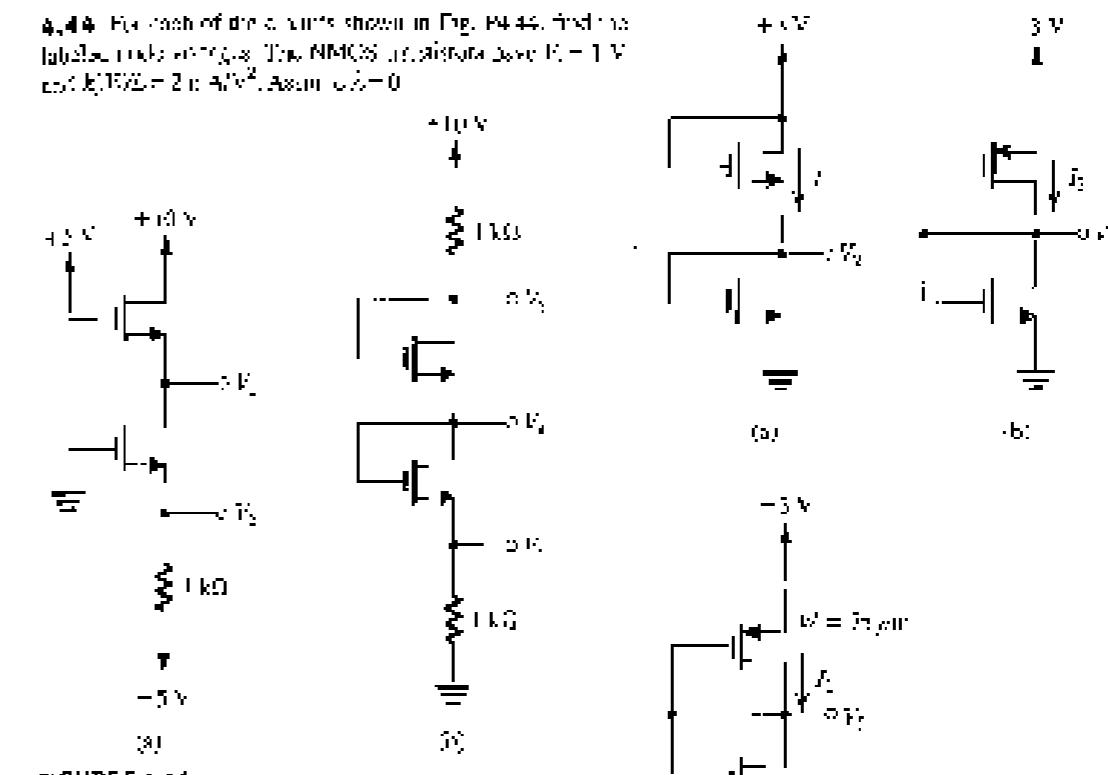


FIGURE P4.44

*4.45 For the PMOS transistor in the circuit shown in Fig. P4.45, $V_T = 0.5\text{ mA/V}^2$, $WL = 25$, and $V_{DD} = 1\text{ V}$. For $I = 100\mu\text{A}$, find the voltages V_{DS} and V_{GS} for $R = 0$, $10\text{ k}\Omega$, $1\text{ k}\Omega$, and $100\text{ }\Omega$. For negative bias, let $V_{GS} = V_{DS} + V_{DS}/2(V_{DS} - V_{GS})^2$.



FIGURE P4.45

*4.46 For the devices in the circuit of Fig. P4.46, $|V_T| = 1\text{ V}$, $\lambda = 0$, $\gamma = 0$, $k'_D/L = 50\mu\text{A}/\text{V}^2$, $L = 1\mu\text{m}$, and $W = 10\mu\text{m}$. Find V_1 and V_2 . How do these values change if C_{ox} and D_{SD} are reduced to have $W = 100\mu\text{m}$?

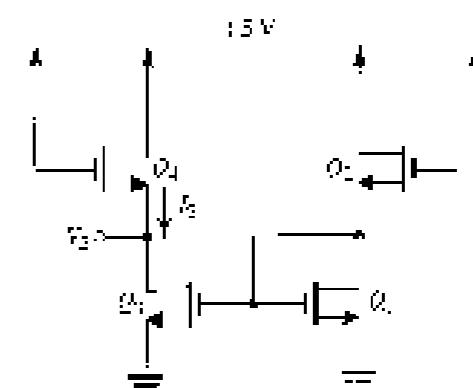


FIGURE P4.46

4.47 For the devices in the circuit of Fig. P4.47, $|V_T| = 1\text{ V}$, $\lambda = 0$, $\gamma = 0$, $k'_D/L = 50\mu\text{A}/\text{V}^2$, $L = 1\mu\text{m}$, and $W = 10\mu\text{m}$, unless otherwise specified. Find the labeled currents and voltages.

FIGURE P4.47

- 4.48** In the circuit of Fig. P4.48, transistors Q_1 and Q_2 have $V_t = -V_s$, and the process transconductance parameter $K_f = 100 \mu\text{A/V}^2$. Assuming $I_s = 0$, find V_{ds} , V_g , and V_b for each of the following cases:

- (a) $i_D(Z_1) = 1 \mu\text{A}/V$; $i_D = 20$
 (b) $i_D(Z_1) = 1.5 \mu\text{A}/V$; $i_D = 30$

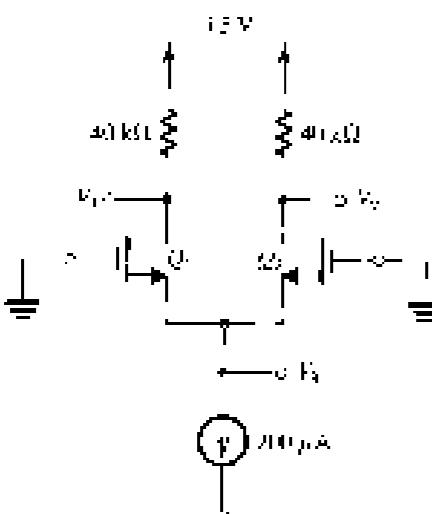


FIGURE P4.48

SECTION 4.4: THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

- 4.49** Consider the CS amplifier of Fig. 4.26(a) for the case $V_{DD} = 5 \text{ V}$, $R_d = 24 \text{ k}\Omega$, $k_f(V_{DS}) = 1 \text{ mA/V}^2$, and $V_t = 1 \text{ V}$.

(a) Find the coordinates of the two end points of the zero-gain segment of the output transfer characteristic, that is, points A and B in the plot of Fig. 4.26(c).

(b) If the amplifier is biased to operate with an overdrive voltage V_{DS} of 0.5 V , find the coordinates of the bias point Q_2 on the transfer characteristic of Fig. 4.26(c), and the value of A_{vD} and of the incremental gain A_v at the bias point.

(c) For the conditions in (b) and disregarding the reduction caused by the MOSFET's negative feedback characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input, while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of the amplifier and switch yield? By what percent is this gain value different from the gain value calculated above? Why is there a difference?

4.50 We wish to investigate the operation of the CS amplifier circuit shown in Example 4.8 for various bias conditions, that is, for bias at various points along the saturation region segment of the transfer characteristic. Prepare a table

giving the values of i_D (mA), V_{DS} (V), $V_{GS} = V_{DS} + V_t$, A_{vD} (mV/V), the magnitude of the largest allowable positive output signal, $|V_{DS}|$ (V), and the magnitude of the largest allowable negative output signal, $|V_{DS}|$ (V) for values of $V_{DS} = V_{GS}$ in the range of 1 V to 0 V in increments of 0.1 V , that is, there should be twelve rows for $V_{GS} = 1 \text{ V}, 0.9 \text{ V}, \dots, 0.1 \text{ V}$. Note that i_D is determined by the MOSFET operating condition V_{GS} by the MOSFET current in the triode region.

4.51 Various measurements are made on an NMOS amplifier. One finds the drain resistance $R_d = 70 \text{ k}\Omega$. First, dc measurements show the drain-to-source drain resistance V_{DS} to be 2 V and the gate-to-source bias voltage to be 1.2 V . Then, ac measurements with small signals show the voltage gain to be -10 mV/V . What is the value of V_t for this transistor? For the process transconductance parameter, $k_f = 50 \mu\text{A/V}^2$, where is the MOSFET's g_m ?

***4.52** Refer to the expression for the drain-to-gate voltage given in Eq. 4.42. Various steps are sometimes placed in front of the value of the drain-to-gate voltage, V_{DG} . For our purposes here, let this factor equal to 0.2 V . Also, assume that $V_{DS} = 5 \text{ V}$.

- (a) Without allowing any margin for output voltage swing, what is the maximum voltage gain achievable?
 (b) If we are required to allow 0.1 V output voltage swing, i_D of 0.5 V , and the bias voltage should be established at the drain to obtain maximum gain, what gain value is achievable? What input signal results in a $\pm 1.5 \text{ V}$ output swing?
 (c) For the situation in (b), if R_d is increased to establish a dc drain current of $100 \mu\text{A}$, for the given process technology, $k_f = 100 \mu\text{A/V}^2$.

4.53 The expression for the incremental voltage gain A_v given in Eq. 4.41 can be written as

$$A_v = -\frac{2(V_{DS} - V_{GS})}{V_{DS}}$$

where V_{DS} is the bias voltage at the drain terminal (Fig. 4.26). The expression indicates that for given values of V_{DS} and V_{GS} , the gain magnitude can be increased by biasing the transistor at a lower V_{DS} . This, however, reduces the allowable output signal swing in the negative direction. Assuming linear operation around the bias point, show that the large-signal negative output signal peak v_o that is not coupled while the transistor remains saturated is

$$v_o = (V_{DS} - V_{GS}) \left[1 - \frac{1}{A_v} \right]$$

For $V_{DD} = 5 \text{ V}$ and $V_{GS} = 0.5 \text{ V}$, provide a table of values for A_v , i_D , and the corresponding v_o for $V_{DS} = 1 \text{ V}, 1.5 \text{ V}, 2 \text{ V}$, and 2.5 V . If $V_{GS} = 1 \text{ mV}$, find i_D and A_v for the design for which $V_{DS} = 1 \text{ V}$.

4.54 Figure P4.54 shows a CS amplifier in which the load resistor R_d has been replaced with another NMOS transistor Q_3 , connected as a two-terminal device. Note that because the V_t of Q_3 is zero, it will be operating in saturation at all times, even when $i_D = 0$ and $i_{D3} = i_{D2}$. Note also that the two transistors conduct equal drain currents. Using $i_{D2} = i_{D3}$, show that for the range of V_{GS} for which Q_1 is operating in saturation, i_D is the

$$i_D = \frac{V_{GS}}{2} + \frac{V_{DS}}{2} + V_t$$

dc output voltage will be given by

$$v_o = V_{DD} - V_t + \frac{1}{2} \frac{\sqrt{V_{DS}}}{k_f(V_{DS})} V_t = \frac{\sqrt{V_{DS}}}{4(k_f(V_{DS}))} V_t$$

where we have assumed $V_t = V_D - V_S$. Thus the circuit functions as a linear amplifier, even for large input signals. For $k_f(V_{DS}) = 50 \mu\text{A/V}^2$ and $V_{DD} = 5 \text{ V}$, find i_D , voltage gain,

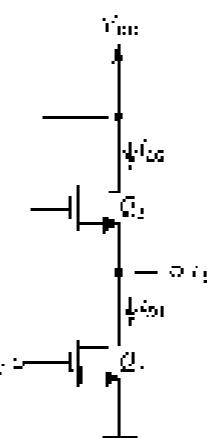


FIGURE P4.54

SECTION 4.5: BIASING IN MOS AMPLIFIER CIRCUITS

4.55 Consider the classical biasing scheme shown in Fig. 4.30(b), using a $\pm 5 \text{ V}$ supply. For the MOSFET, $V_t = 1 \text{ V}$, $k_f = 50 \mu\text{A/V}^2$, $W = 240 \text{ }\mu\text{m}$, and $L = 6 \text{ }\mu\text{m}$. Assuming that the drain current is 2 mA , with one-third of the supply voltage across each of R_d and R_s . Use $12 \text{ M}\Omega$ for the larger of R_d and R_s . What are the values of R_d , R_s , R_b , and R_{b2} ? If you have chosen R_s to be in two significant digits, for your design, how far is the drain voltage from the edge of saturation?

4.56 Using the circuit topology displayed in Fig. 4.30(a), arrange to bias the NMOS transistor at $i_D = 2 \text{ mA}$ with no voltage between gate and drain during triode operation. The available supplies are $\pm 1.5 \text{ V}$ for the NMOS transistor, $V_t = 0.8 \text{ V}$, $k_f = 30 \mu\text{A/V}^2$, $W = 20 \text{ }\mu\text{m}$, and $L = 4 \text{ }\mu\text{m}$. Use a gate bias resistor of $10 \text{ M}\Omega$. Specify R_s and R_d to ten significant digits.

***4.57** In an electronic instrument using the biasing scheme shown in Fig. 4.30(a), a manufacturer specifies that R_d is zero, $V_t = 1 \text{ V}$, $R_{b2} = 5.5 \text{ M}\Omega$, and $R_{b1} = 2.2 \text{ M}\Omega$. What is the value of V_t required if supplier specifications allow $k_f(V_{DS})$ to vary from $230 \text{ to } 348 \mu\text{A/V}^2$ and V_{DD} vary from 1.5 to 2.4 V , where the current in i_D is to vary from 12 to 18 mA ? What value of R_s should now be used to limit the maximum error of i_D to 0.15 mA ? Choose a appropriate standard 5% resistor value (refer Appendix G). What extreme values of current flow result?

4.58 An enhancement NMOS transistor is connected in the bias circuit of Fig. 4.30(a), with $V_t = 1 \text{ V}$ and $R_s = 1 \text{ k}\Omega$. The transistor has $V_t = 2 \text{ V}$ and $k_f(V_{DS}) = 2 \text{ mA/V}^2$. With V_t , bias current results. Use a transistor for which $k_f(V_{DS})$ is 50% higher, what is the resulting percentage increase in i_D ?

4.59 The bias circuit of Fig. 4.30(a) is used in a design with $V_t = 5 \text{ V}$ and $R_s = 1 \text{ k}\Omega$. For an enhancement MOSFET with $k_f(V_{DS}) = 2 \text{ mA/V}^2$, the source voltage was measured and found to be 2 V . What must V_t be for this device? If a device for which V_t is 0.5 V less is used, what does V_t become? What bias current results?

4.60 Design the circuit of Fig. 4.30(a) for an enhancement MOSFET having $V_t = 2 \text{ V}$ and $k_f(V_{DS}) = 2 \text{ mA/V}^2$, i.e., $V_{DD} = 10 \text{ V}$. Design for a drain current of 1 mA and for the largest possible voltage gain (that is, the largest possible V_{DS} consistent with allowing a $\pm 1 \text{ V}$ peak-to-peak voltage swing at the drain). Assume that the signal voltage at the source terminal of the FET is zero.

4.61 Design the circuit in Fig. 4.46 to either the transistor operating in saturation with V_{GS} biased 1 V from the edge of the triode region, with $i_D = 1 \text{ mA}$ and $V_{DD} = 3 \text{ V}$. For each of the following two devices (see a $10-\text{mA}$ current in the valence band):

- (a) $V_t = 1 \text{ V}$ and $k_f(V_{DS}) = 0.5 \text{ mA/V}^2$
 (b) $V_t = 2 \text{ V}$ and $k_f(V_{DS}) = 1.25 \text{ mA/V}^2$

For each case, specify the values of V_{GS} , V_D , V_S , R_s , R_d , and R_b .

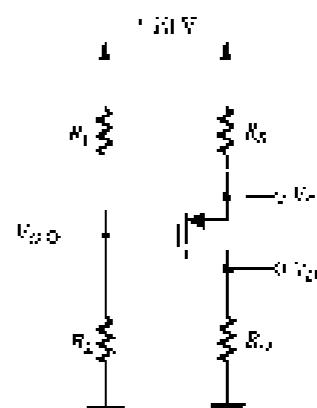


FIGURE P4.61

***4.62** A very common way to evaluate the stability of the bias current I_b is to consider the sensitivity of I_b relative to a particular transistor parameter or environmental quantity, η . The sensitivity of I_b relative to the MOSFET parameter $K = \mu C_s W/L^2$ is given by¹⁸

$$\frac{\partial I_b}{\partial K} = \frac{\partial I_b}{\partial I_{DS}} \cdot \frac{\partial I_{DS}}{\partial K} = \frac{I_{DS}}{K}$$

and the value, when multiplied by the variability for tolerances of K , provides the corresponding expected variability of I_b . The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 4.50(a).

- (a) Show that for V_D constant,

$$V_D = V_{DD} - 2(V_{GS} + V_{DS})$$

(b) For a MOSFET having $K = 100 \mu A/V^2$ with L variability of $\pm 10\%$, $V_{DD} = 1 \text{ V}$, find the value of R_2 that would result in $I_b = 100 \mu A$ with a variability of $\pm 1\%$. Also, find V_{GS} and the required value of V_{DS} .

(c) If the available supply $V_{DD} = 5 \text{ V}$, find the value of R_2 for $I_b = 100 \mu A$. Also, find the sensitivity function and give the expected variability of I_b in this case.

4.63 For the circuit in Fig. 4.50(a), with $L = 1 \times 14$, $K_F = 1$, $K_S = 5 \text{ mA}$, and $V_{DD} = 10 \text{ V}$, consider the behavior in each of the following two cases. In each case, find the voltages V_{GS} , V_{DS} , and V_{DD} that result:

- (a) $V_D = 1 \text{ V}$ and $\sqrt{A_{vD}} = 0.4 \text{ mA/V}^2$
 (b) $V_D = 2 \text{ V}$ and $\sqrt{A_{vD}} = 1.25 \text{ mA/V}^2$

4.64 For the circuit of Fig. 4.52, if $K_F = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, and $V_{DD} = 10 \text{ V}$, calculate the following two resistors. End the voltage V_{GS} and V_D :

- (a) $V_D = 1 \text{ V}$ and $\sqrt{A_{vD}} = 0.5 \text{ mA/V}^2$
 (b) $V_D = 2 \text{ V}$ and $\sqrt{A_{vD}} = 1.15 \text{ mA/V}^2$

4.65 Using the feedback bias arrangement shown in Fig. 4.52 with a 5-V supply and an NMOS device for which $K_F = 1 \text{ mA}$, $K_S = 0.4 \text{ mA/V}^2$, and R_1 established a drain current of 0.2 mA. If resistor values are limited to those on the 5% resistor scale (see Appendix G), what values would you choose? What values of current and V_D are left?

4.66 Figure P4.66 shows a variation of the feedback-bias circuit of Fig. 4.52. Using a 5-V supply with an NMOS transistors for which $K_F = 1.2 \text{ mA}$, $K_S = 4.2 \text{ mA/V}^2$, and $I_b = 0$ provide a design which is set for saturation at $I_{DS} = 2 \text{ mA}$, with R_2 large enough to ensure saturation operation for a 2-V negative signal swing at the drain. Use 22-MΩ as the target resistance for the feedback network. What values of R_2 , R_{CP} , and R_{SD} have you arrived? Specify all resistors to two significant digits.

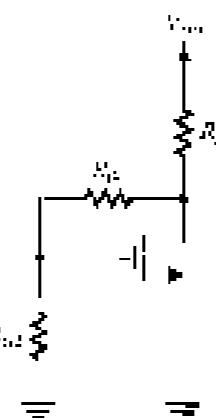


FIGURE P4.66

SECTION 4.6: SMALL-SIGNAL OPERATION AND MODELS

4.67 In problem 4.66, calculate the nonlinear distortion due to a MOSFET amplifier. Let the signal v_s be a sine wave with amplitude V_{pp} , and substitute $v_o = V_{DD}/2$ in Eq. (4.57). Using the argument of density sum $\theta = \frac{1}{2} + \frac{1}{2} \pi \times 50$, show that the ratio of the v_o/v_{s0} at frequency 200 to the v_o/v_{s0} at frequency 100, expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second harmonic distortion} = \frac{1}{4} \frac{V_{pp}}{V_{DD}} \times 100\%$$

If a power audio application V_{DD} is 10 mV, find the minimum operating voltage at which the transistor should be operated so that the second harmonic distortion is kept below than 1%.

4.68 On silicon NMOS transistor having $K_F(100) = 2 \text{ mA/V}^2$, let the transistor be biased at $V_{GS} = 1 \text{ V}$. For operation in saturation, what drain current I_{DS} is required if a 0.1-V signal is superimposed on V_{DS} ? Assume an operating frequency of 100 Hz. Calculate i_c by evaluating the total collector current i_c and subtracting the drain current I_{DS} . Repeat for a -0.1-V signal. Use these results to estimate $g_m < 0$ for 100 Hz at this bias point. Compare with the value of g_m obtained using Eq. (4.62).

4.69 Consider the FET amplifier of Fig. 4.31 for the case $V_D = 2 \text{ V}$, $K_F(100) = 1 \text{ mA/V}^2$, $V_{GS} = 4 \text{ V}$, $V_{DD} = 10 \text{ V}$, and $R_1 = 1.6 \text{ k}\Omega$.

- (a) Find the dc drain current I_{DS} and V_D .
 (b) Calculate the value of g_m at the bias point.
 (c) Calculate the value of the voltage gain.
 (d) If the MOSFET has $A = 10^4 \text{ V}^{-2}$, find v_o at the bias point and calculate the output current.

***4.70** An NVDs amplifier is to be designed to provide a 0.5-V peak output signal for a 50-kHz ac input. It can be used as a drain resistor R_D up to 1000 Ω at 1500 mA/V is needed.

What y_o is required? Using a dc voltage of 9 V, what values of R_2 and R_{SD} would you choose? What POF ratio is required if $R_{SD} = 100 \text{ m}\Omega$? Let $V_D = 0.5 \text{ V}$ and $V_{DD} = 10 \text{ V}$.

***4.71** To ILAs, problem we investigate small-signal design of the class amplifier circuit of Fig. 4.21. First, let the voltage gain be precisely $A_v = -v_o/v_s$, together with Eq. (4.71) for v_o , to show that

$$A_v = \frac{A_{vD}R_D}{V_{DD}} = \frac{2(V_{DD} - V_{GS})}{V_{DD}}$$

which is the expression we obtained in Section 4.4 (see 4.21). Now, let the maximum $|v_s|$ be the input signal be v_s . To keep the second-order harmonic distortion to an acceptable level, we bias our NVDs to operate at an overdrive voltage $|v_s| > 5$. Let $V_{DD} = 10 \text{ V}$. Now, to maximize the voltage gain $|A_v|$, we desire for the low as possible R_D . Show that the gain $|A_v|$ is maximized with $R_D = 5 \text{ k}\Omega$ (negative signal voltage swing of about one-half $|A_v|$ at a white noise voltage saturation mode operation) is 2000 .

$$A_v = \frac{V_{DD} + 2(V_{GS} - V_{DS})}{1 + 2(V_{GS} - V_{DS})}$$

Show that V_{GS} , V_{DS} , A_v , and R_D for the case $V_{DD} = 9 \text{ V}$, $V_{GS} = 10 \text{ mV}$, and $v_s = 10 \text{ mV}$, is desired to operate the transistor at $I_D = 100 \mu \text{A}$. Find the values of R_2 and R_{SD} , assuming that the In-Process technology $K_F = 100 \mu \text{A/V}^2$.

4.72 In the table below, for a single-element MOS transistor operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate g_m using one of Eqs. (4.65), (4.70), or (4.71). In the table, v_{GS} is the gate voltage in V , d_{SD} dimensions in μm , A_{vD} and A_{vS} in mA/V^2 , $A_{vD} = 250 \text{ mA/V}^2$, and $A_{vS} = 0.4 \text{ mA/V}^2$.

4.73 An NVDs technology has $A_{vD} = 50 \text{ mA/V}^2$ and $A_{vS} = 0.2 \text{ V}$. For a transistor with $L = 1 \mu\text{m}$, find the value of the drain resistance $r_d = 0.2 \text{ m}\Omega$ and $I_D = 0.5 \text{ mA}$. Also, find the required V_{GS} .

4.74 For the NVDs amplifier in Fig. P4.74, replace the transistor with its equivalent circuit of Fig. 4.30(d). Do the conversions for the voltage gains v_o/v_s and v_o/v_p .

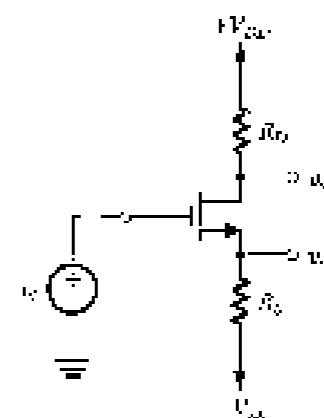


FIGURE P4.74

4.75 In the circuit of Fig. P4.75, the NMOS transistor has $V_T = 0.9 \text{ V}$ and $K_S = 5 \text{ mA}$ and operates with $V_D = 3 \text{ V}$. When is the voltage v_s 0.1 V ? What is V_o and the gain becomes for v_s increased to 1 mV ?

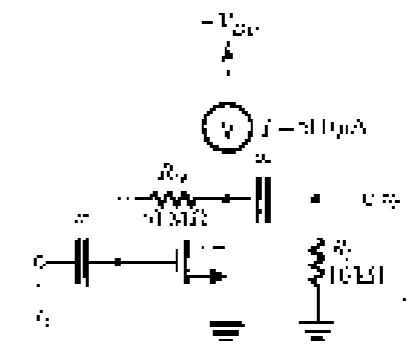


FIGURE P4.75

In Case $n = 1$ (Type 1), $\frac{V_{GS}}{V_{DD}} = \frac{1}{2}$; in Case $n = 2$ (Type 2), $\frac{V_{GS}}{V_{DD}} = \frac{1}{3}$; in Case $n = 3$ (Type 3), $\frac{V_{GS}}{V_{DD}} = \frac{1}{4}$; in Case $n = 4$ (Type 4), $\frac{V_{GS}}{V_{DD}} = \frac{1}{5}$; in Case $n = 5$ (Type 5), $\frac{V_{GS}}{V_{DD}} = \frac{1}{6}$; in Case $n = 6$ (Type 6), $\frac{V_{GS}}{V_{DD}} = \frac{1}{7}$; in Case $n = 7$ (Type 7), $\frac{V_{GS}}{V_{DD}} = \frac{1}{8}$; in Case $n = 8$ (Type 8), $\frac{V_{GS}}{V_{DD}} = \frac{1}{9}$; in Case $n = 9$ (Type 9), $\frac{V_{GS}}{V_{DD}} = \frac{1}{10}$; in Case $n = 10$ (Type 10), $\frac{V_{GS}}{V_{DD}} = \frac{1}{11}$; in Case $n = 11$ (Type 11), $\frac{V_{GS}}{V_{DD}} = \frac{1}{12}$; in Case $n = 12$ (Type 12), $\frac{V_{GS}}{V_{DD}} = \frac{1}{13}$; in Case $n = 13$ (Type 13), $\frac{V_{GS}}{V_{DD}} = \frac{1}{14}$; in Case $n = 14$ (Type 14), $\frac{V_{GS}}{V_{DD}} = \frac{1}{15}$; in Case $n = 15$ (Type 15), $\frac{V_{GS}}{V_{DD}} = \frac{1}{16}$; in Case $n = 16$ (Type 16), $\frac{V_{GS}}{V_{DD}} = \frac{1}{17}$; in Case $n = 17$ (Type 17), $\frac{V_{GS}}{V_{DD}} = \frac{1}{18}$; in Case $n = 18$ (Type 18), $\frac{V_{GS}}{V_{DD}} = \frac{1}{19}$; in Case $n = 19$ (Type 19), $\frac{V_{GS}}{V_{DD}} = \frac{1}{20}$; in Case $n = 20$ (Type 20), $\frac{V_{GS}}{V_{DD}} = \frac{1}{21}$; in Case $n = 21$ (Type 21), $\frac{V_{GS}}{V_{DD}} = \frac{1}{22}$; in Case $n = 22$ (Type 22), $\frac{V_{GS}}{V_{DD}} = \frac{1}{23}$; in Case $n = 23$ (Type 23), $\frac{V_{GS}}{V_{DD}} = \frac{1}{24}$; in Case $n = 24$ (Type 24), $\frac{V_{GS}}{V_{DD}} = \frac{1}{25}$; in Case $n = 25$ (Type 25), $\frac{V_{GS}}{V_{DD}} = \frac{1}{26}$; in Case $n = 26$ (Type 26), $\frac{V_{GS}}{V_{DD}} = \frac{1}{27}$; in Case $n = 27$ (Type 27), $\frac{V_{GS}}{V_{DD}} = \frac{1}{28}$; in Case $n = 28$ (Type 28), $\frac{V_{GS}}{V_{DD}} = \frac{1}{29}$; in Case $n = 29$ (Type 29), $\frac{V_{GS}}{V_{DD}} = \frac{1}{30}$; in Case $n = 30$ (Type 30), $\frac{V_{GS}}{V_{DD}} = \frac{1}{31}$; in Case $n = 31$ (Type 31), $\frac{V_{GS}}{V_{DD}} = \frac{1}{32}$; in Case $n = 32$ (Type 32), $\frac{V_{GS}}{V_{DD}} = \frac{1}{33}$; in Case $n = 33$ (Type 33), $\frac{V_{GS}}{V_{DD}} = \frac{1}{34}$; in Case $n = 34$ (Type 34), $\frac{V_{GS}}{V_{DD}} = \frac{1}{35}$; in Case $n = 35$ (Type 35), $\frac{V_{GS}}{V_{DD}} = \frac{1}{36}$; in Case $n = 36$ (Type 36), $\frac{V_{GS}}{V_{DD}} = \frac{1}{37}$; in Case $n = 37$ (Type 37), $\frac{V_{GS}}{V_{DD}} = \frac{1}{38}$; in Case $n = 38$ (Type 38), $\frac{V_{GS}}{V_{DD}} = \frac{1}{39}$; in Case $n = 39$ (Type 39), $\frac{V_{GS}}{V_{DD}} = \frac{1}{40}$; in Case $n = 40$ (Type 40), $\frac{V_{GS}}{V_{DD}} = \frac{1}{41}$; in Case $n = 41$ (Type 41), $\frac{V_{GS}}{V_{DD}} = \frac{1}{42}$; in Case $n = 42$ (Type 42), $\frac{V_{GS}}{V_{DD}} = \frac{1}{43}$; in Case $n = 43$ (Type 43), $\frac{V_{GS}}{V_{DD}} = \frac{1}{44}$; in Case $n = 44$ (Type 44), $\frac{V_{GS}}{V_{DD}} = \frac{1}{45}$; in Case $n = 45$ (Type 45), $\frac{V_{GS}}{V_{DD}} = \frac{1}{46}$; in Case $n = 46$ (Type 46), $\frac{V_{GS}}{V_{DD}} = \frac{1}{47}$; in Case $n = 47$ (Type 47), $\frac{V_{GS}}{V_{DD}} = \frac{1}{48}$; in Case $n = 48$ (Type 48), $\frac{V_{GS}}{V_{DD}} = \frac{1}{49}$; in Case $n = 49$ (Type 49), $\frac{V_{GS}}{V_{DD}} = \frac{1}{50}$; in Case $n = 50$ (Type 50), $\frac{V_{GS}}{V_{DD}} = \frac{1}{51}$; in Case $n = 51$ (Type 51), $\frac{V_{GS}}{V_{DD}} = \frac{1}{52}$; in Case $n = 52$ (Type 52), $\frac{V_{GS}}{V_{DD}} = \frac{1}{53}$; in Case $n = 53$ (Type 53), $\frac{V_{GS}}{V_{DD}} = \frac{1}{54}$; in Case $n = 54$ (Type 54), $\frac{V_{GS}}{V_{DD}} = \frac{1}{55}$; in Case $n = 55$ (Type 55), $\frac{V_{GS}}{V_{DD}} = \frac{1}{56}$; in Case $n = 56$ (Type 56), $\frac{V_{GS}}{V_{DD}} = \frac{1}{57}$; in Case $n = 57$ (Type 57), $\frac{V_{GS}}{V_{DD}} = \frac{1}{58}$; in Case $n = 58$ (Type 58), $\frac{V_{GS}}{V_{DD}} = \frac{1}{59}$; in Case $n = 59$ (Type 59), $\frac{V_{GS}}{V_{DD}} = \frac{1}{60}$; in Case $n = 60$ (Type 60), $\frac{V_{GS}}{V_{DD}} = \frac{1}{61}$; in Case $n = 61$ (Type 61), $\frac{V_{GS}}{V_{DD}} = \frac{1}{62}$; in Case $n = 62$ (Type 62), $\frac{V_{GS}}{V_{DD}} = \frac{1}{63}$; in Case $n = 63$ (Type 63), $\frac{V_{GS}}{V_{DD}} = \frac{1}{64}$; in Case $n = 64$ (Type 64), $\frac{V_{GS}}{V_{DD}} = \frac{1}{65}$; in Case $n = 65$ (Type 65), $\frac{V_{GS}}{V_{DD}} = \frac{1}{66}$; in Case $n = 66$ (Type 66), $\frac{V_{GS}}{V_{DD}} = \frac{1}{67}$; in Case $n = 67$ (Type 67), $\frac{V_{GS}}{V_{DD}} = \frac{1}{68}$; in Case $n = 68$ (Type 68), $\frac{V_{GS}}{V_{DD}} = \frac{1}{69}$; in Case $n = 69$ (Type 69), $\frac{V_{GS}}{V_{DD}} = \frac{1}{70}$; in Case $n = 70$ (Type 70), $\frac{V_{GS}}{V_{DD}} = \frac{1}{71}$; in Case $n = 71$ (Type 71), $\frac{V_{GS}}{V_{DD}} = \frac{1}{72}$; in

4.76 For a 0.8 μm CMOS transistor process, $V_{\text{dd}} = 0.8 \text{ V}$, $V_{\text{t}} = -0.9 \text{ V}$, $n_A C_{\text{ox}} = 90 \text{ }\mu\text{A/V}^2$, $p_A C_{\text{ox}} = 30 \text{ }\mu\text{A/V}^2$, $C_L = 1.2 \text{ fF/eV}$, $\beta_F = 0.32 \text{ V}^{-1}$, $\gamma = 0.5 \text{ V}^{-1/2}$, V_A (in channel devices) = 82 fJ/nm^2 and V_A (in channel devices) = 121 fJ/nm^2 . Find the small-signal model parameters (I_{ds} , r_{ds} and r_{ds}) for a device with an NMOS and a PMOS transistor having $L = 2 \mu\text{m}$, $W = 2 \text{ nm}$ and operating at $V_{\text{dd}} = 130 \text{ }\mu\text{V}$ with $|V_{\text{gs}}| = 1 \text{ V}$. Also find the negative voltage V_{g} which each device must be.

4.77 Figure P4.77 shows a discrete-circuit CS amplifier employing the class A biasing as was studied in Section 3.1. The input signal v_{in} is coupled to the base through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies (at a very large capacitor, shown as infinite). The output voltage signal v_{out} develops at C_{load} , coupled to a load resistance via a very large capacitor (shown as infinite).

- (a) If the measurement has $R_1 = 1\text{ k}\Omega$, and $A_f^2 \gg 1 - 2\text{ mA/V}^2$, verify that the bias circuit maintains $V_{DD} = 2\text{ V}$, $I_D = 1\text{ mA}$, and $V_{DS} = +7.5\text{ V}$. That is, measure these values and verify that they are consistent with the values of the circuit or appropriate device parameters.

(b) Find g_m and r_o if $V_s = 100\text{ mV}$.

(c) Draw a equivalent small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies.

(d) Using $V_s = 100\text{ mV}$, calculate v_o .

4.78 The fundamental relationship that describes MCBET is given by the equation $\ln(\frac{P_1}{P_2}) = \frac{R}{M} \ln(\frac{T_2}{T_1})$.

$$L = \frac{1}{2} \partial_1 \frac{\Psi}{\lambda} \partial_1$$

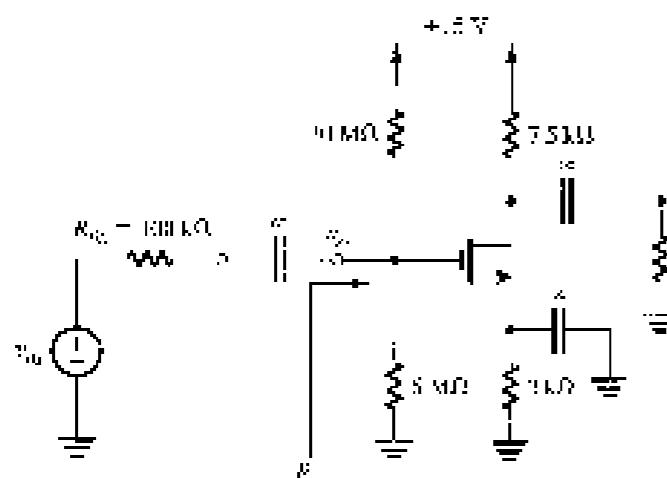


FIGURE P4.77

Show that the parabolic curve together with the tangent at point, whose coordinates are (x_0, y_0) . The slope of this tangent is y_0 , in this has short. Show that this tangent intersects the x -axis at $x_1 = x_0 - \frac{y_0}{2y_0'}$, it thus that $x_1 = 2x_0 - x_0^2$.

SECTION 4.7: SINGLE-STAGE MOS AMPLIFIERS

4.79 Calculate the output voltage at the load terminals of a bridge source amplifier for which $v_s = 2 \text{ mV/V}$, $R_o = 50 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, and $A_{OL} = 10 \text{ M}\Omega$. The amplifier is fed from a speaker with a Thévenin resistance of $0.5 \text{ M}\Omega$, and the output load consists of a speaker with a load resistance of $2\text{ }\Omega$.

B4.80 This problem investigates a redesign of the common source amplifier of Exercise 4.12 whose bias design was shown in Exercise 4.30 and shown in Fig. 4.40. Please read these two exercises.

- (c) The open-circuit voltage gain of the CS amplifier can be written as

$$A_{oc} = -\frac{2(V_{ce0} - V_{ce})}{V_{CE0}}$$

Verify that this expression yields the results in Exercise 4-42 (i.e., $A_{oc} = -15 \text{ V/V}$).

(d) A_{oc} can be doubled by reducing V_{ce} by a factor of 2, that is, from 1 V to 0.5 V while V_{ce0} is kept unchanged. What corresponding values for R_L , R_{ce} , g_m , and β apply?

(e) Find A_{oc} and R_{in} with μ_0 taken into account.

(f) For the conditions of (e), compute the current I_L .

100 kΩ, the same value of ground resistance $R_g = 4.8 \text{ M}\Omega$, and the same value of load resistance $R_L = 15 \text{ k}\Omega$, evaluate the new value of n-equivalent voltage gain G_n with n taken into account. Use your results to choose obtained in Exercises 11.9 and 11.12, and comment.

4-B1 A common-gate amplifier using an n-channel enhancement MOS transistor for which $\mu_A = 3 \text{ mA/V}^2$ has a load resistance (R_L) and a 7-k Ω load resistor (R_2). The input source is driven by a voltage source having $z = 200\text{k}\Omega$ resistance. What is the input resistance of the amplifier? What is the overall voltage gain (A_v)? If the circuit allows a bias current increase by a factor of 4 while maintaining linear operation, what does happen to its source and voltage gains because?

4.82 A 4×3 amplifier using an NMOS transistor biased at the midpoint of Fig. 4.41 for which $g_m = 2 \text{ mA/V}$ is found to have an output voltage gain of $4 \times 6 = 24 \text{ V/V}$. What value should a resistor R_2 inserted in the source lead have to reduce the voltage gain by a factor of 10?

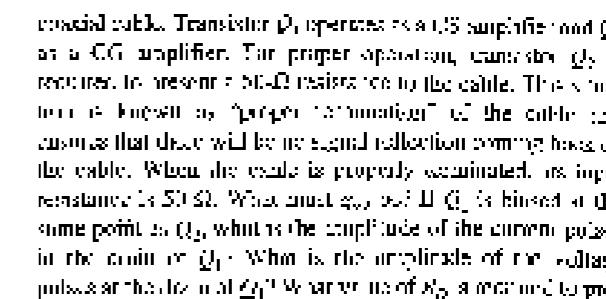
4.83 The overall voltage gain of the amplifier of Fig. 4.44 was measured with a resistance R_2 of 1 k Ω in place and found to be -10 V/V. When R_2 is shorted, the circuit operating conditions become linear at gain double. What must x_2 be? What value of R_2 is needed to obtain an overall voltage gain of -8 V/V?

4.54 Crystal measurements performed on the source D (lower of Fig. 4.44(a)) show that the open circuit voltage V_{oc} is 0.99 V/V. Also, when R_L is infinite and its value is varied, it is found that the gain is halved for $R_L = 500 \Omega$. If the amplifier remained linear throughout this measurement, what are the values of α and β ?

4.85 The source follower of Fig. 4-66(a) uses a MOSFET meant to have $g_m = 5 \text{ mA/V}^2$ and $\beta = 20,000$. Find the operating voltage $g_m V_A$, and the output resistance. What will v_{out} approach when a 1-k Ω load resistance (R_L) is connected?

4.86 Figure 4E.86 shows a scheme for coupling and uncoupling a high-frequency pulse train. The circuit includes two PIN-FETs, where bias density n_b is not shown and $n_d = 10^{12}$

FIGURE P4.86



*B4.87 The M03SEH1 in the circuit of Fig. B4.87 has $V_T = 1.0 \text{ V}$, $k = 0.8 \mu\text{A/V}^2$, and $V_D = 10 \text{ V}$.

- (a) Find the values of R_1 , R_2 and R_3 so that $i_g = 0$ mA, the largest possible voltage. (b) R_T is limited with a maximum voltage swing of the drain of $\pm 1\text{ V}$ is possible, and the input resistance at the gate is $10\text{ M}\Omega$.

(b) Find the values of g_m and r_o at the bias point.

(c) If terminal X is grounded, terminal Z is connected to a signal source having a resistance of $1\text{ M}\Omega$, and the input Y connected to a load resistance of $10\text{ k}\Omega$. Find the voltage gain from signal source to load.

(d) If terminal Y is grounded, find the voltage gain from X-Z with Z open-circuited. What is the output resistance of the source to load?

(e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of $10\text{ }\mu\text{A}$ and having a resistance of $100\text{ }\mu\Omega$, find the voltage signal that can be measured at Y. For some value, describe the effect of ...

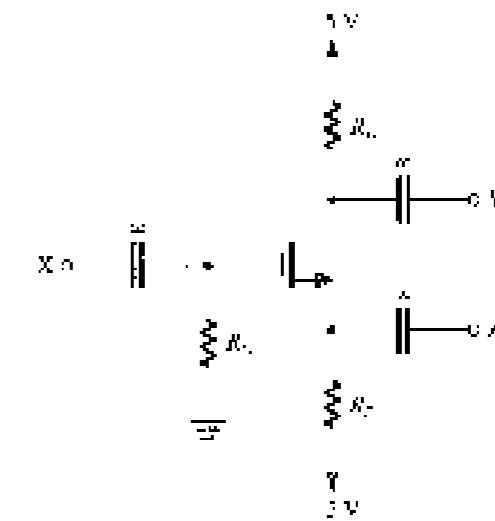


FIGURE PAGE

*4.68 (a) The NMOS transistor in the source-follower circuit of Fig. P-38 has $k_n = 2 \text{ mA/V}^2$ and a length l_0 . Find the open-circuit voltage gain and the output resistance.

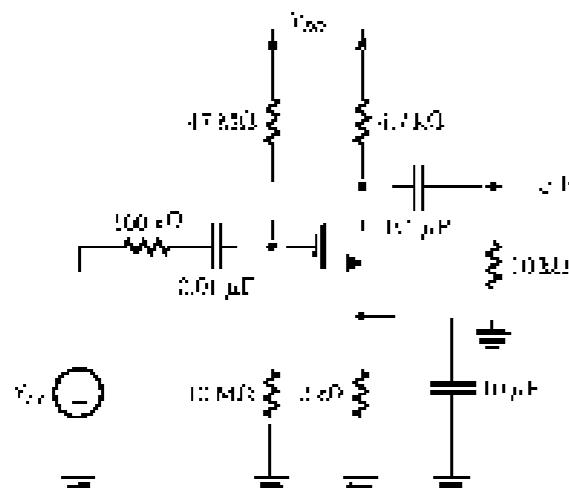


FIGURE P4.101

4.102 In NMOS transistors with discrete CN amplifier circuit of Fig. 4.100, let $V_{DD} = 10 \text{ mV}$ and $r_s = 100 \text{ kΩ}$. If $\mu_n = 1 \text{ mA/V}^2$, $L = 0.8 \mu\text{m}$, $V_t = 1 \text{ mV}$, $C_{ox} = 10 \text{ fF}$ and $C_{gd} = 0.2 \text{ pF}$, find I_D .

4.103 Consider the low-frequency response of the CN amplifier of Fig. 4.100. Let $R_F = 0.5 \text{ MΩ}$, $R_s = 2 \text{ MΩ}$, $\mu_n = 2 \text{ mA/V}^2$, $V_t = 20 \text{ mV}$, and $R_o = 1 \text{ kΩ}$. Find A_{vdc} . Also, design the coupling and bypass networks to locate the three frequencies at 10 Hz, 10 Hz, and 3 Hz. Use a minimum load capacitance with values as specified in Fig. 4.100. What value of C_F results?

4.104 Figure P4.102 shows a NMOS coupled pair design to be used and analyzed was presented in Example 4.10. Specifically, if a MOSFET is biased at $I_D = 1.36 \text{ mA}$ and has $\mu_n = 0.725 \text{ mA/V}^2$, $L = 47 \text{ } \mu\text{m}$, the midband gain you showed that $V_{GS} = 1.3 \text{ mV}$ and $R_o = 3.33 \text{ MΩ}$. Since these are static values for the two transistors in the coupled pair, they are reproduced below.

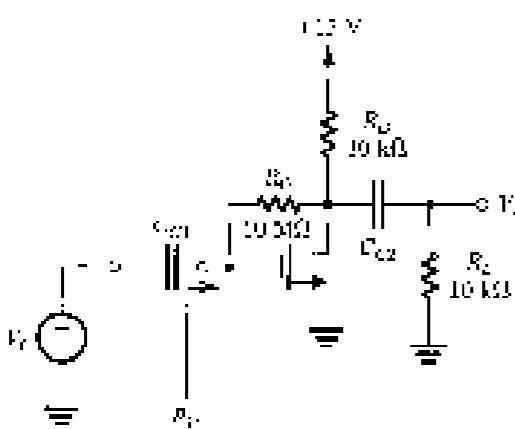


FIGURE P4.104

at least a decade lower. (Hint: it is useful to note the role the C_{gd} has on the R_o and r_s .)

SECTION 4.10: THE CMOS DIGITAL LOGIC INVERTER

4.105 For a digital logic inverter fabricated in a $0.8 \mu\text{m}$ CMOS technology for which $\mu_n = 1.2 \text{ mA/V}^2$, $L = 0.8 \mu\text{m}$, $V_t = 1.5 \text{ mV}$, $V_{DD} = 5 \text{ V}$, $I_D = I_{DS} = 0.8 \text{ mA}$, $R_s = 1.2 \text{ kΩ}$, and $R_o = 2.1 \text{ MΩ}$. Find:

- the output voltage $V_{out} = V_{DD}$ and $V_{out} = 0$;
- the drain current that the inverter can sink or source while the output remains within 0.1 V of ground or V_{DD} , respectively;
- V_{GS1} , V_{GS2} , and V_{GS3} .

4.106 For the test voltage generator in Problem 4.103, investigate how the threshold voltage of the drain of V_{DD} varies with the degree of mismatch of the NMOS and PMOS devices. Use the formula given in Exercise 4.11, and find V_d for the cases $(V_{DD})_d = 1.95 V_d$, $(V_{DD})_d = 0.15 V_d$, $(V_{DD})_d$ matched case, and $(V_{DD})_d = 2.45 V_d$.

4.107 For an inverter design with equal-sized NMOS and PMOS transistors and indicated in the technology specification problem 4.105 above, find V_{DD} and V_{out} and hence the noise margin.

4.108 Repeat Exercise 4.11 for $V_{DD} = 10 \text{ V}$ and 1 V .

4.109 Repeat Exercise 4.12 for $V_{DD} = 0.5 \text{ V}$, 1.5 V , and 2 V .

4.110 For a technology in which $V_t = 0.05 \text{ mV}$, show that the maximum current for the CMOS inverter is I_{DS} while its midband gain does not exceed $0.1V_{DD}/(R_sL)$. If $V_{DD} = 12 \text{ V}$, $\mu_n = 2 \text{ mA/V}^2$, $L = 20 \mu\text{m}$, $r_s = 0.5 \mu\text{m}$, find the required transistor width to obtain a current of 1 mA .

4.111 For the inverter specified in Problem 4.106, find the peak current drawn from the 5 V supply during switching.

4.112 For the inverter specified in Problem 4.106, find the voltage value when the inverter is loaded with a capacitance $C = 0.05 \text{ pF}$. Use both Eq. 4.12 and the approximate expression in Eq. (4.137), and compare them.

4.113 Consider an inverter fabricated in the CMOS technology specified in Problem 4.105 and having $L = 0.8 \mu\text{m}$ and $\mu_n/\mu_p = 2.0 \text{ mA/V}^2$. It is required to limit the propagation delay to 10 ps when the inverter is loaded with 0.05 pF capacitors and the required device widths W_1 and W_2 .

4.114 (a) In the transfer characteristic shown in Fig. 4.10, the segment BC is vertical because the body effect is neglected. Taking the body effect into account use small-signal analysis to show that the slope of the transfer characteristic is

$$a_i = k_b = V_{DD}/2 \beta$$

$$\frac{-k_b V_d}{(V_{DD}/2) - V_d}$$

where V_d is the drain voltage for Q_1 and Q_2 assume Q_1 and Q_2 to be matched.

(b) A CMOS inverter with series devices $k_b V_d/r_s = 1/(2R_s)$ is biased by connecting a resistor $R_s = 10 \text{ MΩ}$ between input and output. What is the dc voltage at input and output? What is the short-circuit current and input resistance of the resultant inverter? Assume the inverter to have the characteristics specified in Problem 4.105 with $V_d = 50 \text{ mV}$.

SECTION 4.11: THE DEPLETION-TYPE MOSFET

4.115 A depletion-type version of MOSFET 1 with $V_{DD} = 2 \text{ mA/V}^2$ and $V_t = 1 \text{ V}$ has no drain and gate pads. For the region of operation and drain current for $V_d = 0.1 \text{ V}$, 0.5 V , and 5 V . Neglect the charge-length modulation effect.

4.116 For a particular depletion-mode NMOS device, $V_t = -2 \text{ V}$, $k_b V_d = 200 \mu\text{A/V}^2$, and $L = 0.02 \mu\text{m}$. When operated at $V_d = 0$, maximize the drain current at flow for $V_{DD} = 1 \text{ V}$, 2 V , and 10 V . What are these drain currents for the device with L doubled with $k_b V_d = 10 \mu\text{A/V}^2$? (It is also doubled.)

4.117 Neglecting the drain-to-body ohmic drain resistance, show that for a depletion-type NMOS transistors (Fig. 4.11) the relationship is given by

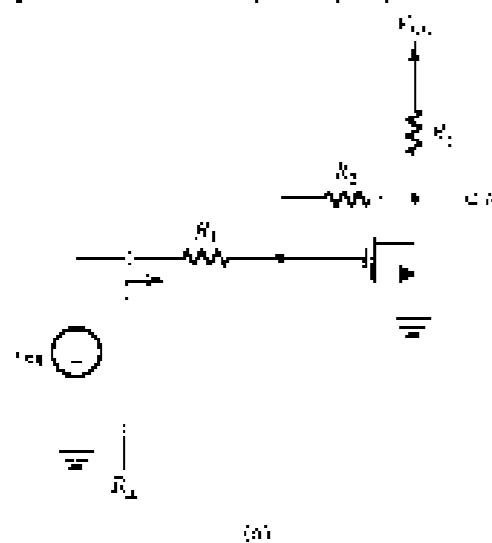
$$I = [k_b^2 (V_d - V_t)^2 / 2V_d] \quad \text{for } V_d > V_t$$

$$I = [k_b^2 (V_d - V_t)^2 / 2V_d] \quad \text{for } V_d < V_t$$

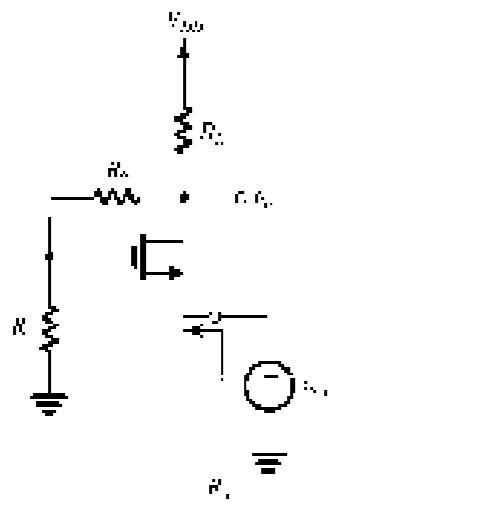
(Recall that V_t is assumed to be the V_t obtained for the case $V_d = 2 \text{ V}$ and $k_b V_d = 2 \text{ mA/V}^2$).

$$n =$$

and $N_2 = 1$ MΩ, find the overall voltage gain v_o/v_{in} and the input resistance R_i for each circuit. Neglect the body effect. Do these circuits conform to the no-amp rule? Why or why not?



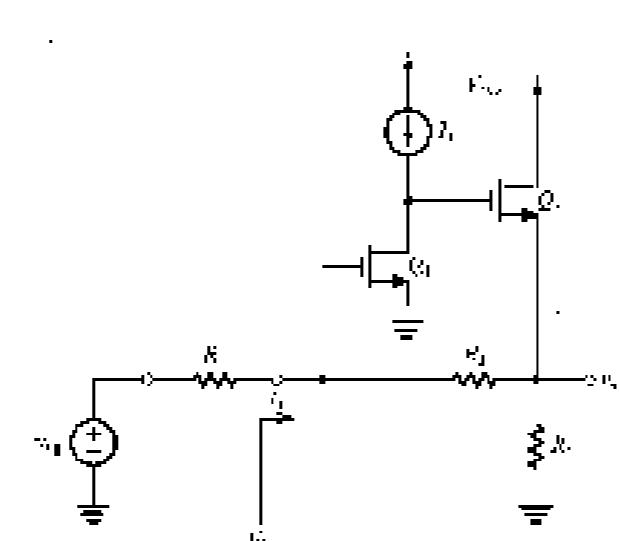
(a)



(b)

For NMOS transistors with $V_t = 0.1$ V, find V_{DSR} , V_D/V_{DS} , and V_A for bias conditions $I_D = 0.1$ mA and $m = 0.5$. The values of k_p and λ are specified in Problem 4.123; namely, $k_p = 1$ nA/V² and $\lambda = 100$ fA. For $R = 0.5$ MΩ, $R_s = 1$ MΩ, and $R_f = 10$ kΩ, find the required value of V_{DSR} .

4.123 In the amplifier shown in Fig. P4.123, resistances $R_1 = 100$ Ω and $R_2 = 20$ kΩ are replaced by $R_{1B} = 0.8$ kΩ using the appropriate choice of M/L ratio. In a particular application, I_B is to be sized to generate $I_D = 10 \mu\text{A}$, while Q_1 is intended to operate at $I_D = 1$ mA. For $R_f = 2.522$, the (R_1/R_f) requirement is to be satisfied 1% of the current in R_f (i.e., I_f) having no load component, and $I_f = 10 \mu\text{A}$, and the values of R_1 and R_f can satisfy all the requirements. (Hence V_{DS} must be > 2 V.) What is the voltage gain v_o/v_{in} ? Using a test circuit known as Miller's test (Chapter 3), find the input resistance $R_i = R_1/(1 + V_{DS}/V_t)$. Now, calculate the value of the overall voltage gain v_o/v_{in} . Does this result confirm you of the inverting configuration of the op-amp? Comment. How would you modify the circuit if no inverting configuration is desired?



(c)

4.124 (a) Recreate the bias design of the circuit of Problem 4.123 (shown in Fig. P4.123). For $V_t = 200$ μA/V² and $V_{DS} = 3.3$ V, find $(V_{DS})_1$ and $(V_{DS})_2$ to obtain the operating conditions specified in Problem 4.123.

FIGURE P4.121

4.122 For the two circuits in Problem 4.121 (shown in Fig. P4.121), we wish to consider the d -to- b bias design. Since v_{in} has a zero-drain component, we short-circuit its generator.



Bipolar Junction Transistors (BJTs)

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INTRODUCTION

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 4, since, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 3, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. As we learned also in

Chapter 1, the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work, play, and indeed, live. The invention of the BJT also contributed to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1960s and 1970s that it became a serious competitor to the BJT. At the time of this writing (2017), the MOSFET is undoubtedly the most widely used electronic device, and CMOS technology is the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications. For instance, the reliability of BJT circuits under severe environmental conditions makes them the dominant device in automotive electronics, an important and still-growing area.

The BJT remains popular in discrete circuit design, in which a very wide selection of BJT types are available to the designer. Here we should mention that the characteristics of the bipolar transistor are so well understood that one is able to design transistor circuits whose performance is reasonably predictable and quite insensitive to variations in device parameters.

The BJT is still the preferred device in many demanding analog circuit applications, both integrated and discrete. This is especially true in very high-frequency applications such as radio-frequency (RF) circuits for wireless systems. A very high-speed digital logic circuit largely based on bipolar transistors, namely emitter-coupled logic, is still in use. Finally, bipolar transistors can be combined with MOSFETs to create monolithic circuits that take advantage of the high input impedance and low-power operation of MOSFETs and the very high frequency operation and high current-handling capability of bipolar transistors. The resulting technology is known as BiMOS or BiCMOS, and it is finding increasingly larger areas of application (see Chapters 6, 7, 9, and 11).

In this chapter, we shall start with a simple description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of carriers and holes to a study of the traces or terminal characteristics. Current models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, by the end of the chapter, the reader should be able to perform bipolar transistor analysis of transistor circuits and to design single-stage transistor amplifiers and simple logic inverters.

5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

5.1.1 Simplified Structure and Modes of Operation

Figure 5.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see Appendix A, which deals with fabrication technology).

As shown in Fig. 5.1, the BJT consists of three semiconductor regions: the emitter region (n -type), the base region (p -type), and the collector region (n -type). Such a transistor is called an *npn* transistor. Another transistor, a *pn* of the *npn*, shown in Fig. 5.2, has a p -type emitter, an n -type base, and an n -type collector, and is appropriately called a *pnp* transistor.

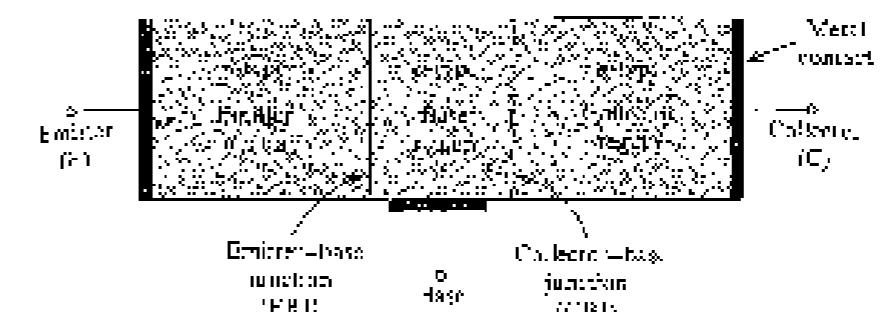


FIGURE 5.1 A simplified structure of the npn transistor.

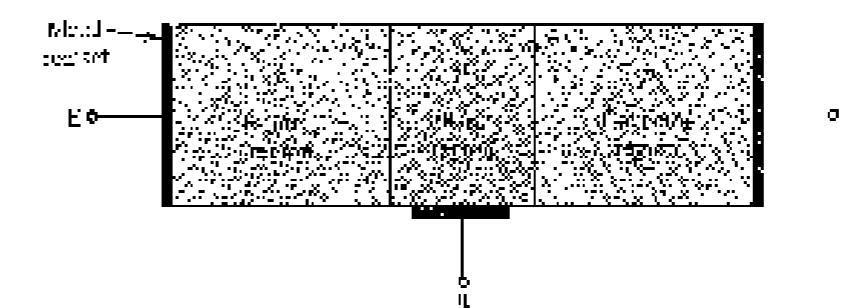


FIGURE 5.2 A simplified structure of the pnp transistor.

A terminal is connected to each of the three semiconductor regions of the transistor, with the terminals labeled emitter (E), base (B), and collector (C).

The transistor consists of two pn junctions, the emitter-base junction (EBJ) and the collector-base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 5.1.

The *active mode*, which is also called *forward active mode*, is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the *cutoff mode* and the *saturation mode*. The *reverse active mode* has very limited application but is conceptually important.

As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current conduction process in a bipolar transistor, which is the reason for the name bipolar.

TABLE 5.1 BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Reverse active	Reverse	Forward
Saturation	Forward	Forward

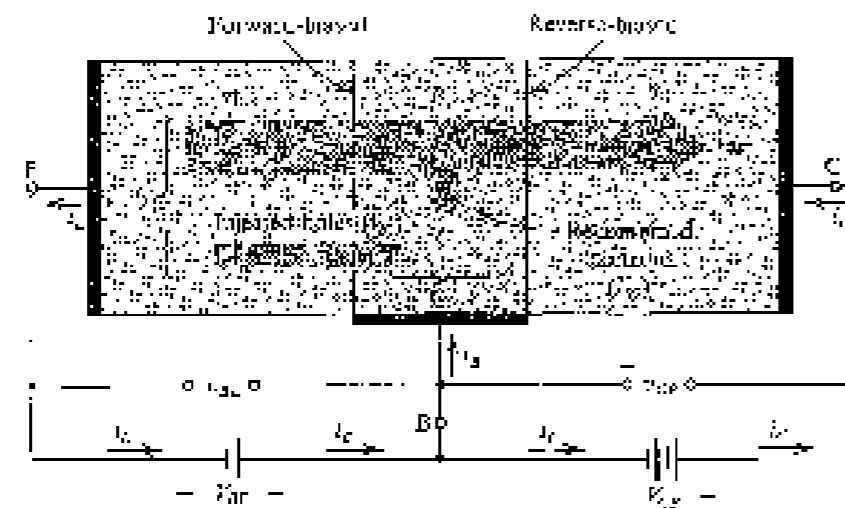


FIGURE 5.3 Current flow in a pnp transistor biased to operate in the reverse mode. (Reverse current components due to $N_{D1} < 0$ and thermally generated minority carriers are not shown.)

5.1.2 Operation of the pnp Transistor in the Active Mode

Let us start by considering the physical operation of the transistor in the active mode.¹ This situation is illustrated in Fig. 5.5 for the pnp transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage V_{BE} causes the p-type base to be higher in potential than the n-type emitter, thus forward-biasing the emitter-base junction. The collector-base voltage V_{BC} causes the n-type collector to be at a higher potential than the p-type base, thus reverse-biassing the collector-base junction.

Current Flow In the following description of current, "we only diffusion-current components are considered. Drift currents, due to thermally generated minority carriers, are usually very small and can be neglected. Nevertheless, we will have more to say about these reverse current components at a later stage.

The forward bias on the emitter-base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter-base junction will constitute the emitter current I_E , as indicated in Fig. 5.5. The direction of I_E is "out of" the emitter lead, which is in the direction of the hole current, and opposite to the direction of the electron current, with the emitter current I_E being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be determined by the electron component.

¹ It is assumed in this section that the reader is familiar with the operation of the pn junction under forward-bias conditions (Section 3.7.5).

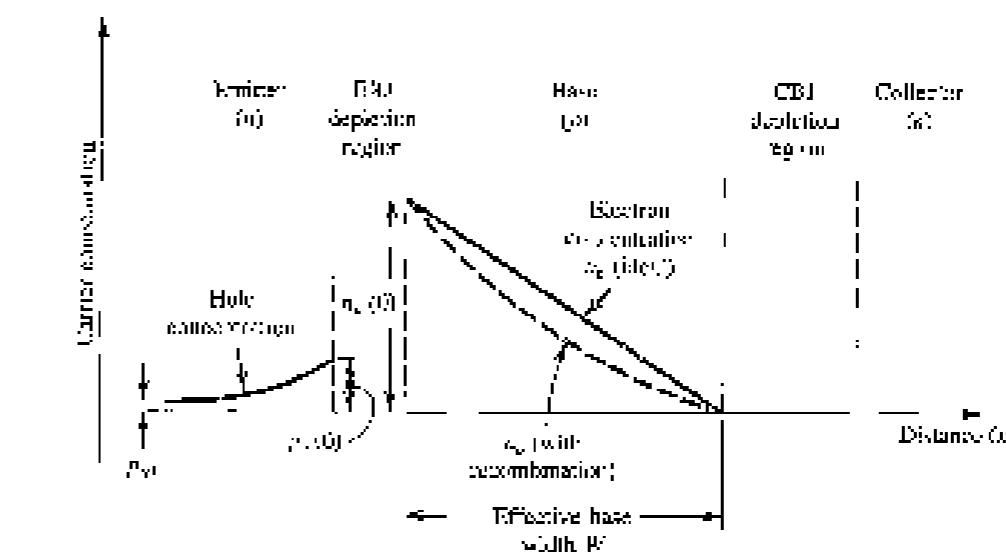


FIGURE 5.4 Profiles of minority-carrier concentrations in the base of a pnp transistor operating in the active mode: $N_p > 0$ and $N_n > 0$.

Let us now consider the electrons injected from the emitter into the base. These electrons will be minority carriers in the p-type base region. Because the base is usually very thin, in the steady state the excess minority-carrier (electron) concentration in the base will have an almost-straight-line profile, as indicated by the solid straight line in Fig. 5.4. The electron concentration will be highest (denoted by $n_e(0)$) at the emitter side and lowest (zero) at the collector side.² As in the case of any forward-biased pn junction (Section 3.7.5), the electron fraction $n_e(x)$ will be proportional to $e^{-\alpha_x x}$:

$$n_e(x) = n_{e0} e^{-\alpha_x x} \quad (5.1)$$

where n_{e0} is the thermal-equilibrium value of the minority-carrier (electron) concentration in the base region, α_x is the forward base-emitter bias voltage, and V_T is the thermal voltage, which is equal to approximately 25 mV at room temperature. The reason for the zero concentration at the collector side of the base is that the positive collector voltage V_{BC} causes the electrons at that end to be swept across the CBJ depletion region.

The tapered minority-carrier concentration profile (Fig. 5.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion current I_e is directly proportional to the slope of the straight-line concentration profile:

$$I_e = A_s q D_s \frac{dn_e(x)}{dx} = A_s q D_s \left(-\frac{n_e(0)}{W} \right) \quad (5.2)$$

² This minority-carrier distribution in the base results from the boundary conditions imposed by the two junctions. It is not an exponential decay distribution, which would result if the base region were infinitely thick. Rather, the thin base causes the n-side carrier to decay linearly. Furthermore, the reverse bias on the n-type-p-type junction causes the electron concentration at the collector side of the base to be zero.

where A_B is the cross-sectional area of the base-emitter junction in the depletion region in the p-region, q is the magnitude of the electron charge, D_n is the electron diffusivity in the base, and W is the effective width of the base. Observe that the negative slope of the minority-carrier concentration results in a negative current I_B away from the base; that is, I_B flows from right to left in the negative direction of x .

Some of the electrons I_B , once diffusing through the base region will recombine with holes, which are the majority carriers in the base. However, since the base is usually very thin, the proportion of electrons "lost" through this recombination process will be quite small. Nevertheless, the recombination in the base region causes the excess minority-carrier concentration profile to deviate from a straight line and take the slightly concave shape indicated by the lower line in Fig. 5.2. The slope of the concentration profile at the EBL is slightly higher than that at the OBL, with the difference accounting for the small number of electrons lost in the base region through recombination.

The Collector Current From the description above we see that most of the diffusing electrons will reach the boundary of the collector-base depletion region. Because the collector is more positive than the base (by ϕ_{ce} volt), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus go "undected" to constitute the collector current I_C . Thus $I_C = I_B$, which will yield a negative value for I_C , indicating that I_C flows in the negative direction of the x axis (i.e., from right to left). Since we will take this to be the positive direction of I_C , we can drop the negative sign in Eq. (5.2). Doing this and substituting for $n_2(0)$ from Eq. (5.1) we can thus express the collector current I_C as

$$I_C = I_B e^{\frac{q\phi_{ce}}{kT}} \quad (5.3)$$

where the saturation current I_S is given by

$$I_S = A_B q D_n n_0 / W$$

Substituting $n_2(0) = n_2^2/N_A$, where n_2 is the intrinsic carrier density and N_A is the doping concentration in the base, we can express I_C as

$$I_C = \frac{A_B q D_n n_0^2}{N_A W} e^{\frac{q\phi_{ce}}{kT}} \quad (5.4)$$

An important observation to make here is that the magnitude of I_C is independent of ϕ_{ce} . That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and register as collector current.

The saturation current I_S is inversely proportional to the base width W and is directly proportional to the area of the EBL. Typically I_S is in the range of 10^{-12} A to 10^{-15} A (depending on the size of the device). Because k is proportional to $T^{3/2}$, I_S is a strong function of temperature, approximately doubling for every 5°C rise in temperature. (For the dependence of n_0 on temperature, refer to Eq. 3.37.)

Since I_C is directly proportional to the junction area (i.e., the device size), it will also be related to I_S the scale current. Two transistors that are identical except that one has an EBL twice, say, twice that of the other will have saturation currents with the same ratio I_C/I_S , i.e., 2. Thus for the same value of ϕ_{ce} the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design.

The Base Current The base current I_B is composed of two components. The first component I_{B1} is due to the holes injected from the base region into the emitter region. This current component is proportional to $e^{\frac{q\phi_{be}}{kT}}$,

$$I_{B1} = \frac{A_B q D_p n_0^2}{N_A L_e} e^{\frac{q\phi_{be}}{kT}} \quad (5.5)$$

where D_p is the hole diffusivity in the emitter, L_e is the hole diffusion length in the emitter, and N_A is the doping concentration of the emitter.

The second component of base current I_{B2} is due to holes that have to be supplied by the external circuit in order to realize the holes lost from the base through the recombination process. An expression for I_{B2} can be found by noting that if the average time for a minority carrier to recombine with a majority hole in the base is denoted τ_b (called minority-carrier lifetime), then in τ_b seconds the minority-carrier charge in the base, Q_b , recombines with holes. Of course in the steady state, Q_b is regenerated by electron injection from the emitter. To replenish the holes, the current Q_b/τ_b must supply the base with a positive charge equal to Q_b every τ_b seconds,

$$I_{B2} = \frac{Q_b}{\tau_b} \quad (5.6)$$

The minority-carrier charge stored in the base region, Q_b , can be found by reference to Fig. 5.2. Specifically, Q_b is represented by the area of the triangle under the straight-line distribution in the base. Thus

$$Q_b = A_B q \times \frac{1}{2} N_A W$$

Substituting for $Q_b(0)$ from Eq. (5.1) and replacing n_1 by n_2^2/N_A gives

$$Q_b = \frac{A_B q W n_0^2}{2 N_A} e^{\frac{q\phi_{be}}{kT}} \quad (5.7)$$

which can be substituted in Eq. (5.6) to obtain

$$I_{B2} = \frac{1}{2} \frac{A_B q W n_0^2}{N_A} e^{\frac{q\phi_{be}}{kT}} \quad (5.8)$$

Combining Eqs. (5.5) and (5.8) and utilizing Eq. (5.4), we obtain for the total base current I_B the expression

$$I_B = I_S \frac{(D_p N_A W + 1) W^2 + \tau_b \omega_c}{2 D_p N_A L_e} \quad (5.9)$$

Comparing Eqs. (5.3) and (5.9), we see that I_C can be expressed as a function of I_S as follows:

$$I_C = \frac{I_S}{\beta} \quad (5.10)$$

That is,

$$I_C = \left(\frac{I_S}{\beta} \right) e^{\frac{q\phi_{ce}}{kT}} \quad (5.11)$$

where β is given by

$$\beta = \frac{(D_p N_A W + 1) W^2 + \tau_b \omega_c}{2 D_p N_A L_e} \quad (5.12)$$

from which we see that β is a constant for a particular transistor. For modern BJT transistors, β is in the range 50 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the constant β is called the common-emitter current gain.

Equation (5.10) indicates that the value of β is highly influenced by two factors: the width of the base region, W , and the relative doping of the base region and the emitter region, (N_A/N_D) . To obtain a high β which is highly desirable since β represents a gain parameter, the base should be thin (W small) and lightly doped and the emitter heavily doped (making N_A/N_D small). Finally, we note that the discussion thus far assumes an idealized situation where β is a constant for a given transistor.

The Emitter Current. Since the current that enters a transistor must leave it, it can be seen from Fig. 5.3 that the emitter current i_E is equal to the sum of the collector current i_C and the base current i_B ; that is,

$$i_E = i_C + i_B \quad (5.14)$$

Use of Eqs. (5.10) and (5.13) gives

$$i_E = \frac{\beta - 1}{\beta} i_C \quad (5.15)$$

Thus,

$$i_E = \frac{\beta - 1}{\beta} I_{C0} e^{\frac{qV_C}{kT}} \quad (5.16)$$

Alternatively, we can express Eq. (5.14) in the form

$$i_C = \alpha i_E \quad (5.17)$$

where the constant α is related to β by

$$\alpha = \frac{\beta}{\beta + 1} \quad (5.18)$$

Thus the emitter current in Eq. (5.15) can be written

$$i_E = (I_{C0}/\alpha) e^{\frac{qV_C}{kT}} \quad (5.19)$$

Finally, we can use Eq. (5.19) to express β in terms of α ; that is,

$$\beta = \frac{\alpha}{1 - \alpha} \quad (5.20)$$

It can be seen from Eq. (5.20) that α is a constant (for a particular transistor) that is less than but very close to unity. For instance, if $\beta = 100$, then $\alpha = 0.99$. Equation (5.19) reveals an important fact: Small changes in α correspond to very large changes in β . This rather unusual observation may seem itself physically, with the result that transistors of the same type may have widely different values of β . For reasons that will become apparent later, α is called the common-base current gain.

Finally, we should note that because α and β characterize the operation of the BJT in the "forward-active" mode (as opposed to the "reverse-active" mode, which we shall discuss shortly), they are often denoted α_F and β_F . We shall use α and β interchangeably and, similarly, α_F and β_F .

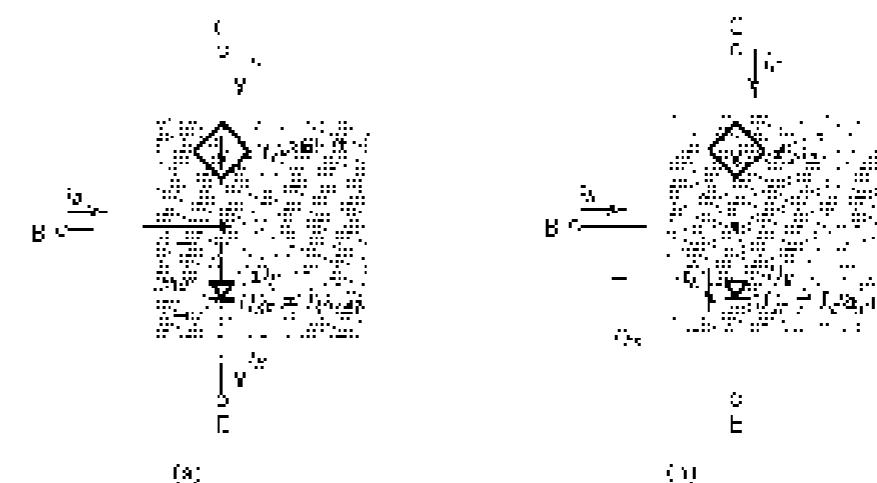


FIGURE 5.5 Large-signal equivalent circuit models of the npn BJT operating in the forward active mode.

Recapitulation and Equivalent-Circuit Models. We have presented a first-order model for the operation of the npn transistor in the active (or "forward") active mode. Basically, the forward-bias voltage V_{BE} causes an exponentially reduced current i_B to flow in the collector terminal. The collector current i_C is independent of the value of the collector voltage as long as the collector-base junction remains reverse-biased; that is, $V_{CB} \geq 0$. Thus in the active mode the collector terminal behaves as an ideal constant-current source whose the value of the current is determined by i_{C0} . The base current i_B is a factor $1/\beta$ of the collector current, and the emitter current is equal to the sum of the collector and base currents. Since i_B is much smaller than i_C (i.e., $\beta \gg 1$, $i_B \ll i_C$), more precisely, the collector current is a fraction α of the emitter current, with α smaller than but close to unity.

This first-order model of transistor operation in the forward active mode can be represented by the equivalent circuit shown in Fig. 5.5(a). Here diode D_2 has a scale current I_{C0} equal to I_{C0}/α and thus provides a current i_C related to i_E according to Eq. (5.18). The current of the controlled source, which is equal to the collector current, is controlled by i_E according to the exponential relationship indicated in requirement of Eq. (5.1). This model is also called a voltage-controlled current source. It can be converted to the current-controlled current-source model shown in Fig. 5.5(b) by expressing the current of the controlled source as αi_E . Note that this model is also nonlinear because of the exponential relationship of the current i_E through diode D_2 and the voltage V_{CE} . From this model we observe that if the transistor is used as a two-port network with the input port between B and C and the output port between C and E (i.e., with β as a common terminal), then the current gain observed is equal to α . Thus α is called the common-base current gain.

Small-Signal Model. In the small-signal model of the BJT, the dependent source is replaced by a dependent voltage source. If the dependent voltage source is denoted by v_{C2} , then the circuit diagram is as shown in Fig. 5.6(a). The dependent voltage source is controlled by the collector voltage V_C and has a value proportional to V_C . The dependent voltage source is connected between the collector terminal and ground. The dependent voltage source is labeled with a beta symbol.

and the collector-emitter voltage V_{CE} is increased to give the desired performance. The input current I_{BE} is also increased.

The output current I_C is proportional to the collector-emitter voltage V_{CE} by virtue of the law of conservation of charge. In the forward active mode, the current gain α_F is given by

$$\alpha_F = \frac{I_C}{I_B} = \frac{V_{CE}}{V_{BE}}$$

For a given collector current I_C , the collector-emitter voltage V_{CE} is given by

$$V_{CE} = \frac{I_C}{\alpha_F} = \frac{I_C}{V_{BE}/V_{CE}}$$

or

$$V_{CE} = \frac{I_C V_{CE}}{V_{BE}} + V_{CE}$$

$$V_{CE} = \frac{I_C}{V_{BE}} + V_{CE}$$

5.1.3 Structure of Actual Transistors

Figure 5.6 shows a more realistic (but not simplified) cross section of a real BJT. Note that the collector virtually surrounds the emitter region, thus making it difficult for the electrons injected into the thin base to escape being collected. In this way, the resulting α_F is close to unity and β_F is large. Also, observe that the device is not symmetrical. For more detail on the physical structure of actual devices, the reader is referred to Appendix A.

The actual BJT structure is not symmetrical because that if the emitter and collector are interchanged and the transistor is operated in the reverse active mode, the resulting values of α_F and β_F denoted α_R and β_R , will be different from the forward active mode values, α_F and β_F . Furthermore, because the structure is optimized for forward active operation, α_F and β_F will be much lower than their forward mode counterparts. Of course, α_R and β_R are related by equations identical to those that relate α_F and β_F . Typically, α_R is in the range of 0.01 to 0.5, and the corresponding range of β_R is 0.01 to 1.

The structure in Fig. 5.6 indicates also that the CBJ has a much larger area than the EBJ. It follows that, if the transistor is operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased) and the separation is modeled in the manner of Fig. 5.5(b), we obtain the model shown in Fig. 5.7. Here diode D_2 represents the collector-base junction and has a scale current I_{2S} that is much larger than the scale current I_{1S} of diode D_1 . The two scale currents have, of course, the same ratio as the areas of the corresponding junctions. Furthermore, a simple and elegant formula relates the scale currents I_{1S} , I_{2S} , and I_S and the current gains α_F and α_R namely

$$\alpha_F I_{1S} = \alpha_R I_{2S} = I_S \quad (5.20)$$

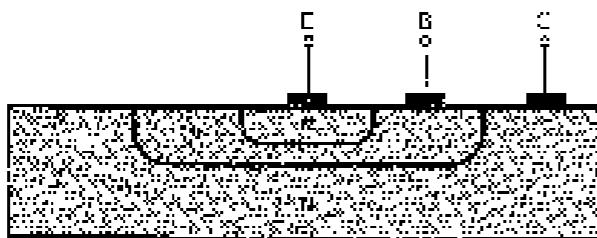


FIGURE 5.6 Cross-sectional view of a real BJT.

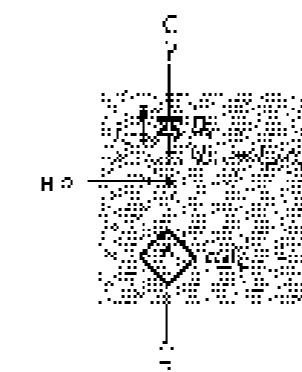
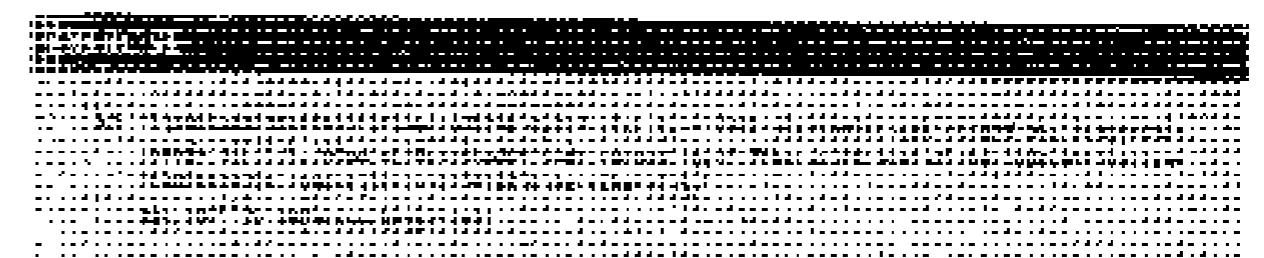


FIGURE 5.7 Model for the reverse active mode used in exercise 5.4, mode 5(a), with the CBJ forward biased and the EBJ reverse biased.

The large scale current I_{2S} has the effect that for the same current, the CBJ exhibits a lower voltage drop when forward biased than the forward voltage drop of the EBJ, V_{BE} . This point will have implications for the BJT's operation in the saturation mode.



5.1.4 The Ebers-Moll (EM) Model

The model of Fig. 5.5(a) can be combined with that of Fig. 5.7 to obtain the circuit model shown in Fig. 5.8. Note that we have relabelled the currents as through D_1 and D_2 , and the corresponding control currents of the controlled sources as i_{1X} and i_{2X} . Ebers and Moll, two

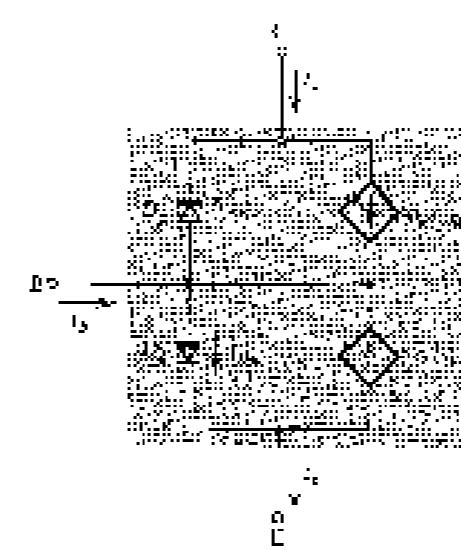


FIGURE 5.8 The Ebers-Moll (EM) model of the reverse active mode.

early workers in the area, have shown that the composite model can be used to predict the operation of the BJT in all of its possible modes. To see how this can be done, we derive expressions for the terminal currents i_x , i_y , and i_z in terms of the junction voltages v_{BE} and v_{BC} . Toward that end, we write an expression for the current at each of the three nodes of the model in Fig. 5.8 as follows:

$$i_x = i_{B2} - \alpha_B i_{C2} \quad (5.21)$$

$$i_y = -i_{B2} + \alpha_E i_{C2} \quad (5.22)$$

$$i_B = (1 - \alpha_E) i_{B2} + (1 - \alpha_B) i_{C2} \quad (5.23)$$

Then we use the diode equation to express i_{B2} and i_{C2} as

$$i_{B2} = I_{S2} (e^{v_{BE}/V_T} - 1) \quad (5.24)$$

and

$$i_{C2} = I_{S2} (e^{v_{BC}/V_T} - 1) \quad (5.25)$$

Substitution for i_{B2} and i_{C2} in Eqs. (5.21), (5.22), and (5.23) and using the relationship in Eq. (5.20) yield the required expressions:

$$i_x = \frac{I_{S2}}{\alpha_B} [e^{v_{BE}/V_T} - 1] - I_S e^{v_{BC}/V_T} \quad (5.26)$$

$$i_y = I_S e^{v_{BC}/V_T} - 1 - \left(\frac{I_{S2}}{\alpha_E} \right) e^{v_{BE}/V_T} - 1 \quad (5.27)$$

$$i_B = \left(\frac{I_{S2}}{\alpha_E} \right) [e^{v_{BE}/V_T} - 1] + \left(\frac{I_{S2}}{\alpha_B} \right) [e^{v_{BC}/V_T} - 1] \quad (5.28)$$

which

$$\beta_E = \frac{\alpha_E}{1 - \alpha_E} \quad (5.29)$$

and

$$\beta_B = \frac{\alpha_B}{1 - \alpha_B} \quad (5.30)$$

As a first application of the BIM model, we shall use it to predict the terminal currents of a transistor operating in the forward active mode. Here v_{BE} is positive and in the range of 0.0 V to 0.8 V, and v_{BC} is negative. One can easily see that terms containing e^{v_{BC}/V_T} will be negligibly small and can be neglected to obtain

$$i_x \approx \left(\frac{I_{S2}}{\alpha_B} \right) e^{v_{BE}/V_T} + I_S \left(1 - \frac{1}{\alpha_E} \right) \quad (5.31)$$

$$i_y \approx I_S e^{v_{BC}/V_T} + I_S \left(\frac{1}{\alpha_E} - 1 \right) \quad (5.32)$$

$$i_B \approx \frac{I_{S2}}{\alpha_E} e^{v_{BE}/V_T} - I_S \left(\frac{1}{\alpha_B} + \frac{1}{\alpha_E} \right) \quad (5.33)$$

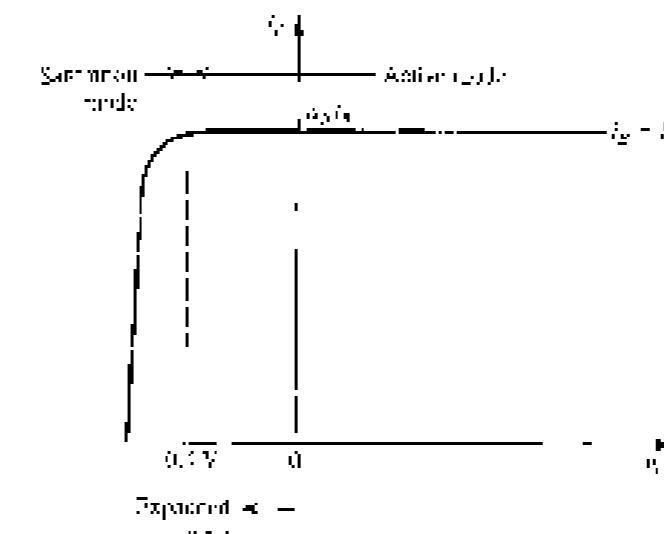


FIGURE 5.9: Collector current-voltage characteristics of an npn transistor with a constant emitter current I_E ; the curves show the transition from active mode operation for $v_{CE} < -0.4$ V and the collector cut-off for $v_{CE} > 0$.

In each of these three equations, one can normally neglect the second term on the right-hand side. This results in the familiar current-voltage relationships we derived earlier, namely, Eqs. (5.18), (5.3), and (5.11), respectively.

Thus far, we have stated the condition for forward active mode operation as $v_{BE} \geq 0$ to ensure that the CBJ is reverse biased. In actual fact, however, a p-n junction does not become effectively forward biased until the forward voltage across it exceeds approximately 0.5 V. It follows that one can maintain active-mode operation of an npn transistor for negative v_{BE} down to approximately -0.1 V or so. This is illustrated in Fig. 5.9, which shows a sketch of i_C versus v_{CE} for an npn transistor operated with a constant-emitter current I_E . Observe that i_C remains constant at $\approx I_E$ for v_{CE} going negative to approximately -0.1 V. Below this value of v_{CE} , the CBJ begins to conduct sufficiently that the transistor leaves the active mode and enters the saturation mode of operation, where i_C increases. We shall study BJT saturation next. For now, however, note that we can use the EM equations to verify that the terms containing e^{v_{BC}/V_T} remain negligible small for v_{BC} as high as 0.4 V.

EXERCISE

- 5.6 For the BJT with $\alpha_E = 100$, $\alpha_B = 10$, $\beta_E = 10^3$, $\beta_B = 10^2$, and $I_S = 10^{-12}$ A, calculate the second term on the right-hand side of each of Eqs. (5.26), (5.27), and (5.28) and show that it can be neglected. The values correspond to a transistor with $V_T = 25$ mV, $N_D = 10^{12}$ A/V², $N_A = 10^{13}$ A/V², $N_C = 10^{14}$ A/V², $N_B = 10^{15}$ A/V², $N_{A'} = 10^{16}$ A/V², $N_{B'} = 10^{17}$ A/V², $N_{C'} = 10^{18}$ A/V², and $N_{D'} = 10^{19}$ A/V².

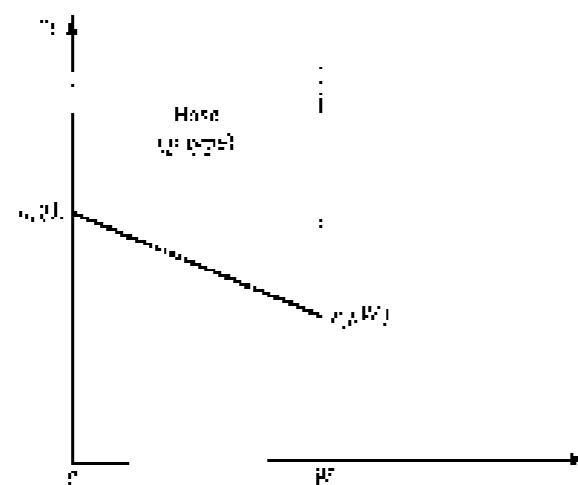


FIGURE 6.10 (Continued) part 1 of the 10-story concrete elevator shaft base of an office building operating in the tenth floor office.

5.1.5 Operation in the Saturation³ Mode

Figure 5.9 indicates that as v_{DS} is lowered below approximately 0.2 V, the BJT enters the saturation mode of operation. Ideally, v_{DS} has no effect on the collector current in the active mode, but the situation changes dramatically in saturation. Increasing v_{DS} in the negative direction—that is, increasing the forward bias voltage of the CBJ—increases i_C . To see this analytically, consider the Ebers-Mull expression for i_C in Eq. (5.27) and, for simplicity, neglect the terms not involving exponential's to obtain

$$i_r = i_0 e^{i\omega_r t} - \left(\frac{i\omega_r}{2\alpha_r} e^{i\omega_r t} \right). \quad (6.31)$$

The first term on the right-hand side is a result of the forward-biased CBF, and the second term is a result of the forward-biased CBJ. The second term starts to play a role when v_{ds} exceeds approximately 0.4 V or so. As v_{ds} is increased, this term becomes larger and subtracts from the first term, causing β to reduce, eventually reaching zero. Of course, one can operate the saturated transistor at any value of β , between 0 and β_0 . We will have more to say about saturation-mode operation in subsequent sections. Here, however, it is instructive to examine the minority-carrier concentration profile in the base of the saturated transistor, as shown in Fig. 9.10. Observe that because the CBF is now forward-biased, the electron concentration at the collector edge of the base is no longer zero; instead, it is a value proportional to $\beta^{1/2}$. Also note that the shape of the concentration profile is reduced in correspondence with the reduction in β .

¹ Summarization in a DLT means something completely different than, i.e., in a MOSBET, the sum of the frequencies of the DLT is analogous to the source region of operation of the MOSBET. On the other hand, the destination region of operation of the MOSBET corresponds to the active load of DLT (SCHOTTKY).

EXERCISES

- 3.7 (a) Use the bond expression in Eq. (3.50) and (3.51) to show that the π -conjugation length of the 5,9-diquaternary bisphenol A is 10 atoms, which corresponds to 10 carbon atoms.

(b) For the TGA, $\delta = 10\%$, $\delta_0 = 1 \times 10^{-3}$ or $= 1$, and $\alpha_0 = 0.001$. Find α_0 if $\delta = 0.5\%$, $\delta_0 = 0.5\%$, and $\alpha_0 = 0.57$. Also, find the value of α_0 at which $\delta = 0$.

(c) At 100 °C, linear α -pinene has a 50% weight loss in about 10 minutes. Calculate α_0 using Eq. (3.26) for 100 °C initial rate of 0.97 min⁻¹ (0.97 × 0.50 = 0.49), 5.76 mmol⁻¹ (1 mol pinene = 5.76 mmol), and $\delta = 10\%$.

5.1.6 The *ppp* Translator

The pnp transistor operates in a manner similar to that of the npn device described above. Figure 5.11 shows a pnp transistor biased to operate in the active mode. Here the voltage V_{B2} causes the p-type emitter to be higher in potential than the n-type base, thus forward-biasing the base-emitter junction. The collector-base junction is reverse-biased by the voltage V_{C2} , which keeps the p-type collector lower in potential than the n-type base.

Unlike the i_B (transistor) current in the pnp device, the i_B (pn junction) is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{BE} . Since the component of emitter current contributed by electrons injected from base to emitter is large enough by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the first component of base current, i_{B1} . Also, a number of the holes injected into the base will recombine with the majority carriers in the base (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to the second component of base current, i_{B2} . The bases that succeed in reaching the boundary of the depletion region of the collector-base junction will be attracted by the negative voltage on the collector. Thus those holes will be swept across the depletion region into the collector and appear as collector current.

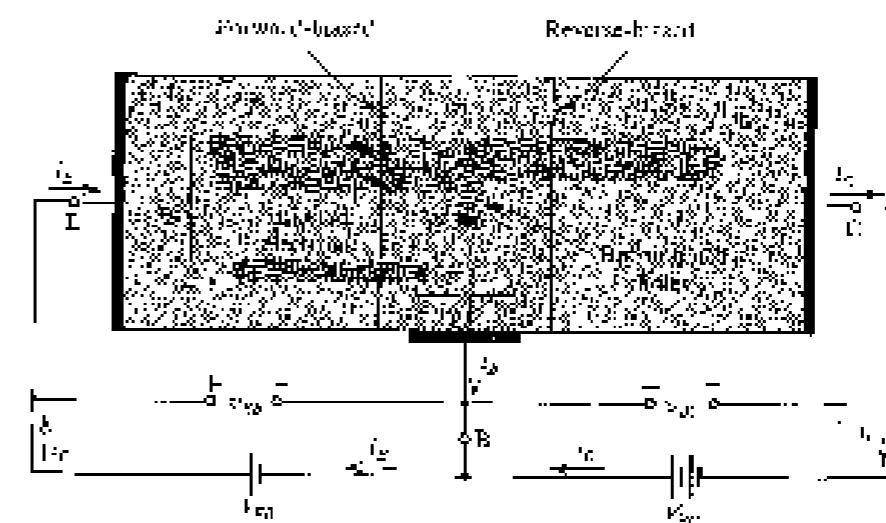


FIGURE 5.11 Content flow in a user navigation-based document in the active mode.

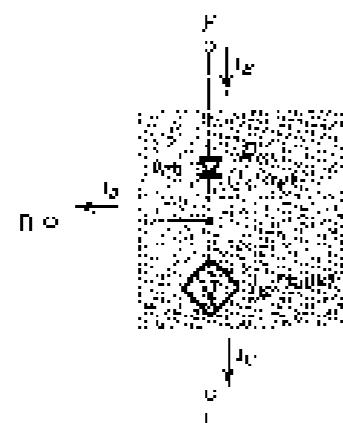


FIGURE 5.12 Large-signal model of the n-p-n transistor operating in the active mode.

It is easily seen from the above description that the current-voltage relationships in the p-n-p transistor will be identical to those of the n-p-n transistor except that v_{BE} is to be replaced by v_{CB} . Also, the large-signal active-mode operation of the p-n-p transistor can be modeled by the circuit depicted in Fig. 5.12. As in the n-p-n case, another version of this equivalent circuit is possible in which the current source is replaced with a current-controlled current source βv_{CE} . Finally, we note that the p-n-p transistor can operate in the saturation mode in a manner analogous to the described for the n-p-n device.

EXERCISES

- 5.1 Consider the circuit in Fig. 5.12 operating in the active mode of operation whose bias is specified. The emitter is fed by an independent current source with amplitude 2 mA , and the collector-emitter voltage is constrained at a -30-V constant. Find the emitter voltage, the base current, and the collector current if the p-n-p transistor $\beta = 50\%$ and $V_A = 10\text{ V}$.
- Ans. 0.65 V ; $I_B = 0.03\text{ mA}$; $I_C = 0.15\text{ mA}$
- 5.2 For the p-n-p transistor having $\beta = 100$, a unity $\beta - 100$ voltage gain $A_V = 100$, and $V_A = 100\text{ V}$, find the collector current if the base current is 1 mA .
- Ans. 0.6 mA ; $I_C = 60\text{ mA}$

5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.1 Circuit Symbols and Conventions

The physical structure used thus far to explain transistor operation is rather cumbersome to employ in drawing the schematic of a multiteristoric circuit. Fortunately, a very descriptive and convenient circuit symbol exists for the BJT. Figure 5.13(a) shows the symbol for the n-p-n transistor; the p-n-p symbol is given in Fig. 5.13(b). In both symbols, the emitter is distinguished by an arrowhead. This distinction is important because, as we have seen in the last section, p-n-p BJTs are not symmetric devices.

The polarity of the device—n-p-n or p-n-p—is indicated by the direction of the arrowhead on the emitter. This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base-emitter junction. Since we have adopted a

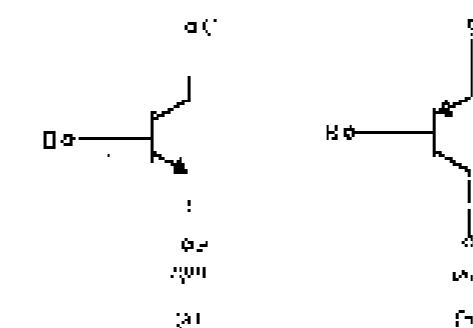


FIGURE 5.13 Circuit symbols for BJTs.

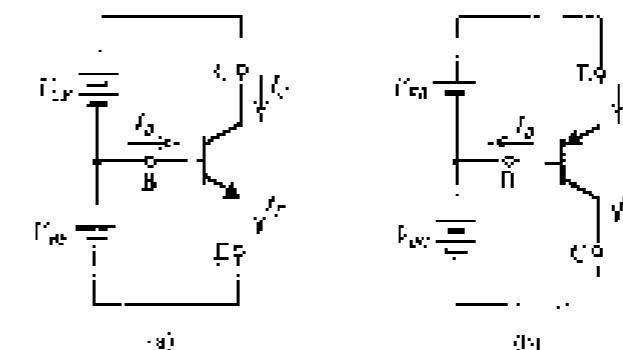


FIGURE 5.14 Voltage variables and current-flow conventions used in active mode.

drawing convention by which currents flow from top to bottom, we will always draw p-n-p transistors in the manner shown in Fig. 5.13 (e.g., with the emitter on top).

Figure 5.14 shows n-p-n and p-n-p transistors biased to operate in the active mode. It should be mentioned in passing that the housing hexagon cut shown, utilizing two dc voltage sources, is not a usual one and is used here merely to illustrate operation. Practical biasing schemes will be presented in Section 5.5. Figure 5.14(a) indicates the reference and actual directions of current flow throughout the transistor. Our convention will be to take the reference direction to coincide with the normal direction of current flow. Hence, normally, we should not encounter a negative value for v_{BE} , i_B , or i_C .

The convenience of the circuit drawing convention that we have adopted should be obvious from Fig. 5.14. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. The arrowhead on the emitter also implies the polarity of the collector-base voltage that should be applied in order to forward bias the emitter-base junction. Just a glance at the circuit symbol of the p-n-p transistor, for example, indicates that we should make the emitter lighter in voltage than the base (by v_{CB}) in order to cause current to flow into the emitter (downward). Note that the symbol v_{BE} means the voltage by which the emitter (E) is higher than the base (B). Thus, for a p-n-p transistor operating in the active mode, v_{BE} is positive, while in an n-p-n transistor, v_{BE} is positive.

From the discussion of Section 5.1 it follows that an n-p-n transistor whose BEJ is forward biased will operate in the active mode as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V . Otherwise, the transistor leaves the active mode and enters the saturation region of operation.

TABLE 5.2 Summary of the BJT Current-Voltage Relationships in the Active Mode

$i_e = I_s e^{\frac{V_{BE}}{V_T}}$
$i_c = \frac{i_e}{\beta} = \left(\frac{I_s}{\beta}\right) e^{\frac{V_{BE}}{V_T}}$
$i_o = \frac{i_e}{\alpha} = \left(\frac{I_s}{\alpha}\right) e^{\frac{V_{BE}}{V_T}}$
Note: For the pnp transistor, replace i_{ce} with i_{eb} .
$i_s = m \quad i_p = (1 - \alpha)i_n = \frac{i_n}{\beta - 1}$
$i_n = \beta i_n \quad i_n = (\beta + \alpha)i_p$
$\beta = \frac{\alpha}{1 - \alpha} \quad \alpha = \frac{\beta}{\beta + 1}$
$V_T = \text{thermal voltage} = \frac{kT}{q} = 26 \text{ mV at room temperature}$

In a pnp transistor, the pnp transistor will operate in the active mode if the EBJ is forward biased and the collector voltage is not allowed to rise above that of the base by more than $6.4 V$, or α . Otherwise, the CBJ becomes forward biased, and the pnp transistor enters the saturation region of operation.

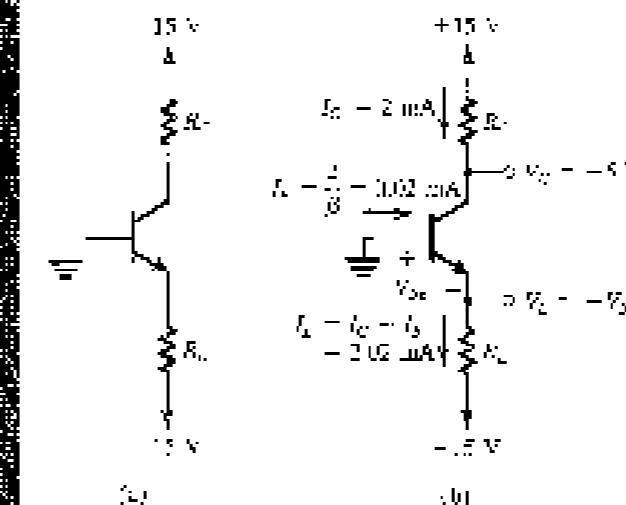
For easy reference, we present in Table 5.2 a summary of the BJT current-voltage relationships in the active mode of operation. Note that, for simplicity we use β and α rather than α_1 and β_1 .

The Constant n In the diode equation (Chapter 3) we used a constant n in the exponential and mentioned that its value is between 1 and 2. For modern bipolar junction transistors the constant n is close to unity except in special cases: (1) at high currents (i.e., high relative to the normal current range of the particular transistor) the i_c - V_{BE} relationship exhibits a value of n that is close to 2, and (2) at low currents the i_c - V_{BE} relationship shows a value of n of approximately 2. Note that, for our purposes we shall assume it's always that $n = 1$.

The Collector-Base Reverse Current (I_{CBO}) In our discussion of current flow in transistors we ignored the small reverse currents caused by thermal generation and drift carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector-base junction deserves some mention. This current, denoted I_{CBO} , is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript B). This current is usually in the microampere range, a value that is many orders higher than the normally predicted values. As with the diode reverse current, I_{CBO} contains a substantial leakage component, and its value is dependent on V_{BE} . I_{CBO} depends strongly on temperature, approximately doubling for every 10°C rise.

⁴The nonlocalized condition of i_{ce} is different to that of i_c because i_{ce} contains a substantial voltage component.

The transistor in the circuit of Fig. 5.15(a) has $\beta = 100$ and exhibits a $V_T = 0.7 \text{ V}$ at $i_c = 1 \text{ mA}$. Design the circuit so that a current of 2 mA flows through the collector and a voltage of $+5 \text{ V}$ appears at the collector.

**FIGURE 5.15** Circuit for Example 5.1.

Solution

Refer to Fig. 5.15(b). We note in the circuit that since we are required to design for $V_C = +5 \text{ V}$, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_{CE} = +5 \text{ V}$ the voltage drop across R_C must be $15 - 5 = 10 \text{ V}$. Now, since $i_c = 2 \text{ mA}$, the value of R_C should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $V_{BE} = 0.7 \text{ V}$ at $i_c = 1 \text{ mA}$, the value of i_{EB} at $i_c = 2 \text{ mA}$ is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.711 \text{ V}$$

Since the base is at 0 V , the emitter voltage should be

$$V_E = -0.711 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for R_E can be determined from

$$R_E = \frac{V_E - (-0.7)}{I_E}$$

$$= \frac{-0.711 + 0.7}{2.02} = 0.005 \text{ }\mu\Omega$$

This completes the design. We should note, however, that the calculations have been made with a safety factor that is usually neither necessary nor justified in practice because, for instance, of the expected tolerances of component values. Nevertheless, we chose to do the design precisely in order to illustrate the various steps involved.

EXERCISES

5.10. The circuit shown in Fig. 5.10 is a common-emitter amplifier operating from a 12-V supply. The load resistance is $R_L = 10 \text{ k}\Omega$.



FIGURE 5.10

(a) Calculate the output voltage v_{o} for $i_B = 13 \mu\text{A}$. (b) If the input voltage v_{in} is increased to 1.5 V, what is the new value of i_B ? (c) If the input voltage v_{in} is decreased to -0.5 V, does the output voltage v_o increase or decrease? Explain.

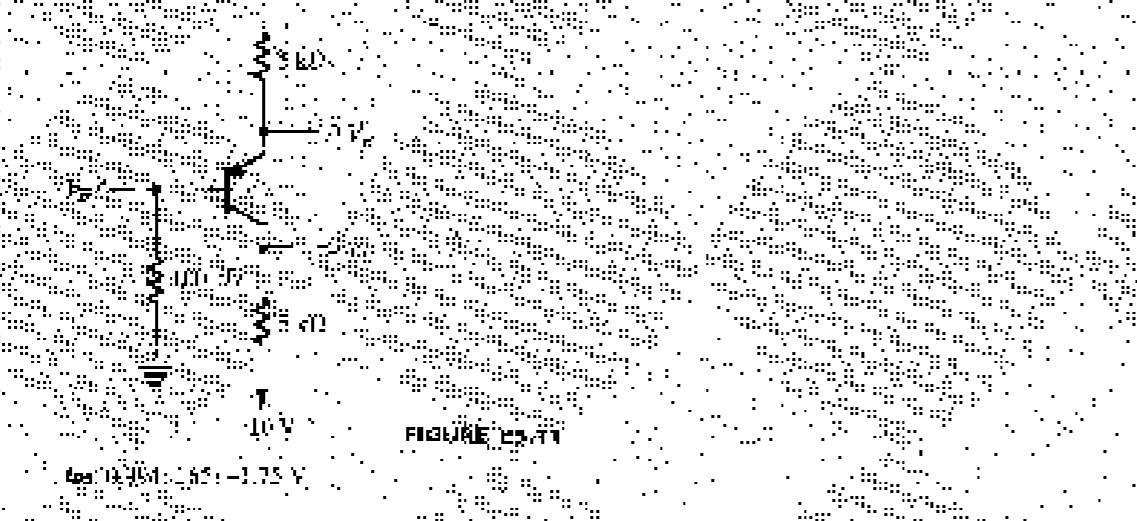
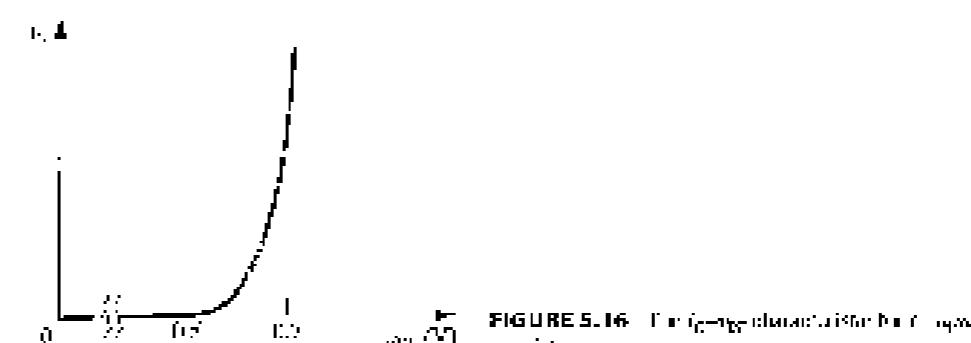


FIGURE 5.11

$i_B = 13 \mu\text{A}$; $i_C = 1.75 \text{ mA}$; $i_E = 1.88 \text{ mA}$. (a) What is the output voltage v_o ? (b) If the input voltage v_{in} is increased to 1.5 V, what is the new value of i_B ? (c) If the input voltage v_{in} is decreased to -0.5 V, does the output voltage v_o increase or decrease? Explain.

FIGURE 5.16 The i_v - v_v characteristic for a diode.

5.2.2 Graphical Representation of Transistor Characteristics

It is sometimes useful to describe the unidirectional i_v - v_v characteristics graphically. Figure 5.16 shows the i_v - v_v characteristic, which is the exponential relationship

$$i_v = I_v e^{(v_v - V_{t0})/kT}$$

which is identical (except for the value of constant k) to the diode i_v - v_v relationship. The i_v - v_{ce} and i_v - v_{be} characteristics are also exponential but with different scale constants I_v/kT for i_v , and i_v/kT for i_v . Since the constant of the exponential characteristic, $1/kT$, is quite high (≈ 40), the curve rises very sharply. For v_{ce} smaller than about 0.5 V, the current is negligibly small.⁵ Also, most of the normal current range i_{ce} lies in the range of 0.6 V to 0.8 V. In performing rapid first-order dc calculations we normally will assume that $V_{t0} \approx 0.7$ V, which is similar to the approach used in the analysis of diode circuits (Chapter 3). For a pnp transistor, the i_v - v_{ce} characteristic will look identical to that of Fig. 5.16 with v_{ce} replaced with v_{be} .

As in silicon diodes, the voltage across the collector-base junction decreases by about 2 mV for each rise of 1°C in temperature, provided that the junction is operating at a constant current. Figure 5.17 illustrates this temperature dependence by depicting i_v - v_{ce} curves at three different temperatures for an n-p-n transistor.

The Common-Base Characteristics. One way to describe the operation of a bipolar transistor is to plot i_v versus v_{ce} for various values of i_b . We have already constructed one such graph, in Fig. 5.9, which we used to introduce the saturation mode of operation. A conventional experimental setup for measuring such characteristics is shown in Fig. 5.18(a). Observe that in these measurements the base voltage is held constant, here at ground potential, and thus the base serves as a common terminal between the input and output ports. Consequently, the resulting set of characteristics, shown in Fig. 5.18(b), are known as common-base characteristics.

⁵ The i_v - v_{ce} characteristic is the BJT's counterpart of the i_v - v_{ce} characteristic of the enhancement-MOSFET. They share the important feature that in both cases the voltage has to exceed a "threshold" for the device to conduct appreciably. In the case of the MOSFET, there is a formal threshold voltage, V_{t0} , often taken typically in the range of 0.5 V to 1.0 V. For the BJT, there is no "apparent" threshold at approximately 0.5 V. The i_v - v_{ce} characteristic of the MOSFET is parabolic and thus is less steep than the i_v - v_{ce} characteristic of the BJT. This difference has a direct and significant implication for the value of transient resistance r_{ce} related with resistance r_{ce} .

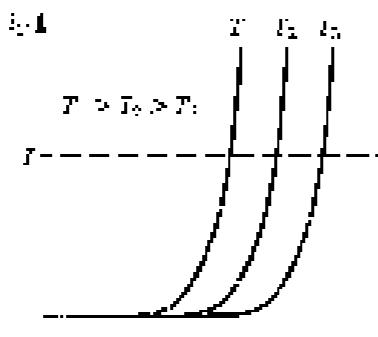


FIGURE 5.17 Effect of temperature on the I_c - V_{CE} characteristics. At a constant emitter current (saturation), $\alpha_{FE} = \text{constant} = 2 \text{ mV}^2/\text{C}$.

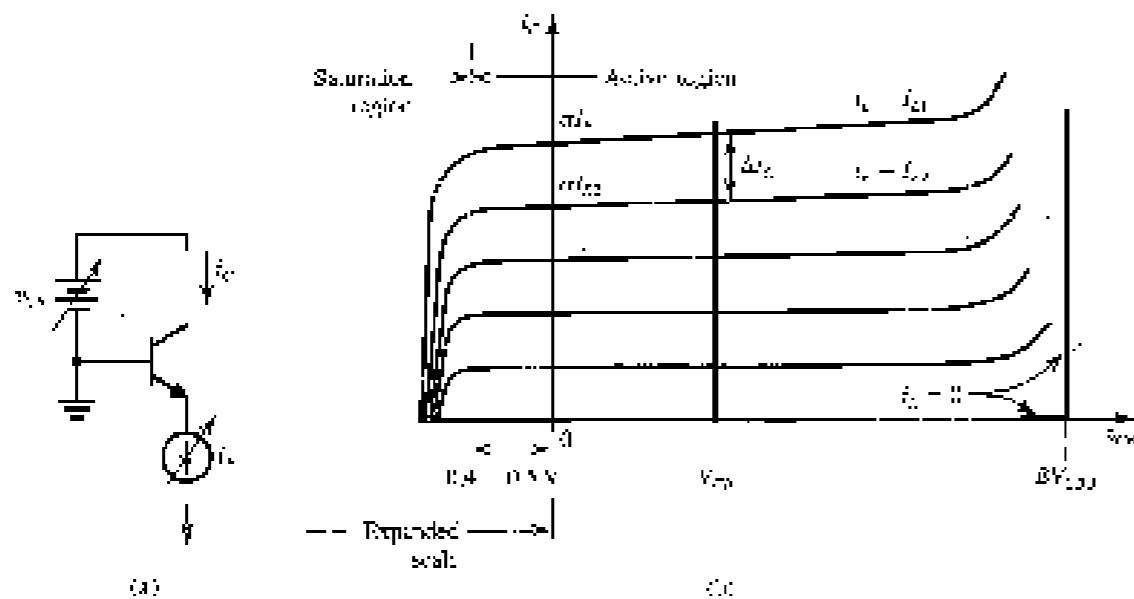


FIGURE 5.18 The I_c - V_B characteristics of an open transistor.

In the active region of operation, obtained for $V_{BE} > 0.1 \text{ V}$, or so, the I_c - V_{CE} curves deviate from our expectations in two ways. First, the curves are no longer perfectly straight lines but show a small negative slope, indicating that I_c depends slightly on V_{CE} in the active mode. We shall discuss this phenomenon shortly. Second, at relatively large values of V_{CE} , the collector current shows a rapid increase, which is a breakdown phenomenon that we will consider at a later stage.

As indicated in Fig. 5.18(b), each of the characteristic curves intersects the vertical axis at a current level equal to βI_E , where I_E is the constant emitter current at which the particular curve is measured. The resulting value of β is a total or large-signal β , that is, $\beta = I_C/I_E$, where I_C and I_E denote total collector and emitter current, respectively. Here we recall that β is appropriately called the common-base current gain. An incremental or small-signal β can be determined by measuring the change in I_C , ΔI_C , obtained as a result of changing I_E by an increment ΔI_E , $\alpha = \Delta I_C/\Delta I_E$. This measurement is usually made at a constant V_{CE} , as indicated in Fig. 5.18(b). Usually, the values of incremental and total β differ slightly, but we shall not make a distinction between the two in this book.

Finally, turning to the saturation region, the Ebers-Moll equations can be used to obtain the following expression for the I_c - V_{CE} curve in the saturation region (for $I_C = I_S$):

$$I_C = \alpha_{FE} I_S \left(\frac{1}{\sqrt{V_{CE}}} - \alpha_{FE} \right)^{1/2}. \quad (5.32)$$

We can use this equation to determine the value of V_{CE} at which I_C is reduced to zero. Recalling that the CBJ is much larger than the PBJ, the forward-voltage drop α_{FE} will be smaller than α_{PE} , resulting in a collector-emitter voltage, V_{CE} , of 0.1 V to 0.3 V in saturation.

EXERCISES

- 5.12 Consider a npn transistor with $\alpha_{FE} = 100$ and $\alpha_{PE} = 10$. If the base bias is varied, the emitter current I_E (in mA) versus collector voltage V_{CE} (in V) shows the following curves. Plot the temperature dependence of V_{CE} at $I_E = 1 \text{ mA}$ if the collector current is supplied through a 1 k Ω resistor. Assume that the temperature coefficient of α_{FE} is $+0.01^\circ\text{C}^{-1}$.
- 5.13 Based on the data in Exercise 5.12, calculate the I_c - V_{CE} relationship with the following circuit. Assume that the load resistance is $10 \text{ k}\Omega$ and the supply voltage V_{CC} is 12 V. The load line has a negative slope of $-0.01 \text{ V}/\text{V}$ and an intercept of 12 V. Calculate the operating point for the transistor (assuming $\alpha_{FE} = 100$) and round it to 0.01 V. Repeat for $\alpha_{FE} = 0.01$.
- Ans. $V_{CE} = 0.615 \text{ V}$, $V_{BE} = 0.535 \text{ V}$.

5.2.3 Dependence of I_c on the Collector Voltage—The Early Effect

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that their I_c - V_{CE} characteristics are not perfectly horizontal straight lines. To see this dependence more clearly, consider the circuit shown in Fig. 5.19(a). The transistor is connected in the common-emitter configuration; that is, here the emitter serves as a common terminal between the input and output ports. The voltage V_{CE} can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of V_{CE} , the corresponding I_c - V_{CE} characteristic curve can be measured point-by-point by varying the dc source connected between collector and emitter and measuring the corresponding collector current. The result is the family of I_c - V_{CE} characteristic curves shown in Fig. 5.19(b) and known as common-emitter characteristics.

At low values of V_{CE} , as the collector voltage goes below half of the base by more than 0.1 V, the collector-base junction becomes forward biased and the transistor leaves the active mode and enters the saturation mode. We shall shortly look at the details of the I_c - V_{CE} curves in the saturation region. At this time, however, we wish to examine the characteristic curves in the active region in detail. We observe that the characteristic curves, though still straight lines, have finite slopes. In fact, when extrapolated, the characteristic lines meet at a point on the negative v_{ce} axis, at $v_{ce} = -V_0$. The voltage V_0 , a positive number, is a parameter for the particular BJT, with typical values in the range of 50 V to 100 V. It is called the Early voltage, after J. M. Early, the engineering scientist who first studied this phenomenon.

At a given value of v_{ce} , increasing v_{ce} increases the reverse-bias voltage on the collector-base junction and thus increases the width of the depletion region of this junction (refer to Fig. 5.3). This in turn results in a decrease in the effective base width W . Recalling that I_c is inversely proportional to W (Eq. 5.1), we see that I_c will increase and that I_c increases proportionally. This is the Early effect.

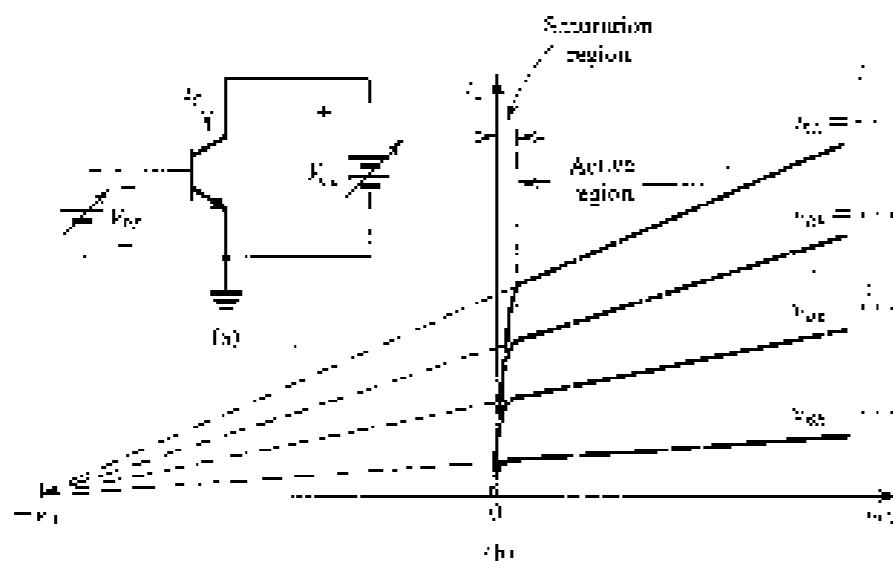


FIGURE 5.19 (a) Conceptual circuit for deriving the i - v characteristics of the BJT. (b) The i - v characteristics of a practical BJT.

The linear dependence of i_C on V_{CE} can be accounted for by assuming that i_B remains constant and including the factor $(1 + \alpha_{FE}/V_A)$ in the equation for i_C as follows:

$$i_C = I_{CBO} e^{\frac{qV_{CE}}{kT}} \left[1 + \frac{V_{BE}}{V_A} \right] \quad (5.36)$$

The nonzero slope of the i_C - V_{CE} straight line indicates that the output resistance looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o = \left. \frac{\partial V_{CE}}{\partial i_C} \right|_{V_{BE} \text{ constant}} \quad (5.37)$$

Using Eq. (5.36) we can show that

$$r_o = \frac{V_A - V_{CE}}{i_C} \quad (5.38)$$

where i_C and V_{CE} are the coordinates of the point Σ , which the BJT is operating on the particular i_B - V_{BE} curve (i.e., the curve obtained for $\alpha_{FE} = V_{BE}$). Alternatively, we can write

$$r_o = \frac{V_A}{I_P} \quad (5.38a)$$

where I_P is the value of the collector current with the Early effect neglected; that is,

$$I_P = I_{CBO} e^{\frac{qV_{CE}}{kT}} \quad (5.38b)$$

It is rarely necessary to include the dependence of i_C on r_{oE} in design and analysis. However, the finite output resistance r_o can have a significant effect on the gain of transistors amplifiers, as will be seen in later sections and chapters.

The output resistance r_o can be included in the circuit model of the transistor. This is illustrated in Fig. 5.20, where we show large-signal circuit models of a common-emitter open transistor operating in the active mode. Observe that diode D_2 models the exponential dependence of i_C on V_{CE} and thus has a scale current $I_{D2} = I_{CBO}/\beta$. Also note that the two models

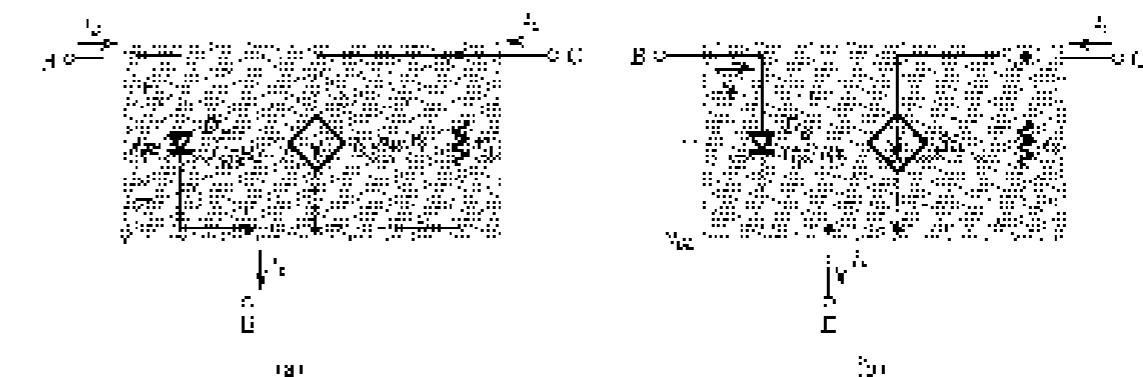
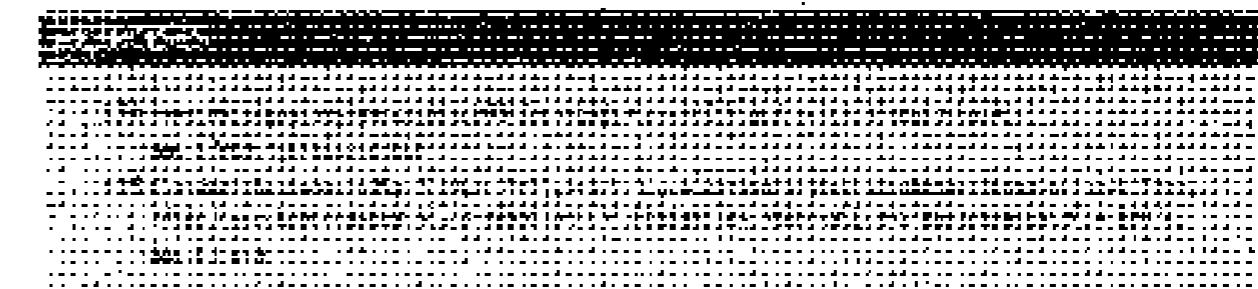


FIGURE 5.20 Large-signal equivalent circuit models of an n-p-n BJT operating in the active mode in the common-emitter configuration.

differ only in how the control function of the transistor is expressed: In the circuit of Fig. 5.20(a), voltage V_{CE} controls the collector current source, while in the circuit of Fig. 5.20(b), the base current i_B is the control parameter for the current source βi_B . Here we note that β represents the ideal current gain (i.e., when V_A is not present) of the transistor in its common-emitter configuration, which is the reason for its name, the common-emitter current gain.



5.2.4 The Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 5.21. Here the base current i_B rather than the base-emitter voltage V_{BE} is used as a parameter. That is, each i_C - V_{CE} curve is measured with the base fed with a constant current i_B . The resulting characteristics look similar to those in Fig. 5.19 except that here we show the breakdown phenomenon, which we shall discuss shortly. We should also mention that although it is not obvious from the graphs, the slope of the curves in the active regions of operation differ from the corresponding slope in Fig. 5.19. This, however, is a rather subtle point and beyond our interest at this moment.

The Common-Emitter Current Gain β . An important transistor parameter is the current-gain current gain β , or simply β . Thus far we have defined β as the ratio of the collector current to the collector-to-the-base current, and we have assumed that β is constant for a given transistor, independent of the operating conditions. In the following we examine these two points in some detail.

Consider a transistor operating in the active region at the point labeled Q in Fig. 5.21, that is, at a collector current I_{CQ} , a base current I_{BQ} , and a collector-emitter voltage V_{CEQ} . The

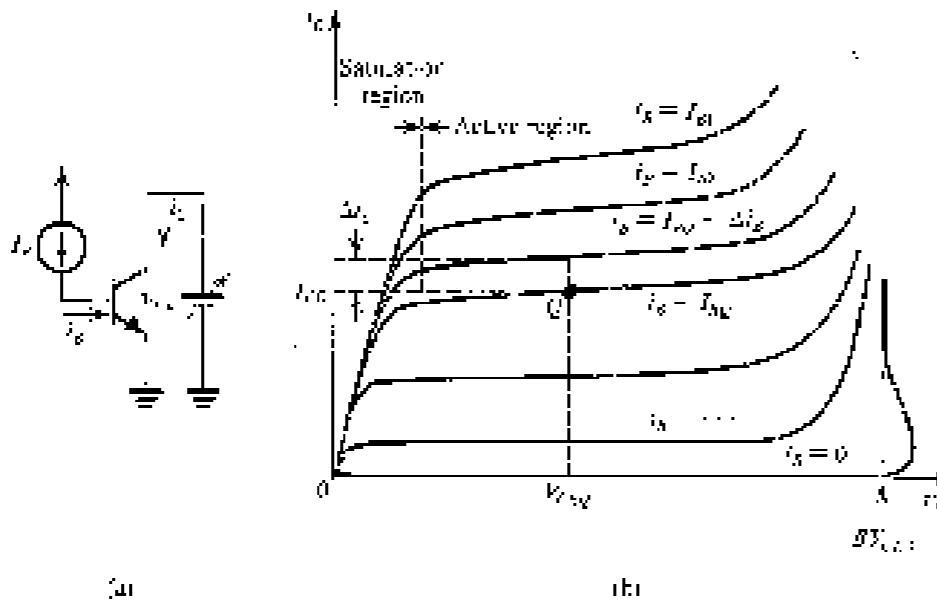


FIGURE 5.21 (a) Small-signal equivalent circuit of the BJT in common-emitter mode; (b) the origin of the saturation region in more detail.

ratio of the collector current to the base current is the large-signal or dc \$\beta\$:

$$\beta_{dc} = \frac{I_C}{I_{BQ}} \quad (5.39)$$

which is the \$\beta\$ we have been using in our description of transistor operation. It is commonly referred to as the mean (or dc) \$\beta\$ and is symbolized by the hybrid, or \$h\$, two-port parameter to characterize transistor operation (see Appendix B). One can define another \$\beta\$ based on incremental or small-signal quantities. Referring to Fig. 5.21 we see that while keeping \$V_{BE}\$ constant at the value \$V_{BEQ}\$, changing \$I_B\$ from \$I_{BQ}\$ to \$I_{BQ} + \Delta I_B\$ results in \$I_C\$ increasing from \$I_{CQ}\$ to \$(I_{CQ} + \Delta I_C)\$. Thus we can define the incremental or ac \$\beta\$:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}_{(V_{BE} = \text{constant})} \quad (5.40)$$

The magnitudes of \$\beta_{dc}\$ and \$\beta_{ac}\$ differ, typically by approximately 10% to 30%. In this book we shall not normally make a distinction between the two. Finally, we should mention that the small-signal \$\beta\$ or \$\beta_{ac}\$ is also known as the alternate symbol \$\beta_{ac}\$. Because the small-signal \$\beta\$ or \$\beta_{ac}\$ is defined and measured at a constant \$V_{BE}\$ — that is, with a zero signal component between collector and emitter — it is known as the short-circuit common-emitter current gain.

The value of \$\beta\$ depends on the current at which the transistor is operating, and the relationship is plotted in Fig. 5.22. The physical processes that give rise to this relationship are beyond the scope of this book. Figure 5.22 also shows the temperature dependence of \$\beta\$.

The Saturation Voltage \$V_{CESat}\$ and Saturation Resistance \$R_{CESat}\$. An expanded view of the common-emitter characteristics in the saturation region is shown in Fig. 5.23. The fact that the curves are "bunched" together in the saturation region implies that the incremental \$\beta\$ is lower here than in the active region. A possible operating point in the saturation region is that labeled X, it is characterized by a base current \$I_B\$, a collector current \$I_{CQ}\$, and a collector-emitter voltage \$V_{CESat}\$. Note that \$I_{CQ} < \beta_{dc} I_B\$. Since the value of \$I_{CQ}\$ is established

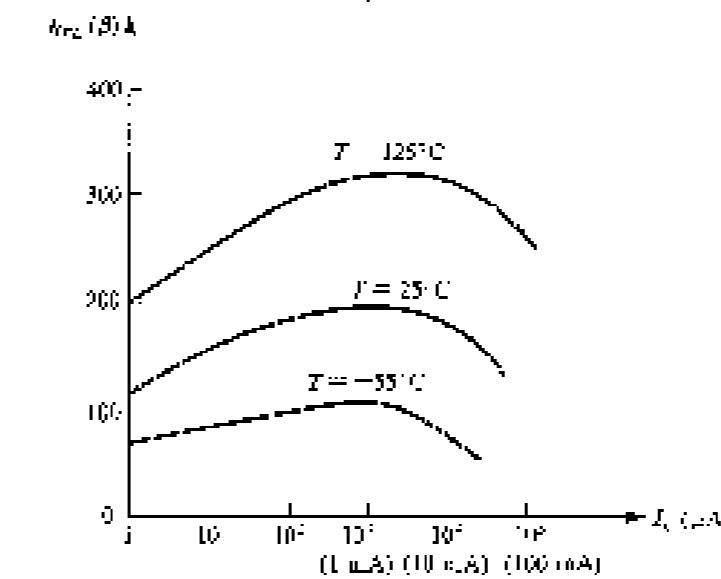


FIGURE 5.22 \$\beta\$ vs. \$I_C\$ for three temperatures in a modern integrated-circuit n-well silicon transistor intended for operation around 1 mA.

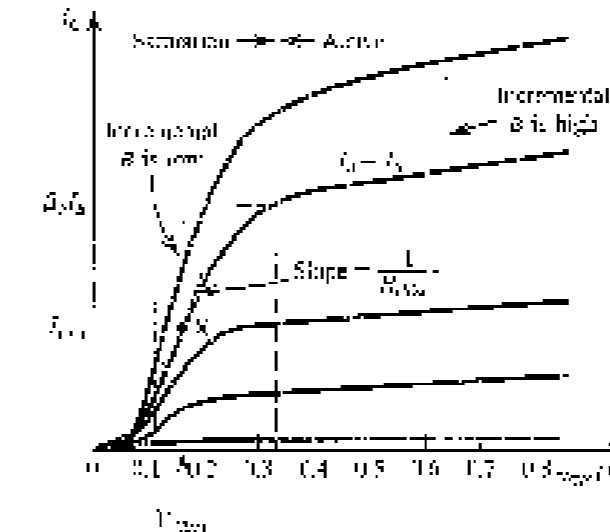


FIGURE 5.23 An expanded view of the common-emitter characteristics in the saturation region.

by the circuit designer, a saturated transistor is said to be operating at a forced \$\beta\$ given by

$$\beta_{forced} = \frac{I_C}{I_B} \quad (5.11)$$

Thus,

$$\beta_{forced} < \beta_{dc} \quad (5.12)$$

The ratio of \$\beta_{dc}\$ to \$\beta_{forced}\$ is known as the overdrive factor. The greater the overdrive factor, the deeper the transistor is driven into saturation and the lower \$V_{CESat}\$ becomes.

The i_c - v_{ce} curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance $R_{CE(sat)}$:

$$R_{CE(sat)} = \frac{\partial v_{CE}}{\partial i_c} \Big|_{v_{CE} = 0} \quad (5.43)$$

Typically, $R_{CE(sat)}$ ranges from a few ohms to a few tens of ohms.

Figure 5.24(b) shows one of the i_c - v_{ce} characteristic curves of the saturated transistor shown in Fig. 5.24(a). It is interesting to note that the curve intersects the v_{ce} axis at $v_{ce} = 0$ at a value, referred to as the v_{cesat} , voltage. We have also shown in Fig. 5.24(b) the output or operating point X of slope $1/R_{CE(sat)}$. When extrapolated, the tangent intersects the v_{ce} -axis at a voltage $V_{CE(sat)}$, typically approximately 0.1 V. It follows that the i_c - v_{ce} characteristic of a saturated transistor can be approximately represented by the equivalent circuit shown in Fig. 5.24(c). At the collector side, the transistor is represented by a resistor $R_{CE(sat)}$.

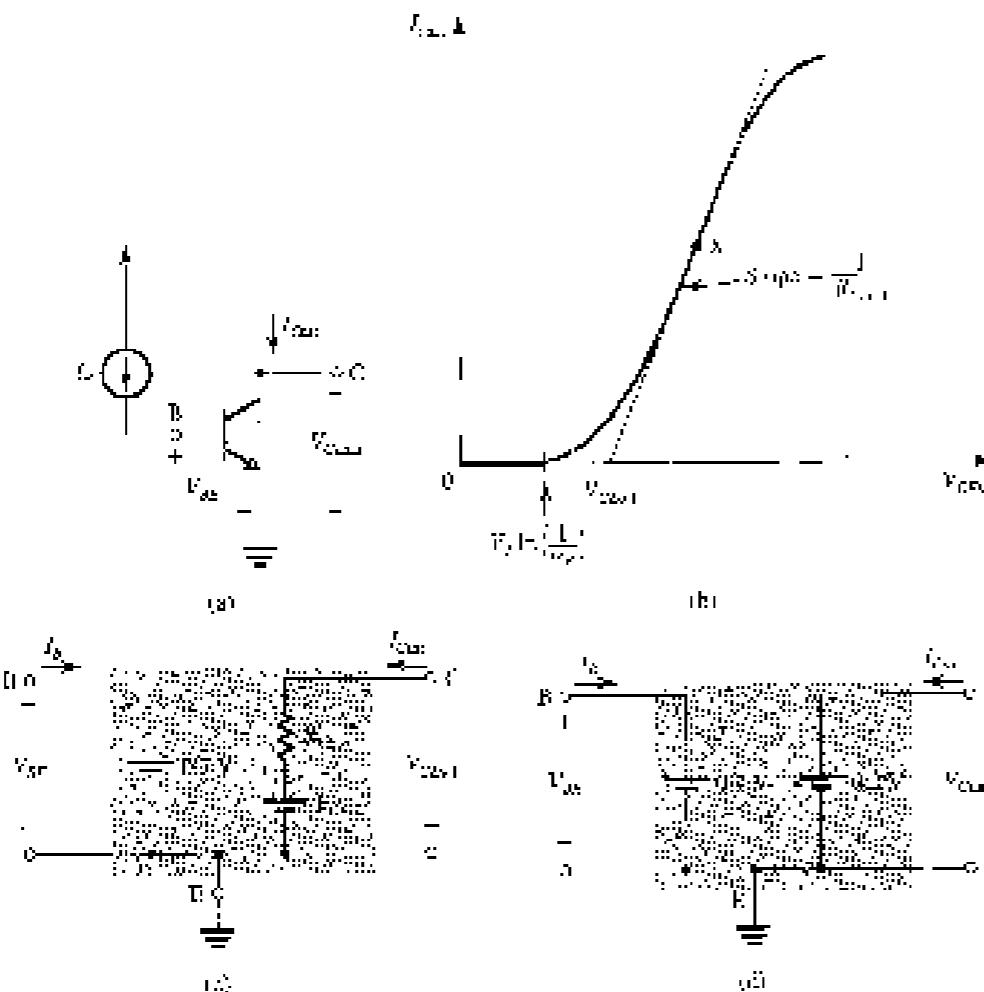


FIGURE 5.24 (a) Common-emitter equivalent circuit diagram with a constant base current I_B . (b) The i_c - v_{ce} characteristic curve corresponding to $v_B = I_B$. The curve can be approximated by a straight line of slope $1/R_{CE(sat)}$. (c) Equivalent circuit representation of the saturated transistor. (d) Amplified equivalent circuit model of the saturated transistor.

series with a voltage $V_{CE(sat)}$. Thus the saturation voltage $V_{CE(sat)}$ can be found from:

$$V_{CE(sat)} = V_{CE(0)} + I_{C(sat)}R_{CE(sat)} \quad (5.44)$$

Typically, $V_{CE(sat)}$ falls in the range of 0.1 V to 0.3 V. For many applications the even simpler model shown in Fig. 5.24(d) suffices. The collector voltage of a saturated transistor, though small, makes the BJT less attractive as a switch than the MOSFET, whose i_v - v characteristics go right through the origin of the i_v - v plane.

It is interesting and instructive to use the Shockley model to derive analytical expressions for the characteristics of the saturated transistor. Toward that end we use Eqs. (5.34) and (5.37), substitute $b_2 = I_B$, and neglect the small terms that do not scale exponentially, thus,

$$I_C = \frac{I_B}{\beta_1} e^{v_{ce}/V_T} + I_{C(sat)} e^{v_{ce}/V_T} \quad (5.45)$$

$$I_C = I_B e^{v_{ce}/V_T} + \frac{I_{C(sat)}}{\beta_1} e^{v_{ce}/V_T} \quad (5.46)$$

Dividing Eq. (5.46) by Eq. (5.45) and writing $v_{ce} = v_{ce(0)} + v_{ce}$ enables us to express v_{ce} in the form

$$v_{ce} = (I_B/I_C) \left(\frac{v_{ce(0)} - V_T}{e^{v_{ce}/V_T} + \frac{I_{C(sat)}}{I_B}} \right) \quad (5.47)$$

This is the equation of the i_c - v_{ce} characteristic curve obtained when the base is driven with a constant current I_B . Figure 5.25 shows a typical plot of the normalized collector current $i_c/(I_B \beta_1)$.

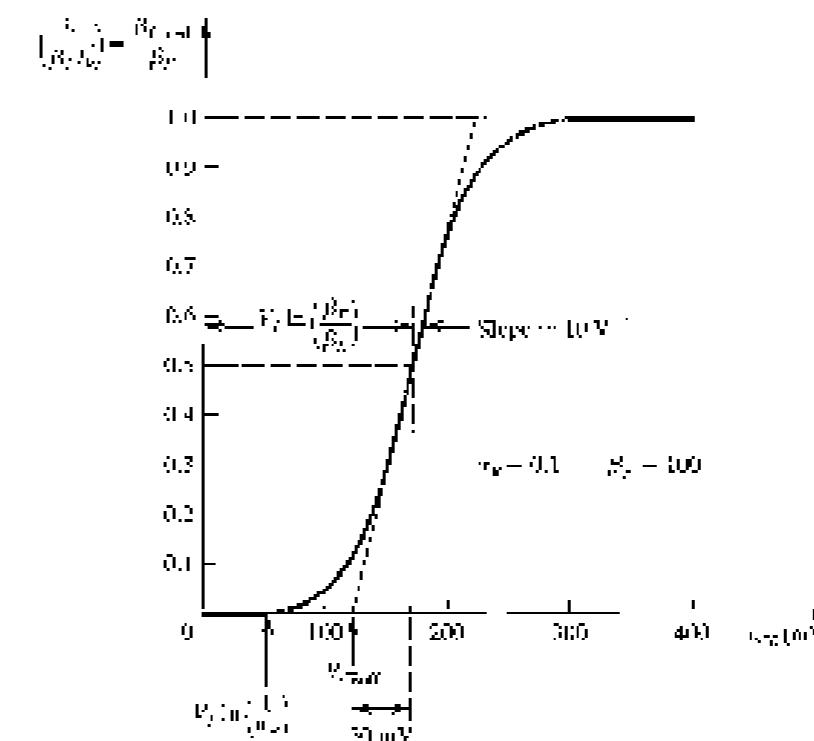


FIGURE 5.25 Plot of the normalized i_c versus v_{ce} for an operating condition with $I_B = 100$ and $r_V = 0.1$. This is a plot of Eq. (5.47), which is derived using the Shockley model.

which is equal to (β_{max}/β_0) , versus i_C . As shown, the curve can be approximated by a straight line coincident with the tangent at the point $\beta_{max}/\beta_0 = 0.5$. It can be shown that this tangent has a slope of approximately 10^{-4} V^{-1} , independent of the transistor parameters. Thus,

$$\theta_{max} = 1/10\beta_0 T_A \quad (5.48)$$

Other important parameters of the normalized plot are indicated in Fig. 5.25. Finally, we can obtain an expression for $V_{CE(sat)}$ by substituting $i_C = I_{sat} = \beta_{max}i_B$ and $v_{ce} = V_{CE(sat)}$ in Eq. (5.47),

$$V_{CE(sat)} = V_T \ln \frac{1 + (\beta_{max} + 1)/\beta_0}{1 - (\beta_{max}/\beta_0)} \quad (5.49)$$

EXERCISES

- 5.16 A NPN transistor operating at $T_A = 27^\circ\text{C}$ has $\beta_0 = 100$ and $\beta_{max} = 1000$. The operating junction voltage is $V_{BE} = 0.7\text{ V}$ and the value of V_T at $i_B = 0$ is 26 mV . Find the collector current I_C and the collector-to-emitter voltage V_{CE} when the transistor is operating in the active mode at $i_B = 10\text{ mA}$.

Ans. 30 mA ; 100 mV ; 118 mV ; $140 \pm 2\text{ mV}$

- 5.17 A measurement on a standard BJT operating in saturation mode indicates that the collector current is $I_C = 100\text{ mA}$ at $V_{CE} = 10\text{ V}$ and $i_B = 10\text{ mA}$. What are the values of the saturation voltage $V_{CE(sat)}$ and the saturation current I_{sat} ?

5.2.5 Transistor Breakdown

The maximum voltages that can be applied to a BJT are limited by the EBJ and CBJ breakdown effects that follow the avalanche multiplication mechanism described in Section 5.7.1. Consider first the common-base configuration. The i_C-v_{ce} characteristics in Fig. 5.16(b) indicate that for $i_B = 0$ (i.e., with the emitter open-circuited) the collector or base junction breaks down at a voltage denoted by BV_{BZ} . For $i_B > 0$, breakdown occurs at voltages smaller than BV_{BZ} . Typically, BV_{BZ} is greater than 30 V .

Next consider the common-emitter characteristics of Fig. 5.21, which show breakdown occurring at a voltage BV_{CE} . Here, although breakdown is still of the avalanche type, the details of the characteristic are more complex than in the common-base configuration. We will not explain these in detail; it is sufficient to point out that typically BV_{CE} is about half BV_{BZ} . On transistor data sheets, BV_{CE} is sometimes referred to as the sustaining voltage V_{Ker} .

Breakdown of the CBJ in either the common-base or common-emitter configuration is non-destructive as long as the power dissipation in the device is kept well below its limits. This, however, is not the case with the breakdown of the collector-base junction. The EBJ breaks down in an avalanche manner at a voltage BV_{BC} much smaller than BV_{BZ} . Typically, BV_{BC} is in the range of 6 V to 8 V , and the breakdown is destructive in the sense that the β of the transistor is permanently reduced. This does not prevent use of the BJT as a varistor diode to generate reference voltages in IC design. In such applications one is not concerned with the β -degradation

effect. A circuit arrangement to prevent EBJ breakdown in IC amplifiers will be discussed in Chapter 9. Transistor breakdown and the maximum allowable power dissipation are important parameters in the design of power amplifiers (Chapter 14).

EXERCISE

- 5.18 A common-emitter circuit is designed to have a voltage gain of $A_v = 100$ at $f = 100\text{ Hz}$.

What value of R_E would you choose if $V_{CC} = 12\text{ V}$, $R_C = 1\text{ k}\Omega$, and $R_B = 10\text{ k}\Omega$?

Ans. $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$

5.19 A common-emitter circuit is designed to have a voltage gain of $A_v = 100$ at $f = 100\text{ Hz}$.

What value of R_E would you choose if $V_{CC} = 12\text{ V}$, $R_C = 1\text{ k}\Omega$, and $R_B = 10\text{ k}\Omega$?

Ans. $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$

5.20 A common-emitter circuit is designed to have a voltage gain of $A_v = 100$ at $f = 100\text{ Hz}$.

What value of R_E would you choose if $V_{CC} = 12\text{ V}$, $R_C = 1\text{ k}\Omega$, and $R_B = 10\text{ k}\Omega$?

Ans. $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$

5.21 A common-emitter circuit is designed to have a voltage gain of $A_v = 100$ at $f = 100\text{ Hz}$.

What value of R_E would you choose if $V_{CC} = 12\text{ V}$, $R_C = 1\text{ k}\Omega$, and $R_B = 10\text{ k}\Omega$?

Ans. $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$; $10\text{ k}\Omega$; $100\text{ }\mu\text{A}$

5.2.6 Summary

We conclude our study of the current-voltage characteristics of the BJT with a summary of important results in Table 5.3.

5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

Having studied the terminal characteristics of the BJT, we are now ready to consider its two major areas of application: as a signal amplifier² and as a digital-circuit switch. The basis for the amplifier application is the fact that when the BJT is operated in the active mode, it acts as a voltage-controlled current source. Changes in the base-emitter voltage give rise to changes in the collector current i_C . Thus in the active mode the BJT can be used to implement a transconductance amplifier (see Section 1.5). Voltage amplification can be obtained simply by passing the collector current through a load resistor R_L , as will be seen shortly.

² An introduction to amplifiers from an external terminals point of view is presented in Sections 1.1 and 1.5. It would be helpful for readers who are not familiar with basic amplifier concepts to review this material before proceeding with the study of BJT amplifiers.

Since we are particularly interested in linear amplification, we will hence devise a way to achieve it in the face of the highly nonlinear behavior of the transistor, namely, that the collector current i_C is exponentially related to v_{BE} . We will use the approach described in general terms in Section 1.4. Specifically, we will bias the transistor to operate at a dc base-emitter voltage V_{BE} , and a corresponding dc collector current I_{C0} . Then we will superimpose the signal to be amplified, v_{in} , on the dc voltage V_{BE} . By keeping the amplitude of the signal v_{in} small, we will be able to constrain the transistor to operate on a short, almost linear segment of the i_C-v_{BE} characteristic; thus, the change in collector current, i_C , will be linearly related to v_{in} . We will study the small-signal operation of the BJT later in this section and in greater detail in Section 5.5. First, however, we will look at the "big picture": We will study the total or large-signal operation of a BJT amplifier. From the transfer characteristic of the circuit we will be able to see clearly the region over which the circuit can be operated as a linear amplifier. We also will be able to see how the BJT can be employed as a switch.

5.3.1 Large-Signal Operation—The Transfer Characteristic

Figure 5.26(a) shows the basic structure (a sketch) of the most commonly used BJT amplifier, the grounded-emitter or common-emitter (CE) circuit. The total input voltage v_i (bias + signal) is applied between base and emitter; that is, $v_{BE} = v_i$. The total output voltage v_o (bias + signal) is taken between collector and ground; that is, $v_{CE} = v_{oB}$. Resistor R_L has two functions: to establish a dc bias voltage at the collector, and to convert the collector signal current i_C to an output voltage, v_{oB} or v_o . The supply voltage V_{CC} is needed to bias the BJT as well as to supply the power needed for the operation of the amplifier.

Figure 5.26(b) shows the voltage transfer characteristic of the CE circuit of Fig. 5.26(a). To understand how this characteristic arises, we first express v_o as

$$v_o = v_{oB} = V_{CC} - R_L i_C \quad (5.50)$$

Next we observe that since $v_{BE} = v_i$, the transistor will be effectively cutoff for $v_i < 0.5$ V or so. Thus, for the range $0 < v_i < 0.5$ V, i_C will be negligibly small, and v_o will be equal to the supply voltage V_{CC} (segment XY of the transfer curve).

As v_i is increased above 0.5 V, the transistor begins to conduct, and i_C increases. From Eq. (5.50), we see that v_o decreases. However, since initially i_C will be large, the BJT will be operating in the active mode, which gives rise to the sharply descending segment YZ of the voltage transfer curve. The equation for this segment can be obtained by substituting in Eq. (5.50) the active-mode expression for i_C , namely,

$$\begin{aligned} i_C &\equiv I_{C0} e^{V_i/V_T} \\ &= I_{C0} e^{v_i/V_T} \end{aligned}$$

where we have, for simplicity, neglected the Early effect. Thus we obtain

$$v_o = V_{CC} - R_L I_{C0} e^{v_i/V_T} \quad (5.51)$$

We observe that the exponential term in this equation gives rise to the steep slope of the YZ segment of the transfer curve. Active mode operation ends when the collector voltage (v_{CE} or v_{oB}) falls by 0.4 V or so below that of the base (v_{BE} or v_i). At this point, the BJT turns off, and the transistor enters the saturation region. This is indicated by point Z on the transfer curve.

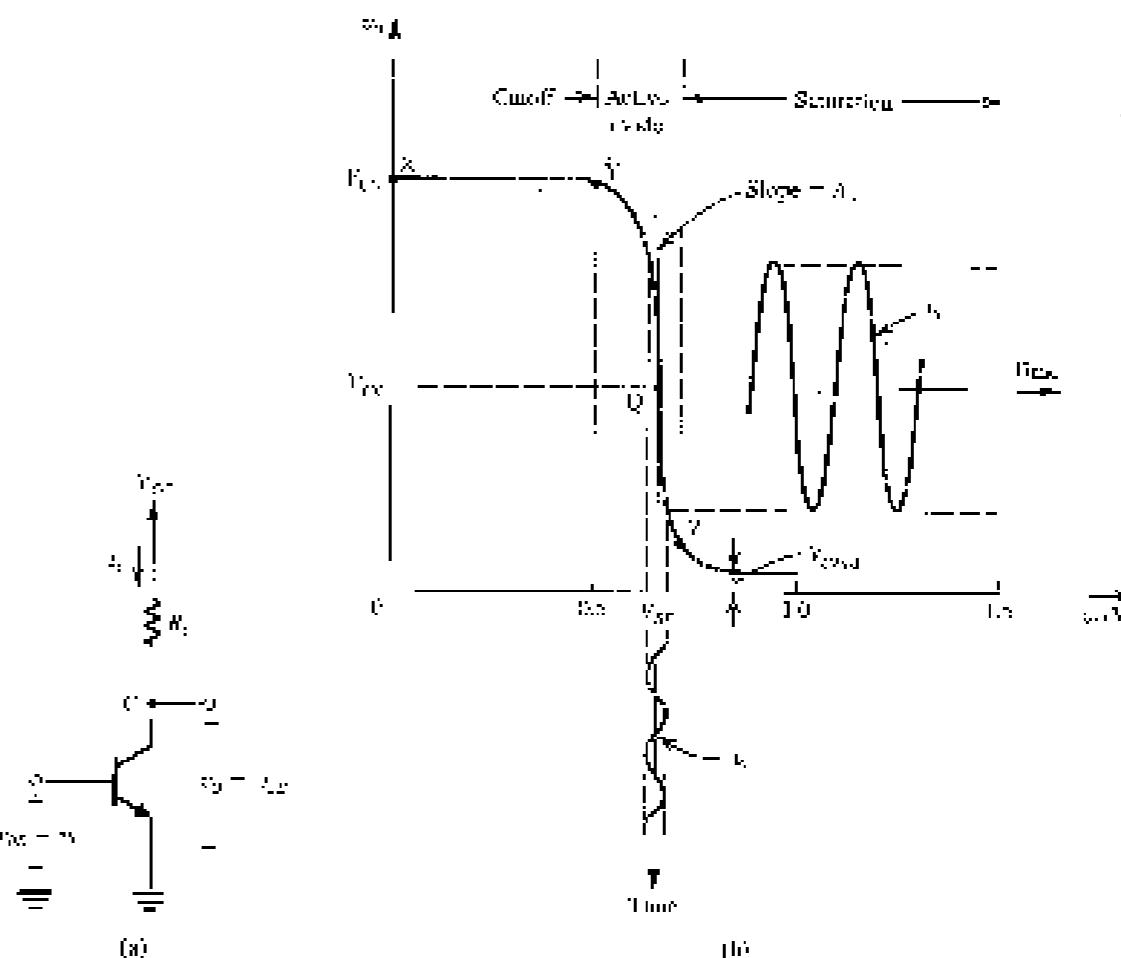


FIGURE 5.26. (a) Basic common-emitter amplifier circuit. (b) Transfer characteristic i_C vs. v_{BE} of the circuit in (a). The amplifier is biased at a point Q, and a small AC signal v_{in} is superimposed on the dc bias voltage v_{BE} . The resulting output signal v_o appears superimposed on the dc collector voltage v_{oB} . The amplitude of v_o is larger than that of v_{in} by the voltage gain A_v .

Observe that a further increase in v_{BE} causes v_{oB} to decrease only slightly; in the saturation region, $v_{oB} = V_{CESat}$, which falls in the narrow range of 0.1 V to 0.2 V. It is the low-current V_{CESat} that gives this region of BJT operation the name saturation. The collector current will also remain nearly constant at the value I_{C0} .

$$I_{C0} = \frac{V_{CC} - V_{CESat}}{R_L} \quad (5.52)$$

We recall from our study of the saturation region of operation in the previous section that the saturated BJT exhibits a very small resistance R_{CE0} between its collector and emitter. Thus, when saturated, the transistor in Fig. 5.26 provides a low-resistance path between the collector node C and ground and hence can be thought of as a closed switch. On the other hand, when the BJT is cut off, it conducts negligibly small (ideally zero)

current and thus acts as an open switch, effectively disconnecting node C from ground. The status of the switch (i.e., open or closed) is determined by the value of the control voltage V_{BE} . Very shortly, we will show that the BJT voltage can also be controlled by the base current.

5.3.2 Amplifier Gain

To operate the BJT as a linear amplifier, it must be biased at a point in the active region. Figure 5.26(b) shows such a bias point, labeled Q (for quiescent point), and characterized by a dc base-emitter voltage V_{BEQ} and a dc collector-emitter voltage V_{CEQ} . If the collector current at this value of V_{BE} is denoted I_C , that is,

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \quad (5.52)$$

then from the circuit in Fig. 5.26(a) we can write

$$V_{CE} = V_{CC} - R_C I_C \quad (5.53)$$

Now, if the signal to be amplified, v_i , is superimposed on V_{BE} and kept sufficiently small, as indicated in Fig. 5.26(b), the instantaneous operating point will be constrained to a relatively short, almost linear segment of the transfer curve around the bias point Q. The slope of this linear segment will be equal to the slope of the tangent to the transfer curve at Q. This slope is the voltage gain of the amplifier for small input signals around Q. An expression for the small-signal gain A_v can be found by differentiating the expression in Eq. (5.51) and evaluating the derivative at point Q; that is, for $v_i = V_{BEQ}$,

$$A_v = \left. \frac{dV_{CE}}{dV_i} \right|_{V_{BE}=V_{BEQ}} \quad (5.54)$$

Thus,

$$A_v = -\frac{1}{V_T} I_S e^{\frac{V_{BEQ}}{V_T}} R_C$$

Now, using Eq. (5.52) we can express A_v in compact form:

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{BEQ}}{V_T} \quad (5.55)$$

where V_{BEQ} is the dc voltage drop across R_C .

$$V_{BEQ} = V_{BE} - V_{CEQ} \quad (5.56)$$

Observe that the CE amplifier is inverting, that is, the output signal is 180° out of phase relative to the input signal. The simple expression in Eq. 5.55 indicates that the voltage gain of the common-emitter amplifier is the ratio of the dc voltage drop across R_C to the thermal voltage V_T (≈ 25 mV at room temperature). It follows that to maximize the voltage gain we should use as large a voltage drop across R_C as possible. For a given value of V_{CEQ} , Eq. (5.57) indicates that an increase V_{BEQ} we have to operate at a lower V_{BE} . However, reference to Fig. 5.26(b) shows that a lower V_{BE} means a bias point Q closer to the end of the active-region segment, which might not leave sufficient room for the negative-cutoff signal swing

without the amplifier entering the saturation region. If this happens, the negative peaks of the waveform of v_o will be flattened. Indeed, it is the need to allow sufficient room for input signal swing that determines the most effective placement of the bias point Q on the active-region segment, V_A , of the transfer curve. Placing Q too high on this segment not only results in reduced gain (because V_{BE} is lower but could possibly limit the available positive signal swing). At the point where the positive-swing peak would be clamped off at a level equal to V_{CE} . Finally, it is useful to note that the theoretical maximum gain, A_v , is obtained by biasing the BJT at the edge of saturation, which of course would not leave any room for negative signal swing. The resulting gain is given by

$$A_v = \frac{V_{CE} - V_{CEQ}}{V_T} \quad (5.58)$$

Thus,

$$A_{max} = -\frac{V_{CE}}{V_T} \quad (5.59)$$

Although the gain can be increased by using a larger supply voltage, other considerations come into play when determining an appropriate value for V_{CE} . In fact, the trend has been toward using lower and lower supply voltages, currently approaching 1 V or so. At such low supply voltages, large gain values can be obtained by replacing the resistance R_C with a constant-current source, as will be seen in Chapter 6.



Consider a common-emitter circuit using a BJT having $I_S = 10^{-12}$ A, a collector resistor $R_C = 5.6$ kΩ, and a power supply $V_{CC} = 10$ V.

- Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C ?
- Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE} , find the amplitude of the output sine-wave signal (assume linear operation).
- Find the positive increment in v_{BE} (above V_{BEQ}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3$ V.
- Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff flow, i.e., $v_{CE} = 0.99V_{CEQ}$.

Solution

(a)

$$\begin{aligned} I_C &= \frac{V_{CE} + V_{BE}}{R_C} \\ &= \frac{10 - 3.2}{5.6} = 1.43 \text{ mA} \end{aligned}$$

The value of V_{CE} can be determined from

$$1 \times 10^{-1} = 10^{-1} e^{V_{CE}/V_T}$$

which results in

$$V_{CE} = 0.18 \text{ mV}$$

(b)

$$\begin{aligned} A_V &= -\frac{V_{CE}}{V_T} \\ &= -\frac{10 - 0.18}{0.026} = -372 \text{ mV} \end{aligned}$$

$$\hat{V}_C = 272 \times 0.005 = 1.36 \text{ V}$$

(c) For $i_{CQ} = 0.3 \text{ mA}$,

$$i_T = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA}$$

To increase i_C from 1 mA to 1.617 mA, i_{CQ} must be increased by

$$\begin{aligned} \Delta i_{CQ} &= V_T \ln \left(\frac{1.617}{1} \right) \\ &= 13 \text{ mV} \end{aligned}$$

(d) For $i_Q = 0.99V_{CE} = 0.9 \text{ V}$,

$$i_T = \frac{10 - 0.9}{6.8} = 0.547 \text{ mA}$$

To decrease i_C from 1 mA to 0.547 mA, i_{CQ} must change by

$$\begin{aligned} \Delta i_{CQ} &= V_T \ln \left(\frac{0.547}{1} \right) \\ &= -105.2 \text{ mV} \end{aligned}$$

EXERCISE

5.70 For the values given in the first column of Table 5.1, assume $V_T = 26 \text{ mV}$. If the collector current is increased to 1.5 mA, what will result? (a) V_{CE} (b) i_T (c) A_V (d) \hat{V}_C (e) i_{CQ} (f) Δi_{CQ} (g) i_T if V_{CE} is reduced to 0.5 V (h) ΔV_{CE} (i) Δi_T (j) ΔA_V (k) $\Delta \hat{V}_C$ (l) Δi_{CQ} (m) ΔV_{CE} (n) Δi_T (o) ΔA_V (p) $\Delta \hat{V}_C$

Given: $R_E = 10 \text{ k}\Omega$; $R_C = 10 \text{ k}\Omega$; $R_B = 100 \text{ k}\Omega$; $R_{CE} = 1 \text{ M}\Omega$; $i_{CQ} = 1 \text{ mA}$; $V_{CC} = 10 \text{ V}$; $V_{BE} = 0.7 \text{ V}$; $V_T = 26 \text{ mV}$

5.3.3 Graphical Analysis

Although formal graphical methods are off the practical scene in the analysis and design of most transistors circuits, it is alternative to verify graphically the operation of a simple transistor amplifier circuit. Consider the circuit of Fig. 5.27, which is similar to the circuit we have been studying except for an added resistor in the base lead, R_B . A graphical analysis of the operation of this circuit can be performed as follows: First, we have to determine the dc bias point. Because that end we set $v_i = 0$ and use the technique illustrated in Fig. 5.24 to determine the dc base current, i_{BQ} . We recall now to the i_C-v_{CE} characteristics shown in Fig. 5.20. We know that the operating point will lie on the i_C-v_{CE} curve corresponding to the value of i_{CQ} given earlier we have determined (by curve for $i_B = i_BQ$). Where it lies on the curve will be determined by the collector circuit. Specifically, the collector circuit imposes the constraint

$$v_{CE} = V_{CC} - i_C R_C$$

which can be rewritten as

$$i_C = \frac{V_{CC} - v_{CE}}{R_C} = \frac{1}{R_C} v_{CE}$$

which represents a linear relationship between v_{CE} and i_C . This relationship can be represented by a straight line, as shown in Fig. 5.28. Since R_C can be considered the amplifier load,

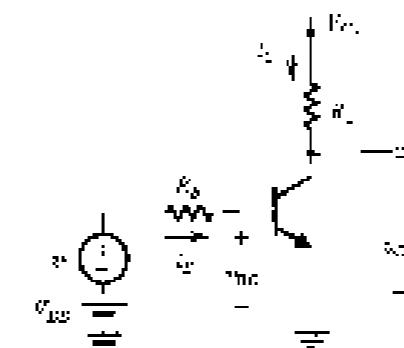


FIGURE 5.27 Circuit whose operation is to be analyzed graphically.

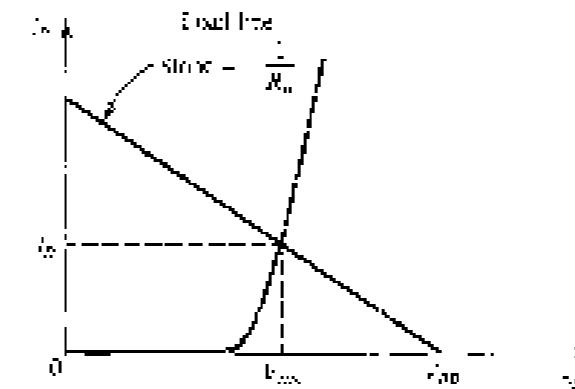


FIGURE 5.28 Graphical construction for determining the operating point in the circuit of Fig. 5.27.

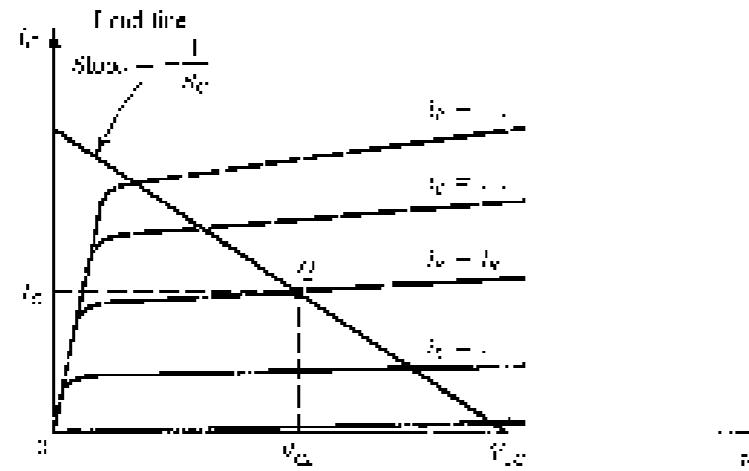


FIGURE 5.29 Graphical construction of the dc load line and the Q-point, corresponding to voltage \$V_{CE}\$ in the curve of Fig. 5.23.

The straight line of slope \$-\frac{1}{R_L}\$ is known as the load line.⁷ The dc bias point, or quiescent point, \$Q\$ will be at the intersection of the load line and the \$i_C - V_{CE}\$ curve corresponding to the base current \$i_B\$. The coordinates of point \$Q\$ give the dc collector current \$i_C\$ and the dc collector-to-emitter voltage \$V_{CE}\$. Observe that for an amplifier operation, \$Q\$ should be in the active region and furthermore should be located so close to \$Q_1\$ as to allow for a reasonable signal swing as the input signal \$v_i\$ is applied. This will become clearer shortly.

The situation when \$v_i\$ is applied is illustrated in Fig. 5.30(a), which shows a signal \$v_i\$, having a triangular waveform being superimposed on the dc voltage \$V_{BE}\$. Corresponding to each instantaneous value of \$V_{BE} = v_i(t)\$, one can draw a straight line with slope \$-\frac{1}{R_L}\$. Such an "instantaneous load line" intersects the \$i_C - V_{CE}\$ curve at a point whose coordinates give the total instantaneous values of \$i_C\$ and \$v_{CE}\$ corresponding to the particular value of \$V_{BE} + v_i(t)\$. As an example, Fig. 5.30(a) shows the straight lines corresponding to \$v_i = 0\$, \$v_i\$ at its positive peak, and \$v_i\$ at its negative peak. Now, if the amplitude of \$v_i\$ is sufficiently small so that the instantaneous operating point is confined to an almost-linear segment of the \$i_C - V_{CE}\$ curve, then the resulting signals \$v_C\$ and \$v_{CE}\$ will be triangular in waveform, as indicated in the figure. This, of course, is the small-signal approximation. In summary, the graphical construction in Fig. 5.30(a) can be used to determine the (small) instantaneous value of \$i_C\$ corresponding to each value of \$v_i\$.

Next, we move to the \$i_C\$-characteristics of Fig. 5.30(b). The operating point will move along the load line of slope \$-\frac{1}{R_L}\$ as it goes through the instantaneous values determined from Fig. 5.30(a). For example, when \$v_i\$ is at its positive peak, \$i_C = i_{C2}\$ (from Fig. 5.30(a)), and the instantaneous operating point in the \$i_C - V_{CE}\$ plane will be at the intersection of the load line and the curve corresponding to \$i_C = i_{C2}\$. In this way, one can determine the waveforms of \$i_C\$ and \$v_{CE}\$ and hence of the signal components \$v_C\$ and \$v_{CE}\$, as indicated in Fig. 5.30(b).

Effects of Bias-Point Location on Allowable Signal Swing. The location of the dc bias point in the \$i_C - V_{CE}\$ plane significantly affects the maximum allowable signal swing at the collector. Refer to Fig. 5.30(b) and observe that the positive peaks of \$v_{CE}\$ cannot go beyond

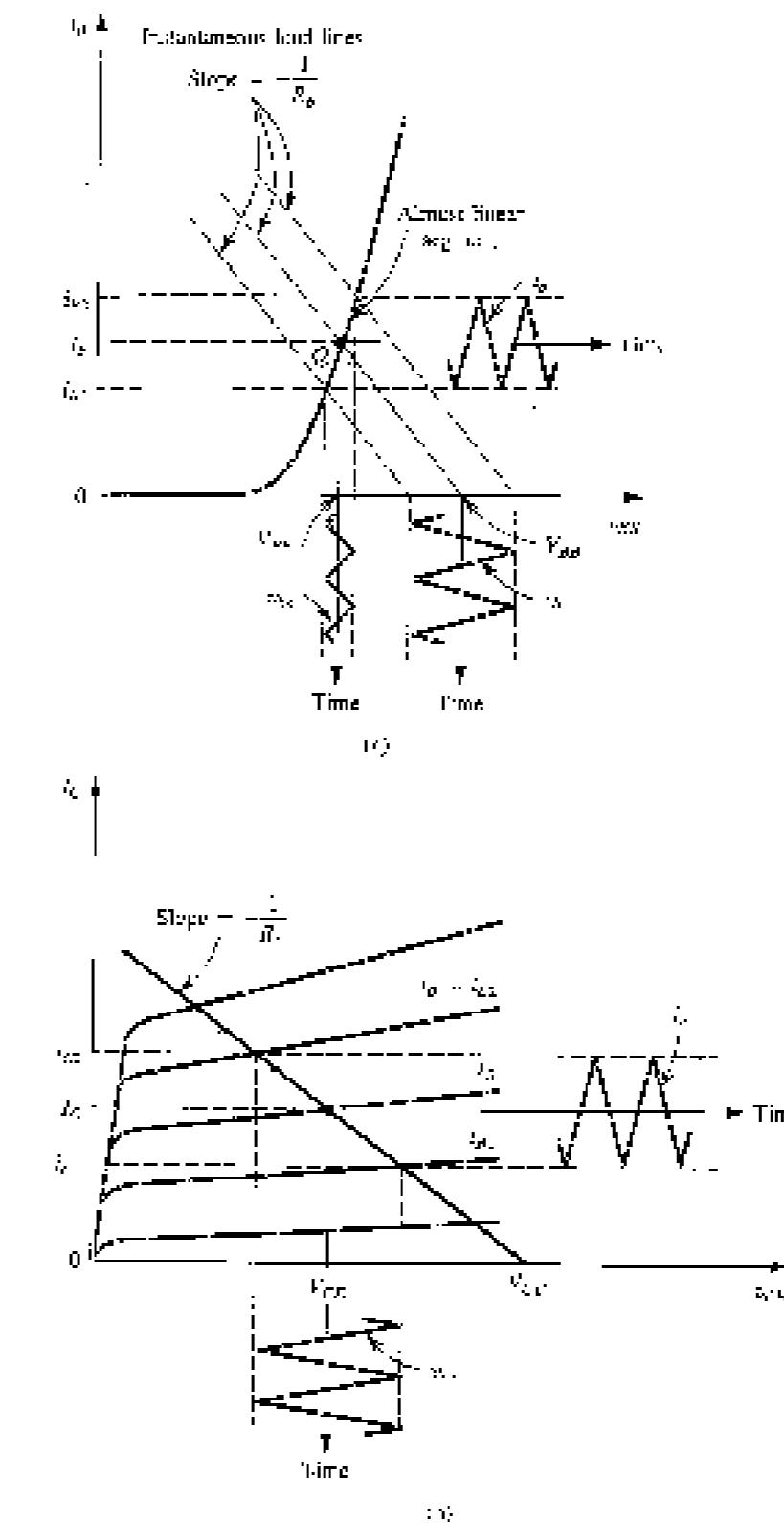


FIGURE 5.30 Graphical determination of the signal components \$v_C\$, \$i_C\$, and \$v_{CE}\$ when a signal is applied to \$i_C\$ superimposed on the \$v_i\$ voltage (Fig. 5.27).

⁷ The term load line is also employed for the straight line in Fig. 5.24.

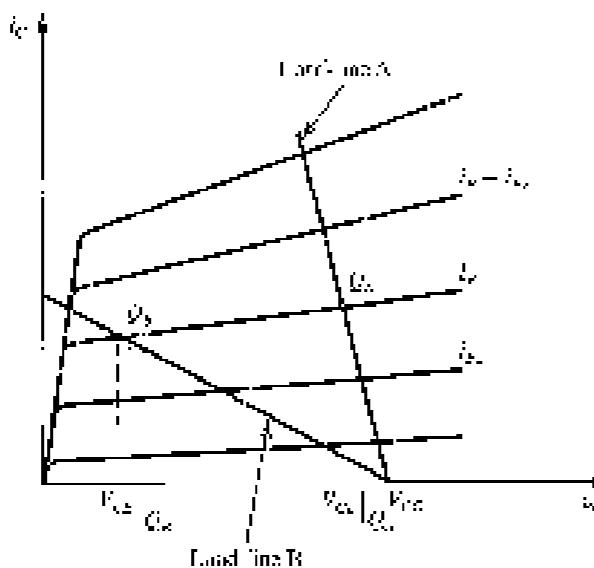


FIGURE 5.31 Effect of two-point load on total overshoot of signal swing; load m_1 and m_2 results in dead point \bar{x}_d which it can bypassing x_{th} which is the closure K_c , and thus, limits the positive swing of $x(t)$. At $t = t_0$ the system has stable limit cycle at \bar{x} in operating point less closer to the saturation region than limit cycle operating point of $x(t)$.

V_{BE} , otherwise the transistor enters the cutoff region. Similarly, the negative parts of v_x cannot extend below a few tenths of a volt (usually, 0.3 V), otherwise the transistor enters the saturation region. The location of the bias point in Fig. 5.36(b) allows for an approximately equal swing in each direction.

Next consider Fig. 5.31. Here we show two lines corresponding to two values of R . Line A corresponds to a low value of R_0 and results in the operating point Q_1 , where the value of V_{CE} is very close to V_{CE0} . Thus the positive swing of v_o will be severely limited; in this situation it is said that there is not sufficient "head room." On the other hand, line B, which corresponds to a large R_0 , results in the bias point Q_2 , where V_{CE0} is too low. Thus for line B, although there is ample room for the positive excursion of v_o (there is a lot of head room), the negative signal swing is severely limited by the proximity to the saturation region (there is not sufficient "tail room"). A compromise between these two situations is obviously called for.

EXERCISE

ANSWER: $\frac{1}{2} \cdot 10^{-10} \text{ J} = 5 \times 10^{-11} \text{ J}$

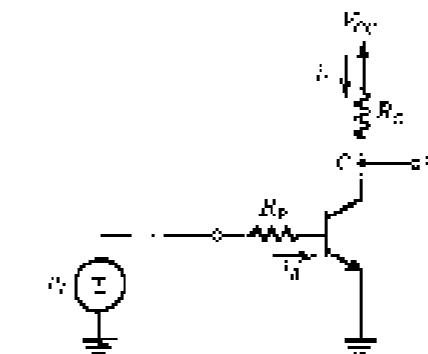


FIGURE 5.32 A diagram of the U.S. scale of biomass losses due to the BPP.

5.3.4 Operation as a Switch

To operate the BJT as a switch, we utilize the cut-off and the saturation modes of operation. To illustrate, consider once more the common-emitter circuit shown in Fig. 5.72 as the input v is varied. For v_{BE} less than about 0.5 V, the transistor will be cut-off; thus $i_B = 0$, $i_C = 0$, and $v_{CE} = V_{CC}$. In this state, node C is disconnected from ground; the switch is in the open position.

To turn the triode section on, we have to increase v_2 above 0.5 V. In fact, for appreciable currents to flow, v_{N2} should be about 0.7 V and v_2 should be higher. The base current, v_1 , will be

$$i_k = \frac{v_k - V_{\text{off}}}{k} \quad (5.60)$$

and the following current will

$$L = \mathcal{B}_\theta \quad (56)$$

which applies only when the source is in the active mode. This will be the case as long as the CBI is not forward biased, that is, as long as $v_{DS} < -0.4$ V, where v_D is given by

$$Y_0 = Y_{\text{obs}} + \delta_{\text{obs}} \quad (5.62)$$

Obviously, as v_T is increased, i_T will increase (Eq. 5.60). i_C will correspondingly increase (Eq. 5.61), and v_C will decrease (Eq. 5.62). Eventually, v_C will become lower than v_T by 0.1 V, at which point the transistor leaves the active region and enters the saturation region. This edge-of-saturation (EOS) point is defined by

$$I_{\text{Lumin}} = \frac{V_{\text{gr}}}{R_s} 0.3 \quad , \quad (5.63)$$

Where we have assumed that V_{eff} is approximately 0.2 V, per

$$(m=0), \quad \frac{I_{C\text{-BS}}}{S} \quad (3.64)$$

The corresponding value of α required to drive the transistor to the edge-of-saturation can be found from

$$V_{\text{max}} \equiv (v_{\text{max}}, R_{\text{eff}}, V_{\text{ext}}) \quad (3.18)$$

Increasing α above V_{BE0} increases the base current, which drives the transistor deeper into saturation. The collector-to-emitter voltage, however, decreases only slightly. As a reasonable approximation, we shall usually assume that for a saturated transistor, $V_{CE0} \approx 0.2$ V. The collector current then remains nearly constant at I_{C0} .

$$I_{\text{ext}} = \frac{V_{\text{ext}} - V_{\text{cell}}}{R_s} \quad (7.66)$$

Because these diodes are the base has very little effect on I_{CQ} , and therefore in this state the switch is closed with a low short-circuit resistance ($R_{on,low}$) and a small reverse voltage (V_{DSS}) (see Fig. 3.26c).

Finally, recall that in saturation one can force the transistor to operate at any desired β below its normal value, that is, the ratio of the collector current I_{CQ} to the base current can be set at will and is therefore called the forced β .

$$\beta_{(n,i)} = \frac{I_{\text{L},i}}{I} \quad (5.67)$$

A small (but) the ratio of I_{sat}/I_{max} is known as the overdrive factor.

The controller in Fig. 5.3.3 is specified to cover β in the range of 50 to 150. Find the value of K_{ctrl} such that saturation with an overshoot factor of at least 10.

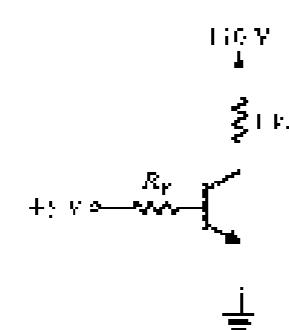


FIGURE 5.33 Case for Example 5.

Solution

8. You also can never be sure what the next doctor will say.

$$V_C = V_{\text{sat}} \approx 0.2 \text{ V}$$

The last collector sentence is given as

$$i_{c.v.} = \frac{110 - 0.2}{1} = 98 \text{ mA}$$

To satisfy the law, ship with the lowest S as need to provide a long current of 2.1 km.

$$L_{S, \text{soft}} = \frac{l_{\text{soft}}}{d} = \frac{1.8}{50} = 0.195 \text{ m}$$

For an investment factor of 10, the user can set aside the

$$(z = 12 \times 0.198 = 1.96 \text{ m})$$

Thus we require a value c_1 , c_2 such that

$$\frac{-5 - 0.7}{8} = -0.71$$

$$R_0 = \frac{4\pi}{16\pi} = 2 \text{ k}\Omega$$

EXERCISE

- 5.27 Consider the circuit in Fig. 5.27 for the case of $V_1 = -5 \text{ V}$, $V_2 = +5 \text{ V}$, $R_1 = 1 \text{ k}\Omega$, and $\beta = 100$. Calculate the base current and collector current, and the output voltage if the transistor is saturated. What value should R_1 be raised to in order to keep the transistor in the linear operating region? Ans.: $I_B = 1.8 \text{ mA}$, $I_C = 179.18 \text{ mA}$, $V_{out} = -4.99 \text{ V}$; $R_1 = 5.55 \text{ k}\Omega$.

5.4 BJT CIRCUITS AT DC

We are now ready to consider the analysis of BJT circuits to which only dc voltages are applied. In the following examples we will use the simple model in which V_{BE} of a cut-off transistor is 0.7 V and $|V_{CE}|$ of a saturated transistor is 0.2 V, and we will neglect the Early effect. Better models can, of course, be used to obtain more accurate results. This, however, is usually achieved at the expense of speed of analysis, and more importantly, it could impede the circuit designer's ability to gain insight regarding circuit behavior. Accurate results using elaborate models can be obtained using circuit simulation with SPICE, as we shall see in Section 3.1.1. Thus - a task always done in the final stages of a design and certainly before circuit fabrication. Computer simulation, however, is not a substitute for quick pencil-and-paper circuit analysis, an essential ability that aspiring circuit designers must master. The dc load-line analysis is a step in that direction.

As will be seen, in analyzing a circuit the first question that one must answer is: In which mode is the transistor operating? In some cases, the answer will be obvious. In many cases, however, it will not. Needless to say, as the reader gains practice and experience in transistor circuit analysis and design, the answer will be obvious in an ever larger proportion of problems. The answer, however, can always be determined by utilizing the following procedure:

Assume that the transistor is operating in the active mode, and proceed to determine the critical voltages and currents that correspond. Then check for consistency of the results with the assumption of active-mode operation; that is, is v_{CE} of an *n*-type transistor greater than -0.2 V for $v_{BE} < v_{CBO}$ and lower than $0 - V_T$? If the answer is yes, then our task is complete. If the answer is no, assume saturation-mode operation, and proceed to determine currents and voltages and then to check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to examine the ratio $|I_{SD}|/I_S$ and to verify that it is

lower than the transistor β ; i.e., $\beta_{\text{min}} < \beta$. Since β is a given transistor value over a wide range, one should use the lowest specified β for this test. Finally, note that the order of these two assumptions can be reversed.

Consider the circuit shown in Fig. 5.34(a), which is identical to Fig. 5.34(b) except that the collector-emitter voltage is now +10 V. We wish to determine the collector current I_C and the collector voltage V_C at steady state. We will assume that β is specified to be 100.

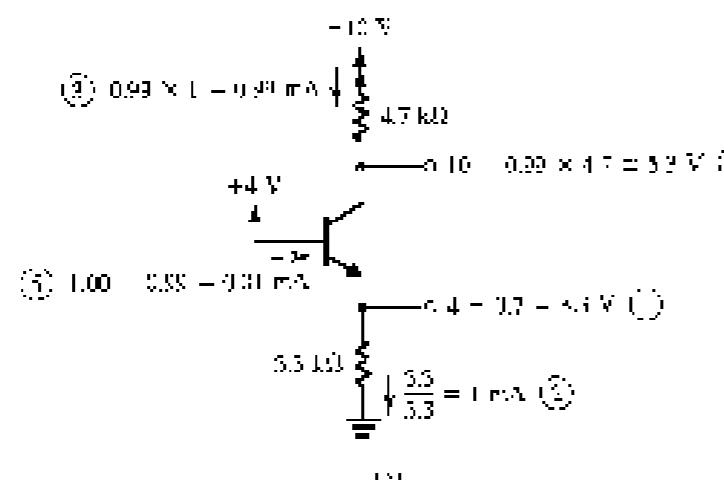
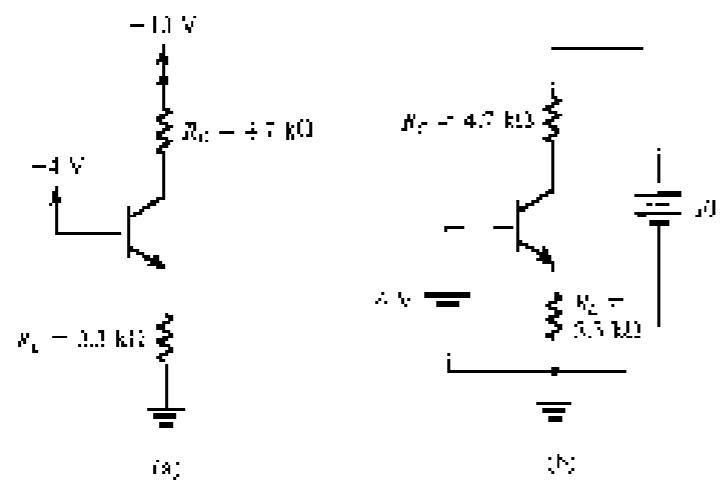


FIGURE 5.34 Analysis of the circuit for Example 5.4, (a) showing the circuit diagram, (b) showing the analysis steps in order.

Solution

Referring to the circuit in Fig. 5.34(a), we see that the base is connected to -4 V and the emitter is connected to ground through a resistance R_B . It therefore is safe to conclude that the base-emitter junction will be forward biased. Assuming that this is the case and assuming that V_{BE} is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \approx 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position: we know the voltage at the two ends of R_L and thus can determine the current I_L through it:

$$I_L = \frac{V_L - 0}{R_L} = \frac{5.3}{5.3} = 1 \text{ mA}$$

Since the collector is connected through R_C to the -10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which is essential for active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_L$$

The value of α is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} = 0.99$$

Thus I_C will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm's law to determine the collector voltage V_C :

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 = 5.2 \text{ V}$$

Since the base is at +4 V, the collector-base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode, as assumed.

It remains only to determine the base current I_B , as follows:

$$I_B = \frac{I_C}{\beta + 1} = \frac{1}{101} = 0.01 \text{ mA}$$

Before closing this example we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 5.34(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

FIGURE 5.35 Analysis of the circuit of Fig. 5.34(a) to determine the voltages in all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 5.34 except that the voltage at the base is now +6 V. Assuming that the transistor β is specified to be at least 50.

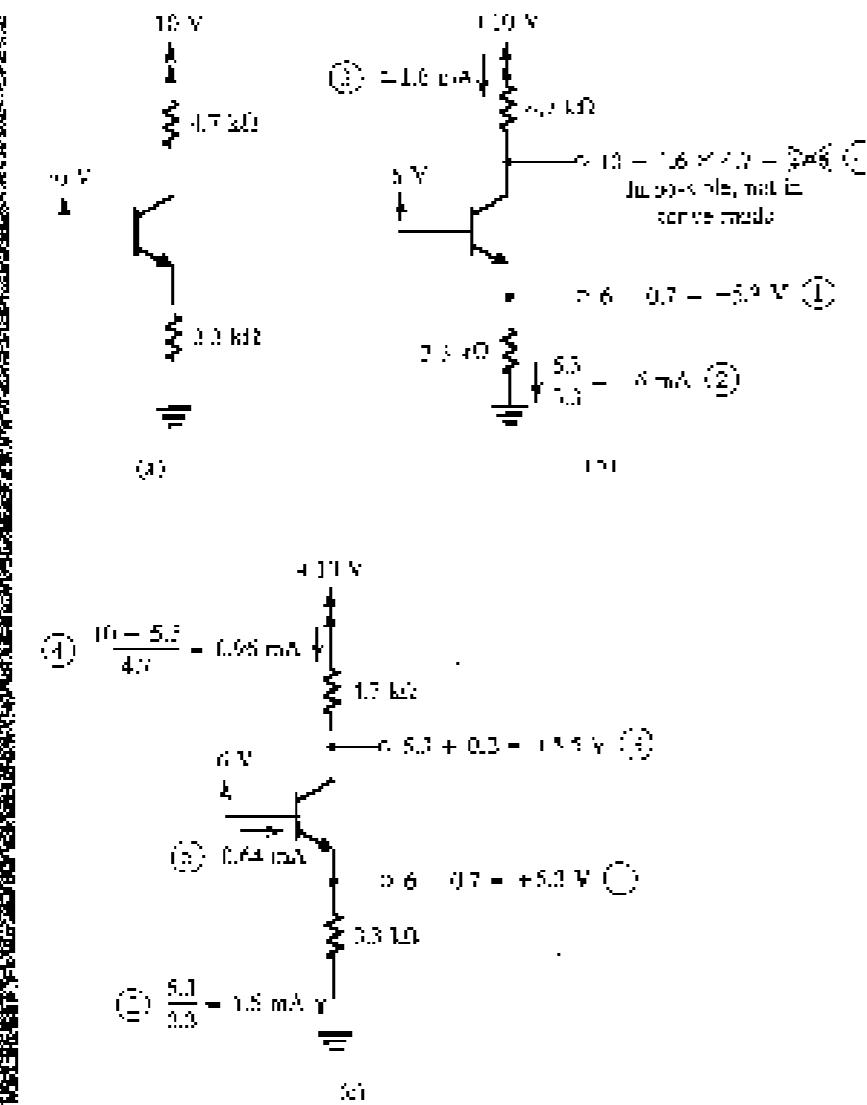


FIGURE 5.35 Analysis of the circuit in Fig. 5.35(a). Note that the circled numbers indicate the order of analysis steps.

Solution

Assuming active-mode operation, we have

$$V_1 = 6 - V_{BE} \approx 6 - 0.7 = 5.3 \text{ V}$$

$$I_E = \frac{V_1}{R_2} = \frac{5.3}{1.6} = 1.6 \text{ mA}$$

$$V_C = 10 - 1.6 \times I_P \approx 10 - 7.52 = 2.48 \text{ V}$$

The results of the analysis performed above are illustrated in Fig. 5.35(b).



Since the collector voltage calculated appears to be less than the base voltage by 0.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the saturation mode. Assuming this to be the case, we have

$$V_{CE} = 6 - 0.7 = 5.3 \text{ V}$$

$$I_C = \frac{V_1}{R_2} = \frac{5.3}{1.6} = 1.6 \text{ mA}$$

$$V_T = V_T + V_{CE(sat)} \approx 0.53 - 0.2 = 0.33 \text{ V}$$

$$I_C = \frac{10 - 5.3}{2.3} = 0.90 \text{ mA}$$

$$I_S = I_T - I_C = 1.6 - 0.90 = 0.64 \text{ mA}$$

Thus the transistor is operating at a forced β :

$$\beta_{forced} = \frac{I_C}{I_S} = \frac{0.90}{0.64} = 1.4$$

Since β_{forced} is less than the minimum specified value of β , the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of β should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified β . Obviously, if a transistor with the minimum β is saturated, then transistors with higher values of β will also be saturated. The details of the analysis are shown in Fig. 5.35(c), where the order of the analysis steps is indicated by the circled numbers.

Example 5.6

We wish to analyze the circuit in Fig. 5.36(b) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that discussed in Examples 5.4 and 5.5 except that the bias voltage is zero.

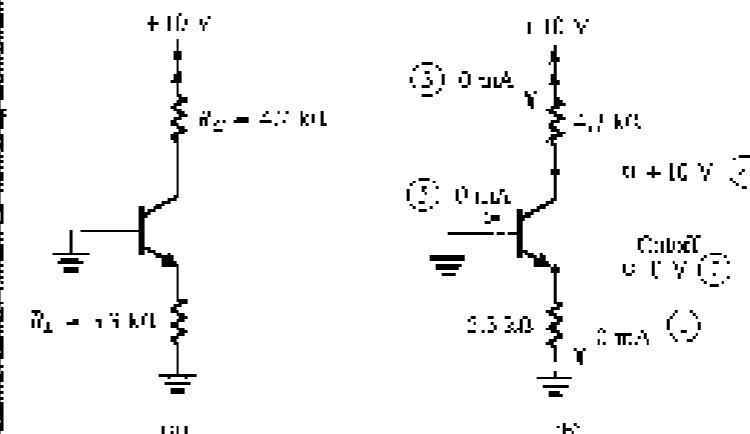


FIGURE 5.36 Example 5.6 (a) circuit; (b) analysis with the order of the analysis steps indicated by circled numbers.



Solution

Since the base is at zero volts and the collector is connected to ground through R_C , the emitter-base junction cannot conduct and the emitter current is zero. Also, the collector-base junction cannot conduct, since the n-type collector is connected through R_C to the negative power supply while the p-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the cutoff mode of operation.

The emitter voltage will obviously be zero, while the collector voltage will be equal to -10 V , since the voltage drop across R_C is zero. Figure 5.36(b) shows the analysis details.

EXERCISES

- 5.23 For the circuit in Fig. 5.36(a), what is the highest voltage of collector voltage that permits the transistor to remain in the active mode? Assume $\alpha = 0.99$.
 Ans. -4.7 V .
- 5.24 Redesign the circuit of Fig. 5.36(a), find new values for R_B and R_C , establish a collector current of 0.5 mA and a reverse bias voltage on the collector-base junction with a maximum of -0.7 V .
 Ans. $R_B = 6 \times 4.25 \times 10^3 = 26.5\text{ k}\Omega$.
- 5.25 For the circuit in Fig. 5.36(a), find the value to which the base voltage can be increased so that the transistor remains in saturation with a current of 5 mA .
 Ans. $+5.18\text{ V}$.

We desire to analyze the circuit of Fig. 5.37(a) to determine the voltages at all nodes and the currents through all branches.

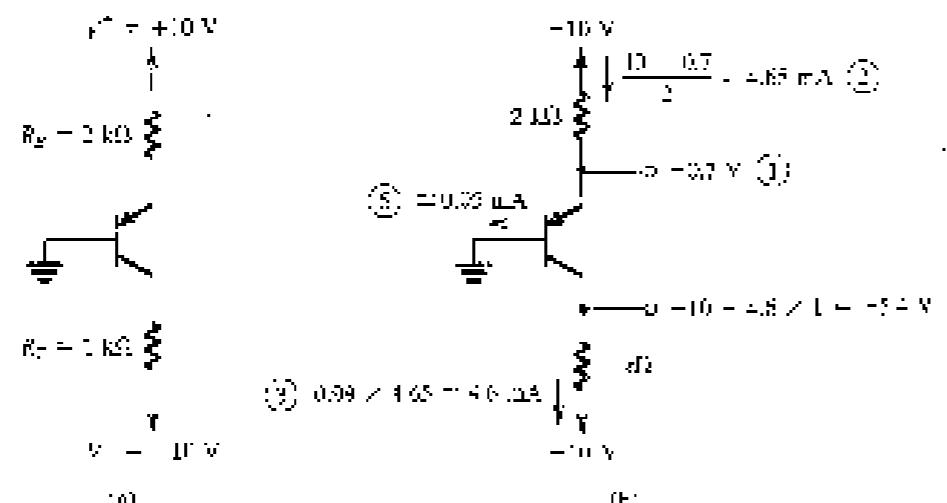


FIGURE 5.37 Example 5.27(c) circuit (b) analysis with the steps solved by circled numbers.

Solution

The base of this pnp transistor is grounded, while its emitter is connected to a positive supply ($V_B = +10\text{ V}$) through R_B . It follows that the emitter-base junction will be forward biased with

$$V_{BE} = V_{B1} = 0.7\text{ V}$$

Thus the emitter current will be given by

$$I_E = \frac{V_B - V_{BE}}{R_B} = \frac{10 - 0.7}{2} = 4.65\text{ mA}$$

Since the collector is connected to a negative supply (more negative than the base voltage) through R_C , it is possible that this transistor is operating in the active mode. Assuming this to be the case, we obtain

$$I_C = \alpha I_E$$

Since no value for β has been given, we shall assume $\beta = 100$, which results in $\alpha = 0.99$. Since large variations in β result in small differences in α , this assumption will not be critical as far as determining the value of I_C is concerned. Thus,

$$I_C = 0.99 \times 4.65 = 4.6\text{ mA}$$

The collector voltage will be

$$\begin{aligned} V_C &= V_B - I_C R_C \\ &= -10 + 4.6 \times 1 = -5.4\text{ V} \end{aligned}$$

Thus the collector-base junction is reverse biased by 0.7 V , and the transistor is indeed in the active mode, which supports our original assumption.

It remains only to calculate the base current,

$$I_B = \frac{I_E}{\beta + 1} = \frac{4.65}{101} = 0.05\text{ mA}$$

Obviously, the value of β critically affects the base current. Note, however, that in this circuit the value of β will have no effect on the mode of operation of the transistor. Since β is generally an ill-specified parameter, this circuit represents a good design. As a rule, one should strive to design the circuit such that its performance is insensitive to the value of β if possible. The analysis details are illustrated in Fig. 5.37(b).

EXERCISES

- 5.25 For the circuit in Fig. 5.36(a), find the largest voltage of collector voltage that permits the transistor to remain in the active mode.
 Ans. $-2.16\text{ k}\Omega$.
- 5.26 Redesign the circuit of Fig. 5.36(a). Find new values for R_B and R_C to establish a collector current of 1 mA and a reverse bias on the collector-base junction of -5 V . Assume $\alpha = 1$.
 Ans. $R_B = 9.3\text{ k}\Omega$, $R_C = 2.4\text{k}\Omega$.

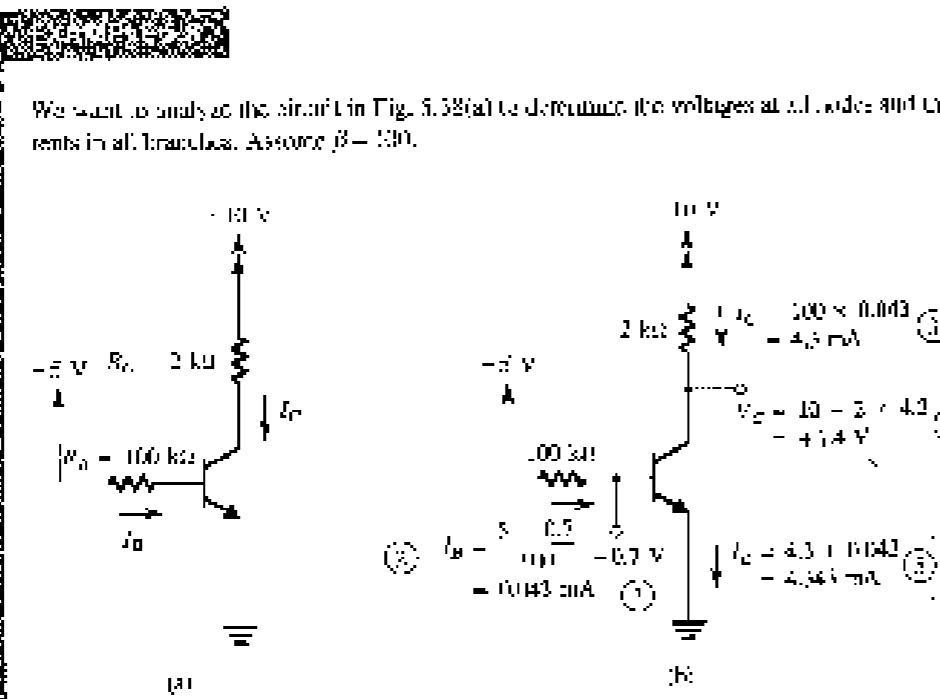


FIGURE 5.38 Example 5.3 (a) initial; (b) analysis with steps indicated by circled numbers.

Solution

The base-emitter junction is clearly forward-biased. Thus,

$$I_B = \frac{(5 - V_{BE})}{R_B} = \frac{5 - 0.2}{100} = 0.048 \text{ mA}$$

Assume that the transistor is operating in the active mode. We may then write

$$I_C = \beta I_B = 100 \times 0.048 = 4.8 \text{ mA}$$

The collector voltage can now be determined as

$$V_C = +10 - I_C R_L = 10 - 4.8 \times 2 = +1.2 \text{ V}$$

Since the base voltage V_B is

$$V_B = V_{BE} = +0.2 \text{ V}$$

it follows that the collector-base junction is reverse-biased by 0.2 V and the transistor is indeed in the active mode. The emitter current will be given by

$$I_E = (\beta + 1) I_B = 101 \times 0.048 \approx 4.8 \text{ mA}$$

We note from this example that the collector and emitter currents depend critically on the value of β . In fact, if β were 10% higher, the transistor would leave the active mode and enter saturation. Therefore this clearly is a bad design. The analysis details are illustrated in Fig. 5.38(b).

EXERCISE

- 05.27 The circuit of Fig. 5.38(a) is to be fabricated using a transistor type whose β is specified to be in the range of 100 to 150. If the resulting values of I_B and I_C are multiplied by 1.05, what will be the minimum current in the collector? Assume that the collector-emitter voltage is 0.2 V. Hint: Assume that the collector-emitter voltage is guaranteed to be in the active mode. What is the range of collector voltage if the fabricated circuit is to exhibit?

05.28 If $R_B = 1.5 \text{ k}\Omega$, $I_B = 0.2 \text{ V}$, and $V_C = 10 \text{ V}$, what is the minimum value of β required to ensure that the transistor remains in the active mode?

- We want to analyze the circuit of Fig. 5.39 to determine the voltages at all nodes and the currents through all branches. The minimum value of β is specified to be 30.

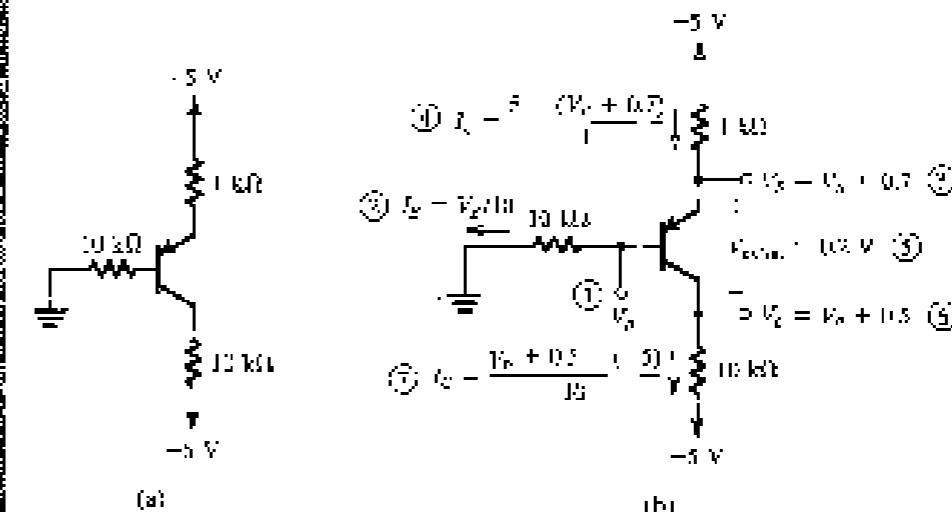


FIGURE 5.39 Example 5.3 (a) initial; (b) analysis with steps numbered.

Solution

A quick glance at this circuit reveals that the transistor will be either active or saturated. Assuming active-mode operation and neglecting the base current, we see that the base voltage will be approximately zero volts, the emitter voltage will be approximately -0.2 V, and the emitter current will be approximately 4.8 mA. Since the maximum current that the collector can support while the transistor remains in the active mode is approximately 2.5 mA, it follows that the transistor is definitely saturated.

Assuming that the transistor is saturated and denoting the voltage at the base by V_B (refer to Fig. 5.39(b)), it follows that

$$V_T - V_B - V_{CE} = V_B + 0.2$$

$$V_B = V_T - V_{CE} = V_T - 0.2 - 0.5 = V_T - 0.5$$

$$I_C = \frac{-\beta}{1 + \beta} V_B = \frac{5 - V_B}{1 + \beta} = 4.0 - V_B \text{ mA}$$

$$I_C = \frac{V_B}{R_E} = 0.1 V_B \text{ mA}$$

$$I_A = \frac{V_C - (-\beta)}{10} = \frac{V_B - 0.5 - \beta}{10} = 0.1 V_B - 0.05 \text{ mA}$$

Using the relationship $I_A = I_B + I_C$, we obtain

$$4.0 - V_B = 0.1 V_B - 0.05 + 0.25$$

which results in

$$V_B = \frac{3.75}{2} = 1.875 \text{ V}$$

Substituting in the equations above, we obtain

$$V_C = 3.875 \text{ V}$$

$$V_{BE} = 0.63 \text{ V}$$

$$I_B = 1.17 \text{ mA}$$

$$I_C = 0.86 \text{ mA}$$

$$I_A = 0.81 \text{ mA}$$

It is clear that the transistor is saturated, since the value of β is

$$\beta_{\text{actual}} = \frac{0.86}{0.11} = 2.8$$

which is much smaller than the specified minimum β .

Solution

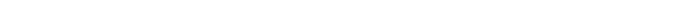
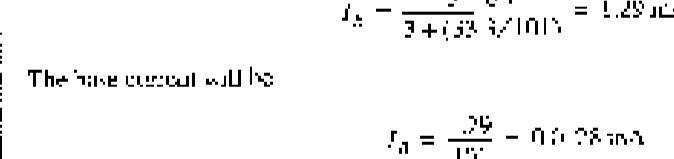
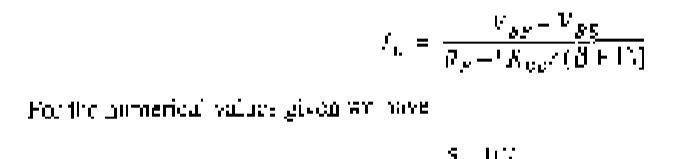
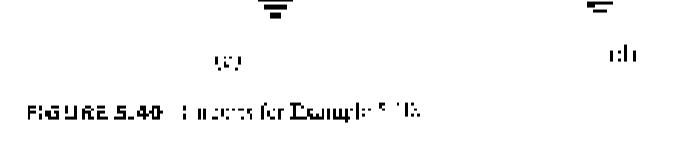
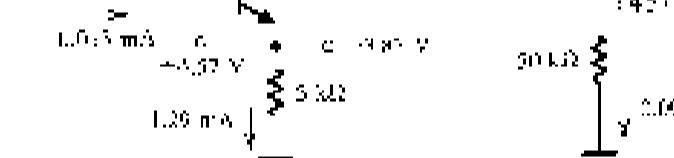
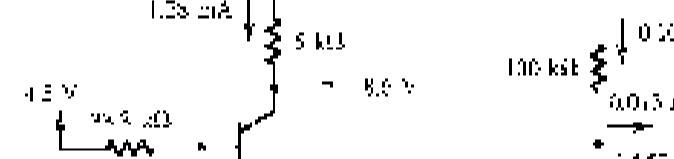
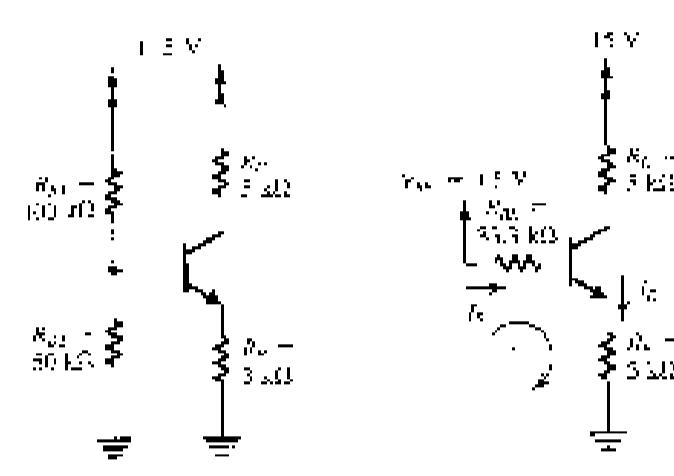
The first step in the analysis consists of simplifying the base circuit using Ohm's law. The result is shown in Fig. 5.40(b), where

$$V_{B0} = +15 \frac{R_{E1}}{R_{E1} + R_{E2}} = 15 \frac{50}{50 + 50} = -5 \text{ V}$$

$$R_{B0} = (R_{B1} \parallel R_{B2}) = (100 \parallel 50) = 33.33 \Omega$$

To evaluate the bias or the emitter current, we have to write a loop equation around the loop marked L in Fig. 5.40(b). Note, though, that the current through R_{E2} is different than the current through R_E . The loop current, then, will be

$$V_{BL} = I_B R_{E1} + V_{BE1} + I_T R_E$$



The base voltage is given by

$$\begin{aligned} V_B &= V_{BE} + I_C R_E \\ &= 0.7 + 1.29 \times 5 = 4.57 \text{ V} \end{aligned}$$

Assume active-mode operation. We can evaluate the collector current as

$$I_C = \alpha I_B = 0.99 + 1.29 = 1.28 \text{ mA}$$

The collector voltage can now be evaluated as

$$V_C = -15 - I_C R_C = -15 - 1.28 \times 5 = -3.6 \text{ V}$$

It follows that the collector is higher in potential than the base by 4.02 V, which means that the transistor is in the active mode, as had been assumed. The results of the analysis are given in Figs. 5.40(c) and (d).

EXERCISE

5.40B If the transistor in the circuit of Fig. 5.40(a) is replaced with another having half the value of β , i.e., $\beta = 20$, find the new value of I_C , and express the change in Δ as a percentage.

$$\Delta I_C = 1.15\% \quad (\text{Ans.})$$

We wish to analyze the circuit in Fig. 5.41(a) to determine the voltages at all nodes and the currents through all branches.

Solution

We first recognize that part of this circuit is identical to the circuit we analyzed in Example 5.10—namely, the circuit of Fig. 5.40(a). The difference, of course, is that in the new circuit we have an additional transistor Q_2 together with its associated resistors R_{E2} and R_{C2} . Assume that Q_2 is still in the active mode. The following values will be identical to those obtained in the previous example:

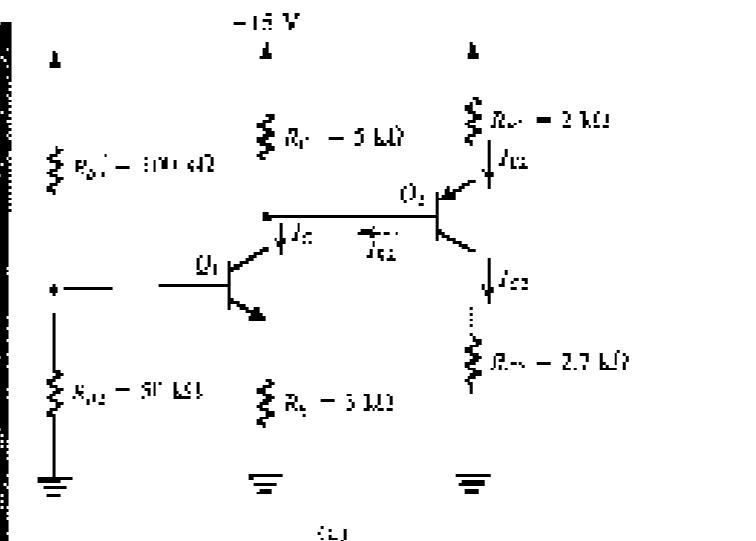
$$V_B = 4.57 \text{ V} \quad I_{C1} = 1.29 \text{ mA}$$

$$I_{B1} = 0.0128 \text{ mA} \quad I_{E1} = 1.28 \text{ mA}$$

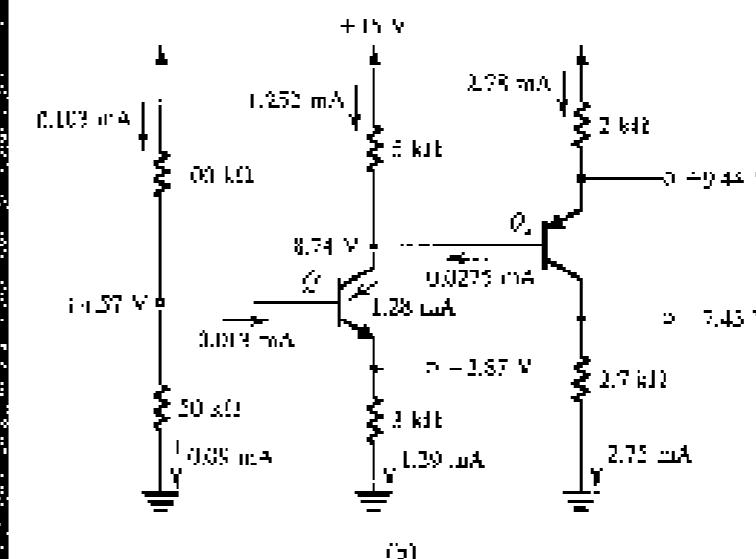
However, the collector voltage will be different than previously calculated since part of the collector current I_{C1} will flow in the base lead of Q_2 (I_{B2}). As a first approximation we may assume that I_{B2} is much smaller than I_{C1} ; that is, we may assume that the current through R_{C1} is almost equal to I_{C1} . This will enable us to calculate V_{C1} :

$$\begin{aligned} V_{C1} &= -15 - I_{C1} R_C \\ &= -15 - 1.28 \times 5 = -18.6 \text{ V} \end{aligned}$$

Thus Q_1 is in the active mode, as had been assumed.



(a)



(b)

FIGURE 5.41 Circuits for Example 5.41

As far as Q_2 is concerned, we note that its emitter is connected to +15 V through R_{E2} . It is therefore safe to assume that the emitter-base junction of Q_2 will be forward biased. Thus the emitter of Q_2 will bear a voltage V_{E2} given by

$$V_{E2} = V_{CE2} + V_{BE2} = 0.6 - 0.7 = -0.1 \text{ V}$$

The emitter current of Q_2 may now be calculated as

$$I_{E2} = \frac{-0.1}{R_{E2}} = \frac{15 - 9.3}{2} = 7.85 \text{ mA}$$

Since the collector of Q_1 is returned to ground via R_{C1} , it is possible that Q_1 is operating in the active mode. Assume this to be the case. We now find I_{C1} as

$$\begin{aligned} I_{C1} &= \alpha_1 I_{B1} \\ &= 0.99 \times 2.85 = 2.82 \text{ mA} \quad (\text{assuming } \beta_1 = 100) \end{aligned}$$

The collector voltage of Q_1 will be

$$V_{C1} = I_{C1} R_{C1} = 2.82 \times 2.7 = 7.62 \text{ V}$$

which is lower than V_B by 0.98 V. Thus Q_1 is in the active mode, as assumed.

It is important at this stage to find the magnitude of the error incurred in our calculations by the assumption that I_E is negligible. The value of I_E is given by

$$I_E = \frac{I_{B1}}{\beta_1 + 1} = \frac{2.85}{101} = 0.028 \text{ mA}$$

which is indeed much smaller than $I_A = 1.28 \text{ mA}$. If desired, we can obtain more accurate results by iterating one more time, assuming I_E to be 0.028 mA. The new values will be

$$\text{Current in } R_{C1}: I_{C1} = 1.28 - 0.028 = 1.252 \text{ mA}$$

$$V_{C1} = 15 - 1.252 = 8.74 \text{ V}$$

$$V_{B2} = 8.74 + 0.7 = 9.44 \text{ V}$$

$$I_{B2} = \frac{9.44 - 9.04}{2} = 0.70 \text{ mA}$$

$$I_{C2} = 0.99 \times 0.70 = 0.69 \text{ mA}$$

$$V_{C2} = 2.73 \times 2.7 = 7.43 \text{ V}$$

$$I_{E2} = \frac{0.70}{101} = 0.0069 \text{ mA}$$

Note that the new value of I_E is very close to the value used in our iteration, and no further iterations are warranted. The final results are indicated in Fig. 5.11(b).

The reader justifiably might be wondering about the necessity for using an iterative scheme in solving a linear circuit theory problem. Indeed, we can obtain the exact solution if we can still continue as we are doing, with a first-order model exact to by writing appropriate equations. The reader is encouraged to find this setting and then compare the results with those obtained above. It is important, however, to note that in most such problems it is quite sufficient to obtain an approximate solution, provided that we can obtain it quickly and, of course, correctly.

In the above examples, we frequently used a precise value of α to calculate the collector current. Since $\alpha \approx 1$, the error in such calculations will be very small if one assumes $\alpha = 1$ and $\beta = \beta_0$. Therefore, except in calculations that depend critically on the value of α (e.g., the calculation of base current), one usually assumes $\alpha = 1$.

EXERCISES

5.4.10 The circuit in Fig. 5.11(a) finds the load current for a given power input. Find the power input required to give a 10 mA load current.

5.4.11 (Op-amp) An op-amp has a 10 mA output current. If the output voltage is 10 V, what is the power dissipated by the op-amp? (Assume $\beta = 100$.)

5.4.12 The circuit in Fig. 5.11(b) is to be connected to the circuit in Fig. 5.4.1(a) as indicated; specifically, the collector of Q_1 is to be connected to the collector of Q_2 . The β 's are 100. Find the open-circuit V_{CE} and the values of V_B and I_E .



FIGURE 5.30

For the circuit in Fig. 5.30, assume $\beta = 100$ and $V_{BE} = 0.7 \text{ V}$. Find the open-circuit V_{CE} and the values of V_B and I_E .

PROBLEMS

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 5.4.2(a). Assume $\beta = 100$.

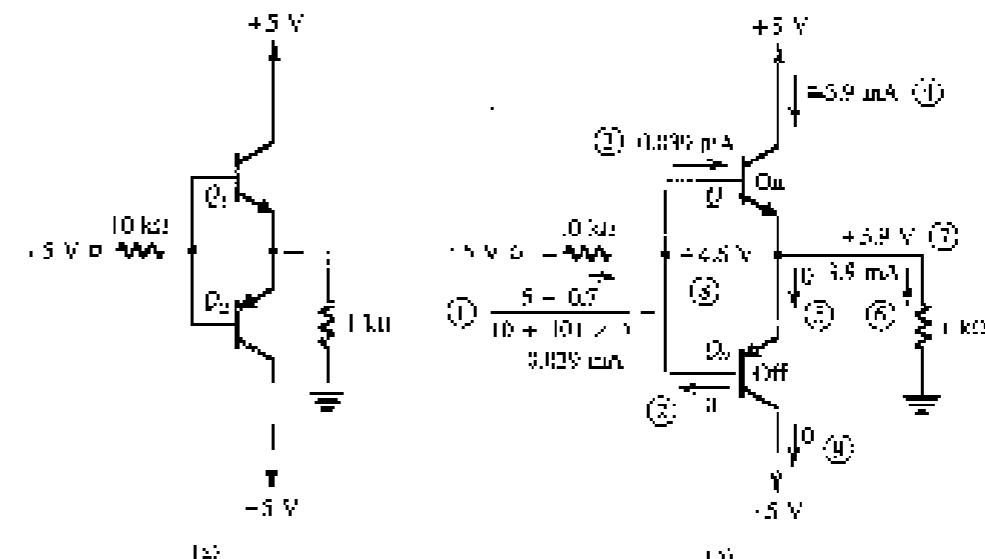


FIGURE 5.42 Example 5.12: (a) circuit; (b) analysis with steps numbered.

Solution

By examining the circuit we conclude that the two transistors Q_1 and Q_2 cannot be simultaneously conducting. Thus if Q_1 is on, Q_2 will be off, and vice versa. Assume that Q_1 is on. It

follows that current will flow from ground through the 1 k Ω load resistor into the emitter of Q_2 . Thus the base of Q_2 will be at a negative voltage, and base current will be flowing out of the base through the 10-k Ω resistor and into the +5 V supply. This is impossible, since if the base is negative, current in the 10-k Ω resistor will have to flow into the base. Thus we conclude that our original assumption—that Q_2 is on—is incorrect. It follows that Q_2 will be off and Q_1 will be on.

The question now is whether Q_1 is active or saturated. The answer in this case is obvious. Since the base of Q_1 will be +5 V supply and since zero current flows into the base of Q_1 , it follows that the base of Q_1 will be at a voltage lower than +5 V. Thus the collector-base junction of Q_1 is reverse biased and Q_1 is in the active mode. It remains only to determine the currents and voltages using techniques already described in detail. The results are given in Fig. 5.43(2).

EXERCISE

Solve the problem in Example 5.12 with the voltage feeding the bases being +2.4 V. Assume that $V_{BE} = 0.7$ V and $\beta = 100$.

5.5 BIASING IN BJT AMPLIFIER CIRCUITS

The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable, and insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type. Another important consideration in bias design is locating the dc bias point in the V_{CE} - I_C plane to allow for maximum output signal swing (see the discussion in Section 5.1.7). In this section, we shall deal with various approaches to solving the bias problem in transistors designed with discrete devices. Bias methods for integrated-circuit design are presented in Chapter 6.

Before presenting the "good" biasing schemes, we should point out why two obvious arrangements are not good. First, attempting to bias the BJT by fixing the voltage V_{BE} (e.g., in instance, using a voltage divider across the power supply V_{CC} as shown in Fig. 5.43(3)) is not a viable approach. The very sharp exponential relationship between the small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE} . Second, biasing the BJT by establishing a constant current at the base, as shown in Fig. 5.43(4), where $I_B \approx V_{BE}/(0.7\beta R_B)$, is also not a recommended approach. Here the typically large variations in the value of β among units of the same device type will result in correspondingly large variations in I_C and hence in V_{CE} .

5.5.1 The Classical Discrete-Circuit Bias Arrangement

Figure 5.44(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2 . In addition, a resistor R_3 is connected to the emitter.

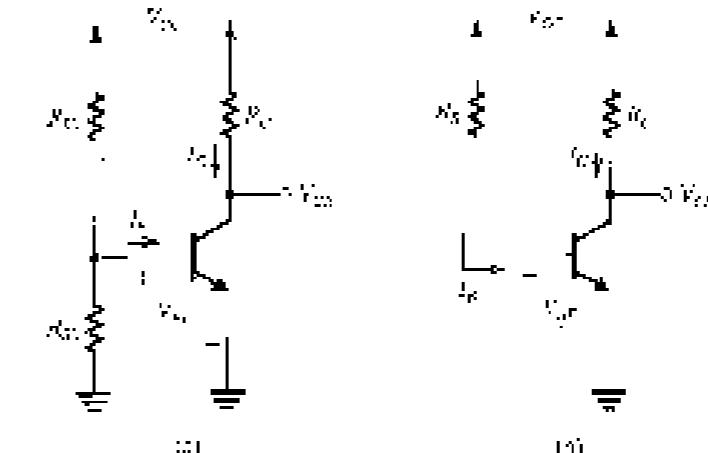


FIGURE 5.43 Two new bias schemes: (a) biasing the BJT by fixing V_{BE} by fixing I_B . (b) reverse biasing the collector-base junction. (a) V_{BE} is considered to be "good." Neider scheme is implemented.

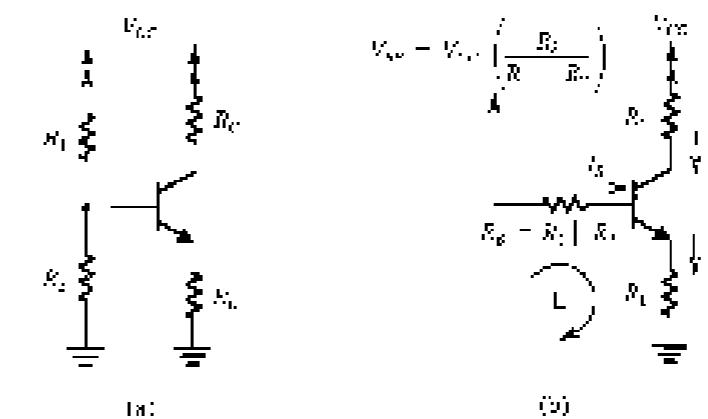


FIGURE 5.44 Classical biasing for BJTs using a single power supply: (a) circuit with the voltage divider supplying the base bypassed with its Thevenin equivalent.

Figure 5.44(b) shows the same circuit with the voltage-divider network replaced by its Thevenin equivalent.

$$V_{BE} = \frac{R_1}{R_1 + R_2} V_{CC} \quad (5.68)$$

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \quad (5.69)$$

The current I_B can be determined by writing a Kirchhoff loop equation for the base-emitter-ground loop, labeled L, and substituting $I_B = I_s / (\beta - 1)$:

$$I_B = \frac{V_{BE} - V_{BE}}{R_T + R_B / (\beta - 1)} \quad (5.70)$$

To make I_C insensitive to temperature and β variation,³ we design the circuit to satisfy the following two constraints:

$$V_{BE} \gg V_{CE} \quad (5.71)$$

$$R_E \ll \frac{R_L}{\beta + 1} \quad (5.72)$$

Condition (5.71) ensures that small variations in V_{BE} (~ 0.7 V) will be swamped by the much larger V_{CE} . There is a limit, however, on how large V_{CE} can be. For a given value of the supply voltage V_{CC} , the higher the value we use for V_{CE} , the lower will be the sum of voltages across R_E and the collector-base junction (V_{CEQ}). On the other hand, we want the voltage across R_E to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want V_{CE} (or V_{CEQ}) to be large to provide a large signal swing (before transistor saturation). Thus, as is the case in any design, we have a set of conflicting requirements, and the solution must be a compromise. As a result of this, one designs for V_{BE} about $\frac{1}{2}V_{CC}$, V_{CE} (or V_{CEQ}) about $\frac{1}{2}V_{CC}$, and R_E about $\frac{1}{2}V_{CC}$.

Condition (5.72) makes I_C insensitive to variations in β and could be satisfied by selecting R_E small. This in turn is achieved by using low values for R_1 and R_2 . Lower values for R_1 and R_2 , however, will draw a higher current from the power supply, and will result in a lowering of the input resistance of the amplifier if the input signal is coupled to the base, which is the trade-off involved in this part of the design. It should be noted that Condition (5.72) means that we want to make the base voltage independent of the value of β and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects R_1 and R_2 such that their current is in the range of I_B to $0.1I_B$.

Further insight regarding the mechanism by which the bias arrangement of Fig. 5.44(a) stabilizes the dc emitter (I_E and hence collector) current is obtained by considering the feedback action provided by R_E . Consider that for some reason the emitter current increases. The voltage drop across R_E , and hence V_E will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider R_1, R_2 , which is the case if R_E is small, I_E will remain constant and the increase in V_E will result in a corresponding decrease in V_{CE} . This in turn reduces the collector (I_C and I_E) current, a change opposite to that originally assumed. Thus R_E provides a negative feedback action that stabilizes the bias current. We shall study negative feedback formally in Chapter 8.

We wish to design the bias network of the amplifier in Fig. 5.44 to establish a current $I_B = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_E and another one-third to the voltage drop across R_L , leaving one-third

³ Bias design seeks to stabilize emitter current I_E ; since $I_E = \alpha I_B$, and α varies very little. That is, a small I_B will result in a small I_E , and vice versa.

for possible signal swing at the collector. Thus,

$$V_A = -V \quad (5.73)$$

$$V_F = 4 - V_{BE} \approx 13\text{ V}$$

and R_E is determined from

$$R_E = \frac{V_F}{I_C} = \frac{13}{1} = 13\text{ k}\Omega$$

From the discussion above we select a voltage-divider current of $0.1I_B = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, I_C (AC)

$$R_1 = R_2 = \frac{12}{0.1} = 120\text{ k}\Omega$$

and

$$\frac{R_1}{R_1 + R_2} V_{CC} = 4\text{ V}$$

Thus $R_1 = 80\text{ k}\Omega$ and $R_2 = 80\text{ k}\Omega$.

At this point it is desirable to find a more accurate estimate for I_E , taking into account the nonzero base current. Using Eq. (5.73),

$$I_E = \frac{V_F - 0.7}{13\text{ k}\Omega + 130\text{ k}\Omega} = 0.69\text{ mA}$$

This is quite a bit less than the value we were aiming for (1 mA). It's easy to see from the above equation that a simple way to zero in on the nominal value would be to reduce R_E from $13\text{ k}\Omega$ by the magnitude of the second column (i.e., $130\text{ k}\Omega$). Thus a more suitable value for R_E in this case would be $R_E = 3\text{ k}\Omega$, which results in $I_E = 1.01\text{ mA} \approx 1\text{ mA}$.

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to $I_B/0.1$, i.e., 1 mA, resulting in $R_1 = 8\text{ k}\Omega$ and $R_2 = 8\text{ k}\Omega$. We shall refer to the circuit using these latter values as design 2, for which the scaled value of I_E using the initial value of R_E of $13\text{ k}\Omega$ will be

$$I_E = \frac{4 - 0.7}{8 + 130} = 0.69 \approx 1\text{ mA}$$

In this case, design 2, we need not change the value of R_E .

Finally, the value of R_L can be determined from

$$R_L = \frac{12 - V_A}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99\text{ mA} \approx 1\text{ mA}$ results, for both designs, in

$$R_L = \frac{12 - 3}{1} = 9\text{ k}\Omega$$

EXERCISE

For design 1 with $\alpha = 0.05$, the coverage of the nominal 95% C.I. is 0.94, while the coverage of the nominal 90% C.I. is 0.99. For design 2 with $\alpha = 0.05$, the coverage of the nominal 95% C.I. is 0.995, while the coverage of the nominal 90% C.I. is 0.99.

5.5.2 A Two-Power-Supply Version of the Classical Bias Arrangement

A somewhat simpler Max arrangement is possible if two master supplies are available, as shown in Fig. 5-25. Writing a loop equation for the loop labeled 7, gives

$$I_{\text{in}} = \frac{V_{\text{SS}} - V_{\text{in}}}{R_s + R_{\text{in}}/(S+1)} \quad (3.73)$$

This equation is identical to Eq. (5.70) except for V_{ex} replacing V_{an} . Thus the zero-current steady-state of Eqs. (5.71) and (5.72) apply here as well. Note that if the reservoir is to be used with the base grounded (i.e., in the common-base configuration), then R_b can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then R_b is needed. We shall study the various DFT amplifier configurations in Section 5.3.

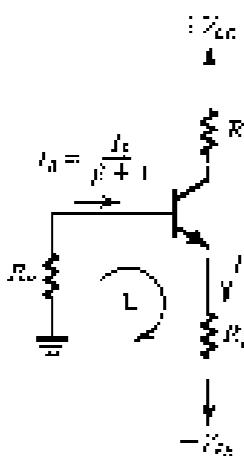


FIGURE 5.45 Biasing the DUT using two power supplies. Resistor R_3 is necessary only if the signal v_i to be applied is very coupled to the bias. Otherwise, the bias capacitor C_3 can be left out, and by using ground as a virtual common signal source, resulting in a much higher independence of the bias current.

EXERCISE

DS-44 The four arrangements of Fig. 3-45 each need 30 ohms of load impedance. Design the circuit to eliminate a de-magnetizing current of 1.0 ampere per pole. Use the voltage gain of 10000 with the following component values: $R_1 = 10\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = 10\text{ k}\Omega$, $R_4 = 10\text{ k}\Omega$, $C_1 = 1\text{ }\mu\text{F}$.

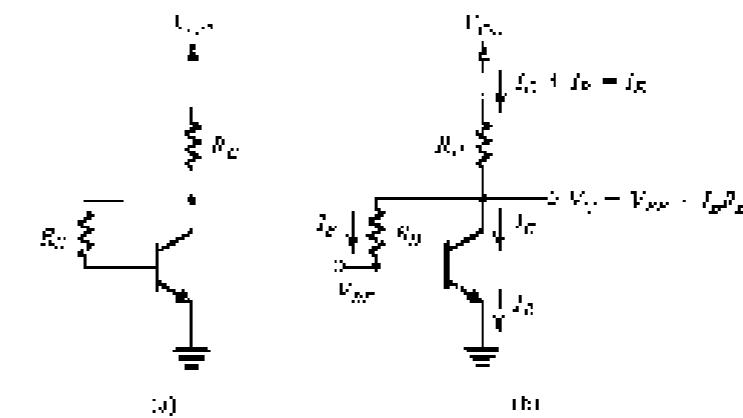


FIGURE 5.40 (a) A common-emitter frequency-selective feedback oscillator with a feedback resistor R_f . (b) Analytical expression for ω_0 .

5.5.3 Biasing Using a Collector-to-Base Feedback Resistor

Figure 5.20(a) shows a simple but effective absorptive biasing arrangement suitable for common-emitter amplifiers. The circuit explores a resistor R_3 connected between the collector and the bias. Resistor R_3 provides negative feedback, which helps to stabilize the bias point of the BJT. We shall study feedback formally in Chapter 8.

An analysis of the chart is shown in Fig. 5.16(b), from which we can write

$$V_{AC} = I_x R_C + I_x R_o - V_{oe}$$

$$= I_o R_C - \frac{I_x}{\delta - 1} R_C - V_{oe}.$$

Using the conductance current is given by

$$I_2 = \frac{V_{\text{cr}} - V_{\text{eff}}}{E_{\text{cr}} + E_{\text{eff}}/(1+\gamma)} \quad (3.71)$$

It is interesting to note that this equation is identical to Eq. (5.20), which governs the operation of the traditional bias circuit, except that V_{BE} replaces V_{CE} and R_C replaces R_B . It follows that to obtain a value of I_D that is insensitive to variation of β , we select $R_W/(\beta - 1) \approx R_C$. Note, however, that the value of R_W determines the allowable signal swing at the collector stage.

$$V_{CE} = I_B R_E + I_C \frac{R_S}{\beta + 1} \quad (3.73)$$

EXERCÍCIOS

DS-24 Then in the year 1971, Fig. 5-16, I obtained a detailed photograph of the same crater at the same time as the one shown in Fig. 5-15. The crater has a diameter of 2.17 km and a depth of 1.15 km. The floor of the crater is at the same level as the surrounding terrain. The crater rim is very steep and has a height of 1.15 km above the floor. The crater floor is relatively flat and has a depth of 1.15 km below the rim. The crater rim is composed of a thick layer of material, possibly a mixture of rock and soil, which has been eroded by water and wind over time. The crater floor is composed of a thin layer of material, possibly a mixture of rock and soil, which has been deposited by water and wind over time. The crater rim is composed of a thick layer of material, possibly a mixture of rock and soil, which has been eroded by water and wind over time. The crater floor is composed of a thin layer of material, possibly a mixture of rock and soil, which has been deposited by water and wind over time.

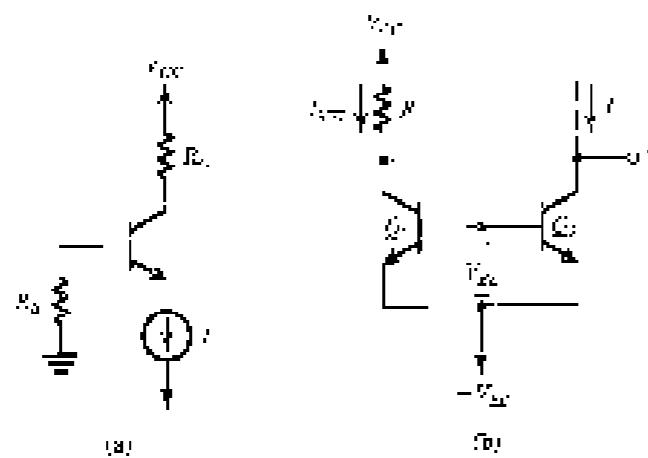


FIGURE 5.47 (a) A BJT biased using a constant-current source I . (b) Circuit for implementing the current source I .

5.5.4 Biasing Using a Constant-Current Source

The BJT can be biased using a constant-current source I as indicated in the circuit of Fig. 5.47(a). This circuit has the advantage that the collector current is independent of the values of β and R_B . Thus R_B can be made large, resulting in a increase in the input resistance of the base without adversely affecting bias stability. Further, current-source biasing leads to significant design simplifications, as will become obvious in later sections and chapters.

A simple implementation of the constant-current source I is shown in Fig. 5.47(b). The circuit utilizes a pair of matched transistors Q_1 and Q_2 , with Q_1 connected as a diode by shorting its collector to its base. If we assume that Q_1 and Q_2 have high β values, we can neglect their base currents. Thus the current through Q_2 will be approximately equal to I_{BQ1} :

$$I_{BQ1} = \frac{V_{BE1} - V_{T}}{R} \quad (5.76)$$

Now, since Q_1 and Q_2 have the same V_{BE} , their collector currents will be equal, resulting in

$$I = I_{CQ1} = \frac{V_{CC} - V_{BE} - V_{T}}{R} \quad (5.77)$$

Neglecting the Early effect in Q_1 , the collector current will remain constant at the value given by this equation as long as Q_2 remains in the active region. This can be guaranteed by keeping the voltage in the collector of Q_1 greater than that at the base ($V_{CE1} > V_{B1}$). The connection of Q_1 and Q_2 in Fig. 5.47(b) is known as a current mirror. We will study current mirrors in detail in Chapter 6.

EXERCISE

- Given $V_{CC} = 12\text{V}$, $V_T = 0.025\text{V}$, $\beta = 100$, $R_B = 10\text{k}\Omega$, $R_C = 1\text{k}\Omega$, $R_E = 100\text{k}\Omega$, $I = 1\text{mA}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ1} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ2} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ3} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ4} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ5} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ6} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ7} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ8} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ9} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ10} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ11} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ12} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, $R_{C2} = 1\text{k}\Omega$, $R_{E2} = 100\text{k}\Omega$, $I_{BQ13} = 10\mu\text{A}$, $V_{BE1} = 0.7\text{V}$, $V_{BE2} = 0.6\text{V}$, $V_{T2} = 0.025\text{V}$, $\beta_2 = 100$, $R_{B2} = 10\text{k}\Omega$, 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Use of Eq. (5.78) yields

$$i_C = I_C e^{\frac{V_{BE}}{V_T} + \frac{V_T}{2}} \quad (5.82)$$

Now, if $V_{BE} \ll V_T$ we may approximate Eq. (5.82) as

$$i_C \approx I_C \left(1 + \frac{V_{BE}}{V_T} \right) \quad (5.83)$$

Here we have expanded the exponential in Eq. (5.82) in a series and retained only the first two terms. This approximation, which is valid only for V_{BE} less than approximately 10 mV, is referred to as the **small-signal approximation**. Under this approximation the total collector current is given by Eq. (5.83) and can be rewritten

$$i_C = I_C + \frac{I_C}{V_T} v_{BE} \quad (5.84)$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_s

$$i_s = \frac{I_C}{V_T} v_{BE} \quad (5.85)$$

This equation relates the signal current in the collector to the corresponding base-emitter signal voltage. It can be rewritten as

$$i_s = g_m v_{BE} \quad (5.86)$$

where g_m is called the **transconductance**, and from Eq. (5.85), i_s is given by

$$g_m = \frac{i_s}{v_{BE}} \quad (5.87)$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C . Thus to obtain a constant predictable value for g_m , we need a constant predictable I_C . Finally, we note that BJTs have relatively high transconductance (as compared to MOSFETs, which we studied in Chapter 4); for instance, at $I_C = 1$ mA, $g_m = 40$ mA/V.

A graphical interpretation for g_m is given in Fig. 5.49, where it is shown that g_m is equal to the slope of the $i_C - v_{BE}$ characteristic curve at $i_C = I_C$ (i.e., at the bias point Q_0). Thus,

$$g_m = \frac{di_C}{dv_{BE}} \Big|_{v_{BE}=0} \quad (5.88)$$

The small-signal approximation implies keeping the signal amplitude small so that the operation is restricted to an **admittance-regime** of the $i_C - v_{BE}$ exponential curve. Increasing the signal amplitude will result in the collector current having components linearly related to v_{BE} . This, of course, is the same approximation that we discussed in the context of the amplifier transfer curve in Section 5.3.

The analysis above suggests that for small signals ($v_{BE} \ll V_T$), the transistor behaves as a voltage-controlled current source. The input port of this controlled source is between base and emitter, and the output port is between collector and emitter.¹ The transconductance of the controlled source is g_m , and the output resistance is infinite. The latter ideal property is a result of our first-order model of transistor operation in which the collector voltage has no effect on the collector current in the active mode. As we have seen in Section 5.2, practical

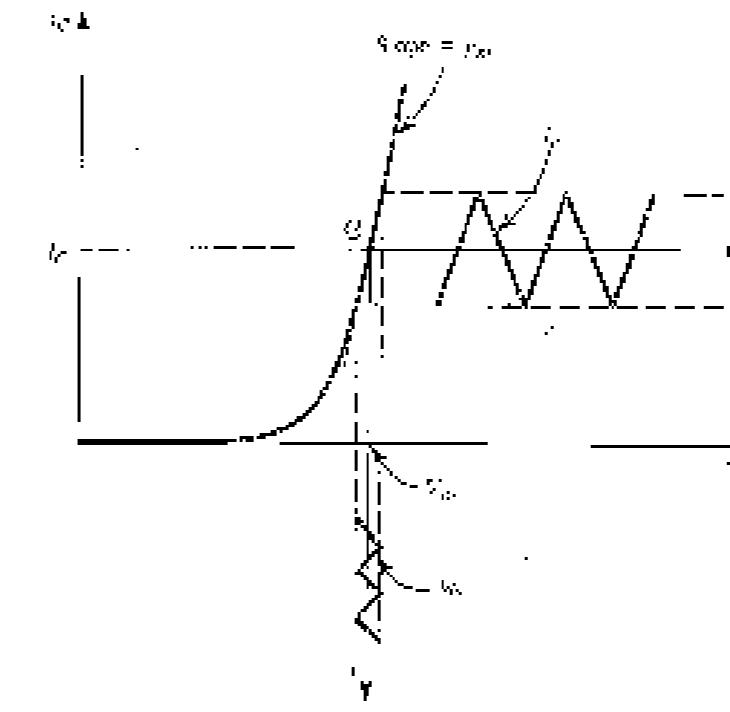


FIGURE 5.49 Small-signal operation of the transistor under the small-signal condition. A small-signal voltage v_{BE} with a triangular waveform is superimposed on the dc bias voltage v_{BE0} . In practice, the collector signal current i_C also exhibits a waveform, superimposed on the dc current I_C . Here, $i_s = g_m v_{BE}$, where v_{BE} is the change in v_{BE} about the bias point Q_0 .

Bjts have finite output resistance because of the Purly effect. The effect of the output resistance on amplifier performance will be considered later.

EXERCISE

- 1.36 If Eq. (5.86) is true, determine the input conductance g_{in} for the BJT in Fig. 5.49. Assume $I_C = 1$ mA, $V_T = 26$ mV, and $v_{BE} = 10$ mV.

5.6.2 The Base Current and the Input Resistance at the Base

To determine the resistance seen by v_{BE} , we first evaluate the total base current i_B using Eq. (5.84), as follows:

$$i_B = \frac{i_s}{\beta} = \frac{i_s}{\beta} + \frac{I_C}{\beta V_T} v_{BE} \quad (5.89)$$

Thus,

$$i_B = i_s + i_b \quad (5.89)$$

where i_s is equal to I_C/β and the signal component i_s is given by

$$i_s = \frac{1}{\beta V_T} I_C v_{BE} \quad (5.90)$$

Substituting for I_C/V_T by g_m gives

$$i_e = \frac{g_m V_{BE}}{k} \quad (5.91)$$

The small-signal input resistance between base and emitter, looking into the base, is denoted by r_i and is defined as

$$r_i = \frac{V_{BE}}{i_e} \quad (5.92)$$

Using Eq. (5.91) gives

$$r_i = \frac{\beta}{g_m} \quad (5.93)$$

Thus r_i is directly dependent on β and is inversely proportional to the bias current I_B . Substituting for g_m in Eq. (5.93) from Eq. (5.87) and replacing I_C/β by I_B gives an alternative expression for r_i ,

$$r_i = \frac{V_T}{I_B} \quad (5.94)$$

5.6.3 The Emitter Current and the Input Resistance at the Emitter

The total emitter current i_E can be determined from

$$i_E = \frac{i_S}{\alpha} = \frac{i_C}{\alpha} + \frac{i_B}{\alpha}$$

Hence,

$$i_E = i_S + i_B \quad (5.95)$$

where i_S is equal to i_C/α and the signal current i_B is given by

$$i_B = \frac{i_S}{\alpha} - \frac{I_B}{\alpha} V_T = \frac{I_B}{V_T} g_m \quad (5.96)$$

If we denote the small-signal resistance between base and emitter, looking into the emitter, by r_o , it can be denoted as

$$r_o = \frac{V_T}{i_B} \quad (5.97)$$

Using Eq. (5.92) we find that r_o , called the emitter resistance, is given by

$$r_o = \frac{V_T}{I_B} \quad (5.98)$$

Comparison with Eq. (5.87) reveals that

$$r_o = \frac{\alpha}{\beta g_m} = \frac{1}{g_m} \quad (5.99)$$

The relationship between r_i and r_o can be found by combining their respective definitions in Eqs. (5.92) and (5.97) as

$$r_o = i_B r_i = i_E$$

Thus

$$r_o = (i_E/i_S)r_i$$

which yields

$$r_o = (\beta + 1)r_i \quad (5.100)$$

Example 5.10

A common-emitter circuit has a collector voltage $V_C = 10$ V, a collector load $R_C = 1000 \Omega$, and a bias current $I_B = 10 \mu A$. The transistor has a transconductance $g_m = 100 \mu A/V$ and a short-circuit current gain $\beta = 100$. Calculate the output voltage V_O .

5.6.4 Voltage Gain

In the preceding section we have established only that the transistor senses the base-emitter signal i_{BE} and causes a proportional current, $-g_m i_{BE}$, to flow in the collector lead at a high (likely infinite) impedance level. In this way the transistor is acting as a voltage-controlled current source. To obtain an output voltage signal, we may force this current to flow through a resistor, as is done in Fig. 5.48(a). Then the total collector voltage V_C will be

$$\begin{aligned} V_C &= V_{CE} - i_C R_C \\ &= V_{CE} - (i_E + i_B) R_C \\ &= (V_{CE} - i_C R_C) - i_B R_C \\ &= V_C - i_B R_C \end{aligned} \quad (5.101)$$

Here the quantity V_C is the dc bias voltage at the collector, and the signal voltage is given by

$$\begin{aligned} v_o &= -i_B R_C = -g_m i_{BE} R_C \\ &= -(\beta + 1) R_C / g_m \end{aligned} \quad (5.102)$$

Thus the voltage gain of this amplifier is

$$A_v = \frac{v_o}{v_i} = -g_m R_C \quad (5.103)$$

Here again we note that because g_m is directly proportional to the collector bias current, the gain will be as large as the collector bias current is made. Substituting for g_m from Eq. (5.87) enables us to express the gain in the form

$$A_v = -\frac{i_C R_C}{V_T} \quad (5.104)$$

which is identical to the expression we derived in Section 5.5 (Eq. 5.89).

Example 5.11

A common-emitter circuit has a collector voltage $V_C = 10$ V, a collector load $R_C = 1000 \Omega$, and a bias current $I_B = 10 \mu A$. The transistor has a transconductance $g_m = 100 \mu A/V$ and a short-circuit current gain $\beta = 100$. Calculate the output voltage V_O .

5.5.5 Separating the Signal and the DC Quantities

The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 5.49(a) is composed of two components: a dc component and a signal component. For instance, $v_{ce} = V_{ce0} + v_{ce}$, $i_c = I_c + i_{cs}$, and so on. The dc components are determined from the AC circuit given in Fig. 5.48(b) and from the relationships imposed by the transistor (Eqs. 5.28 through 5.31). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 5.50. Observe that since the voltage of the ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced V_{cc} and V_{be} with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 5.50 is useful only as far as it shows the various signal currents and voltages; it is not an actual amplifier circuit since the dc bias circuit is not shown.

Figure 5.50 also shows the expressions for the current increments (β , α , and β_0) obtained when a small signal v_{ce} is applied. These relationships can be represented by a circuit. Such a circuit should have three terminals—C, B, and E—and should yield the same signal currents indicated in Fig. 5.50. The resulting circuit is then *equivalent to the transistor as far as small-signal operation is concerned*, and thus it can be considered an equivalent small-signal circuit model.

5.5.6 The Hybrid- π Model

An equivalent circuit model for the BJT is shown in Fig. 5.51(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the term resistance looking into

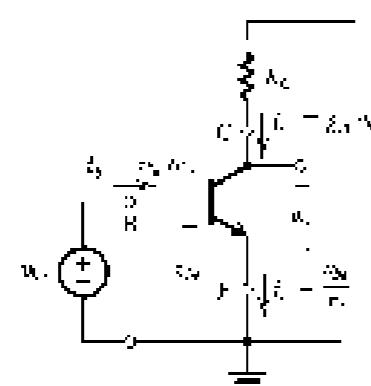


FIGURE 5.50 The amplifier circuit of Fig. 5.49(a) with the dc sources (V_{cc} and V_{be}) eliminated (short-circuited). Thus, only the signal components are present. Note that this is a representation of the signal operation of the BJT and not its total amplifier circuit.

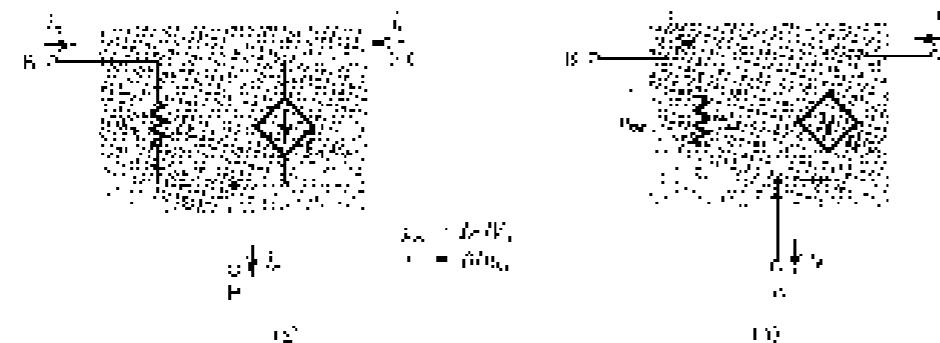


FIGURE 5.51 Two slightly different versions of the small-signal hybrid- π model for the small-signal operation of the BJT. The dependent circuit in (a) represents the BJT as a voltage-controlled current source (dependent voltage source), and that in (b) is due to the BJT as a current-controlled current source (dependent current source).

the base, r_b . The model obviously yields $i_c = \beta v_{ce}$ and $i_e = \alpha v_{ce}/r_b$. Now we observe, however, is whether the model also yields the correct expression for i_p . This can be shown as follows:

At the emitter node we have

$$\begin{aligned} i_p &= \frac{v_{ce}}{r_b} - i_e r_{ce} = \frac{v_{ce}(1 - \alpha r_{ce})}{r_b} \\ &\sim \frac{\beta_0(1 + \beta)}{r_b} = \beta_0 \sqrt{\frac{v_{ce}}{1 + \beta}} \\ &= v_{ce}/r_d \end{aligned}$$

A slightly different equivalent circuit model can be obtained by expressing the current of the controlled source ($\beta_0 v_{ce}$) in terms of the base current (i_b) as follows:

$$\begin{aligned} \beta_0 v_{ce} &= \beta_0(i_b r_{ce}) \\ &= (\beta_0 r_{ce}) i_b = \beta_0 i_b \end{aligned}$$

This results in the alternative equivalent circuit model shown in Fig. 5.51(b). Here the transistor is represented as a current-controlled dependent current source, with the source current being $\beta_0 i_b$.

The two models of Fig. 5.51 are simplified versions of what is known as the hybrid- π model. This is the most widely used model for the BJT.

It is important to note that the small-signal equivalent circuits of Fig. 5.51 model the operation of the BJT at a given bias point. This should be obvious from the fact that the model's parameters β_0 and r_d depend on the value of the dc bias current I_C , as indicated in Fig. 5.51. Finally, although the models have been developed for an n-p-n transistor, they apply equally well to a p-n-p transistor with no change of polarization.

5.5.7 The T Model

Although the hybrid- π model (one of its two variants shown in Fig. 5.51) can be used to carry out small-signal analysis of a transistor circuit, there are situations in which an alternative model, shown in Fig. 5.52, is much more convenient. This model, called the T model, is shown

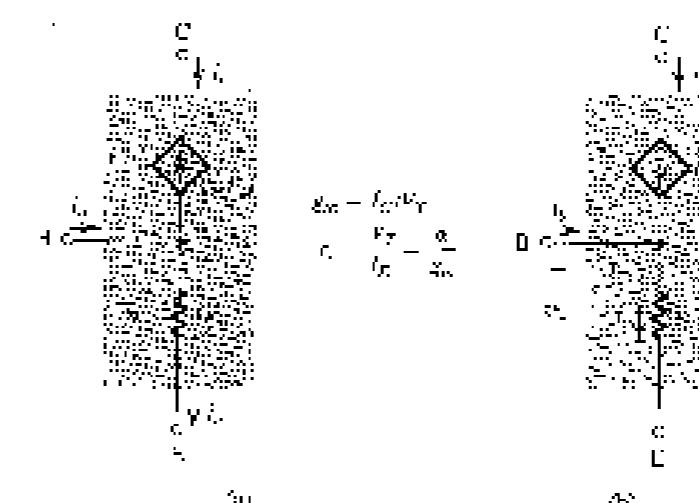


FIGURE 5.52 Two slightly different versions of the T model of the BJT. The circuit in (a) is a voltage-controlled current source representation and that in (b) is a current-controlled current source representation. These models explicitly show the finite conductance (called the collector load resistance for the C-E hybrid circuit).

In two versions in Fig. 5.52, the model of Fig. 5.52(a) represents the BJT as a voltage-controlled current source with the control voltage being v_{ce} . Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 5.52(a) we see clearly that the model yields the correct expressions for i_b and i_c . For i_b we note that at the bias node we have

$$\begin{aligned} i_b &= \frac{v_{be}}{r_e} - g_m v_{ce} = \frac{v_{be}}{r_e} (1 - g_m r_e) \\ &= \frac{v_{be}}{r_e} (1 - \alpha) = \frac{v_{be}}{r_e} \left(1 - \frac{\beta}{\beta + 1}\right) \\ &= \frac{v_{be}}{(\beta + 1)r_e} = \frac{i_c}{\beta + 1} \end{aligned}$$

as should be the case.

If in the model of Fig. 5.52(b) the current of the controlled source is expressed in terms of the emitter current as follows:

$$\begin{aligned} g_m v_{ce} &= g_m (i_c r_e) \\ &= (i_c r_e) i_c = \alpha i_c \end{aligned}$$

we obtain the alternative T model shown in Fig. 5.52(b). Here the BJT is represented as a current-controlled current source but with the control signal being i_c .

5.6.8 Application of the Small-Signal Equivalent Circuits

The availability of the small-signal BJT circuit models makes the analysis of transistor amplifiers easier a systematic process. The process consists of the following steps:

1. Determine the dc operating point of the BJT and in particular the dc collector current I_C .
2. Calculate the values of the small-signal model parameters: $g_m = I_C / V_T$, $r_e = \beta / g_m$, and $r_o = V_T / I_C = \alpha / g_m$.
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer later in this chapter.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance). The process will be illustrated by the following examples.

We wish to analyze the transistor amplifier shown in Fig. 5.53(a) to determine its voltage gain. Assume $\beta = 100$.

Solution

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $i_b = 0$. The dc base current will be

$$\begin{aligned} I_B &= \frac{V_{BE} - V_{BE0}}{R_{B0}} \\ &\approx \frac{0.7 - 0.7}{100} = 0.003 \text{ mA} \end{aligned}$$

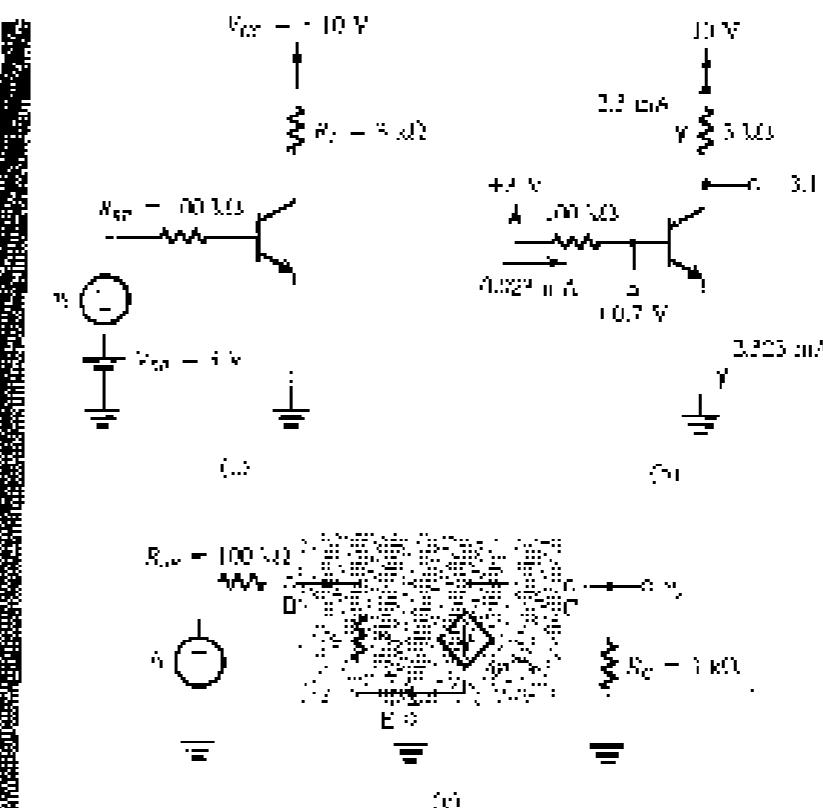


FIGURE 5.53 Example 5.4. (a) DC circuit diagram for the transistor amplifier.

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.003 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$\begin{aligned} V_C &= E_C - I_C R_C \\ &= -10 + 2.3 \times 3 = -4.1 \text{ V} \end{aligned}$$

Since $V_C \approx -0.7 \text{ V}$ (less than V_E), it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 5.53(b).

Having determined the operating point, we may now proceed to determine the small-signal model parameters:

$$\begin{aligned} r_e &= \frac{V_T}{I_C} = \frac{25 \text{ mV}}{2.3 / 0.991 \text{ mA}} = 10.8 \text{ Ω} \\ g_m &= \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V} \\ r_o &= \frac{R_C}{\beta} = \frac{3.1}{92} = 33.9 \text{ kΩ} \end{aligned}$$

To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid-pi-equivalent-circuit models of Fig. 5.51. Using the first results in the equivalent,

circuit given in Fig. 5.53(c). Noise diode V_1 quantities are included in the equivalent circuit. It is most important to note that the dc supply voltage V_{cc} has been replaced by a short circuit in the signal equivalent circuit because the circuit terminal connected to V_{cc} will always have a constant voltage; that is, the signal voltage at this terminal will be zero. In other words, a direct terminal connection is considered to have no voltage, per se, considered as a signal ground.

Analysis of the equivalent circuit in Fig. 5.53(c) proceeds as follows:

$$\begin{aligned} v_{ce} &= v_i \frac{r_\pi}{r_\pi + R_{in}} \\ &= v_i \frac{1.09}{1.09 + 100} = 0.011 v_i \end{aligned} \quad (5.105)$$

The output voltage v_o is given by

$$\begin{aligned} v_o &= -g_m v_{ce} R_C \\ &= -82 \times 0.011 v_i \times 3 = -0.234 v_i \end{aligned}$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -0.4 \text{ V/V} \quad (5.106)$$

where the minus sign indicates a phase reversal.

To gain more insight into the operation of transistor amplifiers, we will re-consider the waveforms at various points in the circuit analyzed in the previous example, in this progression: (a) input voltage waveform. First determine the maximum amplitude that v_i is allowed to have. To do this, with the magnitude of v_i set to this value, give the waveforms of $i_B(t)$, $v_{ce}(t)$, $i_C(t)$, and $v_o(t)$.

Solution

One constraint on signal amplitude is the small-signal approximation, which stipulates that v_{ce} should not exceed about 10 mV. If we take the swing of the waveform v_{ce} to be 20 mV peak-to-peak and work backward, Eq. (5.105) can be used to determine the maximum possible peak of v_i ,

$$v_i = \frac{V_{ce}}{0.011} = \frac{10}{0.011} = 9.09 \text{ V}$$

To check whether or not the transistor remains in the active mode with v_i having a peak value $V_i = 9.09 \text{ V}$, we have to evaluate the collector voltage. The voltage at the collector will consist of a constant voltage v_b superimposed on the ac voltage $v_c = 3 \text{ V}$. The peak voltage of the resulting waveform will be

$$v_c = V_c \times \text{gain} = 0.9 \times 4.02 = 3.62 \text{ V}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of $3.1 - 3.62 = 0.28 \text{ V}$, which is lower than the bias voltage by less than 0.1 V. Thus, the transistor will remain in the active mode with v_c having a peak value of 0.91 V. Nevertheless, we will use a somewhat conservative figure of 0.8 V, as shown in Fig. 5.54(a), and complete the analysis of this problem. The signal current in the base will be triangular, but, with a peak value I_B of

$$I_B = \frac{V_i}{R_{in} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.006 \text{ mA}$$

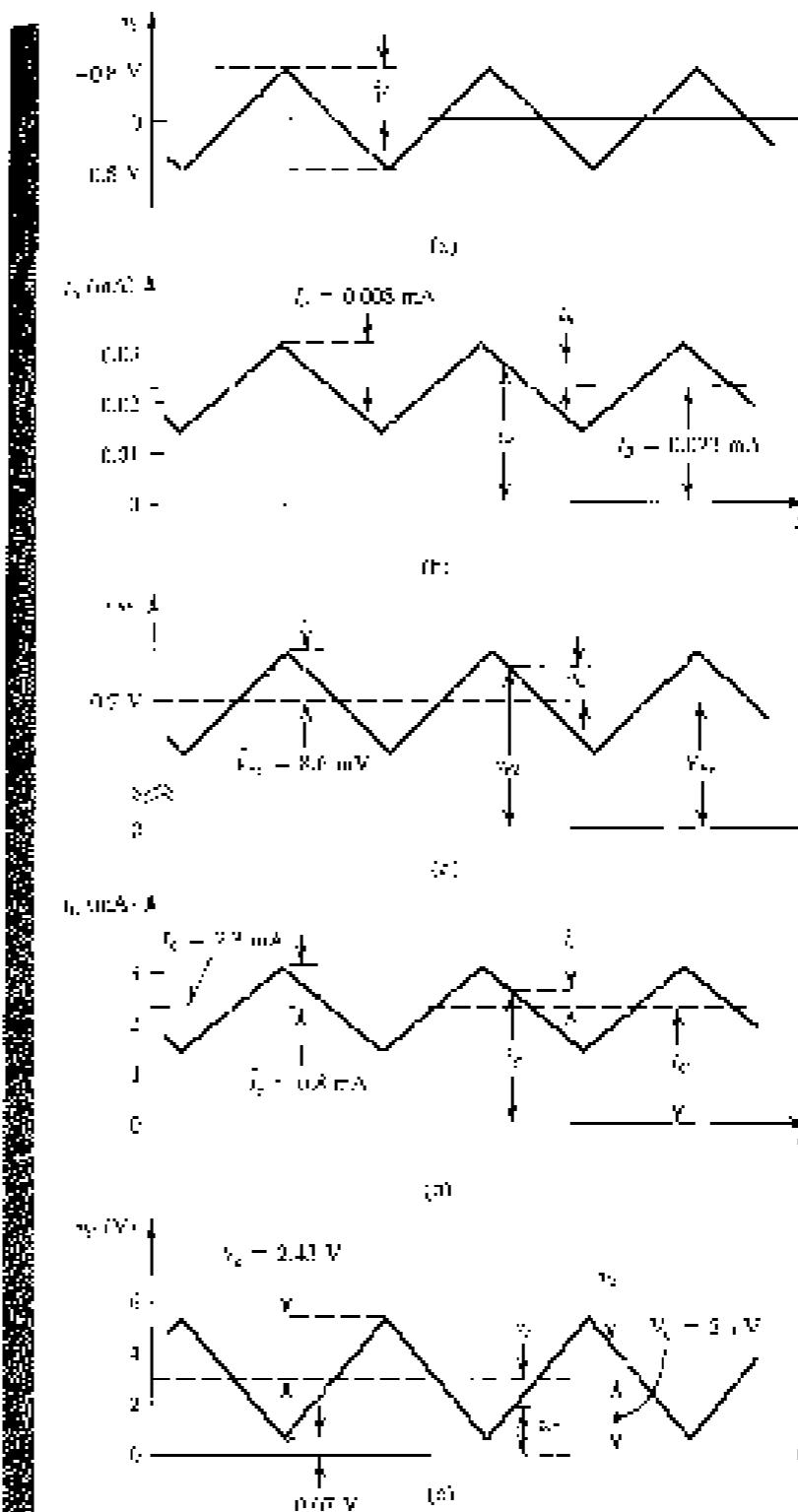


FIGURE 5.54 Signal waveforms in the circuit of Fig. 5.53.

This triangular-wave current will be superimposed on the quiescent base current I_B , as shown in Fig. 5.54(b). The base-emitter voltage will consist of a DC component superimposed on the AC V_{BE} , that is, approximately 0.7 V. The peak value of the triangular waveform will be

$$V_{B4} = \frac{V_B - V_{BE}}{R_E + R_{BE}} = 0.8 - \frac{1.72}{100 + 0.7} = 0.6 \text{ mV}$$

The total v_B is sketched in Fig. 5.54(c).

The signal current in the collector will be triangular in waveform, with a peak value I_C given by

$$I_C = \beta I_B = 100 \times 0.008 = 0.4 \text{ mA}$$

This current will be superimposed on the quiescent collector current $I_C = 0.3 \text{ mA}$, as shown in Fig. 5.54(d).

Finally, the signal voltage at the collector can be obtained by multiplying i_C by the voltage gain, A_V ,

$$V_T = 2.0 \times 0.8 = 2.4 \text{ V}$$

Figure 5.54(e) shows a sketch of the total collector voltage v_T versus time. Note the phase reversal between the input signal v_B and the output signal v_T .

We need to analyze the circuit of Fig. 5.55(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C is a coupling capacitor whose purpose is to couple the signal v_B to the emitter while blocking dc. In this way the dc bias established by V_B and V_E together with R_E and R_L will not be disturbed when the signal v_B is connected. For the purpose of this example, C will be assumed to be very large and ideally infinite—that is, acting as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor is used to couple the output signal v_T to other parts of the system.

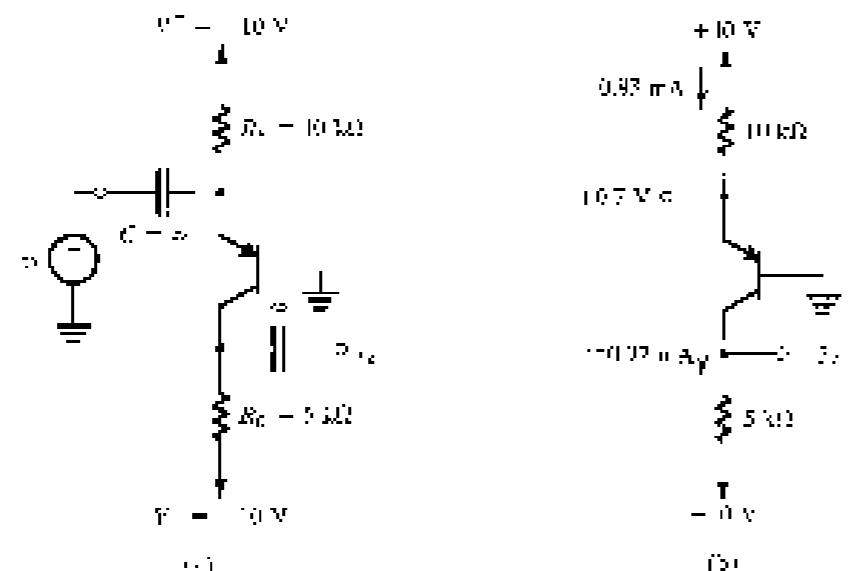


FIGURE 5.55 Examples for the small-signal analysis:

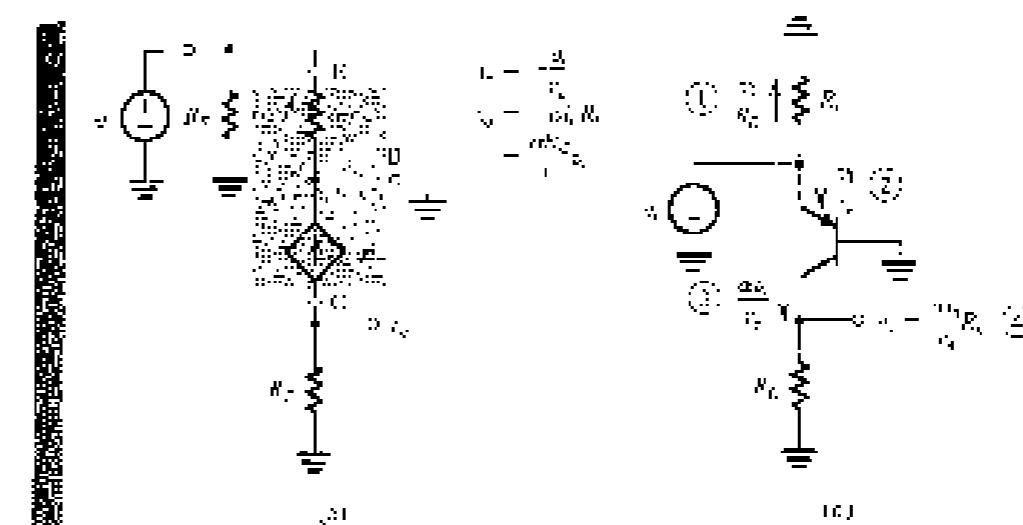


FIGURE 5.55 (Continued) (a) Small-signal model; (b) small-signal model for the circuit in (b).

Solution

We start by determining the dc operating point as follows (see Fig. 5.55(a))

$$I_B = \frac{-10 - V_E}{R_B} = \frac{-10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming $\beta = 100$, then $\alpha = 0.93$, and

$$\begin{aligned} I_C &= 0.93 I_B = 0.92 \text{ mA} \\ V_C &= 10 + I_C R_C \\ &= 10 + 0.92 \times 5 = 14.6 \text{ V} \end{aligned}$$

Thus the transistor is in the active mode. Furthermore, the collector signal can swing from -0.4 V to +0.4 V (that is, 0.4 V above the base voltage) without the transistor going into saturation. However, a negative 5.6 V swing in the collector voltage will (theoretically) cause the minimum collector voltage to be -1.0 V, which is more negative than the power-supply voltage. It follows that if we attempt to apply an input that results in such a output signal, the transistor will cutoff and the negative peaks of the output signal will be clipped, as illustrated in Fig. 5.56. The waveform in Fig. 5.56, however, is shown as a sine wave except for the clipped peaks; that is, the effect of the nonlinear $I_C = \alpha V_C$ characteristic is not taken into account. This is not correct since if we are driving the transistor into cutoff all the negative signal peaks, then we will surely be exceeding the small-signal limit, as will be shown later.

Let us now proceed to determine the small-signal voltage gain. Toward that end, we eliminate the dc sources and replace the BJT with its equivalent circuit of Fig. 5.52(b). Note that because the base is grounded, the T model is somewhat more convenient than the hybrid π model. Nevertheless, identical results can be obtained using the latter.

Figure 5.55(c) shows the resulting small-signal equivalent circuit of the amplifier. The model parameters are

$$\alpha = 0.99$$

$$r_o = \frac{V_T}{I_C} = \frac{25 \text{ mV}}{0.91 \text{ mA}} = 27.3 \Omega$$

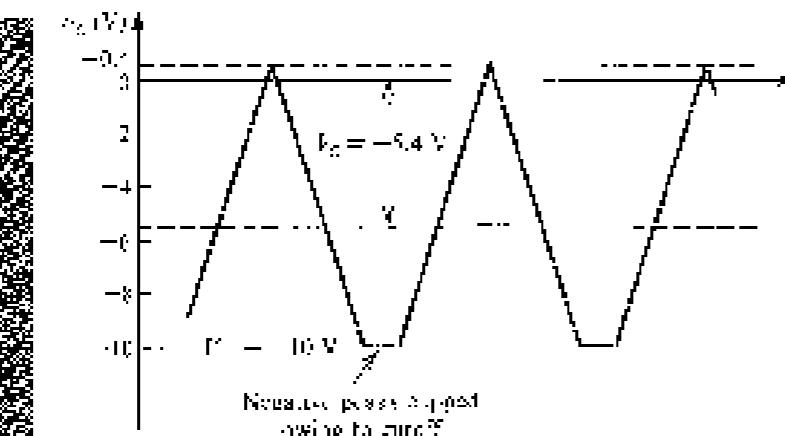


FIGURE 5.56 Distortion in a BJT signal due to transistor cutoff. Note that it is assumed that no distortion due to the transistor nonlinear characteristics is occurring.

Analysis of the circuit in Fig. 5.55(c) to determine the output voltage v_{out} and hence the voltage gain $A_v(v_i)$ is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = 183.3 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 5.1. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the pnp type.

Returning to the question of allowable signal amplitudes, we observe from Fig. 5.56(c) that $v_i = 0$. That is, if small-signal operation is desired (no limiting), then the peak of v_i should be limited to approximately 10 mV. With v_i set to this value, as shown for a sine-wave input in Fig. 5.57,

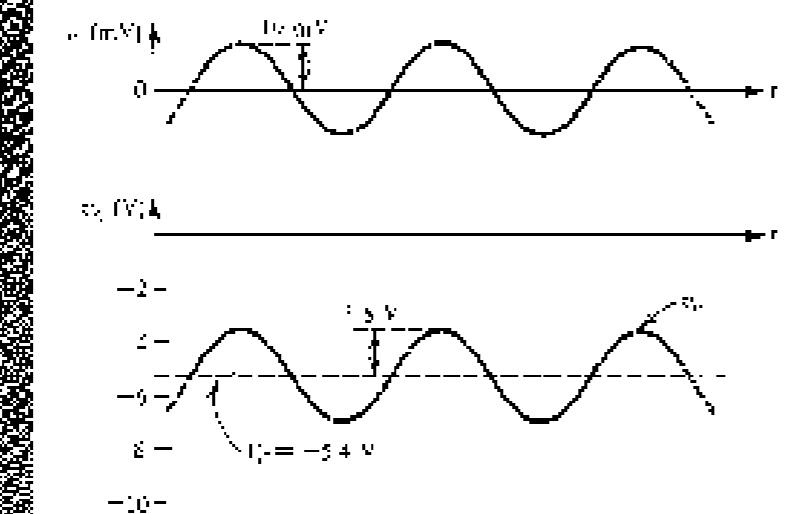
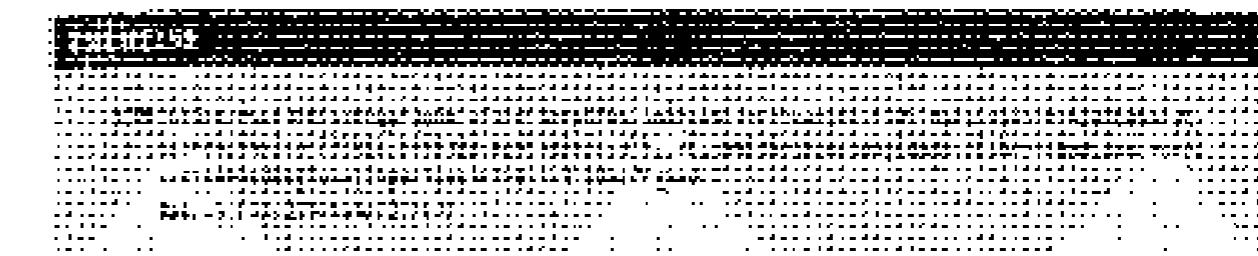


FIGURE 5.57 Input and output waveforms for the circuit of Fig. 5.55. Observe that the amplitude is maintained by a property of the common-base configuration.

the peak amplitude at the collector v_C will be

$$\hat{v}_C = 183.3 \times 0.01 = 1.833 \text{ V}$$

and the total instantaneous collector voltage $v_C(t)$ will be as depicted in Fig. 5.58.



5.6.9 Performing Small-Signal Analysis Directly on the Circuit Diagram

In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 5.59(d) illustrates this process for the circuit we have just analyzed. The reader is urged to follow this direct-analysis procedure (the steps are numbered). Observe that the equivalent circuit model is necessarily altered; we are only using the step of drawing the circuit with the BJT replaced with its model. Direct analysis, however, has an additional very important benefit: It provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly in the stage of selecting a circuit configuration appropriate for a given application.

5.6.10 Augmenting the Small-Signal Models to Account for the Early Effect

The Early effect, discussed in Section 5.2, causes the collector current to depend not only on the bias v_{BE} or v_{CE} . The dependence on v_{CE} can be modeled by assigning a finite output resistance to the controlled-current source in the hybrid- π model, as shown in Fig. 5.59. The output resistance r_o was defined in Eq. (5.37); its value is given by $r_o = (V_A + V_{CE})/I_C = V_A/I_C$, where V_A is the Early voltage and V_{CE} and I_C are the coordinates of the collector point. Note that in the models of Fig. 5.58 we have renamed r_o as r_{oC} in order to conform with the literature.

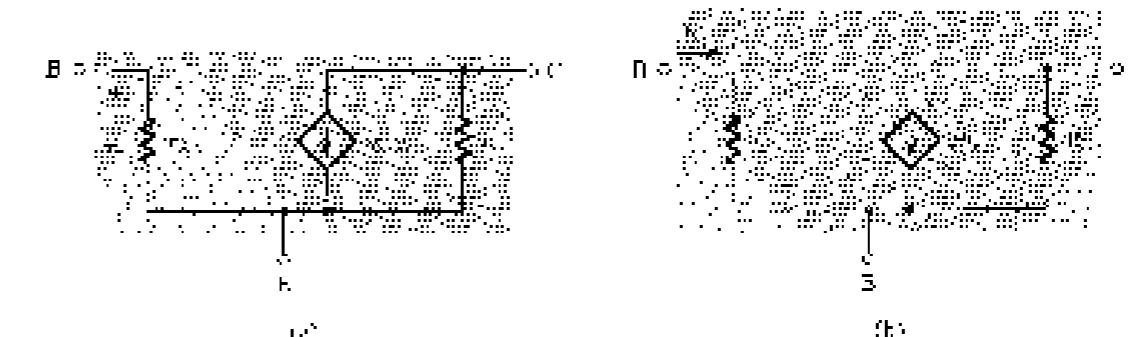


FIGURE 5.59 The hybrid- π small-signal model: (a) two versions, \pm the resistance r_o included.

The question arises as to the effect of r_o on the operation of the transistor as an amplifier. In amplifier circuits in which the emitter is grounded (as in the circuit of Fig. 5.59), r_o simply appears in parallel with R_L . Thus, if we include r_o in the equivalent circuit of Fig. 5.59(a), for example, the output voltage v_o becomes

$$v_o = -g_m i_{be} (R_L + r_o)$$

Thus the gain will be somewhat reduced. Obviously if $r_o \gg R_L$, the reduction in gain will be negligible, and one can ignore the effect of r_o . In general, in such a configuration r_o can be neglected if it is greater than $10R_L$.

When the emitter of the transistor is not grounded, including r_o in the model can complicate the analysis. We will make comments regarding r_o and its inclusion or exclusion in frequent occasions throughout the book. We should also note that in integrated circuit BJT amplifiers, r_o plays a dominant role, as will be seen in Chapter 8. Of course, if one is performing an accurate analysis or an analytical design using computer-aided analysis, then r_o can be easily included (see Section 5.11).

Finally, it should be noted that either of the models in Fig. 5.22 can be augmented to account for the Early effect by including r_o between collector and emitter.

5.6.11 Summary

The analysis and design of BJT amplifier circuits is greatly facilitated if the relationships between the various small-signal model parameters are at your fingertips. For easy reference, these are summarized in Table 5.4. Over time, however, we expect the reader to be able to recall these from memory.

EXERCISE

5.40. A common-emitter circuit is shown with its various small-signal source terms labeled. Assume $V_{CC} = 100$ V, $\beta = 100$, $\alpha = 0.99$, the transistor junction contact resistance $r_{ce} = 10\ \Omega$, and $r_o = 100\ \Omega$. The input signal is sinusoidal with peak-to-peak amplitude $2 mV$. The output voltage is measured across a load resistor $R_L = 1 k\ \Omega$. Find the output voltage amplitude and the power delivered to the load. (Hint: Use the hybrid- π model of Fig. 5.22.)

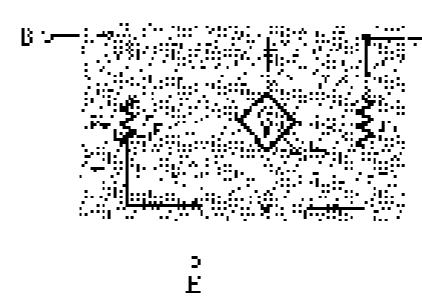


FIGURE 5.40

TABLE 5.4 Small-Signal Models of the BJT

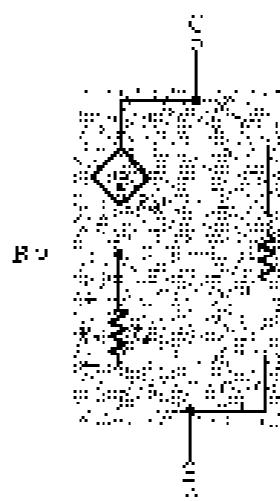
Hybrid- π Model

B (v_{be}) Version



T Model

B (g_o) Version



T Model

B (v_{ce}) Version

T Model

B (i_o) Version

T Model

B (g_o) Version

T Model

B (v_{ce}) Version

T Model

B (i_o) Version

T Model

B (g_o) Version

T Model

B (i_o) Version

T Model

B (g_o) Version

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B (i_o) Version

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B (g_o) Version

T Model

B (i_o) Version

5.7 SINGLE-STAGE BJT AMPLIFIERS

We have studied the large-signal operation of BJT amplifiers in Section 5.3 and identified the region over which a properly biased transistor can be operated as a linear amplifier for small signals. Methods for determining the BJT were studied in Section 5.5, and a detailed study of small-signal amplifier operation was presented in Section 5.6. We are now ready to consider practical transistor amplifiers, and we will do so in this section for circuits suitable for discrete-circuit fabrication. The design of integrated-circuit BJT amplifiers will be studied in Chapter 6.

There are basically three configurations for implementing single-stage BJT amplifiers: the common-emitter, the common-base, and the common-collector configuration. All three are studied below, utilizing the same basic structure with the same biasing arrangements.

5.3.1 The Basic Structure

Figure 5.59 shows the basic circuit that we shall take to implement the various configurations of BJT amplifiers. Among the various biasing schemes possible for discrete BJTs amplifiers (Section 5.5), we have selected, for simplicity and convenience, the one employing constant-current biasing. Figure 5.59 indicates the dc currents in all branches and the dc voltages at all nodes. We should note that one would want to select a large value for R_B in order to keep the input resistance at the base large. However, we also want to limit the dc voltage drop across R_E and even more importantly the variability of this dc voltage resulting from the variation in β values among transistors of the same type. The dc voltage V_B determines the allowable signal swing at the collector.

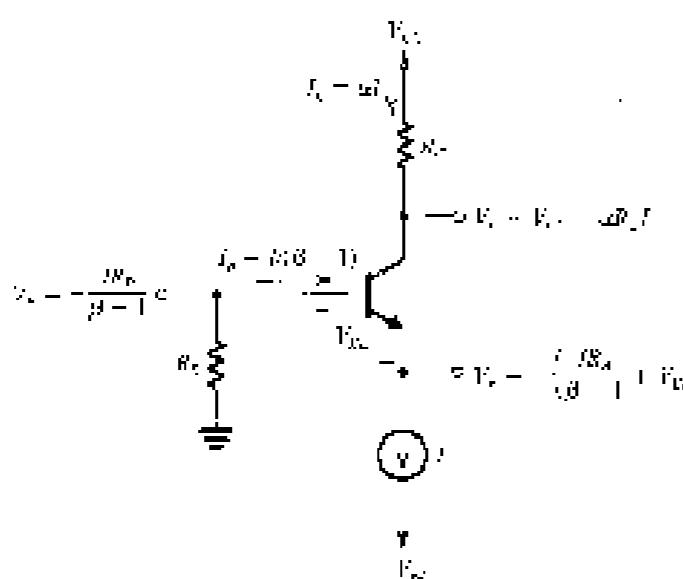
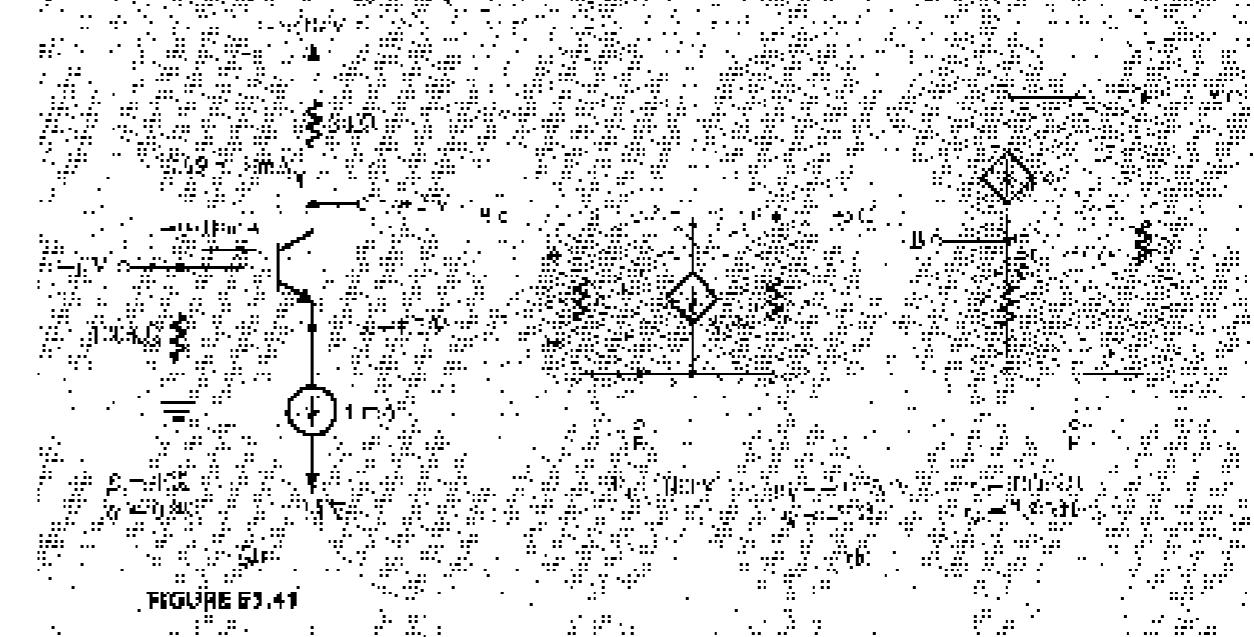


FIGURE 5.59 Results from model-based simulation of a single-pulse, discrete-dose-rate, RPT simplified optimization.

EXERCISE

541 Chapter 11: The First Derivative Test for Functions of Several Variables



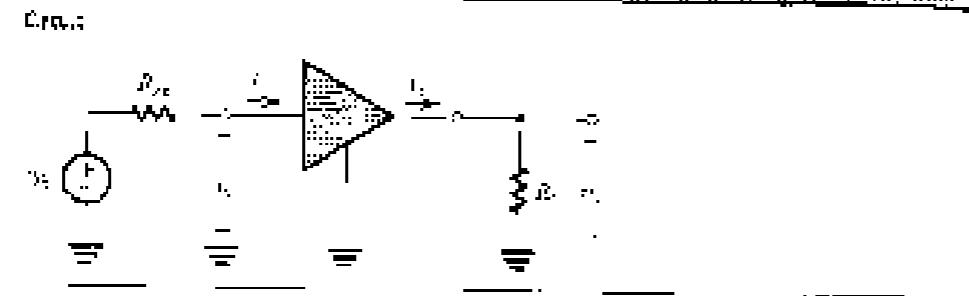
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5.3.2 Characterizing BJT Amplifiers

As we begin our study of BJT amplifier circuits, it is important to know how to characterize the performance of amplifiers as circuit building blocks. An introduction to this subject was presented in Section 1.5. However, the material of Section 1.5 was limited to unilateral amplifiers. A number of the amplifier circuits we shall study in this book are not unilateral; that is, they have internal feedback that may cause their input resistance to depend on the load resistance. Similarly, internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier. To accommodate nonunilateral amplifiers, we present in Table 3.5 a general set of parameters and equivalent circuits that we will employ in characterizing and comparing transistor amplifiers. A number of remarks are in order:

- i. The amplifier in Table 2.5 is shown fed with a signal source having an open-circuit voltage v_{os} and an internal resistance R_{os} . These can be the parameters of an actual signal source or the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study in a cascade amplifier. Similarly, R_L can be an external load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

This section is continued in Section 4.2. Readers who completed Section 4.2.2 can skip this section.

TABLE 5.5 Characteristic Parameters of Amplifiers**Definitions****(a)** Input resistance with no load:

$$R_{in} = \left| \frac{V_{in}}{I_{in}} \right|_{I_{in}=0}$$

(b) Output resistance:

$$R_{out} = \left| \frac{V_{out}}{I_{out}} \right|_{I_{out}=0}$$

(c) Open-circuit voltage gain:

$$A_{voc} = \left| \frac{V_{out}}{V_{in}} \right|_{I_{out}=0}$$

(d) Current gain:

$$A_{ic} = \left| \frac{I_{out}}{I_{in}} \right|_{I_{out}=0}$$

(e) Short-circuit current gain:

$$A_{is} = \left| \frac{I_{out}}{I_{in}} \right|_{V_{out}=0}$$

(f) Open-circuit voltage-current gain:

$$G_{ic} = \left| \frac{V_{out}}{I_{in}} \right|_{I_{out}=0}$$

(g) Terminal voltage-current gain:

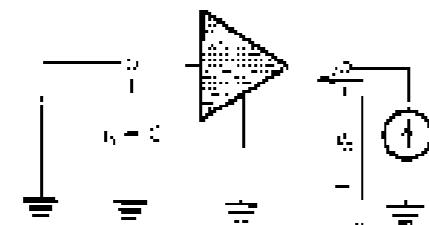
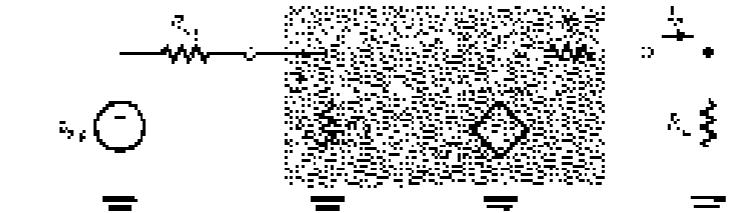
$$G_{iv} = \left| \frac{V_{out}}{I_{out}} \right|_{I_{in}=0}$$

(h) Short-circuit transconductance:

$$G_m = \left| \frac{I_{out}}{V_{in}} \right|_{I_{out}=0}$$

(i) Output resistance of amplifier model:

$$R_o = \left| \frac{V_{out}}{I_{out}} \right|_{I_{in}=0}$$

**Equivalent Circuits****(a)** A:**(b)** B:**(c)** C:**Relationships**

$$\text{(a)} \quad R_{in} = \frac{R_{in}}{R_{in} + R_{in}}$$

$$\text{(b)} \quad R_{in} = \frac{R_{in}}{R_{in} + R_{in}} A_{voc} R_{in} = R_{in}$$

$$\text{(c)} \quad A_{ic} = A_{ic} \frac{R_{in}}{R_{in}}$$

$$\text{(d)} \quad G_{ic} = G_{ic} \frac{R_{in}}{R_{in}}$$

$$\text{(e)} \quad A_{is} = G_{is} R_{in}$$

$$\text{(f)} \quad G_{is} = G_{is} \frac{R_{in}}{R_{in}}$$

2. Parameters R_{in} , A_{ic} , A_{is} , and G_{is} pertain to the amplifier proper. That is, they do not depend on the values of R_{in} and R_{in} . By contrast, R_{in} , R_{in} , A_{ic} , A_{is} , G_{ic} , and G_{is} may depend on one or both of R_{in} and R_{in} . Also, observe the relationships of related pairs of these parameters; for instance, $R_{in} = R_{in} R_{in}$, and $R_{in} = R_{in} R_{in}$.

3. As mentioned above, for noninductive amplifiers, R_{in} may depend on R_{in} , and R_{in} may depend on R_{in} . One such amplifier circuit is studied in Section 5.7.6. No such dependencies exist for unity-gain amplifiers, for which $R_{in} = R_{in}$ and $R_{in} = R_{in}$.

4. The loading of the amplifier on the signal source is determined by the input resistance R_i . The value of R_i determines the current i that the amplifier draws from the signal source. It also determines the proportion of the signal v_{in} that appears at the input of the amplifier proper, that is, v_i .
5. When evaluating the gain A_v from the open-circuit value A_{vo} , R_o is the output resistance to use. This is because A_v is based on feeding the amplifier with an ideal voltage signal v_i . This should be evident from Equivalent Circuit A in Table 5.5. On the other hand, if we are evaluating the overall voltage gain G_v from its open-circuit value G_{vo} , the output resistance to use is R_{oi} . This is because G_v is based on feeding the amplifier with v_{in} , which has an internal resistance R_{in} . This should be evident from Equivalent Circuit C in Table 5.5.
6. We urge the reader to carefully examine and reflect on the definitions and the six relationships presented in Table 5.5. Example 5.17 should help in this regard.

A transistor amplifier is fed with a signal source having an open-circuit voltage v_{in} of 10 mV and an internal resistance R_{in} of 100 kΩ. The voltage at the amplifier input and the output voltage v_o are measured both without and with a load resistance $R_L = 10 \text{ k}\Omega$ connected to the amplifier output. The measured results are as follows:

	v_i (mV)	v_o (mV)
Without R_L	9	99
With R_L connected	5	50

Find all the amplifier parameters.

Solution

First, we use the data obtained for $R_L = 0\Omega$ to determine

$$A_{vo} = \frac{99}{9} = 10 \text{ V/V}$$

and

$$G_{vo} = \frac{99}{10} = 9 \text{ V/V}$$

Now, since

$$G_{vo} = \frac{R_o}{R_o + R_{in}} A_{vo}$$

$$9 = \frac{R_o}{R_o + 100} > 10$$

which gives

$$R_o = 900 \text{ k}\Omega$$

Next, we use the data obtained when $R_L = 10 \text{ k}\Omega$ is connected to the amplifier output to determine

$$A_v = \frac{v_o}{v_i} = 8.75 \text{ V/V}$$

and

$$G_v = \frac{v_o}{v_{in}} = 7 \text{ V/V}$$

The values of A_v and A_{vo} can be used to determine R_i as follows:

$$A_v = A_{vo} \frac{R_i}{R_i + R_o}$$

$$8.75 = 10 \frac{R_i}{10 + R_i}$$

which gives

$$R_i = 1.43 \text{ k}\Omega$$

Similarly, we use the values of G_v and G_{vo} to determine R_{in} from

$$G_v = G_{vo} \frac{R_i}{R_i + R_{in}}$$

$$7 = 9 \frac{10}{10 + R_{in}}$$

resulting in

$$R_{in} = 2.86 \text{ k}\Omega$$

The value $v^2 R_i$ can be determined from

$$\frac{v_i}{v_{in}} = \frac{R_i}{R_i + R_{in}}$$

Thus,

$$\frac{9}{10} = \frac{R_i}{R_i + 100}$$

which yields

$$R_i = 100 \text{ k}\Omega$$

The short-circuit transconductance G_A can be found as follows:

$$G_A = \frac{A_{vo}}{R_o} = \frac{10}{100} = 10 \text{ mA/V}$$

and the current gain β can be determined as follows:

$$\beta = \frac{v_o/R_2}{v_i/R_1} = \frac{v_o}{v_i} \frac{R_2}{R_1}$$

$$\frac{v_o}{R_2} = 0.75 \times \frac{100}{10} = 75 \text{ mA}$$

Finally, we determine the short-circuit current gain A_{cs} as follows. From Equivalent Circuit A, the short-circuit output current is

$$i_{os} = A_{cs} v_i / R_2 \quad (5.107)$$

However, to determine A_{cs} , we need to know the value of R_s obtained with $R_2 = 0$. Toward this end, note that from Equivalent Circuit A, the open-circuit circuit current can be found as

$$i_{oc} = G_{ce} v_{ce} / R_1 \quad (5.108)$$

Now, equating the two expressions for i_{os} and substituting for G_{ce} , b_1 ,

$$G_{ce} = \frac{R_1}{R_1 + R_{ce}} = A_{cs}$$

and for v_{ce} , from

$$v_c = v_{ce} \frac{R_{ce} / R_{ce} + R_{ce}}{R_{ce} + R_{ce}}$$

results in

$$R_{ce} / R_{ce} = R_{ce} \left(1 - \frac{R_{ce}}{R_1} \left(\frac{R_{ce}}{R_{ce}} + 1 \right) \right)^{-1} \approx 81.6 \text{ k}\Omega$$

We now can use

$$i_{os} = A_{cs} / R_{ce} R_{ce} / R_1$$

to obtain

$$A_{cs} = \frac{i_{os}}{v_i} = 10 \times 81.6 / 1.23 = 672 \text{ A/A}$$

EXERCISE

- 5.42 Refer to the amplifier of Example 5.12. (a) If the input voltage is 10 mV, find the output voltage. (b) If the load resistance is increased to 10 k Ω , what will the output voltage be? (c) If the load resistance is increased to 100 k Ω , what will the output voltage be? (d) If the load resistance is increased to 1 M Ω , what will the output voltage be?

5.7.2 The Common-Emitter (CE) Amplifier

The CE configuration is the most widely used of all BJT amplifier circuits. Figure 5.60(a) shows a CE amplifier implemented using the circuit of Fig. 5.39. To establish a signal ground or ac ground, as it is sometimes called, the emitter's large capacitor C_E (usually in the μF or tens of μF range), is connected between emitter and ground. This capacitor is required to provide a very low impedance to ground (ideally, zero impedance); i.e., in effect, a short circuit at all signal frequencies of interest. In this way, the emitter signal current passes through C_E to ground and thus bypasses the output resistance of the current source I (and any other circuit component that might be connected to the emitter), hence C_E is called a bypass capacitor. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 5.8. For our purposes here we shall assume that C_E 's acting as a perfect short circuit and thus is establishing a zero signal voltage at the emitter.

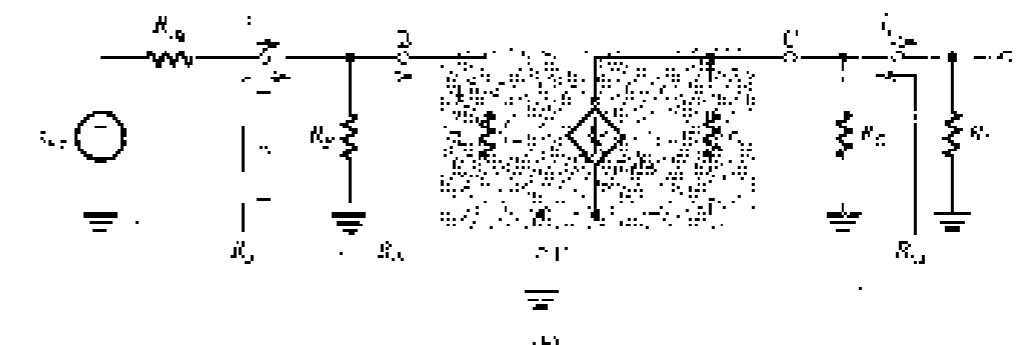
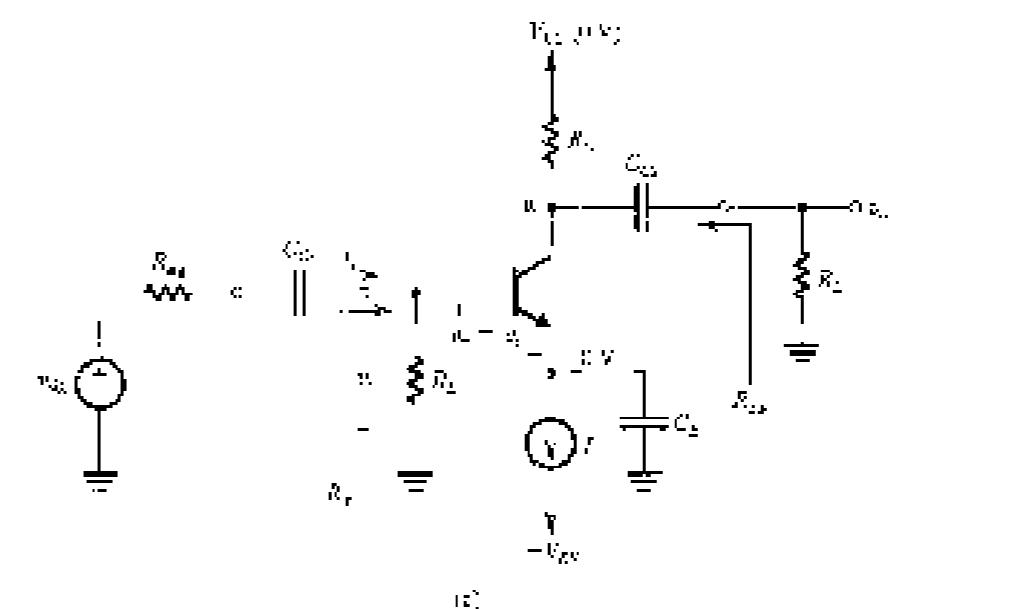


FIGURE 5.60 (a) A common-emitter stage using the structure of Fig. 5.39. (b) Equivalent circuit obtained by replacing the pair of transistors with its hybrid π model.

In order not to disturb the dc bias currents and voltages, the signal to be amplified, shown as a voltage source v_{in} with an internal resistance R_{in} , is connected to the base through a large capacitor C_{in} . Capacitor C_{in} , known as a coupling capacitor, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again we shall assume this to be the case and defer discussion of imperfect signal coupling, arising as a result of the rise of the impedance of C_{in} in low frequencies, to Section 5.9. At this juncture, we should point out that in situations where the signal source can provide a dc bias path for the dc base current I_b without significantly changing the bias point, we may connect the source directly to the base, thus bypassing with C_{in} , as well as R_{in} . Utilizing R_L has the added benefit of raising the input resistance of the amplifier.

The voltage signal resulting at the collector, v_{out} , is coupled to the load resistance R_L via another coupling capacitor C_{out} . We shall assume that C_{out} also acts as a perfect short circuit at all signal frequencies of interest; thus the output voltage $v_o = v_{out}$. Note that R_L can be an actual load resistor to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of a subsequent amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 7.)

To determine the terminal characteristics of the CE amplifier, that is, its input resistance, voltage gain, and output resistance, we replace the BJT with its hybrid π small-signal model. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 5.60(b). We observe at once that this amplifier is unilateral and thus $R_{in} = R_s$ and $R_{out} = R_L$. Analysis of this circuit is straightforward and proceeds in a step-by-step manner, from the signal source to the amplifier load. At the amplifier input we have

$$R_{in} = \frac{v_i}{i} = R_s \parallel R_e \quad (5.100)$$

where R_s is the input resistance looking into the base. Since the emitter is grounded,

$$R_{in} = r_e \quad (5.110)$$

Normally, we select $R_s \gg r_e$ with the result that

$$R_{in} \approx r_e \quad (5.111)$$

Thus, we note that the input resistance of the CE amplifier will typically be a few kilohms, which can be thought of as low to moderate. The fraction of source signal v_{in} that appears across the input terminals of the amplifier proper can be found from

$$v_i = v_{in} \frac{R_s}{R_s + R_{in}} \quad (5.112)$$

$$= v_{in} \frac{(R_s + r_e)}{(R_s + r_e) + R_{in}} \quad (5.113)$$

which for $R_s \gg r_e$ becomes

$$\alpha = v_i / v_{in} = \frac{r_e}{r_e + R_{in}} \quad (5.114)$$

Next we note that

$$v_o = v_i \quad (5.115)$$

At the output of the amplifier we have

$$v_o = -g_{oA}(r_o \parallel R_L) \quad (5.116)$$

Bounding v_o by v we can write to the voltage gain of the amplifier proper, that is, the voltage gain from base to collector,

$$A_v = -g_{oA}(r_o \parallel R_L) \quad (5.116)$$

This equation simply says that the voltage gain from base to collector is found by multiplying v_o by the total resistance between collector and ground. The open-circuit voltage gain A_{oc} can be obtained by setting $R_L \rightarrow \infty$ in Eq. (5.116); thus,

$$A_{oc} = -g_{oA}(r_o) \quad (5.117)$$

from which we note that the effect of r_o is simply to reduce the gain, usually only slightly since typically $r_o \gg R_L$, resulting in

$$A_{oc} \approx -R_o R_L \quad (5.118)$$

The output resistance R_{out} can be found from the equivalent circuit of Fig. 5.60(b) by looking back into the output terminal while short-circuiting the source v_{in} . Since this will result in $v_o = 0$, we see that

$$R_{out} = R_C \parallel r_o \quad (5.119)$$

Thus r_o reduces the output resistance of the amplifier, again usually only slightly since typically $r_o \gg R_C$ and

$$R_{out} \approx R_C \quad (5.120)$$

Recalling that for this unilateral amplifier $R_{in} = R_{out}$ we can utilize A_{oc} and R_C to obtain the voltage gain A_v corresponding to any particular R_L ,

$$A_v = A_{oc} \frac{R_L}{R_L + R_C} \quad (5.121)$$

The reader can easily verify that this approach does in fact lead to the expression for A_v in Eq. (5.116), which we have derived directly.

The overall voltage gain from source to load, G_o , can be obtained by multiplying (v_o/v_{in}) from Eq. (5.115) by A_v from Eq. (5.121).

$$G_o = \frac{(R_L \parallel r_o)}{(R_L \parallel r_o) + R_{out}} A_{oc} (r_o \parallel R_L) \quad (5.122)$$

For the case $R_L \gg r_o$, this expression simplifies to

$$G_o \approx -\frac{b(R_C \parallel R_L) r_o}{r_o + R_{out}} \quad (5.123)$$

From this expression we note that if $R_{out} \gg r_o$, the overall gain will be highly dependent on β . This is not a desirable property since β varies considerably between units of the same transistor type. At the other extreme, if $R_{out} \ll r_o$, we see that the expression for the overall

voltage gain reduces to

$$G_v \equiv -g_s (R_C \parallel R_L + r_o) \quad (5.123)$$

which is the gain A_{vB} . In other words, when R_{L1} is small, the overall voltage gain is almost equal to the gain of the CB circuit stage, which is independent of β . Typically a CB amplifier can realize a voltage gain on the order of a few hundred, which is very significant. It follows that the CE amplifier is used to realize the bulk of the voltage gain required in a usual amplifier design. Unfortunately, however, as we shall see in Section 5.9, the low-frequency response of the CE amplifier can be rather limited.

Before leaving the CE amplifier, we wish to evaluate its short-circuit current gain, A_{ic} . This can be easily done by referring to the amplifier equivalent circuit in Fig. 5.61(b). When R_L is short-circuited, the current through it will be equal to $-g_s v_o$,

$$i_o = -g_s v_o$$

Since i_o is related to $i_e v_o$,

$$i_o = v_o = g_s R_o$$

The short-circuit current gain can be found as

$$A_{ic} = \frac{i_o}{i_e} = -g_s R_o \quad (5.124)$$

Substituting $R_o = R_A \parallel r_o$, we can see that in the case $R_A \gg r_o$, A_{ic} reduces to β , which is to be expected since β is, by definition, the short-circuit current gain of the common-emitter configuration.

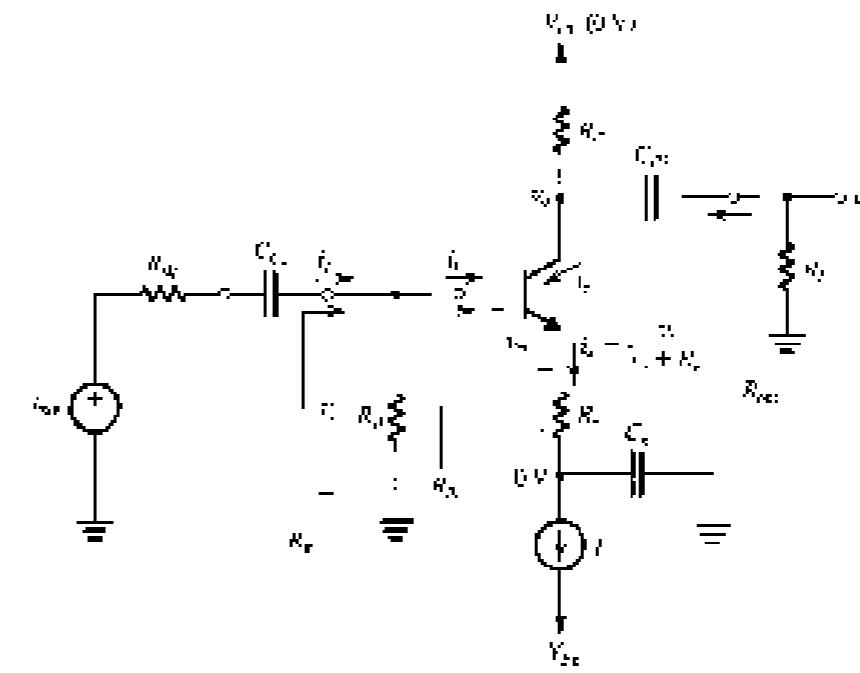
In conclusion, the common-emitter configuration can provide large voltage and current gains, but R_i is relatively low and R_{oE} is relatively high.

EXERCISE

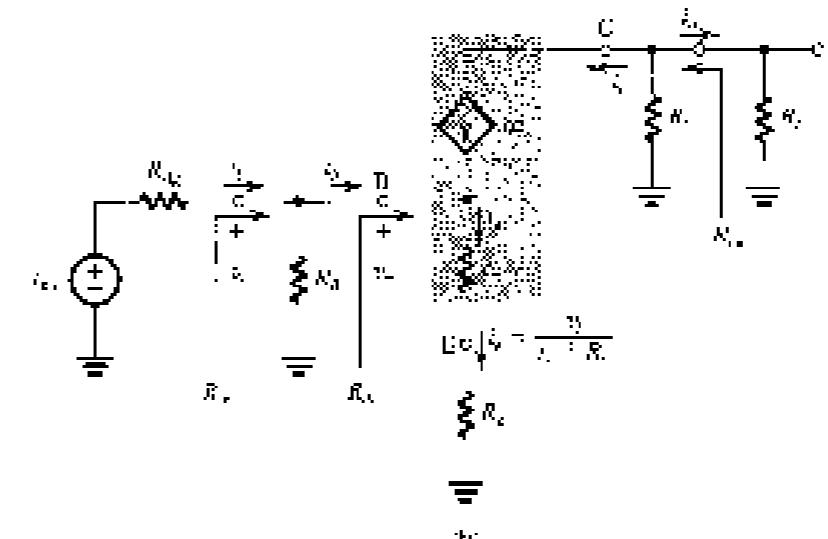
- 5.43 Consider the CE amplifier of Fig. 5.60(a), as was discussed in Exercise 5.3. In particular, let us assume the input signal is applied to the collector of the PNP transistor, so that the point V_{BE} is at 0 V. Calculate the voltage gain A_{vB} of the amplifier with $r_o = 100 \Omega$ and $R_A = 10 k\Omega$. Assume $\beta = 50$ and $r_s = 100 \Omega$. From the input voltage gain, calculate the output voltage v_o and the total harmonic distortion D_H under the following operating conditions: $V_{CC} = 20 \text{ V}$, $I_C = 1 \text{ mA}$, $R_C = 1 k\Omega$, $R_L = 1 k\Omega$, and $R_E = 100 \Omega$.

5.7.4 The Common-Emitter Amplifier with an Emitter Resistance

Including a resistance r_e in the signal path between emitter and ground, as shown in Fig. 5.61(a), can lead to significant changes in the amplifier characteristics. This extra resistor can be utilized by the designer as an effective design tool for tailoring the amplifier characteristics to fit the design requirements.



(a)



(b)

FIGURE 5.61 (a) A common-emitter amplifier with an emitter resistance r_e . (b) Equivalent circuit obtained by adding the β model.

Analysis of the circuit in Fig. 5.61(a) can be performed by replacing the BJT with one of its small-signal models. Although any one of the models of Figs. 5.51 and 5.52 can be used, the most convenient for this application is one of the two T models. This is because a resistance R_e in the emitter will appear in series with the emitter resistance r_e of the T model and one thus be added to it, simplifying the analysis considerably. In fact, whenever there is a

resistance in the emitter lead, the T model would prove more convenient to use than the π load- π model.

Replacing the HJL with the π model of Fig. 5.52(b) results in the amplifier small-signal equivalent circuit model shown in Fig. 5.61(b). Note that we have not included the BJT output resistance r_o ; including r_o complicates the analysis considerably. Since for the discrete amplifier at least it turns out that the effect of r_o on circuit performance is small, we shall not include it in the analysis here. This is not the case, however, for the IC version of this circuit, and we shall indeed take r_o into account in the analysis in Chapter 6.

To determine the amplifier input resistance R_{in} , we note from Fig. 5.61(b) that R_{in} is the parallel equivalent of R_s and the input resistance at the base R_b ,

$$R_{in} = R_s \parallel R_b. \quad (5.123)$$

The input resistance at the base R_b can be found from

$$R_b = \frac{v}{i_b}$$

where

$$i_b = (1 - \alpha)i_e = \frac{i_e}{\beta + 1}$$

and

$$i_e = \frac{v}{r_o + R_s}. \quad (5.124)$$

Thus,

$$R_b = (\beta + 1)(r_o + R_s). \quad (5.125)$$

This is a very important result. It says that the input resistance looking into the base is $(\beta + 1)$ times the load resistance in the emitter. Multiplication by the factor $(\beta + 1)$ is known as the resistance-reflection rule. The factor $(\beta + 1)$ arises because the base current is $1/(\beta + 1)$ times the emitter current. The expression for R_{in} in Eq. (5.125) shows clearly that including a resistance R_s in the emitter can substantially increase R_{in} . Indeed the value of R_{in} is increased by the ratio

$$\begin{aligned} \frac{R_{in} \text{ (with } R_s \text{ included)}}{R_{in} \text{ (without } R_s)} &= \frac{(\beta + 1)(r_o + R_s)}{(\beta + 1)r_o} \\ &= 1 + \frac{R_s}{r_o} \cdot 1 + g_m R_s. \end{aligned} \quad (5.126)$$

Thus the circuit designer can use the value of R_s to control the value of R_{in} and hence R_{out} . Of course, for this control to be effective, R_s must be much larger than R_{in} ; in other words, R_s must dominate the input resistance.

To determine the voltage gain A_{vo} we see from Fig. 5.61(b) that

$$\begin{aligned} v_o &= -g_m(R_s \parallel R_o) \\ &= -\alpha i_e (R_s \parallel R_o) \end{aligned}$$

Substituting for i_e from Eq. (5.126) gives

$$A_{vo} = \frac{v_o}{v_i} = -\frac{\alpha(R_s \parallel R_o)}{r_o + R_s} \quad (5.127)$$

Since $\alpha \ll 1$,

$$A_{vo} = -\frac{R_s \parallel R_o}{r_o + R_s}. \quad (5.128)$$

This simple relationship is very useful and is definitely worth remembering: The voltage gain from base to collector is equal to the ratio of the total resistance in the collector to the total resistance in the emitter. This statement is a general one and applies to any amplifier circuit. The open-circuit voltage gain A_{vo} can be found by setting $R_o \rightarrow \infty$ in Eq. (5.127).

$$A_{vo} \approx -\frac{\alpha R_o}{r_o + R_s}, \quad (5.129)$$

which can be expressed alternatively as

$$\begin{aligned} A_{vo} &= \frac{\alpha}{r_o} \frac{R_o}{1 + R_o/r_o}, \\ A_{vo} &= \frac{g_m R_o}{1 + (R_o/r_o)} \equiv -\frac{g_m R_o}{1 + g_m R_o}. \end{aligned} \quad (5.130)$$

Including R_s thus reduces the voltage gain by the factor $(1 + g_m R_s)$, which is the same factor by which R_s is increased. This points out an interesting trade-off between gain and input resistance. Note, though, that the designer can exercise through the choice of an appropriate value for R_s .

The output resistance R_{out} can be found from the circuit in Fig. 5.61(b) by inspection:

$$R_{out} = R_o. \quad (5.131)$$

At this point we should note that for this amplifier, $R_n = R$ and $R_{in} = R_b$.

The short-circuit current gain A_i can be found from the circuit in Fig. 5.61(b) as follows:

$$\begin{aligned} i_o &= -R_s \\ i_s &= v_o/R_o \end{aligned}$$

Thus,

$$A_i = -\frac{\alpha R_o i_s}{v_o}$$

Substituting for i_s from Eq. (5.126) and for R_{in} from Eq. (5.125),

$$A_i = -\frac{\alpha(R_s \parallel R_o)}{r_o + R_s}, \quad (5.127)$$

which for the case $R_s \gg R_{in}$ reduces to

$$A_i = -\frac{\alpha(\beta + 1)(r_o + R_s)}{r_o + R_s} = \beta$$

the same value as for the CE circuit.

The overall average gain from sources in 1ns/l can be obtained by multiplying 4.4 by 67.4%.

$$G_{ij} = \frac{R_{ij}}{R_{ik}} \cdot A_{ik} = -\frac{R_{ij}}{R_{ik} \cdot R_{jk}} \cdot \alpha(R_{ik} \parallel R_{jk})$$

Substituting η in R_{eff} by $R_{\text{eff}}(R_{\text{ex}})$, assuming that $R_{\text{ex}} \ll R_{\text{eff}}$, and substituting for R_{ex} from Eq. (5.127) results in

$$G_i = -\frac{\beta(R_i - \|R_i\|)}{R_{ii} + (\beta+1)\|r_i + R_i\|} \quad (5.145)$$

We note that the gain is lower than that of the CR amplifier because of the additional term $(\beta + 1)R_s$ in the denominator. The gain, however, is less sensitive to the value of β , as desired.

Another important consequence of including the resistance R_s in the circuit is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base, v_2 , appears between the base and the emitter. Specifically, from the circuit in Fig. 5.6 [3], we see that

$$\frac{v_i}{v_j} = \frac{\tau_j}{\tau_i - \theta_j} = \frac{1}{1 - g_i(\bar{\theta}_j)} \quad (5.1.30)$$

Thus, for the same α_2 , the signal at the input terminal of the amplifier, β_2 , can be greater than for the C_B amplifier by the factor $(1 + g_{m2}R_2)$.

To summarize, including a resistance R_1 in the emitter of the CT amplifier results in the following characteristics:

- The input resistance R_i is increased by the factor $(1 + g_m R_s)$.
 - The voltage gain from base to collector, A_{vB} , is reduced by the factor $(1 - g_m R_s)$.
 - For the same nonlinear distortion, the input signal v_i can be increased by the factor $(1 + g_m R_s)$.
 - The overall voltage gain is less dependent on the value of β .
 - The high-frequency response is significantly improved (as we shall see in Chapter 6).

With the exception of gain reduction, these characteristics represent performance improvement items. Indeed, the reduction in gain is the price paid for obtaining the other perk-to-params improvements. In many cases this is a good bargain; it is the underlying motive for the use of negative feedback. That the resistance R_2 introduces negative feedback in the amplifier circuit can be seen by reference to Fig. 5.61(a): If for some reason the collector current increases, the emitter current also will increase, resulting in an increased voltage drop across R_2 . Thus the emitter voltage rises, and the base-emitter voltage decreases. The latter effect causes the collector current to decrease, countering the initially assumed change, an indication of the presence of negative feedback. In Chapter 8, where we shall study negative feedback formally, we will find that the factor $(1 + g_m R_2)$ which appears repeatedly is the "amount of negative feedback" introduced by R_2 . Finally, we note that the negative feedback action of R_2 gives it the name emitter degeneration resistance.

Before leaving this circuit, we wish to point out that we have shown a number of the circuit analysis steps directly on the circuit diagram in Fig. 5.61(a). With practice, the reader should be able to do all of the small-signal analysis directly on the given's diagram, thus dispensing with the task of drawing a complete small-signal equivalent circuit model.

EXERCISES

- 5.4 Consider the surface $\mathbf{r}(u,v) = \langle u^2 - v^2, 2uv, u^2 + v^2 \rangle$. At the point $(1,1)$, find the following:
 (a) The tangent plane.
 (b) The normal vector.
 (c) The curvature κ and torsion τ .
 (d) The Gaussian curvature K and mean curvature H .
 (e) The first fundamental form E, F, G and second fundamental form A .
 (f) The principal curvatures k_1, k_2 and the corresponding principal directions.

5.7.5 The Common-Base (CB) Amplifier

By establishing a signal ground on the base terminal of the BJT, a circuit configuration aptly named common-base or grounded-base amplifier is obtained. The input signal is applied to the emitter, and the output is taken at the collector, with the base forming a common terminal between the input and output ports. Figure 5.67(a) shows a CBJ amplifier stage in the circuit of Fig. 5.39. Observe that since both the dc and ac voltages at the base are zero, we have connected the base directly to ground, thus eliminating resistor R_B altogether. Coupling capacitors C_{in} and C_{out} perform similar functions to those in the CB circuit.

The small-signal equivalent circuit model of the amplifier is shown in Fig. 5.62(a). Since resistor R_{L} appears in series with the emitter terminal, we have elected to use the T-model for the transistor. Although the hybrid- π model would yield identical results, the T-model is more convenient in this case. We have not included r_o . This is because including r_o would complicate the analysis considerably, for it would appear between the output nodes of the amplifier. Fortunately, it turns out that the effect of r_o on the performance of a discrete CE amplifier is very small. We will consider the effect of r_o when we study the DC biasing of CE amplifiers in Chapter 6.

From inspection of the equivalent circuit model in Fig. 8.62(b), we see that the input resistance is

$$f_{\lambda} = f_{\lambda} \quad (6.137)$$

This should have been explained since we are looking into the emitter, and the base is grounded. Typically r_e is a few ohms to a few tens of ohms; thus the FET amplifier has a low output resistance.

To determine the voltage gain, we write at the collector node

$$g_{\mu\nu} = \phi(t) \delta_{\mu\nu} + \tilde{g}_{\mu\nu}$$

and authorizes him to sign documents for me.

$$I_4 =$$

Sight

$$A_{ij} = \frac{V_2}{V_1} - \frac{g_i(R_j \parallel R_k)}{g_i(R_k \parallel R_j)} \quad (2.136)$$

which crossed zero its positive sign is identical to the expression for δ , for the CE amplitude.

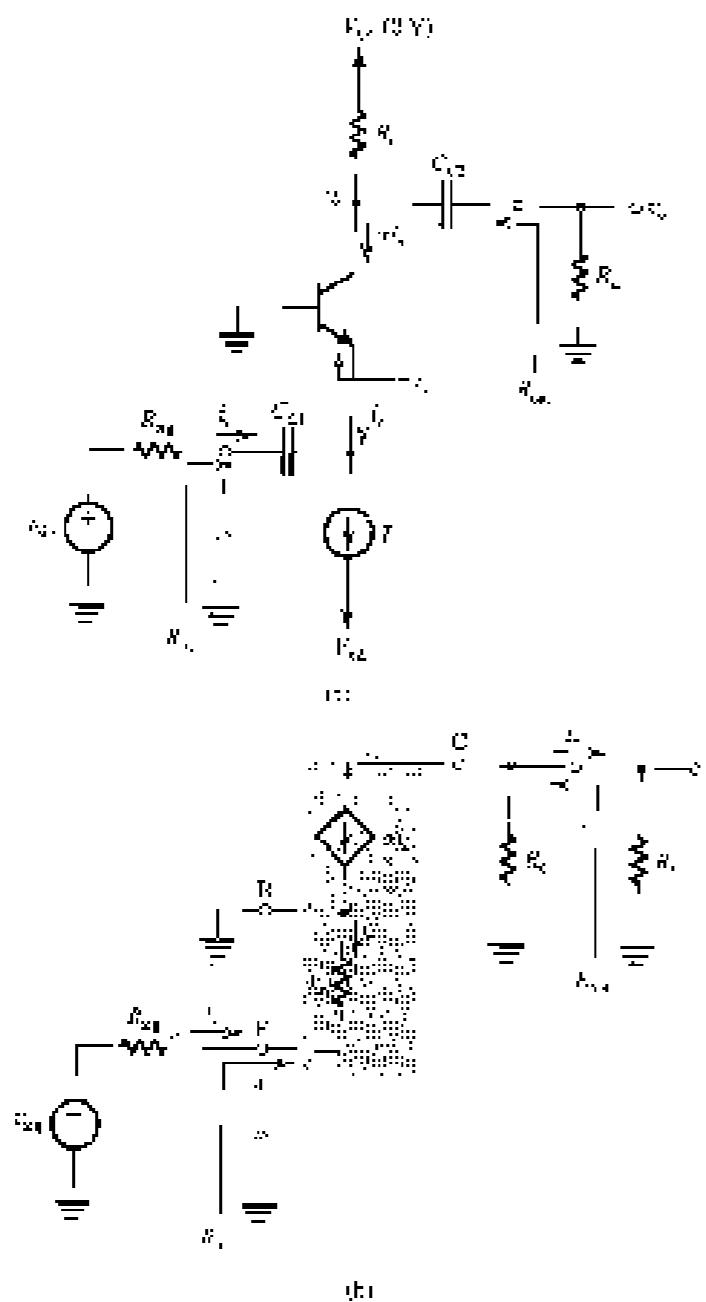


FIGURE 5.62. (a) A common-base amplifier using a diode as a current source. (b) Equivalent circuit obtained by neglecting the transistor's internal model.

The open-circuit voltage gain A_{v} can be found from Eq. (5.138) by setting $R_L = \infty$:

$$A_{\text{v}} = g_m R_C \quad (5.139)$$

Again, this is identical to A_{v} for the CE amplifier except that the CB amplifier is noninverting. The output resistance of the CB circuit can be found by inspection from the circuit in

Fig. 5.62(b):

$$R_{\text{out}} = R_C$$

which is similar to the case of the CE amplifier. Here we should note that the CB amplifier with r_o neglected is unidirectional, with the result that $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_C$.

The short-circuit current gain A_s is given by

$$A_s = \frac{-\alpha i_c}{i_b} = \frac{-\alpha^2}{r_i} = \alpha \quad (5.140)$$

which corresponds to our definition of α as the short-circuit current gain of the CB configuration.

Although the gain of the CB amplifier proper has the same magnitude as that of the CE amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CB amplifier can cause the input signal to be severely attenuated, specifically

$$\frac{V_i}{V_{\text{in}}} = \frac{R_i}{R_{\text{in}} + R_i} = \frac{r_i}{R_{\text{in}} + r_i} \quad (5.141)$$

from which we see that except for situations in which R_{in} is on the order of r_i , the signal transmission factor V_i/V_{in} can be very small. It is useful at this point to mention that one of the applications of the CB circuit is to amplify high-frequency signals that appear on a coaxial cable. To prevent signal reflection on the cable, the CB amplifier is required to have an input resistance equal to the characteristic resistance of the cable, which is usually in the range of 50 Ω or 75 Ω .

The overall voltage gain G_v of the CB amplifier can be obtained by multiplying the ratio V_i/V_{in} of Eq. (5.141) by A_s from Eq. (5.138),

$$G_v = \frac{\frac{r_i}{R_{\text{in}} + r_i} (\alpha R_C || R_L)}{\frac{\alpha (R_C || R_L)}{R_{\text{in}} + r_i}} \quad (5.142)$$

Since $\alpha \approx 1$, we see that the overall voltage gain is simply the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit. We also note that the overall voltage gain is almost independent of the value of β (except through the small dependence of α on β), a desirable property. Observe that for R_{in} of the same order as R_C and R_L , the gain will be very small.

In summary, the CB amplifier exhibits a very low input resistance (r_i), a short-circuit current gain that is nearly unity (α), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE amplifier ($\alpha(R_C || R_L)$), and for the CB amplifier, a relatively high output resistance (R_C). Because of its very low input resistance, the CB circuit alone is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB amplifier has excellent high-frequency performance as well, which as we shall see in Chapter 6 makes it useful together with other circuit ICs in the implementation of high-frequency amplifiers. Finally, a very significant application of the CB circuit is as a unity-gain current amplifier or current buffer. It accepts an input signal current at a low input resistance and delivers a nearly equal current at very high output resistance at the collector (the output resistance excluding R_C and neglecting r_i is infinite). We shall study such an application in the context of the IC version of the CB circuit in Chapter 6.

EXERCISES

5.6.15 Consider the amplifier of Fig. 5.59(a) using the T model with common-emitter feedback. Feed it by a sinusoidal source, resulting in Fig. 5.61(a). The bias conditions and the values of the TBJT small-signal parameters are the same as in Fig. 5.59, and the values of R_1 , R_2 , R_{out} , and R_{in} are also the same. Calculate the small-signal voltages with respect to ground at the output and at the collector in terms of β , r_e , and r_{ce} .

5.6.16 Design a CE amplifier with a voltage gain of $A_v = -10$. The input resistance is to be $10 \text{ k}\Omega$, and the output resistance is to be $100 \text{ }\mu\text{V}$. Use the TBJT with $\beta = 100$ and $r_{ce} = 100 \text{ }\Omega$. Assume $r_e = 10 \text{ }\Omega$.

5.7.6 The Common-Collector (CC) Amplifier or Emitter Follower

The last of the basic BJT amplifier configurations is the common-collector (CC) circuit, a very important circuit that finds frequent application in the audio and both in all-signal and large-signal amplifiers (Chapter 14) and even in digital circuits (Chapter 11). The circuit is also commonly known by the alternative name *emitter follower*, the reason for which will shortly become apparent.

An emitter follower circuit based on the structure of Fig. 5.59 is shown in Fig. 5.63(a). Observe that since the collector is to be at signal ground, we have eliminated the collector resistance R_C . The input signal is capacitively coupled to the base, and the output signal is capacitively coupled from the emitter to a load resistance R_L .

Since, as far as signals are concerned, resistance R_C is connected in series with the emitter, the T model of the BJT would be the most convenient one to use. Figure 5.63(b) shows the small-signal equivalent circuit of the emitter follower with the TBJT replaced by its T model augmented to include r_o . Here it is relatively simple to take r_o into account, and we shall do so. Inspection of the circuit in Fig. 5.63(b) reveals that r_o appears in effect in parallel with R_L . Therefore, the circuit is redrawn to emphasize this point, and reduced to simplify the analysis, in Fig. 5.63(c).

Unlike the CE and CB circuits we studied above, the emitter follower circuit is *noncentertapped*; that is, the input resistance depends on R_L , and the output resistance depends on R_{in} . Care therefore must be exercised in characterizing the emitter follower. In the following we shall derive expressions for R_{in} , R_{out} , G_{av} , and K_{v} . The expressions that we derive will shed light on the operation and characteristics of the emitter follower. More important than the actual expressions, however, are the methods we use to obtain them. It is in these that we hope the reader will become proficient.

Reference to Fig. 5.63(c) reveals that the BJT has a resistance ($r_o + R_L$) in series with the emitter resistance r_o . This application of the transmission-line reflection rule results in the equivalent circuit shown in Fig. 5.64(a). Recall that in referring resistances to the base side, we multiply all resistances in the emitter by $(\beta + 1)$, the ratio of i_e to i_b . In this way the voltages remain unchanged.

Inspection of the circuit in Fig. 5.64(a) shows that the input resistance at the base, R_{in} , is

$$R_{\text{in}} = (\beta + 1)(r_o + 1) \| R_{\text{in}} \quad (5.14-1)$$

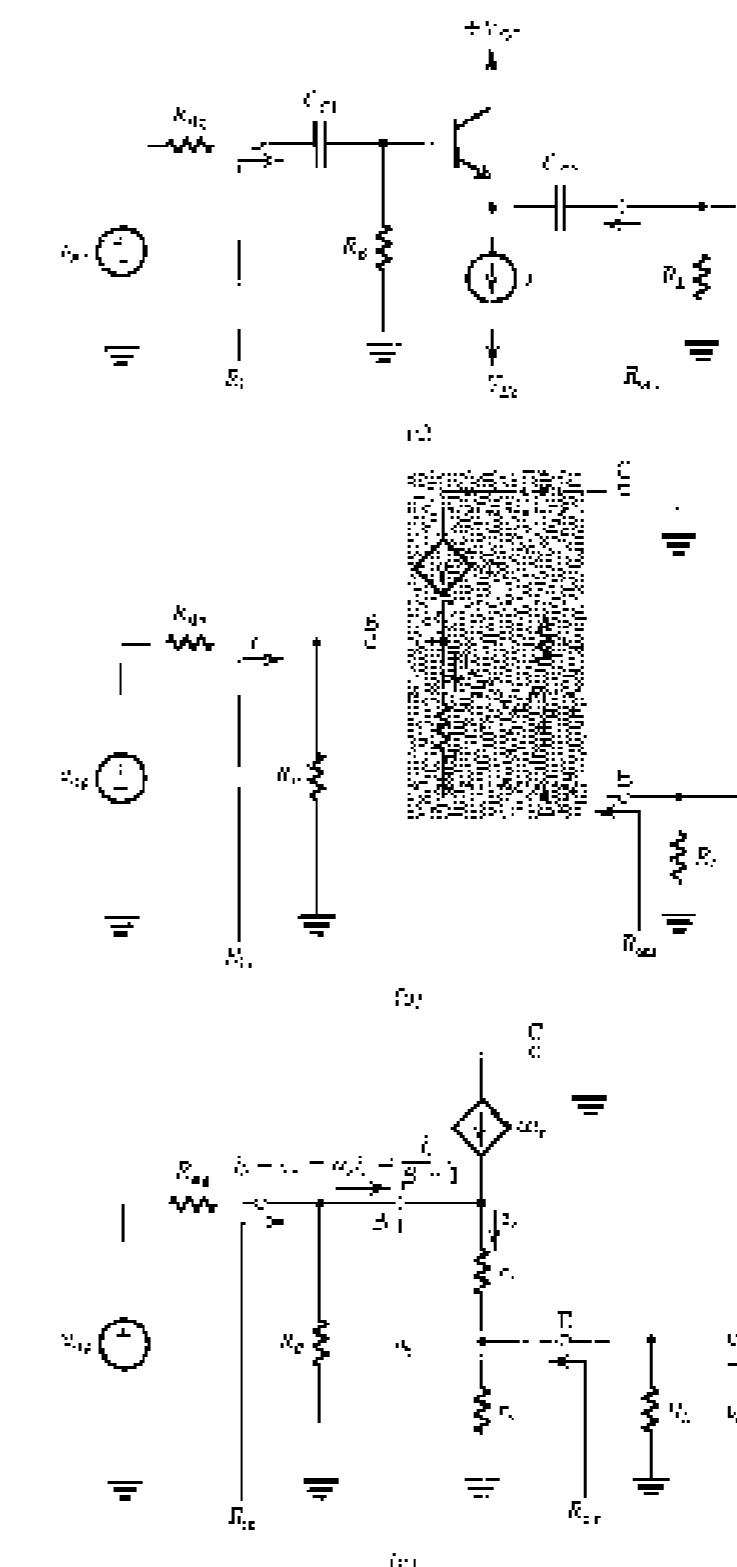


FIGURE 5.63 (a) An emitter follower circuit based on the structure of Fig. 5.59. (b) Small-signal equivalent circuit of the emitter follower with the collector resistance R_C removed. (c) Simplified small-signal equivalent circuit showing the effect of the output resistance r_o on the load R_L . This simplifies the analysis considerably.

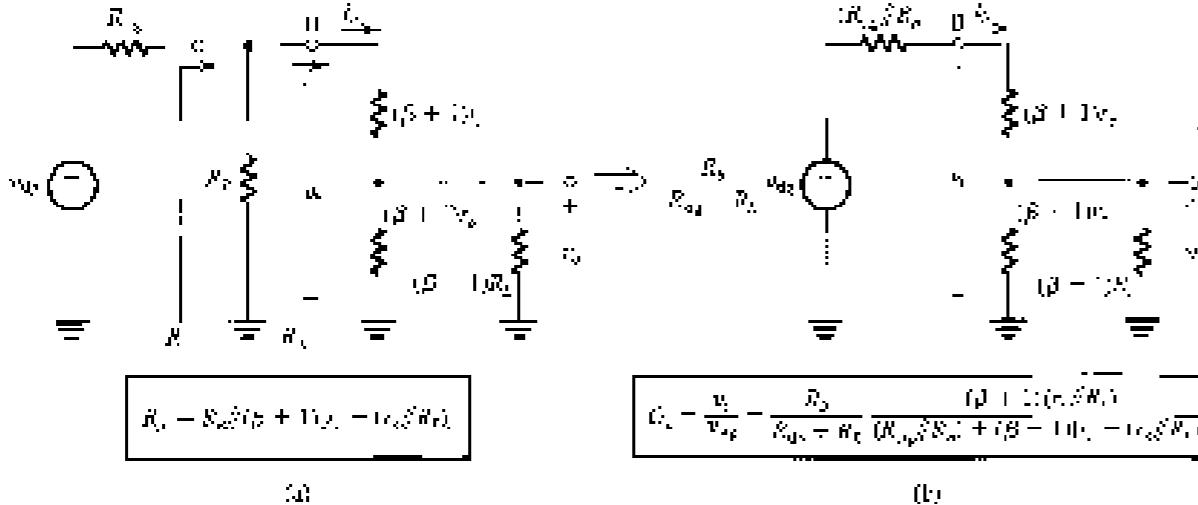


FIGURE 5.34 (a) An equivalent element of the π - π_0 between obtained from the circuit in Fig. 5.33 by reflecting all the sources in the circuit in its backplane. (b) The circuit after applying the π - π_0 theorem to the input circuit, composed only of R_{in} and R_{out} .

From which we see that the emitter-follower acts to raise the resistance level of R_1 (or $R_2 \parallel r_{e2}$, to be exact) by the factor ($\beta + 1$) and presents at the source the increased resistance. The total input resistance of the full circuit is:

R. k. S.

In which we see that to realize the full effect of the increased R_{in} , we have to choose a large value for the bias resistance R_2 as is natural. (E.g., from a bias design point of view.) Also, whenever possible, we should dispense with R_2 altogether and connect the signal source directly to the base (in which case we'd so dispense with C_{in}).

To find the overall voltage gain G_v , we first apply Thevenin theorem at the input side of the circuit in Fig. 5.64(a) to simplify it to the form shown in Fig. 5.64(b). From the latter circuit, we can obtain G_v as found by utilizing the voltage division rule that:

$$G_1 = \frac{K_2}{R_{11} + R_{21}} \frac{(b - 1)(r_1 - R_2)}{(R_{11} - R_{21}) + (b - 1)(r_1 + r_2 - R_2)} \quad (5.42)$$

We observe that the voltage gain is less than unity; however, for $R_3 \gg R_{ce}$ and $(\beta + 1) > 1$ ($r_o \parallel R_2$) $1 + (R_{ce} / R_3)$ becomes very close to unity. Thus the voltage at the emitter (v_e) follows very closely the voltage at the input, which gives the circuit the name emitter follower.

Rather than reflecting the emitter resistance network into the base side, we can do the converse: Reflect the base resistance network to the emitter side. To keep the voltage uncharged, we divide all the base-side resistances by $(\beta + 1)$. This is the dual of the resistance reflection rule. Doing this for the circuit in Fig. 5.63(c) results in the alternate emitter follower equivalent circuit shown in Fig. 5.63(n). Here also we can simplify the circuit by applying Thevenin's theorem at the input side, resulting in the circuit in Fig. 5.63(o). Inspection

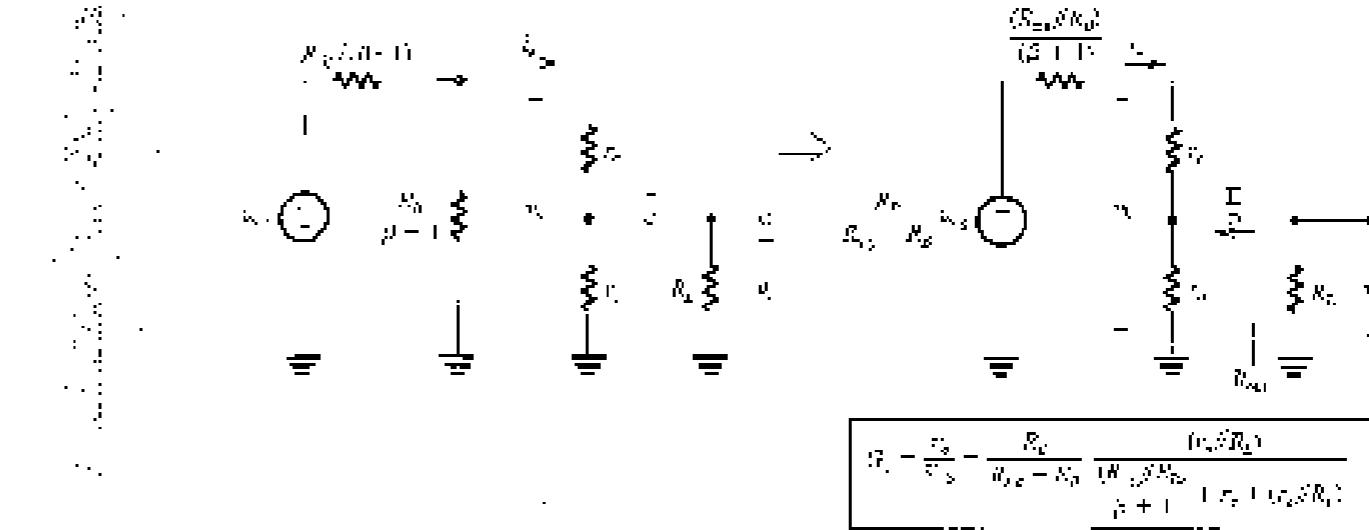


FIGURE 3.85 (a) An alternative equivalent circuit for the network shown in Fig. 3.84. (b) The circuit in (a) after application of thevenin theorem to the input circuit components.

of the latter reveals that the output voltage and the resistors R_1 , R_2 can be found by a simple application of the voltage divider rule, with the result that

$$G_1 = \frac{R_3}{R_{21} + R_2} \frac{(G_2 + R_{21})}{\frac{R_{21}}{S-1} + G_2 - G_1 + R_{21} R_{22}} \quad (5.45)$$

which, as expected, is identical to the expression in Eq. (8.174) except that both the numbers and denominators of the second factor on the right-hand side have been divided by $(\beta - 1)$. To gain further insight regarding the behavior of the enthalpy function, let's simplify this expression in the usual case of $\theta_1 < \theta_c$ and $\varepsilon_1 < R_c$. The result is

$$\frac{R_{M_1} R_{M_2}}{R_{M_3}} = \frac{R_1}{\frac{R_{M_1}}{2 + \epsilon} + R_2 + R_3} \quad (5.146)$$

which clearly indicates that the gain approaches unity when $K_{\text{eq}}/\beta = 1$; because β is smaller than R_E , or alternatively when $(\beta + 1)K_{\text{eq}}$ becomes much larger than R_{in} . This is the buffering action of the emitter follower, which derives from the fact that the circuit has a short-circuit current gain that is approximately equal to $(\beta + 1)$.

This is equivalent to represent the output of the emitter follower by its Thevenin equivalent circuit. The open-circuit output voltage will be $G_{\text{v}}V_{\text{cc}}$, where G_{v} can be obtained from Eq. (5.145) by setting $R_{\text{L}} = \infty$.

$$C_{\text{in}} = \frac{K_B}{R_{\text{in}} + R_{\text{in}}} \frac{1}{R_{\text{in}} + R_{\text{in}} - r_{\text{in}} + r_{\text{out}}} \quad (S-1-7)$$

Note that r_o usually is large and the second factor becomes almost unity. The first factor approaches unity for $N_A \gg R_{in}$. The Thevenin resistance is the output resistance R_{out} . It can be determined by inspection of the circuit in Fig. 5.60(b). Reduce v_{in} to zero. "Fix" the base terminal and look back into the circuit. The result is

$$R_{out} = r_o \left(1 + \frac{R_{in} \| R_E}{\beta + 1} \right) \quad (5.148)$$

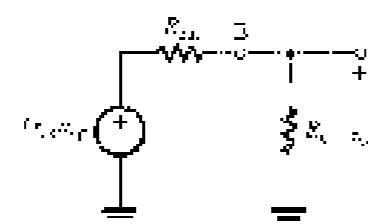
Usually r_o is much larger than the parallel component between the parentheses and can be neglected, leaving

$$R_{out} \approx r_o \left(1 + \frac{R_{in}}{\beta + 1} \right) \quad (5.149)$$

Thus the output resistance of the emitter follower is low, again a result of its impedance transformation or buffering action, which leads to the division of $(R_{in} \| R_E)$ by $(\beta + 1)$. The Thevenin equivalent circuit of the emitter follower is shown together with the feedback bias G_{in} and R_{out} in Fig. 5.66. This circuit can be used to find r_o and hence G_{in} for any value of R_E .

In summary, the emitter follower exhibits a high input resistance, a low output resistance, a voltage gain that is smaller than but close to unity, and a relatively large current gain. It is therefore ideally suited for applications in which a high-resistance source is to be connected to a low-resistance load—namely, as the last stage in output stages in a multistage amplifier, where its purpose would be not to supply additional voltage gain but rather to give the cascade amplifier a low output resistance. We shall study the design of amplifier output stages in Chapter 11.

Before leaving the emitter follower, the question of the maximum allowed signal swing receives comment. Since only a small fraction of the input signal appears between the base and the emitter, the emitter follower exhibits linear operation for a wide range of input signal amplitude. There is, however, an absolute upper limit imposed on the value of the output signal amplitude by one diode effect. To examine this corner about the emitter the circuit of Fig. 5.63(a) when the input signal is a sine wave. As the input goes negative,



$$\begin{aligned} G_{in} &= \frac{R_E}{R_{in} + R_E (R_{in} / R_E)} \frac{r_o}{(\beta + 1) + r_o / R_E} \\ &\approx \frac{R_E}{R_{in} (\beta + 1)} \end{aligned}$$

FIGURE 5.66 Thevenin equivalent circuit of the output of the emitter follower of Fig. 5.60(a). This circuit can be used to find r_o and hence the overall voltage gain $G_{out} = v_{out}/v_{in}$ for any load R_L .

the output v_o will also go negative, and the current in R_E will be flowing from ground into the emitter terminal. The transistor will cut off when this current becomes equal to the bias current I . Thus the peak value of v_o can be found from

$$\frac{V_T}{R_E} = I$$

$$V_T = IR_E$$

The corresponding value of v_{in} will be

$$V_{in} = \frac{IR_E}{G_{in}}$$

Increasing the amplitude of v_{in} above this value results in the transistor becoming cut off and the negative peaks of the output signal waveform being clipped off.

EXERCISE

- 5.7.1 The circuit shown in Fig. 5.67(a) is used to determine the bias point $V_B = -10$ mV and $R_E = 1 k\Omega$. The transistor is biased at $\beta = 50$ with $r_o = 100 \Omega$, $N_A = 100$, and $V_A = 100$ V. For $R_{in} = 100 k\Omega$, G_{in} , r_o , and R_{out} . What is the largest peak amplitude of the output signal that can be used without the transistor cutting off? (In order to find the bias point, determine the base-emitter signal voltage $V_{BE} = 0.3$ mV and calculate the corresponding amplitude of the current.) What will the overall voltage gain G_{out} be if R_E is changed to $2 k\Omega$? (In this case, $V_B = -10$ mV and $R_{in} = 100 k\Omega$.)
- Answers: 500 mV, 2.5 V/V, 0.8 V/V; 84.63 V/V, 0.3 V/V; 0.763 V/V; 0.655 V/V

5.7.7 Summary and Comparisons

For easy reference and enable comparisons, we present in Table 5.6 the formulas for determining the characteristic parameters of discrete single-stage BJT amplifiers. In addition to the remarks already made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

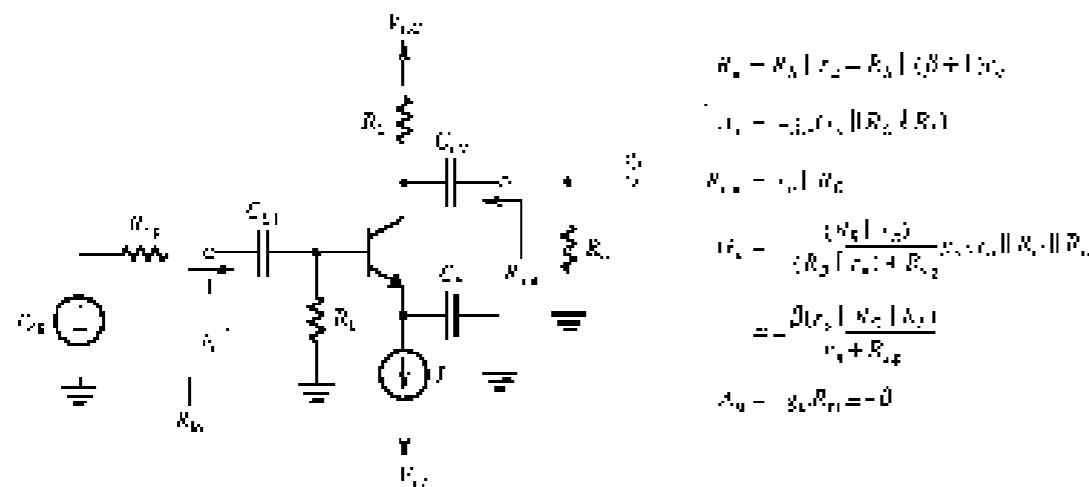
1. The CB configuration is the best choice for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor R_E in the emitter lead of the CE stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CB amplifier makes it useful only in specific applications. As we shall see in Chapter 6, it has a much better high-frequency response than the CE amplifier. This superiority will make it useful as a high-frequency amplifier, especially when combined with the CE circuit. We shall see one such combination in Chapter 6.

4. The emitter follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier.

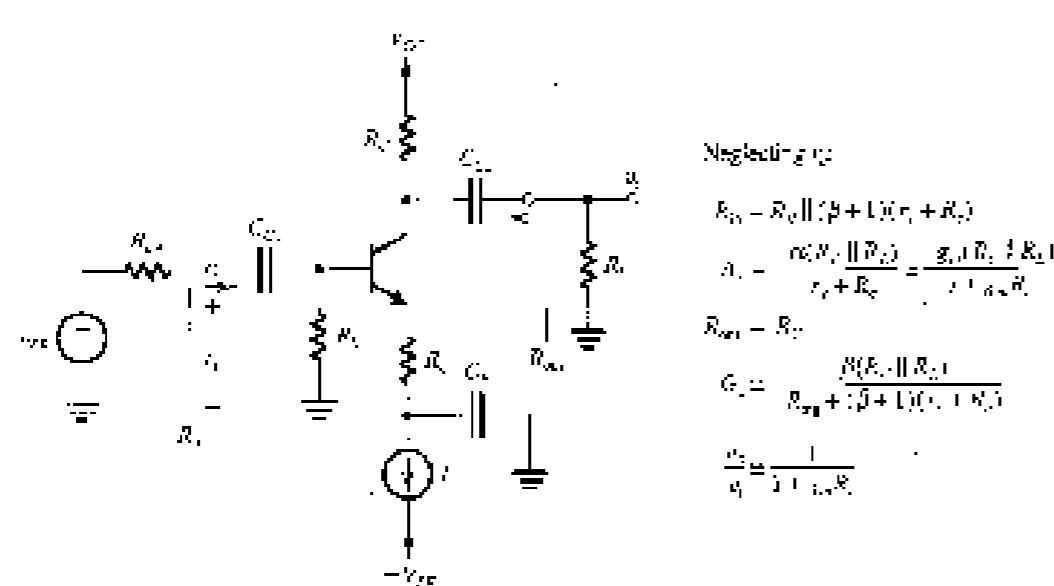
Finally, we should note again that the Exercises in this section (except for that relating to the emitter follower) used the same component values to allow for vertical comparisons.

TABLE 5.6 Characteristics of Single-Stage Discrete BJT Amplifiers

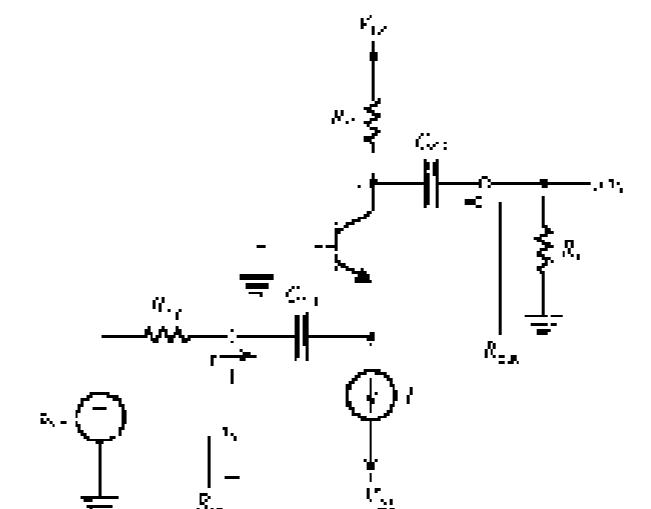
Common Emitter



Common Emitter with Emitter Resistance



Common Base



Neglecting r_o :

$$R_{in} = r_s$$

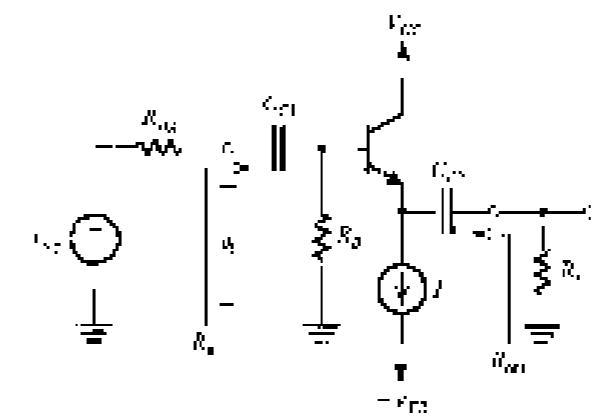
$$A_v = g_m (R_L + R_2)$$

$$R_{out} = R_L$$

$$C_{in} = \frac{\alpha(R_2 + R_L)}{R_{in} + R_2}$$

$$A_{v0} = \alpha$$

Common Collector or Emitter Follower



$$R_{in} = R_1 \parallel (\beta + 1)(r_s + R_2 + R_1)$$

$$A_v = \frac{(r_s + R_2)}{(r_s + R_2) + r_o}$$

$$R_{out} = r_o \parallel \frac{R_{in} \parallel R_2}{\beta + 1}$$

$$C_{in} = \frac{R_2}{R_2 + R_{in} \parallel R_1} \frac{R_{in} \parallel R_2}{\beta + 1} = \frac{1}{\beta + 1} R_2$$

$$A_{v0} = \beta + 1$$

5.8 THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

Thus far we have assumed transistor action to be instantaneous, and as a result the transistor models we have developed do not include any elements (i.e., capacitors or inductors) that would cause time or frequency dependence. Actual transistors, however, exhibit charge-storage phenomena that limit the speed and frequency of their operation. We have already encountered such effects in our study of the pn junction in Chapter 3 and learned that they can be modeled using capacitances. In the following we study the charge-storage effects that take place in the BJT and take them into account by adding capacitances to the hybrid-p

model. The resulting parameter in BJT mode will be able to predict the observed dependence of amplifier gain on frequency and the time delays that transistor switches and logic gates exhibit.

5.8.1 The Base-Charging or Diffusion Capacitance C_{de}

When the transistor is operating in the active or saturation modes, minority-carrier charge is stored in the base region. In fact, we have already derived an expression for this charge, Q_e , in the case of an n-p-n transistor operating in the active mode (Eq. 5.7). Using the result [Eq. (5.5)] together with Eqs. (5.3) and (5.7), we can express Q_e in terms of the collector current I_C :

$$Q_e = \frac{W^2}{2D_p} I_C + V_{BE} t_0 \quad (5.150)$$

where t_0 is a device constant.

$$t_0 = \frac{R^2}{2D_p} \quad (5.151)$$

with the dimension of time. It is known as the forward-bias transit time and represents the average time a charge carrier (electron) spends in crossing the base. Typically, t_0 is in the range of 20 ps to 100 ps. For operation in the reverse-active mode, a corresponding expression t_0 applies and is many orders of magnitude larger than t_0 .

Equation (5.150) applies for large signals and shows Q_e exponentially related to I_C . Q_e will similarly depend on V_{BE} . Thus this charge-storage mechanism represents a nonlinear capacitive effect. However, for small signals, we can define the small-signal diffusion capacitance C_{de} :

$$\begin{aligned} C_{de} &= \frac{dQ_e}{dV_{BE}} \\ &= \tau_0 \frac{dI_C}{dV_{BE}} \end{aligned} \quad (5.152)$$

resulting in

$$C_{de} = \tau_0 g_m = \tau_0 \frac{I_C}{V_{TF}} \quad (5.153)$$

5.8.2 The Base-Emitter Junction Capacitance C_{je}

Using the development in Chapter 2, and in particular Eq. (3.59), the base-emitter junction or depletion-layer capacitance C_{je} can be expressed as

$$C_{je} = \frac{C_{j0}}{1 - \frac{V_{BE}}{V_{j0}}} \quad (5.154)$$

where C_{j0} is the value of C_{je} at zero voltage, V_{j0} is the BJT built-in voltage (typically 0.7 V), and α is the grading coefficient of the BJT junction (typically, 0.5). It turns out, however, that because the BJT is forward biased in the active mode, Eq. (5.154) does not provide an accurate prediction of C_{je} . Alternatively, one typically uses an approximate value for C_{je} :

$$C_{je} = 2C_{j0} \quad (5.155)$$

5.8.3 The Collector-Base Junction Capacitance C_{cb}

In active-mode operation, the CBJ is reverse biased, and its junction or depletion capacitance, usually denoted C_{cb} , can be found from:

$$C_{cb} = \frac{C_{j0}}{\left(1 + \frac{V_{CB}}{V_{j0}}\right)^{\alpha}} \quad (5.156)$$

where C_{j0} is the value of C_{je} at zero voltage, V_{j0} is the CBJ built-in voltage (typically, 0.75 V), and α is the grading coefficient (typically, 0.2–0.5).

5.8.4 The High-Frequency Hybrid- π Model

Figure 5.67 shows the hybrid- π model of the BJT, including capacitive effects. Specifically, there are two capacitances: the emitter-base capacitance $C_e = C_{je} + C_{cb}$ and the collector-base capacitance C_{cb} . Typically, C_e is in the range of a few picofarads to a few tens of picofarads, and C_{cb} is in the range of a fraction of a picofarad to a few picofarads. Note that we have also added a resistor r_e to model the resistance of the silicon material of the base region between the base terminal B and a fictitious intrinsic base terminal B' that is right under the emitter region (refer to Fig. 5.6). Typically, r_e is a few tens of ohms, and its value depends on the current level and other complicated factors. Since usually $r_e \ll r_o$, its effect is negligible at low frequencies. Its presence is felt, however, at high frequencies, as will become apparent later.

The values of the hybrid- π equivalent circuit parameters can be determined at a given bias point using the formulas presented in this chapter. They can also be found from the transistor's measurement as specified on the BJT data sheets. For computer simulation, SPICE uses the parameters of the given IC technology to evaluate the BJT model parameters (Section 5.11).

Before proceeding, a note on notation is in order. Since we are now dealing with voltages and currents that are functions of frequency, we have reverted to using symbols that are uppercase letters with lowercase subscripts (e.g., V_s , I_s). This conforms to the notation system used throughout this book.

5.8.5 The Cutoff Frequency

The transistor data sheets do not usually specify the value of C_{je} . Rather, the behavior of β from I_C versus frequency is usually given. In order to determine C_{je} and C_{cb} , we shall derive an expression for I_C , the CE short-circuit current gain, as a function of frequency in terms of

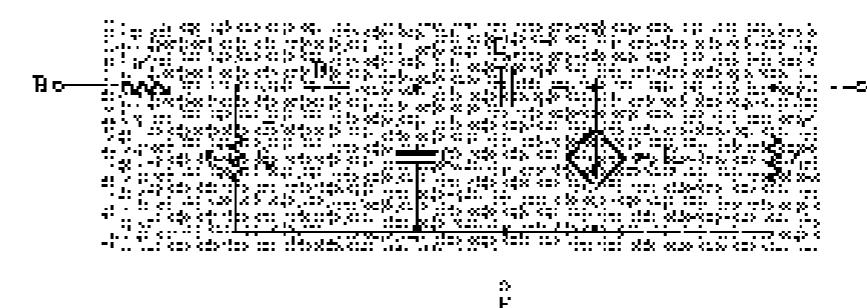
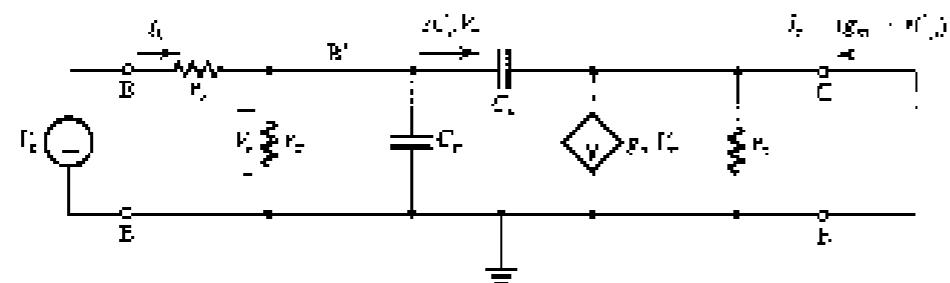


FIGURE 5.67 The high-frequency hybrid- π model.

FIGURE 5.68 Circuit for evaluating expression for β , $\beta = I_C/I_E$.

the hybrid π components. For this purpose consider the circuit shown in Fig. 5.68, in which the collector is returned to the emitter. A noise equation in C provides the short-circuit current density current I_{ss} as

$$I_{\text{ss}} = (g_m + sC_p)V_B \quad (5.157)$$

A relationship between V_B and I_C can be established by multiplying I_C by the impedance seen between B' and E:

$$V_B = I_C(1 + s(C_p + C_s)) = \frac{I_C}{1/\beta_0 + s(C_p + C_s)} \quad (5.158)$$

Thus β_0 can be obtained by combining Eqs. (5.157) and (5.158):

$$\beta_0 = \frac{I_C}{I_{\text{ss}}} = \frac{g_m + C_p}{1/\beta_0 + s(C_p + C_s)}$$

At the frequencies for which this model is valid, $sC_p \gg sC_s$; thus we can neglect the sC_s term in the numerator and write

$$\beta_0 = \frac{g_m V_B}{1 + s(C_p + C_s)V_B}$$

Thus,

$$\beta_0 = \frac{\beta_0}{1 + s(C_p + C_s)\omega} \quad (5.159)$$

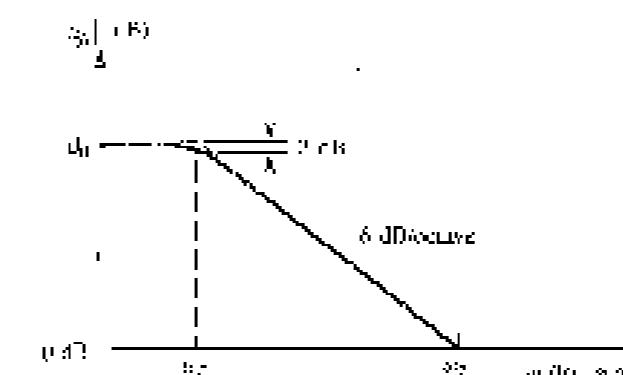
where β_0 is the low-frequency value of β . Thus β_0 has a single pole (or STC) response¹² with a 3-dB frequency at $\omega = \omega_0$, where

$$\omega_0 = \frac{1}{(C_p + C_s)\beta_0} \quad (5.160)$$

Figure 5.69 shows a plot of β_0 versus I_C . From the -6-dB/octave slope it follows that the frequency at which β_0 drops to unity, which is called the unity-gain bandwidth f_T , is given by

$$\omega_T = \beta_0 f_T \quad (5.161)$$

¹²The frequency response of a load-invariant (STC) network was reviewed in Section 4.6. A more detailed discussion of this important topic can be found in Appendix D.

FIGURE 5.69 Beta plot of β_0 .

Then

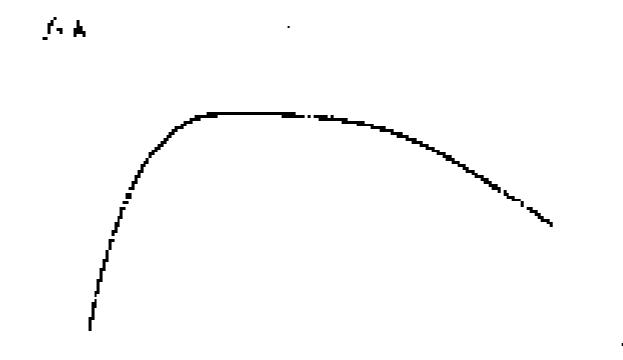
$$\omega_T = \frac{\lambda_0}{C_p + C_s} \quad (5.162)$$

and

$$f_T = \frac{\lambda_0}{2\pi(C_p + C_s)} \quad (5.163)$$

The unity-gain bandwidth f_T is usually specified on the data sheets of a transistor. In some cases f_T is given as a function of I_C and V_{CE} . To see how f_T changes with I_C , recall that g_m is directly proportional to I_C , but only part of C_p (the diffusion capacitance C_{ds}) is inversely proportional to I_C . It follows that f_T increases at low currents, as shown in Fig. 5.70. However, the decrease in f_T at high currents, also shown in Fig. 5.70, cannot be explained by this argument; rather it is due to the same phenomenon that causes β to decrease at high currents. In the region where β is almost constant, C_p is dominated by the diffusion part.

Typically, f_T is in the range of 100 MHz to tens of GHz. The value of f_T can be used in Eq. (5.159) to determine $C_p + C_s$. The capacitance C_s is usually determined separately by measuring the capacitance between base and collector at the desired reverse-bias voltage V_{BR} :

FIGURE 5.70 Variation of f_T with I_C .

acting as perfect short circuits at all signal frequencies of interest. We also neglected the internal capacitances of the BJT. That is, C_{g} and C_{gs} of the BJT high-frequency model (Fig. 5.67) were assumed to be sufficiently small to act as open circuits at all signal frequencies of interest. As a result of ignoring all capacitive effects, the gain expressions derived in Section 5.7.3 were independent of frequency. In reality, however, this situation only applies over a limited, though usually wide, band of frequencies. This is illustrated in Fig. 5.71(b), which shows a sketch of the magnitude of the overall voltage gain, $|A_V|$, of the common-emitter amplifier versus frequency. We observe that the gain is almost constant over a wide frequency band, called the midband. The value of the midband gain A_M corresponds to the overall voltage gain A_V that we derived at Section 5.7.3, namely,

$$A_M = \frac{V_o}{V_{\text{in}}} = \frac{(R_E \parallel r_{\text{out}})}{(R_E + r_{\text{in}}) + R_{\text{ds}}} g_{\text{m}}(r_{\text{in}} \parallel R_{\text{ds}} \parallel R_E) \quad (5.184)$$

Figure 5.71(b) shows that the gain falls off at signal frequencies below and above the midband. The gain fall-off in the low-frequency band is due to the fact that even though C_{g} , C_{gs} , and C_{os} are large capacitors (typically, in the μF range), as the signal frequency is reduced their impedances increase and they no longer behave as short circuits. On the other hand, the gain falls off in the high-frequency band as a result of C_{g} and C_{os} , which become very small (in the fraction of a pF to the pF range), their impedances at sufficiently high frequencies decrease; thus they can no longer be considered as open circuits. Our objective in this section is to study the mechanisms by which these two sets of capacitors affect the amplifier gain in the low-frequency and the high-frequency bands. In this way we will be able to determine the frequencies f_L and f_H , which define the extent of the midband, as shown in Fig. 5.71(b).

The midband is obviously the useful frequency band of the amplifier. Usually, f_L and f_H are the frequencies at which the gain drops by 1 dB below its value at midband; that is, at f_L and f_H , $\text{gain} = A_M / \sqrt{2}$. The amplifier bandwidth or 3-dB bandwidth is defined as the difference between the lower (f_L) and upper (f_H) 3-dB frequencies:

$$\Delta f = f_H - f_L \quad (5.185)$$

Since usually $f_L \ll f_H$,

$$\Delta f \approx f_H$$

A figure-of-merit for the amplifier is its gain-bandwidth product, defined as

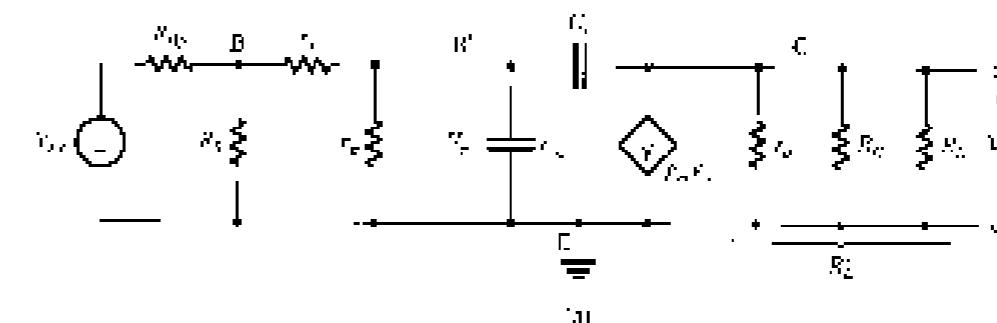
$$\text{GBW} = A_M / \Delta f \quad (5.186)$$

It will be shown at a later stage that in amplifier design, it is usually possible to trade off gain for bandwidth. One way of accomplishing this, for instance, is by including an emitter-degeneration resistance R_{d} , as we have done in Section 5.7.4.

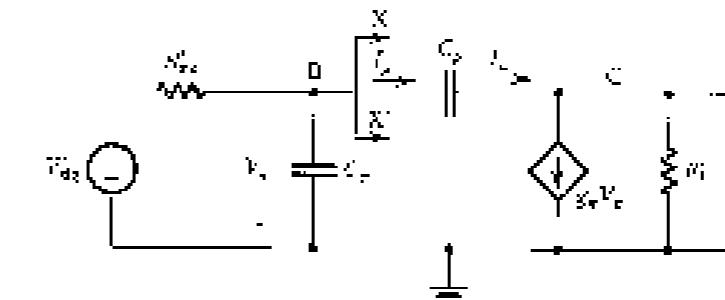
5.8.2 The High-Frequency Response

To determine the gain, or the transfer function, of the amplifier of Fig. 5.71(a) at high frequencies, and in particular for the upper 3-dB frequency f_H , we replace the BJT with the high-frequency model of Fig. 5.67. At these frequencies C_{g} , C_{gs} , and C_{os} will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit, shown in Fig. 5.72(a).

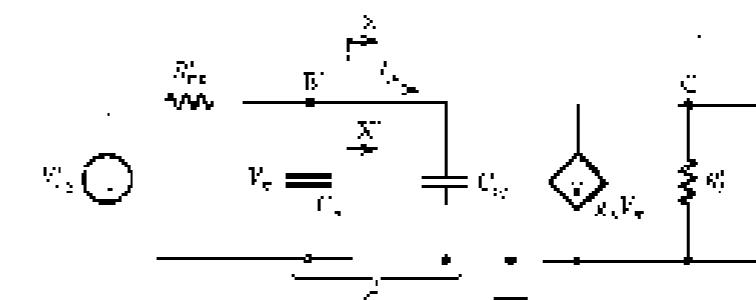
The equivalent circuit of Fig. 5.72(a) can be simplified by utilizing Thévenin's theorem at the input side and by combining the three parallel resistances at the output side. Specifically, the reader should be able to show that applying Thévenin's theorem *twice* simplifies the resistive network at the input side to a signal generator V_{in} and a resistance R'_{in} :



(a)



(b)



(c)

FIGURE 5.72 Determining the high-frequency response of the CE amplifier: (a) equivalent circuit; (b) the circuit of (a) simplified with the dependent and the output-side load equivalents; (c) the circuit of (b) with the input-side load equivalent C_{in} .

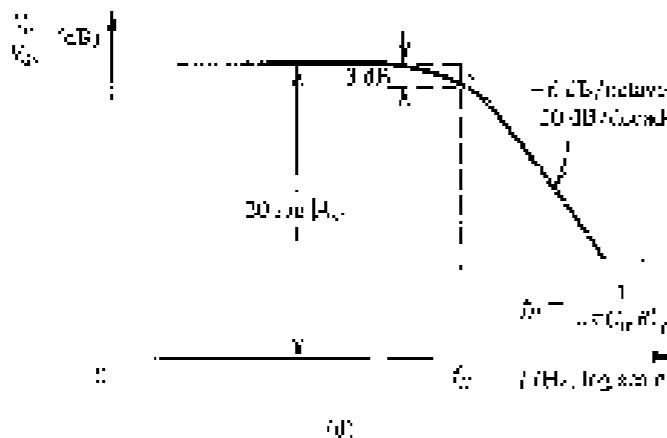


FIGURE 5.72 A hand-drawn sketch of the frequency response of the midband of a low-pass STC circuit.

where

$$V'_{in} = V_{in} \frac{R_s}{R_s + R_{in}} \frac{r_s}{r_s + (R_{in} \parallel R_s)} \quad (5.167)$$

$$R'_{in} = r_s + (r_s + (R_s \parallel R_{in}))^{-1} \quad (5.168)$$

Observe that R'_{in} is the resistance seen looking back into the positive network between nodes B' and B.

The circuit in Fig. 5.72(b) can be simplified further if we can find a way to deal with the leading capacitance C_p that connects the output node to the "input" node, B'. To do this end consider first the output node. It can be seen that the total current is $i_o = V_o / R_{out}$, where V_o is the output voltage of the transistor and i_o is the current supplied through the very small capacitance C_p . In the vicinity of f_0 , which is close to the edge of the roll-off, it is reasonable to assume that i_o is much smaller than $\beta_o V_o$, with the result that V_o can be given approximately by

$$V_o \approx \beta_o V_{in} R'_o = \beta_o R'_o V_{in} \quad (5.169)$$

Since $V_o = V_{in}$, Eq. (5.169) indicates that the gain from B' to C' is $\beta_o R'_o$, the same value as in the midband. The current i_o can now be found from

$$\begin{aligned} i_o &= \beta C_p (V_{in} - V_o) \\ &= \beta C_p (V_{in} - (\beta_o R'_o) V_{in}) \\ &= \beta C_p (1 - \beta_o R'_o) V_{in} \end{aligned}$$

Now, in Fig. 5.72(b), the left-hand side of the circuit, at XX', knows of the existence of C_p only through the current i_o . Therefore we can replace C_p by an equivalent conductance G_p between B' and ground as long as C_p draws a current equal to i_o . That is,

$$\beta C_p V_{in} = i_o = \beta C_p (1 - \beta_o R'_o) V_{in}$$

which results in:

$$G_p = \beta_o (1 - \beta_o R'_o) \quad (5.170)$$

Using G_p enables us to simplify the equivalent circuit in the input side to that shown in Fig. 5.72(c), which we recognize as a single-time-constant (STC) network of the low-pass type (see Section 5.6 and Appendix D). Therefore we can express V_o in terms of V_{in} as

$$V_o = V'_{in} \frac{1}{1 + j\omega/\omega_0} \quad (5.171)$$

where ω_0 is the corner frequency of the STC network composed of C_p and R'_{in} ,

$$\omega_0 = 1/C_p R'_{in} \quad (5.172)$$

where C_p is the input input capacitance of B.

$$C_p = C_{in} + C_{ox} = C_{in} + C_o (1 + \omega_0 R'_o) \quad (5.173)$$

and R'_{in} is the effective source resistance given by Eq. (5.168). Combining Eqs. (5.169), (5.171), and (5.173) give the voltage gain in the high-frequency band as

$$\frac{V_o}{V_{in}} = \frac{-\beta_o r_s}{R_s + R_{in} + r_s + (R_{in} \parallel R_s)} \frac{r_s + \beta_o R_s}{r_s + (R_{in} \parallel R_s)} \frac{1}{1 + j\omega/\omega_0} \quad (5.174)$$

The quantity between the square brackets of Eq. (5.174) is the midband gain, and except for the fact that here r_s is taken into account, this expression is the same as that in Eq. (5.164). Thus,

$$\frac{V_o}{V_{in}} = \frac{\beta_o}{1 + \frac{j\omega}{\omega_0}} \quad (5.175)$$

from which we deduce that the upper 3-dB frequency f_H must be

$$f_H = \frac{\omega_0}{2\pi} = \frac{1}{2\pi C_p R'_{in}} \quad (5.176)$$

Thus we see that the high-frequency response will be that of a low-pass STC network with a 3-dB frequency f_H determined by the time constant $C_p R'_{in}$. Fig. 5.72(d) shows a sketch of the magnitude of the high-frequency gain.

Before leaving this section we wish to make a number of observations:

1. The upper 3-dB frequency is determined by the intersection of R'_{in} and C_p . If $R_{in} \gg R_{in}'$ and $r_s \gg R_{in}'$, then $R'_{in} \approx R_{in} \parallel r_s$. Thus the extent to which R_{in} determines f_H depends on its value relative to r_s . If $R_{in} \ll r_s$, then $R'_{in} \approx r_s$; on the other hand, if R_{in} is on the order of or smaller than r_s , then it has much greater influence on the value of ω_0 .
2. The input capacitance C_{in} is usually dominated by C_{ox} , which in turn is made large by the multiplication effect that C_p undergoes. Thus although C_p is usually very small, its effect on the high-frequency response can be significant as a result of its

- and inversion by the factor $(1 + g_m R_2)$, which is approximately equal to the midband gain of the amplifier.
- The multiplication effect that C_2 undergoes comes about because it is connected between two nodes (B' and C) whose voltages are related by a large negative gain $(-g_m R_2)$. This effect is known as the **Miller effect**, and $(1 + g_m R_2)$ is known as the **Miller multiplier**. It is the Miller effect that causes the C^+ amplifier to have a large input capacitance C_{in} , and hence a low f_L .
 - To extend the high-frequency response of a BJT amplifier, we have to find configurations in which the Miller effect is absent or at least reduced. We shall return to this subject at great length in Chapter 6.
 - The above analysis, resulting in an SLC, or a single-pole response, is simplified one. Specifically, it is based on neglecting r_o relative to $g_m V_{ce}$, an assumption that applies well at frequencies not too much higher than f_L . A more exact analysis of the circuit in Fig. 5.7(a) will be considered in Chapter 6. The results shown, however, are more than sufficient for our present needs.

Example 5.7 It is required to find the midband gain and the upper -3-dB frequency of the common-emitter amplifier of Fig. 5.7(a) for the following case: $V_{CC} = V_{BE} = 0.0$ V, $i = 1 \mu\text{A}$, $R_S = 100 \text{ k}\Omega$, $R_C = 3 \text{ k}\Omega$, $R_{AE} = 5 \text{ k}\Omega$, $R_E = 0$, $V_A = 100 \text{ V}$, $C_2 = 1 \text{ pF}$, $f_L = 800 \text{ MHz}$, and $r_o = 50 \text{ M}\Omega$.

Solution

The transistor is biased at $I_C = 1 \mu\text{A}$. Thus the values of its hybrid π -model parameters are

$$r_{\pi} = \frac{V_T}{I_C} = \frac{25 \text{ mV}}{1 \mu\text{A}} = 25 \text{ m}\Omega/\text{V}$$

$$r_{\pi} + \frac{\beta}{I_C} = \frac{100}{1 \mu\text{A}} = 100 \text{ k}\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{100 \text{ V}}{1 \mu\text{A}} = 100 \text{ k}\Omega$$

$$C_{\pi} = C_{AE} = \frac{g_m}{\omega_c} = \frac{40 \times 10^{-3}}{2 \pi \times 800 \times 10^9} = 3 \text{ pF}$$

$$C_2 = 1 \text{ pF}$$

$$r_s = 50 \text{ }\Omega$$

The midband voltage gain is

$$A_{21} = -\frac{R_C}{R_S + R_{AE} r_{\pi} + r_s + (R_S + R_{AE}) R_{AE} R_C^2}$$

where

$$\begin{aligned} R_C^2 &= r_{\pi} \parallel R_C \parallel R_E \\ &= (100 + 5) \text{ k}\Omega = 5 \text{ k}\Omega \end{aligned}$$

Thus,

$$r_{\pi} R_2^2 = 25 \times 5 = 125 \text{ m}\Omega$$

and

$$\begin{aligned} A_{21} &= \frac{100}{100+5} \times \frac{2.5}{2.5+0.05+(100+5)} \times 125 \\ &= -39 \text{ V/V} \end{aligned}$$

and

$$20 \log |A_{21}| = 32.45$$

To determine f_L , we use the C_{in} ,

$$\begin{aligned} C_{in} &= C_2 + C_{AE}(1 + g_m R_2) \\ &= 7 + 1 + 125 = 128 \text{ pF} \end{aligned}$$

and the effective source resistance R_{eq} ,

$$\begin{aligned} R_{eq} &= r_s \parallel (r_{\pi} + (R_S + R_{AE}) R_C^2) \\ &= 25 \parallel (0.05 + (100+5) \text{ k}\Omega) \\ &= 6.7 \text{ k}\Omega \end{aligned}$$

Thus,

$$f_L = \frac{1}{2\pi C_{in} R_{eq}} = \frac{1}{2\pi \times 128 \times 10^{-12} \times 6.7 \times 10^3} = 154 \text{ MHz}$$

EXERCISE

5.11-12 The circuit in Fig. 5.7(b) is the same as Fig. 5.7(a), except that the collector load is R_C and the source is V_{CC} (not r_s). Determine the value of r_{π} and the low-frequency gain and bandwidth of the circuit. (Ans. $r_{\pi} = 25 \text{ m}\Omega$; $A_{21} = -39 \text{ V/V}$; $f_L = 154 \text{ MHz}$.)

5.9.2 The Low-Frequency Response

To determine the low-frequency gain (or transfer function) of the common-emitter amplifier circuit, we show in Fig. 5.73(a) the circuit with the dc sources eliminated (current source I open circuited) and voltage source V_{CC} short-circuited. We shall perform the small-signal analysis directly on this circuit. We will, of course, ignore C_2 and C_1 since at such low frequencies their impedances will be very high and thus can be considered as open circuits. Also, to keep the analysis simple and thus focus attention on the mechanisms that limit the amplifier gain at low frequencies, we will neglect r_o . The reader can verify through SPICE simulation that the effect of r_o on the low-frequency amplifier gain is small. Finally, we shall also neglect r_s , which is usually much smaller than r_{π} , with which it appears in series.

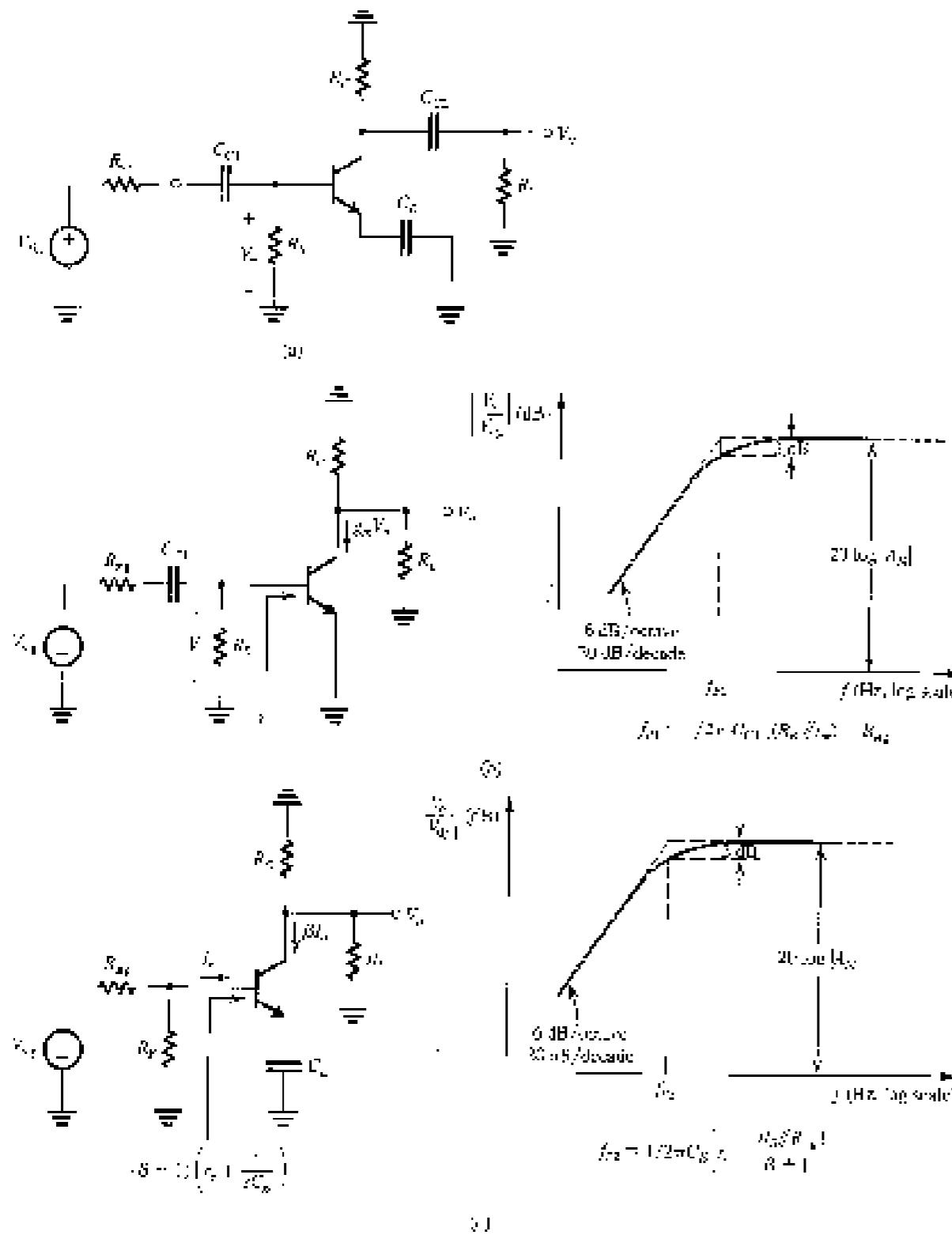


FIGURE 5.73 Analysis (a), (b), (c) low-frequency response of the CE common-emitter amplifier circuit with de coupling removed; (b) the effect of C_g is determined with C_{C1} and C_{C2} assumed to be perfect short circuits; (c) the effect of C_g is determined with C_{C1} and C_{C2} assumed to be perfect short circuits.

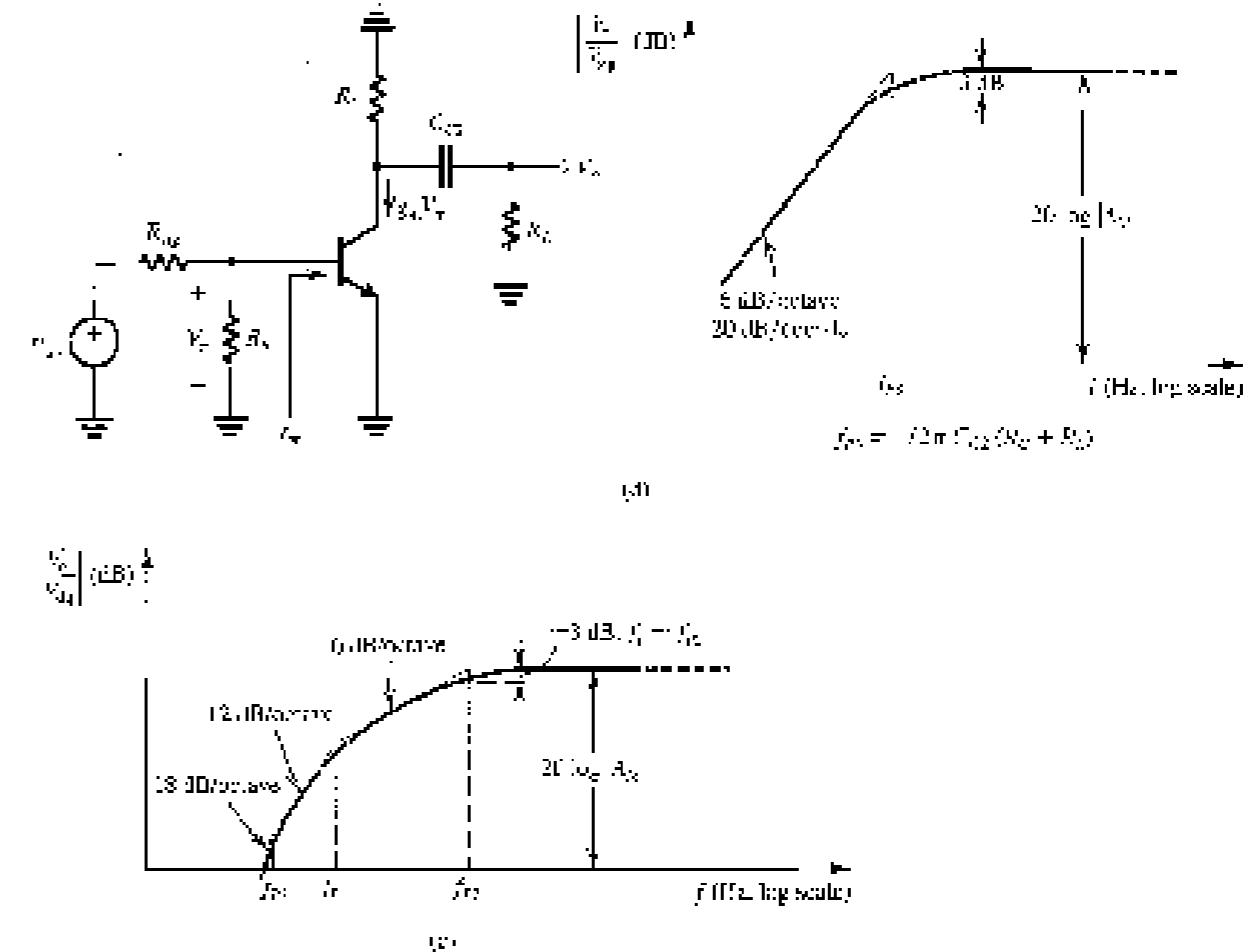


FIGURE 5.74 (a) without C_g ; (b) the effect of C_g is determined with C_{C1} and C_{C2} assumed to be perfect short circuits; (c) the effect of C_g is determined with C_{C1} and C_{C2} assumed to be perfect short circuits; note that C_{C1} , C_{C2} , and C_g do not interact and that their break-off (pole) frequencies are widely separated.

Our first cut at the analysis of the circuit in Fig. 5.72(a) is to consider the effect of the three capacitances C_{C1} , C_{C2} , and C_g one at a time. That is, when finding the effect of C_{C1} , we shall assume that C_g and C_{C2} are acting as perfect short circuits, and when considering C_g , we assume that C_{C1} and C_{C2} are perfect short circuits, and so on. This is obviously a major simplifying assumption—and one that might not be justified. However, it should serve as a first cut at the analysis enabling us to gain insight into the effect of these capacitances.

Figure 5.73(b) shows the circuit with C_g and C_{C2} replaced with short circuits. The voltage V_b at the base of the transistor can be written as

$$V_b = V_{in} \frac{R_b \parallel r_{be}}{(R_b \parallel r_{be}) + R_{eq} + \frac{1}{sC_{C1}}}$$

and the output voltage is obtained as

$$V_o = -K_A V_b (R_L \parallel R_{eq})$$

These two equations can be combined to obtain the voltage gain V_o/V_{in} including the effect of C_{x1} as

$$\frac{V_o}{V_{in}} = -\frac{(R_s \parallel r_e)}{(R_a + r_e) + R_{x1}} \frac{1}{s + \frac{1}{C_{x1}(R_a \parallel r_e) + R_{x1}}} \quad (5.77)$$

from which we observe that the effect of C_{x1} is to introduce the frequency-dependent factor between the square brackets on the right-hand side of Eq. (5.77). We recognize this factor as the transfer function of a single-Low-constant (SLC) network of the high-pass type (see Section 1.6 and Appendix D) with a corner (or break) frequency ω_{p1} :

$$\omega_{p1} = \frac{1}{C_{x1}(R_a \parallel r_e) + R_{x1}} \quad (5.78)$$

Note that $(R_a \parallel r_e) + R_{x1}$ is the resistance seen between the terminals of C_{x1} when V_{in} is set to zero. The SLC high-pass factor introduced by C_{x1} will cause the amplifier gain to roll off at low frequencies at the rate of 6 dB/octave (20 dB/decade) with a 3-dB frequency at $f_{p1} = \omega_{p1}/2\pi$, as indicated in Fig. 5.72(b).

Next, we consider the effect of C_2 . For this purpose we assume that C_x and C_{x2} are acting as perfect short circuits and thus obtain the circuit in Fig. 5.73(c). Referring r_x and C_x into the base circuit and utilizing Thevenin theorem enables us to obtain the base current as

$$I_b = V_{in} \frac{R_s}{R_s + R_{x2} \parallel (R_a + R_{x1}) + (\beta + 1)(r_e + \frac{1}{sC_{x2}})}$$

The collector current can then be fixed as βI_b , and the output voltage as

$$\begin{aligned} V_o &= -\beta I_b (R_s \parallel R_a) \\ &= -\frac{R_s}{R_s + R_{x2} \parallel (R_a + R_{x1}) + (\beta + 1)(r_e + \frac{1}{sC_{x2}})} V_{in} \end{aligned}$$

Thus the voltage gain including the effect of C_x can be expressed as

$$\frac{V_o}{V_{in}} = \frac{R_s}{R_s + R_{x2} \parallel (R_a + R_{x1}) + (\beta + 1)r_e} \frac{s}{s + \frac{1}{C_{x2}(r_e + \frac{1}{sC_{x2}})}} \quad (5.79)$$

We observe that C_x introduces the SLC high-pass factor on the extreme right-hand side. Thus C_x causes the gain to fall off at low frequency at the rate of 6 dB/octave with a 3-dB frequency equal to the corner (or break) frequency of the high-pass SLC factor; that is,

$$\omega_{p2} = \frac{1}{C_x(r_e + \frac{1}{sC_{x2}})} \quad (5.80)$$

Observe that $[r_e + (R_a \parallel R_{x1})/(\beta + 1)]$ is the resistance seen between the two terminals of C_x when V_{in} is set to zero. The effect of C_x on the amplifier frequency response is illustrated by the sketch in Fig. 5.73(d).

Finally, we consider the effect of C_{x2} . The circuit with C_x and C_{x2} assumed to be acting as perfect short circuits is shown in Fig. 5.73(e), for which we can write

$$V_o = V_{in} \frac{R_s}{(R_s + r_e) + R_{x2}}$$

and

$$V_o = -\beta I_b \frac{R_s}{R_s + \frac{1}{sC_{x2}} + R_a} \quad (5.81)$$

These two equations can be combined to obtain the low-frequency gain including the effect of C_{x2} as

$$\frac{V_o}{V_{in}} = \frac{R_s}{(R_s + r_e) + R_{x2}} \frac{\beta(sR_s \parallel R_a)}{s + \frac{1}{C_{x2}(R_s + R_{x2})}} \quad (5.82)$$

We observe that C_{x2} introduces the frequency-dependent factor between the square brackets, which we recognize as the transfer function of a high-pass SLC network with a break frequency ω_{p2} :

$$\omega_{p2} = \frac{1}{C_{x2}(R_s + R_{x2})} \quad (5.83)$$

Here we note that as expected, $(R_s + R_{x2})$ is the resistance seen between the terminals of C_{x2} when V_{in} is set to zero. Thus capacitor C_{x2} causes the low-frequency gain of the amplifier to decrease at the rate of 6 dB/octave with a 3-dB frequency $f_{p2} = \omega_{p2}/2\pi$, as illustrated by the sketch in Fig. 5.73(f).

Now that we have determined the effects of each of C_{x1} , C_x , and C_{x2} acting alone, the question remains what will happen when all three are present at the same time. This question has two parts: First, what happens when all three capacitors are present but do not interact? The answer is that the amplifier low-frequency gain can be expressed as

$$\frac{V_o}{V_{in}} = A_{in} \left(\frac{s}{s + \omega_{p1}} \right) \left(\frac{s}{s + \omega_{p2}} \right) \left(\frac{s}{s + \omega_{p3}} \right) \quad (5.84)$$

from which we see that it acquires three break frequencies at ω_{p1} , ω_{p2} , and ω_{p3} , all in the low-frequency band. If the three frequencies are widely separated, their effects will be distinct, as indicated by the sketch in Fig. 5.73(g). The important point to note here is that the 3-dB frequency f_p is determined by the highest of the three break frequencies. This is usually the break frequency caused by the bypass capacitor C_x , simply because the resistance R_{x2} is usually quite small. Thus, even if one uses a large value for C_x , f_p is usually the highest of the three break frequencies.

If ω_{p1} , ω_{p2} , and ω_{p3} are close together, none of the three dominates, and to determine f_p , we have to evaluate V_o/V_{in} in Eq. (5.84) and calculate the frequency at which it drops to $|A_{in}|/2$. The work involved in doing this, however, is usually too great and is rarely justified in practice, particularly because in any case, Eq. (5.84) is an approximation based on the assumption that the three capacitors do not interact. This leads to the second part of the question: What happens when all three capacitors are present and interact? We do know that C_{x1} and C_x usually interact and that their combined effect is two poles at frequencies that will differ somewhat from ω_{p1} and ω_{p2} . Of course, one can derive the overall transfer function taking this interaction into account and find more precisely the low-frequency response. This, however, will be too complicated to yield additional insight. As an alternative, for hand

calculations we can obtain a reasonably good estimate for f_2 using the following formula, which we will now derive here:¹

$$f_2 = \frac{1}{2\pi C_{\text{in}} R_{\text{in}}} + \frac{1}{C_{\text{p}} R_{\text{p}}} + \frac{1}{C_{\text{c2}} R_{\text{c2}}} \quad (5.184)$$

or equivalently,

$$f_2 = f_b + f_{R_p} + f_{R_{\text{c2}}} \quad (5.185)$$

where R_{in} , R_{p} , and R_{c2} are the resistances seen by C_{in} , C_{p} , and C_{c2} , respectively, when V_{in} is set to zero and the other two capacitors are replaced with short circuits. Equations (5.184) and (5.185) provide insight regarding the relative contributions of the three capacitors to f_2 . Thus, we note that a far more precise determination of the low-frequency gain and the 3-dB frequency f_2 can be obtained using SPICE (Section 5.11).

Selecting Values for C_{in} , C_{p} , and C_{c2} . We now address the design issue of selecting appropriate values for C_{in} , C_{p} , and C_{c2} . The design objective is to place the lower 1-dB frequency f_2 at a specified location while minimizing the component values. Since as mentioned above C_{in} usually sees the lowest of the three resistances, its total capacitance is minimized by selecting C_{in} so that its contribution to f_2 is dominant. That is, by relevance to Eq. (5.185), we may select C_{in} such that $1/(C_{\text{in}} R_{\text{in}})$ is, say, 80% of $\omega_2 = 2\pi f_2$, leaving each of the other capacitors to contribute 10% to the value of ω_2 . Example 5.19 should help to illustrate this process.

We wish to select appropriate values for C_{in} , C_{p} , and C_{c2} for the common-emitter amplifier whose low-frequency response was analyzed in Example 5.18. The amplifier has $R_{\text{b}} = 100\text{k}\Omega$, $R_{\text{c}} = 8\text{k}\Omega$, $R_{\text{L}} = 5\text{k}\Omega$, $A_{\text{v}} = -20$, $\beta_0 = 100$, $v_A = 20\text{mV/V}$, and $r_s = 2.5\text{M}\Omega$. It is required to have $f_2 = 100\text{Hz}$.

Solution

We first determine the resistances seen by the three capacitors C_{in} , C_{p} , and C_{c2} as follows:

$$\begin{aligned} R_{\text{in}} &= (\beta_0 r_s / v_A) + R_{\text{c}} \\ &\approx (100 \times 2.5) + 5 = 7.5\text{k}\Omega \end{aligned}$$

$$\begin{aligned} R_{\text{p}} &= r_s = \frac{\beta_0}{\beta_0 + 1} R_{\text{c}} \\ &= 0.05 \times \frac{100 \times 5}{100 + 1} = 0.05\text{k}\Omega = 500\text{ }\Omega \end{aligned}$$

$$R_{\text{c2}} = R_{\text{c}} + R_{\text{L}} = 5 + 5 = 10\text{k}\Omega$$

Now, selecting C_{in} so that it contributes 80% of the value of ω_2 gives

$$\begin{aligned} \frac{1}{C_{\text{in}} R_{\text{in}}} &= 0.8 \times 2\pi \times 100 \\ C_{\text{in}} &= 2.5\text{nF} \end{aligned}$$

¹ For the interested reader can refer to Chapter 7 of the fourth edition of this book.

Next, if C_{p} is to contribute 10% of ω_2 ,

$$\begin{aligned} \frac{1}{C_{\text{p}} R_{\text{p}}} &= 0.1 \times 2\pi \times 100 \\ C_{\text{p}} &= 2.5\text{nF} \end{aligned}$$

Similarly, if C_{c2} is to contribute 10% of ω_2 , its value should be selected as follows:

$$\begin{aligned} \frac{1}{C_{\text{c2}} R_{\text{c2}}} &= 0.1 \times 2\pi \times 100 \\ C_{\text{c2}} &= 2.5\text{nF} \end{aligned}$$

In practice, we would select the nearest standard values for the three capacitors while ensuring that $f_2 \leq 100\text{Hz}$.

EXERCISE

5.82 A common-emitter amplifier has $C_{\text{in}} = 10\text{pF}$, $R_{\text{b}} = 100\text{k}\Omega$, $R_{\text{c}} = 8\text{k}\Omega$, $R_{\text{L}} = 5\text{k}\Omega$, $\beta_0 = 100$, $r_s = 2.5\text{M}\Omega$, and $A_{\text{v}} = -20$. Determine the required values of C_{p} and C_{c2} to achieve a 3-dB frequency of $f_2 = 100\text{Hz}$.

5.8.4 A Final Remark

The frequency response of the other amplifier configurations will be studied in Chapter 6.

5.10 THE BASIC BJT DIGITAL LOGIC INVERTER

The most fundamental component of a digital system is the logic inverter. In Section 1.1, the logic inverter was studied at a conceptual level, and the realization of the inverter using voltage-controlled switches was presented. Having studied the BJT, we can now consider its application in the realization of a simple logic inverter. Such a circuit is shown in Fig. 5.74. The reader will note that we have already studied this circuit in some detail. In fact, we used it in Section 5.3.4 to illustrate the operation of the BJT as a switch. The operation of the circuit as a

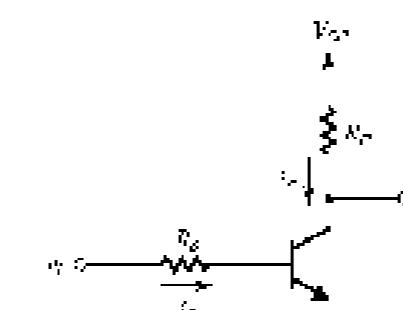


FIGURE 5.74 Basic BJT digital logic inverter.

logic inverter makes use of three off and saturation modes. In very simple terms, if the input voltage v_i is "high," at a value close to the power-supply voltage V_{CC} , representing a logic "1" in a positive-logic system, the transistor will be conducting and, with appropriate choice of values for R_1 and R_2 , saturated. Then the output voltage will be $V_{DD} \approx 0.2$ V, representing a "low" logic level in logic 0 in a positive-logic system. Conversely, if the input voltage is "low," at a value close to ground (e.g., $V_{DD}/2$), then the transistor will be cut off, i_c will be zero, and $v_o = V_{DD}$, which is "high" in logic 1.

The choice of cutoff and saturation as the two modes of operation of the BJT in the inverter circuit is motivated by the following two factors:

1. The power dissipation in the circuit is relatively low in both cutoff and saturation; In cutoff all currents are zero except for very small leakage current i_b , and in saturation the voltage across the transistor is very small (V_{CE}).
2. The output voltage levels (V_{DD} and $V_{DD}/2$) are well defined. In contrast, if the transistor is operated in the active region, $v_o = V_{DD} - i_c R_2 = V_{DD} / (1 + \beta)$, which is slightly dependent on the rather ill-controlled transistor parameter β .

5.10.1 The Voltage Transfer Characteristic

As mentioned in Section 1.7, the most useful characterization of an inverter circuit is in terms of its voltage transfer characteristic, v_o versus v_i . A sketch of the voltage transfer characteristic (VTC) of the inverter circuit of Fig. 5.74 is presented in Fig. 5.75. The transfer characteristic is approximated by three straight-line segments corresponding to the operation of the BJT in the cutoff, active, and saturation regions, as indicated. The actual transfer characteristic will obviously be a smooth curve but will closely follow the straight-line segments indicated. We shall now compute the coordinates of the breakpoints of the transis-

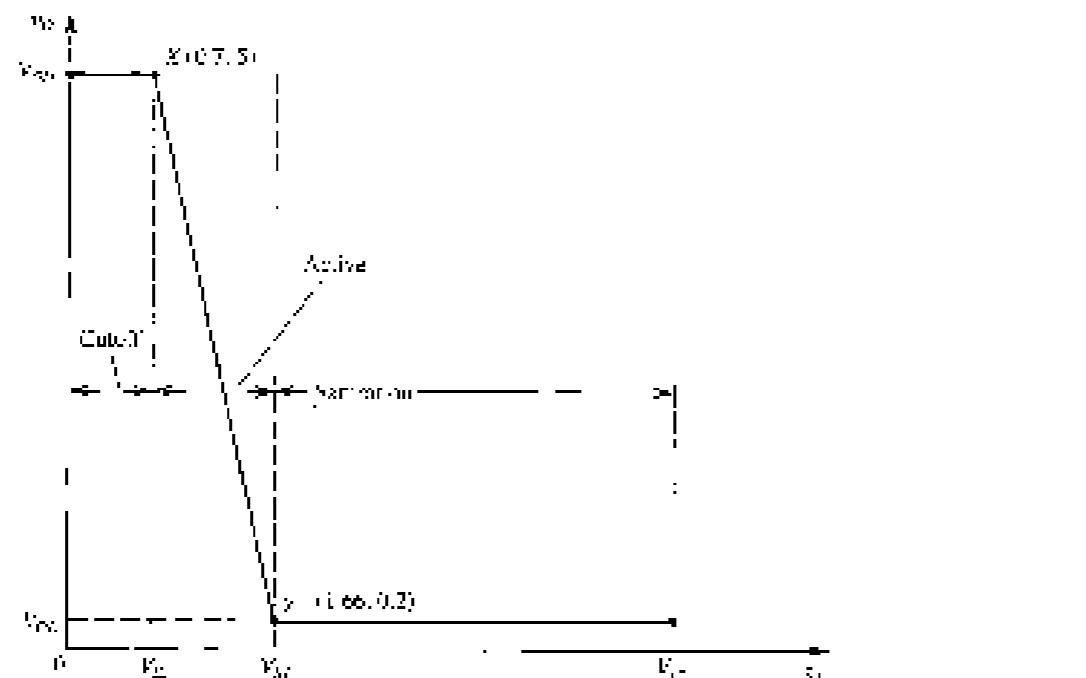


FIGURE 5.75 Sketch of the voltage transfer characteristic of the inverter circuit of Fig. 5.74 for the case $R_1 = 10\text{ k}\Omega$, $R_2 = 1\text{ k}\Omega$, $\beta = 50$, and $V_{CC} = 5\text{ V}$. For the calculation of the active region of v_o , see Fig. 5.76.

characteristic of Fig. 5.75 for a representative case— $R_1 = 10\text{ k}\Omega$, $R_2 = 1\text{ k}\Omega$, $\beta = 50$, and $V_{CC} = 5\text{ V}$ —as follows:

1. At $v_i = V_{D1} = V_{CE(sat)} = 0.2$ V, $i_b = V_{CE} - V_{BE} = 5\text{ V}$,
2. At $v_i = V_{D2}$, the transistor begins to turn on; thus,

$$V_{D2} \approx 0.7\text{ V}$$

3. For $V_{D1} < v_i < V_{D2}$, the transistor is in the active region. It operates as an amplifier whose small-signal gain is

$$A_v = \frac{v_o}{v_i} = -\beta \frac{R_2}{R_1 + r_e}$$

The gain depends on the value of r_e , which, in turn, is determined by the collector current and, in turn, by the value of v_i . As the current through the transistor increases, r_e decreases and we can neglect r_e relative to R_1 , thus simplifying the gain expression to

$$A_v = -\beta \frac{R_2}{R_1} = -50 \times \frac{1}{10} = -5\text{ V/V}$$

4. At $v_i = V_{D2}$, the transistor enters the saturation region. Thus V_{D2} is the value of v_i that results in the transistor being in the edge of saturation.

$$i_b = \frac{(V_{CC} - V_{CE(sat)})/R_2}{\beta}$$

For the values we are using, we obtain $i_b = 0.006\text{ mA}$, which can be used to find V_{D2} :

$$V_{D2} = i_b R_2 + V_{BE} \approx 1.66\text{ V}$$

5. At $v_i = V_{D2} = 0.7\text{ V}$, the transistor will be deep in saturation with $v_o = V_{DD(sat)} = 0.2\text{ V}$, and

$$\begin{aligned} \beta_{sat} &= \frac{(V_{CC} - V_{CE(sat)})/R_2}{(V_{DD} - V_{D2})/R_1} \\ &= \frac{50}{0.13} = 11 \end{aligned}$$

6. The noise margins can now be computed using the formulas from Section 1.7,

$$NM_T = V_{DD} - V_{D2} - V_{BE} = 5 - 1.66 - 0.7 = 3.64\text{ V}$$

$$NM_L = V_{D2} - V_{DD} = 0.7 - 0.2 = 0.5\text{ V}$$

Obviously, the two noise margins are vastly different making this inverter less than ideal.

7. The gain in the transition region can be computed from the coordinates of the breakpoints X and Y.

$$\text{Voltage gain} = \frac{Y - 0.2}{X - 0.7} = -5\text{ V/V}$$

which is equal to the approximate value found above (the two numbers are exactly the same value is a coincidence).

5.10.2 Saturated Versus Nonsaturated BJT Digital Circuits

The inverter circuit just discussed belongs to the saturated variety of BJT digital circuits. A historically significant family of saturated BJT logic circuits is transistor-transistor logic



FIGURE 5.76 The minority-carrier charge stored in the well-known saturation model is divided into two components: that in blue produces the gradient that gives rise to the diffusion current across the base, and that in gray results from using the transistor's deep-injection mechanism.

(TTL). Although some versions of TTL remain in use, integrated bipolar digital circuits generally are no longer the technology of choice in digital system design. This is because their speed of operation is severely limited by the relatively long turn-on delay required to turn off a saturated transistor, as we will now explain briefly.

In our study of BJT saturation in Section 5.1.5, we made use of the minority-carrier distribution in the base region (see Fig. 5.10). Such a distribution is shown in Fig. 5.76, where the minority-carrier charge stored in the base has been divided into two components: The component represented by the blue triangle produces the gradient that gives rise to the diffusion current across the base; the other component, represented by the gray rectangle, causes the transistor to be driven deeper into saturation. The deeper the transistor is driven into saturation (i.e., the greater is the base overdrive factor), the greater the amount of the "gray" component of the stored charge will be. It is this "extra" stored base charge that represents a serious problem when it comes to turning off the transistor. Before the collector current can begin to decrease, all of the extra stored charge must first be removed. This adds a relatively large component to the turn-off time of a saturated transistor.

From the above we conclude that to achieve high operating speeds, the BJT should not be allowed to saturate. This is the case in current-mode logic (CML), and for the particular form called emitter coupled logic (ECL), which will be studied briefly in Chapter 11. There, we will show why ECL is currently the highest-speed logic-circuit family available. It is based on the current-switching mechanism that was discussed conceptually in Section 1.7 (Fig. 1.33).

EXERCISE

- 5.33 Consider the circuit of Fig. 5.71 when the input voltage is increased to the input threshold voltage. The output voltage increases to the output level V_{out} . What is the differential voltage dependent on the input voltage? The output voltage is given by $V_{out} = V_{DD} - R_o \cdot I_{CQ}$. The output current is given by $I_{CQ} = \frac{V_{DD} - V_{out}}{R_o + R_s}$. The differential voltage is given by $\Delta V_{out} = \frac{\partial V_{out}}{\partial V_{in}}$.

To do this calculation, use the input-output values of the example circuit discussed earlier (i.e., $R_o = 10\text{ k}\Omega$, $R_s = 1\text{ k}\Omega$, $V_{DD} = 5\text{ V}$, $V_{out} = 3\text{ V}$). Note that the input-output capacitance, which determines the TTF, is not used here, as it is not relevant for this exercise.

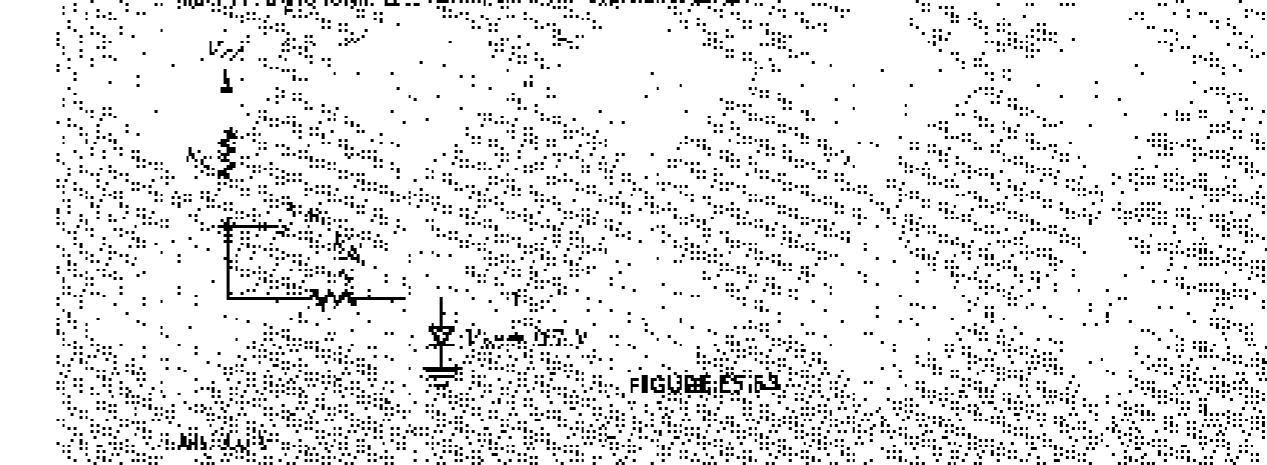


FIGURE 5.78

5.11 THE SPICE BJT MODEL AND SIMULATION EXAMPLES

As we did in Chapter 4 for the MOSFET, we conclude this chapter with a discussion of the models that SPICE uses to simulate the BJT. We will also illustrate the use of SPICE in computing the dependence of β on the bias current and in simulating a CB amplifier.

5.11.1 The SPICE Ebers-Moll Model of the BJT

In Section 5.1.4, we studied the Ebers-Moll model of the BJT and showed a form of this model, known as the injection form, in Fig. 5.8. SPICE uses an equivalent form of the Ebers-Moll model, known as the current-form, which is shown in Fig. 5.77. Here, the currents of

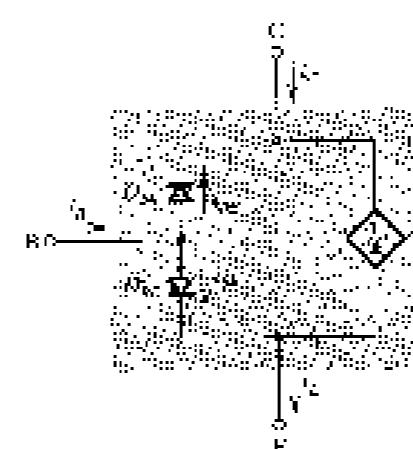


FIGURE 5.77 The current-form of the Ebers-Moll model for a BJT.

the base-emitter diode (D_{BE}) and the base-collector diode (D_{BC}), are given, respectively, by

$$i_{BE} = \frac{i_b}{\beta_0} (e^{v_{BE}/V_T} - 1) \quad (5.18a)$$

and

$$i_{BC} = \frac{i_b}{\beta_0} (e^{v_{BC}/V_T} - 1) \quad (5.18b)$$

where α_F and α_B are the emission coefficients of the BEJ and BCJ, respectively. These coefficients are generalizations of the generation of the p-n junction diode. (We have so far assumed $\alpha_F = \alpha_B = 1$. The controlled current-source i_{DS} in the transport model is referred as

$$i_{DS} = i_b (e^{\gamma_{DS} v_{BE}/V_T} - e^{\gamma_{DS} v_{BC}/V_T}) \quad (5.18c)$$

Observe that i_{DS} represents the carrier component of i_b and i_b that arises as a result of the minority carrier diffusion across the base, or carrier transport across the base (hence the name transport model). The reader can easily show that, for $\alpha_F = \alpha_B = 1$, the relations

$$i_C = i_{DS} + i_{BE} \quad (5.18d)$$

$$i_E = i_{DS} + i_{BC} \quad (5.18e)$$

$$i_B = i_C - i_E \quad (5.18f)$$

The D-T currents in the transport model result in expressions identical to those derived in Eqs. (5.23), (5.26), and (5.27), respectively. Thus, the transport form (Fig. 5.77) of the Ebers-Moll model is exactly equivalent to its injection form (Fig. 5.26). Moreover, it has the advantage of being simpler, requiring only a single controlled source from collector to emitter. Hence, it is preferred for computer simulation.

The transport model can account for the Burly effect (studied in Section 5.2.3) in a forward-biased BJT by including the factor $(1 - v_{BE}/V_A)$ in the expression for the anode current i_{DS} , as follows:

$$i_{DS} = I_b (e^{\gamma_{DS} v_{BE}/V_T} - e^{\gamma_{DS} v_{BC}/V_T}) (1 - \frac{v_{BE}}{V_A}) \quad (5.19)$$

Figure 5.78 shows the large-signal Ebers-Moll BJT model used in SPICE. It is based on the transport form of the Ebers-Moll model shown in Fig. 5.77. Here, resistors r_B , r_C , and r_E are added to represent the reverse bias areas of, respectively, the base, emitter, and collector regions. The dynamic operation of the BJT is modeled by two non-linear capacitors, C_{BE} and C_{BC} . Each of these capacitors generally includes a diffusion component (i.e., C_{BE} and C_{BC} include depletion or junction capacitance C_J and C_{JS}) to account for the charge-storage effects within the BJT (as described in Section 5.8). Furthermore, the BJT model includes a depletion junction capacitance C_{DS} to account for the collector-substrate junction in integrated-circuit BJTs, where a reverse-biased p-n junction is formed between the collector and the substrate (which is common to all components of the IC).

For small-signal (ac) analysis, the SPICE BJT model is equivalent to the hybrid π model of Fig. 5.67, but augmented with r_B , r_C , and r_E (C-BJT's C_{DS} furthermore). The

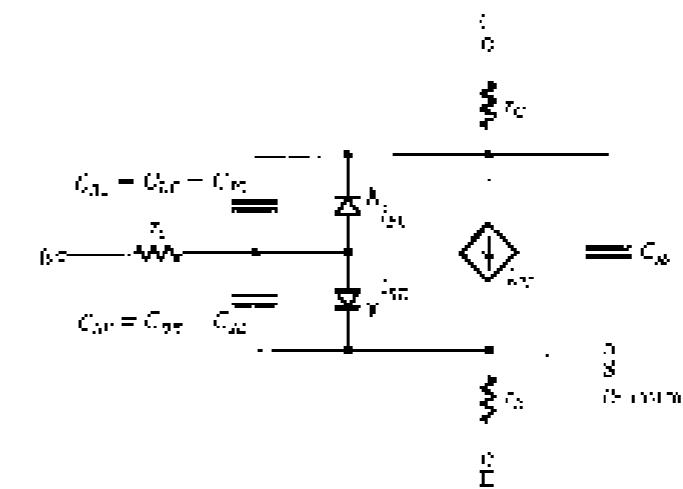


FIGURE 5.78 The SPICE large-signal Ebers-Moll model for n-p-n BJT.

model includes a large resistance r_C between the base and collector (in parallel with C_{BE}) to account for the dependence of i_C on v_{CE} . This dependence can be noted from the CB characteristics of the BJT in Fig. 5.13(b), where i_C is observed to increase with v_{CE} . Since each i_C - v_{CE} curve in Fig. 5.13(b) is measured at a constant i_B , an increase in i_C with v_{CE} implies a corresponding decrease in i_B with v_{CE} . The resistance r_C is very large, typically greater than $10^3 \Omega$.

Although Fig. 5.77 shows the SPICE model for the npn BJT, the corresponding model for the pnp BJT can be obtained by reversing the direction of the currents and the polarity of the diodes and terminal voltages.

5.11.2 The SPICE Gummel-Poon Model of the BJT

The large-signal Ebers-Moll BJT model described in Section 5.11.1 lacks a representation of some second-order effects present in actual devices. One of the more important such effects is the variation of the current gains, β_0 and β_F , with the current i_b . The Ebers-Moll model assumes β_0 and β_F to be constant, thereby neglecting their current dependence (as depicted in Fig. 5.27). To account for this, and other second-order effects, SPICE uses a more complete, yet more complex, BJT model called the Gummel-Poon model, named after Gummel and Poon, two pioneers in this field. This model is based on the relationship between the electrical terminal characteristics of a BJT and its base charge. It is beyond the scope of this book to delve into the model's details. However, it is important for the reader to be aware of the existence of such a model.

In SPICE, the Gummel-Poon model automatically simplifies to the Ebers-Moll model when certain model parameters are not specified. Consequently, the BJT model to be used by SPICE need not be explicitly specified by the user (unlike the MOSFET case in which the model is specified by the LEVEL parameter), but discrete BJTs, the values of the SPICE model parameters can be determined from the data specified on the BJT data sheets, supplemented (if needed) by key measurements. For instance, in Example 5.26 (Section 5.1.4), we will use the QM3504 npn BJT (from Fairchild Semiconductor) w/ a SPICE model in

available in PSpice. In fact, the PSpice library includes the SPICE model parameters for many of the commercially available discrete BJTs. For I_C BJTs, the values of the SPICE model parameters are determined by the IC manufacturer (using both measurements on the fabricated devices and knowledge of the details of the fabrication process) and are provided to the IC designers.

5.11.3 The SPICE BJT Model Parameters

Table 5.8 provides a listing of some of the BJT model parameters used in SPICE. The reader should be already familiar with these parameters. In the absence of a user-specified value for a particular parameter, SPICE uses a default value that typically results in the corresponding effect being ignored. For example, if no value is specified for the forward Early voltage V_{AF}, SPICE assumes that V_{AF} = ∞ and does not account for the Early effect. Although ignoring the forward Early voltage V_{AF} can be a serious issue in some circuits, the same is not true, for example, for the value of the reverse Early voltage V_{AR}.

5.11.4 The BJT Model Parameters BF and BR in SPICE

Before leaving the SPICE model, a comment on β is in order. SPICE interprets the user-specified model parameters BF and BR as the *absolute maximum* values of the forward and reverse dc current gains, respectively, versus the operating current. These parameters are not equal to the

TABLE 5.8 Parameters of the SPICE BJT Model (Partial Listing)¹⁷

SPICE Parameter	Book Symbol	Description	Units
I _S	I_s	Saturation current	A
R _F		Bias modulation forward current gain	
R _R		Bias modulation reverse current gain	
A _F	a_F	Forward current emission coefficient	
A _R	a_R	Reverse saturation emission coefficient	
V _{AF}	V_{AF}	Forward Early voltage	V
V _{AR}	V_{AR}	Reverse Early voltage	V
R _H	r_h	Zero bias base-emitter resistance	Ω
R _C	r_c	Collector-emitter resistance	Ω
R _E	r_e	Emitter ohmic resistance	Ω
T _F	t_f	Ideal forward transit time	s
T _R	t_r	Ideal reverse transit time	s
C _{JC}	$C_{j_{ce}}$	Zero-bias base-collector depletion junction capacitance	F
M ₁	m_{12}	Base-collector grading coefficient	
V _{TC}	V_T	Base-collector turn-on potential	V
C _{JE}	$C_{j_{be}}$	Zero-bias base-emitter depletion junction capacitance	F
M ₂	m_{21}	Base-emitter grading coefficient	
V _{TT}	V_B	Base-emitter Miller-on potential	V
C _{JS}		Zero-bias collector substrate depletion junction capacitance	F
M ₃		Collector-to-substrate grading coefficient	
V _{BS}		Collector substrate built-in potential	V

collected current. Independent parameters β_F (β_{A_F}) and β_R exist in the Ulrich-Moll model (and throughout this chapter) for the forward and reverse dc current gains of the BJT. SPICE uses a current-dependent model for β_F and β_R , and the user can specify other parameters (not shown in Table 5.8) for this model. Only when such parameters are not specified, and the Early effect is neglected, will SPICE assume that β_F and β_R are constant and equal to BF and BR, respectively. Furthermore, SPICE computes values for both β_F and β_R ; the two parameters that we generally assume to be approximately equal. SPICE then uses β_F for our small-signal (ac) analysis.

DEPENDENCE OF β ON THE BIAS CURRENT

In this example, we use PSpice to simulate the dependence of β_F on the collector bias current for the Q2N3904 discrete BJT (from Fairchild Semiconductor) whose model parameters are listed in Table 5.9 and are available in PSpice.¹⁸ As shown in the Capture schematic¹⁹ of Fig. 5.80, the V_{CE} of the BJT is fixed using a constant voltage source (in this example, $V_{CE} = 2\text{ V}$) and a constant source I_B is applied to the base. To illustrate the dependence of β_F on the collector current I_C , we perform a dc analysis simulation in which the sweep variable is the collector current I_C . The β_F in the BJT, which corresponds to the ratio of the collector current I_C to the base current I_B , can then be plotted versus I_C using Probe (the graphical interface of PSpice), as shown in Fig. 5.80. We see that at operating at the maximum value of I_C (i.e., $I_C = 163\text{ mA}$ at $V_{CE} = 2\text{ V}$, the BJT is biased at an $I_C = 10\text{ mA}$). Since increasing the bias current also increases the power dissipation, it is clear from Fig. 5.80 that the choice of current I_C is a trade-off between the current gain β_F and the power dissipation. Generally speaking, the optimum I_C depends on the application and technology selected, but, for example, for the Q2N3904 BJT operating at $V_{CE} = 2\text{ V}$, increasing I_C by a factor of 20 (from 10 mA to 200 mA) results in a drop in β_F of about 22% (from 163 to 122).

TABLE 5.9 SPICE Model Parameters of the Q2N3904 Discrete BJT²⁰

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
T _{TF} -T _{TO17}	21.1	T _{TF} -T _{TO3}	25.5-41.0 ^b	T _{TF} -T _{TO5}	45.0	T _{TF} -T _{TO11}	78.5-101.0 ^b
T _{TR} -T _{TO17}	275-1.4	T _{TR} -T _{TO3}	40.0 ^b	T _{TR} -T _{TO5}	16.0 ^b	T _{TR} -T _{TO11}	20.0 ^b
T _{IC} -T _{TO17}	10.0-3.0 ^b	T _{IC} -T _{TO3}	10.0-7.5 ^b	T _{IC} -T _{TO5}	0.0-2.0 ^b	T _{IC} -T _{TO11}	0.0-0.7 ^b
T _{VB} -T _{TO17}	200-31.2 ^b	T _{VB} -T _{TO3}	20.0-4 ^b	T _{VB} -T _{TO5}	3.0-0 ^b	T _{VB} -T _{TO11}	1.0-0 ^b

^a The Q2N3904 model is included in the evaluation (EV_N3904) library of PSpice (Part of V2.2 Library). To obtain this, go to Tools->Get Models->From Internet->Fairchild Semiconductors.

^b The value is contained in the Capture schematic and the corresponding PSpice circuit file (one of 21 SPICE examples, and other can be found in the text's CD as well as on the website (www.fairchildsemi.com)). In these schematics (as shown in Fig. 5.76), we use variable parameters to control the values of the various device components. This allows one to investigate the effect of changing component values by simply changing the corresponding parameter values.

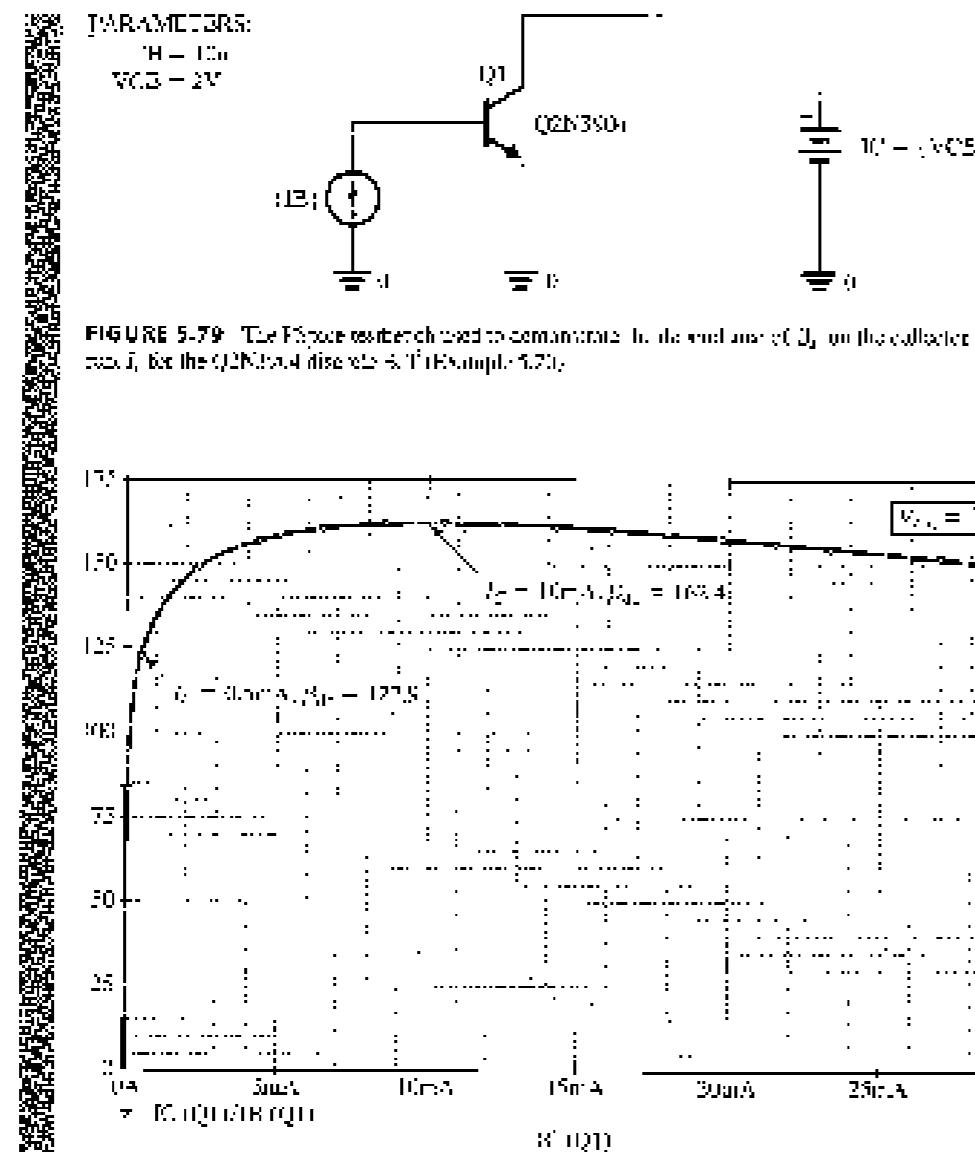


FIGURE 5.80 The variation of β_L vs. I_C for $V_B = 2\text{V}$ in the Q2N3904 diode CE amplifier (Example 5.20).

THE CE AMPLIFIER WITH Emitter RESISTANCE

In this example, we use PSpice to compute the low-frequency response of the CE amplifier and investigate its three-point stability. A capture schematic of the CE amplifier is shown in Fig. 5.81. We will use part Q2N3904 for the BJT and a $\pm 5\text{-V}$ power supply. We will also assume a signal-source resistance $R_{SS} = 10\text{k}\Omega$, a load resistor $R_L = 10\text{k}\Omega$, and bypass and coupling capacitors of

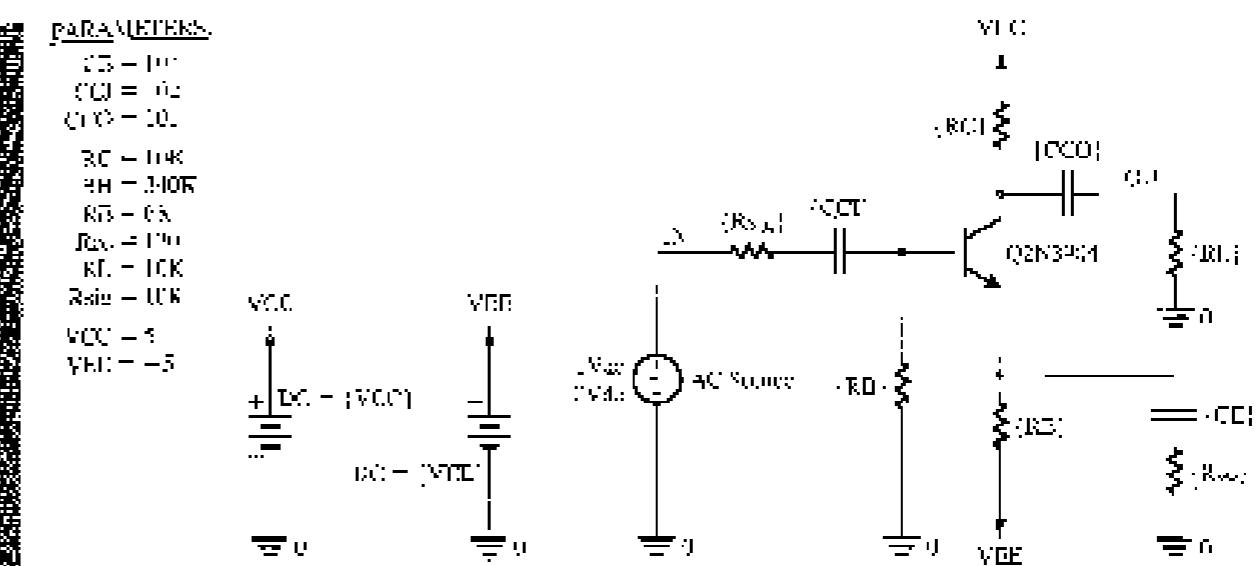


FIGURE 5.81 Capture schematic of the CE amplifier in Example 5.21.

0.5A. To enable us to investigate the effect of introducing a resistance in the signal path of the emitter, a resistor R_E is connected in series with the emitter bypass capacitor C_E . Note that the roles of R_E and R_{BE} are different. Resistor R_E is the emitter degeneration resistor because it appears in the direct path between the emitter and ground. It is therefore used to help stabilize the bias point for the amplifier. The equivalent resistance $R_E + R_{BE} + R_{SS}$ is the small-signal emitter degeneration resistance because it appears in the ac (small-signal) path between the emitter and ground and helps stabilize the gain of the amplifier. In this example, we will investigate the effects of both R_E and R_{BE} on the performance of the CE amplifier. However, as should always be the case with computer simulation, we will begin with an appropriate parallel- π -polar circuit. In this way, maximum advantage and insight can be obtained from simulation.

Based on the plot of β_L versus I_C in Fig. 5.80, a collector bias current I_C of 0.5 mA is selected for the BJT, resulting in $\beta_L = 122$. This choice of I_C is a reasonable compromise between power dissipation and current gain. Furthermore, a collector bias voltage V_{CB} of 0 V (i.e., at the mid-supply value) is selected to achieve a high signal swing at the amplifier output. For $V_{CC} = 2\text{V}$, the result is that $V_T = -2\text{V}$ requires bias resistors with values

$$R_{BE} = \frac{V_{CC} - V_T}{\beta_L} = 10\text{k}\Omega$$

and

$$R_E = \frac{V_T - V_{CE}}{\beta_L} = 6.1\text{k}\Omega$$

Assuming $V_{BB} = 0.7\text{V}$ and using $\beta_L = 122$, we can determine

$$R_{BB} = \frac{V_B}{I_C} = \frac{V_{BB} + V_T}{I_C/\beta_L} = 520\text{k}\Omega$$

Next, the formulae of Section 5.7.4 can be used to determine the input resistance R_{in} and the small-signal voltage gain $|A_{v1}|$ of the CE amplifier:

$$R_{in} = R_E \parallel (\beta_{dc} + 1) (r_o + R_E) \quad (5.193)$$

$$|A_{v1}| = \left| -\frac{R_E}{R_{in} + R_{in}} \times \frac{R_C \parallel R_L}{r_o + R_E} \right| \quad (5.194)$$

For simplicity, we will assume $\beta_{dc} \approx \beta_{ac} = 120$, resulting in

$$r_o = \sqrt{\frac{\beta_{dc}}{\beta_{dc} + 1} \frac{V_T}{I_C}} = 49.6 \text{ k}\Omega$$

Thus, with no emitter degeneration (*i.e.*, $R_E = 0$), $R_{in} = 5.1 \text{ k}\Omega$ and $|A_{v1}| = 23.3 \text{ V/V}$. Since Eq. (5.194) and assuming R_E is large enough to have a negligible effect on R_{in} , it can be shown that the emitter degeneration resistor R_E decreases the voltage gain $|A_{v1}|$ by a factor of:

$$\frac{1 + \frac{R_E}{r_o} + \frac{R_{in}}{r_o}}{1 + \frac{R_E}{r_o}}$$

Therefore, to limit the reduction in voltage gain to a factor of 2, we will select

$$R_E = r_o \times \frac{R_{in}}{R_{in} + 1} \quad (5.195)$$

Thus, $R_E = R_{in} = 130 \text{ }\Omega$. Substituting this value in Eqs. (5.193) and (5.194) shows that R_{in} increases from $5.1 \text{ k}\Omega$ to $20.9 \text{ k}\Omega$ while $|A_{v1}|$ drops from 23.3 V/V to 13.8 V/V .

We will now use SPICE to verify our design and investigate the performance of the CE amplifier. We begin by performing a bias-point simulation to verify that the BJT is properly biased in the active region and that the dc voltages and currents are within the desired specifications. Based on this simulation, we have increased the value of R_3 to $340 \text{ k}\Omega$ in order to limit I_C to about 0.5 mA , using a standard 1% resistor value (Appendix G). Next, to measure the midband gain A_{v1} and the 3-dB frequencies f_L and f_H , we apply a 1-V ac voltage at the input, perform an ac analysis simulation, and plot the output voltage magnitude (in dB) versus frequency as shown in Fig. 5.82. This corresponds to the magnitude response of the CE amplifier because we chose 1-V input signal.¹⁴ Accordingly, without emitter degeneration, the midband gain is $|A_{v1}| = 23.3 \text{ V/V} = 11.7 \text{ dB}$ and the 3-dB bandwidth is $BW = f_H - f_L = 143.7 \text{ kHz}$. Using an $R_E = 130 \text{ }\Omega$ results in a drop in the midband gain $|A_{v1}|$ by a factor of 2 (*i.e.*, 6 dB). Interestingly, however, BJT bias is reduced by approximately the same factor as the drop in $|A_{v1}|$. As we will learn in Chapter 8 when we study negative feedback, the emitter-degeneration resistor R_E provides negative feedback, which allows us to trade off gain for other desirable properties such as a larger input resistance, and a wider bandwidth.

To conclude this example, we will demonstrate the improved bias-point for dc operating-point stability achieved when an emitter resistor R_E is used (see the discussion in Section 5.5.4). Specifically, we will increase/decrease the value of the parameter BT (*i.e.*, the ideal maximum

¹⁴ The reader should not be alarmed about the use of such a large signal amplitude. Recall (Section 2.9.1) that in a small-signal (ac) circuit, SPICE first finds the small-signal equivalent circuit, i.e., the dc bias point, and then analyzes this circuit (*i.e.*, SPICE only uses $\omega = 0$) to see what is done with any ac signal amplitude. However, a 1-V ac input is convenient to use as the result of no component response in the voltage gain of the circuit.

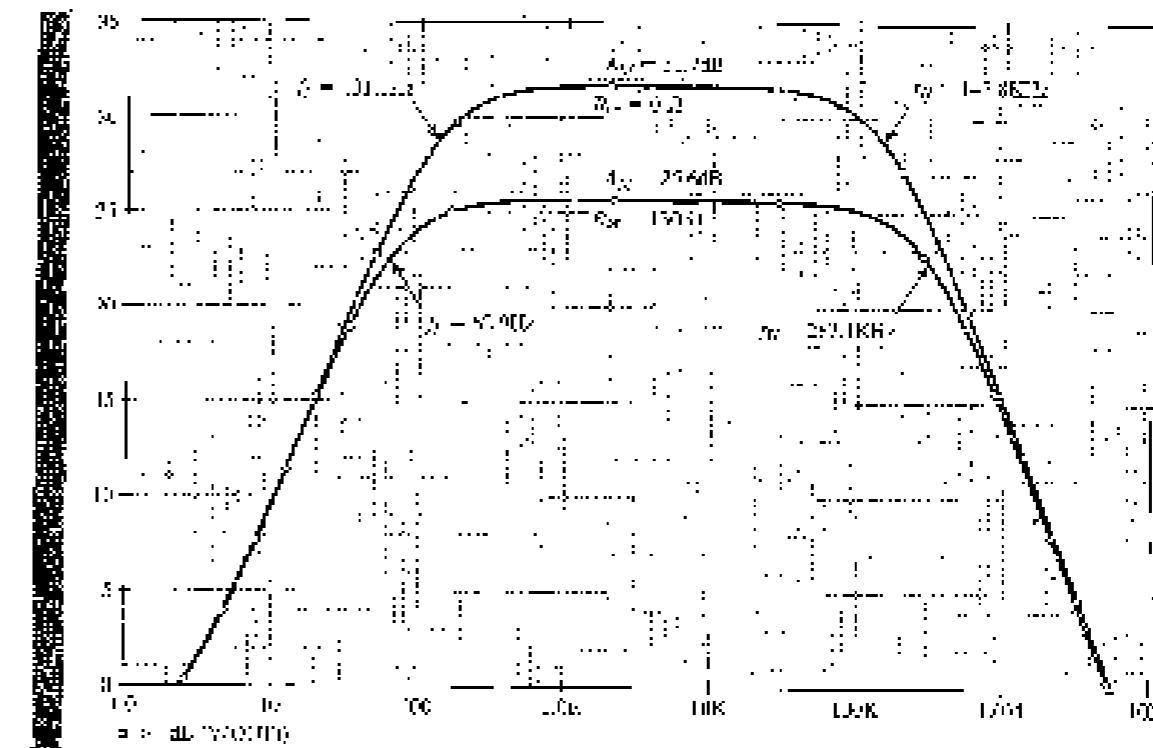


FIGURE 5.82 Frequency response of the CE amplifier in Example 5.2.1 with $R_E = 0$ and $R_E = 130 \text{ }\Omega$.

forward current g_{m0} in the SPICE model for part Q2N2904 by a factor of 2 and perform a bias-point calculation. The corresponding changes in BJT parameters (β_{dc} and β_{ac}) and bias-point (including I_C and V_{CE}) are presented in Table 5.13 for the case of $R_E = 6 \text{ k}\Omega$. Note that β_{dc} is not

TABLE 5.13 Changes in the Bias Point of the CE Amplifier in Example 5.2.1 with $R_E = 6 \text{ k}\Omega$ due to a Factor of 2 Increase in g_{m0}

BF in SPICE	$R_E = 6 \text{ k}\Omega$				$R_E = 0$			
	β_{dc}	β_{ac}	$I_C (\text{mA})$	$V_{CE} (\text{V})$	β_{dc}	β_{ac}	$I_C (\text{mA})$	$V_{CE} (\text{V})$
20%	319	519	0.452	0.484	109	35.0	0.477	1.727
40% (Continued vs. 10%)	124	123	0.395	0.402	118	122	0.264	0.161
80%	173	144	0.518	-0.53	181	151	0.588	0.971

equal to β_{dc} as we assumed, but is slightly larger. For the case without emitter degeneration, we will use $V_T = 25$ in the schematic of Fig. 5.81. Furthermore, to minimize the sum of I_C and I_{CBO} in both cases of the voltage obtained for minimum BT, we use $R_E = 1.12 \text{ M}\Omega$ to limit I_C to approximately 0.5 mA . The corresponding variations in the BJT bias point are also shown in Table 5.13. Accordingly, we see that emitter degeneration makes the bias point of the CE amplifier much less sensitive to changes in β . However, unless a large output capacitor C_O is used, this reduced bias sensitivity comes at the expense of a reduction in the midband gain (as we observed in this example when we simulated the frequency response of the CE amplifier with no $R_E = 1 \text{ V}$).

SUMMARY

- Depending on the bias conditions and its operating mode, the BJT can operate in one of four possible modes: off (breakdown between base, collector, and emitter), the FEI (forward-emitter injection), the CBI (forward-biased saturation), or reverse active (the CBI is reverse-biased and the FEI forward-biased).
- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes. The reverse-active mode of operation is also important, but less often.
- A BJT operating in the active mode provides a collector current $I_C = I_B \beta$, where the base current $I_B = I_{BE}/\alpha$, and the emitter current $I_{BE} = I_B + I_C$. Also, $\beta = \alpha/\gamma$ and thus $\beta = \alpha/(1 - \alpha)$ and $\beta = \beta/(\beta + 1)$. See Table 5.2.
- In common-emitter operation in the active mode, the collector voltage of an npn transistor must be kept higher than approximately 0.1 V below the base voltage. For a pnp transistor the collector voltage must be lower than approximately 0.4 V above the base voltage. Otherwise, the CBI becomes non-reversible, and the transistor enters the FEI regime ($I_C > 0$).
- A convenient and intuitively appealing model for the biasing and operation of the BJT is the Ebers-Moll model shown in Fig. 5.8. A trade-off in performance between its parameters is $\alpha \beta \gamma = \alpha \beta \gamma_0 = 1$. While $\alpha \beta \gamma$ is close to unity, γ_0 is very small (0.01–0.2), and β_0 is also extremely small. Use of the EBM model enables expressing the terminal currents in terms of the voltages V_{BE} and V_{CE} . The resulting relationships are given in Eqs. (5.26) and (5.48).
- In a saturated transistor, $|V_{CE(s)}| \approx 0.2$ V and $I_{CE(s)} = (V_{CE} - V_{CE(s)})/R_E$. The ratio of $I_{CE(s)}$ to the base current is the forward transconductance β . The collector-to-emitter resistance, $R_{CE(s)}$, is small (few tens of ohms).
- At a constant collector current, the magnitude of the base-to-emitter voltage decreases by about 2 mV for every 1°C rise in temperature.
- With the emitter open-circuited ($V_E = 0$), the C-E weaks toward a reverse voltage $|V_{CE(s)}|$ that is typically 500 mV. For $\beta > 1$, the breakdown voltage is less than $|BV_{CEO}|$ in the common-emitter configuration (the breakdown voltage specified is $|BV_{CEO}|$, which is about half $|BV_{CEO}|$). The emitter-base junction breakdown reverse bias of 0.4 to 0.5 V. This breakdown voltage has a positive dependence on β .
- A summary of the current-voltage characteristics and large-signal models of the BJT, with the relevant circuit models, is presented in Table 5.4.
- The dc analysis of transistor circuits is greatly simplified by assuming that $|V_{BE} \approx 0.7$ V.

and multiplication of C_b by $(1 + g_m R'_b)$, known as the Miller effect, is the most significant factor limiting the high-frequency response of the CE amplifier.

- For the analysis of the effect of C_{BE} , C_{CE} , and C_b on the low-frequency gain of the CE amplifier, refer to Section 5.9.3 and in particular to Fig. 5.73.

PROBLEMS

SECTION 5.1: DEVICE STRUCTURE AND PHYSICAL OPERATION

- 5.1** The terminal voltages of various npn transistors are measured during operation in their respective circuits with the following results:

Case No.	E	B	C	V_{BE} (mV)	V_{CE} (mV)	I_C (mA)	β (Miller)
1	0	0.1	0.1	-	-	-	-
2	0	0.8	0.1	-	-	-	-
3	-0.7	0	0.7	-	-	-	-
4	-0.7	0	-0.5	-	-	-	-
5	0.1	0.7	0	-	-	-	-
6	0.7	-2.0	0	-	-	-	-
7	0	0	5.0	-	-	-	-
8	-0.10	5.0	5.0	-	-	-	-

In this table, where the entries are in volts, β indicates the difference between the base (positive) probe of the voltmeter and V_{BE} indicated. For each case, identify the mode of operation of the transistor.

- 5.2** An npn transistor has an n – p junction of $10 \mu\text{m} \times 10 \mu\text{m}$. The doping concentration is $n = 10^{17} \text{ cm}^{-3}$ in the emitter, $N_D = 10^{15} \text{ cm}^2$ in the base, $N_A = 10^{16} \text{ cm}^2$, and in the collector $N_P = 10^{15} \text{ cm}^2$. The transistor is operating at $T = 300$ K, where $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$. For electrons diffusing in the base, $D_n = 15 \text{ } \mu\text{m}^2/\text{s}$ and $D_p = 21.2 \text{ } \mu\text{m}^2/\text{s}$. For holes diffusing in the collector, $D_p = 0.6 \text{ } \mu\text{m}^2/\text{s}$ and $D_n = 1.7 \text{ } \mu\text{m}^2/\text{s}$. Calculate β and β assuming that the base width is 75 μm .

- (a) 1.00
(b) 2.00
(c) 5.00

For case (b), $|V_C| = 1$ mV, and $I_B = I_C = V_{CE}/R_E$, and the minority carrier charge stored in the base, $(N_A V_{CE}) = N_A^2/2$. Recall that the electric charge $q = 1.6 \times 10^{-19} \text{ C}$ and $\mu = 10^{-12} \text{ C/V s}$.

- 5.3** Two transistors, fabricated with the same technology but having different carrier densities, when connected at a reverse-bias voltage of 0.15 V, have collector currents of 0.2 mA and 1.2 mA. Find I_B for each device. What are the reverse-junction areas?

- 5.4** In a particular BJT, the base current is 7.5 μA , and the collector current is 100 μA . Find β and α for this device.

- 5.5** For the values of β that correspond to α values of 0.5, 0.8, 0.9, 0.95, 0.99, 0.995, and 0.999,

- 5.6** For the values of β that correspond to β values of 1, 2, 10, 20, 100, 200, 1000, and 2000,

- 5.7** Measurement of V_{BE} and the terminal currents when β and α of an npn transistor are tabulated below. For each, calculate the missing current value as well as α , β , and γ , as indicated by the table.

Transistor No.	E	B	C	V_{BE} (mV)	V_{CE} (mV)	I_C (mA)	β	α	γ
1	0	0	0	-	-	-	-	-	-
2	0	0.8	0.1	-	-	-	-	-	-
3	-0.7	0	0.7	-	-	-	-	-	-
4	-0.7	0	-0.5	-	-	-	-	-	-
5	0.1	0.7	0	-	-	-	-	-	-
6	0.7	-2.0	0	-	-	-	-	-	-
7	0	0	5.0	-	-	-	-	-	-
8	-0.10	5.0	5.0	-	-	-	-	-	-

- 5.8** Consider an npn transistor whose base-emitter drop is 0.76 V at a collector current of 10 mA. What current will it conduct if $V_{BE} = 0.70$ V? What is its base-emitter voltage for $I_C = 10$ μA ?

- 5.9** Show that for a transistor with α close to unity, β changes by a small per unit change in α when α changes per unit change in β given approximately by

$$\frac{\delta \beta}{\beta} \approx \beta \left(\frac{\Delta \alpha}{\alpha} \right)$$

- 5.10** An npn transistor of a type whose β is specified to range from 60 to 300 is connected in a circuit with source grounded, collector at 10 V, and a load of $100 \text{ }\mu\text{A}$ generated from the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor? (Note: Perhaps you can see why this is a bad way to establish the operating condition in the collector of a BJT.)

- 5.11** A particular BJT when operating in the active mode with a collector current of 10 mA is known to have $V_{BE} = 0.70$ V and $\beta = 100 \mu\text{A}$. Use these data to create specific transistor models of the form shown in Figs. 5.5(a) and (b).

5.12 Using the large-signal model of Fig. 5.5(c), consider the case of a transistor for which the base is connected to ground, the collector is connected to a 10-V dc source, it has a 3-kΩ resistor, and a 2-mA current source is connected to the emitter with the polarity so that current is drawn out of the emitter terminal. If $\beta = 100$ and $i_b = 10^{-12}$ A, find the voltages at the emitter and the collector if you忽略 the base current.

5.13 Consider an npn transistor for which $\beta_0 = 100$, $\alpha_0 = 0.1$, and $I_0 = 10^{-12}$ A.

- (a) If the transistor is operated in the forward-active mode with $I_b = 10 \mu\text{A}$ and $V_{ce} = 1$ V, find V_{be} , i_c , and I_0 .
 (b) Now, operate the transistor in the reverse mode, where with a forward-bias voltage V_b equal to the value of V_{ce} from (a) and with $V_{cb} = 1$ V. Find I_b , I_0 , and I_c .

5.14 A transistor characterized by the Ebers-Moll model shown in Fig. 5.8 is operated with both emitter and collector grounded and a base current of 1 mA. If the collector-junction is 10 times larger than the emitter junction and $\alpha_0 = 1$, find V_{ce} and i_c .

5.15 (a) Use the Ebers-Moll expressions in Eqs. (5.20) and (5.21) to show that the i_c - v_{be} relationship indicated in Fig. 5.9 can be described by

$$i_c = \alpha_0 i_b + \beta \frac{1}{\beta_0} - \alpha_0 \frac{v_{be}}{\beta_0} > 0$$

(b) Calculate and sketch i_c - v_{be} curves for a transistor for which $I_0 = 10^{-12}$ A, $\alpha_0 = 1$, and $\beta_0 = 100$. Use the graphs for $I_b = 0$, 0.5 mA, and 1 mA. Do this for the values of β and α_0 for which (a) $i_c = 0.501 I_b$, and (b) $i_c = 0$.

5.16 Consider the pnp large-signal model of Fig. 5.12 applied to a transistor having $I_0 = 10^{-12}$ A and $\beta = 20$. If the

emitter is connected to ground, the base is connected to a current source that yields 20 μA out of the base terminal, and the collector is connected to a negative supply of -10 V via a 10-kΩ resistor, find the collector voltage, the emitter current, and the base voltage.

5.17 A pnp transistor has $\beta_0 = 0.8$ and a saturation current of 1 A. What do you expect i_c to be if $i_b = 10 \text{ mA}$? If $\beta_0 = 5$ A?

5.18 A pnp transistor modeled with the circuit in Fig. 5.12 is connected with its base at ground, collector at -1.5 V, and a 200-Ω current is injected into its emitter. It is said to have $\beta = 10$; what are its base and collector voltages? In which direction does i_c flow? If $I_b = 10^{-12}$ A, what voltage results in the emitter? What does the collector current become if a transistor with $\beta = 100$ is substituted? (Note: The fact that the collector current changes by less than 1% for a change in β illustrates that this is a good way to estimate the possible collector current.)

5.19 A pnp power transistor operates with an emitter-to-collector voltage of 5 V, an emitter current of 10 A, and $V_{ce} = 0.85$ V. The $\beta = 5$, what base current is required? What is α_0 for this transistor? Compare the emitter-base junction size of this transistor with that of a small-signal transistor that conducts $I_0 = 1$ mA with $V_{ce} = 10^4$ V. How much larger is it?

SECTION 5.2: CURRENT-VOLTAGE CHARACTERISTICS

5.20 For the circuit in Fig. 5.20 assume that the transistors have very large β . Some component parts have more

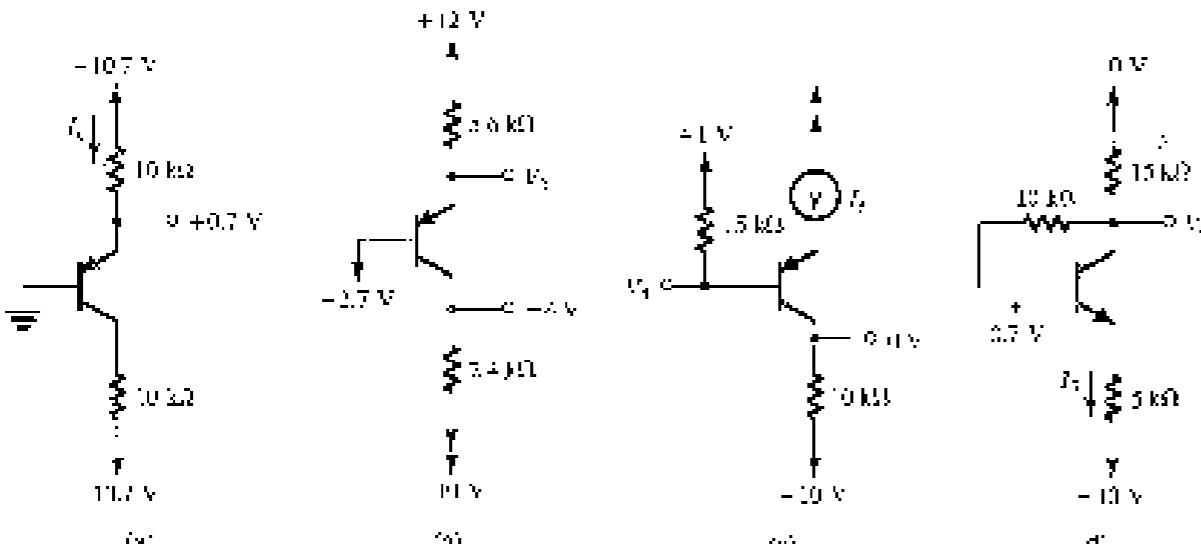


FIGURE P5.20

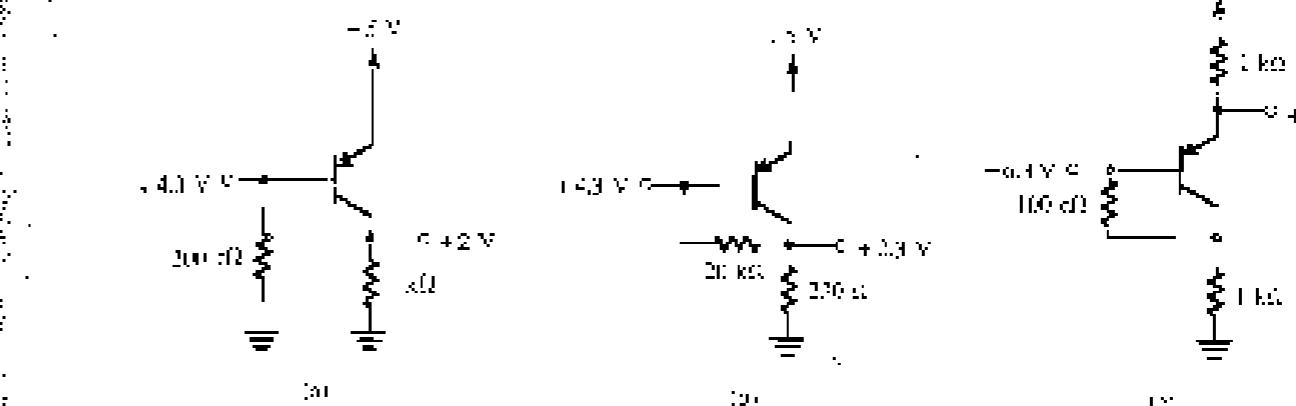


FIGURE P5.21

than two digits will be rounded indicated in the figure. Find the values of the other labeled voltages and currents.

5.21 Make calculations on the circuits of Fig. P5.21 provided labeled voltages as indicated. Find the values of β for each transistor.

5.22 Examination of the value of standard values for resistors with 5% tolerance (Appendix G) reveals that the closest values to those found in the designs of Example 5.1 are 3.1 kΩ and 5.6 kΩ. For these values, use approximate solution techniques (e.g., $V_{ce} \approx 0.7$ V and $\alpha = 1$) to determine the values of collector current and collector voltage that are likely to result.

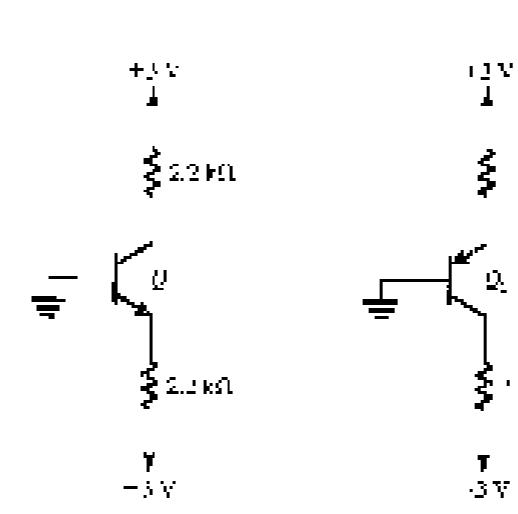


FIGURE P5.24

5.23 Redesign the circuit in Example 5.1 to provide $V_c = 12$ V and $I_c = 1$ mA.

5.24 For each of the circuits shown in Fig. P5.24, find the emitter, base, and collector voltages and currents. Use $\beta = 30$, forward bias $|V_{be}| = 0.7$ V independent of collector level.

5.25 Redesign Problem 5.24 using conditions for which $V_{ce} = 0.7$ V and $I_c = 1$ mA.

5.26 For the circuit shown in Fig. 5.26, measurement indicates that $V_b = -1$ V. Assuming $V_{ce} = 0.7$ V, calculate V_{ce} , i_b , i_c , and V_c for a collector with $\beta = \infty$ biased, with values of V_b , V_{ce} , and V_c as stated.

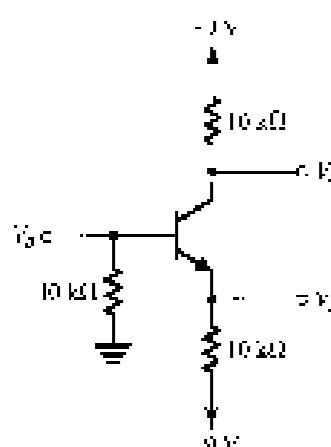


FIGURE P5.28

5.35 The collector current of a BJT is measured to be 20 mA at 25°C. If the temperature of the device is raised to 85°C, what do you expect $I_{C(85)}$ to become?

5.36 Augment the model of the open BJT shown in Fig. 5.20(a) by a current source representing I_{CBO} . Assume that r_o is very large and thus can be neglected. In terms of this addition, what do α_0 , β_0 , and β_0/α_0 become? If the base lead is bypassed while the emitter is connected to ground and the collector is connected to a positive supply, find the emitter and collector currents.

5.37 An open BJT is accidentally connected with collector and emitter leads interchanged. The resulting currents in the normal emitter and base leads are 0.5 mA and 1 mA, respectively. What are the values of α_0 and β_0 ?

5.38 A BJT whose emitter current is fixed at 1 mA has a base-emitter voltage of 0.60 V at 25°C. What base-emitter voltage will it have at 75°C? At 100°C?

5.39 For a BJT having an Early voltage of 200 V, what is its output resistance at 1 mA? At 100 μA?

5.40 What does α_{BO} become if the junction temperature rises to 300°C?

5.41 If the transistor has $\alpha = 1$ and is operated at a base-emitter-base voltage of 720 mV, what emitter current flows at 25°C? At 100°C?

5.42 Consider a transistor for which the base-emitter voltage drop is 0.7 V at 10 mA. What current flows for $V_{BE} = 0.5$ V?

5.43 In Problem 5.42, the stated voltages are measured at 25°C. What values correspond to 25°C? At 100°C?

5.44 Use the Ebers-Moll expressions in Eqs. (E26) and (5.27) to derive Eq. (5.35). Note that the emitter current is set to a constant value I_0 . Ignore the terms not involving exponentials.

5.45 Use Eq. (5.35) to plot the i_C-i_{CE} characteristics of an open transistor having $\alpha_0 = \alpha_{BO} = 0.1$ and $I_0 = 0.1$ mA. For

give the fact $\beta = 10^3$ mA/0.5 mA, and $T = 300$ K. Use an expand x scale for the negative values of i_C and i_{CE} in order to show the details of the saturation region. Neglect the early effect.

***5.36** For the saturated transistor shown in Fig. P5.36, use the BJT expressions to show that $\alpha_0 \approx 1$

$$V_{CBO} = V_T \ln \left[\frac{1 + \frac{I_{CBO}}{I_0}}{1 + \frac{I_{CE0}}{I_0}} \right]$$

To a BJT with $\alpha_0 = 0.1$, evaluate V_{CBO} for $I_{CBO}/I_0 = 0.5$, 0.1, 0.05, and 0.01.

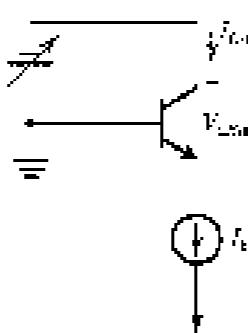


FIGURE P5.36

5.37 Use Eq. (5.36) to plot i_C versus i_{CE0} for an open transistor having $I_0 = 10^{-3}$ A and $V_T = 100$ mV. Provide curves for $\alpha_0 = 0.05, 0.10, 0.20, 0.50$, and 0.75 times. Show the characteristic for i_{CE0} up to 10 V.

5.38 For a particular BJT transistor operating at V_{BE} of 600 mV and $I_0 = 1$ mA, the i_C-i_{CE} characteristic has a slope of 2×10^{-3} A. To what value of i_{CE0} can resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 30 mA, what would the output resistance become?

5.39 For a BJT having an Early voltage of 200 V, what is its output resistance at 1 mA? At 100 μA?

5.40 Measurements of the i_C-i_{CE} characteristics of a complementary transistor operating at $V_{CE} = 720$ mV show $\alpha_{CE0} = 1.5$ mA at $i_{CE0} = 2$ V and that $i_C = 2.4$ mA at $i_{CE0} = 4$ V. What is the corresponding value of i_C near saturation? At what value of i_{CE0} is $i_C = 10$ mA? What is the value of the Early voltage for this transistor? What is the output resistance that corresponds to operation at $i_{CE0} = 720$ mV?

5.41 Use the pnp equivalent circuit models that correspond to those shown in Fig. 5.20 for the pnp case.

5.42 A BJT operating at $\beta_0 = 10^3$ and $\beta_0 = 10^4$ undergoes a reduction in base current of 0.8 μA. It is found that when α_0/β_0 is held constant, the corresponding reduction in collector current is 0.1 mA. What are the values of α_0 and β_0 that apply? If the base current is increased from 0.8 μA to 1.0 μA,

and α_{BO} is increased from 8% to 10%, what net collector-current results? Assume $V_T = 100$ mV.

5.43 For a transistor device β and α_0 is selected as Fig. 5.22, estimate values of β at -55°C, 25°C, and 125°C for $I_0 = 1.0$ μA, $\alpha_0 = 0.1$ mA, for each current, reduce the temperature coefficient for temperatures above and below room temperature (true values needed).

5.44 Figure P5.44 shows a diode-connected BJT transistor. If $\alpha_0 = 0$ results in an active operating point in the BJT will internally result in the active mode; that is, its base and collector currents will be controlled by i_Q . Use the Ebers-Moll equations to show that the diode-connected transistor has the i_C-i_V characteristics

$$i_C = \frac{I_{Q0}(e^{v_{CE}/V_T} - 1)}{e^{i_Q/V_T}}$$

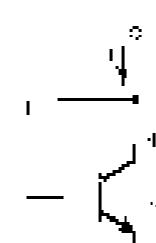


FIGURE P5.44

5.45 A BJT for which $\alpha_0 = 0.2$ operates with a constant base current, but with the collector open. What value of V_{CBO} would you measure?

5.46 For the structure of i_C-i_{CE} , V_{CE0} , and the contact resistance R_{CE0} of a BJT operated at a constant base current of 0.1 mA, and a forced β of 20. The transistor has $\beta_0 = 50$ and $\beta_0 = 0.2$.

***5.47** Use Eq. (5.47) to show that the saturation resistance $R_{SCE0} = \alpha_0/\beta_0$ of a BJT transistor operated with a constant base current I_{B0} is given by

$$R_{SCE0} = \frac{V_T}{\partial_i C_E / \partial (i_C - i_B)}$$

where

$$z = \frac{i_C}{i_B} = \frac{\beta_0 \alpha_0}{\beta_0 + \alpha_0}$$

Find R_{SCE0} for $\alpha_0 = \beta_0/2$.

5.48 For a transistor for which $\beta_0 = 10$ and $\beta_0 = 10^4$, find the value of R_{SCE0} for $i_{B0} = 0.1$ mA, evaluating R_{SCE0} at $i_C = 4$ mA and at $i_C = 0.3$ mA (using Eq. 5.48). Note because here we are modeling operation at a very low forced β , the value of R_{SCE0} will be much larger than that given by Eq. 5.48.

5.49 A transistor has $\alpha_0 = 150$ and the collector junction is 20 times larger than the emitter junction. Evaluate V_{CBO} for $\beta_0 = 100$, 0.05, 0.01, 0.001, and 0.0001. For each, give the maximum possible positive and

5.50 A particular npn BJT with $\alpha_0 = 750$ at $i_0 = 0.01$ μA, and having $\beta = 100$, has a collector-base junction 20 times larger than the emitter-base junction.

(a) Find α_0 , β_0 , and β_0/α_0 .
the Early voltage of about 0.2 mA and constant base current, what is the base-emitter voltage and the base current?
(b) For the situation in (a) but with a double, i.e., enhanced base current, what is the value of forced β ? What are the base-emitter and base-collector voltages? What are V_{CBO} and R_{SCE0} ?

5.51 A BJT with two base contacts has $V_{CE0} = 100$ mV with the cathode connected to the collector, and the collector-emitter junction is grounded. The collector is open-circuited, V_{CE0} becomes 1 mV. Estimate values of α_0 , β_0 , and β_0/α_0 for this transistor.

5.52 A BJT for which $\alpha_0 = 0.5$ mA has $V_{CE0} = 140$ mV at $I_0 = 10$ μA and $V_{CE0} = 170$ mV at $I_0 = 20$ mA. Determine the values of its saturation resistance, R_{SCE0} , and its offset voltage, V_{CBO} . At 50, determine the values of β_0 and β_0/α_0 .

5.53 A BJT for which $V_{CE0} = 30$ V is constructed as shown in Fig. P5.53. What voltages would you measure on the collector, base, and emitter?

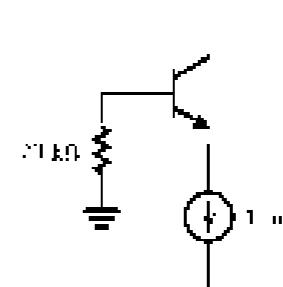


FIGURE P5.53

SECTION 5.3: THE BJT AS AN AMPLIFIER AND AS A SWITCH

5.54 For a common-emitter amplifier circuit operated with $V_{CE0} = 10$ V, biased at $V_{BE} = 0.7$ V. Find the voltage gain, the maximum allowed output voltage swing without the transistor entering saturation, and the corresponding minimum input signal amplitude.

5.55 For the common-emitter arrangement in Fig. 5.23, with $V_{CE0} = 410$ V and $\beta_0 = 1$ mA. For $V_{BE} = 0.7$ V, find the following dc collector dissipation at 1 mA, 2 mA, 3 mA, 5 mA, and 9 mA. For each, give the maximum possible positive and

negative output voltage determined by V_{CE} to keep the transistor in the active region. Please you do not make it stable.

5.56 Consider the common-emitter circuit of Fig. P5.55(a) when operated with a dc supply $V_{CC} = -5$ V. It is required to find the point i_1 at which the transistor should be biased; that is, find the value of V_B so that the output sinusoidal wave signal v_o resulting from an input sine wave signal v_i of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain of the small-signal operation around the bias point? Hint: To obtain the maximum possible output amplitude for a given input, you need i_1 to be as far away as possible from the edge of saturation as possible without entering saturation at any time, but i_1 without v_{CE} decreasing below 0.4 V.

5.57 The transistor in the circuit of Fig. P5.57 is biased at a dc collector current of 0.5 mA. What is the voltage gain? Hint: Use Thevenin theorem to convert the circuit to the form in Fig. 5.26(c).

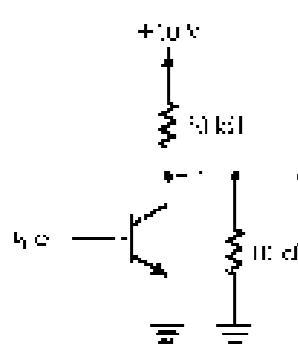


FIGURE P5.57

5.58 Sketch and label the voltage transfer characteristic of the pnp common-emitter amplifier shown in Fig. P5.58.

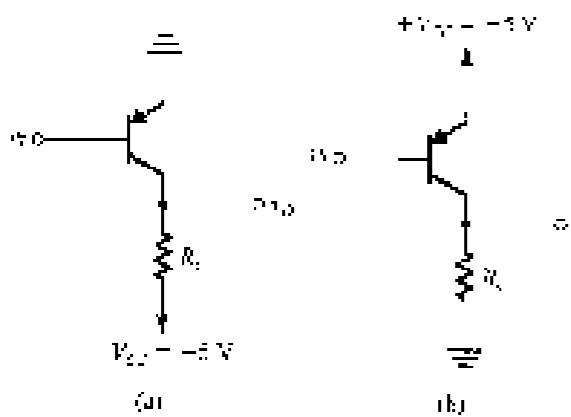


FIGURE P5.58

***5.59** In deriving the expression for small-signal voltage gain A_v in Eq. (5.56) we neglected the Early effect. Devise this expression including the Early effect. Hint: Hint: Hint:

$$i_1 = I_{BO} e^{(V_B - V_T)/V_A} \left(1 - \frac{g_m}{V_A} \right)$$

in Eq. (5.56). Now that the gain expression changes to

$$A_v = \frac{I_C R_L / V_A}{\left[1 + \frac{I_C R_L}{V_A + V_{BE}} \right]} = \frac{(V_{CC} - V_{CE}) / V_A}{\left[1 + \frac{V_{CE} - V_{CE}}{V_A + V_{CE}} \right]}$$

For the case $V_{CE} = 3$ V and $V_{CC} = 2.5$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

5.60 We can the common-emitter amplifier circuit of Fig. 5.26(a) is biased with a certain V_{CE} , the dc voltage at the collector is found to be 13 V. If $V_B = -5$ V and $R_C = 1\text{k}\Omega$, find I_C and the small-signal voltage gain. For a change $V_{CE} = 5$ mV, calculate the resulting A_{v1} . Calculate it two ways: by finding A_{v1} using the transistor exponential characteristics and approximately using the small-signal values β and α . Repeat for $V_{CE} = 5$ mV. Summarize your results in a table.

5.61 Consider the common-emitter amplifier circuit of Fig. 5.26(a) when operated with a supply voltage $V_{CC} = -5$ V.

- What is the desired maximum voltage gain that this amplifier can provide?
- What value of V_{CE} and the operating behavior of the transistor provide a voltage gain of -100 V/V?
- If the dc collector current I_C at the bias point in (a) is to be 3.5 mA, what value of R_C should be used?
- What is the value of V_{CE} required to prevent the bias point mentioned above? Assume that i_1 , R_L , and $\beta = 10^{15}$ A.
- If a sine-wave signal v_i having a 5-mV peak amplitude is superimposed on V_{CE} , find the corresponding output voltage signal v_o , that will be superimposed on V_{CE} assuming linear operation around the bias point.
- Characterize the signal current i_1 , that will be superimposed on the dc bias current i_1 .
- What is the value of the dc base current i_B at the bias point? Assume $\beta = 100$. Characterize the signal current that will be superimposed on the base current i_B .
- Dividing the amplitude of v_i by the amplitude of i_1 , estimate the incremental (or small-signal) input resistance of the amplifier.
- Sketch and clearly label correlated graphs between i_B and i_1 . Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

5.62 The essence of transistor operation is that a change in age, V_A , produces a change in i_1 , V_{CE} . By keeping V_A constant, i_1 is approximately linearly related to V_{CE} . $\beta = g_m$ does what g_m is known as the transistor transconductance. By passing V_A through R_L , an output voltage signal v_{o1} is obtained. Use the expression for the small-signal voltage gain in Eq. (5.56) to derive an expression for A_{v1} . Find the value of g_m for a transistor model $\beta = 10^4$.

5.63 Consider the two-terminal source shown in Fig. P5.63 with the following additional information. For each line, use the lowest colored line: $i_1 = 1\text{ }\mu\text{A}$, $10\text{ }\mu\text{A}$, $100\text{ }\mu\text{A}$, and $1\text{ }\text{mA}$. Assume the lines to be horizontal, and let $\beta = 100$. Let $V_{CE} = 5$ V and $R_C = 1\text{k}\Omega$, where peak-to-peak collector voltage swing v_{o1} results in i_1 varying over the range 10 μA to 100 μA . At a new bias point (not the one shown in the figure), $V_B = -1.7$ V and the value of i_1 and V_{CE} at this point, $V_B = -1.7$ V and of $R_L = 100\text{ }\Omega$, find the required value of R_L .

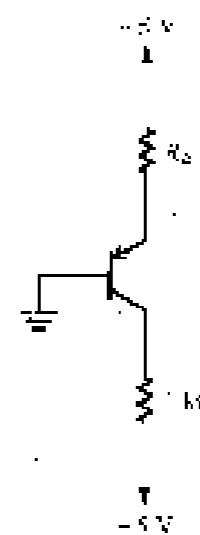


FIGURE P5.63

5.64 Sketch the i_1-v_{CE} characteristics of a pnp transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_1 = 20\text{ }\mu\text{A}$, $30\text{ }\mu\text{A}$, $100\text{ }\mu\text{A}$, and $1\text{ }\text{mA}$. For the purpose of this sketch, assume that $i_1 = \beta(V_{CE} - V_T) - P$. Also, sketch the load line obtained for $V_{CE} = 10$ V and $R_L = 1\text{k}\Omega$. If the collector current in the base is $30\text{ }\mu\text{A}$, write the equation for the corresponding V_{CE} voltage. Also, write the equation for the load line, and solve the two equations for i_1 , V_{CE} , and i_B . If the input signal causes a sinusoidal signal of 20 μA peak amplitude to be superimposed on i_1 , find the corresponding signal components of i_B and v_{CE} .

5.65 For the circuit in Fig. P5.55 select a value for R_{L2} so that the transistor saturates with an overdrive factor of 10. The BJT is specified to have a minimum β of 20 and $V_{CE(sat)} = 0.2$ V. What is the value of V_{CE} ? β is assumed?

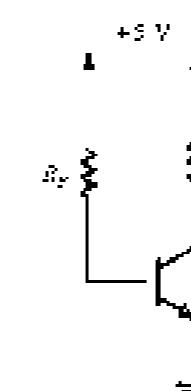


FIGURE P5.65

5.66 For the circuit in Fig. P5.55 select a value for R_{L2} so that the transistor saturates with a drive factor of 5. Assume $V_{CE} = 0.2$ V and $V_{CE(sat)} = 0.2$ V. For what value of i_1 does saturation begin? What is i_1 at this point? For $v_i = 4$ V and 6 V, what are the values of v_o , i_1 , i_B , and i_C ? Answer your sketch by adding a plot of i_1

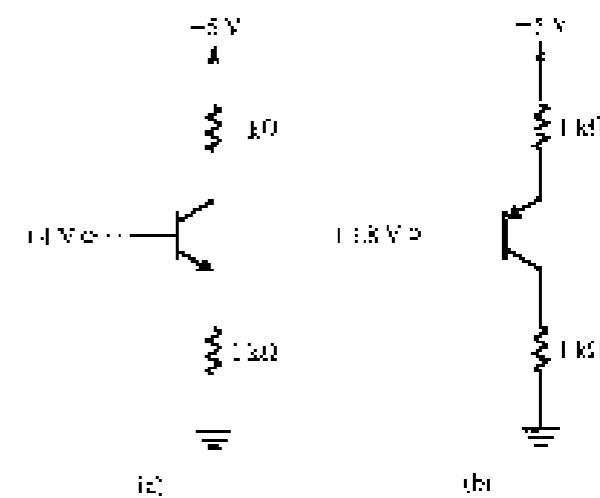


FIGURE P5.66

5.68 Consider the operation of the circuit shown in Fig. P5.68. i_1 is zero except from zero. For this transistor, assume $\beta = 50$, $i_{BO} = 0$, and the nonlinear equations: if $V_{CE} < 0.5$ V, $i_C = 0$; when i_1 is conducting, if $V_{CE} = 0.7$ V, $i_C = 0.1$ A; and the transistor is deeply in saturation, at $V_{CE} = 0.6$ V. Sketch and label i_1 , i_C , and v_{CE} versus v_i . You want i_1 and i_C to be exactly 50% of v_i . What are the values of i_1 , i_C , and v_{CE} for $v_i = 1$ V and 3 V? For what value of i_1 does saturation begin? What is i_1 at this point? For $v_i = 4$ V and 6 V, what are the values of v_o , i_1 , i_C , and i_{BO} ? Answer your sketch by adding a plot of i_1

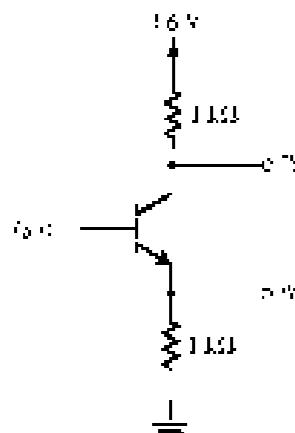


FIGURE PS.68

SECTION 5.4: BJT CIRCUITS AT DC

5.69 The transistor in the circuit of Fig. PS.69 has a very high β . Find V_C and I_C for V_B (a) 13 V, (b) +1 V, and (c) 0 V. Assume $V_{BE} \approx 0.7$ V.

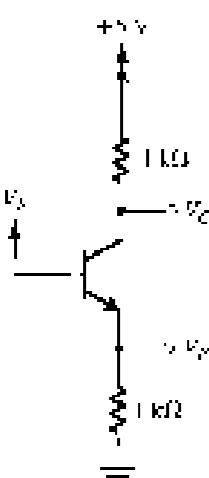


FIGURE PS.69

5.70 The transistor in the circuit of Fig. PS.69 has a very high β . Find the largest value of V_B for which the transistor still operates in the active mode. Also, find the value of V_C for which the transistor operates in saturation with a desired I_C .

5.71 Consider the operation of the circuit shown in Fig. PS.71 for $|V_B|$ at +1 V, 0 V, and -1 V. Assume that V_{BE} is 0.7 V for usual currents and that β is very high. What values of V_C and I_C exist? At what value of V_B does the emitter current reduce to one-tenth of its value for $V_B = 0$ V? For what value of V_B is the transistor just at the edge of conduction? What

values of V_B and V_C correspond? For what value of V_B does the transistor just saturate (when the base-to-collector junction reaches 0.5 V of forward bias)? What values of V_B and V_C correspond? Find the value of V_B for which the transistor operates in saturation with a desired β of 2.

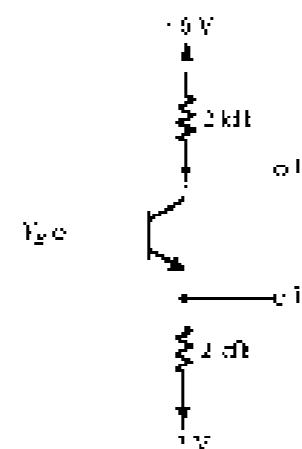


FIGURE PS.71

5.72 For the circuit shown in Fig. PS.72, assume $\alpha=1$ and $v_{ce}=0.5$ V at the edge of conduction. What are the values of V_C and I_C for $V_B = 0$ V? For what value of V_B does the transistor cut off? Saturated? In each case, what values of V_C and I_C result?

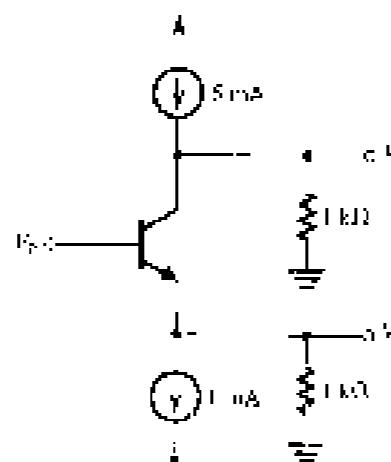


FIGURE PS.72

5.73 Consider the circuit in Fig. PS.69 with the base voltage V_B obtained using a voltage divider across the 5-V supply. Assuming the transistor B to be very large (i.e., ignoring the base current), design the voltage divider to obtain a $V_B = 2$ V. Design for a 0.2 mA current in the voltage divider. Now, if the BJT $\beta = 100$, analyze the circuit to determine the collector current and the collector voltage.

5.74 A single measurement indicates the emitter voltage of the transistor in the circuit of Fig. PS.74 to be 1.0 V. Under the assumption that $|V_{BE}| = 0.7$ V, what are V_B , I_B , I_C , V_C , β , and v_{ce} ? What kind of measurement would you make to verify that the transistor is operating in the active mode?

5.75 For the circuit in Fig. PS.75, find V_{BE} , V_C , and I_C if $R_B = 100\text{ k}\Omega$, $R_C = 1\text{ k}\Omega$, and $\beta = 100$.

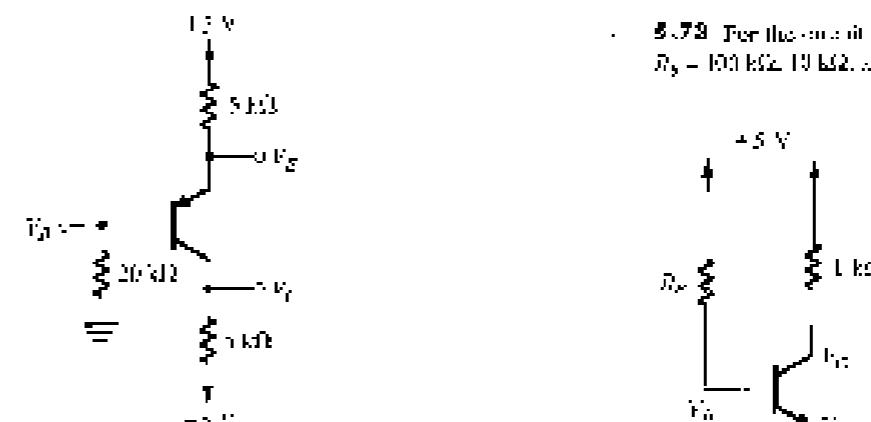


FIGURE PS.75

5.76 Design a circuit using a pnp transistor for which $\alpha = 1$ and $V_{BE} = 0.7$ V using two resistors connected appropriately to 12 V so that $I_E = 2$ mA and $V_{CE} = 1.5$ V. What exact values of R_1 and R_2 would be needed? Now, consult a table of standard resistor values (e.g., that provided in Appendix G) to select suitable practical values. What are the values of I_E and V_{CE} then?

5.77 In the circuit shown in Fig. PS.76, the transistor has $\beta = 50$. Find the values of V_B , V_C , and I_C . If R_B is raised to 27 kΩ, what value of V_B is required? With $R_B = 27$ kΩ, what value of β would return the voltages to the values best obtained?

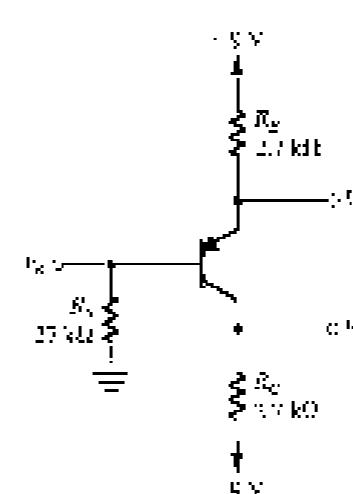


FIGURE PS.77

5.78 In the circuit shown in Fig. PS.78, the transistor has $\beta = 30$. Find the values of V_B , V_C , and I_C , and verify that the transistor is operating in the active mode. What is the largest value for R_C that may be used while the transistor remains in the active mode?

5.79 For the circuit in Fig. PS.79, find V_{BE} , V_C , and I_C if $R_B = 100\text{ k}\Omega$, $R_C = 1\text{ k}\Omega$, and $\beta = 100$.

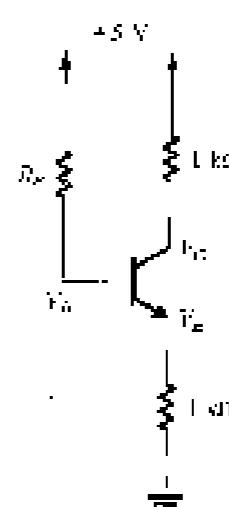


FIGURE PS.78

5.80 For the circuit in Fig. PS.79, find V_{BE} for the labeled node voltages and branch currents. Assume β to be very high and $V_{BE} = 0.7$ V.

5.81 Repeat the analysis of the circuits in Problem 5.79 using $\beta = 10$. Find all the labeled node voltages and branch currents. Assume $|V_{BE}| = 0.7$ V.

5.82 It is required to design the circuit in Fig. 7.31 so that a current of 1 mA is established in the emitter and a voltage of +2 V appears at the collector. The transistor specified has a nominal β of 100. However, the β value can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when $\beta = 100$ and that at the extreme values of β the emitter current does not change by more than 10% of its nominal value. Also, design for as large a value for R_C as possible. Give the values of R_E , R_C , and R_B to the nearest kilohm. What is the expected range of collector current and collector voltage corresponding to the range of $|V_{BE}|$ (0.7 to 0.8)?

5.83 The pnp transistor in the circuit of Fig. PS.81 has $\beta = 50$. Find the value for R_C to obtain $V_C = 15$ V. What happens if the transistor is replaced with another having $\beta = 100$?

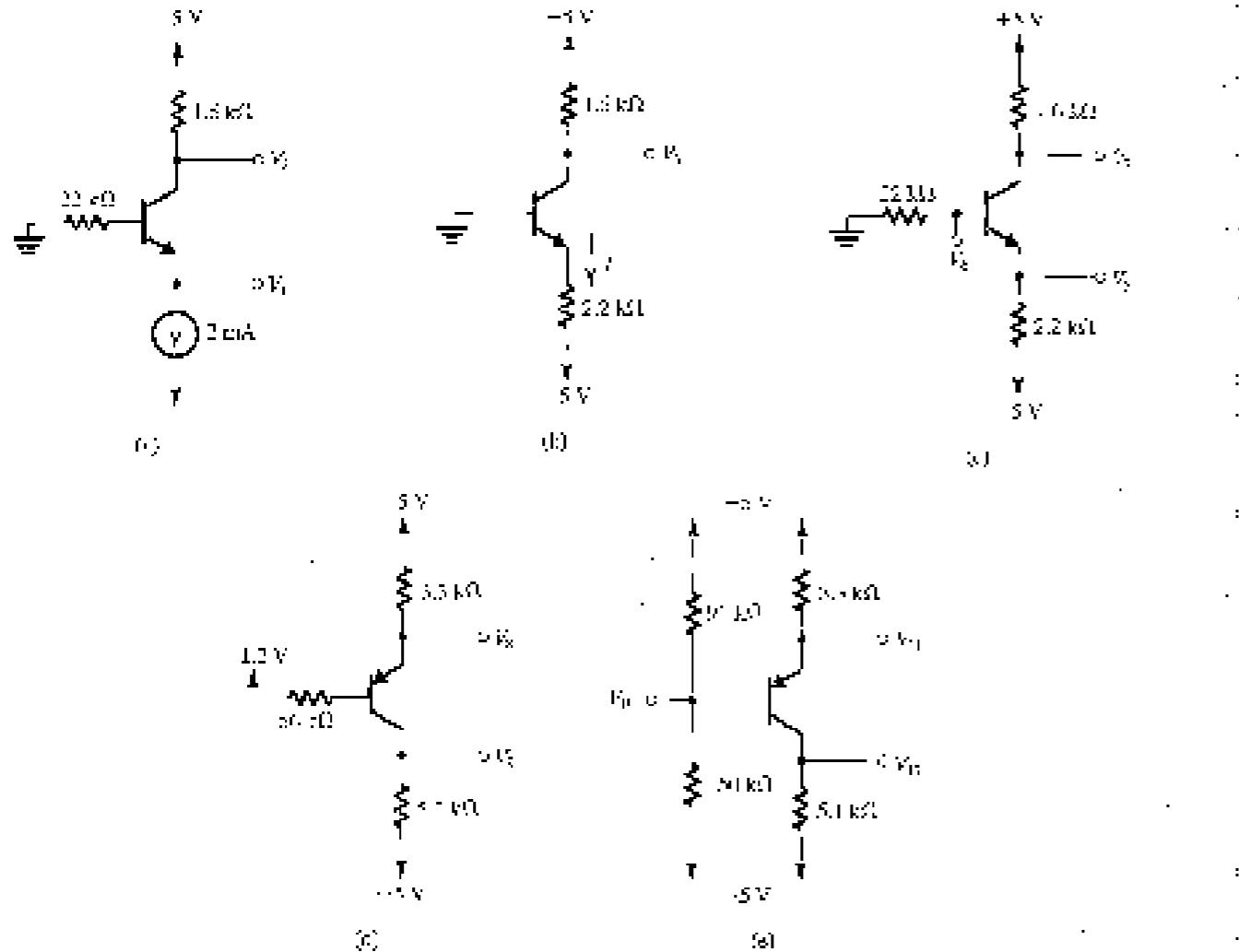


FIGURE P5.79

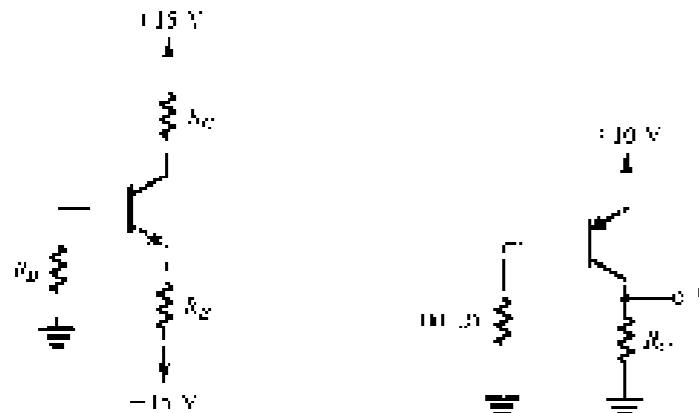


FIGURE P5.37

125.8 Consider the circuit shown in Fig. PS.83. It is required that at $t = 0$ the bias voltages across transistors B_1 and B_2 are unequal to provide negative feedback action so as to provide temperature compensation for the emitter-base voltage of Q_1 and Q_2 . Second, now resistor R_{12} whose purpose is provide negative feedback, moves on resistance in the branch. Using $|V_{BE1}| = |V_{BE2}| = 0.7\text{ V}$, standard values of current and $\beta = 100$, find the voltages V_{B1} , V_{B2} , V_{C1} , V_{C2} and V_{CE1} initially with R_{12} short-circuited and then with it connected. Neglect r_e , $\beta = 100$, initially with R open circuit and r_o connected.

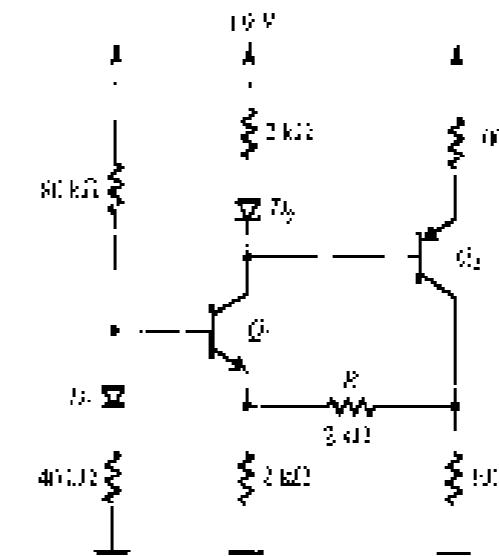


FIGURE P5.93

15.84 For the circuit diagram in Fig. PS 15.7, find the labeled node voltages.

- 50
10

***P5.85** Using $\beta = \infty$, design the circuit shown in Fig. P5.83 so that the bias currents in Q_1 , Q_2 , and Q_3 are 2 mA, 2 mA, and 4 mA, respectively, and $V_T = 0$, $V_{BE} = -4$ V, and $V_{CE} = 2$ V. For each transistor, select the nearest standard value of H from the table of standard values for H given in Appendix G. Show, from $i_c = \beta i_b$, the values of I_1 , I_2 , I_3 , V_{CE} , and V_T .

5.86 For the circuit in Fig. P5.86, find V_L and I_2 for $\omega = 5 \text{ rad/s}$, 5 V , and -15 V . The BJT's have $\beta = 100$.

***5.87** Find approximate values for the collector voltage in the circuits of Fig. 55.87. Assume constant β for each of the transistors. (Over, fairly by assuming all resistances are negligible in accuracy, and we have assumed this.)

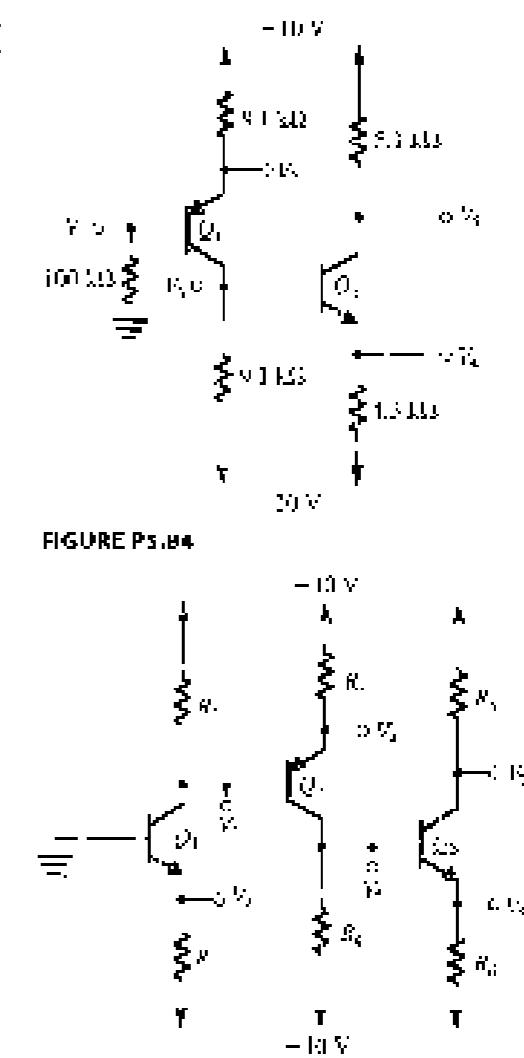


FIGURE P5.8

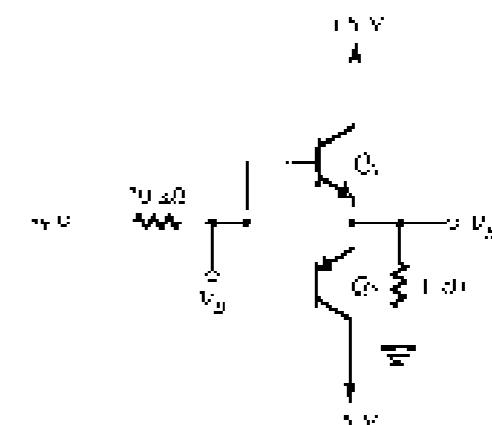


FIGURE P5.8c

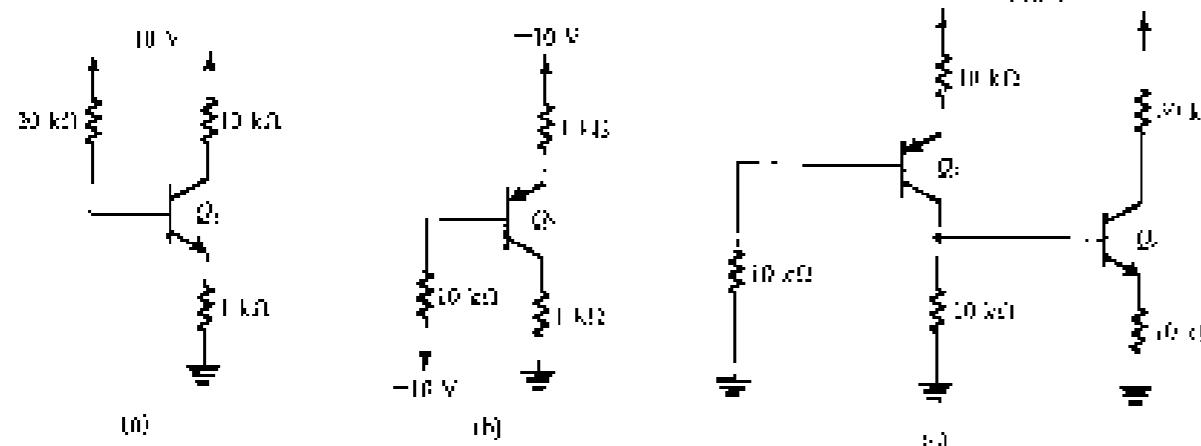


FIGURE P5.87

SECTION 5.5: BIASING IN BJT AMPLIFIER CIRCUITS

P5.88 For the circuit in Fig. 5.43(a), neglect the base current to an emitter with the exception of the voltage divider. It is required to bias the transistor at $I_C = 1 \text{ mA}$, which requires selecting R_B and R_C so that $V_{CE} = 0.650 \text{ V}$. If $V_{BE} = 0.7 \text{ V}$, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and R_{B2} are the same value, that is, each can be in the range of 1.00 to 1.01 of its nominal value, what is the range obtained for V_{CE} ? What is the corresponding range of I_C ? If $R_C = 1 \text{ k}\Omega$, what is the range obtained for V_0 ? Comment on the efficiency of this biasing arrangement.

P5.89 It is required to bias the transistor in the circuit of Fig. 5.43(b) at $I_C = 1 \text{ mA}$. The transistor β is specified to be maximally 100, but it can fall to 50 or 50 to 100. For $V_{BE} = 0.7 \text{ V}$ and $R_C = 1 \text{ k}\Omega$, find the required value of R_B to achieve $I_C = 1 \text{ mA}$ for the two β 's considered. What is the expected range for I_C and V_{CE} ? Comment on the efficiency of this bias design.

P5.90 Consider the single-supply bias network shown in Fig. 5.11(a). Provide a design using a 12-V supply in which the supply dc (12V) is applied voltages between R_B , R_{C1} , and R_C with a total current of 3 mA. The transistor β is specified to have a minimum value of 50; use a voltage divider consisting of R_{B1}/R_{B2} no higher than 1.01. Since a reasonable design would operate for the two transistors for which β is very low, do your initial design with $\beta = 50$. Then choose suitable β 's assuming (see Appendix G), making the choice in a way that will result in a V_{CE} that is slightly higher than the ideal. Specify the values you have chosen for R_B , R_{C1} , R_C , and R_{C2} . Now, find V_{BE} , V_{CE} , I_C , and V_0 for your final design, using $\beta = 90$.

P5.91 Repeat Problem 5.90, but use a voltage-divider circuit which is $\beta/2$. Check your design for $\beta = 50$; if you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 5.90 ($\mu = 20$).

***P5.92** It is required to redesign the bias circuit of Fig. 5.41 for a BJT whose terminal $\beta = 100$.

(a) Find the current ratio (R_B/R_{B1}) that will guarantee I_C remains within ±5% of its nominal value for β as low as 50 and as high as 150.

(b) If the resistance value listed in (a) is used, find an expression for the voltage $V_{CE} = V_{CC} R_{C1} / (R_C + R_{C1})$ that will result in a voltage drop of $V_{CE}/2$ across R_{C1} .

(c) For $V_{BE} = 0.7 \text{ V}$, find the required values of R_B , R_{C1} , and R_C to obtain $I_C = 2 \text{ mA}$ and to satisfy the requirement on stability of I_C in (a).

(d) Find R_C so that $V_{CE} = 3 \text{ V}$ for $\beta = 50$ for its nominal value.

Check your design by calculating the resulting range of I_C .

***P5.93** Consider the two-supply biasing network shown in Fig. 5.5-5 using -5-V supplies. It is required to design the circuit so that $I_C = 3 \text{ mA}$ and V_{CE} is placed midway between V_{CC} and V_{EE} .

(a) For $\beta = \infty$, what values of R_B and R_C are required?

(b) If the BJT is specified to have a minimum β of 50, (i.e., the largest value for β consistent with the need to limit the voltage drop across it to less than the voltage across R_{C2}), what standard 10% resistor values (see Appendix G) would you use for R_B , R_{C1} , and R_{C2} ? In making your selection, use somewhat lower values in order to compensate for the low- β effects.

(c) For the values you selected in (b), find V_{BE} , V_{CE} , and I_C for $\beta = \infty$ and $\beta = 50$.

P5.94 Utilizing 12-V power supplies, it is required to design a version of the circuit in Fig. 5.43(b) in which the signal will be coupled to the emitter and thus R_B can be set to zero. Find values for R_B , R_{C1} , and R_C that minimize current of 1 mA is obtained and in doing so gain is maximized while allowing ±1 V of signal swing at the collector. If temperature increases from the nominal value of 25°C to 125°C, express the percentage change in collector bias current. In addition, if $\beta = 100$ → 2 mA/V²/°C change in V_{BE} results from the transistor β changes over this temperature range. Even 1% in β ?

P5.95 Using a 12-V power supply, design a version of the circuit of Fig. 5.10 to provide a dc emitter current of 0.5 mA and a ±1-V signal swing at the collector. The BJT has a gain of $\beta = 100$. Use standard 10% resistor values (see Appendix G). If the actual BJT used has $\beta = 50$, what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for $\beta = 10$.

P5.96 (a) Using a 12-V power supply, design the feedback bias circuit of Fig. 5.46 to provide $I_C = 2 \text{ mA}$ and $V_{CE} = V_{CC}/2$ for $\beta = 50$.

(b) Select standard 5% resistor values, then measure V_{CE} and I_C for $\beta = 50$.

(c) Find V_{BE} and I_C for $\beta = \infty$.

(d) To improve the efficiency that obtains when high- β transistors are used, we now desire to add additional current to flow through R_E . This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P5.96. Design this circuit for $\beta = 50$ to have a current through R_E equal to the base current. Use given values of V_{CC} and I_C and show how to $\beta = \infty$.

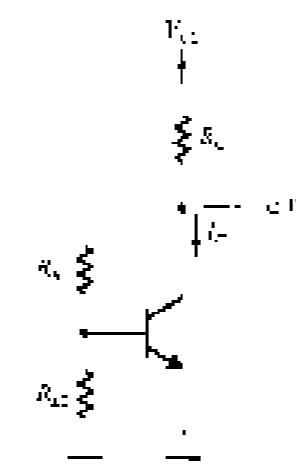


FIGURE P5.96

P5.97 A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P5.97. Find I_C for $\beta = \infty$ and $\beta = 50$.

values of I_C , R_B , R_C given $I_C(0) = 2 \text{ mA}$ and $V_{CC} = 1.5 \text{ V}$, $T = 30^\circ\text{C}$.

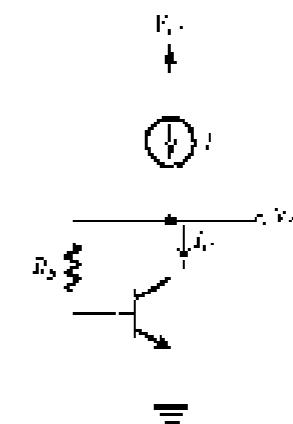


FIGURE P5.97

P5.98 The circuit in Fig. P5.98 provides a constant current I_C , as long as the circuit to which the collector is connected does not draw the BJT into the active mode. Show that

$$I_C = \frac{(V_{CC} - (R_E/(R_E + R_L))V_{CE})}{R_E + (R_E + R_L)/(\beta + 1)}$$

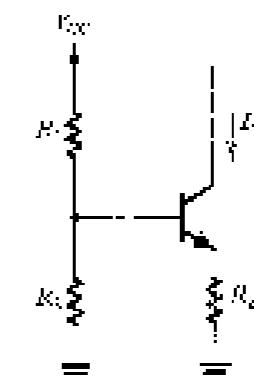


FIGURE P5.98

***P5.99** The current- β circuit shown in Fig. 18.30 provides the bias current to Q1 (that is, is independent of R_E) in nearly a law manner as the value of β , so long as Q1 operates in the active mode. Provide a design meeting the following specifications: Use 12-V supply; $I_C = 1 \text{ mA}$; $V_{CE} = 2 \text{ V}$ for $\beta = \infty$; the voltage across R_E decreases by 1% as β falls for $\beta = 50$; $V_{BE} = 0.7 \text{ V}$ for $\beta = \infty$ and 2.5 V for $\beta = 10$; use standard 10% resistor values (see Appendix G). What values for R_B , R_E , R_C , and R_{C2} do you choose? What values of I_C and V_{CE} result for $\beta = 50$, 100, and 200?

and r_e is 1.5 k Ω . Draw the complete amplifier model using the hybrid-pi BJT equivalent circuit. Calculate the overall voltage gain (v_o/v_i) when $\beta = 100$, and the BJT β included by the values of the model parameters? To what value must β be increased to double the overall voltage gain?

E.115 For the circuit shown in Fig. E5.115, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use $\alpha = 0.99$). Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in} ? Calculate the overall voltage gain (v_o/v_{in}) .

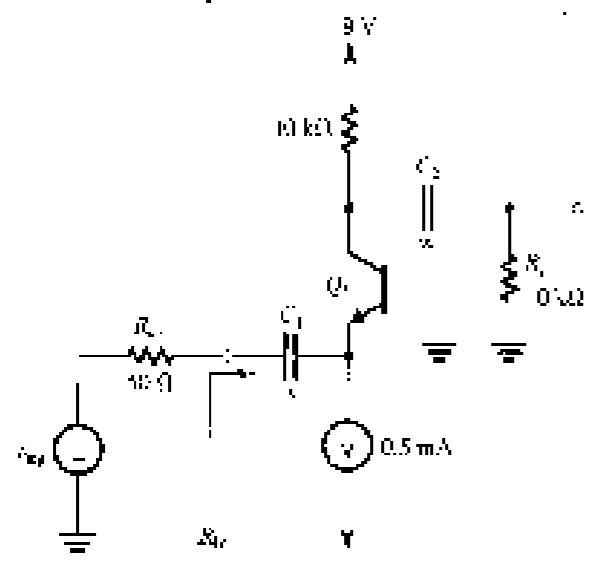


FIGURE E5.115

E.116 In the circuit shown in Fig. E5.116, the transistor has a $\beta = 100$. What is the voltage at the collector? Find the input resistance R_{in} and R_o , and the overall voltage gain

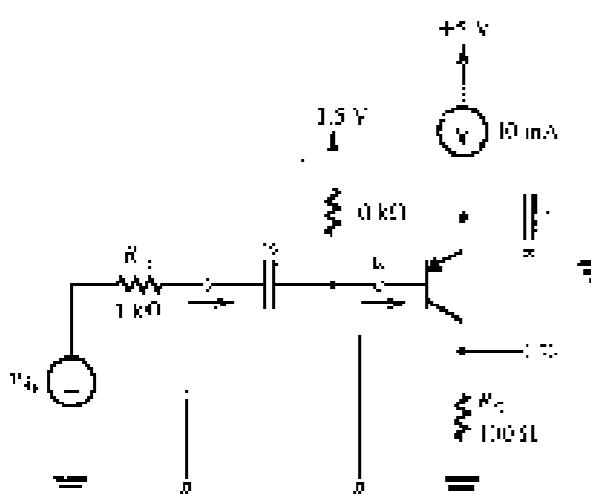


FIGURE E5.116

(v_o/v_{in}) . For a current signal of 0.4 mA, what values of v_{in} and v_o are required?

E.117 Consider the augmented hybrid-pi model shown in Fig. 5.50(a). Disregard α ; assume $\alpha = 1$. What is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain, for $V_b = 25$ V and $V_a = -25$ V.

E.118 Consider the amplifier shown in Fig. 5.59 and analyzed in Example 5.14 under the condition that β is not well controlled. For what value of β does the error begin to decrease? We can conclude that $\beta \geq 10$ is adequate in the circuit. Now, consider the effect of reduced β , say, to $\beta = 2$. What values of r_s , g_{ce} , and r_o result? What is the overall voltage gain? Note: You can see that this circuit, using v_{in} , current control at base, is very insensitive to β but is not immune to it.

E.119 Reconsider the circuit shown in Fig. 5.59; take the condition that the signal source has an internal resistance $r_s = 100\Omega$. What does the overall voltage gain become? What is the largest input signal voltage that can be used without clipping?

E.120 Redesign the circuit of Fig. 5.59 by raising the resistance r_s used by a factor of 10 to the resistance seen by the input v_{in} to 15 k Ω . What value of voltage gain can be obtained if the bias voltage is 12 V? (Assume 12 Vdc is applied to collector IV, in which the right-hand supply is tied to ground.) How does β need to be "adjusted" to the equivalent resistances of the hexabipolar junction?

E.121 Using the BJT equivalent circuit model of Fig. 5.50(a), sketch the equivalent circuit of a transistor amplifier for which a resistance R_s is connected between the emitter and ground, the collector is grounded, and no input signal (i.e., no v_{in}) is present between the base and ground. If it is assumed the transistor is properly biased to operate in the active region, tell how the circuit will operate.

(a) the voltage gain between base and collector, that is, v_o/v_{in} is given by

$$\frac{v_o}{v_{in}} = \frac{R_o}{R_s + r_o}$$

(b) the input resistance

$$R_{in} = \frac{r_s}{\beta} + (\beta + 1)(R_s + r_o)$$

Find the numerical values for v_o/v_{in} and R_{in} for the case $R_s = 1\text{k}\Omega$, $\beta = 100$, and the emitters current $I_{e0} = 1\text{mA}$.

E.122 When the collector of a transistor is connected to its base, the transistor still operates internally? In the active region because the collector-base junction is still in effect reverse biased. Use the simplified hybrid-pi model and the

parameters for a 1-signal resistance of the resulting two-terminal device (transistor model connected transistors).

***E.123** Design an amplifier using the configuration of Fig. 5.50(a). The power supplies available are ± 10 V. The input signal source has a resistance of 100 k Ω , and it is required that the output load resistance match this value. (Note that $R_s = r_s$, $R_o = r_o$.) The amplifier is to have the greatest possible voltage gain, and the target linear operating range signal component across the base-emitter junction should be limited to no more than 10 mV. Find appropriate values for R_s and R_o . What is the value of voltage gain in dB?

***E.124** The circuit in the circuit shown in Fig. E5.124 is biased to operate in the active mode. Assuming that β is very large, find the collector bias current I_c . Replace the transistors with the small-signal equivalent circuit model of Fig. 5.50(a); then, go to replace the dc power supply with a short circuit. Analyze the resulting ac voltage equivalent circuit to show that

$$\frac{v_o}{v_{in}} = \frac{R_o}{R_s + r_o}$$

$$\frac{R_{in}}{v_{in}} = \frac{-\alpha R_s}{R_s + r_o}$$

Find the values of the voltage gains (i.e., $\alpha = 1$). Now, if the terminal labeled v_o is connected to ground, what does the voltage gain v_o/v_{in} become?

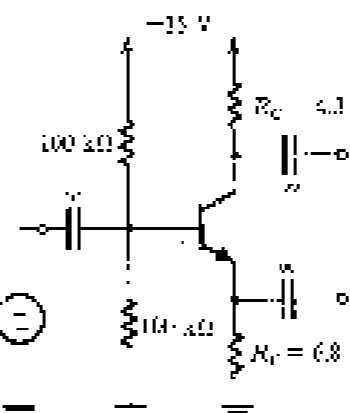


FIGURE E5.124

SECTION 5.7: SINGLE-STAGE BJT AMPLIFIERS

E.125 An amplifier is measured to have $R_s = 10\text{k}\Omega$, $A_{vo} = 100$ V/V, $v_{in} = 1\text{mV}$, $r_s = 100\Omega$. At 0.1 when a load resistance R_o of 1 k Ω is connected between the output terminals, the input resistance is found to decrease to 8 k Ω . The amplifier is fed with a signal source having an internal resistance of 2 k Ω , and G_{in} , A_{vo} , R_{in} , R_{out} , and r_o .

E.126 Figure E5.126 shows an alternative equivalent circuit for representing any linear two-port network including voltage

amplifiers. This non-unilateral equivalent circuit is based on the g parameter two-port representation (see Appendix H).

(a) Using the values of R_s , A_{vo} , and R_o found in Example 5.17 together with the measured value of R_s of 100 k Ω obtained when a load R_o of 10 k Ω is connected in the o port, determine the value of the feedback factor.

(b) Now use the equivalent circuit of Fig. E5.126 to determine R_s of the two-port of R_{in} is connected when the o port is fed with a signal generator having $A_{vo} = 100$ V. Check your results against those found in Example 5.17.

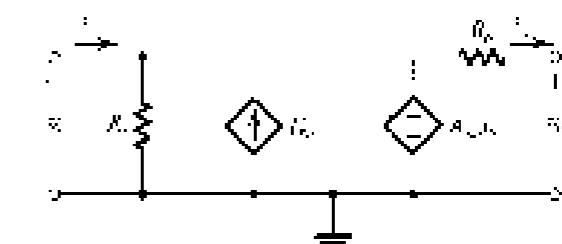


FIGURE E5.126

E.127 Refer to Table 4.5. By applying the expression for G_{in} obtained from Equivalent Circuit A to that obtained from Two-Port Equivalent Circuit C with $G_{in} = (R_s/R_s + R_{in})A_{vo}$, show that

$$\frac{R_s + R_{in}}{R_s + R_{in} + R_o} = \frac{R_o}{R_s + R_{in}}$$

Now, use this expression to:

- (a) Show that for $R_o = \infty$, $R_{in} = R_s$.
- (b) Show that for $R_{in} = 0$, $R_{in} = R_o$.
- (c) For $R_{in} = R_s$, $R_o = \infty$ (i.e., the output buffer is open circuited), and evaluate the value for the small-signal operation in Example 5.17.

E.128 A common-emitter amplifier, the type shown in Fig. 5.50(a), is biased to operate at $I_c = 0.2$ mA and has a collector resistance $R_c = 24$ k Ω . The transistor has $\beta = 100$ and a target V_b . The signal source is directly coupled to the base, and C_{in} and R_s are eliminated. If $V_b = V_{cc}$, the voltage gains A_{vo} and R_{in} can be used to determine the overall voltage gain when a 11 k Ω load resistor is connected to the collector and the source resistance $R_{in} = 10$ k Ω .

E.129 Repeat Problem E5.128 with a 25-k Ω resistance inserted in the signal path in the emitter. Furthermore, compute the maximum amplitude of the input signal v_{in} that can be applied without distortion, assuming that to limit distortion the signal between base and emitter must not exceed 5 mV.

E.130 For the common-emitter amplifier shown in Fig. E5.130, if $V_{cc} = 9$ V, $R_s = 27$ M Ω , $R_c = 15$ k Ω , $R_{in} = 1.2$ k Ω , and $R_o = 3.2$ k Ω , the transistor has $\beta = 100$ and $V_b = .00$ V,

Calculate the dc bias current i_B if the amplifier operates between a source v_{in} whose $R_{in} \approx 10\text{ k}\Omega$ and a load of $1\text{ k}\Omega$, replace the resistor with its hybrid- π model, and find the values of R_1 , the voltage gain v_{out}/v_{in} , and the current gain β/γ .

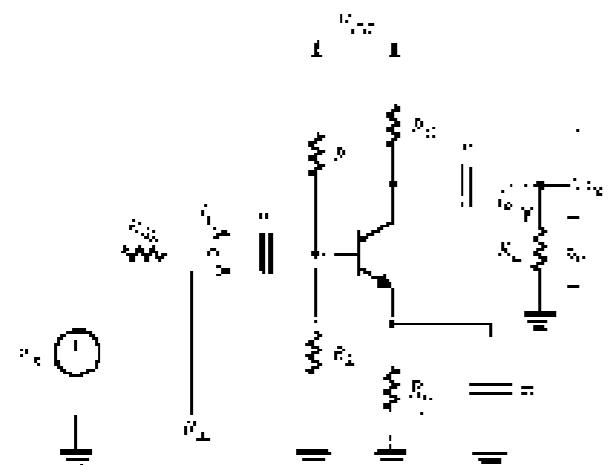


FIGURE P5.133

P5.134 Using the options of Fig. P5.30, design an amplifier to operate between a $10\text{ k}\Omega$ source and a $2\text{ k}\Omega$ load with a gain v_{out}/v_{in} of -8 V/V . The power-supply amplitude is 9 V , i.e., an emitter current of appears merely 2 mA and a current of 1 mA is available that can be voltage-controlled to feed the base, with the bias voltage at 1 V , base bias, one-third of the supply. The transistors available have $\beta = 100$ and $V_T = 100\text{ mV}$. Use standard 5% resistor values Appendix C.

P5.135 A designer, having carried the situation described in Problem 5.133 and evaluating the available gain as being approximately -8 V/V , wishes to explore the possibility of improvement by reducing the loading of the source by the circuit as it is. As in the experiment, the designer varies the resistance level by a factor of approximately $\times R_1 = 1.5\text{ k}\Omega$, $R_2 = 17\text{ k}\Omega$, $R_3 = 3.6\text{ k}\Omega$, and $R_L = 6.8\text{ k}\Omega$ (load and values of 5% tolerance resistors). With $V_{CC} = 9\text{ V}$, $R_s = 10\text{ k}\Omega$, $R_1 = 2\text{ k}\Omega$, $\beta = 100$, and $V_T = 100\text{ mV}$, what does the gain become? Hint: i_B remains constant.

P5.136 Consider the CE amplifier circuit in Fig. 5.60(a). It is required to design the circuit, i.e., find values for R_1 , R_2 , and R_L to meet the following specifications:

- (a) $R_{in} = 5\text{ k}\Omega$.
- (b) The dc voltage drop across R_1 is required to be $< 0.5\text{ V}$ (i.e., the minimum dc voltage gain v_{out}/v_{in} from v_{in} to v_{out} is to be > 1.0 , making it possible, consistent with the requirement that the collector voltage never falls by more than approximately 0.3 V

below the base voltage with the signal between base and emitter being as high as 0.1 V).

Assume that v_{in} is a small-signal source. The ac bias supply $V_{bb} = 5\text{ V}$, and the β of either $\beta = 100$ or a very large Early voltage. Use standard 5%-tolerance values, and specify the value of R_{in} to significant figures. What bias voltage V_{bb} is open-circuit voltage gain down to 0.1 V ? Assume $R_{in} = R_1 = 10\text{ k}\Omega$; what is the overall voltage gain?

P5.137 In the circuit of Fig. P5.134, v_{in} is a small-signal sinusoidal voltage with zero average. The transistor $\beta = 100$.

- (a) Find the value of R_1 to establish about 1 mA collector current, or about 0.5 mA .
- (b) Find R_2 to establish a dc collector voltage of about -5 V .
- (c) For $R_1 = 10\text{ k}\Omega$ and the transistor $\beta = 200$ ($\beta = 100$), draw the small-signal equivalent circuit of the stage and determine its overall voltage gain.

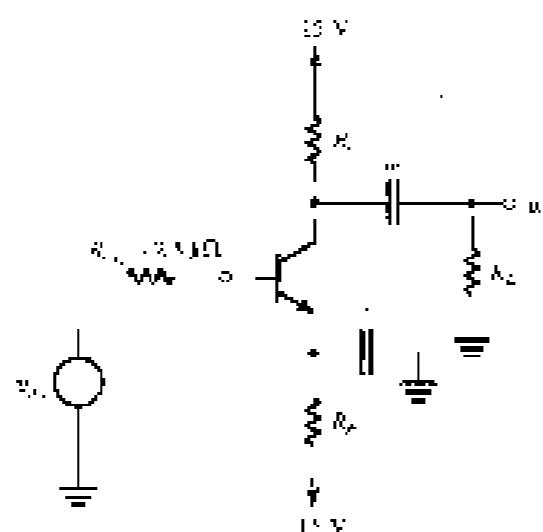


FIGURE P5.137

P5.138 The circuit in Fig. P5.138 consists of two identical stages. The amplifier connects in series, i.e., the terminal the input resistance of the second stage, if r_o considers the load resistance of the first stage.

- (a) For $V_{CC} = 15\text{ V}$, $R_1 = 100\text{ k}\Omega$, $R_2 = 17\text{ k}\Omega$, $R_3 = 3.9\text{ k}\Omega$, $R_L = 5.8\text{ k}\Omega$, and $\beta = 100$, determine the dc collector current, the collector-to-emitter voltage of each transistor.
- (b) Draw the small-signal equivalent circuit of the entire stage, and give the values of all its component. Neglect v_T and r_o .
- (c) Find R_{in} and v_{out}/v_{in} for $R_{in} = 5\text{ k}\Omega$.
- (d) Find R_{in} and v_{out}/v_{in} .
- (e) For $R_2 = 2\text{ k}\Omega$, find v_{out}/v_{in} .
- (f) If the overall voltage gain v_{out}/v_{in} ,

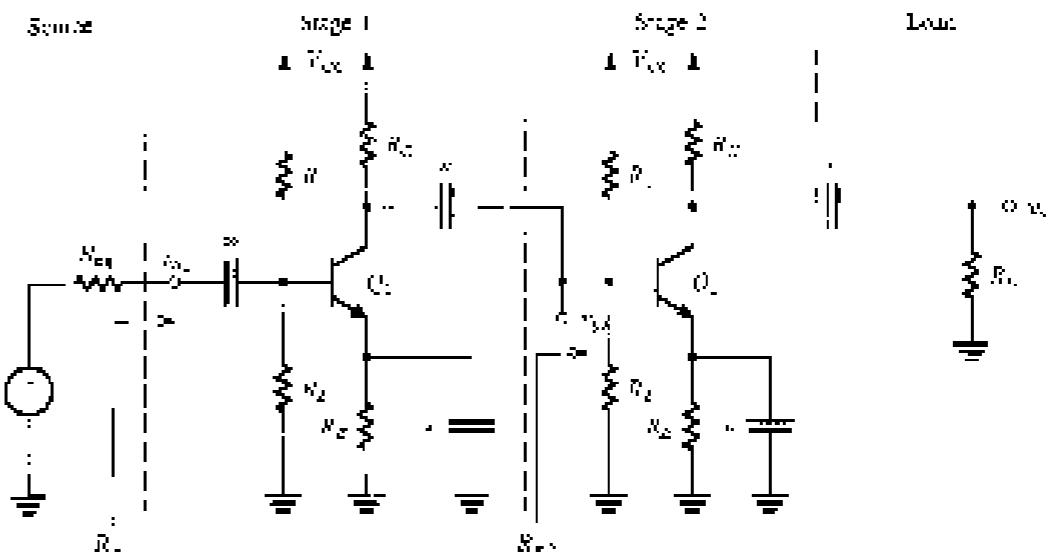


FIGURE P5.138

P5.139 In the circuit of Fig. P5.136, v_{in} is a small-signal sinusoidal voltage. Find R_1 and the gain v_{out}/v_{in} . Assume $\beta = 100$. If the amplitude of the signal v_{in} is to be limited to 1 mV , what is the largest signal at the output? What is the corresponding signal at the output?

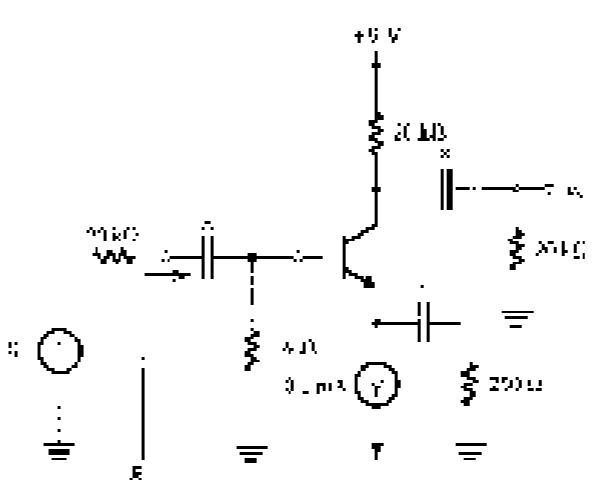


FIGURE P5.139

- (a) What is the ratio of maximum to minimum voltage gain obtainable, R_1 ?
- (b) What value of R_1 could be used to limit the small-signal current to minimum value to 1 mA ?
- (c) If the R_1 source $= 10\text{ k}\Omega$ is used, by what factor is the gain reduced (compared to the case without R_1) for a BJT with a ratio of β ?

S.137 Consider the CE amplifier of Fig. 5.63(a), with $R_b = 10\text{ k}\Omega$, $R_C = 10\text{ k}\Omega$, $V_{CC} = 10\text{ V}$, and $\beta = 100/22$. To what value must I be set in order that the input resistance at E is equal to that of the source ($v_s = 100\text{ mV}$)? What is the resulting voltage v_{o2} across the output to the load? Assume $r_o = 1$.

***S.138 143** Consider the CE amplifier of Fig. 5.63(a) with the collector voltage signal coupled to a $1\text{-k}\Omega$ load resistance through a large capacitor. If all the power supplies are 10 V , the source has a resistance of $50\text{ }\Omega$. Design the circuit so that the amplifier's input resistance is matched to that of the source and the output signal swing is as large as possible with relatively low distortion (v_{o2} limited to 10 mV). Find I and R_C and the overall voltage gain obtained and the output signal swing. Assume $r_o = 1$.

S.141 For the circuit in Fig. PS.141, find the input resistance R_{in} and the voltage gain v_o/v_{in} . Assume that the source provides a small signal v_{in} and that $\beta = 100$.

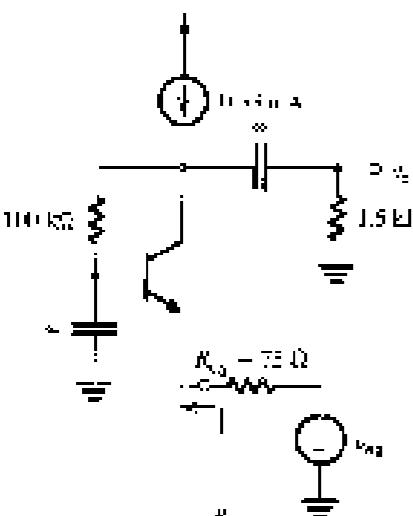


FIGURE PS.141

S.142 Consider the emitter follower of Fig. 5.63(a) with $I = 1\text{ mA}$, $\beta = 100$, $V_{CC} = 10\text{ V}$, $R_C = 100\text{ }\Omega$, $R_E = 20\text{ k}\Omega$, and $R_L = 1\text{ k}\Omega$.

(a) Find R_{in} , v_o/v_{in} , and v_{o2}/v_{in} .

(b) If v_{in} is a sine-wave signal, to what value should its amplitude be limited in order that the transistor remains conducting at all times? For example, if $v_{in} = 0$, is the corresponding capacitance to the base-emitter junction?

(c) If the signal amplitude exceeds the base-emitter junction's reverse bias limit of 0.3 V , what is the corresponding amplitude of v_{o2} ?

(d) Find the open-circuit voltage gain v_o/v_{in} and the output-to-source short-circuit voltage v_{o2} assuming the value of v_{o2}/v_{in} obtained with $R_L = 50\text{ }\Omega$.

S.143 For the emitter follower circuit shown in Fig. PS.143, the BJT need is specified to have β between the range of 40 to 200 on dissolving silicon for the circuit designer. For the two extreme values of β ($\beta = 40$ and $\beta = 200$), find

- (a) I , V_B and R_C
- (b) the input resistance R_{in}
- (c) the voltage gain v_o/v_{in}

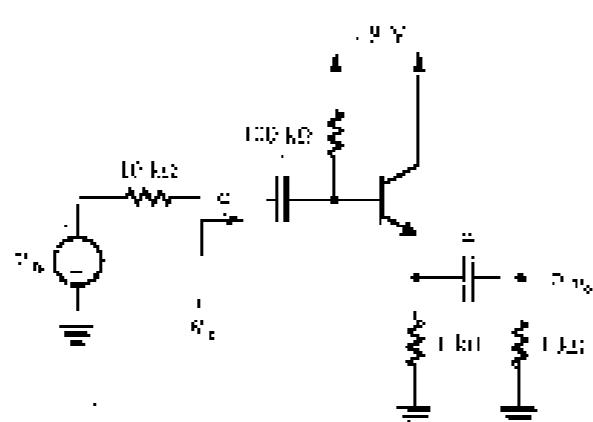


FIGURE PS.143

S.144 For the emitter follower in Fig. PS.144, the signal source is directly coupled to the transistor base. If the dependent current v_{o2}/v_{in} is zero, find the DC collector current. Assume $\beta = 100$. Neglecting r_o , β and R_C , the voltage gain v_o/v_{in} , the current gain i_c/I , and the output resistance R_{out} .

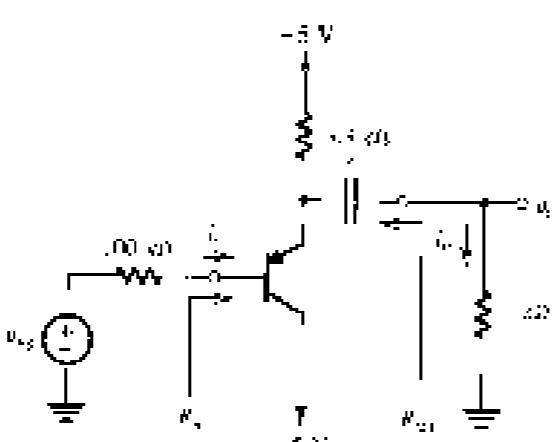


FIGURE PS.144

S.145 In the emitter follower of Fig. 5.63(a), the signal source is directly coupled to the base. Thus, C_{BE} is $\parallel R_b$ is eliminated. The source has $R_s = 10\text{ k}\Omega$ and the component of v_{in} with the transistor $v_{in} = 100\text{ mV}$ and $V_{CC} = 10\text{ V}$. The base current $I = 2.5\text{ mA}$ and $V_{CE} = 3\text{ V}$. What is the input resistance

of the follower? Find the gain v_o/v_{in} without load and with a load of $1\text{k}\Omega$. With the $1\text{k}\Omega$ load connected, find the largest possible negative output signal. What is the largest possible positive output signal? (Assumption: r_o is negligible up to the point that the base-collector junction is forward biased by 0.1 V .)

S.146 The circuit in lower of Fig. 5.63(a), when driven from a $10\text{ k}\Omega$ source, was found to have an open-circuit voltage gain of 3.95 and an output resistance of $200\text{ }\Omega$. The output resistance increased to $300\text{ }\Omega$ when the source resistance was increased to $20\text{ k}\Omega$. Find the overall voltage gain when the follower is driven by a $9\text{ k}\Omega$ source and loaded by $6\text{-m}\Omega$ resistor. Assume $r_o = 0$ for P_{in} .

***S.147** For the circuit in Fig. PS.147, called a homedopped follower:

- (a) Find the dependent current and v_{o2}/v_{in} for $r_o = 10\text{ }\Omega$. By neglecting β , each is 1 model frequency, r_{o2} , and analyze the circuit to determine the input resistance R_{in} and the voltage gain v_o/v_{in} .
- (b) Repeat (a) to the case when capacitor C_2 is over-damped. Compare the results with those obtained in (a) to test the accuracy of bootstraping.

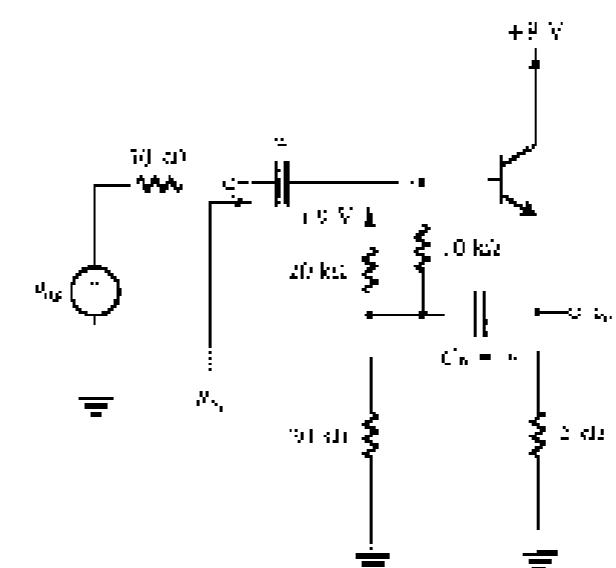


FIGURE PS.147

*****S.148** For the follower circuit in Fig. PS.148 let assume in Q_1 we're $\beta = 50$ and transistor Q_2 are $\beta = 100$, and neglect the effect of r_o (use $V_{BE} = 0.7\text{ V}$).

(a) Find the collector currents of Q_1 and Q_2 . Also, find the DC voltages V_{o1} and V_{o2} .

(b) If a load resistor $R_L = 1\text{k}\Omega$ is connected to the output terminal, find the voltage gain from the base to the emitter of

Q_1 , v_o/v_{in} , and find the input resistance R_{in} looking into the base of Q_1 . (Hint: Consider Q_2 as an open-circuit load by a voltage v_{o2} at its base.)

(c) Replacing Q_2 with its input resistance R_{in2} found in (b), analyze the circuit of emitter follower Q_1 to determine its input resistance R_{in1} and the gain from v_{in} to its emitter, v_o/v_{in} .

(d) If the circuit is fed with a source having a $100\text{ k}\Omega$ resistance, find the transmission to the base of Q_1 , v_o/v_{in} .

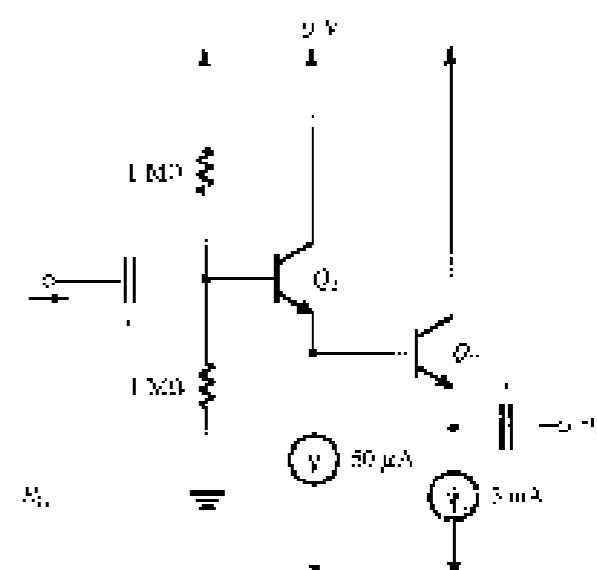


FIGURE PS.148

SECTION 5.6: THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

S.149 An open-circuit is operated at $I_0 = 0.5\text{ mA}$, $V_{CE} = 2\text{ V}$. It has $\beta_0 = 100$, $V_{BE} = 50\text{ mV}$, $r_{o2} = 20\text{ }\Omega$, $C_{BE} = 50\text{ fF}$, $V_{o2} = 0.75\text{ V}$, $r_{o1} = 0.5\text{ }\Omega$, $r_{o2} = 100\text{ }\Omega$. Sketch the complete hybrid-pi model, and specify the values of all its components. Also, find f_T .

S.150 Measurement of v_{o2} at 1 GHz transistors at 500 MHz shows that $I_0 = 2.5\text{ nA}$, $I_0 = 0.7\text{ mA}$, and $I_0 = 1.6\text{ nA}$, $I_0 = 1.0\text{ nA}$. Furthermore, C_{BE} was measured and found to be 0.05 pF . Find f_T for each of the two collector currents listed. What are r_{o1} and r_{o2} ?

S.151 A particular BJT operates at $I_0 = 2\text{ mA}$, $V_{CE} = 1\text{ V}$, $C_{BE} = 10\text{ pF}$, and $\beta = 100$. While v_{in} , I_0 and f_T for this situation?

S.152 For the transistor discussed in Problem S.151, C_{BE} includes a relatively small, dependent-base-emitter conductance of 2 pF .

Transistor (unit)	β	V_{BE0} (mV)	f_T (GHz)	R_s (Ω)	V_{DS0} (mV)	C_{DS} (pF)	f_H (MHz)
(a)	100	(mV/0.1)	(GHz)	100	0	0.7	1
(b)	25			100	0	0.7	4
(c)	100	2.5		100	0.0	0.1	
(d)	10			100	0.0	2	
(e)	0.1			100	0.0	2	
(f)	1			0	40.0	2	
(g)	100			1000	1	0.5	80

If the device is operated at $I_C = 0.2 \text{ mA}$, what does α/β become?

*5.153 A current-gain-frequency BJT has f_T of 10 GHz, $C_{DS} = 0.1 \text{ pF}$ when operated at $I_C = 0.2 \text{ mA}$. What is C_{DS} in this situation? Also, find α , $\beta = 100$, β/α and β/β .

*5.154 From RBJ values, unity-gain bandwidth is 1.4 GHz and $\beta = 200$, at what frequency does the midband β/α become 0.1? What is f_H ?

*5.155 At a sufficiently high frequency, measurement of the complex input impedance of a $n-p-n$ junction-gated varactor and an empty junction diode approximating β_0 . For what frequency is the $|Z_{in}|$ of β_0 in such an estimate of β_0 equal to within 10% of the condition that $r_i < r_o/10$? Neglect C_{DS} .

*5.156 Calculate the two series above for parts (a) through (g), under the conditions indicated. Neglect r_i .

SECTION 5.9: FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

*5.157 A designer wishes to investigate the effects of changing the bias current (I_B) on the midband β/α and high-frequency response of the CE amplifier circuit, as in Examples 5.18, 5.19, 5.20, 5.21, or 5.22, but with β_0 and f_T chosen unchanged at 100 A and 800 MHz, respectively. To do so, the input voltage is nearly unchanged, the resistor values R_E and R_C are 1 k Ω , by a factor of 2, to 10 k Ω and 4 k Ω , respectively. Assume $r_o = 50 \text{ M}\Omega$ and recall that $V_A = 100 \text{ V}$ and that the term $\alpha = 1 - \beta^2$. As before, the amplifier is fed with a source having $R_{in} = 5 \text{ k}\Omega$ and feeds a load $R_L = 5 \text{ k}\Omega$. Find the new values of β_0 , f_H , and the midband product, $|\beta_0|f_H$. Comment on the result. Note that the price paid for whatever improvement in performance is achieved is an increase in power. By what factor does the power P_o increase?

*5.158 The purpose of this problem is to investigate the high-frequency response of the CE amplifier when it is fed with a relatively large source resistance R_{in} . Refer to the amplifier in Fig. 5.71(a) and to a high-frequency equivalent circuit

model and the analysis shown in Fig. 5.72. Let $R_{in} \gg R_{in}$, β_0 of Part 5.157, $\beta_0/\beta_0' = 1$, and $\beta_0 R_V C_{in} \gg C_{in}$.

Under these conditions, show that

(a) the midband gain $A_{vB} = -\beta_0 R_C / R_{in}$,

(b) the upper 3-dB corner frequency $f_H = 1/(2\pi C_{in} R_{in})$,

(c) the gain-bandwidth product $A_{vB} f_H = 1/(2\pi C_{in} R_{in})$.

Assume this approximate value of the gain-bandwidth product for the case $R_{in} = 25 \text{ k}\Omega$ and $C_{in} = 1 \text{ pF}$. Now, if the transistor is biased at $I_C = 1 \text{ mA}$ and has $\beta = 100$, and the midband gain and f_H for the two cases, $R_{in}' = 25 \text{ k}\Omega$ and $R_{in} = 2.5 \text{ k}\Omega$. On the same coordinates, sketch back plots for the gain margin and ω_c (corner frequency) for the two cases. What f_H is close to when the gain is unity? What value of R_{in} corresponds?

*5.159 Consider the common-emitter amplifier of Fig. 5.159 under the following conditions: $R_{in} = 5 \text{ k}\Omega$, $V_{in} = 10 \text{ V}$, $R_E = 22 \text{ k}\Omega$, $\beta_0 = 100$, $R_C = 4.7 \text{ k}\Omega$, $R_L = 5.6 \text{ k}\Omega$, $V_{cc} = 5 \text{ V}$. The drain current can be shown to be $I_D = 0.3 \text{ mA}$, at which $\beta_0 = 120$, $r_o = 400 \text{ k}\Omega$, and $r_i = 50 \text{ M}\Omega$. Find the input resistance R_{in} and the midband gain A_{vB} . The transistor is specified to have $f_T = 300 \text{ MHz}$ and $C_{DS} = 1 \mu\text{F}$ at the upper 3-dB frequency f_H .

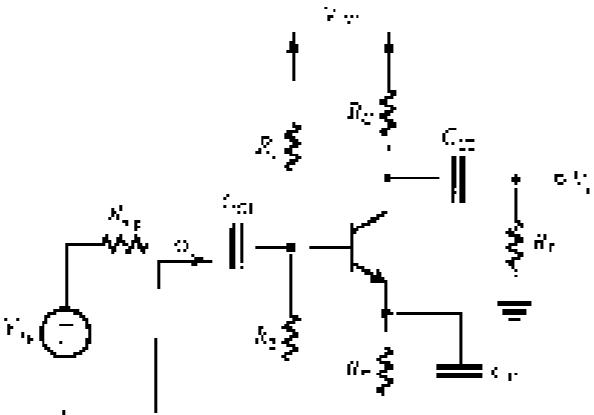


FIGURE P5.159

*5.160 Investigate the CE amplifier circuit in Fig. P5.150, $R_{in} = 10 \text{ k}\Omega$, $R_E = 38.1 \text{ k}\Omega$, $R_C = 27 \text{ k}\Omega$, $R_L = 1.73 \text{ k}\Omega$, and $\beta_0 = 100$. The collector current is 0.4 mA, $\beta = 200$, $\beta_0 = 100$, and $C_{in} = 0.8 \text{ pF}$. Neglect the effect of r_o on r_i and the load voltage gain on the upper 3-dB frequency f_H .

*5.161 The amplifier shown in Fig. P5.61 has $R_{in} = R_E = 1 \text{ k}\Omega$, $R_C = 47 \text{ k}\Omega$, $\beta = 100$, $C_{in} = 0.2 \text{ pF}$, and $f_T = 600 \text{ MHz}$.

(a) Find the drain-to-source current of the converter.

(b) Find r_i and r_o .

(c) Neglect r_o and the midband voltage gain from r_i to r_o to neglect the effect of r_o on r_i . What is the ratio C_{in}/C_{DS} that makes these contributions to the drain-to-source of r_i equal?

(d) Use the gain obtained in (c) to find the equivalent of R_{in} that is shorted across r_i . Hence find R_{in} .

(e) Find the overall gain of the circuit.

(f) Find f_H .

(g) Find f_U .

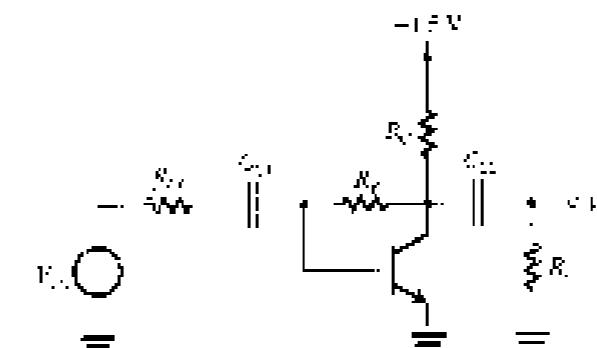


FIGURE P5.161

*5.162 Refer to Fig. 5.62. Utilizing the RBJ high-frequency hybrid model with $r_i = 0$ and $r_o = \infty$, derive an expression for Z_{in} as a function of r_o and C_{in} . Find the frequency at which the impedance has a phase angle of 45° for the case in which the BJT has $f_T = 400 \text{ MHz}$ and the bias current is relatively high. What is the frequency when the bias current is reduced to 1/10? $C_{in} = C_{DS} = 1 \mu\text{F}$. Assume $\alpha = 1$.

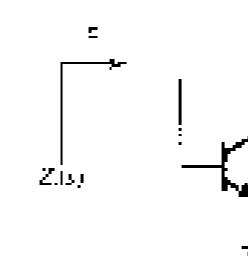


FIGURE P5.162

*5.163 For the amplifier in Fig. P5.166, whose component values were specified in Problem 5.159, let $V_{cc} = 5 \text{ V}$, $R_E = 1 \text{ k}\Omega$, and $C_{in} = 10 \mu\text{F}$. Find the break frequencies f_B , f_H , and f_U .

existing from C_{in} , C_{DS} and C_{in} respectively. Note that R_{in} has to be taken into account in evaluating r_i . Hence, estimate the value of the lower 3-dB frequency f_L .

*5.164 For the amplifier described in Problem 5.163, design the coupling and bypass capacitors for a low 3-dB frequency of 100 Hz. Design ω_c and the combination of each of C_{in} and C_{DS} to determine f_L is only 2%.

*5.165 Consider the circuit of Fig. P5.69. For $R_{in} = 10 \text{ k}\Omega$, $R_E = r_i$, $V_{in} = 0 \text{ V}$, $r_i = 100 \text{ M}\Omega$, $r_o = 100 \text{ k}\Omega$, $\beta = 100$, and $R_C = 1 \text{ M}\Omega$, what is the ratio C_{in}/C_{DS} that makes these contributions to the drain-to-source of r_i equal?

*5.166 For the common-emitter amplifier of Fig. P5.164, $r_i = 1 \text{ k}\Omega$, and r_o , and assume the current source to be ideal.

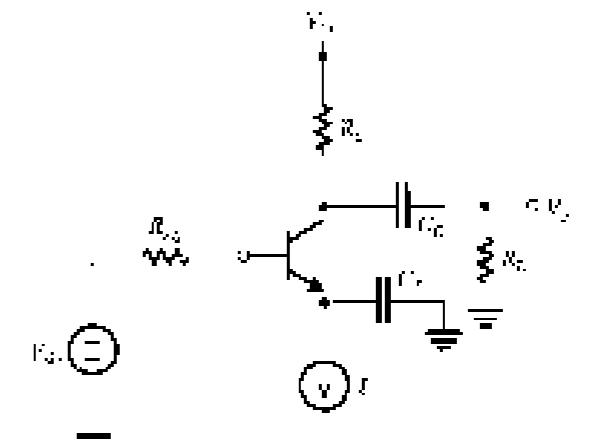


FIGURE P5.166

(a) Derive an expression for the midband gain.
(b) Derive expressions for the break frequency as caused by C_{in} and C_{DS} .

(c) Give an expression for the amplifier voltage gain $1/A$.

(d) For $R_{in} = R_E = R_C = 10 \text{ k}\Omega$, $\beta = 100$, and ω_c as the midband gain.

(e) Select values for C_{in} and C_{DS} to place the two break frequencies a decade apart and to obtain a low 3-dB frequency of 100 Hz while using the total capacitance.

(f) Sketch a Bode plot for the gain magnitude, to estimate the frequency at which the gain becomes 0 dB.

(g) Evaluate the power gain at 100 Hz.

*5.167 The RBJ common-emitter amplifier of Fig. P5.167 includes a β/α Miller degeneration feedback R_f .

(a) Assuming $\alpha = 1$, neglecting r_i and r_o , and assuming the current source to be ideal, derive an expression for the small-signal voltage gain A , i.e., $A = V_o/V_{in}$, that applies in the midband and the low-frequency band. Hence find the midband gain A_M and the lower 3-dB frequency f_L .

- (b) Show that increasing R_s reduces the magnitude of A_{vD} by a $\sqrt{2}$ factor. What is this factor?
 (c) Show that increasing R_s reduces f_T by the same factor as in (b) and thus also reduces R_s to obtain a gain of 10 dB at the double pole.
 (d) For $I = 1 \text{ mA}$, $V_{ce} = 10 \text{ Vdc}$, and $C_L = 10 \text{ pF}$, find the average power dissipation in the inverter.

5.170 Design a n-channel inverter to operate from a 1.5-V supply. With the input connected to $V_{DD} = 1.5 \text{ V}$, supply current I_{DD} is also equal to I_D . The total power dissipation should be $< 0.5 \text{ mW}$, and forced β should be 10. Use $V_{GS} = 0.7 \text{ V}$ and $V_{DS} = 0.1 \text{ V}$.

5.171 For the circuit in Fig. 5.1-1, consider the two voltage clippings of 0.5 V and 0.2 V to X and Y are combination, and find the output voltage for each combination. Tabulate your results. How many input combinations are there? What happens when any input is high? What happens when both inputs are low? This is a logic gate that implements the NOR function: $Z = X + Y$. This logic gate structure is called, historically, Resistor-Transistor Logic (RTL).

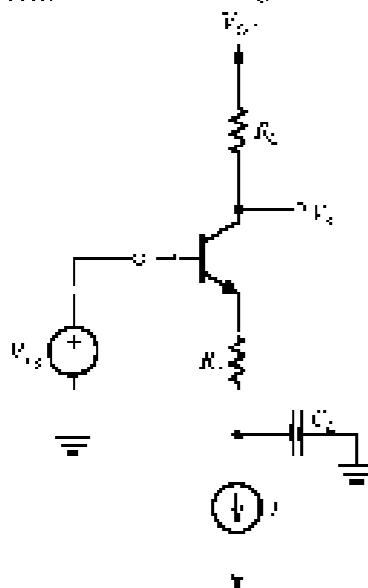


FIGURE PS.167

SECTION 5.10: THE BASIC BIT DIGITAL LOGIC INVERTER

5.168 Consider the inverter shown in Fig. 5.74. In Exercise 5.12, the following expression is derived for V_{out} when the inverter is driving M identical inverters:

$$V_{out} = V_{DD} - R_s \frac{V_{DD} - V_{out}}{R_s + R_o/M}$$

For the same component values used in the analysis in the text (i.e., $V_{DD} = 5 \text{ V}$, $R_s = 1 \text{ k}\Omega$, $R_o = 10 \text{ k}\Omega$, and $V_{out} = 0.7 \text{ V}$), find the minimum value of M that will still guarantee a high output voltage V_{out} of at least 1 V. Assume $\beta = 50$ and $V_{GS} = 0.7 \text{ V}$.

5.169 The purpose of this problem is to find the power dissipation of the inverter shown in Fig. 5.74 in each of its two states. Assume that the component values are as given in the text (i.e., $V_{DD} = 5 \text{ V}$, $R_s = 1 \text{ k}\Omega$, $R_o = 10 \text{ k}\Omega$, and $V_{out} = 0.7 \text{ V}$). With the input v_{in} at 0.2 V, the transistor is cut off. Let the inverter be driving 10 identical inverters. Find the total current i_s supplied by the inverter and hence the power dissipation in R_s .

- (b) With the input high and the transistor saturated, find the power dissipation in the inverter, neglecting the power dissipated in the base circuit.

(c) Use the results of (a) and (b) to find the average power dissipation in the inverter.

5.173 Consider the inverter circuit of Fig. 5.74 with a load capacitor C connected between the output node and ground. We wish to find the contribution of C to the high-to-low delay time of the inverter, t_{H-L} (Fig. 1.35). Toward that end, assume that prior to $t = 0$, the transistor is cut off and saturated and $v_o = V_{DD} - V_{out}$. Then, at $t = 0$, let the input fall to the "low" level, and assume that the transistor turns on instantaneously. Note that neglecting the turn-off time of a saturated transistor is an unrealistic assumption, but one that will help us concentrate on the effect of C . Now, with the transistor cut off, the capacitor C will charge through R_s , and the output voltage will rise exponentially from $V_{DD} - V_{out}$ to $V_{out} = V_{DD}$. Find an expression similar to $v_o(t)$. Calculate the value of t_{H-L} , which in this case is the time for v_o to increase by $(V_{DD} - V_{out})/2$. Use $V_{DD} = 5 \text{ V}$, $V_{out} = 0.2 \text{ V}$, $R_s = 1 \text{k}\Omega$, and $C = 10 \text{ pF}$. (Hint: The step response of RC circuits is reviewed in Section 1.7 and in greater depth in Appendix E.)

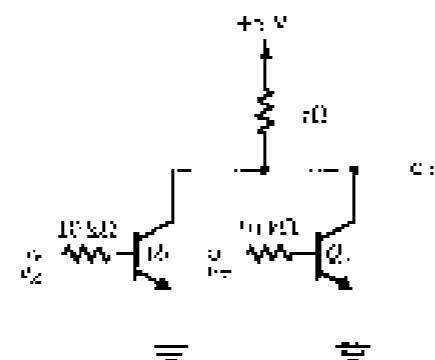


FIGURE PS.171

5.172 Consider the inverter of Fig. 5.74 with a load capacitor C connected between the output node and ground. We wish to find the contribution of C to the low-to-high delay time of the inverter, t_{L-H} . (For low-current applications of inverter delays, refer to Fig. 1.35.) Toward that end, assume that prior to $t = 0$, the transistor is cut off and saturated and $v_o = V_{DD} - V_{out}$. Then, at $t = 0$, let the input fall to the "low" level, and assume that the transistor turns on instantaneously. Note that neglecting the turn-off time of a saturated transistor is an unrealistic assumption, but one that will help us concentrate on the effect of C . Now, with the transistor cut off, the capacitor C will charge through R_s , and the current voltage will rise exponentially from $V_{DD} - V_{out}$ to $V_{out} = V_{DD}$. Find an expression similar to $v_o(t)$. Calculate the value of t_{L-H} , which in this case is the time for v_o to increase by $(V_{DD} - V_{out})/2$. Use $V_{DD} = 5 \text{ V}$, $V_{out} = 0.2 \text{ V}$, $R_s = 1 \text{k}\Omega$, and $C = 10 \text{ pF}$. (Hint: The step response of RC circuits is reviewed in Section 1.7 and in greater depth in Appendix E.)

PART II

ANALOG AND DIGITAL INTEGRATED CIRCUITS

CHAPTER 6

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CHAPTER 7

Differential and Multistage Amplifiers 687

CHAPTER 8

Feedback 791

CHAPTER 9

Op-Amp and Data-Converter Circuits 871

CHAPTER 10

CMOS Logic Circuits 949

INTRODUCTION

Having studied the major electronic devices (the MOSFET and the BJT) and their basic circuit applications, we are now ready to consider the design of more complex analog and digital integrated circuits and systems. The five chapters of Part II are intended for this purpose. They provide a carefully selected set of topics suitable for a second course in electronics. Nevertheless, the flexibility inherent in this book should permit replacing some of the topics included with a selection from the special topics presented in Part III. As well, if desired, Chapter 10 on CMOS logic circuits can be studied at the beginning of the course.

Study of Part II assumes knowledge of MOSFET and BJT characteristics, models, and basic applications (Chapters 4 and 5). To review and consolidate the material and differences between the two devices, Section 6.2 with its three tables (6.1–6.3) is a must read. The remainder of Chapter 6 provides a systematic study of the circuit building blocks utilized in the design of analog IC's. In each case, both low-frequency and high-frequency operation are considered. Chapter 7 continues this study, concentrating on the most widely used configuration in analog IC design, the differential pair. It concludes with a section on multistage amplifiers. In both chapters, MOSFET circuits are presented first, simply because the MOSFET is now the device that is used in over 90% of integrated circuits. Bipolar transistor circuits are presented with the same depth but presented second and, of course, more briefly.

A detailed study of the pivotal topic of feedback is presented in Chapter 8. Such a study is essential for the proper application of feedback in the design of amplifiers, to effect desirable properties such as more precise gain values, and to avoid anomalies such as instability. The analog material of Part II is integrated together in Chapter 9 by the study of op-amp circuits. Chapter 9 also presents an introduction to analog-to-digital and digital-to-analog converters, and thus serves as a bridge to the study of CMOS digital logic circuits in Chapter 10. Here again we concentrate on CMOS because it represents the technology in which the vast majority of digital systems are implemented.

The second course, based on Part II, is intended to prepare the reader for the practice of electronic design, and, if desired, to provide an advanced course on analog and digital IC design.

CHAPTER 6

Single-Stage Integrated-Circuit Amplifiers

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INTRODUCTION

Having studied the two major transistor types, the MOSFET and the BJT, and their basic discrete-circuit amplifier configurations, we are now ready to begin the study of integrated-circuit amplifiers. This chapter and the next are devoted to the design of the basic building blocks of IC amplifiers.

In this chapter, we begin with a brief section on the design philosophy of integrated circuits, and how it differs from that of discrete circuits. Throughout this chapter, MOS and

Bipolar circuits are presented side-by-side, which allows a certain economy in presentation and, more importantly, provides an opportunity to compare and contrast the two circuit types. Toward that end, Section 6.2 provides a comprehensive comparison of the attributes of the two transistor types. This should serve both as a review as well as a guide to very interesting similarities and differences between the two devices.

Following the study of IC biasing, the various configurations of single-stage IC amplifiers are presented. This material builds on the study of basic discrete-amplifier configurations in Sections 4.7 and 5.7.

In addition to classical single-stage amplifiers, we also study some configurations that utilize two amplifying transistors. These "compound circuit topologies" are usually treated as single-stage amplifiers (for reasons that will become clear later).

Current mirrors and current-source circuits play a major role in the design of IC amplifiers, where they serve both as biasing and load elements. For this reason, we return to the subject of current mirrors later in the chapter and consider some of their advanced (and interesting) forms.

Although CMOS circuits are the most widely used at present, there are applications in which the addition of bipolar transistors can result in superior performance. Circuits that combine NMOS and bipolar transistors, in a technology known as BiMOS or BiCMOS, are presented at appropriate locations throughout the chapter. The chapter concludes with SPICE simulation examples.

6.1 IC DESIGN PHILOSOPHY

Integrated-circuit fabrication technology (Appendix A) places constraints on—and provides opportunities for—the circuit designer. Thus, while chip area considerations dictate that large- and even moderate-value resistors are to be avoided, constant-current sources are readily available. Large capacitors, such as those we used in Sections 4.7 and 5.7 for signal coupling and bypasses, are not available to be used, except perhaps as components external to the IC chip. Even then, the number of such capacitors has to be kept to a minimum; otherwise the number of chip terminals and hence its cost increase. Very small capacitors, in the picofarad and fraction of a picofarad range, however, are easy to fabricate in IC MOS technology and can be combined with MOS amplifiers and MOS switches to realize a wide range of signal processing functions, both analog (Chapter 12) and digital (Chapter 14).

As a general rule, in designing IC MOS circuits, one should strive to realize as many of the functions required as possible using MOS transistors only and, when needed, small MOS capacitors. MOS transistors can be sized; that is, their W and L values can be selected, to fit a wide range of design requirements. Also, arrays of transistors can be combined for, more generally, more easily to have desired characteristics to realize such useful circuit building blocks as current mirrors.

At this juncture, it's useful to mention that to pack a larger number of devices on the same IC chip, the trend has been to reduce the device dimensions. At the time of this writing (2003), CMOS process technologies capable of producing devices with a 0.1- μm minimum channel length are in use. Such small devices need to operate with dc voltage supplies close to 1 V. While low-voltage operation can help to reduce power dissipation, it poses a host of challenges to the circuit designer. For instance, such MOS transistors must be operated with overdrive voltages of only 0.2 V or less. In our study of MOS amplifiers, we will make frequent comments on such issues.

The MOS-amplifier circuits that we will study will be designed almost entirely using MOSFETs of both polarities—that is, NMOS and PMOS—as are readily available in CMOS

technology. As mentioned earlier, CMOS is currently the most widely used IC technology for both analog and digital as well as combined analog and digital (or mixed-signal) applications. Nevertheless, bipolar integrated circuits still offer many exciting opportunities to the analog design engineer. This is especially the case for general-purpose circuit packages, such as high-quality op-amps that are intended for assembly on printed-circuit (pc) boards (as opposed to being part of a system-on-chip). As well, bipolar circuits can provide much higher output currents and are favored for certain applications, such as in the automotive industry, for their high reliability under severe environmental conditions. Finally, bipolar circuits can be combined with CMOS in innovative and exciting ways.

6.2 COMPARISON OF THE MOSFET AND THE BJT

In this section we present a comparison of the characteristics of the two major electronic devices: the MOSFET and the BJT. To facilitate this comparison, typical values for the important parameters of the two devices are first presented.

6.2.1 Typical Values of MOSFET Parameters

Typical values for the important parameters of NMOS and PMOS transistors fabricated in a number of CMOS processes are shown in Table 6.1. Each process is characterized by its minimum allowed channel length, L_{min} ; thus, for example, in a 0.18- μm process, the smallest transistor has a channel length $L = 0.18 \mu\text{m}$. The technologies presented in Table 6.1 are in descending order of channel length, with that having the shortest channel length being the most modern. Although the 0.8- μm process is now obsolete, its data are included to show trends in the values of various parameters. It should also be mentioned that although Table 6.1 stops at the 0.18- μm process, in the Line of Ericssson (LOE), a 0.13- μm fabrication process is commercially available and a 0.09- μm process is in the advanced stages of development. The 0.18- μm process, however, is currently the most popular and the one for which data are widely available. An important caution, however, is in order. The data presented in Table 6.1 do not pertain to any particular commercially available process. Accordingly, these generic data are not intended for use in an actual IC design; rather, they allow trends and, as we shall see, help to illustrate design trade-offs as well as enable us to work out design examples and problems with parameter values that are as realistic as possible.

TABLE 6.1 Typical Values of CMOS Device Parameters

Parameter	0.8 μm		0.5 μm		0.25 μm		0.18 μm	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$I_{DSS} (\mu\text{A})$	15	15	9	9	6	6	4	4
$C_{ox} (\text{fF}/\mu\text{m}^2)$	1.6	2.3	3.8	3.8	5.9	5.9	8.6	8.6
$\mu (\text{cm}^2/\text{V}\cdot\text{s})$	500	250	500	180	450	160	150	100
$\mu C_{ox} (\text{fA}/\text{V}^2)$	125	58	100	48	95	95	395	36
$V_{TH} (\text{V})$	-0.7	-0.7	-0.7	-0.8	-0.41	-0.52	-0.18	-0.45
$V_{GS} (\text{V})$	5	5	3.3	3.3	2.5	2.5	1.8	1.8
$V_{DS} (\text{V}/\mu\text{s})$	25	20	20	20	5	6	5	6
$C_{gd} (\text{fF}/\mu\text{m})$	0.2	0.3	0.4	0.4	0.9	0.5	0.37	0.30

As indicated in Table 6.1, the trend has been to reduce the junction allowable current density. This trend has been motivated by the desire to pack more transistors on a chip as well as to operate at higher speeds or, in analog terms, over wider bandwidths.

Observe that the oxide thickness, t_{ox} , scales down with the channel length, reaching 4 nm for the 0.18- μm process. Since the oxide capacitance, C_{ox} , is inversely proportional to t_{ox} , we see that C_{ox} increases as the technology scales down. The surface mobility μ_s decreases as the technology minimum feature size is decreased, and μ_s decreases much faster than ρ_{sd} . As a result, the ratio μ_s/ρ_{sd} has been decreasing with each generation of technology. Falling from about 0.5 for older technologies to 0.2 or so for the newest ones. Despite the reduction of μ_s and ρ_{sd} , the transconductance parameter $k'_t = \mu_s C_{ox}$ and $k'_f = \mu_s C_{ox}$ have been steadily increasing. As a result, modern short-channel devices achieve required levels of bias current at lower supply voltages. As well, they achieve higher current densities at a given voltage.

Although the magnitudes of the threshold voltages V_{th} and V_{gs} have been decreasing with L_{min} from about -0.7 to -0.8 V to 0.4 to 0.5 V, the reduction has not been as large as that of the power supply V_{DD} . The latter has been reduced dramatically, from 5 V for older technologies to 1.8 V for the 0.18- μm process. This reduction has been necessitated by the need to keep the electric fields in the smaller devices from reaching very high values. Another reason for reducing V_{DD} is to keep power dissipation as low as possible given that the IC chip now has a much larger number of transistors.

The fact that in modern short-channel CMOS processes (V_{DD}) has become a much larger proportion of the power supply voltage poses a serious challenge to the circuit design engineer. Recalling that $|V_{GS}| = |V_g - V_{DD}|$, where V_g is the overdrive voltage, to keep $|V_{GS}|$ reasonably small, V_{DD} for modern technologies is usually in the range of 0.2 V to 0.5 V. To appreciate this point further, recall that to operate a MOSFET in the saturation region, V_{GS} must exceed $|V_{DD}|$; thus, to be able to have a number of devices stacked between the power supply rails in a regime in which V_{DD} is only 1.8 V or lower, we need to keep V_{DD} as low as possible. We will shortly see, however, that operating at a low V_{DD} has some drawbacks.

Another significant design undesirable feature of modern submicron CMOS technologies is the short-channel conductance effect, very pronounced. As a result, V'_d has been steadily decreasing, which combined with the decreasing values of L_{min} has caused the Early voltage $V_A = V'_d L$ to become very small. Correspondingly, short-channel MOSFETs exhibit low output resistances.

From our study of the MOSFET high-frequency equivalent circuit model in the saturation mode in Section 4.8 and the high-frequency response of the common-source amplifier in Section 4.9, we know that two major MOSFET capacitances are C_{ds} and C_{gs} . While C_{ds} has an overlap component, C_{ov} , it is entirely an overlap capacitance. Both C_{ds} and the overlap component of C_{gs} are almost equal and are denoted C_{ov} . The last line of Table 6.1 provides the value of C_{ov} per micron of gate width. Although the normalized C_{ov} has been staying more or less constant with the reduction in L_{min} , we will shortly see that the shorter devices exhibit much higher operating speeds and wider amplitude bandwidths than the longer devices. Specifically, we will, for example, see that f_T for a 0.25- μm NMOS transistor can be as high as 10 GHz.

6.2.2 Typical Values of ICBT Parameters

Table 6.2 provides typical values for the major parameters that characterize integrated-circuit bipolar transistors. Data are provided for devices fabricated in two different processes. The

¹At the present time, chip power dissipation has become a very serious issue, with some of the recently reported ICs dissipating as much as 100 W. As a result, an important concern in a system designer is what a thermal power-budget design.²

TABLE 6.2 TYPICAL PARAMETERS FOR ICBT

Parameter	Standard High-Voltage Process		Advanced Low-Voltage Process	
	npn	Laterally	npn	Laterally
$A_V (\text{m}^2)$	500	500	2	2
$I_S (\text{A})$	5×10^{-10}	2×10^{-11}	6×10^{-15}	6×10^{-17}
$R_0 (\text{mA})$	200	50	100	30
$V_t (\text{V})$	130	50	35	30
$V_{BE} (\text{V})$	50	60	4	18
f_T	0.25 μm	50 μs	10 μs	650 μs
C_{ds}	1 pF	0.3 pF	3 pF	1.15 pF
C_{ov}	0.5 pF	1 pF	5 pF	5.5 pF
$r_s (\Omega)$	200	200	400	200

Source: Goss et al. (2003), as modified.

standard old process, known as the "high-voltage process," and an advanced, modern process referred to as a "low-voltage process." For each process we show the parameters of the standard npn transistor and those of a special type of pnp transistor known as a lateral pnp opposed to vertical as in the conventional pnp (see Appendix A). In this regard we should mention that a major drawback of standard bipolar integrated-circuit fabrication processes has been the lack of pnp transistors of a quality equal to that of the npn devices. Rather, there are a number of pnp implementations for which the lateral pnp is the most economical to fabricate. Unfortunately, however, as should be evident from Table 6.2, the lateral pnp has characteristics that are much inferior to those of the npn. Note in particular the lower value of β and the much larger value of the forward transit time, t_f , that determines the emitter-base transition capacitance C_{eb} and, hence, the transistor speed of operation. The data in Table 6.2 can be used to show that the unity-gain frequency of the lateral pnp is two orders of magnitude lower than that of the npn transistor fabricated in the same process. Another important difference between the lateral pnp and the corresponding npn transistor is the value of collector current at which their β values reach their maximum. For the high-voltage process, for example, this current is in the tens of microamperes range for the pnp and in the milliampere range for the npn. On the positive side, the problem of the lack of high-quality pnp transistors has spurred analog circuit designers to come up with highly innovative circuit topologies that either minimize the use of pnp transistors or eliminate the dependence of circuit performance on that of the pnp. We shall encounter some of these ingenious circuits later in this book.

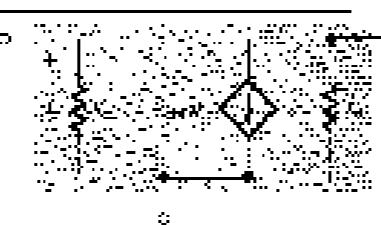
The dramatic reduction in speed we achieved in the advanced low-voltage process should be evident from Table 6.2. As a result, the collector current I_C also has been reduced by about three orders of magnitude. Here we should note that the base width, W_B , achieved in the advanced process is on the order of 0.1 μm , as compared to a few micrometers in the standard high-voltage process. Note also the dramatic increase in speed, for the low-voltage npn transistor, $f_T = 10 \mu\text{s}$ as opposed to 0.3 μs in the high-voltage process. As a result, f_T for the modern npn transistor is 10 GHz to 25 GHz, as compared to the 100 MHz to 100 MHz achieved in the high-voltage process. Although the early voltage, V_A , for the modern process is lower than its value in the old high-voltage process, it is still reasonably high at 35 V. Another feature of the advanced process—something that is not obvious from Table 6.2—is that β for the npn reaches at a collector current of 50 μA or so. Finally, note that ω_c in marine implies npn transistors

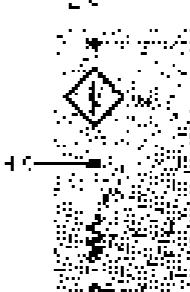
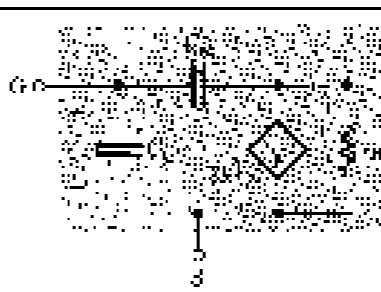
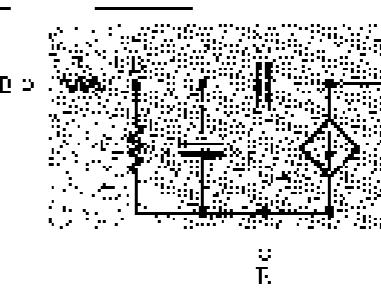
fabricated in the low-voltage process break down at collector-emitter voltages of 8 V, as compared to 50 V or so for the high-voltage process. Thus, while circuits designed with the standard high-voltage process utilize power supplies of ± 15 V (e.g., in commercially available packages like the 741 type), the total power-supply voltage utilized with modern bipolar devices is 5 V (or even 1.1 V to achieve compatibility with some of the submicron CMOS processes).

6.2.2 Comparison of Important Characteristics

Table 6.3 provides a compilation of the important characteristics of the NMOS and the pnp transistors. The material is presented in a manner that facilitates comparison. In the following, we provide comments on the various items in Table 6.3. As yet, a number of numerical examples and exercises are provided to illustrate how the wealth of information in Table 6.3 can be put to use. Before proceeding, note that the PMOS and the pnp transistors can be compared in a similar way.

TABLE 6.3 Comparison of the MOSFET and the EJT

Circuit Symbol	NMOS		pnp	
To Operate in the Active Mode, Two Conditions Have To Be Satisfied	(1) Induce a channel: $v_{GS} \geq V_{GS} - V_t = 0.2 - 0.7$ V Let $v_{GS} = V_t + v_{GS}$	(1) Turned-on EBJ: $v_{BE} \geq V_{BE(on)} - V_{BE(on)} \approx 3.5$ V	(2) Reverse-bias CBI: $v_{CE} < V_{EC(on)} - V_{EC(on)} \approx 0.6$ V or equivalently, $v_{DS} \geq V_{DS(on)} - V_{DS(on)} = 0.2 - 0.5$ V	
Current-Voltage Characteristics in the Active Region	$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_{GS})^2 \left(1 + \frac{2v_{DS}}{V_A}\right)$ $= \frac{1}{2}\mu_n C_{ox} \frac{W}{L} v_{GS} \left(1 + \frac{2v_{DS}}{V_A}\right)$	$i_C = I_D e^{-\frac{v_{BE}}{V_T}} \left(1 + \frac{2v_{CE}}{V_A}\right)$		
Low-Frequency Hybrid- π Model				

NMOS		pnp	
Low-Frequency T Modes	D-C	C-C	E-C
			
Transconductance g_m	$i_D = I_D (V_{GS}/2)$ $g_m = (\mu_n C_{ox} W/L) i_{DS}$	$i_C = I_C (V_{CE}/2)$	
Output Resistance r_o	$r_o = v_{DS}/i_{DS} = \frac{V_A L}{I_D}$	$r_o = v_{CE}/i_C$	
Intrinsic Gain $A_I = g_m R_o$	$A_I = V_A / (V_{GS}/2)$ $A_0 = \frac{2V_A L}{V_{GS}}$ $A_p = \frac{V_A \sqrt{2} \mu_n C_{ox} W L}{\sqrt{I_D}}$	$A_0 = V_A / V_T$	
Output Resistance with Source [Emitter] Grounded	$r_o = R_o / g_m$		
High-Frequency Model			

(Continued)

TABLE 6.4 Comparison of the MOSFET and the BJT (continued)

	NMOS	BJT
Capacitances	$C_{ds} = \frac{2}{3}WL C_{ox} + WL_{ov}C_{ox}$ $C_s = WL_{ov}C_{ox}$	$C_{ds} = C_{ds} + C_{ds}$ $C_{ds} = C_{ds} \beta_{FE}$ $C_{ds} = \lambda C_{ds}$ $C_{ds} = C_{ds} \left(\frac{V_{DS}}{1 + V_{DS}} \right)^2$
Transition Frequency	$f_T = \frac{\beta_{FE}}{2\pi(C_{ds} + C_{ds})}$ For $C_{ds} \gg C_{ds}$ and $C_{ds} = \frac{2}{3}WL C_{ox}$, $f_T = \frac{1.5\beta_{FE}\gamma}{2\pi L}$	$f_T = \frac{\beta_{FE}}{2\pi(C_{ds} + C_{ds})}$ For $C_{ds} \gg C_{ds}$ and $C_{ds} \approx C_{ds}$, $f_T = \frac{2\beta_{FE}\gamma}{3.5\pi L}$
Design Parameters	I_{ds}, V_{GS}, V_{DS}	$I_{ds}, V_{BE}, A_{FE} (\propto L)$
Good Analog Switch?	Yes, because the device is symmetric and has the i_D-i_{DSS} drain-to-source pair directly through the drain.	No, because the device is asymmetric with an offset voltage $V_{DS(on)}$.

Operating Conditions At the outset, note that we shall use active mode or active region to denote both the active mode of operation of the BJT and the saturation-mode of operation of the MOSFET.

The conditions for operating in the active mode are very similar for the two devices. The explicit threshold V_t of the MOSFET has $V_{GS(on)}$ as its implicit counterpart in the BJT. Furthermore, for modern processes, $V_{GS(on)}$ and V_t are almost equal.

Also, placing off the channel of the MOSFET in the drain end is very similar to reverse biasing the collector of the BJT. Note, however, that the asymmetry of the BJT results in $V_{DS(on)}$ and $V_{DS(on)}$ being unequal, while in the symmetrical MOSFET the operating threshold voltages at the source and the drain ends of the channel are identical (V_t). Finally, for both the MOSFET and the BJT to operate in the active mode, the voltage across the device ($V_{DS}-V_{DS(on)}$) must be at least 0.2 V to 0.3 V.

Current-Voltage Characteristics The square-law control characteristic, $i_D \propto v_{GS}$, in the MOSFET should be contrasted with the exponential control characteristic, $i_C \propto e^{v_{BE}}$, of the BJT. Obviously, the latter is a much more sensitive relationship, with the result that i_C can vary over a very wide range (five decades or more) within the same BJT. In the MOSFET, the range of i_D achieved at the same device is much more limited. To appreciate this point further, consider the parabolic relationship between i_D and v_{GS} , and recall from our discussion earlier that v_{GS} is usually kept in a narrow range (0.2 V to 0.4 V).

Next we consider the effect of the device dimensions on its current. For the bipolar transistor the control parameter is the area of the emitter-base junction (EBJ), A_E , which determines the total current i_C . It can be varied over a relatively narrow range, such as 10 to 1. Thus, while the emitter area can be used to achieve current scaling in an IC (as we shall see in the next section in connection with the design of current mirrors) a narrow range of variation reduces its significance as a design parameter. This is particularly so if we compare by

with its counterpart in the NMOSFET, the aspect ratio W/L . MOSFET devices can be designed with W/L ratios for i_D with values such as 0.1 to 100. As a result, W/L is a very significant MOS design parameter. Like A_E , it is also used in current scaling, as we shall see in the next section. Combining the possible range of variation of v_{GS} and W/L one can design MOS transistors to operate over an i_D range of four decades or so.

The channel-length modulation in the NMOSFET and the base-width modulation in the BJT are similarly modeled and give rise to the dependence of $i_D(i_D)$ on $v_{GS}(v_{GS})$ alone, hence to the finite output resistance r_o in the active region. Two important differences, however, exist. In the BJT, V_t is solely a process-technology parameter and does not depend on the dimensions of the BJT. In the MOSFET, the situation is quite different: $V_t = V_t^* L$, where V_t^* is a process-technology parameter and L is the channel length used. Also, in modern electronic processes, V_t is very low, resulting in V_t values much lower than the corresponding values for the BJT.

The last, and perhaps most important, difference between the current-voltage characteristics of the two devices concerns the input current into the control terminal. While the gate current of the MOSFET is practically zero and the input resistance looking into the gate is practically infinite, the BJT draws base current i_B that is proportional to the collector current: $i_B = i_C/\beta$. The finite base current and the corresponding finite input resistance looking into the base is a definite disadvantage of the BJT in comparison to the MOSFET. Indeed, it is the infinite input resistance of the MOSFET that has made possible analog and digital circuit applications that would be feasible with the BJT. Examples include dynamic digital memory (Chapter 11) and switched capacitor filters (Chapter 12).

PROBLEMS

(1) For an NMOS transistor with $W/L = 10$ fabricated in the 0.18- μm process whose data are given in Table 6.1, find the values of $R_{DS(on)}$ and $V_{GS(on)}$ required to operate the device at $I_D = 100 \mu\text{A}$, ignoring channel-length modulation.

(2) Find V_{GS} for an nMOS transistor fabricated in the low-voltage process specified in Table 6.2 and operated at $I_D = 100 \mu\text{A}$. Ignore base width modulation.

Solution

$$(1) I_D = \frac{1}{2}(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{GS}^2$$

Substituting $I_D = 100 \mu\text{A}$, $W/L = 10$, and from Table 6.1, $\mu_n C_{ox} = 187 \mu\text{A/V}^2$ results in

$$100 = \frac{1}{2} \times 187 \times 10 \times V_{GS}^2$$

$$V_{GS} = 0.35 \text{ V}$$

Thus,

$$V_{DS(on)} = V_t + V_{GS} = 0.46 + 0.35 = 0.81 \text{ V}$$

$$(2) I_C = I_D e^{\frac{V_{BE}}{V_t}}$$

Substituting $I_D = 100 \mu\text{A}$ and from Table 6.3, $I_D = 6 \times 10^{-6} \text{ A}$ gives

$$V_{BE} = 0.025 \ln \frac{100 \times 10^{-6}}{6 \times 10^{-6}} = 0.76 \text{ V}$$

EXERCISE

Given a NMOS p-channel transistor in the enhancement mode operating at $T = 25^\circ\text{C}$, $V_{GS} = 1.2\text{ V}$, $V_D = 0.8\text{ V}$, $I_D = 10\text{ mA}$, $\mu_n C_{ox} = 20\text{ }\mu\text{A/V}^2$, $V_T = 0.5\text{ V}$. Neglecting drain-to-body voltage, calculate (a) the intrinsic gain A_0 of the MOSFET, (b) the output resistance r_o of the MOSFET, and (c) the corresponding operating V_{GS} .

Answers: (a) $A_0 = 10^3$; (b) $r_o = 3.1\text{ m}\Omega$ for a load of about $4000\text{ }\Omega$; (c) for V_{GS} negative, $V_{GS} = -0.2\text{ V}$; for $V_{GS} > 0$, $V_{GS} = 2.7\text{ mV}$.

Low-Frequency Small-Signal Models. The low-frequency models for the two devices are very similar except, of course, for the finite base element (finite β) of the BJT, which gives rise to r_e in the hybrid-pi model, and to the unequal currents in the emitter and collector in the T model ($\alpha \neq 1$). Here it is interesting to note that the low-frequency small-signal models become identical if one thinks of the MOSFET as a BJT with $\beta = \gamma g_m / V_T$.

For both devices, the hybrid- π model indicates that the open-circuit voltage gain (from gate to drain bias to collected with the source connected to ground) is $-g_m r_o$. It follows that $g_m r_o$ is the maximum gain available from a single transistor of either type. This important transistor parameter is given in the name intrinsic gain and is denoted A_0 . We will have more to say about the intrinsic gain shortly.

Although not included in the MOSFET low-frequency model shown in Table 6.2, the body effect can have a significant implication for the operation of the MOSFET as an amplifier. In simple terms, if the body (substrate) is not connected to the source, it can act as a second gate for the MOSFET. The voltage signal that develops between the body and the source, v_{BS} , gives rise to a drain current component i_{DSB} , where the body transconductance g_{mB} is proportional to g_m ; that is, $i_{DSB} = z g_m$, where the factor z is in the range of 0.1 to 0.3. We shall take the body effect into account in the study of IC MOS amplifiers in the succeeding sections. The body effect has no counterpart in the BJT.

The Transconductance. For the BJT, the transconductance g_m depends only on the collector current I_C . Recall that V_T is a physical constant $\approx 0.025\text{ V}$ at room temperature. It is interesting to observe that g_m does not depend on the geometry of the BJT, and its dependence on the BJT area is only through the effect of the area on the total collector current I_C . Similarly, the dependence of g_m on V_{GS} is only through the fact that V_{GS} determines the total current in the collector. By contrast, g_m of the MOSFET depends on I_D , V_{GS} , and V_D . Therefore, we use three different (but equivalent) formulae to express g_m of the MOSFET.

The first formula given in Table 6.3 for the MOSFET's g_m is the most directly comparable with the formula for the BJT. It indicates that for the same operating current, I_D , of the MOSFET it is achievable than that of the BJT. This is because $V_{GS}/2$ is the range of 0.1 to 0.2 V, which is four to eight times the corresponding term in the BJT's formula, namely V_T .

The second formula for the MOSFET's g_m indicates that for a given device (i.e., given W/L), g_m is proportional to V_{GS} . Thus, a higher g_m is obtained by operating the MOSFET at a higher overdrive voltage. However, we should recall the limitations imposed on the magnitude of V_{GS} by the limited value of V_{DD} . Put differently, the need to obtain a reasonably high g_m constrains the designer's choice in selecting V_{GS} .

The third g_m formula shows that for a given transistor (i.e., given W/L), g_m is proportional to I_D/V_D . This should be contrasted with the bipolar case, where g_m is directly proportional to I_C .

Output Resistance. The output resistance for both devices is determined by small-signal analysis, with r_o being the ratio of V_o to the bias current (I_B or I_D). Thus, for both transistors,

r_o is inversely proportional to the bias current. The difference in nature and magnitude of r_o between the two devices has already been discussed.

Intrinsic Gain. The intrinsic gain A_0 of the BJT is the ratio of V_A , which is solely a process parameter (35 V to 130 V), and V_T , which is a physical parameter (0.025 V at room temperature). Thus, A_0 of a BJT is independent of the device junction area and of the operating current, and its value ranges from 1000/V to 5000/V. The situation in the MOSFET is very different. Table 6.3 provides three different (but equivalent) formulae for expressing the MOSFET's intrinsic gain. The first formula is the easiest directly comparable to that of the BJT. Here, however, we note the following:

1. The quantity in the denominator is $V_{GS}/2$, which is a design parameter, and although it is becoming smaller in designs using short-channel technologies, it is still much larger than V_T . Furthermore, as we have seen earlier, there are reasons for selecting larger values of V_{GS} .
2. The numerator quantity i_D is both process and device dependent, and it is only has been steadily decreasing.

As a result, the intrinsic gain realized in a single MOSFET amplifying stage fabricated in a modern short-channel technology is only 20/V to 10/V, about two orders of magnitude lower than that for a BJT.

The third formula given for A_0 in Table 6.3 points out a very interesting fact: For a given process technology (V_A and $\mu_n C_{ox}$) and a given device (W/L), the intrinsic gain is inversely proportional to $\sqrt{I_D}$. This is illustrated in Fig. 6.1, which shows a typical plot of A_0 versus the bias current I_D . The plot confirms that the gain increases as the bias current is lowered. The gain, however, levels off at very low currents. This is because the MOSFET enters the saturation region of operation (Section 4.9), where it becomes very much like a BJT with a exponential current-voltage characteristic. The intrinsic gain then becomes constant, just like that of a BJT. Note, however, that although a higher gain is achieved at lower bias currents, the price paid is a lower g_m and less ability to drive capacitive loads and thus a decreased bandwidth. This point will be further illustrated shortly.

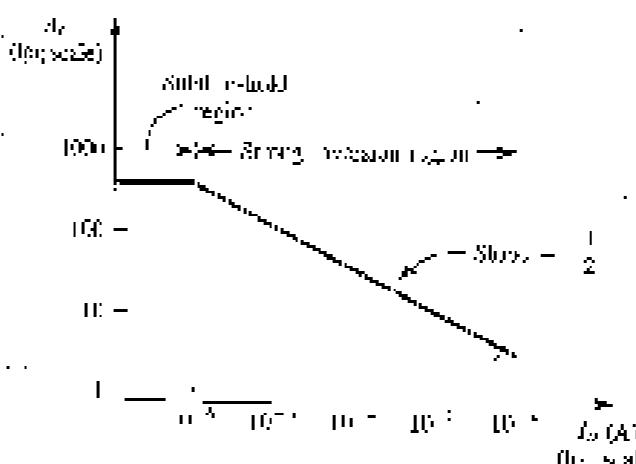


FIGURE 6.1 The intrinsic gain of the MOSFET varies inversely with I_D . Outside the subthreshold region, the value of $A_0 \approx V_A/2\mu_n C_{ox} I_D$ for a case: $\mu_n C_{ox} = 20\text{ }\mu\text{A/V}^2$, $V_A = 20\text{ V}$, $L = 2\text{ }\mu\text{m}$, and $W = 20\text{ }\mu\text{m}$.

Example 6.2

We wish to compare the values of g_m , input resistance at the gate (base), r_{in} , and A_{vD} for an NMOS transistor fabricated in the 0.25 μm technology specified in Table 5.1 and another transistor also listed in the low voltage technology specified in Table 6.2. Assume switch devices for operating at a drain (collector) current of 100 μA . For the MOSFET, let $L = 0.1 \mu\text{m}$ and $W = 1 \mu\text{m}$, and specify the required V_{DD} .

Solution

For the NMOS transistor,

$$I_D = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{GS}^2$$

$$100 = \frac{1}{2} \times 261 \times \frac{1}{0.1} \times V_{GS}^2$$

Thus,

$$V_{GS} = 0.27 \text{ V}$$

$$g_m = \frac{(\mu_n C_{ox}) W}{L} / r_o \\ = \sqrt{2 \times 261 \times 0.1 \times 100} = 0.03 \text{ mA/V}$$

$$r_{in} = \infty$$

$$r_o = \frac{V_D}{I_D} = \frac{2 \times 0.27}{0.1} = 54 \text{ k}\Omega$$

$$A_{vD} = g_m r_o = 0.03 \times 54 = 1.62 \text{ V/V}$$

For the BJT transistor,

$$g_m = \frac{I_D}{V_T} = \frac{0.1 \text{ mA}}{0.025 \text{ V}} = 4 \text{ mA/V}$$

$$R_A = r_e = \beta_0 / g_m = \frac{100}{4 \text{ mA/V}} = 25 \text{ k}\Omega$$

$$r_o = \frac{V_D}{I_D} = \frac{25}{0.1 \text{ mA}} = 350 \text{ k}\Omega$$

$$A_{vD} = g_m r_o = 4 \times 350 = 1400 \text{ V/V}$$

EXERCISE

- 6.6.2. For each NMOS transistor fabricated in the 0.25 μm process specified in Table 5.1 with $L = 0.5 \mu\text{m}$ and $W = 1 \mu\text{m}$, determine the value of r_o obtained at $I_D = 10 \mu\text{A}$, 0.1 mA , and 1 mA .

Ans: 2.5, 25, 250 $\text{k}\Omega$; 0.6, 6, 60 $\text{M}\Omega$; 0.06, 0.6, 6 $\text{G}\Omega$

High-Frequency Operation The simplified high-frequency equivalent circuits for the MOSFET and the BJT are very similar, and so are the formulas for determining their unity-gain frequency (f_T , also called transition frequency), f_T . Recall that f_T is a measure of the intrinsic bandwidth of the transistor itself and does not take into account the effects of capacitive loads. We shall address the issue of capacitive loads shortly. For the time being, note the striking similarity between the approximate formulas given in Table 6.2 for the value of f_T of the two devices. In both cases, f_T is inversely proportional to the square of the drain dimension of the device, the channel length for the MOSFET and the base width for the BJT. These features also clearly indicate that shorter-channel MOSFETs⁷ and narrower-base BJTs are inherently capable of a wider bandwidth of operation. It is also important to note that while for the BJT the approximate expression for f_T indicates that it is effectively grossly determined, the corresponding expression for the MOSFET shows that f_T is proportional to the overdrive voltage, V_{GS} . Thus we have conflicting requirements on V_{GS} : While a higher low-frequency gain is achieved by operating at a low V_{GS} , wider bandwidth requires an increase in V_{GS} . Therefore the selection of a value for V_{GS} involves, among other considerations, a trade-off between gain and bandwidth.

For silicon BJTs fabricated in the modern low voltage process, f_T is in the range of 10 GHz to 20 GHz as compared to the 400 MHz to 600 MHz obtained with the standard high-voltage process. In the NMOS case, NMOS transistors fabricated in a modern submicron technology, such as the 0.18- μm process, achieve f_T values in the range of 5 GHz to 15 GHz.

Before leaving the subject of high-frequency operation, let's look into the effect of a capacitive load on the bandwidth of the common-source (common-emitter) amplifier. For this purpose we shall assume that the frequencies of interest are much lower than f_T of the transistor. Hence we shall not take the transistor capacitances into account. Figure 6.2(a) shows a common-source amplifier with a capacitive load C_L . The voltage gain from gate to drain can be found as follows:

$$\begin{aligned} V_o &= -g_m V_{GS} (r_o + C_L) \\ &= g_m V_{GS} \frac{\frac{1}{sC_L}}{1 + \frac{1}{sC_L r_o}} \\ A_{vD} &= \frac{V_o}{V_{GS}} = -\frac{g_m r_o}{1 + sC_L r_o} \end{aligned} \quad (6.1)$$

Thus the gain has, as expected, a low-frequency value of $-g_m r_o = A_0$ and a frequency response of the single time constant (STC) low-pass type with a break (pole) frequency at

$$\omega_B = \frac{1}{C_L r_o} \quad (6.2)$$

Obviously this pole is formed by r_o and C_L . A sketch of the magnitude of gain versus frequency is shown in Fig. 6.2(b). We observe that the gain crosses the 0-dB line at frequency ω_B .

$$\omega_B = A_0 \omega_0 = (g_m r_o) \frac{1}{C_L r_o}$$

⁷ Although the region is beyond the capabilities of this stage, f_T of MOSFETs can have very short time constants (typically $< 10^{-12}$ s) other than $> 10^{-3}$ s.

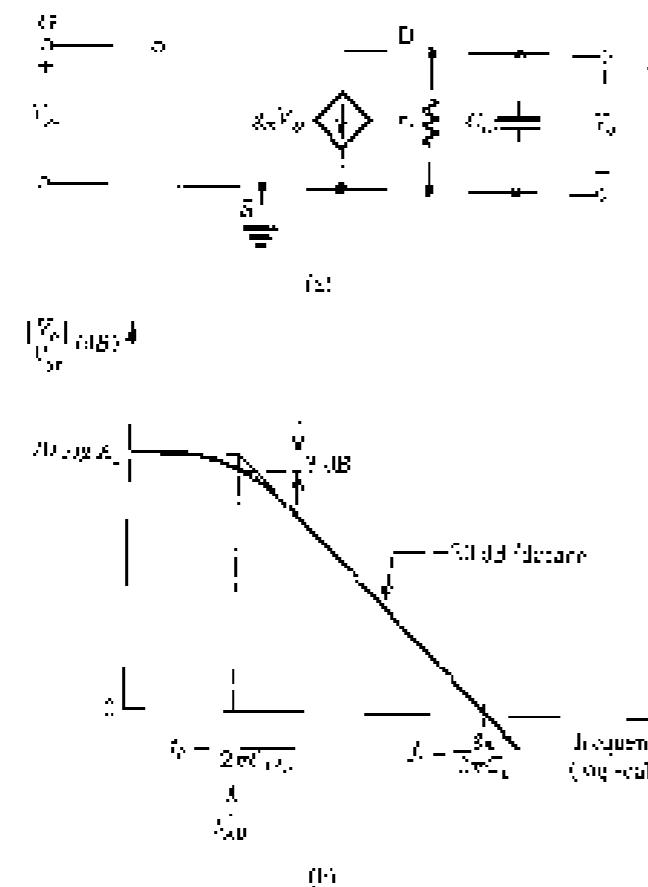


FIGURE 6.2 Frequency response of a CS amplifier loaded with a capacitor C_L and fed with an AC voltage V_{DS} . It is assumed that the MOSFET is operating at frequencies much lower than f_T , and that the external impedances can be taken as constant.

Thus,

$$(b) \quad f_C = \frac{2\pi}{C_L} \quad (6.3)$$

That is, the unity-gain frequency or, equivalently, the gain-bandwidth product¹ f_C , is the ratio of g_m and C_L . We thus clearly see that, for a given capacitive load C_L , a larger gain-bandwidth product is achieved by operating the MOSFET as a higher g_m . Identical analysis and conclusions apply to the case of the BJT. In fact, bandwidth increases as bias current I_C increases.

Design Parameters For the BJT there are three design parameters— I_C , V_{BE} , and f_T (or, equivalently, the area of the emitter-base junction)—of which any two can be selected by the designer. However, since f_T is exponentially related to V_{BE} and is very sensitive to the value of V_{BE} (V_{BE} changes by only 0.01 V for a factor of 10 change in f_T), f_T is much more useful than V_{BE} as a design parameter. As mentioned earlier, the utility of the BJT, though a

¹The unity-gain frequency and gain-bandwidth product of an amplifier are the same when the frequency response is of the single pole type; otherwise the two parameters may differ.

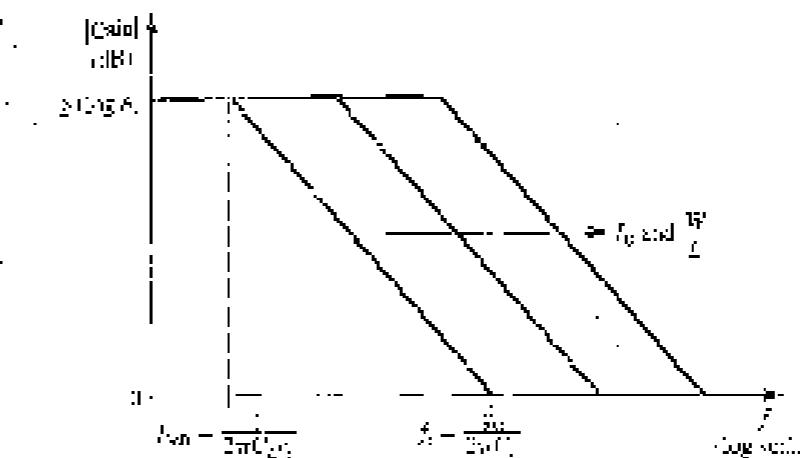


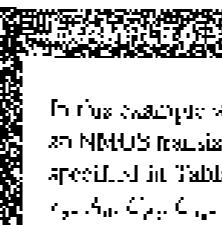
FIGURE 6.3 Figure 6.2 for MOSFET, whereas the bandwidth of MOSFET amplifier loaded by a constant capacitive load C_L .

design parameter, is rather limited because of the narrow range over which A_2 can vary. It follows that for the BJT there is only one effective design parameter: the collector current I_C . Finally, note that we have not considered V_{DS} to be a design parameter, since its effect on f_T is only secondary. Of course, as we learned in Chapter 5, V_{DS} affects the output signal swing.

For the MOSFET there are four design parameters— I_D , V_{DS} , L , and W —of which any three can be selected by the designer. For audio circuit applications the trade-off is selecting a value for L (as between the higher speeds of operation (wider amplifier bandwidth) obtained at lower values of L and the higher currents obtainable at larger values of L). Usually one selects an L of about 25% to 50% greater than L_{min} .

The second design parameter is V_{DS} . We have already made numerous remarks about the effect of the value of V_{DS} on the current. Usually, for submicron technologies, V_{DS} is selected in the range of 0.2 V to 0.4 V.

Once values for L and V_{DS} are selected, the designer is left with the selection of the value of L or W (or, equivalently, W/L). For a given process and for the selected values of L and V_{DS} , I_D is proportional to W/L . It is important to note that the choice of I_D (or, equivalently, of W/L) has no bearing on the value of transconductance A_2 and the corner frequency f_C . However, it affects the value of g_m and hence the gain-bandwidth product. Figure 6.3 illustrates this point by showing how the gain of a common-source amplifier operated at a constant V_{DS} varies with I_D (or, equivalently, W/L). Note that, while the dc gain remains unchanged, increasing W/L and, correspondingly, I_D , increases the bandwidth proportionally. This, however, assumes that the load capacitance C_L is not affected by the device size, an assumption that may not be entirely justified in some cases.



In this example we investigate the gain and the high-frequency response of an opamp using an NMOS transistor. For the new transistor, assume that it is fabricated in the low-voltage process specified in Table 6.3, and assume that $C_L = C_{DS}$. For $I_D = 1 \mu\text{A}$, 100 pF , and -1 mA , find g_m , A_2 , C_{in} , C_{out} , C_{ds} , C_{gs} , and f_C . Adjust the value of I_D so that the gain-bandwidth product f_T of a common-emitter amplifier loaded by a $1 \text{ k}\Omega$ capacitor is approaching the load capacitance.

of height W . For the NMOS transistor, assume that it is fabricated in the 0.25- μm CMOS process with $L = 0.4 \mu\text{m}$. Let the transistor be operated at $V_{DD} = 0.25 \text{ V}$. Find V_{GS} that is required to obtain $I_D = 10 \mu\text{A}$, $100 \mu\text{A}$, and 1 mA . At each value of I_D , find g_m , r_o , A_v , C_{gs} , C_{gd} , and f_T . Also, for each value of I_D , determine the gain-bandwidth product f_T of a current-source amplifier loaded by a 100Ω resistor, neglecting the internal capacitances of the transistor.

Solution

For the PNP transistor:

$$g_m = \frac{I_c}{V_T} = \frac{I_c}{0.025} = 40 I_c \text{ A/V}$$

$$r_o = \frac{V_T}{I_c} = \frac{25}{12} \Omega$$

$$A_v = \frac{V_O}{V_S} = \frac{55}{0.025} = 1200 \text{ V/V}$$

$$C_{gs} = C_p g_m = 10 \times 10^{-12} \times 40 I_c = 0.6 \times 10^{-9} I_c \text{ F}$$

$$C_{gd} = 3C_{gs} = 10 \text{ pF}$$

$$C_g = C_{gs} + C_{gd}$$

$$C_g \approx C_{gd} = 3 \text{ pF}$$

$$f_T = \frac{R_o}{2\pi(C_g + C_p)}$$

$$f_T = \frac{R_o}{2\pi C_g} = \frac{R_o}{2\pi \times 1 \times 10^{-12}}$$

We thus obtain the following results:

	$10 \mu\text{A}$	$40 \mu\text{A}$	1 mA	10 mA	40 mA	100 mA	400 mA	1 A
g_m	0.2	3.6	14.0	4	16	12	5	3.4
r_o	12	350	1400	40	16	50	5	11.6
A_v	40	35	1400	400	16	410	5	15.2

For the NMOS transistor:

$$I_D = \frac{1}{2} \rho_s C_{ox} \frac{W}{L} V_{GS}^2$$

$$= \frac{1}{2} \times 267 \times \frac{W}{L} \times \frac{1}{16}$$

Thus,

$$\frac{W}{L} = 0.12 I_D$$

$$g_m = \frac{I_D}{V_{DD}/2} = \frac{I_D}{0.25/2} = 8 I_D \text{ A/V}$$

$$r_o = \frac{V_D}{I_D} = \frac{5 \times 0.4}{I_D} = \frac{2}{I_D} \Omega$$

$$A_v = g_m r_o = 16 \text{ V/V}$$

$$C_{gs} = \frac{1}{2} W L C_{ox} = C_{gd} = \frac{1}{2} W \times 0.4 \times 0.6 = 0.6 \text{ pF}$$

$$C_g = C_{gs} + C_{gd} = 0.6 \text{ pF}$$

$$f_T = \frac{R_o}{2\pi(C_g + C_p)}$$

$$f_T = \frac{R_o}{2\pi C_g}$$

We thus obtain the following results:

	$10 \mu\text{A}$	$40 \mu\text{A}$	1 mA	10 mA	40 mA	100 mA	400 mA	1 A
g_m	1.2	3.6	14.0	4	16	12	5	3.4
r_o	12	350	1400	40	16	50	5	11.6
A_v	40	35	1400	400	16	410	5	15.2

EXERCISE

6.2.3 For the PNP transistor specified in Exercise 6.2.1, let $I_c = 0.5 \mu\text{A}$, $R_o = 10 \Omega$, and $V_{DD} = 1 \text{ V}$. Find A_v , C_{gs} , C_{gd} , C_g , and f_T for the specified bias conditions (see Table 6.1).

6.2.4 Combining MOS and Bipolar Transistors—BiCMOS Circuits

From the discussion above it should be evident that the BJT has the advantage over the MOSFET of a much higher transconductance (g_m) at the same value of drain current. Thus, in addition to realizing much higher voltage gains per amplifier stage, bipolar transistor amplifiers have superior high-frequency performance compared to their MOS counterparts.

On the other hand, the practically infinite input resistance of the gate of a MOSFET makes it possible to design amplifiers with extremely high input resistances and an almost zero static bias current. Also, as mentioned earlier, the MOSFET provides an excellent implementation of a switch, a function that has made CMOS technology capable of realizing a host of analog circuit functions that are not possible with bipolar transistors.

It can thus be seen that each of the two transistor types has its own distinct and unique advantages. Bipolar technology has been extremely useful in the design of very-high-quality general-purpose circuit building blocks, such as op amps. On the other hand, CMOS, with its very high packing density and its suitability for both digital and analog circuits, has become the technology of choice for the implementation of very-large-scale integrated circuits. Nevertheless, the performance of CMOS circuits can be improved if the designer has available (on the same chip) bipolar transistors that can be employed in functions that require their high g_m and excellent current-driving capability. A technology that allows the fabrication of high-quality bipolar transistors on the same chip as CMOS circuits is aptly called BiCMOS. At appropriate locations throughout this book we shall present interesting and useful BiCMOS circuit examples.

6.2.5 Validity of the Square-Law MOSFET Model

We conclude this section with a comment on the validity of the simple square-law model we have been using to describe the operation of the MOSFET transistor. While this simple model works well for devices with relatively long channels (3–5 µm), it does not provide an accurate representation of the operation of short-channel devices. This is because a number of physical phenomena come into play in these submicron devices, resulting in what are called short-channel effects. Although the study of short-channel effects is beyond the scope of this book, it should be mentioned that MOSFET models have been developed that take these effects into account. However, they are understandably quite complex and do not lend themselves to hand analysis of the type needed to develop insight into circuit operation. Rather, these models are suitable for computer simulation and are instead used in SPICE (Section 6.15). For quick, manual analysis, however, we will continue to use the square-law model which is the basis for the comparison of Table 6.3.

6.3 IC BIASING—CURRENT SOURCES, CURRENT MIRRORS, AND CURRENT-STEERING CIRCUITS

Biasing in integrated-circuit design is based on the use of current-source sources. On an IC chip with a number of amplifier stages, a constant DC current (called a reference current) is generated at one location and is then distributed to various other locations for biasing the various amplifier stages through a process known as current steering. This approach has the advantage that the effort expended on generating a predictable and stable reference circuit, usually utilizing a precision resistor connected to the chip, need not be repeated for every amplifier stage. Furthermore, the bias currents of the various stages track each other in case of changes in power-supply voltage or in temperature.

In this section we study several building blocks and techniques employed in the bias design of IC amplifiers. These circuits are also utilized as amplifier load elements, as will be seen in Section 6.5 and beyond.

6.3.1 The Basic MOSFET Current Source

Figure 6.4 shows the circuit of a simple MOSFET current source. The heart of the circuit is transistor Q_1 , the drain of which is shorted to its gate, thereby forcing it to operate in the saturation mode with⁷

$$I_{D1} = \frac{1}{2} \cdot \frac{W}{L} \cdot I_{DS}^2 \cdot (V_{GS} - V_{th})^2 \quad (6.4)$$

where we have neglected channel-length modulation. The drain current of Q_1 is supplied by V_{DD} through resistor R , which in most cases would be outside the IC chip. Since the gate currents are zero,

$$I_D = I_{ref} = \frac{V_{DD} - V_{th}}{R} \quad (6.5)$$

where the current through R is considered to be the reference current of the current source and is denoted I_{ref} . Equations (6.4) and (6.5) can be used to determine the value required for R .

⁷ Such a transistor is said to be fully connected.

6.3.2 IC BIASING—CURRENT SOURCES, CURRENT MIRRORS, AND CURRENT-STEERING CIRCUITS

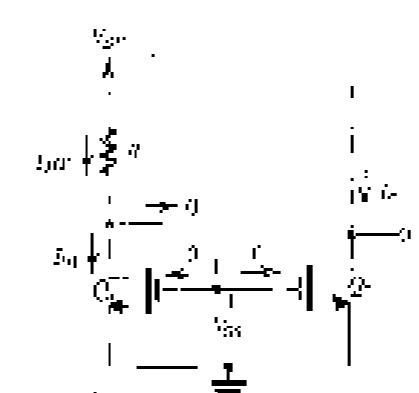


FIGURE 6.4 Circuit for a basic MOSFET current-source circuit.

Now consider resistor Q_2 . It has the same V_{GS} as Q_1 ; thus, if we assume that it is operating in saturation, its drain current, which is the output current I_0 of the current source, will be

$$I_0 = I_{D2} = \frac{1}{2} \cdot \frac{W}{L} \cdot I_{DS}^2 \cdot (V_{GS} - V_{th})^2 \quad (6.6)$$

where we have neglected channel-length modulation. Equations (6.4) and (6.6) enable us to relate the output current I_0 to the reference current I_{ref} as follows:

$$\frac{I_0}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \quad (6.7)$$

This is a simple and attractive relationship: The special connection of Q_1 and Q_2 provides an output current I_0 that is related to the reference current I_{ref} by the ratio of the aspect ratios of the transistors. In other words, the relationship between I_0 and I_{ref} is solely determined by the geometries of the transistors. In the special case of identical transistors, $I_0 = I_{ref}$, and the circuit simply replicates or mirrors the reference current in the output terminal. This has given the circuit composed of Q_1 and Q_2 the name current mirror, a name that is used irrespective of the ratio of device dimensions.

Figure 6.5 depicts the current-mirror circuit with the input reference current shown as being supplied by a current source for both simplicity and generality. The current gain or current transfer ratio of the current mirror is given by Eq. (6.7).

Effect of V_C on I_0 . In the description above for the operation of the current source of Fig. 6.4, we assumed Q_1 to be operating in saturation. This is obviously essential if Q_1 is to supply a

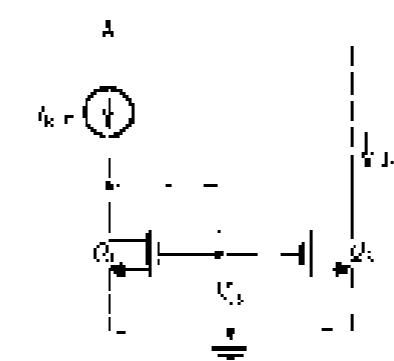


FIGURE 6.5 Basic MOSFET current mirror.

constant current source. To ensure that Q_2 is saturated, the circuit to which the drain of Q_2 is to be connected must establish a drain voltage V_D that satisfies the relationship

$$V_D \geq V_{DS} - V_T \quad (6.8)$$

or, equivalently, in terms of the drain-to-source voltage V_{DS} of Q_1 and Q_2 ,

$$V_D \geq V_{DS} \quad (6.9)$$

In other words, the current source will operate properly with an output voltage V_D as low as V_{DS} , which is a few millivolts (~ 1 volt).

Although this first neglected, channel-length modulation can have a significant effect on the operation of the current source. Consider, for simplicity, the case of two identical devices Q_1 and Q_2 . The drain current of Q_2 , I_{D2} , will equal the current in Q_1 , I_{DS1} , ... the value of V_D that causes the two devices to have the same V_{DS} , that is, $V_D = V_{DS1}$. As V_D is increased above this value, I_{D2} will increase according to the incremental output resistance r_{DS} of Q_2 . This is illustrated in Fig. 6.6, which shows I_{D2} versus V_D . Observe that since Q_2 is operating at a constant V_{DS} determined by passing I_{DS1} through the matched device Q_1 , the curve in Fig. 6.6 is simply the i_V -like characteristic curve of Q_2 for V_{DS} equal to the peak drain voltage V_{DS1} .

In summary, the current source of Fig. 6.4 and the current mirror of Fig. 6.5 have a finite output resistance R_o ,

$$R_o = \frac{\Delta V_D}{\Delta I_D} = r_{DS} = \frac{V_{DS1}}{I_D} \quad (6.10)$$

where I_D is given by Eq. (6.6) and V_{DS1} is the Early voltage of Q_1 . Note, too, that for a given process technology, V_A is proportional to the transistor channel length; thus, to obtain high output-resistance values, current sources are usually designed using transistors with relatively long channels. Finally, note that we can express the current I_D as

$$I_D = \frac{(W/L_1) I_{DS1}}{(W/L_2)} e^{\frac{V_D - V_{DS1}}{V_A}} \quad (6.11)$$

Fig.

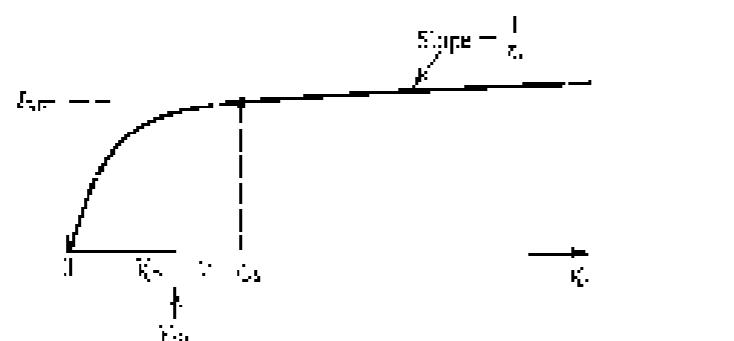


FIGURE 6.6 Output characteristics of the current source in Fig. 6.4 and the current mirror of Fig. 6.5 (the case of Q_2 is plotted in Q_1).

Given $V_{DS1} \approx 5$ V and using $I_{DS1} = 100 \mu\text{A}$, it is required to redesign the circuit of Fig. 6.4 to obtain an output current whose nominal value is $10 \mu\text{A}$. Both Q_1 and Q_2 are matched and have channel length $L = 1 \mu\text{m}$, channel widths $W = 10 \mu\text{m}$, $V_T = 0.7 \text{ V}$, and $k'_v = 200 \mu\text{A}/\text{V}^2$. What is the largest possible value of V_D ? Assuming that for this process technology, the Early voltage $V_A = 30$ V/ μm , find the output resistance of the current source. Also, find the change in output current resulting from a $\pm 1\%$ change in V_T .

Solution

$$I_D = I_{DS1} = \frac{k'_v}{2} \frac{W}{L} \frac{V_D}{V_A} \quad (6.12)$$

$$10 = 100 \times \frac{1}{2} \times 10 \frac{V_D}{30} \quad (6.12)$$

Thus,

$$V_D = 0.316 \text{ V}$$

and

$$V_{DS1} = V_T + V_{DS1} = 0.7 + 0.316 = 1 \text{ V}$$

$$R_o = \frac{V_{DS1} - V_D}{I_D} = \frac{3 - 1}{0.1 \mu\text{A}} = 20 \text{ k}\Omega$$

$$V_{DS1} = V_D \approx 0.3 \text{ V}$$

The L -gate transistors used, $L = 1 \mu\text{m}$. Thus,

$$V_A = 20 \times 1 = 20 \text{ V}$$

$$r_{DS} = \frac{20 \text{ V}}{0.1 \mu\text{A}} = 200 \text{ M}\Omega$$

If the output current will be $100 \mu\text{A}$ at $V_D = V_{DS1} = 1 \text{ V}$, if V_T changes by $\pm 1\%$, the corresponding change in I_D will be

$$\Delta I_D = \frac{\Delta V_D}{r_{DS}} = \frac{1 \text{ V}}{200 \text{ M}\Omega} = 5 \mu\text{A}$$

EXERCISE

6.4 In the design exercise of Example 6.2, it is required to reduce the output current of the current source to one-half its original value, $10 \mu\text{A}$, by $\pm 1\%$ of the drain voltage V_D , and Q_2 be unchanged. Assume that Q_1 and Q_2 remain matched.

Solution: $I_{DS1} = 5 \times 10^{-6} / 249.3 \mu\text{m}^2 = 20.1 \mu\text{A}$

6.3.2 MOS Current-Steering Circuits

As mentioned earlier, once a constant current is generated, it can be replicated to provide the bias currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function. Figure 6.7 shows a simple current-steering circuit.

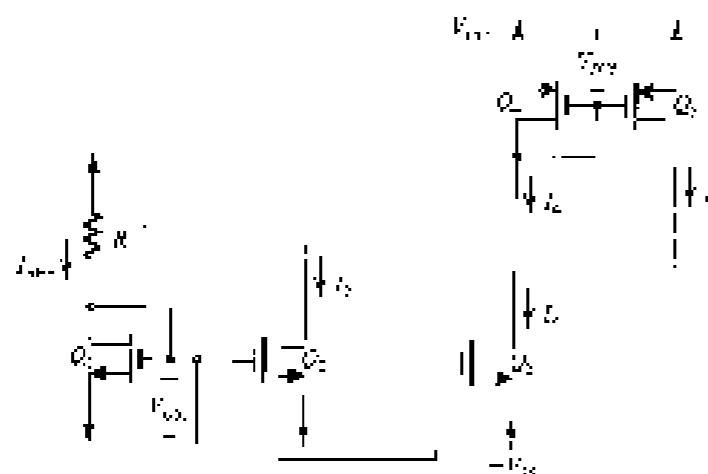


FIGURE 6.7 A CMOS cascode circuit.

Hence Q_1 together with R determine the reference current I_{R1} . Transistors Q_1 , Q_3 , and Q_4 form a two-output current mirror.

$$I_1 = I_{R1} \frac{(W/L)_1}{(W/L)_2} \quad (6.12)$$

$$I_3 = I_{R1} \frac{(W/L)_3}{(W/L)_4} \quad (6.13)$$

To ensure operation in the saturation region, the voltages at the drains of Q_1 and Q_3 are constrained as follows:

$$V_{D1}, V_{D3} > -V_{DD} - V_{CE1} - V_A \quad (6.14)$$

or equivalently,

$$V_{D1}, V_{D3} > -V_{DD} + V_{D1,ss} \quad (6.15)$$

where $V_{D1,ss}$ is the overdrive voltage at which Q_1 , Q_2 , and Q_3 are operating. In other words, the drains of Q_2 and Q_3 will have to remain higher than $-V_{DD}$ by at least the overdrive voltage, which is usually a few tenths of a volt.

Continuing our discussion of the circuit in Fig. 6.7, we see that current I_3 is fed to the input side of a current mirror formed by PMOS transistors Q_3 and Q_4 . This mirror provides,

$$I_3 = I_4 \frac{(W/L)_3}{(W/L)_4} \quad (6.16)$$

where $I_4 = I_2$. To keep Q_3 in saturation, its drain voltage should be

$$V_{D3} < V_{D3} - V_{D3,ss} \quad (6.17)$$

where $V_{D3,ss}$ is the overdrive voltage at which Q_3 is operating.

Finally, an important point to note is that while Q_3 provides current I_3 from a load (not shown in Fig. 6.7), Q_3 makes its current I_3 into a load (not shown in Fig. 6.7). Thus Q_4 is

analogously called a current source, whereas Q_2 would more properly be called a current sink. In an IC, both current sources and current sinks are usually needed.

EXERCISE

A CMOS cascode circuit is shown in Fig. 6.7. Assume $V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$, $V_{GS1} = 0.5\text{ V}$, $V_{GS2} = 0.5\text{ V}$, $V_{GS3} = 0.5\text{ V}$, $V_{GS4} = 0.5\text{ V}$, $V_A = 0.5\text{ V}$, $R = 10\text{ k}\Omega$, and $I_{R1} = 10\text{ mA}$. Find the required drain voltages V_{D1} and V_{D3} so that the output voltage V_{os} is 0.5 V. Assume that the transistors are matched.

6.3.3 BJT Circuits

The basic BJT current mirror is shown in Fig. 6.8. It looks in a fashion very similar to that of the MOS mirror. However, there are two important differences. First, the intrinsic base-emitter current of the BJT (or, equivalently, the finite β) causes an error in the current transfer ratio of the bipolar mirror. Second, the current transfer ratio is determined by the relative areas of the emitter-base junctions of Q_1 and Q_2 .

Let us first consider the case when β is sufficiently high so that we can neglect the base currents. The reference current I_{R1} is passed through the diode-connected transistor Q_1 and thus establishes a conduction voltage V_{BE1} which in turn is applied between base and emitter of Q_2 . Now, if Q_2 is matched to Q_1 , i.e., more specifically, if the EBJ area of Q_2 is the same as that of Q_1 and thus Q_2 has the same scale current I_2 as Q_1 , then the collector current of Q_2 will be equal to that of Q_1 ; that is,

$$I_2 = I_{C1}. \quad (6.18)$$

For this to happen, however, Q_2 must be operating in the active range, which in turn is achieved as long as the collector voltage V_C2 is 0.3 V or so higher than that of the emitter.

To obtain a current transfer ratio other than unity, say α , we simply arrange that the area of the EBJ of Q_2 is α times that of Q_1 . In this case,

$$I_2 = \alpha I_{C1}. \quad (6.19)$$

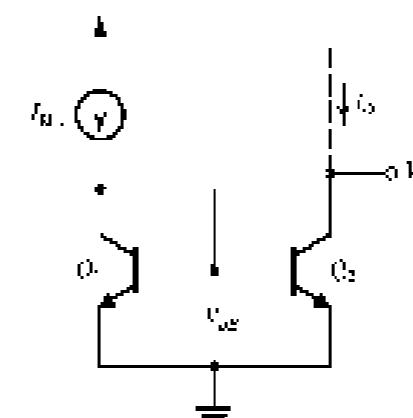


FIGURE 6.8 The basic BJT current mirror.

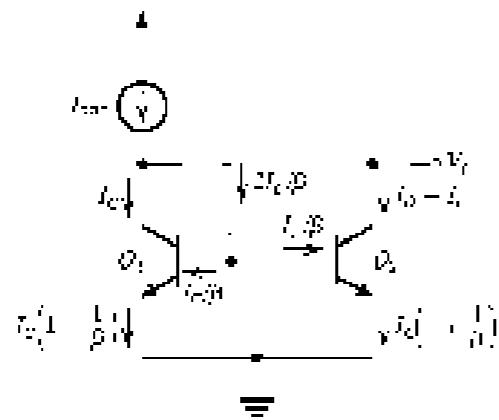


FIGURE 6.9 Analysis of the current ratio taking into account the figure 6 of the Tab. 1.

In general, the current transfer ratio is given by

$$\frac{I_{Q_2}}{I_{\text{EBI}}} = \frac{I_{Q_1}}{I_{\text{EBI}}} = \frac{\text{Area of EBI of } Q_2}{\text{Area of EBI of } Q_1} \quad (6.2)$$

Alternatively, if the size ratio m is an integer, one can think of \mathcal{Q}_1 as equivalent to m basis functions, each matched to \mathcal{Q}_2 and connected in parallel.

Next we consider the effect of finite mismatched on the current transfer ratio. The analysis for the case in which the current transfer ratio is dimensionally unity—that is, for the case in which Q_2 is matched to Q_1 —is illustrated in Fig. 6.8. The key point here is that since Q_1 and Q_2 are matched and have the same V_{ce} , the collector currents will be equal. The rest of the analysis is straightforward. A node equation at the collector of Q_1 yields

$$t_{\text{min}} = t_0 - 2I_F/\beta = I_F \left(1 + \frac{\gamma}{6}\right)$$

Finally, since $T_0 = T_c$, the current transfer gain can be found as

$$\frac{I_0}{I_{\text{REF}}} = \frac{I_0}{I_0 \left[1 + \frac{2}{\beta} \right]} = \frac{1}{1 + \frac{2}{\beta}} \quad . \quad (6.21)$$

Note that as β approaches ∞ , $I_{\text{eff}}/I_{\text{GFR}}$ approaches the nominal value of unity. For typical values of β , however, the error in the current transfer ratio can be significant. For instance, $\beta = 100$ results in a 2% error in the current transfer ratio. Furthermore, the error due to finite β increases as the nominal current transfer ratio is increased. The reader is encouraged to show that for a current with a nominal current transfer ratio m_0 (that is, one in which $I_{\text{eff}} = m_0 I_{\text{GFR}}$) the actual current transfer ratio is given by

$$\frac{I_0}{I_{\text{RMS}}} = \frac{m}{1 + \frac{m-1}{S}} \quad (6.22)$$

In comparison with the MOS current limiter, the IGBT limiter has a finite forward resistance R_f .

$$\bar{q}_n \equiv \frac{\lambda V_n}{2 E_n} - \nu_n = \frac{C_n}{E_n} \quad (6.23)$$

where V_{oL} and r_{oL} are the Early voltage and the output resistance, respectively, of Q_2 . This occurs if we neglect the effect due to finite β , the output current I_o will be at its

quantitative value only when \mathcal{D}_2 has the same V_{CE} as \mathcal{Q}_1 , namely at $V_D = V_{DD}$. As V_D is increased, i_D will correspondingly increase. Taking both the diode and the triode \mathcal{D}_2 into account, we can express the output current of a BJT inductor with a constant current transfer ratio α_{DC} as

$$t_1 = t_{\text{PER}} \cdot \frac{m}{(m+1)} \left(1 + \frac{V_0 - V_M}{V_N} \right) \quad (6.24)$$

where we note that the error term due to the Eary effect is expected so that it reduces to zero for $V_{\text{ex}} = V_{\text{ext}}$.

EXERCISES

⁶ The example of 1991 supports the view that there may be considerable variation in the importance of local factors in the 1990s. In 1991, $\lambda_1 = 0.1$, $\lambda_2 = 0.9$, and $\lambda_3 = 0.0$ ($\lambda_4 = 1 - 0.1 - 0.9 - 0.0 = 0$), which implies that $y_1 < y_2 < y_3$ (but $y_4 = 0$).

...and the best service.

A Simple Current Source In a manner analogous to that in the MOS case, the basic BJT current mirror can be used to implement a simple current source, as shown in fig. 8.10. Here the reference current is

$$I_{KL} = \frac{V_{KL}}{R} \cdot \frac{V_{KL}}{R} \quad (6.25)$$

where V_{ctrl} is the base carrier voltage corresponding to the desired value of output current I_2 .

$$I_{\text{eff}} = \frac{I_{\text{ext}}}{1 + (2/\theta) \left(1 + \frac{V_{\text{ex}} - V_{\text{ext}}}{V} \right)} \quad (276)$$

The overall resistance of this copper - sleeve is $R_{\text{tot}} = 0.1$

$$R_p = r_{\text{eff}} \pm \frac{V_A}{k_p} \pm \frac{V_A}{k_{\text{max}}} \quad (6.27)$$

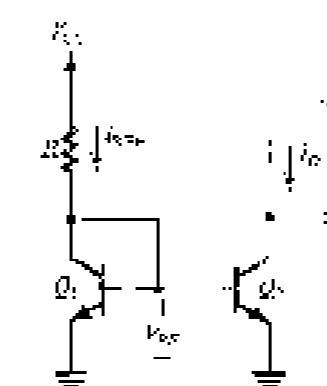


FIGURE 6-10 A simple 4D space-time diagram

EXAMPLE 6.1

Determine the output voltage of V_0 with no input signal. Assume $I_{C1} = 100 \mu A$, $I_{C2} = 200 \mu A$, and the current source current of $I_{R1} = 120 \mu A$ generate current $I_{R2} = 75 \mu A$. The power supply $V_{CC} = 5 V$ from the bottom of V_0 . Assume $\beta = 100$ and $V_A = 50 V$.

Solution: $I_{C1} = 100 \mu A$; $I_{C2} = 200 \mu A$; $I_{R1} = 120 \mu A$; $I_{R2} = 75 \mu A$; $V_{CC} = 5 V$; $\beta = 100$; $V_A = 50 V$

Current Steering. To generate bias currents for different amplifier stages in no IC, the current-steering approach described for MOS circuits can be applied in the bipolar case. As an example, consider the circuit shown in Fig. 6.11. The dc reference current I_{REF} is generated in the branch that consists of the diode-connected transistor Q_1 , resistor R , and the diode-connected transistor Q_2 :

$$I_{REF} = \frac{V_{BE1} - V_{SD1}}{R} = \frac{V_{BE1} - V_{A1}}{R} \quad (6.28)$$

Now, for simplicity, assume that all the transistors have high β and thus that the base currents are negligibly small. We will also neglect the Early effect. The diode-connected transistor Q_1 draws a current mirror with Q_2 ; thus Q_2 will supply a constant current I_{R2} equal to I_{REF} . Transistor Q_3 can supply this current to any load as long as the voltage that develops at the collector does not exceed $|V_{CE3}| = 0.3 V$; otherwise Q_3 would enter the saturation region.

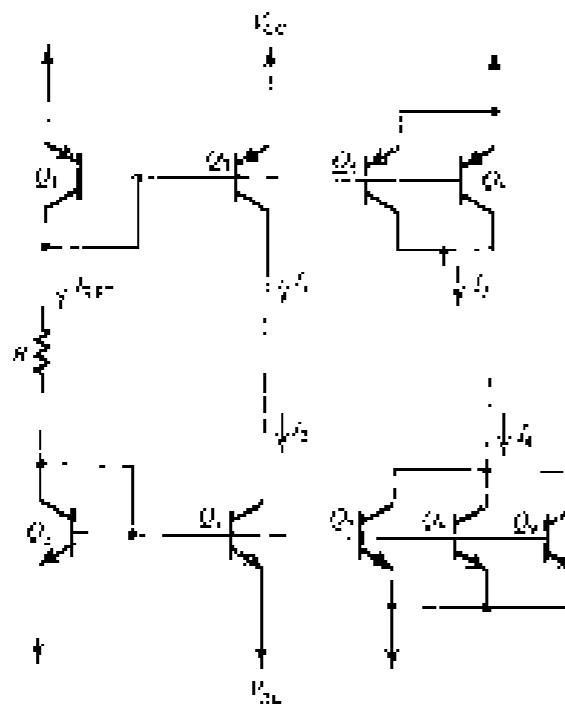


FIGURE 6.11 Generation of a number of constant currents of various magnitudes.

To generate a dc current twice the value of I_{REF} , two transistors, Q_3 and Q_4 , each of which is matched to Q_1 , are connected in parallel, and the combination forms a mirror with Q_2 . Thus $I_3 = 2I_{REF}$. Note that the parallel combination of Q_3 and Q_4 is equivalent to a single transistor with an β 100 times double that of Q_1 , which is precisely what is done when this circuit is fabricated in IC form.

Transistor Q_5 turns on in series with Q_3 ; thus Q_5 generates a constant current I_5 equal to I_{REF} . Note that while Q_5 sources its current to parts of the circuit whose voltage should not exceed $|V_{CE5}| = 0.3 V$, Q_6 sinks its current from parts of the circuit whose voltage should not decrease below $-|V_{CE6}| = 0.3 V$. Finally, to generate a current three times I_{REF} , three transistors, Q_7 , Q_8 , and Q_9 , each of which is matched to Q_5 , are connected in parallel, and the combination is placed in a common-emitter configuration with Q_6 . Again, in an IC implementation, Q_7 , Q_8 , and Q_9 would be replaced with a transistor having a junction area three times that of Q_5 .

EXAMPLE 6.2

Figure 6.12 is a result of a computer simulation of the circuit shown in Fig. 6.11. The input voltage is $V_{IN} = 10 mV$, and the output voltage is V_0 . The output voltage is plotted versus time.

For $V_{CC} = 12 V$, the maximum output voltage for an envelope exceeding $10 V$ is obtained.

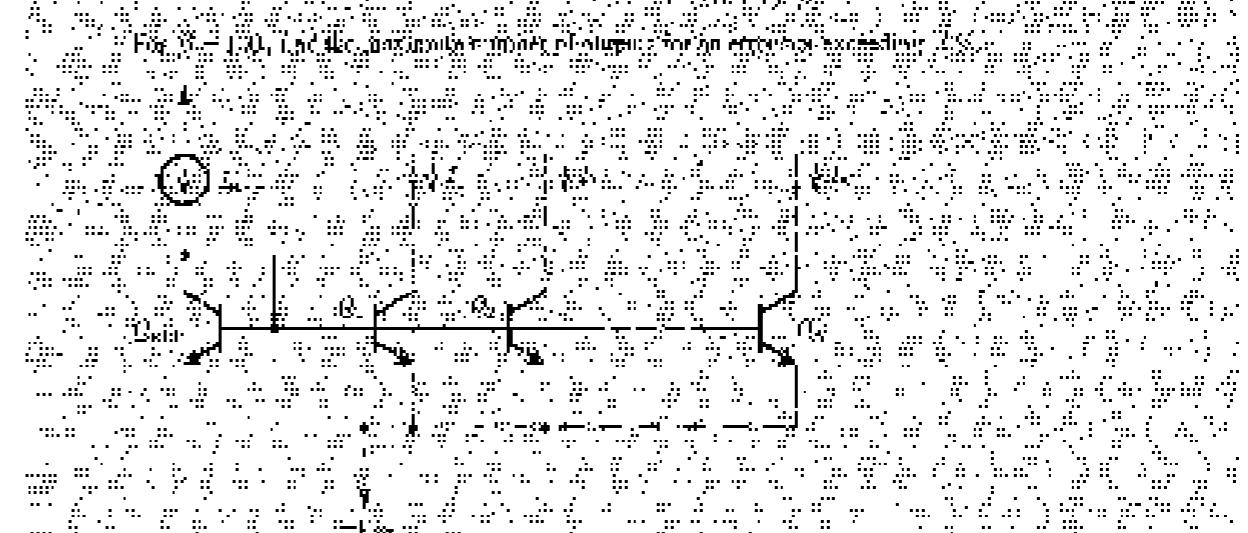


FIGURE 6.12

6.4 HIGH-FREQUENCY RESPONSE—GENERAL CONSIDERATIONS

The amplifier circuits we shall study in this chapter and the next are intended for fabrication using IC technology. Therefore they do not employ bypass capacitors. Moreover, the various stages in an integrated-circuit cascade amplifier are directly coupled; that is, they do not utilize

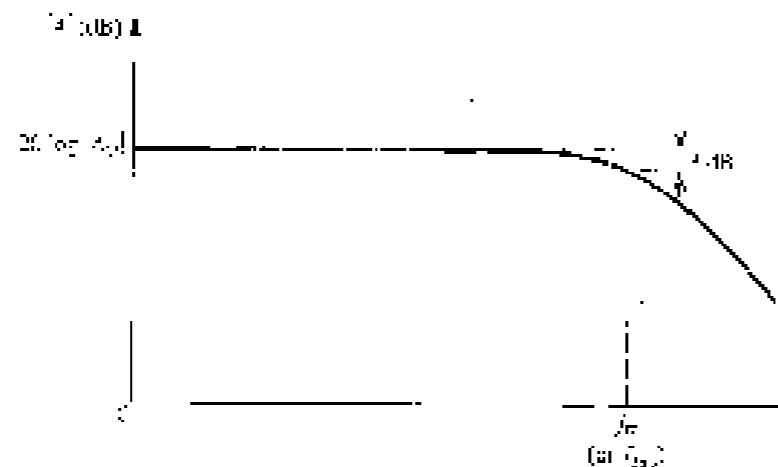


FIGURE 6.12 Frequency response of a direct-coupled JFET amplifier. (a) Bode plot of the magnitude of the low-frequency and dominant-gain \$A_0\$ extending to low frequencies.

single coupling capacitors, such as those we considered in Chapters 4 and 5.⁴ The frequency response of these direct-coupled JFET amplifiers takes the general form shown in Fig. 6.12, from which we note that the gain remains constant at its maximum value \$A_0\$ down to very low frequency (\$\omega_0\$). That is, compared to the capacitively coupled amplifiers that utilize bypass capacitors (Sections 4.9 and 5.9), direct-coupled JFET amplifiers do not suffer gain reduction at low frequencies. The gain, however, falls off at the high-frequency end due to the internal capacitances of the transistor. These capacitances, which are tabulated in the high-frequency device models in Table 6.3, represent the charge storage phenomena that take place inside the transistor.

The high-frequency responses of the CS and CF amplifiers were studied in Sections 4.9 and 5.9. In this chapter and the next, as we study a variety of IC amplifier configurations, we shall also consider their high-frequency behavior. Some of the tools needed for such a study are presented in this section.

6.4.1 The High-Frequency Gain Function

The amplifier gain, taking into account the internal transistor capacitances, can be expressed as a function of the complex-frequency variable \$s\$ in the general form

$$A(s) = A_{dc} F_H(s) \quad (6.29)$$

where \$A_{dc}\$ is the unclamped gain, which for the JFET amplifiers we are studying here is equal to the low-frequency value \$A_0\$. The value of \$A_{dc}\$ can be determined by analyzing the amplifier equivalent circuit while neglecting the effect of the transistor internal capacitances—hence, by assuming the transistors as perfect open circuits. By taking these capacitances into account,

⁴In some cases the designer may use one or two \$C_C\$ bypass coupling capacitors to connect the output of the IC amplifier to ground or to another load.

the gain acquires the factor \$F_H(s)\$, which can be expressed in terms of its poles and zeros,⁵ which are usually real as follows:

$$F_H(s) = \frac{(1 + s/\omega_1)(1 + s/\omega_2)\dots(1 + s/\omega_n)}{(1 - s/\omega_1)(1 + s/\omega_{n+1})\dots(1 + s/\omega_m)} \quad (6.30)$$

where \$\omega_1, \omega_2, \dots, \omega_n\$ are positive numbers representing the \$n\$ real poles and \$\omega_{n+1}, \omega_{n+2}, \dots, \omega_m\$ are positive, negative, or infinite numbers representing the conjugates of the \$m\$ real transmission zeros. Note from Eq. (6.30) that, as \$s\$ should be expected, as \$s\$ approaches 0, \$F_H(s)\$ approaches unity and the gain approaches \$A_{dc}\$.

6.4.2 Determining the 3-dB Frequency \$\omega_p\$

The amplifier designer usually is particularly interested in the part of the high-frequency band that is close to the midband. This is because the designer needs to estimate—and to generate manually—the value of the upper 3-dB frequency \$f_p\$ (or \$3\omega_p\$) for \$f_p = (\omega_p/2\pi)\$. Toward that end it should be mentioned that, in many cases the zeros are either at infinity or such high frequencies as to be of little significance to the determination of \$\omega_p\$. If in addition one of the poles, say \$\omega_{n+1}\$, is of much lower frequency than any of the other poles, then this pole will have the greatest effect on the gain of the amplifier \$A_{dc}\$. In other words, this pole will dominate the high-frequency response of the amplifier, and the amplifier is said to have a dominant-pole response. In such cases the function \$F_H(s)\$ can be approximated by

$$F_H(s) \approx \frac{1}{1 + s/\omega_p} \quad (6.31)$$

which is the transfer function of a first-order (or STC) low-pass network (Appendix B). It follows that if a dominant pole exists, then the determination of \$\omega_p\$ is greatly simplified:

$$\omega_p = \omega_{n+1} \quad (6.32)$$

This is the situation we encountered in the case of the emitter-source coupled amplifier in Section 4.9 and the IX TIEOJ-coupled amplifier analyzed in Section 5.9. As a rule of thumb, a dominant pole exists if the lowest-frequency pole is at least four times (a factor of 4) lower than the nearest pole or zero.

If a dominant pole does not exist, the 3-dB frequency \$\omega_p\$ can be determined from a plot of \$|F_H(j\omega)|\$. Alternatively, an approximate formula for \$\omega_p\$ can be derived as follows: Consider, for simplicity, the case of a circuit having two poles and two zeros in the high-frequency band, namely,

$$F_H(s) = \frac{(1 + s/\omega_1)(1 + s/\omega_2)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \quad (6.33)$$

Substituting \$s = j\omega\$ and taking the squared magnitude gives

$$|F_H(j\omega)|^2 = \frac{(1 + \omega^2/\omega_{p1}^2)(1 + \omega^2/\omega_{p2}^2)}{(1 + \omega^2/\omega_1^2)(1 + \omega^2/\omega_2^2)}$$

⁵At this point we assume that the reader is familiar with the subject of \$s\$-plane analysis and the concept of transfer-function poles and zeros as well as Bode plots. A brief review of this material is presented in Appendix A.

By definition, $\zeta = \omega_p / |\omega_B|^2 = \frac{1}{\zeta}$; thus,

$$\begin{aligned} \frac{1}{2} &= \frac{(1 + \omega_p^2/\omega_{p1}^2)(1 + \omega_p^2/\omega_{p2}^2)}{(1 + \omega_p^2/\omega_{p1}^2)(1 + \omega_p^2/\omega_{p2}^2)} \\ &= \frac{1 + \omega_p^2/\omega_{p1}^2 + 1 + \omega_p^2/\omega_{p2}^2 - \omega_p^2/\omega_{p1}^2\omega_{p2}^2}{1 + \omega_p^2(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2}) + \omega_p^2/\omega_{p1}^2\omega_{p2}^2} \quad (6.34) \end{aligned}$$

Since ω_B is usually smaller than the frequencies of all the poles and zeros, we may neglect the terms containing ω_B^2 and solve for ω_p to obtain

$$\omega_p \equiv \sqrt{\left(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2} + \frac{2}{\omega_{p1}^2\omega_{p2}^2}\right)} \quad (6.35)$$

This relationship can be extended to any number of poles and zeros as

$$\omega_p \equiv \sqrt{\left(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2} + \dots\right) + 2\left(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2} + \dots\right)^2} \quad (6.36)$$

Note that if one of the poles, say, P_1 , is dominant, then $\omega_p \approx \omega_{p1}$, $\omega_p \approx \omega_{p2}, \dots, \omega_{p1}, \omega_{p2}, \dots$, and Eq. (6.35) reduces to Eq. (6.33).

Example 6.3

The high-frequency response of an amplifier is characterized by the transfer function

$$F_H(s) = \frac{(1 + s/10^3)}{(1 + s/10^4)(1 + s/10^5)}$$

Determine the 3-dB frequency approximately and exactly.

Solution

Noting that the low-cut-frequency pole at 10^4 rad/s is two octaves lower than the second pole and a decade lower than the zero, we find that a dominant-pole situation already exists and $\omega_p = 10^4$ rad/s. A better estimate of ω_p can be obtained using Eq. (6.35), as follows:

$$\begin{aligned} \omega_p &= \sqrt{\left(\frac{1}{10^8} + \frac{1}{16 \times 10^8} + \frac{2}{10^8 \times 16 \times 10^8}\right)} \\ &= 9537 \text{ rad/s} \end{aligned}$$

The exact value of ω_p can be calculated from the given transfer function as 9537 rad/s. Finally, we show in Fig. 6.13 a Bode plot and an exact plot for the given transfer function. Note that this is a plot of the high-frequency response of the amplifier normalized relative to its midband gain. That is, if the midband gain is, say, 100 dB, then the entire plot should be shifted upward by 100 dB.

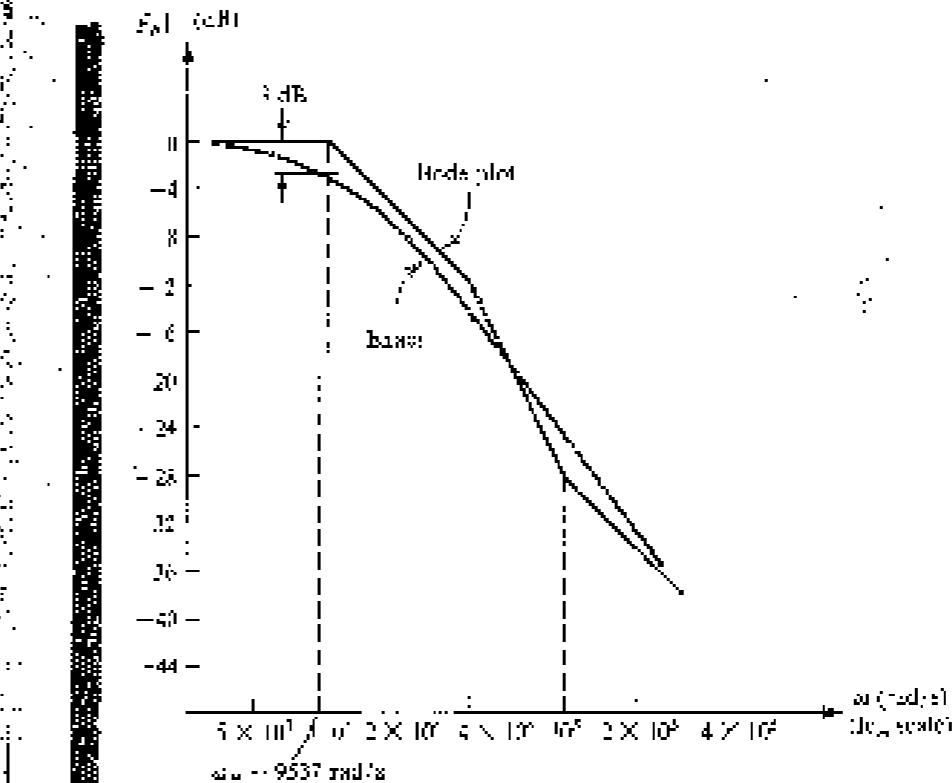


FIGURE 6.13 Normalized high-frequency response of the amplifier in Example 6.3.

6.4.3 Using Open-Circuit Time Constants for the Approximate Determination of f_H

If the poles and zeros of the amplifier transfer function can be determined easily, then we can determine f_H using the techniques above. In many cases, however, it is not a simple matter to determine the poles and zeros by quick-hand analysis. In such cases an approximate value for f_H can be obtained using the following method.

Consider the function $F_H(s)$ (Eq. 6.30), which determines the high-frequency response of the amplifier. The numerator and denominator factors can be multiplied out and $F_H(s)$ expressed in the alternative form

$$F_H(s) = \frac{1 - a_1 s + a_2 s^2 - \dots + a_n s^n}{1 + b_1 s + b_2 s^2 + \dots + b_m s^m} \quad (6.37)$$

where the coefficients a and b are related to the frequencies of the zeros and poles, respectively. Specifically, the coefficient b_1 is given by

$$b_1 = \frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}} + \dots + \frac{1}{\omega_{pn}} \quad (6.38)$$

It can be shown (see Gray and Sze 1996) that the value of b_1 can be obtained by considering the various capacitances in the high-frequency equivalent circuit one at a time while deducing all other capacitors as zero (or equivalently, replacing them with open circuits). That is, to obtain the contribution of capacitor C_j we reduce all other capacitors to zero.

reduce the input signal source to zero, and determine the resistance R_h seen by C_{in} . This process is then repeated for all other capacitors in the circuit. The value of b_1 is computed by summing the individual time constants, called **open-circuit time constants**,

$$b_1 = \sum_i C_i R_i \quad (6.43)$$

where we have assumed that there are no capacitors in the high-frequency equivalent circuit.

This method for determining b_1 is exact; the approximation comes about in using the value of b_1 to determine ω_h . Specifically, if the zeros are not dominant and if one of the poles, say P_1 , is dominant, then from Eq. (5.38),

$$\omega_h \approx \frac{1}{b_1} \quad (6.44)$$

that is, the upper 3-dB frequency will be approximately equal to ω_h , leading to the approximation

$$\omega_h \approx \frac{1}{b_1} = \frac{1}{\sum_i C_i R_i} \quad (6.45)$$

More should be pointed out that, in complex circuits, we usually do not know whether or not a dominant pole exists. Nevertheless, using Eq. (6.41) to determine ω_h normally yields remarkably good results even if a dominant pole does not exist. The method will be illustrated by an example.

Solution

The midband voltage gain is determined by assuming that the capacitors in the MOSFET model are perfect open circuits. This results in the midband equivalent circuit shown in Fig. 6.14(a), from which we find

$$\begin{aligned} A_M &= \frac{V_o}{V_{in}} = \frac{R_L'}{R_L' + R_{in}} \quad (\text{3-dB}) \\ &= \frac{420}{420 + 100} \times 10^3 = -10.0 \text{ V/V} \end{aligned}$$

We shall determine ω_h using the method of open-circuit time constants. The resistance R_h seen by C_{in} is found by setting $C_{\text{in}} = 0$ and short-circuiting the input signal source V_{in} . This results in the circuit

¹The method of open-circuit time constants yields good results only when all the poles are real, as is the case in this chapter.

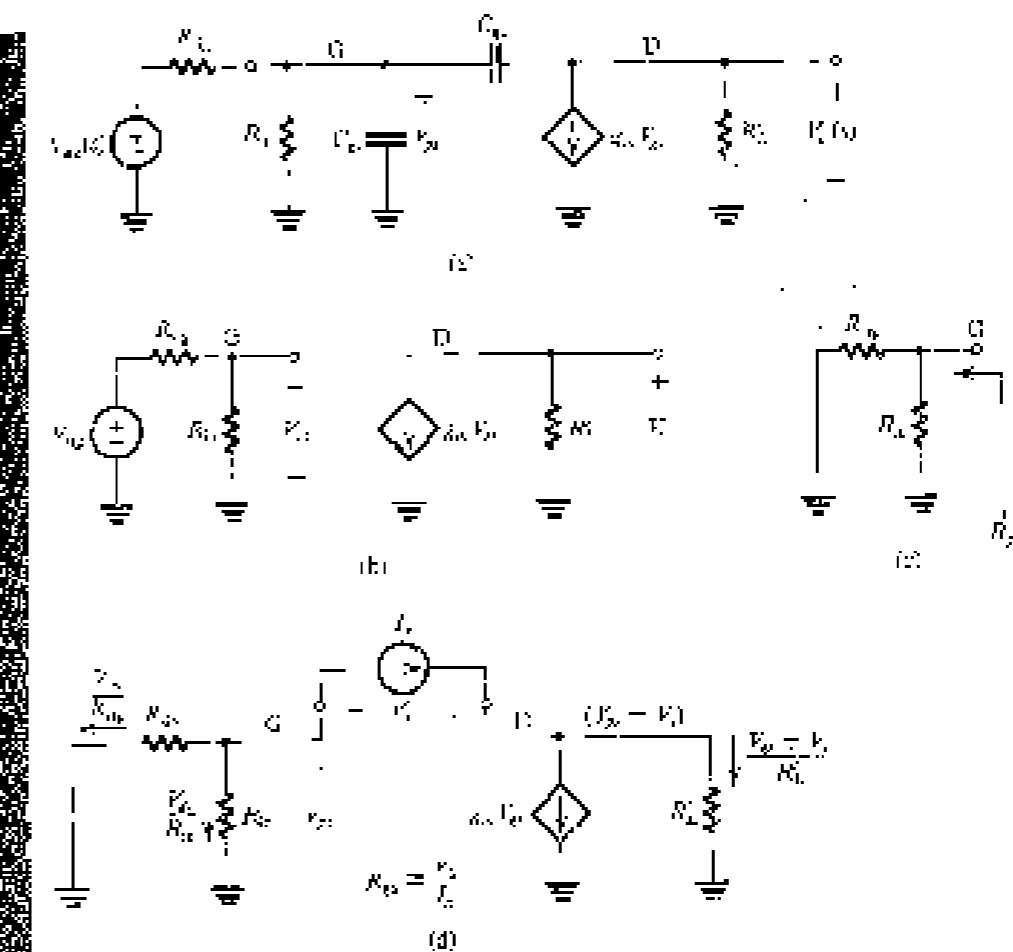


FIGURE 6.14 Circuits for Exercise 6.5: (a) high-frequency equivalent circuit of a MOSFET amplifier; (b) AC equivalent circuit at midband frequencies; (c) circuit for determining the resistance seen by C_{in} ; and (d) circuit for determining the resistance seen by C_2 .

of Fig. 6.14(c), from which we find that

$$R_{in} = R_{in} || R_{ds} = 420 \text{ k}\Omega || 10^3 \text{ m}\Omega = 80.8 \text{ }\mu\Omega$$

Thus the open-circuit time constant is $C_{in} R_{in}$

$$t_{\text{on}} = C_{in} R_{in} = 1 \times 10^{-12} \times 80.8 \times 10^{-3} = 80.8 \text{ ps}$$

The resistance R_h seen by C_{in} is found by setting $C_{in} = 0$ and short-circuiting V_{in} . The result is the circuit in Fig. 6.14(c), to which we apply a test current I_s . Writing a node equation at G gives

$$I_s = -\frac{V_{in} - V_s}{R_{in} + R_{ds}}$$

Thus,

$$V_{in} = -I_s R' \quad (6.46)$$

where $R' = R_{ds}/R_{ds}$. A node equation at D provides

$$I_D = g_m V_{DS} + \frac{V_{DS} - V_S}{R'_D}$$

Substituting the V_{DS} from Eq. (6.42) and rearranging terms yields

$$g_m \frac{V_S}{I_D} = R' + R_D^2 + g_m R'_D R_D = 1.6 \text{ MO}$$

Thus the open-circuit time constant of C_{DS} is

$$\tau_{OC} = C_{DS} R_{DS} \\ = 1.6 \times 10^{-12} \times 1.16 \times 10^5 = 1160 \text{ ns}$$

The upper 3-dB frequency ω_3 can now be determined from

$$\omega_3 = \frac{1}{\tau_{OC} + R_D} \\ = \frac{1}{(0.00116 \times 10^5) \times 10^5} = 870 \text{ rad/s}$$

Thus,

$$f_H = \frac{\omega_3}{2\pi} = 139.5 \text{ kHz}$$

The method of open-circuit time constants has an important advantage in that it tells the circuit designer which of the various capacitances is significant in determining the amplifier frequency response. Specifically, the relative contribution of the various capacitances to the effective time constant τ_{OC} is immediately obvious. For instance, in the above example we see that C_{DS} is the dominant capacitance in determining f_H . We also note that, in effect, increasing C_{DS} (either we use a MOSFET with smaller C_{DS} , or, for a given MOSFET, we reduce R_{DS} by using a smaller K' or R_D^2) if R_D^2 is fixed, for a given MOSFET the only way to increase bandwidth is by reducing the load resistance. Unfortunately, this also decreases the midband gain. This is an example of the usual trade-off between gain and bandwidth, a common circumstance which was mentioned earlier.

6.4.4 Miller's Theorem

In our analysis of the high-frequency response of the common-source amplifier (Section 4.3), and of the common-emitter amplifier (Section 5.3), we employed a technique for regarding the bridging capacitances (C_{DS} or C_J) by an equivalent input resistance. This very useful and effective technique is based on a general theorem known as Miller's theorem, which we now present.

Consider the situation in Fig. 6.15(a). As part of a larger circuit (not shown), we have isolated two circuit nodes, labeled 1 and 2, between which an impedance Z is connected. Nodes 1 and 2 are also connected to other parts of the circuit, as signified by the broken lines emanating from the two nodes. Furthermore, it is assumed that somewhere it has been determined that the voltage at node 2 is related to that at node 1 by

$$V_2 = KV_1 \quad (6.43)$$

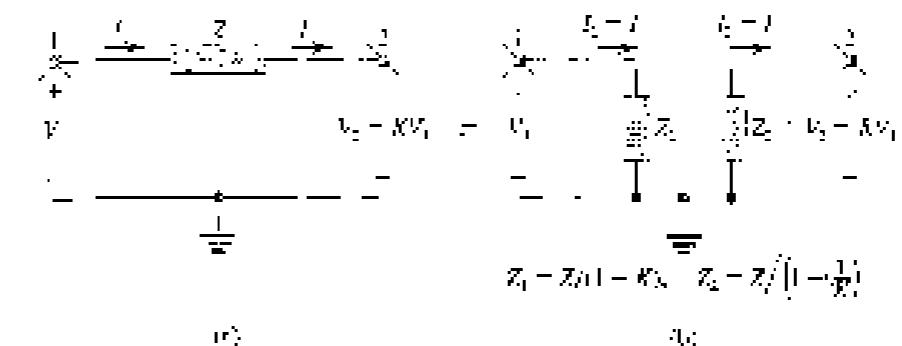


FIGURE 6.15 The Miller equivalent circuit.

In typical situations K is a gain factor that can be positive or negative and that has a magnitude usually larger than unity. This, however, is not an assumption for Miller's theorem.

Miller's theorem states that: Impedance Z can be replaced by two impedances: Z_1 , connected between node 1 and ground and Z_2 , connected between node 2 and ground, where

$$Z_1 = Z/(1-K) \quad (6.44a)$$

and

$$Z_2 = Z/(1-\frac{1}{K}) \quad (6.44b)$$

to obtain the equivalent circuit shown in Fig. 6.15(b).

The proof of Miller's theorem is achieved by deriving Eq. (6.44) as follows: In the original circuit of Fig. 6.15(a), the only way that node 1 "feels the existence" of impedance Z is through the current I that Z draws away from node 1. Therefore, to keep the current unchanged in the equivalent circuit, we must choose the value of Z_1 so that I draws an equal current,

$$I_1 = \frac{V_1 - V_2 - KV_1}{Z_1} = \frac{V_1 - KV_1}{Z_1}$$

which yields the value of Z_1 in Eq. (6.44a). Similarly, to keep the current into node 2 unchanged, we must choose the value of Z_2 so that

$$I_2 = \frac{V_2 - V_1 - KV_1}{Z_2} = \frac{V_2 - KV_1}{Z_2}$$

which yields the expression for Z_2 in Eq. (6.44b).

Although not highlighted, the Miller equivalent circuit derived above is valid only as long as the rest of the circuit remains unchanged; otherwise the ratio of V_2 to V_1 might change. It follows that the Miller equivalent circuit cannot be used directly to determine the output resistance of an amplifier. This is because in determining output resistances it is implicitly assumed that the source signal is reduced to zero and that a low-signal source voltage or current is applied to the output terminals. Obviously a major change in the circuit concerning the Miller equivalent circuit no longer valid.

Example 8.6

Figure 8.6(a) shows an ideal voltage amplifier having a gain of -100 V/V with an input resistance $Z_{in} = 10 \text{ k}\Omega$, between its output and input terminals. Find the Miller equivalent circuit when Z is (a) a $1\text{-M}\Omega$ resistance, and (b) a 1-pF capacitance. In each case, use the equivalent current to determine V_{out}/V_{in} .

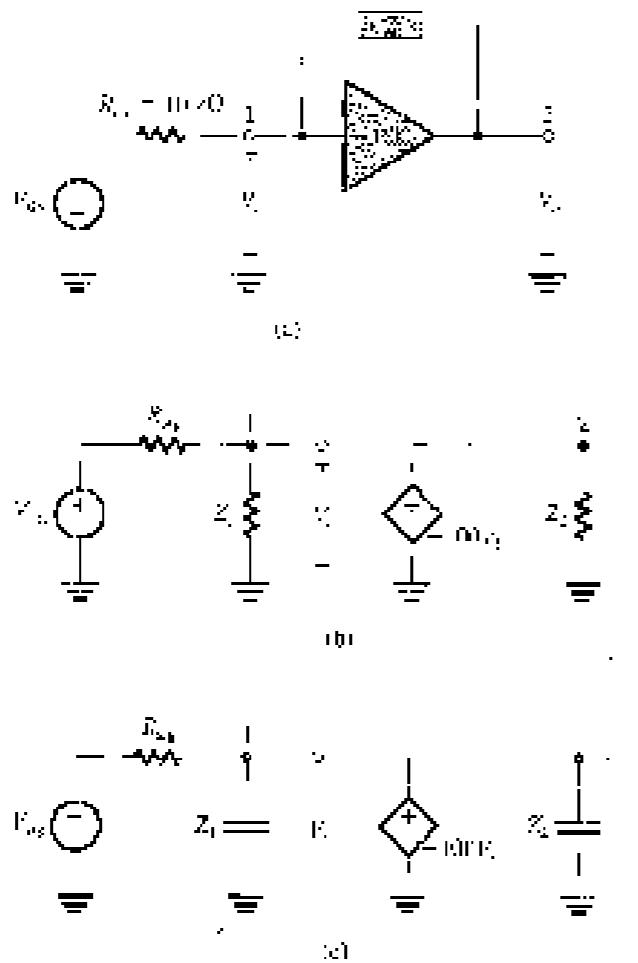


FIGURE 8.16 Circuits for Example 8.6.

Solution

(a) For $Z = 1\text{-M}\Omega$, employing Miller's theorem results in the equivalent circuit in Fig. 8.16(b), where

$$Z_1 = \frac{Z}{1+K} = \frac{1000 \text{ k}\Omega}{1+100} = 9.0 \text{ k}\Omega$$

$$Z_2 = \frac{Z}{1-K} = \frac{1 \text{ M}\Omega}{1-\frac{1}{100}} = 0.99 \text{ M}\Omega$$

The voltage gain can be found as follows:

$$\begin{aligned} \frac{V_o}{V_{in}} &= \frac{V_o}{V_z V_{in}} = \frac{100 \times Z}{Z_1 + R_{in}} \\ &= 100 \times \frac{9.0}{10 + 10} = 49.0 \text{ V/V} \end{aligned}$$

(b) For $Z = 1\text{-pF}$ capacitance—that is, $Z = 1/j\omega C = 1/2 \times 1 \times 10^{-12} \text{ } \Omega$ —applying Miller's theorem allows us to replace Z by Z_1 and Z_2 , where

$$\begin{aligned} Z_1 &= \frac{Z}{1-K} = \frac{1/2 \times 10^{-12}}{1-100} = 1.0 \times 10^{-12} \text{ } \Omega \\ Z_2 &= \frac{Z}{1-K} = \frac{1}{1-100} = 1.0 \times 10^2 \text{ } \Omega \end{aligned}$$

It follows that Z_1 is a resistance $1/2 \times 10^{-12} \text{ } \Omega = 5.0 \text{ p}\Omega$ and Z_2 , Z_1 is a capacitance $1/100 = 1.0 \text{ pF}$. The resulting equivalent circuit is shown in Fig. 8.16(c), from which the voltage gain can be found as follows:

$$\begin{aligned} \frac{V_o}{V_{in}} &= \frac{V_o}{V_z V_{in}} = -100 \frac{Z_1}{1/(j\omega C_1) + R_{in}} \\ &= \frac{-100}{1 + 5.0 \times 10^{-12} \times 1 \times 10^{-12} \times 10 \times 10^3} \\ &= -100 \frac{1}{1 + 5.0 \times 10^{-2}} \end{aligned}$$

This is the transfer function of a first-order low-pass network with a gain of -100 and a 3-dB corner frequency f_{3dB} of

$$f_{3dB} = \frac{1}{2\pi \times 5.0 \times 10^{-12}} = 107.9 \text{ kHz}$$

From Example 8.7, we observe that the Miller replacement of a feedback or adding resistance results, for a negative K , in a smaller resistance [by a factor $(1-K)$] at the input. If the feedback element is a capacitance, its value is multiplied by $(1-K)$ to obtain the equivalent capacitance at the input side. The multiplication of a feedback capacitance by $(1-K)$ is referred to as **Miller multiplication**, or **Miller effect**. We have encountered the Miller effect in the analysis of the CS and CB amplifiers in Sections 4.9 and 5.9, respectively.

EXERCISES

- 8.4-1 A voltage-controlled voltage source has a transconductance of 100 mA/V and is connected to a load of $10 \text{ k}\Omega$. The source is fed back through a 100 pF capacitor to the gate. Find the gain of the circuit and the 3-dB corner frequency.
- 8.4-2 A voltage-controlled voltage source has a transconductance of 100 mA/V and is connected to a load of $10 \text{ k}\Omega$. The source is fed back through a 100 pF capacitor to the gate. Find the gain of the circuit and the 3-dB corner frequency.

Ans. 2.79 dB³

6.11 For the amplifier described in Exercise 6.10, find the exact small-signal current values (using Eq. 6.36) of i_{D1} (in A) for $i_{D2} = 0$, in the cases $V_g = 1, 2$, and 4.

Ans. 0.14, 0.19, 0.35, 0.59

6.12 For the amplifier in Exercise 6.10, calculate the output voltage v_o for $i_{D1} = 0.14$ A and $i_{D2} = 0.35$ A. Assume $V_g = 1$.

Ans. 1.59 V

6.13 In Miller's discussion of performance of low-inertia MOSFETs shown in Fig. 6.13, assume the device to be a load *CS* stage having a finite transconductance A_g . With this in mind, repeat the analysis of the amplifier in Example 6.12, but with $V_g = 1$ V. Calculate the following values: (a) i_{D1} , (b) i_{D2} , (c) v_o , (d) A_v , (e) R_o , and (f) R_s .

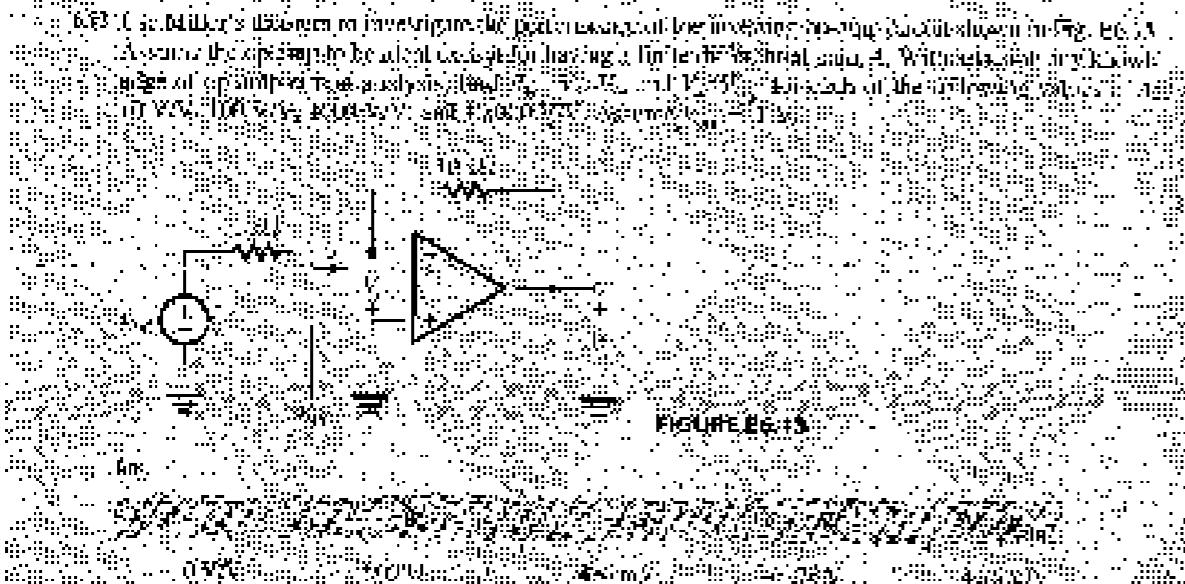


FIGURE 6.17(a)

6.5 THE COMMON-SOURCE AND COMMON-EMITTER AMPLIFIERS WITH ACTIVE LOADS

6.5.1 The Common-Source Circuit

Figure 6.17(b) shows the most basic IC MOS amplifier. It consists of a grounded-source MOS transistor with the drain resistor R_D replaced by a constant-current source I . As we shall see shortly, the current-source load can be implemented using a PMOS transistor and is here also called an active load, and the CS amplifier in Fig. 6.17(a) is said to be active-loaded.

Before considering the small-signal operation of the active-loaded CS amplifier, a word on its dc bias design is in order. Obviously, φ_2 is biased at $V_D = V$, but what determines the dc voltages at the drain and at the gate? Usually, this circuit will be part of a larger circuit in which negative feedback is utilized to fix the values of V_{D1} and V_{G1} . We shall encounter

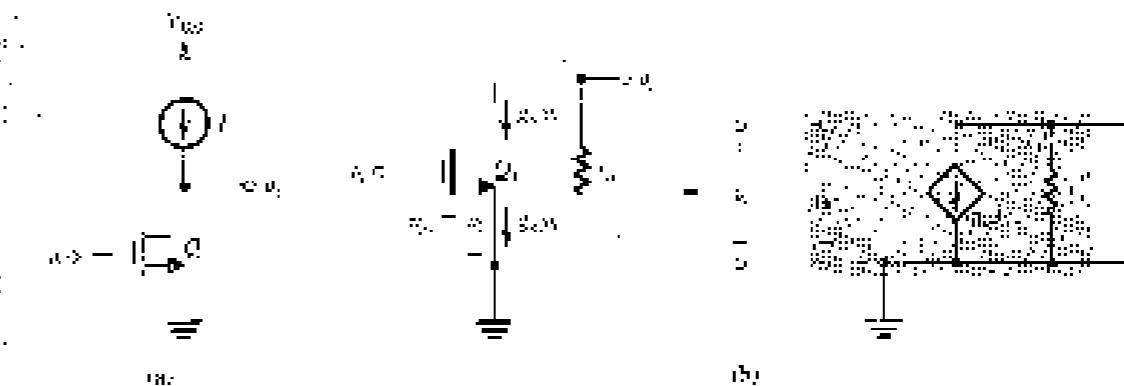


FIGURE 6.17 (a) Small-signal model of the circuit in Fig. 6.17(a); (b) the circuit diagram.

examples of such circuitry in later chapters. For the time-being, however, we shall assume that the MOSFET is biased in open-loop in the saturation region.³

Small-signal analysis of the current-source-loaded CS amplifier is straightforward and is illustrated in Fig. 6.17(b). Here, along with the equivalent circuit model, we show the transistor with its r_o extracted and displayed separately and with the analysis performed directly on the circuit. From Fig. 6.17(b) we see that for this CS amplifier,⁴

$$R_s \rightarrow \infty \quad (6.45a)$$

$$A_{v0} = -g_m R_s \quad (6.45b)$$

$$R_o = r_o \quad (6.45c)$$

We note that A_{v0} in Eq. (6.45b) is the maximum voltage gain available from a common-source amplifier, namely the intrinsic gain of the MOSFET.

$$A_{v0} = g_m r_o \quad (6.46)$$

Recall that in Section 6.2 we discussed in some detail the intrinsic gain A_g and presented in Table 6.3 formulas for its determination.

EXERCISE

6.14 For a NMOS transistor fabricated in a 1.5- μm CMOS process for which $k' = 200 \mu\text{A}/\text{V}^2$ with $V_A = 20 \text{ V}$ and the transconductance A_g (drain current vs. drain-to-gate voltage) of -10 mA/V , what is the drain current i_D at $V_D = 10 \text{ V}$ and $V_G = 1.5 \text{ V}$? What is the value of the drain-to-gate voltage V_{GD} at this point?

6.5.2 CMOS Implementation of the Common-Source Amplifier

A CMOS circuit implementation of the common-source amplifier is shown in Fig. 6.18(a). This circuit is based on that shown in Fig. 6.17(a) with the load current-source I implemented using resistor φ_2 . The latter is the output transistor of the current mirror formed by φ_1 and φ_2 and fed with the bias current I_{BBP} . We shall assume that φ_1 and φ_2 are matched; thus the

³ For the circuit of Fig. 6.17(a), used in classmate amplifiers, the reader should consult Table 1.3.

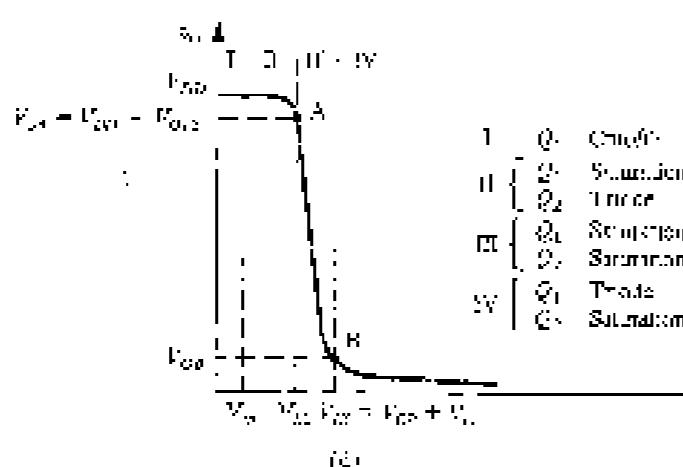
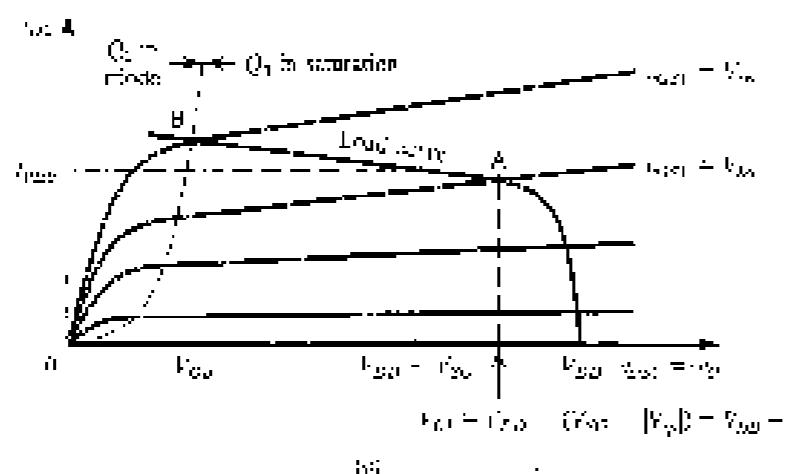
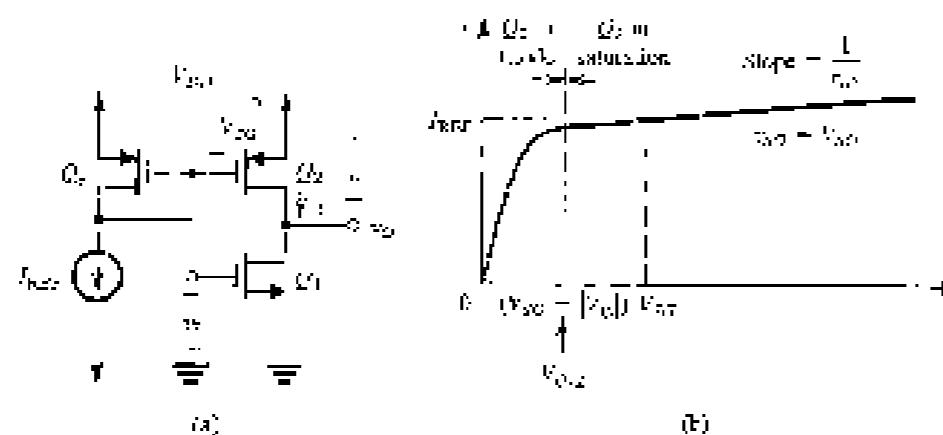


FIGURE 6.1B: The CMOS common-source amplifier: (a) circuit; (b) transfer characteristic of the source-load; (c) empirical representation to determine the transfer characteristic and full transfer characteristics.

load characteristic of the load device will be that shown in Fig. 6.1B(c). This is simply the $v_{ds}-v_{gs}$ characteristic curve of the p-channel transistor Q_2 in a constant source-gate voltage V_{gs2} . The value of V_{gs2} is set by passing the reference bias current I_{ref} through Q_1 . Observe that, as expected, Q_2 behaves as a current source when it operates in saturation, which in turn is ensured when $v_{ds2} > v_{ds20}$ ($V_{ds2} = V_{ds20} + |V_{ds}|V_{ds20}$), where $|V_{ds}|$ is the magnitude of the negative voltage across Q_2 and Q_2 is operating. When Q_2 is in saturation, it exhibits a finite load incremental resistance r_{ds2} :

$$r_{ds2} = \frac{V_{ds2}'}{I_{ref}} \quad (6.47)$$

where V_{ds2}' is the Early voltage of Q_2 . In other words, the current source load is not ideal but has a finite output resistance equal to the transistor r_{ds2} .

Before proceeding to determine the small-signal voltage gain of the amplifier, it is instructive to examine its transfer characteristic, v_{ds} versus v_{gs} . This can be determined using the graphical construction shown in Fig. 6.1B(c). Here we have plotted the $v_{ds}-v_{gs}$ characteristics of the amplifying transistor Q_1 and superimposed the load curve on them. The latter is simply the $v_{ds}-v_{gs}$ curve in Fig. 6.1B(a) "flipped around" and shifted V_{ds20} volts along the horizontal axis. Note, since $v_{ds2} = v_{gs}$, each of the $v_{ds}-v_{gs}$ curves corresponds to a particular value of v_{gs} . The intersection of each particular curve with the load curve gives the corresponding value of v_{ds2} , which is equal to v_{ds} . Thus, in this way, we can obtain the $v_{ds}-v_{gs}$ characteristic point by point. The resulting transfer characteristic is sketched in Fig. 6.1B(d). As indicated, this has four distinct segments, labeled I, II, III, and IV, each of which is obtained for one of the four combinations of the modes of operation of Q_1 and Q_2 , which are also indicated in the diagram. Note also the two break points on the transfer characteristic (A and B) in Fig. 6.1B(d). We urge the reader to carefully study the transfer characteristic and its various details.

Not surprisingly, for amplifier operation segment II is the one of interest. Observe that in region II the transfer curve is almost linear and is very steep, indicating large voltage gain. In region III both the amplifying transistor Q_1 and the load transistor Q_2 are operating in saturation. The end points of region III are A and B; at A, defined by $v_{gs} = V_{gs20} - V_{ds20}$, Q_1 enters the triode region, and at B, defined by $v_{gs} = V_{gs20} + V_{ds20}$, Q_1 enters the triode region. When the admittance is raised at a point in region III, the small-signal voltage gain can be determined by replacing Q_1 with its small-signal model and Q_2 with its output resistance, r_{ds2} . The output resistance of Q_2 constitutes the load resistance of Q_1 . The voltage gain A_{ds} can be found by substituting the results from Eq. (6.45) into

$$A_{ds} = \frac{v}{v_{gs}} = A_{ds1} \frac{R_{ds2}}{R_{ds1} + R_{ds2}} \quad (6.48)$$

to obtain

$$A_{ds} = (g_{m1} r_{ds2}) \frac{r_{ds2}}{r_{ds1} + r_{ds2}} = g_{m1} (r_{ds1} || r_{ds2}) \quad (6.49)$$

indicating that, as expected, A_{ds} will be lower in magnitude than the intrinsic gain of Q_1 , $g_{m1} r_{ds1}$. For the case $r_{ds1} = r_{ds2}$, A_{ds} will be $g_{m1} r_{ds1}/2$. The result in Eq. (6.49) could, of course, have been obtained directly by multiplying $g_{m1} r_{ds1}$ by the total resistance between the output node and ground, $r_{ds1} + r_{ds2}$.

The CMOS common-source amplifier can be designed to provide voltage gains of 10 to 100. It exhibits a very high input resistance; however, its output resistance is also high.

Two final comments need to be made before leaving the common-source amplifier:

1. The circuit is not affected by the body effect since the source terminals of both Q_1 and Q_2 are at signal ground.
2. The circuit is usually part of a larger amplifier circuit (as will be shown in Chapters 7 and 9), and negative feedback is utilized to ensure that the circuit in fact operates in region II of the amplifier transfer characteristics.

Example 6.1

Consider the CMOS common-source amplifier in Fig. 6.1(a) for the case $V_{DD} = 5$ V, $V_{SS} = |V_{DD}| = 0.5$ V, $\mu_nC_{ox} = 200 \mu\text{A/V}^2$, and $\mu_pC_{ox} = 0.5 \mu\text{A/V}^2$. Both transistors, $L = 0.4 \mu\text{m}$ and $W = 2 \mu\text{m}$. Also, $V_{in} = 20$ mV, $V_{D1} = 0$ V, and $I_{SD1} = 100 \mu\text{A}$. Find the small-signal voltage gain. Also, find the coordinates of the extremes of the amplifier region of the transfer characteristic (regions points A and B).

Solution

$$\begin{aligned} g_{sd1} &= \frac{1}{2} \frac{\mu_n C_{ox}}{L} \frac{W}{V_{DD}} I_{SD1} \\ &= \frac{1}{2} \times 200 \times \frac{4}{0.4} \times 100 = 1.0 \text{ mA/V} \\ r_{ds1} &= \frac{V_{DD}}{I_{SD1}} = \frac{5}{0.1 \text{ mA}} = 50 \text{ k}\Omega \\ r_{ds2} &= \frac{V_{DD}}{I_{SD2}} = \frac{10 \text{ V}}{0.1 \text{ mA}} = 100 \text{ k}\Omega \end{aligned}$$

Thus,

$$\begin{aligned} A_v &= -r_{ds1}/(r_{ds1} + r_{ds2}) \\ &= -0.65(\text{mA/V})/(200 + 100/\text{k}\Omega) = -0.3 \text{ V/V} \end{aligned}$$

The extremes of the amplifier region of the transfer characteristic (region III) are found as follows: Refer to Fig. 6.1(b). First, we determine V_{DS1} of Q_1 and Q_2 corresponding to $I_D = I_{SD1} = 100 \mu\text{A}$ using

$$I_D = \frac{1}{2} \frac{\mu_n C_{ox}}{L} \frac{W}{V_{DD} - V_{DS}} \left[V_{DS} - \frac{V_{DD}}{|V_{DS}|} \right]$$

Thus,

$$0.1 = \frac{1}{2} \times 200 \left(\frac{4}{0.4} \right) \frac{100}{|V_{DS}|} \left[1 - \frac{5}{|V_{DS}|} \right] \quad (6.30)$$

where $|V_{DS}|$ is the magnitude of the drain-to-source voltage at which Q_1 and Q_2 are operating, and we have used the fact that $V_{DS1} = V_{DS2}$. Equation (6.30) can be rearranged to the form

$$0.29 = \frac{1}{|V_{DS}|} \left[1 + 0.04 |V_{DS}| \right]$$

which by trial-and-error yields

$$|V_{DS}| = 0.55 \text{ V}$$

thus

$$V_{DS} = 0.5 - 0.55 = -0.5 \text{ V}$$

and

$$V_{DD} - V_{DS} = V_{DD} = 5.5 \text{ V}$$

To find the corresponding value of v_o , V_{DD} , we derive an expression for v_o versus v_i in region III. Noting that in region III Q_1 and Q_2 are in saturation and obviously conduct equal currents, we can write

$$\begin{aligned} i_{D1} &= i_{D2} \\ \frac{1}{2} \frac{\mu_n C_{ox}}{L} \frac{W}{V_{DD}} (v_i - V_{DS})^2 &= \frac{1}{2} \frac{\mu_p C_{ox}}{L} \frac{W}{V_{DD}} (V_{DD} - V_{DS})^2 + \frac{V_{DD} - v_o}{|V_{DS}|} \end{aligned}$$

Substituting numerical values, we obtain

$$8.52(v_i - 0.5)^2 = \frac{1 - 0.08 v_o}{1.05 v_o}$$

which can be rearranged to the form

$$v_o = 7.00 - 55.77(v_i - 0.5)^2 \quad (6.31)$$

This is the equation of segment III of the transfer characteristic. Although it includes v_i , the reader should not be alarmed: Because region III is very narrow, v_i changes very little, and the characteristic is nearly linear. Substituting $v_i = 2.47$ V gives the corresponding value of v_o ; that is, $v_o = 0.88$ V. To determine the coordinates of B, we note that they are defined by $V_{DS} = V_{DD} - V_{DS}$. Substituting in Eq. (6.31) and solving gives $V_{DS} = 0.93$ V and $V_{DD} = 0.55$ V. The width of the amplifier region is therefore

$$\Delta v_i = V_{DS} - V_{DD} = 0.05 \text{ V}$$

and the corresponding output voltage is

$$\Delta v_o = V_{DD} - V_{DS} = -0.14 \text{ V}$$

Thus the "dc/dc-signal" voltage gain is

$$\frac{\Delta v_o}{\Delta v_i} = \frac{-0.14}{0.05} = -2.8 \text{ V/V}$$

which is very close to the small-signal value of -2 , indicating that segment III of the transfer characteristic is quite linear.

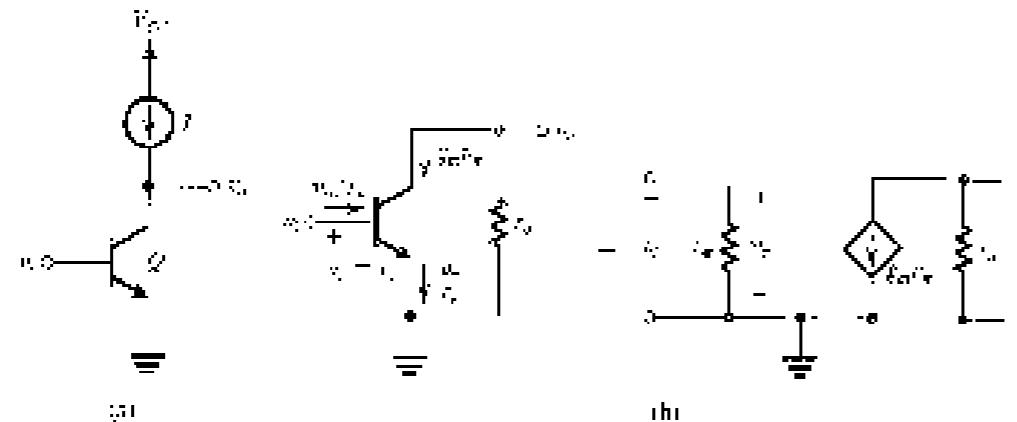


FIGURE 6.19 Two active load common-emitter amplifiers. (a) Small-signal analysis of the amplifier in (a), performed here directly on the bias and using the hybrid-pi model explicitly.

6.5.3 The Common-Emitter Circuit

The active-loaded common-emitter amplifier, shown in Fig. 6.19(b), is similar to the active-loaded common-source circuit studied above. Here also, the bias-stabilizing circuit is not shown. Small-signal analysis is similar to that for the MOS case and is illustrated in Fig. 6.19(b). The results are

$$R_i = r_o \quad (6.52a)$$

$$A_{v1} = -g_m r_o \quad (6.52b)$$

$$R_o = r_o \quad (6.52c)$$

which except for the rather low input resistance \$r_o\$ are similar to the MOSFET case. Recall, however, from the comparison of Section 6.2 that the intrinsic gain \$g_m r_o\$ of the BJT is much higher than that for the MOSFET. This advantage, however, is counterbalanced by the practically infinite input resistance of the common-source amplifier. Further comparisons of the two amplifier types were presented in Section 6.2.

EXERCISE

- 6.16 Consider the active-loaded CE amplifier where the output current source is again converted with a factor of 10. Let \$I = 10 \mu\text{A}\$, \$V_{DD} = 10 \text{ V}\$, the load through the junction capacitance, and \$\beta = 100\$. If the input voltage is \$V_{s1} = 10 \text{ mV}\$, find the output voltage \$V_{o1}\$ and the output current \$I_{o1}\$. Assume \$25 \text{ pF}\$ for \$C_{o1}\$, \$25 \text{ pF}\$ for \$C_{s1}\$, \$1000 \text{ pF}\$ for \$C_{j1}\$, and \$100 \text{ pF}\$ for \$C_{j2}\$. The input resistance is \$10 \text{ M}\Omega\$.

6.6 HIGH-FREQUENCY RESPONSE OF THE CS AND CE AMPLIFIERS

We now consider the high-frequency response of the active-loaded common-source and common-emitter amplifiers. Figure 6.20 shows the high-frequency equivalent circuit of the common-source amplifier. This equivalent circuit applies equally well to the CE amplifier with a simple relabeling; if a dependent \$C_{s1}\$ would be replaced by \$C_s\$, \$C_{s2}\$, \$C_{j1}\$, \$C_{j2}\$, and obviously \$V_{s1}\$ by \$V_s\$.

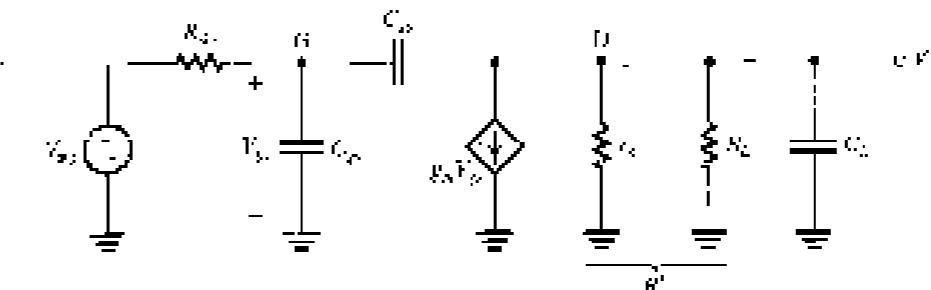


FIGURE 6.20 High-frequency equivalent circuit of the common-source amplifier. For the common-emitter amplifier, the values of \$R_1\$ and \$R_2\$ are modified (as in Figure 6.19) and \$C_{j1}\$ and \$C_{j2}\$ are replaced by \$C_{s1}\$, \$C_{s2}\$ by \$C_s\$, and \$C_{j1}\$ by \$C_{j2}\$.

The input-signal source is represented by \$V_{s1}\$ and \$R_{s1}\$. In some cases, however, \$V_{s1}\$ and \$R_{s1}\$ could be modified values of the signal-source voltage and internal resistance, taking into account other resistive components such as a bias resistor \$R_1\$ or \$R_2\$, the BJT resistances \$r_o\$ and \$r_{ce}\$, etc. We have seen examples of this kind of circuit simplification in Sections 4.9 and 5.9. The load resistance \$R_L\$ represents the combination of an actual load resistance (if one is connected) and the output resistance of the current-source load. To avoid loss of gain, \$R_L\$ is usually on the same order as \$r_o\$. We combine \$R_L\$ with \$r_o\$ and denote their parallel equivalent \$R_L'\$. The load capacitance \$C_L\$ represents the total capacitance between drain (or collector) and ground; it includes the drain-to-body capacitance \$C_{db}\$ (collector-to-substrate capacitance), the input capacitance of a succeeding amplifier stage, and in some cases, as we will see in later chapters, a deliberately introduced capacitance. In IC MOS amplifiers, \$C_L\$ can be relatively substantial.

6.6.1 Analysis Using Miller's Theorem

In situations when \$R_{s1}\$ is relatively large and \$C_L\$ is relatively small, Miller's theorem can be used to obtain a quick but approximate estimate of the 3-dB frequency \$f_3\$. We have already done this in Section 4.9 for the CS amplifier and in Section 5.9 for the CE amplifier. Therefore, here we will only state the result. Figure 6.21 shows the approximate equivalent circuit obtained for the CS case, from which we see that the amplifier has a dominant pole formed

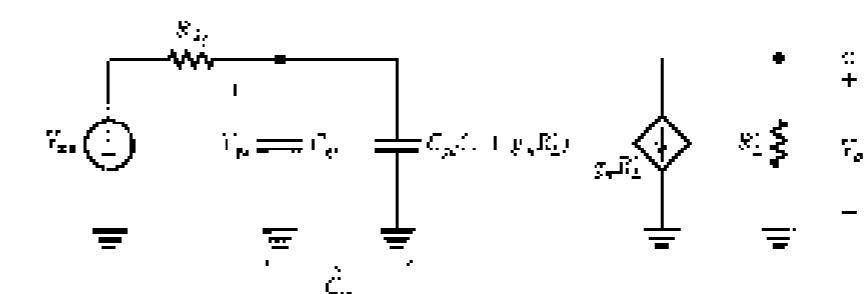


FIGURE 6.21 Approximate equivalent circuit obtained by applying Miller's theorem, using a neg source \$C_L\$ and the load current component supplied by \$g_m V_o\$. This model works reasonably well when \$R_{s1}\$ is large and the amplifier has a low voltage step-up, as is dominated by the pole formed by \$R_{s1}\$ and \$C_{s1}\$.

by R_{in} and C_{in} . Thus,

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A_{\text{in}}}{1 + \frac{1}{\omega_{\text{in}} t_{\text{in}}}} \quad (6.56)$$

where

$$A_{\text{in}} = -g_m R_L'$$

and the 3-dB frequency $f_{\text{in}} = \omega_{\text{in}}/2\pi$ is given by

$$f_{\text{in}} = \frac{1}{2\pi C_{\text{in}} R_{\text{in}}} \quad (6.57)$$

where

$$C_{\text{in}} = C_{\text{gs}} + C_{\text{gd}} (1 - g_m R_L) \quad (6.58)$$

6.6.2 Analysis Using Open-Circuit Time Constants

The method of open-circuit time constants presented in Section 6.4.3 can be directly applied to the CS equivalent circuit of Fig. 6.20, as illustrated in Fig. 6.22, from which we see that the resistance seen by C_{gs} , $R_{\text{eq}} = R_{\text{in}}$, and that seen by C_{gd} is R_L' . The resistance R_{in} seen by C_{gs} can be found by analyzing the circuit of Fig. 6.22(b) with the result that

$$R_{\text{in}} = R_{\text{in},0} \left(1 + g_m R_L' \right) + R_L \quad (6.59)$$

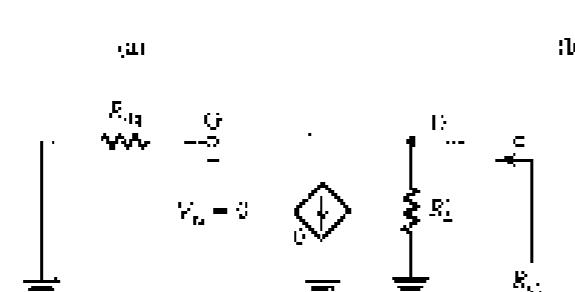
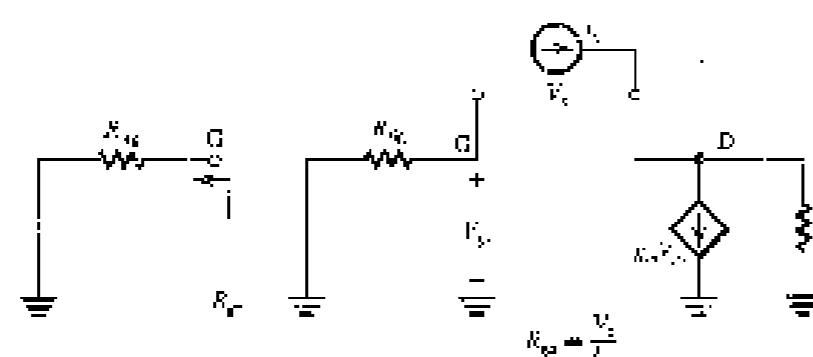


FIGURE 6.22 Application of the open-circuit time constants method to the CS equivalent circuit of Fig. 6.20.

Thus the effective time-constant δ_1 or t_{in} can be found as

$$\begin{aligned} \delta_1 &= C_{\text{gs}} R_{\text{in}} + C_{\text{gs}} R_{\text{in},0} + C_{\text{gs}} R_{\text{in}} \\ &\quad + C_{\text{gs}} R_{\text{L}'0} + C_{\text{gs}} (R_{\text{in},0} (1 - g_m R_L') + R_L) + C_{\text{gs}} R_L \end{aligned} \quad (6.60)$$

and the 3-dB frequency f_{in} is

$$f_{\text{in}} = \frac{1}{2\pi \delta_1} \quad (6.61)$$

For situations in which C_{gs} is substantial, this approach yields a better estimate of f_{in} than that obtained using the Miller equivalence (mainly because in the latter case we completely neglect C_{gs}).

6.6.3 Exact Analysis

The approximate analysis presented above provides insight regarding the mechanism by which and the extent to which the various capacitances limit the high-frequency gain of the CS (and CE) amplifiers. Nevertheless, given that the circuit of Fig. 6.20 is relatively simple, it is instructive to also perform an exact analysis.⁸ This is illustrated in Fig. 6.23. A node equation at the drain provides

$$sC_{\text{gs}}(V_{\text{gs}} - V_{\text{d}}) = g_m V_{\text{ds}} + \frac{V_{\text{o}}}{R_L'} + sC_{\text{gd}} V_{\text{d}}$$

which can be manipulated in the form

$$V_{\text{d}} = \frac{-V_{\text{o}}}{sC_{\text{gd}} R_L'} \frac{1 + r(C_{\text{gs}} + C_{\text{gd}})R_L'}{1 + sC_{\text{gs}}/r} \quad (6.62)$$

A loop equation at the output yields

$$V_{\text{ds}} = I_{\text{d}} R_{\text{L}'0} - V_{\text{o}}$$

in which we can substitute for I_{d} from a node equation at G ,

$$I_{\text{d}} = sC_{\text{gs}} V_{\text{gs}} - sC_{\text{gd}}(V_{\text{ds}} - V_{\text{o}})$$

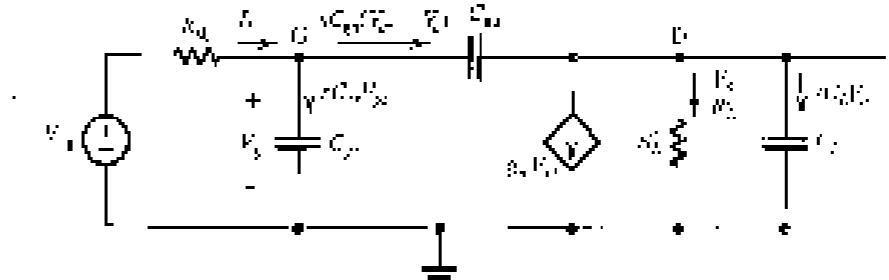


FIGURE 6.23 An exact model of the CS stage (assuming a value of r).

⁸Exact only in the sense that we are not making approximations in the circuit analysis process. This note is remindful, however, that the high-frequency model used represents an approximation of the device performance.

to obtain

$$V_{\text{in}} = R_s [1 + s(C_{\text{gs}} + C_{\text{gd}})(R_{\text{ds}}) + sC_{\text{gd}}R_{\text{ds}}V_{\text{o}}]$$

We can now substitute this equation for V_{in} from Eq. (6.59) to obtain an expression for V_{in} and V_{out} that can be rearranged to yield the small-s gain as

$$\frac{V_{\text{o}}}{V_{\text{in}}} = \frac{-i(g_{\text{m}}R_s)[1 + s(C_{\text{gs}}/g_{\text{m}})]}{1 - s[C_{\text{gs}} + C_{\text{gd}}(1 + g_{\text{m}}R_s)(R_{\text{ds}} + (C_{\text{L}} + C_{\text{gd}})R_s^2)] + s^2(C_{\text{L}} + C_{\text{gd}})(C_{\text{gd}} + C_{\text{L}}C_{\text{gs}}/R_{\text{ds}})R_s^2} \quad (6.60)$$

The transfer function in Eq. (6.60) indicates that the amplifier has a second-order denominator and hence two poles. Now, since the parameter is of the first order, it follows that one of the two transmission zeros is at infinite frequency. This is readily verifiable by noting that as s approaches ∞ , $V_{\text{in}}/V_{\text{out}}$ approaches zero. The second zero is at

$$s = s_2 = \frac{g_{\text{m}}}{C_{\text{gd}}} \quad (6.61)$$

The s_2 is on the positive real axis of the s -plane and has a frequency ω_2 ,

$$\omega_2 = g_{\text{m}}/C_{\text{gd}} \quad (6.62)$$

Since g_{m} is usually large and C_{gd} is usually small, ω_2 is normally a very high frequency and thus has negligible effect on the value of f_T .

It is useful at this point to show a simple method for finding the value of s at which $V_{\text{o}} = 0$, that is, s_p . Figure 6.24 shows the circuit at $s = s_p$. By definition, $V_{\text{o}} = 0$ and a node equation at D yields

$$s_p C_{\text{gd}} V_{\text{in}} = g_{\text{m}} V_{\text{o}}$$

Now, since V_{o} is not zero (why not?), we can divide both sides by V_{o} to obtain

$$s_p = \frac{g_{\text{m}}}{C_{\text{gd}}} \quad (6.63)$$

Before considering the poles, we should note that in Eq. (6.60), as s goes toward zero, $V_{\text{o}}/V_{\text{in}}$ approaches the term $(C_{\text{gd}}R_s^2)$, as should be the case. Let's now take a closer look at the denominator polynomial. First, we observe that the coefficient of the s^2 term is equal to the effective time-constant τ_p obtained using the open-circuit transconductance method as given by Eq. (6.27). Again, this should have been expected since it is the basis for the open-circuit

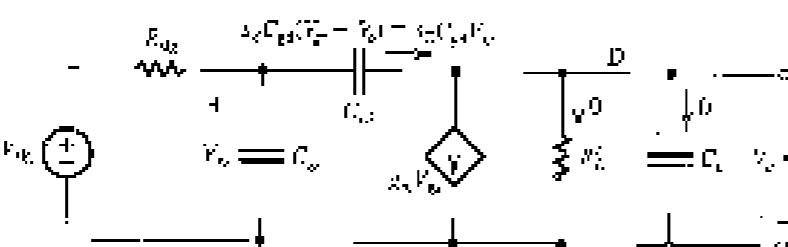


FIGURE 6.24 Miller circuit with $s = s_p$. The output voltage $V_{\text{o}} = 0$ and the drain current is zero according to Eq. (6.63).

time-constants method (Section 6.4.7). Next, denoting the frequencies of the two poles by ω_1 and ω_2 , we can express the denominator polynomial $D(s)$ as

$$\begin{aligned} D(s) &= \left(\frac{s}{\omega_1} + \frac{s}{\omega_2}\right) \left[1 + \frac{s^2}{\omega_1^2}\right] \\ &= 1 + s \left[\frac{1}{\omega_1} + \frac{1}{\omega_2}\right] + \frac{s^2}{\omega_1^2 \omega_2^2} \end{aligned} \quad (6.64)$$

Now, if $\omega_2 \gg \omega_1$, that is, the pole at ω_2 is dominant—we can approximate $D(s)$ as

$$D(s) \approx 1 + \frac{s}{\omega_1} + \frac{s^2}{\omega_1^2 \omega_2^2} \quad (6.65)$$

Equating the coefficients of the s term in denominator polynomial of Eq. (6.64) to that of the term in Eq. (6.65) gives

$$\omega_1 = \frac{1}{[C_{\text{gd}} + C_{\text{gs}}(1 + g_{\text{m}}R_s^2)(R_{\text{ds}} + (C_{\text{L}} + C_{\text{gd}})R_s^2)]} \quad (6.66)$$

where the approximation is that involved in Eq. (6.65). Notice, the expression in Eq. (6.66) is identical to the result obtained using open-circuit time-constants and a little different from the result obtained using the Miller equivalence, the difference being the term $(C_{\text{L}} + C_{\text{gd}})R_s^2$ related to the capacitance of the output, which was ignored in the original (simple) Miller derivation. Setting the coefficients of s^2 in Eqs. (6.60) and (6.65) and using Eq. (6.66) gives the frequency of the second pole,

$$\omega_2 = \frac{iC_{\text{gd}}C_{\text{gs}}(1 + g_{\text{m}}R_s^2)(R_{\text{ds}} + (C_{\text{L}} + C_{\text{gd}})R_s^2)}{[1 + C_{\text{gd}}(C_{\text{gs}} + C_{\text{L}})R_s^2]R_s^2} \quad (6.67)$$

Example 6.10

A CMOS source-follower amplifier of the type shown in Fig. 6.1(a) has $W/L = 1/2$ and $0.16 \mu\text{m}$ for all transistors, $k_nC_{\text{gd}} = 387 \mu\text{A/V}^2$, $k_pC_{\text{gs}} = 96 \mu\text{A/V}^2$, $I_{\text{DD}} = 100 \mu\text{A}$, $V_{\text{DD}} = 5 \text{ V}$, and $V_{\text{A}} = 6 \text{ V}$ for Q_1 , $C_{\text{L}} = 20 \text{ fF}$, $C_{\text{gd}} = 5 \text{ fF}$, $C_{\text{gs}} = 25 \text{ fF}$, and $R_{\text{ds}} = 0 \text{ k}\Omega$. Assume that C_{gd} includes all the capacitances introduced by Q_2 in the output node. Find f_T using both the Miller equivalence and the open-circuit time-constants. Also determine the exact values of $f_{\text{p}}, f_{\text{pd}}$, and f_{g} and hence provide another estimate for f_T .

Solution

$$f_T = f_{\text{SP}} = 100 \mu\text{A} = \frac{1}{2}k_nC_{\text{gs}}\left(\frac{W}{L}\right)V_{\text{DD}}^2$$

Thus,

$$100 = \frac{1}{2} \times 387 \times \frac{7.2}{0.16} \text{ V}_{\text{DD}}^2$$

which results in

$$V_{\text{DD}} = 0.17 \text{ V}$$

Thus,

$$\mu_0 = \frac{I_D}{C_{\text{in}}/2} = \frac{10^7 \text{ mA}}{10.15/2 \text{ pF}} = 1.25 \text{ nA/pF}$$

$$r_{\text{in}} = \frac{V_{\text{in}}}{I_D} = \frac{5 \times 0.36}{0.1} = 18 \text{ k}\Omega$$

$$r_{\text{out}} = \frac{|V_{\text{out}}|}{I_D} = \frac{6 \times 0.36}{0.1} = 21.6 \text{ k}\Omega$$

$$R'_L = r_{\text{in}} \parallel r_{\text{out}} = 18 \parallel 21.6 = 9.82 \text{ k}\Omega$$

$$A_{\text{v1}} = -g_m R'_L = -1.25 \times 9.82 = -12.3 \text{ V/V}$$

Using the Miller equivalence,

$$C_{\text{v1}} = C_{\text{in}} + g_m R'_L$$

$$= 20 + 5(1 + 12.3)$$

$$= 86.5 \text{ pF}$$

$$f_T = \frac{1}{2\pi C_{\text{v1}} R_{\text{in}}}$$

$$< \frac{1}{2\pi \times 86.5 \times 10^{-12} \times 0.1 \times 10^3} = 152 \text{ MHz}$$

Using the open-circuit Miller equivalent circuit:

$$R_{\text{in}} = R_{\text{in1}} = 10 \text{ k}\Omega$$

$$R_{\text{out}} = R_{\text{out1}}(1 + g_m R'_L) + R'_L$$

$$= 12.3 + 12.3 + 9.82 = 142.6 \text{ k}\Omega$$

$$R_{\text{in1}}' = R_{\text{in}}' = 9.82 \text{ k}\Omega$$

Also,

$$\tau_{\text{p1}} = C_{\text{in}} R_{\text{in}} = 20 \times 10^{-12} \times 10 \times 10^3 = 200 \text{ ps}$$

$$\tau_{\text{p2}} = C_{\text{in}} R_{\text{out}} = 20 \times 10^{-12} \times 142.6 \times 10^3 = 711 \text{ ps}$$

$$\tau_{\text{p3}} = C_{\text{in}} R_{\text{in1}}' = 20 \times 10^{-12} \times 9.82 \times 10^3 = 246 \text{ ps}$$

which can be summed to obtain τ_p as

$$\tau_p = \tau_{\text{p1}} + \tau_{\text{p2}} + \tau_{\text{p3}} = 1160 \text{ ps}$$

From which we find the 3-dB frequency f_p ,

$$f_p = \frac{1}{2\pi\tau_p} = \frac{1}{2\pi \times 1160 \times 10^{-12}} \approx 157 \text{ MHz}$$

We note that this is about 25% lower than the estimate obtained using the Miller equivalence. The discrepancy is mostly a result of neglecting C_{v1} in the Miller approach. Note that C_{v1} here has a substantial magnitude and that its contribution to τ_p is significant (246 ps of the total 1160 ps, or 21%).

To determine the exact locations of the zero and the poles, we use the transfer function in Eq. 6.62b. The frequency of the zero is given by Eq. 6.62c:

$$f_z = \frac{1}{2\pi C_{\text{in}}} = \frac{1}{2\pi \cdot 5 \times 10^{-12}} = 31.6 \text{ GHz}$$

The frequencies ω_{p1} and ω_{p2} are found as the roots of the equation obtained by equating the denominator polynomial of Eq. 6.62b to zero:

$$1 + .16 \times 10^{-9}s + 0.0712 \times 10^{-12}s^2 = 0$$

The result is

$$\omega_p = -45.3 \text{ MHz}$$

and

$$\omega_p = 2/5 \text{ GHz}$$

Since $\omega_p / \omega_p \approx f_p$, a good estimate for f_p is

$$f_p \approx f_p = 145.3 \text{ MHz}^2$$

Finally, we note that the estimate of f_p obtained using Eq. 6.66, is about 5% lower than the exact value. Similarly, the estimate of f_p obtained using open-circuit transconductance is 5% lower than the estimate found using the exact value of f_p .

EXERCISES

6.37 For the CS amplifier in Example 6.7, using the values of the components in Table 6.1, compute the 3-dB corner frequency, f_p , at low frequencies, assuming DC voltage source, V_{in} , to be a voltage-controlled voltage source.

Ans: $f_p = 1.79 \text{ GHz}$; this is lower than f_p when $f_T = 179 \text{ GHz}$.

6.38 As a way to understand how to minimize the design of the CS amplifier in Example 6.7, compute the output current according to Eq. 6.62b. From the results, determine the effect of the bias voltage, V_{in} .

Ans: I_{out} varies from 23.3 mA to 1.24 mA.

6.39 An amplifier with a load R_{out} is designed to have a 3-dB corner frequency, f_p , of 100 MHz. To maintain the simplicity of the calculations, decide the collector bias voltage, V_{in} , such that the bias current, I_C , is $0.5 \times 10^{-3} \text{ A}$. Find the new values of r_s , r_o , R_{in} , and R_{out} if the required corner frequency is to be 100 MHz.

Ans: $r_s = 2.10 \text{ k}\Omega$, $r_o = 1.15 \text{ M}\Omega$, $R_{\text{in}} = 55 \text{ M}\Omega$, and $R_{\text{out}} = 1.15 \text{ M}\Omega$.

6.6.4 Adapting the Formulas for the Case of the CE Amplifier

Adapting the formulas presented above to the case of the CE amplifier is straightforward. First, note from Fig. 6.25 how V_{in} and R_{in} are modified to take into account the effect of r_s and r_o .

$$V'_{\text{in}} = V_{\text{in}} \frac{r_s}{r_s + r_o + r_s} \quad (6.68)$$

$$R'_{\text{in}} = r_s (R_{\text{in}} + r_o) \quad (6.69)$$

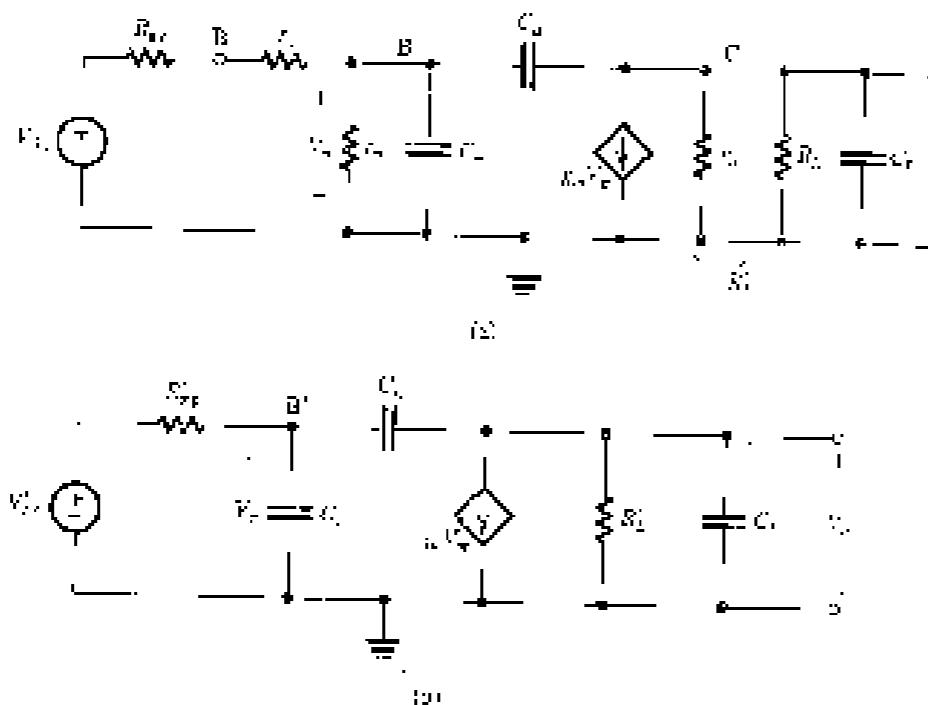


FIGURE 6.25 (b) H₂O-deionized solution sample of the common emulsion polymer, the Kureha emulsion polymer. The Thévenin theorem is employed to analyze the series circuit of the two resistors.

Thus the gain is now given by

$$A_{ij} = -\frac{r_j}{\delta_{ij} - r_j} \langle \vec{q}_j, \vec{F}_i \rangle \quad (6.7)$$

Using Miller's theory, we obtain

$$C_1 = C_0 + C_{\text{eff}}(1 + \mu_0 R^2) \quad (6.2)$$

Correspondence to: The Wellcome Trust Sanger Institute, Cambridge CB10 4WA, UK.

$$f_{\theta} \in \frac{1}{2\pi C}\frac{\partial}{\partial \theta}$$

Although largely unmet, the question of space stations has been raised.

$$\begin{aligned} i_{\alpha} &= C_{\alpha} R_{\alpha} + Q_{\beta} R_{\beta} + C_{\gamma} C_{\gamma}, \\ &= C_{\alpha} R'_{\alpha} + C_{\beta} (1 + e^{-R_{\beta}}) R'_{\beta} + R'_{\gamma} = C_{\alpha} R'_{\alpha} \end{aligned} \quad (6.73)$$

item which can be imported.

$$f_0 = \frac{1}{2\pi^2} \quad (6.3)$$

The exact analysis yields the following approximate results:

$$I_2 = \frac{1}{2} \pi r^2 \quad (3.13)$$

and, occurring near a dominant pole axis.

$$f_{p_1} = \frac{1}{2\pi} \frac{1}{(C_1 + C_2)(1 - p_1)S'_1(R'_{21} + (C_1 + C_2)R)} \quad (6.76)$$

$$Im = \frac{1}{2\pi} \frac{(C_n + C_{n+1}) - g_{nn} R^2 (|K| K_{nn} + |K_n| + C_n + C_{n+1}) R^2}{(C_n C_{n+1} + C_n + C_{n+1}) R^2 - R^4} \quad (6.77)$$

For $f_{\theta_1}, f_{\theta_2} \in \mathcal{F}$

$$f_y = f_x$$

EXEB

Fig. 20. From left to right: H-polar, vertical, horizontal, C-p polarizations showing the longitudinal secondary implementation with a 20 dB loss. The circled frequency is at the half-aligner plane. The parameters are the same as in Fig. 19. The input power is 10 mW and the output power is 10 mW. The circled frequency is at the half-aligner plane. The parameters are the same as in Fig. 19. The input power is 10 mW and the output power is 10 mW.

6.6.5 The Situation When R_{in} Is Low

- There are applications in which the CS amplifier is fed with a low-impedance signal source. Obviously, in such a case, the high-frequency gain will no longer be limited by the interaction of the source resistance and the input capacitance. Rather, the high-frequency limitation increases at the same rate as before, as we shall now show.

Fig. 6.26(a) shows the high-frequency equivalent circuit of the common-source amplifier in the inverting case where R_{in} is zero. The no-load transfer function $V_o/V_{\text{in}} = V_o/V_p$ can be found by setting $R_{\text{out}} = 0$ in Eq. (6.91). The result is

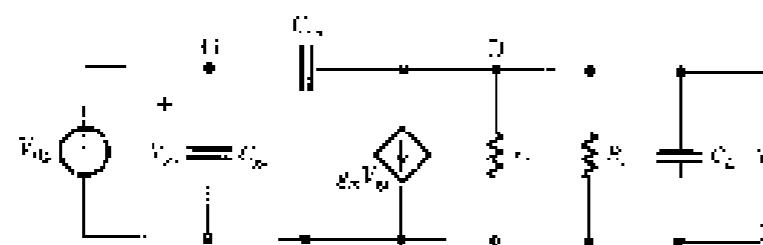
$$\frac{E_{\alpha}}{E_{\beta}} = \left(\frac{g_{\alpha} \partial^2_{\beta} [1 + \cdot(C_{\beta}/g_{\alpha})]}{1 - \sqrt{C_{\beta}} + C_{\beta} + \sqrt{C_{\beta}}} \right) \quad (6.73)$$

Thus, while the duration and the frequency of the note do not change, the high-frequency response is now determined by a pole formed by $C_f + C_{af}$, together with R_f . Thus the feedback frequency is now given by

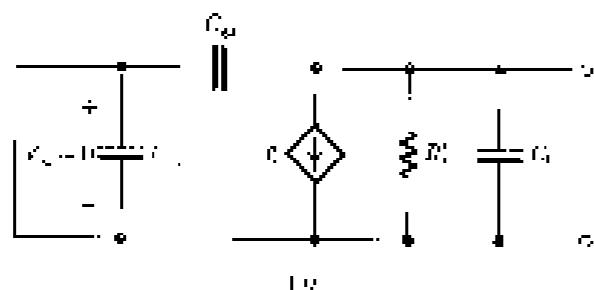
$$t_{\theta} = \frac{1}{2\pi f(1) - C_{\theta}} |B|^2 \quad (6.24)$$

To see how this pole is formed, refer to Fig. 6.26(b), which shows the equivalent circuit with the input signal source reduced to zero. Observe that the circuit reduces to a capacitor ($C_1 + C_2$) in parallel with a resistor R_1 .

As we have seen above, the rank- α -function zero is usually at a very high frequency and thus plays no play a significant role in shaping the high-Laguerre response. The gain of this system will therefore fall off at a rate of 6 dB/ octave (22 dB/ decade) and reach a

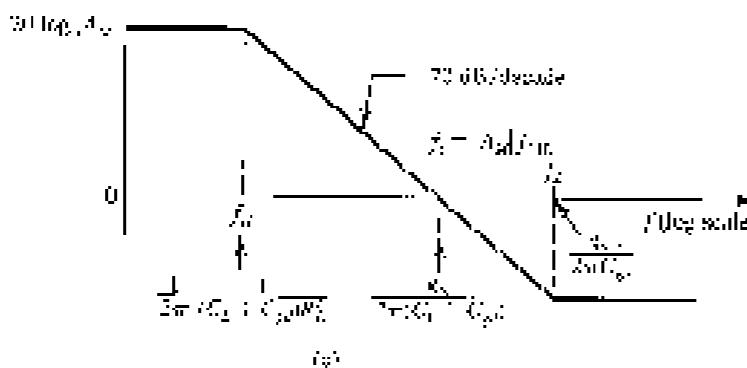


(a)



(b)

Gain (dB)



(c)

FIGURE 6.26 (a) High-frequency equivalent circuit of a CS amplifier fed with a signal source having a very low output resistance. (b) The circuit in (a), with r_{ds} replaced by zero. (c) Decade plot for the gain of the circuit in (b).

unity (0 dB) at a frequency f_1 , which is equal to the gate-bandwidth product,

$$f_1 = A_{d1} f_{in}$$

$$\approx R_o' \frac{1}{2\pi(C_o + C_{inj})R_o'}$$

Thus,

$$f_1 = \frac{2\pi}{2\pi(C_o + C_{inj})R_o'} \quad (6.80x)$$

Figure 6.26(c) shows a sketch of the high-frequency gain of the CS amplifier.

Consider the CS amplifier specified in Example 6.9 when fed with a signal source having a very low output resistance (i.e., $R_{inj} = 0$). Find A_{d1} , f_{inj} , f_1 , and f_2 . If the amplifying transistor is to be operated at twice the original operating voltage while V_{inj} and f_{inj} remain unchanged, what value of I_{dsat} is needed? What are the new values of A_{d1} , f_{inj} , f_1 , and f_2 ?

Solution

In Example 6.9 we found that

$$A_{d1} = -12.3 \text{ V/V}$$

The 3-dB frequency can be found using Eq. (6.79):

$$f_1 = \frac{1}{2\pi(C_o + C_{inj})R_o'}$$

$$= \frac{1}{2\pi(2.5 \times 10^{-12} + 9.82 \times 10^{-12})}$$

$$= 540 \text{ MHz}$$

and the unity-gain frequency, which is equal to the gain-bandwidth product, can be determined as

$$f_2 = A_{d1} f_{inj} = 12.3 \times 540 = 6.6 \text{ GHz}$$

The frequency of the zero is

$$f_0 = \frac{1}{2\pi C_{inj}}$$

$$= \frac{1}{2\pi \cdot 2 \times 10^{-12}} = 40 \text{ GHz}$$

Now, to increase V_{inj} from 0.16 V to 0.32 V, I_{ds} must be quadrupled by changing I_{dsat} to

$$I_{dsat} = 40 \mu\text{A}$$

The new values of g_m , r_{ds} , R_o' , and R_o can be found as follows:

$$g_m = \frac{I_{ds}}{V_{inj}/2} = \frac{40}{0.32/2} = 2.5 \text{ mA/V}$$

$$r_{ds} = \frac{5 \times 0.32}{0.16 \mu\text{A}} = 4.5 \text{ k}\Omega$$

$$R_o' = \frac{5 \times 0.32}{0.16 \mu\text{A}} = 54 \text{ k}\Omega$$

$$R_o = (4.5 + 54) = 58.5 \text{ k}\Omega$$

Thus, the new value of A_{d1} becomes

$$A_{d1} = -g_m R_o' = -2.5 \times 54 = -13.5 \text{ V/V}$$

That is, f_0 becomes

$$\begin{aligned} f_0 &= \frac{1}{2\pi(C_s + C_{os})R_2} \\ &= \frac{1}{2\pi(25 - 5) \times 10^{-12} \times 2.45 \times 10^3} \\ &= 2.16 \text{ GHz} \end{aligned}$$

and the unity-gain frequency (i.e., the gain-bandwidth product) becomes

$$f_t = 6.15 \times 2.16 = 13.3 \text{ GHz}$$

We note that decreasing R_{D2} results in reducing the dc gain by a factor of 2 and increasing the bandwidth by a factor of 1. Thus, the gain-bandwidth product is doubled—a good bargain!

EXERCISES

- (E.24) For the CS amplifier consisting of two NMOS transistors shown in the figure, we have the following values:
 - $V_{DD} = 5 \text{ V}$, $R_D = 10 \text{ k}\Omega$, $R_{S1} = R_{S2} = 10 \text{ k}\Omega$, $R_{G1} = R_{G2} = 10 \text{ k}\Omega$, $C_{os} = 10 \text{ pF}$, $C_s = 10 \text{ pF}$, $R_{L1} = R_{L2} = 10 \text{ k}\Omega$, $I_{DSS1} = I_{DSS2} = 1 \text{ mA}$, $k_n = 1 \text{ mA/V}^2$, $\lambda = 0.05$, $V_{GS1} = V_{GS2} = 1 \text{ V}$.
 (a) Show that the CS amplifier has a load with $R_L = 20 \text{ k}\Omega$ at a particular frequency, where the frequency is related to f_0 by

6.7 THE COMMON-GATE AND COMMON-BASE AMPLIFIERS WITH ACTIVE LOADS

6.7.1 The Common-Gate Amplifier

Figure 6.27(a) shows the basic IC MOS common-gate amplifier. The transistor has its gate grounded and its drain connected to an active load, shown as an ideal constant-current source I_1 . The input signal source v_{in} with a generator resistance R_g is connected to the source terminal. Since the MOSFET source is not connected to the substrate, we show the substrate terminal, B , explicitly and indicate that it is connected to the lowest voltage in the circuit, in this case ground. Finally, observe that except for showing the current-source I_1 , which determines the dc bias current I_1 of the transistor, we have not shown any other bias detail. How the dc voltage V_{DS} will be established and how V_{DS} is determined are left of center to the left. As mentioned before, however, bias stability is usually assured through the application of negative feedback to the larger circuit of which the CG amplifier is a part. For our purposes here, we shall assume that the MOSFET is operating in the saturation region and concentrate exclusively on its small-signal operation.

The Body Effect Since the substrate (i.e., body) is not connected to the source, the body-effect plays a role in the operation of the common-gate amplifier. It turns out, however, that

²⁷ Rather than using R_{D1} to denote the resistor used by signal source, we use R_g since the resistance is associated with the source terminal of the NMOSFET.

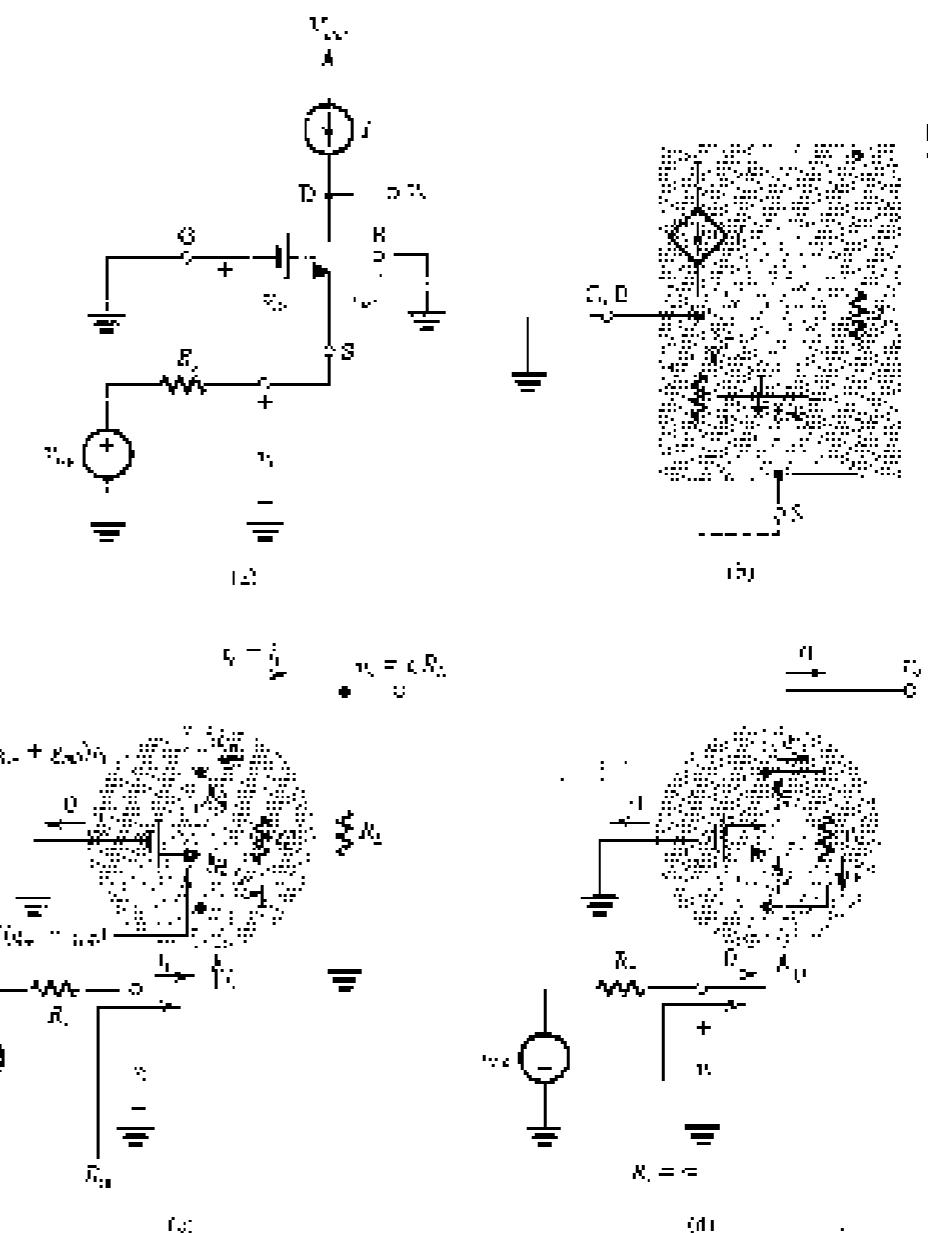


FIGURE 6.27. (a) Active-loaded common-gate amplifier. (b) MOSFET equivalent circuit for the CG case (when the body and gate terminals are connected to ground). (c) Small-signal analysis model, obtained by replacing the circuit diagram with the T model of (b) used implicitly. (d) Open-loop common-gate circuit.

taking the body effect into account in the analysis of the CG circuit is a very difficult task. To see how this can be done, recall that the body terminal acts, in effect, as a second gate for the MOSFET. Thus, just as a signal voltage v_{BS} between the gate and the source gives rise to a drain current signal v_{DS} , so a signal voltage v_{DB} between the body and the source gives rise to a drain current signal v_{DS} . Take the drain current-current bias ratios (β_n , α_n , β_{n2} , α_{n2}), where the body-to-substrate current v_{BS} is a small fraction χ of v_{GS} : $\beta_{n2} = \beta_n \chi$, and $\chi = 0.1$ to 0.2.

Now, since in the CG circuit of Fig. 6.27(a) both the gate and the body terminals are connected to ground, $v_{GS} = v_G$, and the signal current in the drain becomes $(g_m + g_{DS})v_D$. It follows that the body effect in the common-gate circuit can be fully accounted for by simply replacing r_s of the MOSFET by $(g_m + g_{DS})r_s$. As an example, Fig. 6.27(c) shows the MOSFET T-model modified in this fashion.

Small-Signal Analysis The small-signal analysis of the CG amplifier can be performed either on an equivalent circuit (obtained by replacing the MOSFET with its T model in Fig. 6.27(b)) or directly on the circuit diagram with the model used implicitly. We shall opt for the latter approach in order to gain greater insight into circuit operation. Figure 6.27(c) shows the CG circuit prepared for small-signal analysis. Note that we have "extracted" r_s of the MOSFET and shown it separately from the device. As well, we have indicated the resistance $1/(g_m + g_{DS})$, which appears in effect between gate and source looking into the source. Finally, note that a resistance R_L is shown at the output; it is assumed to include the output resistance of the current-source load as well as any load resistance if one is connected.

We now proceed to analyze the circuit of Fig. 6.27(c) to determine the various parameters that characterize the CG amplifier. At this point we strongly urge the reader to consult Table 4.2 for a review of the definitions of amplifier characteristic parameters. This is especially useful here because the CG amplifier is not a unilateral circuit; the resistance r_s connects the output node to the input node, thus destroying unilateralism. As a result, we should expect the amplifier input resistance R_{in} to depend on R_L and the output resistance R_{out} to depend on R_L .

Input Resistance To determine the input resistance R_{in} , we topic: find a way to express i_s in terms of v_{GS} . Inspection of the circuit in Fig. 6.27(c) reveals a key observation: The input current i_s splits at the source node into two components: the source current $i = (g_m + g_{DS})v_D$ and the current through r_s , i_{r_s} . These two components combine at the drain to constitute the current i_s supplied to R_L ; thus $i_s = i$, and $v_D = i_s R_L = i_s K_1$. Now we can write at the source node:

$$i_s = (g_m + g_{DS})v_D + i_{r_s} \quad (6.81)$$

and express i_{r_s} as

$$i_{r_s} = \frac{v_{GS} - v_D}{r_s} = \frac{v_{GS} - i_s K_1}{r_s} \quad (6.82)$$

Equations (6.81) and (6.82) can be combined to yield

$$i_s = \left(g_m + g_{DS} + \frac{1}{r_s} \right) v_{GS} \left(1 + \frac{R_L}{r_s} \right)$$

From which the input resistance R_{in} can be found as

$$R_{in} = \frac{v_{GS}}{i_s} = \frac{r_s + R_L}{1 + (g_m + g_{DS})r_s} \quad (6.83)$$

Observe that for $r_s = \infty$, R_{in} reduces to $1/(g_m + g_{DS})$, which is indeed the input resistance that we found for the discrete CG amplifier analyzed in Section 4.7.5 with r_s neglected (here we also neglected g_{DS}). When r_s is taken into account, this value of input resistance is obtained approximately only for $R_L = 0$. For the usual case of $R_L \gg r_s$, $R_{in} \approx 1/(g_m + g_{DS})$. Interestingly, for large values of R_L approaching infinity, $R_{in} = \infty$. This somewhat surprising result will be illustrated next.

Operation with $R_L = \infty$ Figure 6.27(d) shows the CG amplifier with R_L removed; that is, $R_L = \infty$ and the amplifier is operating with the output open-circuited. We immediately

note that since $v_D = 0$, i_s must also be zero, the current in the source terminal, $i = (g_m + g_{DS})v_D$, simply flows via the drain through r_s and back to the source node. It follows that the drain resistance with no load, R_D , is infinite:

$$R_D = \infty$$

We can also use the circuit in Fig. 6.27(d) to determine the open-circuit voltage gain, A_{oc} , between the input (source) and output (drain) terminals as follows:

$$\begin{aligned} v_D &= i_s r_s \\ &= (g_m + g_{DS})v_{GS} r_s \end{aligned} \quad (6.84)$$

Thus,

$$A_{oc} = 1 + (g_m + g_{DS})r_s \quad (6.85)$$

This is a very important quantity that appears in almost all formulas that characterize the CG MOSFET. We observe that A_{oc} relates from the intrinsic gain of the MOSFET in the linear amplifier. We observe that A_{oc} relates from the intrinsic gain of the MOSFET in the linear amplifier. We observe that A_{oc} is added to A_0 . Typically, respectively, first, there is an additional term of unity, and second, A_{oc} is added to A_0 . Typically, A_{oc} is 10% to 20% larger than A_0 .

We should also note that the gain of the CG circuit is positive. That is, unlike the CS amplifier, the CG amplifier is non-inverting.

Using Eqs. (6.83) and (6.85), we can express the input resistance of the CG amplifier in the simplest and attractive form:

$$R_{in} = \frac{r_s + R_L}{A_{oc}} \quad (6.86)$$

That is, the CG circuit divides the total resistance $(r_s + R_L)$ by the open-circuit voltage gain, which is approximately equal to the intrinsic gain of the MOSFET. Furthermore, since $A_{oc} \equiv (g_m + g_{DS})r_s \equiv A_0$, the expression for R_{in} can be simplified to

$$R_{in} = \frac{1}{A_{oc}} = \frac{R_L}{g_m + g_{DS} + A_0} \quad (6.87)$$

This expression simply says that taking r_s into account adds a resistor (R_L/A_0) to the input resistance. This additional component becomes significant only when R_L is large.

Another interesting result follows directly from the fact that $i_s = 0$ in the circuit of Fig. 6.27(d). The voltage drop across R_L will be zero. Thus $v = v_{GS}$ and the open-circuit overall voltage gain, v_D/v_{GS} , will be equal to A_{oc} .

$$G_{oc} = A_{oc} = 1 + (g_m + g_{DS})r_s \quad (6.88)$$

Voltage Gain The voltage gains A_{oc} and G_{oc} of the loaded CG amplifier of Fig. 6.27(d) can be obtained in a number of ways. The most direct approach is to make use, once more, of the fact that $i_s = 0$ and replace v_D as

$$v_D = i_s R_L = 0 \quad (6.89)$$

The voltage v_D can be expressed in terms of i_s as

$$v_D = i_s R_L \quad (6.90)$$

Dividing Eq. (6.94) by R_2 , (6.90) yields, for the voltage gain A_{v1} ,

$$A_{v1} = \frac{R_2}{r_s + R_{in}} = \frac{R_2}{R_{in}} \quad (6.91)$$

Simplifying for R_{in} from Eq. (6.86) provides

$$A_{v1} = -g_m R_2 + r_o \quad (6.92)$$

In a similar way we can derive an expression for the overall voltage gain, $G_v = v_o/v_{in}$,

$$\begin{aligned} v_o &= i_2 R_2 = i_2 R_1 \\ v_{in} &= (i_2 R_2 + R_{out}) \end{aligned}$$

Thus,

$$G_v = \frac{R_2}{R_{in} + R_{out}} \quad (6.93)$$

in which we can substitute for R_{in} from Eq. (6.86) to obtain

$$G_v = A_{v1} \frac{R_2}{R_2 + r_o + A_{v1} R_2} \quad (6.94)$$

Recalling that $G_{ow} = A_{v1}$, we can express G_v as

$$G_v = G_{ow} \frac{R_2}{R_2 + r_o + A_{v1} R_2} \quad (6.95)$$

Output Resistance. To complete our characterization of the CG amplifier, we find the output resistance. From the study of amplifier characterization in Section 4.7.2 (Table 4.1), we recall that there are two different output resistances: R_{out} , which is the output resistance when v_{in} is set to zero, and R_{out1} , which is the output resistance when v_{in1} is set to zero. Both are illustrated in Fig. 6.28. Obviously, R_{out} can be obtained from the expression for R_{out1} by setting $R_2 = 0$. It is important to be clear on the application of R_{out} and G_{ow} . Since R_{out} is the output resistance when the amplifier is fed with an ideal source v_{in} , it follows that it is the applicable output resistance for determining A_{v1} from G_{ow} :

$$A_{v1} = A_{v1} \frac{R_2}{R_2 + R_{out}} \quad (6.96)$$

On the other hand, R_{out1} is the output resistance when the amplifier is fed with v_{in1} , and its resistance R_{out} thus is the applicable output resistance for determining G_v from G_{ow} :

$$G_v = G_{ow} \frac{R_2}{R_2 + R_{out1}} \quad (6.97)$$

Returning to the circuit in Fig. 6.28(a), we see by inspection that

$$R_{in} = r_s \quad (6.98)$$

A quick verification of this result is achieved by substituting $R_2 = r_o$ in Eq. (6.96) and then observing that the resulting expression for A_{v1} is identical to that in Eq. (6.92), which we derived directly from circuit analysis.

An expression for R_{out1} can be derived using the circuit in Fig. 6.28(b) where a test voltage v_t is applied at the output. Our goal is to find the current i_t drawn from v_t . Toward that

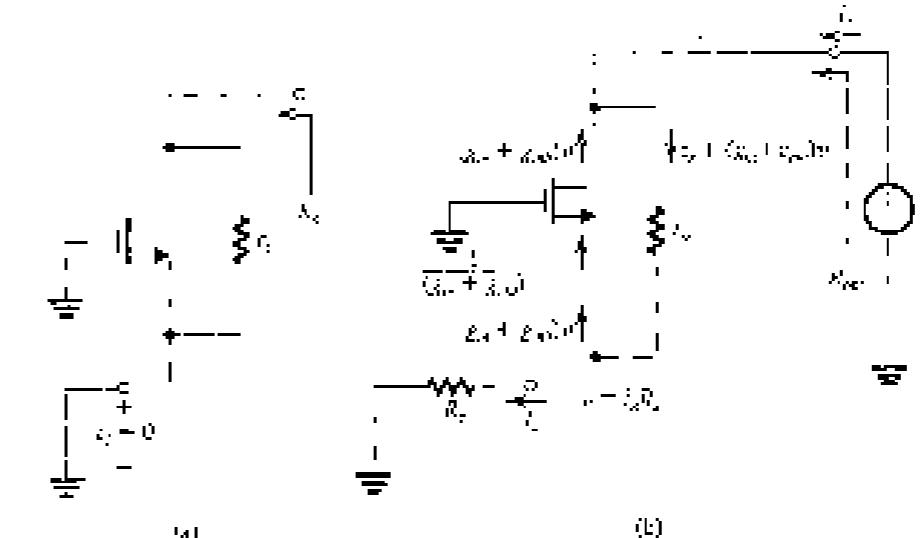


FIGURE 6.28. (a) The output resistance R_{out} is found by setting $v_t = 0$. (b) The output resistance R_{out1} is obtained by setting $v_t = 0$.

and note that the current through R_2 is equal to i_t ; hence we can express the voltage v at the MOSFET source as

$$v = i_t R_2 \quad (6.99)$$

Utilizing the analysis indicated on the circuit diagram in Fig. 6.28(a), we can write for v_s

$$v_s = [1 + (g_m + g_{os})r_s]i_t + v \quad (6.100)$$

Equations (6.99) and (6.100) can be combined to eliminate v and obtain v_s in terms of i_t , and hence $R_{out1} = v_s/i_t$:

$$R_{out1} = r_s + [1 + (g_m + g_{os})r_s]R_2 \quad (6.101)$$

We recognize the term multiplying R_2 as the open-circuit voltage gain A_{v1} , thus R_{out1} can be expressed in an alternative, more compact, form as

$$R_{out1} = r_s + A_{v1} R_2 \quad (6.102)$$

A quick verification of the formula for R_{out1} in Eq. (6.102) can be obtained by substituting it in Eq. (6.97). The result will be seen to be identical to the gain expression in Eq. (6.95), which we derived by direct circuit analysis.

The expressions for R_{out} in Eqs. (6.101) and (6.102) are very useful, especially that we will employ frequently throughout the rest of this book. These formulas give the output resistance not only of the CG amplifier but also of a CS amplifier with a resistive R_2 in the emitter. We will have more to say about this shortly. At this point, however, it is useful to interpret Eqs. (6.101) and (6.102). A key interpretation, immediately available from Eq. (6.102), is that the CG connection increases the output resistance by adding to r_s a component $A_{v1}R_2$. In many cases the latter contribution would dominate, just one can think of the CG MOSFET

as multiplying the resistance R_1 in its source by A_{vA} , which is approximately equal to g_{mF} . Note that this action is the complement of what we saw earlier in regard to R_2 , where the MOSFET acts to divide R_2 by $1 + g_m$. This impedance transformation action of the CG MOSFET is illustrated in Fig. 6.29 and is key to a number of applications of the CG circuit. This is also applied to involvers the use of the CG amplifier as a current buffer. Figure 6.30 shows an equivalent circuit that is valid. We see such an application. The reader is urged to observe that the overall short-circuit current gain G_{ds} is given by

$$G_{ds} = G_{vA} \frac{R_2}{R_{ds}} \approx 1$$

The necessary current gain together with the low input resistance and high output resistance are all characteristics of a good current buffer.

For another unique situation, the formula for R_{ds} can be obtained by expanding Eq. (6.10) in the form

$$R_{ds} = R_s + [1 + (g_{mF} + g_{ds})R_s]r_o \quad (6.109)$$

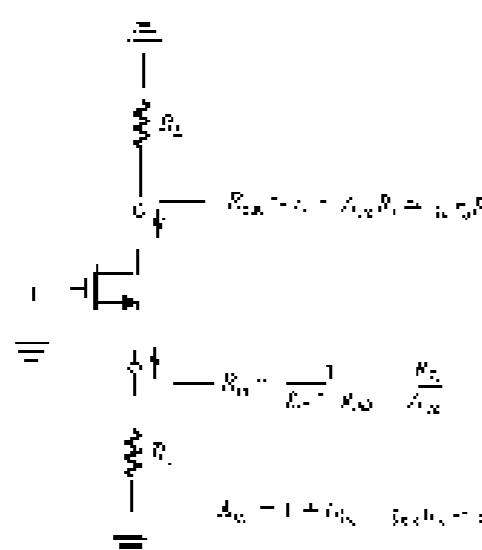


FIGURE 6.29 The impedance transformation property of the CG configuration.

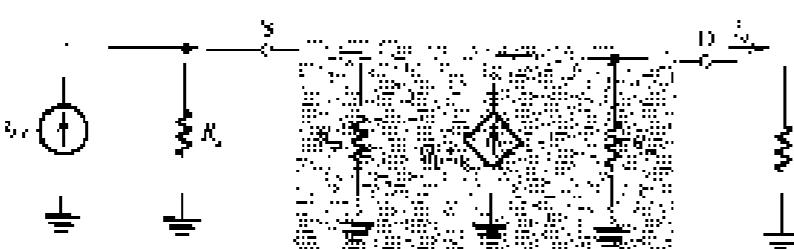


FIGURE 6.30 Equivalent circuit of the CG amplifier illustrating I_D as applied to a current buffer. R_{ds} is given in Eq. 6.20 and $\alpha_{vA} = g_{mF}(R_s/R_{ds})^2$.

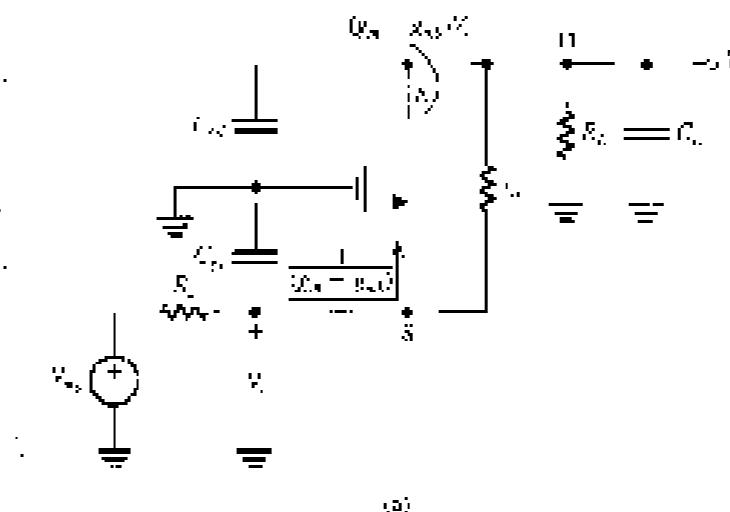
In this expression the second term often dominates, enabling the following approximation:

$$\begin{aligned} R_{ds} &\approx 1 - (g_{mF} + g_{ds})R_s/r_o \\ &\approx (1 + g_{mF})R_s \end{aligned} \quad (6.114)$$

Thus placing a resistance R_2 in the source lead results in multiplying the transistor output resistance by $1 + g_{mF}$. (Recall that we recognize from our discussion of the effect of source loading in Section 4.7.4, We will have more to say about Eq. 6.114 later.)

High-Frequency Response. Figure 6.31(a) shows the CG amplifier with the MOSFET internal capacitances C_{gs} and C_{gd} indicated. For generality, a capacitance C_L is included at the output node to represent the signal capacitance of a succeeding amplifier stage. Capacitance C_L also includes the MOSFET capacitance C_{ds} . Note the C_L appears in effect in parallel with C_{gd} ; therefore, in the following discussion we will lump the two capacitances together.

It is important to note at the outset that each of the three capacitances in the circuit of Fig. 6.31(a) has a grounded node. Therefore none of the capacitances undergoes the Miller-multiplication effect observed in the CS stage. It follows that the CG circuit can be designed to have a much wider bandwidth than that of the CS circuit, especially when the resistance of the signal generator is large.



(a)

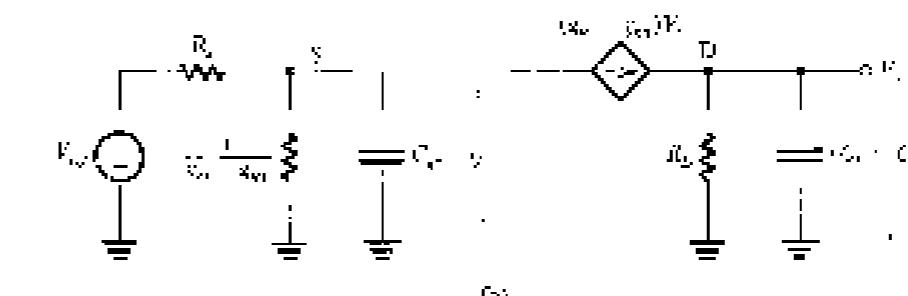


FIGURE 6.31 (a) The common-gate amplifier with the transistors' internal capacitances shown. A load capacitance C_L is connected to node D. (b) Equivalent circuit for the case in (a) of the drain-to-gate bypass circuit.

Analysis of the circuit in Fig. 6.31(c) is greatly simplified if r_o can be neglected. In such a case the input side is isolated from the output side, and the high-frequency equivalent circuit takes the form shown in Fig. 6.31(d). We immediately observe that there are two poles due to the input side with frequency f_{p1} ,

$$f_{p1} = \frac{1}{2\pi C_{in} \left(R_1 \parallel \frac{1}{g_m + g_{os}} \right)} \quad (6.105)$$

and the other at the output side with frequency f_{p2} ,

$$f_{p2} = \frac{1}{2\pi (C_{os} + C_L) R_2} \quad (6.106)$$

The relative locations of the two poles will depend on the specific situation. However, f_{p2} is usually lower than f_{p1} , thus f_{p2} can be dominant. The important point to note is that both f_{p1} and f_{p2} are usually much higher than the frequency ω of the dominant input pole due to the CS stage.

In situations where r_o has to be taken into account (because R_1 and R_2 are large), the method of open-circuit time constants can be employed to obtain an estimate for the 3-dB frequency f_0 . Figure 6.32 shows the circuits for determining the resistances R_{x1} and R_{x2} seen by C_{in} and $(C_{os} + C_L)$, respectively. By inspection we obtain

$$R_{x1} = R_1 \parallel R_2 \quad (6.107)$$

and

$$R_{x2} = R_{os} \parallel R_{os} \quad (6.108)$$

which can be used to obtain f_0 ,

$$f_0 = \frac{1}{2\pi [C_{in} R_{x1} + (C_{os} + C_L) R_{x2}]} \quad (6.109)$$

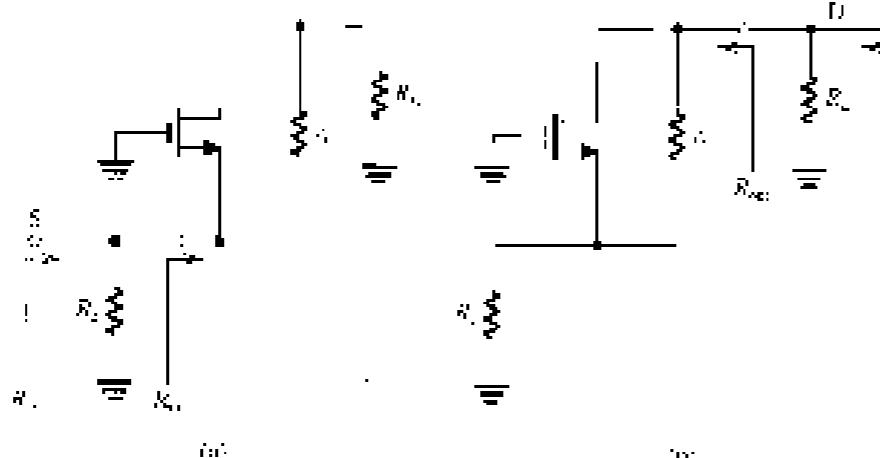


FIGURE 6.32 Circuits for determining R_{x1} and R_{x2} .

Consider a common-gate amplifier specified as follows: $W/L = 7.2 \mu m/0.38 \mu m$, $g_m C_{os} = 187 \mu A/V^2$, $r_o = 18.2 M\Omega$, $I_D = 11.1 \mu A$, $g_{os} = 1.25 \mu A/V$, $\chi = 0.2$, $R_1 = 10 k\Omega$, $R_2 = 20 k\Omega$, $C_{in} = 20 \text{ fF}$, $C_{os} = 2 \text{ pF}$, and $C_L = 0$. Find A_{os} , R_{x1} , R_{x2} , G_{os} , G_L , and f_0 .

Solution

$$g_s + g_{os} = 1.25 \times 1.25 = 1.5 \text{ mA/V}$$

$$A_{os} = 1 + (g_s + g_{os}) r_o = 1 + 1.5 \times 18 = 38 \text{ V/V}$$

$$R_{x1} = \frac{r_o + R_2}{A_{os}} = \frac{18.2 + 20}{38} = 4.2 \text{ k}\Omega$$

$$R_{x2} = r_o + A_{os} R_2 = 18.2 + 38 \times 10 = 298 \text{ k}\Omega$$

$$G_{os} = G_{os} \frac{R_1}{R_{os}} = \frac{1}{2}, \frac{R_1}{R_2 + R_{os}} + 20 \cdot \frac{100}{20 + 298} = 2 \text{ V/V}$$

$$G_{os} = \frac{1.5 \cdot R_1}{R_{os}} = \frac{29 \times 10}{298} = 0.92 \text{ A/A}$$

$$G_L = G_{os} \frac{R_{os}}{R_{os} + R_2} = 0.92 \frac{298}{298 + 10} = 0.7 \text{ A/A}$$

$$R_{os} = R_1 \parallel R_{os} = 10 \parallel 20 = 3 \text{ k}\Omega$$

$$r_o = C_{os} R_{os} = C_{os} R_{os}$$

$$= 20 \times 3 = 60 \text{ k}\Omega$$

$$= 60 / 3.5 = 17.1 \text{ pF}$$

$$f_0 = \frac{1}{2\pi \mu} = \frac{1}{2\pi \times 3.5 \times 10^{-12}} = 366 \text{ MHz}$$

We note that this circuit provides very low current gain, resulting in a resistance level from $R_{x1} = 4 \text{ k}\Omega$ to $R_{x2} = 298 \text{ k}\Omega$ and hence a overall drain current gain of 0.92 A/A. Because of the high output resistance, the output voltage V_{os} is determined primarily by the capacitance at the output node. This additional load capacitance can lower the bandwidth significantly.

EXERCISES

- 6.73 For the CG amplifier given in Fig. 6.31, find the value of r_o when $r_{os} = 50 M\Omega$ and $r_{os} = 100 M\Omega$.
- 6.74 Repeat the problem of Exercise 6.31 for the cascode configuration of Fig. 6.31(b).
- 6.75 For the problem of Exercise 6.31, find the value of r_{os} when $r_{os} = 100 M\Omega$.
- 6.76 For the problem of Exercise 6.31, find the value of r_{os} when $r_{os} = 200 M\Omega$.

6.7.2 The Common-Base Amplifier

Analysis of the common-base amplifier parallels that of the common-gate circuit that we analyzed previously, with one major exception: The BJT has a finite β , and its base conducts signal current, which gives rise to the resistance r_b between base and emitter, looking into the base. Figure 6.33(a) shows the basic circuit for the active-loaded common-base.

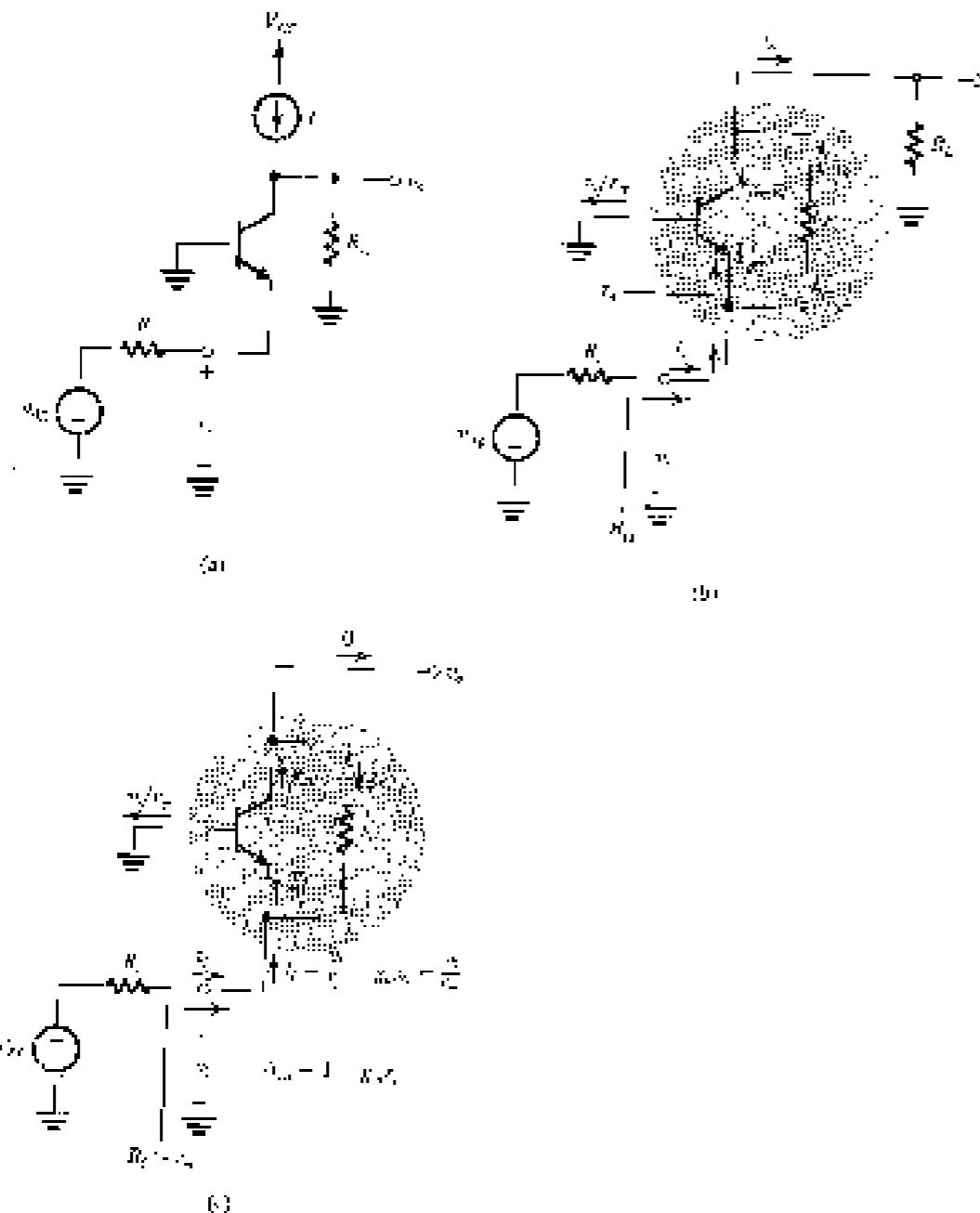


FIGURE 6.33. (a) Active load common-base amplifier. (b) Small-signal analysis, conforming directly to the circuit (a), with the BJT model used in (a) only. (c) Small-signal analysis with compensation included.

amplifier without the bias details. Note that resistance R_L represents the combination of load resistance, if any, and the output resistance of the current source that receives the active load I .

Figure 6.33(b) shows the small-signal analysis performed directly on the circuit with the T model of the BJT used implicitly. The analysis is very similar to that for the MOSFET case except that, as a result of the finite base current, i_B/r_b , the current i_B is related to i by

$$i_B = I - i_v/r_b \quad (6.110)$$

The reader can show that, neglecting r_b , the input resistance at the emitter R_{in} is given by

$$R_{in} = \frac{r_e + R_L}{1 + \frac{r_b}{r_e} + \frac{R_L}{r_e(\beta + 1)\mu}} \quad (6.111)$$

We immediately observe that setting $\beta = \infty$ reduces this expression to that for the MOSFET case (Eq. 6.84) except that here $g_{m0} = 0$. Note that for $\beta = \infty$, $\mu = 1$, and $r_e = \mu C_{BS} = 1/\mu$.

With a slight approximation, the expression in Eq. (6.111) can be written as

$$R_{in} \approx r_e \frac{r_e + R_L}{r_e + R_L / (\beta + 1)} \quad (6.112)$$

Note that setting $r_e = \infty$ yields $R_{in} = r_e$, which is consistent with what we found in Section 5.7.5. Also, for $R_L = 0$, $R_{in} = r_e$. The value of R_{in} increases as R_L is raised, reaching a maximum of $(\beta + 1)r_e = r_e$ for $R_L = \infty$, that is, with the amplifier operating open-circuited (see Fig. 6.33(c)). For $R_L/(\beta + 1) \ll r_e$, Eq. (6.112) can be approximated as

$$R_{in} \approx r_e + \frac{R_L}{A_0} \quad (6.113)$$

where A_0 is the intrinsic gain $\beta_i r_o$. This equation is very similar to Eq. (6.87) in the MOSFET case.

The open-circuit voltage gain and input resistance can be easily found from the circuit in Fig. 6.33(c) as

$$A_{oc} = 1 + g_{m0}r_o = 1 + A_0 \quad (6.114)$$

which is identical to Eq. (6.85) for the MOSFET except for the absence of g_{m0} . The input resistance with no load, R_{in} , is

$$R_{in} \approx r_e \quad (6.115)$$

as we have already found out from Eq. (6.112).

As in the MOSFET case, the output resistance R_{out} is given by

$$R_{out} = r_o \quad (6.116)$$

The output resistance including the source resistance R_s can be found by analysis of the circuit in Fig. 6.34 to be

$$R_{out} = r_o + (1 + g_{m0}r_o)R'_s \quad (6.117a)$$

where $R'_s = R_s/(1 + \mu)$.

Note that the formula in Eq. (6.117a) is very similar to that for the MOSFET case, namely Eq. (6.101). However, there are two differences: First, ρ_{out} is missing, and second, $R'_s = R_s/(1 + \mu)$.

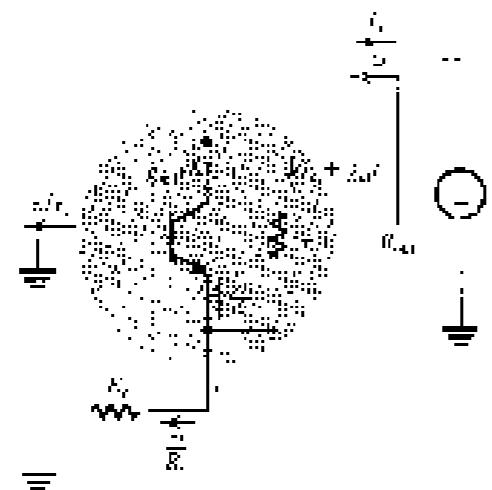


FIGURE 6.34 A circuit of the CB stage to generate A_{vB} . Observe that the current i_B entering the transistor must equal the sum of the two currents i_C and $-i_E$ that leave the transistor through $i_B = i_C - i_E/R_E$.

resistor R_E . The reason β appears in the BJT formula is the finite β of the BJT. The expression in Eq. (6.17a) can also be written in terms of the open-circuit voltage gain A_{vB} , as

$$R_{oB} = r_o + A_{vB} R'_L \quad (6.17b)$$

which is the BJT counterpart of the MOS expression in Eq. (6.10C). Another useful form for R_{oB} can be obtained from Eq. (6.17a),

$$R_{oB} = R'_L + (1 + g_m R'_L) r_o \quad (6.17c)$$

which is the BJT counterpart of the MOS expression in Eq. (6.10B). In Eq. (6.17c) the second term is much larger than the first, resulting in the approximate expression

$$R_{oB} \approx (1 + g_m R'_L) r_o \quad (6.17d)$$

which corresponds to Eq. (6.10C) for the MOS case.

Equation (6.17d) clearly indicates that the inclusion of an emitter resistance R_E increases the CB output resistance by the factor $(1 + g_m R'_L)$. Thus, as R_E is increased from 0 to ∞ , the output resistance increases from $r_o + (1 + g_m R'_L) r_o = (1 + g_m) r_o \approx g_m r_o$. This upper limit on the value of R_{oB} , dictated by the finite β of the BJT, has no counterpart in the MOS case and, as will be seen later, has important implications for circuit design. Finally, we note that for $R_E \ll r_o$, Eq. (6.17d) can be approximated by

$$R_{oB} \approx (1 + g_m R'_L) r_o \quad (6.17e)$$

A useful summary of the formulas for R_{oB} and R_{iB} is provided in Fig. 6.35.

The result above can be used to obtain the overall voltage gain G_v as

$$G_v = G_{vB} \frac{R_L}{R_L + R_{oB}} \quad (6.12b)$$

where

$$G_{vB} = \frac{R'_L}{R'_L + R_E} A_{vB} = \frac{r_o}{r_o + R_E} A_{vB} \quad (6.12c)$$

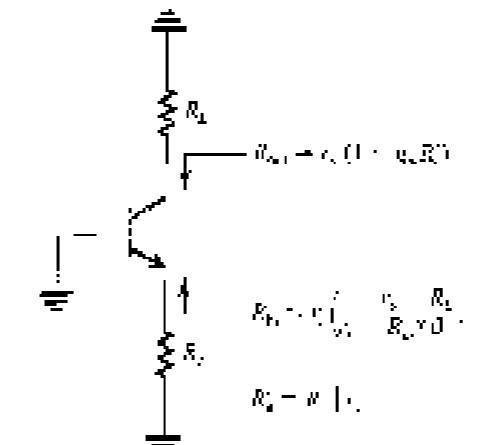


FIGURE 6.35 Input and output resistances of the CB amplifier.

The high-frequency response of the common-base circuit can be evaluated in a manner similar to that used for the MOSFET.

EXERCISE

- 6.35 Consider the BJT circuit of Fig. 6.34 with $V_B = 1$ mA, $\beta = 100$, $r_o = 400$ Ω , $R'_L = 100$ k Ω , $R_E = 1$ k Ω , $R_B = 100$ k Ω , and $G_{vB} = 100$. Find i_B , i_C , i_E , v_{CE} , and v_{BE} . If v_{BE} is a 5-mV peak-to-peak sine wave, find the corresponding peak-to-peak values of i_B , i_C , and i_E . Assume $r_o \gg R_E$.

6.33 A Concluding Remark

The common-gate and common-base circuits have open-circuit voltage gains A_{vG} almost equal to those of the common-source and common-emitter circuits. Their input resistance, however, is much smaller and their output resistance much larger than the corresponding values for the CS and CB amplifiers. These two properties, though not usually desirable in voltage amplifiers, make the CG and CB circuits suitable as current buffers. The inherent Miller effect makes the high-frequency response of the CG and CB circuits far superior to that of the CS and CE amplifiers. The most significant application of the CG and CB circuits is in a configuration known as the cascode amplifier, which we shall study next.

6.8 THE CASCODE AMPLIFIER

By placing a common-gate (common-base) amplifier stage in cascade with a common-source (common-emitter) amplifier stage, a very stable and versatile amplifier circuit results. It is known as the **cascode configuration**¹¹ and has been in use for nearly three quarters of a century, obviously in a wide variety of technologies.

¹¹ The name was coined back in the days of vacuum tubes and is a shortened version of "crossed cathode," since, in the tube version, the output (anode) of the first tube is the cathode of the second.

The basic idea behind the cascode amplifier is to combine the high input resistance and large transconductance achieved in a common-source (common-emitter) amplifier with the current-buffering property and the superior high-frequency response of the common-gate (common-base) circuit. As will be seen shortly, the cascode amplifier can be designed to obtain a wider bandwidth but equal dc gain as compared to the common-source (common-emitter) amplifier. Alternatively, it can be designed to increase the dc gain while leaving the gain-bandwidth product unchanged. Of course, there is a continuum of possibilities between these two extremes.

Although the cascode amplifier is formed by cascading two amplifiers stages, it is often thought of and treated as a single stage amplifier. Therefore it belongs in this chapter.

6.8.1 The MOS Cascode

Figure 6.36(a) shows the MOS cascode amplifier. Here transistor Q_1 is connected in the common-source configuration and provides its output to the input terminal (i.e., source) of transistor Q_2 . Transistor Q_2 has a constant dc voltage, V_{bias} , applied to its gate. Thus the signal voltage at the gate of Q_2 is zero, and Q_2 is operating as a CG amplifier with a constant current load, I . Obviously both Q_1 and Q_2 will be operating at dc drain currents equal to I . As in previous cases, feedback in the overall circuit that incorporates the cascode amplifier establishes an appropriate dc voltage at the gate of Q_1 so that its drain current is equal to I . Also, the value of V_{bias} has to be chosen so that both Q_1 and Q_2 operate in the saturation region at all times.

Small-Signal Analysis We begin with a qualitative description of the operation of the cascode circuit. In response to the input signal voltage v_i , the common-source transistor Q_1 conducts a current signal $i_{ds1}(v_i)$ in its drain terminal and feeds it as the source terminal of the common-gate transistor Q_2 , called the cascode transistor. Transistor Q_2 passes the signal current $i_{ds2}(v_i)$ or, in its drain, where it is supplied to a load resistance R_L (not shown in Fig. 6.36) at a very high output resistance, R_{out} . The cascode transistor Q_2 acts in effect as a buffer, presenting a low input resistance to the drain of Q_1 and providing a high resistance at the amplifier output.

Next we analyze the cascode amplifier circuit to determine its characteristic parameters. Figure 6.36(b) shows the cascode circuit prepared for small-signal analysis and with a resistance R_L shown at the output. R_L is assumed to include the output resistance of current source I as well as an actual load resistance, if any. The diagram also indicates various input and output resistances obtained using the results of the analysis of the CS and CG amplifiers in previous sections. Note in particular that the CS transistor Q_1 provides the cascode amplifier with an infinite input resistance. Also, at the drain of Q_1 looking "downward," we see the output resistance of the CS transistor Q_1 , r_{ds1} . Looking "upward," we see the input resistance of the CG transistor Q_2 .

$$R_{in} = \frac{1}{g_{m1} + g_{m2}r_{ds2}} + R_{ds1} \quad (6.122)$$

where

$$g_{m1,2} = 1 + (g_{sd1} + g_{sd2})r_{ds1} \quad (6.123)$$

Thus the total resistance between the drain of Q_1 and ground is

$$R_{ds1} = r_{ds1} + \frac{1}{g_{m1,2} + g_{m2}r_{ds2}} + R_{ds2} \quad (6.124)$$

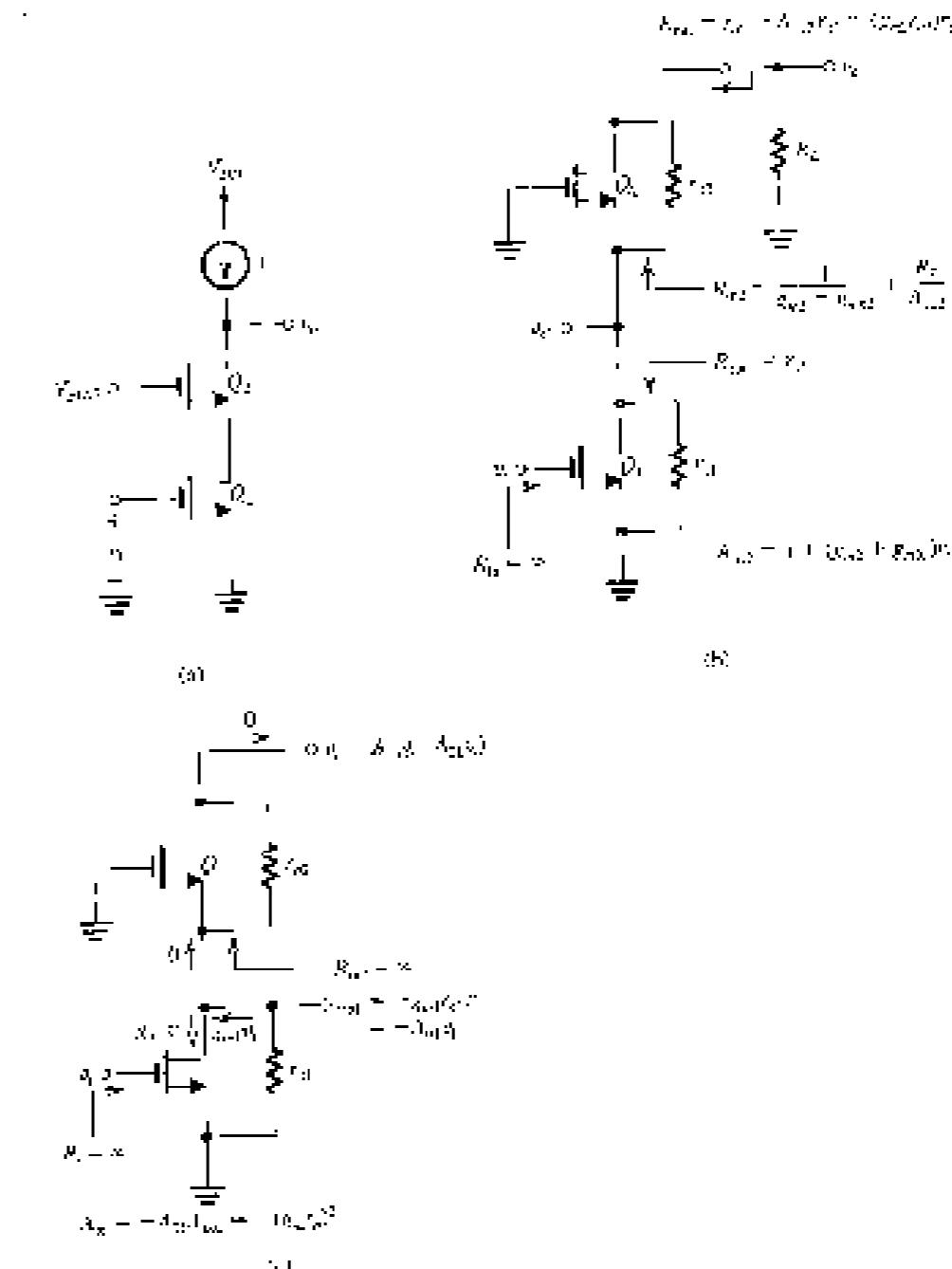


FIGURE 6.36 (a) The MOS cascode amplifier. (b) The circuit prepared for small-signal analysis with an output load resistor R_L included. (c) The circuit with the output load removed.

Figure 6.36(b) also indicates that the output resistance of the cascode amplifier, R_{out} , is given by

$$R_{out} = r_{ds2} + g_{m2}r_{ds1} \quad (6.125)$$

which has been obtained using the formula in Eq. (6.102) and noting that the resistance R_{ds2} is the source of the CG transistor Q_2 is the output resistance r_{ds2} of Q_2 . Substituting for

A_{out} from Eq. (6.127) in Eq. (6.125) yields

$$R_{\text{out}} = r_{\text{ds}} + [1 + (\gamma_{\text{ds}} + g_{\text{m}Q_1})r_{\text{ds}}]r_{\text{d}} \quad (6.126)$$

which can be approximated as

$$R_{\text{out}} \approx (g_{\text{m}Q_1}r_{\text{d}})r_{\text{ds}} = A_{\text{m}}r_{\text{d}} \quad (6.127)$$

Thus the cascode transistor raises the level of output resistance by a factor equal to its intrinsic gain, from r_{d} to $A_{\text{m}}r_{\text{d}}$, the CS amplifier to $A_{\text{m}}r_{\text{d}}$.

Another observation to make of the cascode amplifier circuit in Fig. 6.36(b) is that when a signal source v_{in} with an internal resistance R_{in} is connected to the input, the infinite input resistance of the amplifier causes

$$v_{\text{in}} = v_{\text{in}}$$

Thus,

$$G_v = A_{\text{m}}$$

Also, the input bias amplifier is unilateral; thus,

$$R_{\text{in}} = R_{\text{in}}$$

The open-circuit voltage gain A_{m} of the cascode amplifier can be easily determined from the circuit in Fig. 6.36(b), which shows the amplifier operating with the output open-circuited. Since R_{out} will be infinite, the gain of the CS stage Q_1 will be

$$\frac{v_{\text{d}}}{v_{\text{i}}} = -g_{\text{m}Q_1}r_{\text{d}} \approx -A_{\text{m}}$$

The signal v_{d} will be amplified by the open-circuit voltage gain A_{out} of the CG transistor Q_2 to obtain

$$v_{\text{o}} = A_{\text{out}}v_{\text{d}}$$

Thus,

$$\begin{aligned} A_{\text{m}} &= A_{\text{out}}A_{\text{d}} \\ &\equiv -A_{\text{m}}A_{\text{d}} \end{aligned} \quad (6.128)$$

which for the usual case of equal intrinsic gains becomes

$$A_{\text{m}} = A_{\text{d}}^2 \approx -(g_{\text{m}Q_1}r_{\text{d}})^2 \quad (6.129)$$

We conclude that cascading reduces the magnitude of the open-circuit voltage gain from A_{m} of the CS amplifier to A_{d} .

We are now in a position to derive an expression for the short-circuit transconductance G_{m} of the cascode amplifier. From the definitions and the equivalent circuits in Table 1.3,

$$A_{\text{m}} = G_{\text{m}}R_{\text{d}}$$

Substituting for A_{m} from Eq. (6.128) and for $R_{\text{d}} = R_{\text{out}}$ from Eq. (6.125) gives, for G_{m} ,

$$\begin{aligned} G_{\text{m}} &= \frac{A_{\text{d}}A_{\text{out}}}{r_{\text{ds}} + A_{\text{m}}r_{\text{d}}} \\ &= \frac{g_{\text{m}Q_1}r_{\text{d}}[1 + (\gamma_{\text{ds}} + g_{\text{m}Q_1})r_{\text{d}}]}{r_{\text{ds}}[1 + (\gamma_{\text{ds}} + g_{\text{m}Q_1})r_{\text{d}}]r_{\text{d}}} \\ &\approx g_{\text{m}Q_1} \end{aligned} \quad (6.130)$$

which confirms the value obtained earlier in the qualitative analysis.

The operation of the cascode amplifier could now be apparent. In response to v_{i} , the CG transistor provides a drain current i_{d,Q_2} , which the CG transistor passes on to R_{d} and, in the process, increases the output resistance by A_{d} . It is the increase in R_{d} to $A_{\text{d}}r_{\text{d}}$ that increases the open-circuit voltage gain in $(g_{\text{m}Q_1})(A_{\text{d}}r_{\text{d}}) = A_{\text{m}}^2$. Figure 6.37 provides a useful summary of the operation. Two input equivalent circuits are shown in Fig. 6.37(a) and (b), and an equivalent circuit for determining the voltage gain of the CS stage Q_1 is presented in Fig. 6.37(c). The voltage gain A_{m} can be found from either (a) the two equivalent circuits in Fig. 6.37(a) and (b). Using that in Fig. 6.37(b) gives

$$A_{\text{m}} = -A_{\text{d}} \frac{R_{\text{d}}}{R_{\text{d}} + A_{\text{d}}r_{\text{d}}} \quad (6.131)$$

We immediately see that if we are to realize the large gain of which the cascode is capable, resistance R_{d} should be large. At the very least, R_{d} should be of the order of $A_{\text{m}}r_{\text{d}}$. For $R_{\text{d}} \gg A_{\text{m}}r_{\text{d}}$, $A_{\text{m}} = -A_{\text{d}}^2/2$.

The gain of the CS stage is important, because its value determines the Miller effect in that stage. From the equivalent circuit in Fig. 6.37(c),

$$\frac{v_{\text{d}}}{v_{\text{i}}} = -g_{\text{m}Q_1}r_{\text{d}} \parallel \left(\frac{1}{r_{\text{ds}}} + \frac{R_{\text{d}}}{A_{\text{d}}r_{\text{d}}} \right) \quad (6.132)$$

or $R_{\text{d}} = A_{\text{d}}r_{\text{d}}$

$$\begin{aligned} \frac{v_{\text{d}}}{v_{\text{i}}} &= -g_{\text{m}Q_1}r_{\text{d}} \parallel \left(\frac{1}{r_{\text{ds}}} + r_{\text{ds}} \right) \\ &\equiv -\frac{1}{2}g_{\text{m}Q_1}r_{\text{d}} = -\frac{1}{2}A_{\text{m}} \end{aligned} \quad (6.133)$$

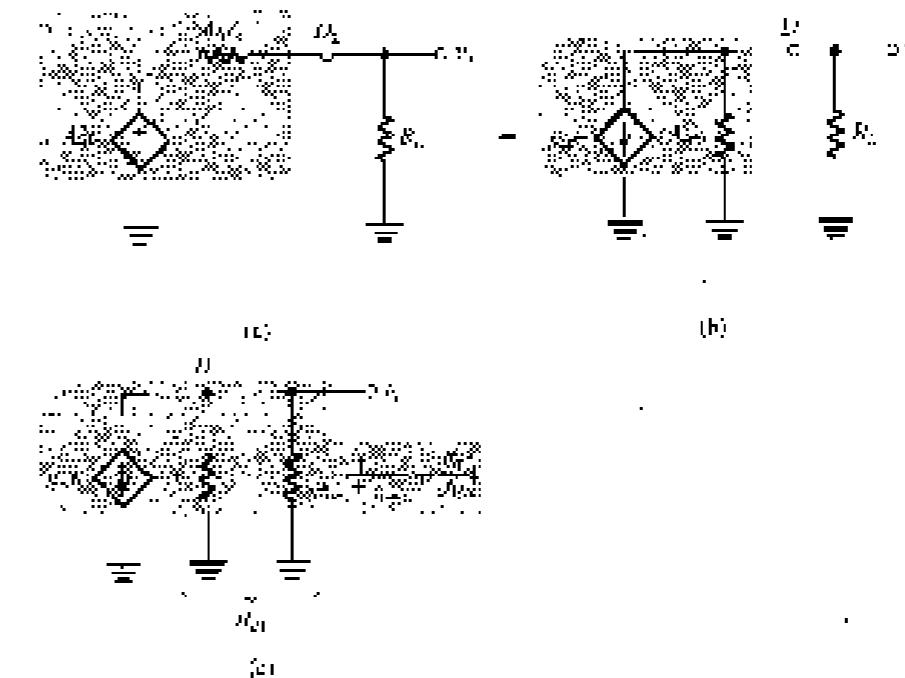


FIGURE 6.37 (a) and (b) Two equivalent circuits for the output of the cascode amplifier. Either circuit can be used to determine the gain $A_{\text{m}} = v_{\text{o}}/v_{\text{i}}$, which is equal to G_{m} when $R_{\text{d}} \rightarrow \infty$ and thus $v_{\text{o}} = v_{\text{d}}$. (c) Equivalent circuit for determining the voltage gain of the CS stage, Q_1 .

Thus we see that when R_1 is large and the cascade amplifier is realizing a substantial gain, a good part of the gain is obtained in the CS stage. This is not good news considering the Miller effect as we shall see shortly. To keep the gain of the CS stage relatively low, R_1 has to be lowered. For instance, for $R_2 = 1\text{ k}\Omega$, $R_3 = 10\text{ k}\Omega$ and values of β

$$\frac{v_0}{v_1} = -g_m \left[r_s \right] \left(\frac{1}{\sqrt{\epsilon_m}} - \frac{1}{g_m} \right)$$

Unfortunately, however, in this case the radius of the cascade is drastically reduced, as can be seen by substituting $R_0 = r_0$ in Eq. (6.13),

$$A_1 = -4 \left(\frac{r_0}{r_0 + 2r_1} \right)^2, \quad r_1 > 0. \quad (6.13)$$

That is, the grid of the cascade becomes equal to that realized in a single CS stage? Does this mean that the cascade can be used for this case? Not really, as we shall prove in

6.6.2 Frequency Response of the MOS Cascoda

Figure 6.39 shows the cascode amplifier with all transistor internal capacitances indicated. Also included is a capacitance C_{in} , the purpose to represent the combination of C_{in} , the input capacitance of a preceding amplifier stage (if any), and a source capacitance (if any). Note that C_{out} and C_{load} appear in parallel, and we shall combine them in the following analysis. Similarly, C_{in} and C_{in} appear in parallel and will be combined.

The easiest and, in fact, quite insightful approach is determining the β -CP frequency f_{β} by the open-circuit voltage-constant method. We shall do so here in the process. Likewise, the formulae derived in Section 5.6.2 and 5.7.1 for the various resistances:

1. Capacitance C_{12} sees a resistance R_{out} .
 2. Capacitance C_{23} sees a resistance $R_{\text{out},1}$, which can be obtained by adapting the formula in Eq. (6.36).

$$R_{\text{ext}} = \frac{1}{(1 + R_{\text{in}})R_{\text{in}} + R_{\text{ext}}} \quad (6.135)$$

where R_1 , the total resistance of Ω_1 , is given by Eq. (12).

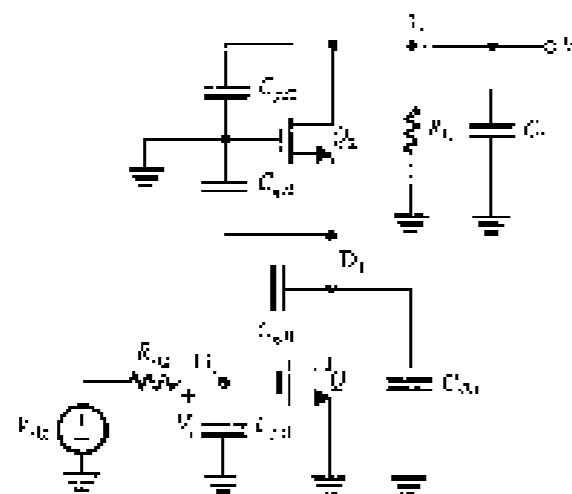


FIGURE 6.38 The *casanova* function takes the various names and responsibilities in relation

4. Capacitors ($C_{act} + C_{par}$) sees a resistance R_{in}

With the resistances determined, the effective rate constant k_{eff} can be computed as

$$\begin{aligned} \tau_R &= C_{R,1} R_{2,1} + C_{R,21} (1 - g_{11} R_{1,1}) R_{1,21} - R_{1,1} \\ &\quad + (C_{R,21} - C_{R,1}) R_{1,1,1}, \quad C_{R,1} \in C_{\mathcal{S}}(S^1(R_1) \parallel R_{1,1}) \end{aligned} \quad (6.126)$$

and the 3-dB frequency (ω_0)

$$J_\mu \equiv \frac{1}{\sqrt{-g}} \partial_\mu$$

To gain insight regarding what limits the high-frequency gain of the MOS cascode amplifier, we rewrite Eq. (6) in the form

$$\begin{aligned} \bar{r}_d = & R_{ds}(C_{sv}) - C_{sv}(1 + g_{sv}(R_d)) + R_{dv}(C_{sv} + C_{av} + C_{dv}) \\ & + (R_v + R_{dv})(C_v + C_{dv}). \end{aligned} \quad (6.177)$$

In the case of a large R_{in} , the first term can dominate, especially if the Miller multiplier ($1 + g_{\text{M}} R_{\text{in}}$) is large. This in turn happens when the load resistance R_L is larger (or the order of) $A_{\text{M}} r_s$, causing R_{in} to be large and requiring the first stage, Q_1 , to provide a large proportion of the gain. It follows that when R_{in} is large, to extend the bandwidth we have to lower R_L to the order of r_s . This in turn lowers R_{in} , and hence R_{in} and render the Miller effect insignificant. Notice however, that the dc gain of the example will then be g_{M} . Thus, while the dc gain will be the same as (or a little higher than) the achieved in μA3 amplifier, the bandwidth will be smaller.

In the case where $R_{\text{eff}} \gg 1$, the Miller effect in Q_1 will no longer be of concern. At the value of R_L (or the order of $1 - r_{\text{in}}$) can then be used to realize the large dc gains possible with a cascode amplifier—that is, a ΔV_{out} on the order of A_{in}^2 . Equation (6.1.27) indicates that in this case the third term will usually be dominant. To pursue this point a little further, consider the case $R_{\text{eff}} = 0$, and assume that the middle term is much smaller than the first and last terms, that

$$V_{\mu} \sim (C_0 + C_{\mu\nu\rho} x^{\rho}) X_{\mu}$$

and the λ will increase as b increases.

$$f_2 = \frac{1}{2\pi(C_1 - C_{1,0})(R_1 \parallel R_{1,0})} \quad (8.13)$$

which is of the same form as the formula for the CS amplifier with $R_{\text{out}} = 0$ (Eq. 6.79). Here, however, $(R_{\text{in}} - R_{\text{out}})$ is larger than R_{in} by a factor of about α_2 . Thus the β_m of the cascade will be lower than that of the CS amplifier by the same factor α_2 . Figure 6.79 shows a sketch of the frequency response of the cascade and of the corresponding common-emitter amplifier. We observe that in this case cascading increases the dc gain by a factor A_2 while keeping the noise-equivalent frequency unchanged.

$$f_i = \frac{1}{2\pi C_0 + C_{i,0}} \quad (0.139)$$

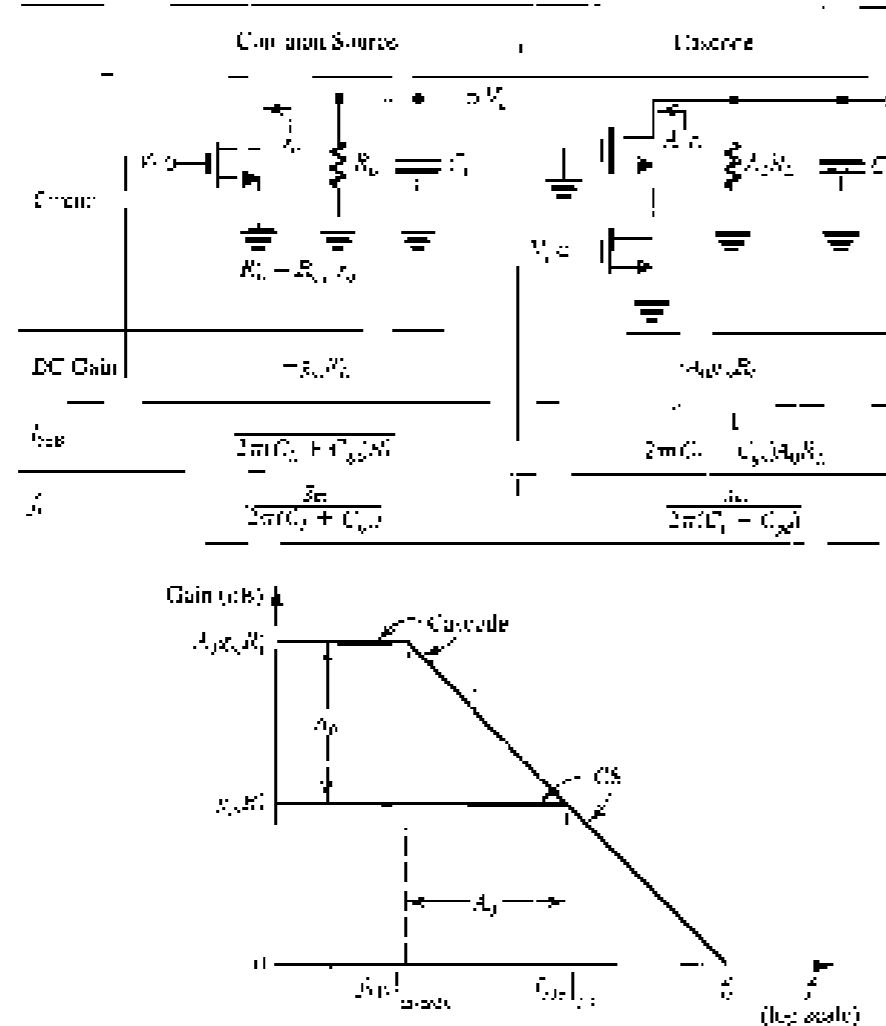


FIGURE 6.39 Effect of cascading two gain stages. In this case $k_T = 0$. Cascoding can increase the Δ gain by the factor A_2 while keeping the Δ -gain frequency constant. Note that to achieve the Δ - g_m gain, the load resistance must be increased by the factor A_2 .

This example illustrates the advantages of cascading by comparing the performance of a cascode amplifier with that of a common-source amplifier in two cases:

- (a) The resistance of the signal source is significant: $R_{SD} = 10 \text{ k}\Omega$
- (b) R_{SD} is negligibly small.

Assume all MOSFETs have W/L of $7.2 \mu\text{m}/36 \mu\text{m}$ and are operating at $I_D = 0.0 \mu\text{A}$, $k_T = 1.25 \text{ m}\text{A/V}$, $g = 0.2$, $L_s = 20 \text{ fF}$, $C_{ox} = 5 \text{ fF}$, $C_{gd} = 5 \text{ fF}$, and $C_{ds} = 5 \text{ fF}$ (assuming $C_{gs} = 5 \text{ fF}$). To match r_o , let $R_o = r_o = 20 \text{ k}\Omega$ for the CS amplifier and $R_o = R_{SD}$ for the cascode amplifier. For all cases determine α_o , f_o , and f_c .

Solution

(a) For the CS amplifier:

$$\alpha_o = g_o r_o = 1.25 \times 20 = 25 \text{ V/V}$$

$$A_{o2} = -g_o (R_o + r_o) = -g_o (r_o + r_o) \\ = -\frac{1}{2} g_o = -0.25 \text{ V/V}$$

$$z_h = C_{gs} R_{SD} + C_{gd} [(1 + g_o R_o) R_{SD} - R_o] + (C_{ds} - C_{gd}) R_o$$

$$R_o' = r_o \| R_o = r_o + r_o = 10 \text{ k}\Omega$$

$$r_o = 20 \times 10 = 5[1 + (2.5)(10 + 10)] = 5 \times 5(10 + 10) \\ = 200 + 725 + 100 = 1025 \text{ pF}$$

From

$$f_o = \frac{1}{2\pi \times 1025 \times 10} = 155 \text{ MHz}$$

$$f_c = \sqrt{A_{o2} f_o} = \sqrt{0.25 \times 155} = 1.94 \text{ GHz}$$

For the cascode amplifier:

$$\alpha_o = g_o r_o = 1.25 \times 20 = 25 \text{ V/V}$$

$$A_{o2} = 1 + g_{o2} + g_{o2} (r_{o2}) = 1 + (1.25 + 0.2 \times 1.25) \times 20 \\ = 1 + 1.5 \times 20 = 31 \text{ V/V}$$

$$R_{SD} = r_o = 20 \text{ k}\Omega$$

$$R_{DS} = \frac{1}{g_{o2} + g_{o2} (r_{o2})} = \frac{1}{1.25 + 31} = 1.5 \text{ k}\Omega$$

$$R_{D1} = R_{SD} \| R_{DS} = 20 \| 1.5 = 1.52 \text{ k}\Omega$$

$$R_{D2} = r_{o2} + A_{o2} r_{o2} = 20 + 31 \times 20 = 640 \text{ k}\Omega$$

$$\frac{V_o}{V_s} = -g_{o2} (R_{o2}) = -1.25 \times 1.22 = -1.5 \text{ V/V}$$

$$A_{o2} = A_{o2} \frac{R_o}{R_o + R_{o2}} = 25 \times 31 \times \frac{20}{20 + 20} = -31.5 \text{ V/V}$$

$$z_h = R_{SD} [C_{gs} + C_{gd} (1 + g_{o2} R_{o2})] + R_{o2} [C_{gs2} + C_{gd2} (1 + g_{o2} R_{o2})]$$

$$+ (C_{ds} - C_{gd2}) (C_{ds} - C_{gd2} + C_{gs2})$$

$$r_o = 10(20 + 5[1 + 1.5] + 1.22 \times 5 + 3 \times 30) = (20 + 640)(5 + 1.5) \\ = 315 + 30.6 + 290.3 \\ = 625 \text{ pF}$$

$$f_o = \frac{1}{2\pi \times 625 \times 10^{-12}} = 344 \text{ MHz}$$

$$f_c = 25.3 \times 244 = 5.92 \text{ GHz}$$

The cascading has increased f_c by a factor of about 3.

(c) For the CS amplifier:

$$A_{v1} = -2.5 \text{ V/V}$$

$$r_i = (C_{g1} + C_s + C_{ds})R_s$$

$$= 5^2 \times 150 \times 10^{-12} = 150 \text{ pS}$$

$$f_s = \frac{1}{2\pi \times 150 \times 10^{-12}} = 1.06 \text{ GHz}$$

$$f_l = 12.5 \times 1.06 = 13.3 \text{ GHz}$$

For the cascode amplifier:

$$A_{v2} = -\frac{R_o}{R_{ds2} + R_{in2}}$$

$$= -1.5 \times 21 \times \frac{640}{100 + 640} = -388 \text{ V/V}$$

$$R_{ds2} = \frac{1}{R_{in2} + r_{ds2}} + \frac{R_o}{A_{v2}} = \frac{1}{1.5} + \frac{1}{388}$$

$$= 21.2 \text{ k}\Omega$$

$$R_{ds2} = 21.1 \parallel 21 = 10.5 \text{ k}\Omega$$

$$r_o = R_{ds2}(C_{g22} + C_{ds2} + C_{s22}) + (R_{ds2} + R_{in2})(C_1 + C_{s12} + C_{d12})$$

$$= 10.5(5 + 20) + (610 \parallel 640)(5 + 5 - 5)$$

$$= 700 + 4800 = 5500 \text{ }\mu\text{m}$$

$$f_s = \frac{1}{2\pi \times 5500 \times 10^{-12}} = 31.2 \text{ MHz}$$

$$f_l = 388 \times 31.2 = 12.1 \text{ GHz}$$

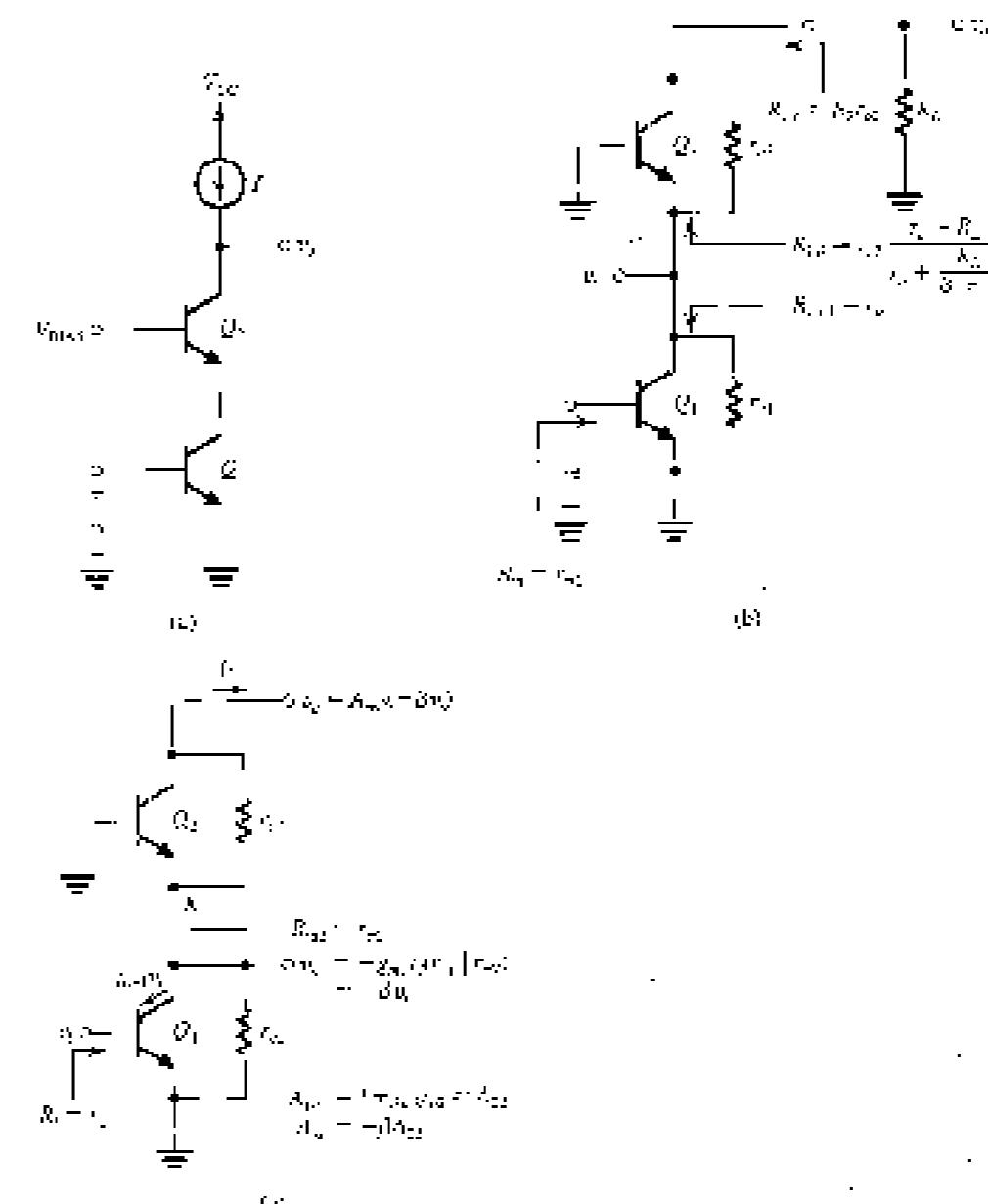
Thus cascading increases the output from 13.3 to 388 V/V. The unity-gain frequency (12.1 GHz bandwidth product), however, remains nearly constant.

EXERCISES

- 4.26 What is the Miller voltage gain A_{vM} required for a cascode amplifier requirement of $\beta = 100$, $r_{ds1} = 10 \text{ m}\Omega$, $C_{g1} = 20 \text{ fF}$, $R_s = 10 \text{ k}\Omega$, $R_{ds2} = 10 \text{ k}\Omega$, and $R_o = 10 \text{ M}\Omega$?
- 4.27 Consider a cascode amplifier operating at a bias current of $I_b = 10 \text{ }\mu\text{A}$ and for which $\beta = 100$, $r_{ds1} = 10 \text{ m}\Omega$, $C_{g1} = 20 \text{ fF}$, $R_s = 10 \text{ k}\Omega$, $R_{ds2} = 10 \text{ k}\Omega$, $R_o = 10 \text{ M}\Omega$, $C_{s12} = 10 \text{ fF}$, $C_{d12} = 10 \text{ fF}$, $C_{g22} = 20 \text{ fF}$, $C_{s22} = 10 \text{ fF}$, $C_{d22} = 10 \text{ fF}$, $V_{DD} = 10 \text{ V}$, $V_{SS} = -10 \text{ V}$, $V_{DD2} = 10 \text{ V}$, $V_{SS2} = -10 \text{ V}$, $V_{DD3} = 10 \text{ V}$, $V_{SS3} = -10 \text{ V}$, $V_{DD4} = 10 \text{ V}$, $V_{SS4} = -10 \text{ V}$, $V_{DD5} = 10 \text{ V}$, $V_{SS5} = -10 \text{ V}$, $V_{DD6} = 10 \text{ V}$, $V_{SS6} = -10 \text{ V}$, $V_{DD7} = 10 \text{ V}$, $V_{SS7} = -10 \text{ V}$, $V_{DD8} = 10 \text{ V}$, $V_{SS8} = -10 \text{ V}$, $V_{DD9} = 10 \text{ V}$, $V_{SS9} = -10 \text{ V}$, $V_{DD10} = 10 \text{ V}$, $V_{SS10} = -10 \text{ V}$, $V_{DD11} = 10 \text{ V}$, $V_{SS11} = -10 \text{ V}$, $V_{DD12} = 10 \text{ V}$, $V_{SS12} = -10 \text{ V}$, $V_{DD13} = 10 \text{ V}$, $V_{SS13} = -10 \text{ V}$, $V_{DD14} = 10 \text{ V}$, $V_{SS14} = -10 \text{ V}$, $V_{DD15} = 10 \text{ V}$, $V_{SS15} = -10 \text{ V}$, $V_{DD16} = 10 \text{ V}$, $V_{SS16} = -10 \text{ V}$, $V_{DD17} = 10 \text{ V}$, $V_{SS17} = -10 \text{ V}$, $V_{DD18} = 10 \text{ V}$, $V_{SS18} = -10 \text{ V}$, $V_{DD19} = 10 \text{ V}$, $V_{SS19} = -10 \text{ V}$, $V_{DD20} = 10 \text{ V}$, $V_{SS20} = -10 \text{ V}$, $V_{DD21} = 10 \text{ V}$, $V_{SS21} = -10 \text{ V}$, $V_{DD22} = 10 \text{ V}$, $V_{SS22} = -10 \text{ V}$, $V_{DD23} = 10 \text{ V}$, $V_{SS23} = -10 \text{ V}$, $V_{DD24} = 10 \text{ V}$, $V_{SS24} = -10 \text{ V}$, $V_{DD25} = 10 \text{ V}$, $V_{SS25} = -10 \text{ V}$, $V_{DD26} = 10 \text{ V}$, $V_{SS26} = -10 \text{ V}$, $V_{DD27} = 10 \text{ V}$, $V_{SS27} = -10 \text{ V}$, $V_{DD28} = 10 \text{ V}$, $V_{SS28} = -10 \text{ V}$, $V_{DD29} = 10 \text{ V}$, $V_{SS29} = -10 \text{ V}$, $V_{DD30} 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6.3.3 The BJT Cascode

Figure 6.40(a) shows the BJT cascode amplifier. The circuit is very similar to the MOS cascode, and the small-signal analysis follows in a similar fashion, as indicated in Fig. 6.40(b). Here we have shown the various input and output resistances. Observe that unlike the MOSFET cascode, which has an infinite input resistance, the BJT cascode has an input resistance of r_{in} (neglecting r_{ds}). The formula for R_{in} is the one we found in the analysis



in the common-base circuit (Eq. 6.112), the output resistance $R_{o,p} = \beta_2 r_o$ is found by substituting $K_p = r_o$ in Eq. (6.119) and making the approximation that $r_o r_h \gg \beta_2 R_{o,p}$. Note that $R_{o,p}$ is the largest output resistance that a C-B transistor can provide.

The open-circuit voltage gain A_{oc} and the no-load input resistance R_i can be found from the circuit in Fig. 6.4(b), in which the output is open-circuited. Observe that $R_{in} = r_{ds}$, which is usually much smaller than r_{ce} . As a result the total resistance between the collector of β_2 and ground is approximately r_{ce} . Thus the voltage gain realized at the C_B transistor β_1 is $-g_{ce}r_{ce} = -\beta$. Recalling that the open-circuit voltage gain of a CB amplifier is $(1 + g_{ce}r_{ce})\beta = \beta$, we see that the voltage gain A_{oc} is

$$A_{\text{ext}} = -\frac{g}{c} \mathbf{l}, \quad (6.140)$$

Putting all of these results together we obtain for the BJT cascode amplifier the equivalent circuit shown in Fig. 6.41(a). We note that compared to the common-emitter amplifier, cascading increases both the open-circuit voltage gain and the output resistance by a factor equal to the transistor β . This should be contrasted with the factor A_{in} encountered in the MOS cascode. The equivalent circuit can be easily converted to the transconductance form shown in Fig. 6.41(b). It shows that the short-circuit transconductance G_{m} of the cascode amplifier is equal to the transconductance g_{m} of the BJT. This should have been expected since G_{m} provides a current $g_{\text{m}} V_{\text{in}}$ to the emitter of the cascode transistor (Q_2), which in turn passes the current $g_{\text{m}} V_{\text{in}}$ (assuming $\text{Q}_2 = 0$) to its collector and to the load resistance R_L . In the process the cascode transistor reduces the resistance level from r_o at the collector of Q_1 to $g_{\text{m}} r_o$ at the collector of Q_2 . This is the by-now-familiar current buffering action of the common-base transistor.

The voltage gain of the CE transistor Q_1 can be determined from the equivalent circuit (Fig. 6.11(a)). The resistance between the collector of Q_1 and ground is the parallel equivalent

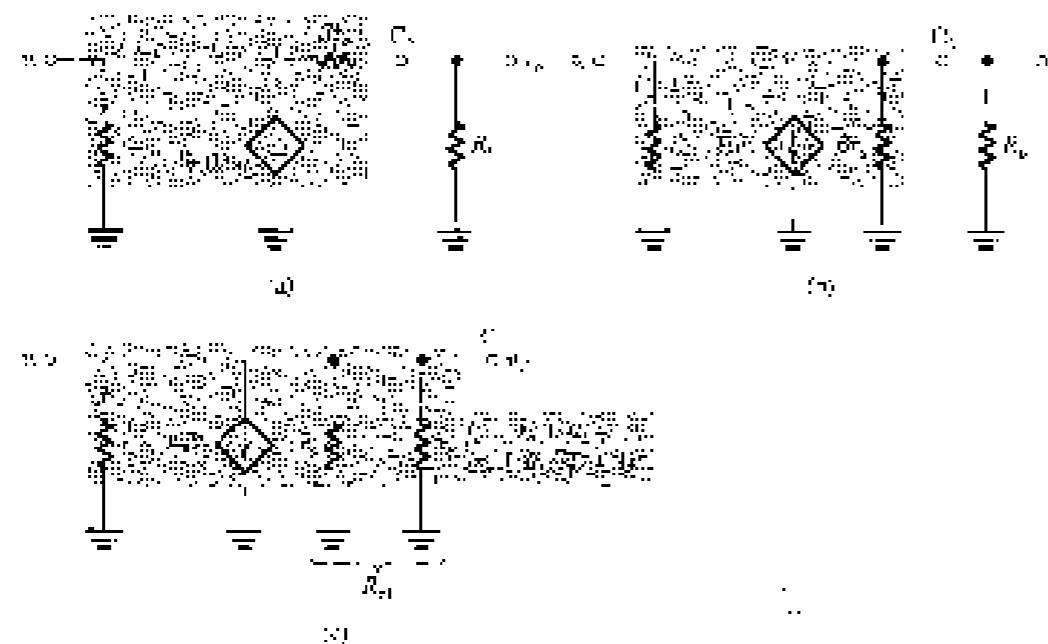


FIGURE 6.41 (a) Equivalent circuit for the two-stage amplifier in terms of the open-circuit voltage gain A_{v1} , $\beta_1 I_V$; (b) Equivalent circuit in terms of the overall short-circuit transconductance $g_{m1} = g_{o1}$; (c) High-level circuit for determining the sum of the currents I_o .

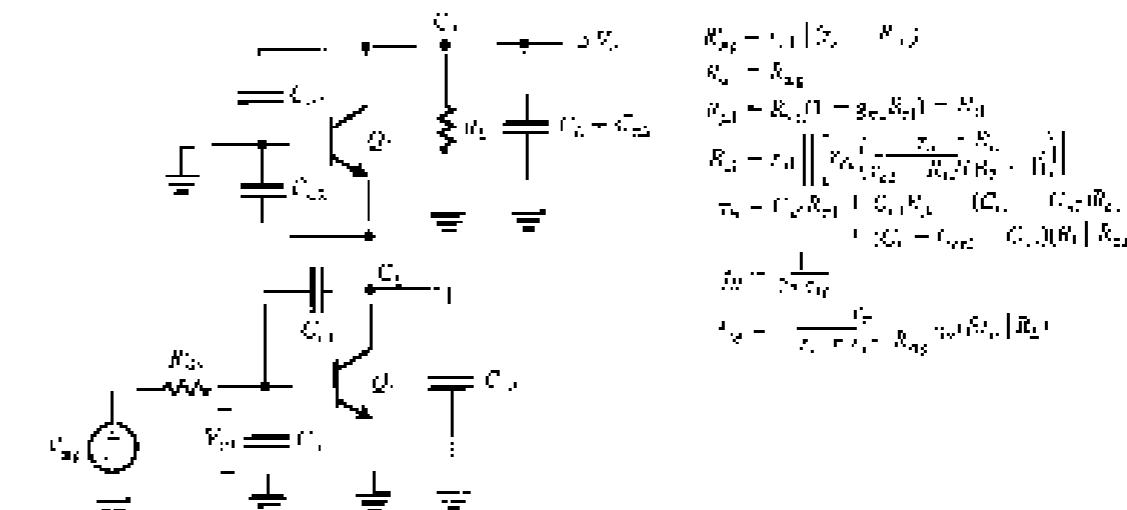


FIGURE 6.42 Determining the secondary sequence of the H₁-cysteine synthetase. Statistical analysis of the 31 experiments of Figure 6.41 gave estimates for each of the positions and the sub-unit C₁, 60% higher than the 100% limit.

at the output resistance of Q_1 , r_o , and the input resistance of the CT transistor, Q_2 , namely R_{in} . Note that for $R_{in} \ll r_o$ the latter reduces to r_o , as expected. However, R_{in} increases as R_{in} is increased. Of particular interest is the value of R_{in} obtained for $R_{in} = R_o$, namely $r_o = 12\Omega$. In addition, the load line is also of β_2 . The CT stage has a voltage gain of $-\beta_2/2$.

Finally, we present in Fig. 6.12 the circuit and the networks for determining the frequency response of the bipolar cascade. The analysis parallels that carried in the MOSFET case.

FRS1

The performance of the Class A PAF of Section 3 has been implemented in software as shown in Figure 16. The PAF is based on the design of the TGA-1000A amplifier. It has a 100 dB gain, 100 kHz bandwidth, and a 100 dB dynamic range. The PAF is designed to operate in a 100 MHz bandwidth, with a 100 dB dynamic range, and a 100 dB gain. The PAF is designed to operate in a 100 MHz bandwidth, with a 100 dB dynamic range, and a 100 dB gain. The PAF is designed to operate in a 100 MHz bandwidth, with a 100 dB dynamic range, and a 100 dB gain.

2.8.4 A Cascode Current Source

η : mentioned above, to realize the high voltage gain of which the cascode amplifier is capable, the load resistance R_L must be increased as the value of A_{vca} , for the MOSFET cascode or S_{ca} for the bipolar cascode. Recall, however, that R_L includes the output resistance of the driver, and implements the current-source load. Fig. 6.18 shows that the current source must have an output resistance that is at least A_{vca} for the MOS case (S_{ca} , for the BJT case). This rules out using the simple current-source circuits of Section 6.2 since their output resistances are

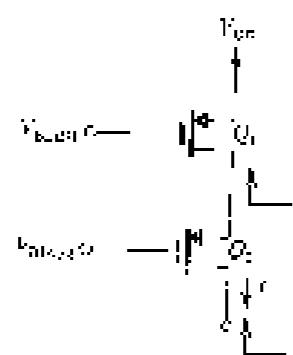


FIGURE 8.93 A second approach to

equal to r_o . Fortunately, there is a conceptually simple and effective solution—merely applying the cascading principle to the current source implementation. The idea is illustrated in Fig. 6.17, where \mathcal{Q}_1 is the current source transistor and \mathcal{Q}_2 is the electrode transistor. The V_{DS} voltage $V_{DS(1)}$ is chosen so that \mathcal{Q}_1 provides the required value of I . $V_{DS(2)}$ is chosen to keep \mathcal{Q}_2 in saturation at all times. While the resistance looking into the drain of \mathcal{Q}_1 is r_{o1} , the electrode resistor \mathcal{Q}_2 multiplies this resistance by $(\mu_{n,\text{sat}})$ and provides an output resistance for the current source given approximately by

$$R_n \in \{g_{\pi \circ f_i, j}\}_{i,j} \quad (6.12)$$

A similar arrangement can be used in the bipolar case. We will study a greater variety of current sources and current mirrors with improved performance in Section 6.7.

6.3.5 Double Cascading

The essence of the operation of the MOS cascode is that the CG cascode transistor multiplies the resistance in its source, which is r_s , of the CS transistor Q_1 , by its intrinsic gain A_{v1} to provide an output resistance $A_{v1}r_s$. It follows that we can increase the output resistance further by adding another level of cascading, as discussed in Fig. 14-14.

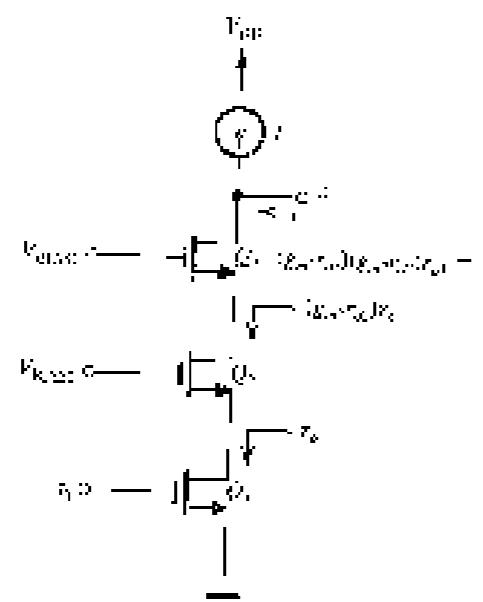


FIGURE G.44 Events and

now set \bar{Q}_3 is added, with the result that the output resistance is increased by the factor A_{in} . Thus, the output resistance of this double-gate-source amplifier is $A_{\text{in}}^2 r_o$. Note that an additional bias voltage has to be generated for the additional cascode transistor \bar{Q}_3 .

A drawback of double cascoding is that an additional transistor is now placed between the power-supply rails. Furthermore, since we are now dealing with output levels since on the order of V_{DD} , the current source I will also need to be implemented using a double cascode which adds yet one more transistor to the stack. The difficulty posed by stacking additional transistors is appreciated by recalling that in modern CMOS process technologies V_{DD} is only a little more than 1 V.

Finally, note that since the largest output resistance possible in a bipolar cascode is β , setting a certain level of cascoding does not provide any advantage.

6.8.6 The Folded Case

To avoid the problem of stacking a large number of transistors across a low-voltage power supply, one can use a PMOS transistor for the cascode device, as shown in Fig. 6.45. Here, as before, the NMOS transistor Q_1 is operating in the CS configuration, but the CG stage is implemented using the PMOS transistor Q_2 . An additional current source I_2 is needed to bias Q_2 and provide it with its active bias. Note that Q_1 is now operating at a bias current of $(I_1 - I_2)$. Finally, a low voltage V_{bias} is needed to provide an appropriate dc level for the gate of the cascode transistor Q_2 . Its value has to be selected so that Q_2 and Q_1 operate in the saturation region.

The small-signal operation of the circuit in Fig. 6.15 is similar to that of the NMOS cascode. The difference here is that the signal current $q_1 q_2$ is folded down and made to flow into the source terminal of Q_1 , which gives the circuit the name folded cascode.¹² The folded cascode is a very popular technique used in CMOS amplifiers.

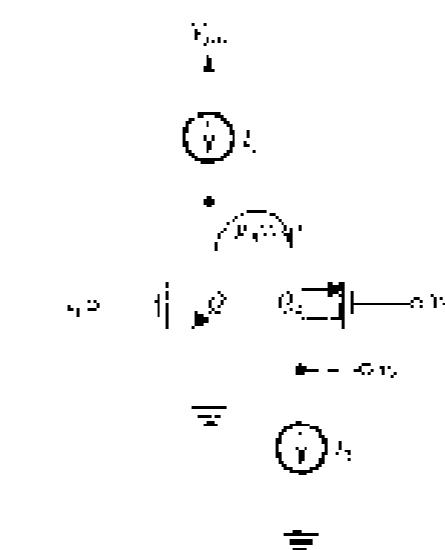


FIGURE 6.49 The Jitterbox.

¹⁴ The *z*-axis can be thought of as having been folded. In this way in the regular cascade sometimes referred to as a telescope cascade because the stacking of lenses has a resemblance to the action of a telescope.

EXERCISE

- 6.29 Consider the circuit shown in Fig. 6.5 for the case where $V_{DD} = 15$ V, $V_T = -1.5$ V, T_1 is operating in NMOS mode with drain current $I_D = 20 \mu A$, and T_2 is L . The current source I_1 is implemented using the simple-current mirror in Section 6.2, current source I_2 is set using a controlled-current source version of the circuit in Fig. 6.4(b). The transistors T_1 and T_2 are selected so that each operates at a drain-to-source voltage of 0.2 V.

 - What value of drain-to-source voltage is required for T_2 to switch off?
 - What is the minimum voltage required for the proper operation of current source I_2 ? Assume 0.1-V peak-to-peak signal with zero bias voltage at the drain of T_1 , what is the turn-on voltage of T_2 in this case?
 - What is the value of I_2 if T_2 has drain-to-source resistance equal to 10Ω ?
 - What is the minimum voltage required for proper operation of current source I_2 ?
 - Given the drain-to-source voltages in the previous question, what is the minimum range of signal swing at the gate of T_2 ? (Assume $V_{DD} = 15$ V, $V_T = -1.5$ V, $I_1 = 20 \mu A$, $I_2 = 0.5 \mu A$, $R_{DS1} = 10 \Omega$, and $R_{DS2} = 10 \Omega$.)

3.8.7 BiCMOS Cascades

As mentioned before, if the technology permits, the circuit designer can combine bipolar and MOS transistors in circuit configurations that take advantage of the unique features of each. As an example, Fig. 6.4-6 shows two possibilities for the Pd/MOS implementation of the cascode amplifier. In the circuit of Fig. 6.4-6(a), a MOSFET is used for the input device, thus providing the cascode with an infinite input resistance. On the other hand, a bipolar transistor is used for the cascode device, thus providing a large output resistance; this

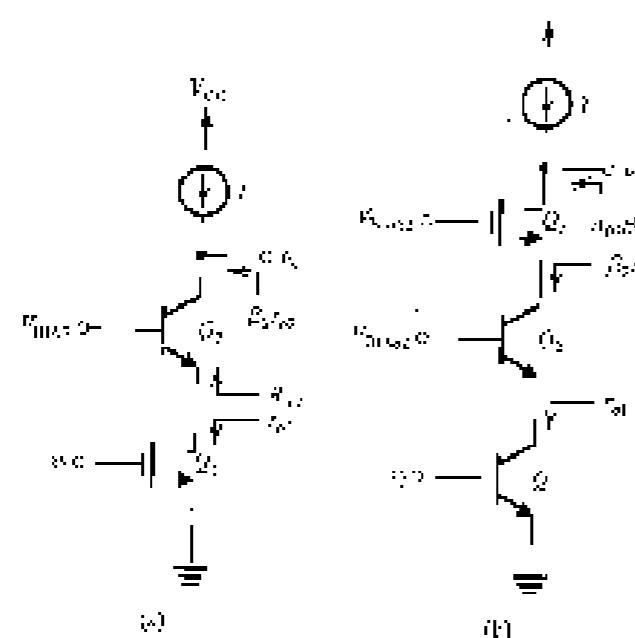


FIGURE 6.4G RICMOS (cont.)

EXERCISE

possible with a MOSFET cascode. This is because β of the BJT is usually larger than A_{vD} of the MOSFET and, more importantly, because τ_p of the BJT is much longer than τ_p of modern submicron MOSFETs. Also, the bipolar CB transistor provides a lower input resistance R_{in} than is usually obtained with a CG transistor, especially when R_s is low. The result is a lower total resistance between the gate of O_1 and ground and hence a reduced Miller effect in O_1 .

The circuit in Fig. 6-6(b) utilizes a MOSFET to implement the second level of cascading in a bipolar cascode amplifier. The reason for a MOSFET stage here is that while the maximum possible output resistance obtainable with a BJT is R_{out} , there is no such limit with the MOSFET, and indeed, O_2 raises the output resistance by the factor β_{MOS} .

REF ID: A6200

³ See also the discussion of the relevant provisions of the SIC 2008 classification rules in Part II of this paper. For the R-75, see Art. V, note 18; for the MCGTER, see Part IV, note 15; for the AIAA, see note 25.

6.9 THE CS AND CE AMPLIFIERS WITH SOURCE (EMITTER) DEGENERATION

Introducing a relatively small resistance (i.e., a "small" multiple of $1/k_B T_{DS}$) in the source of a CS amplifier (the emitter of a common-emitter amplifier) introduces negative feedback into the amplifier stage. As a result this technique provides the circuit designer with an additional parameter that can be effectively utilized to obtain certain desirable performance trade-offs for the gain reduction that source (emitter) degeneration causes. We have already seen some of this in sections 4.7 and 5.7. In this section we consider source and collector degeneration in CS amplifiers where r_o and $k_B T_{DS}$ have to be taken into account. We also demonstrate the use of source (emitter) degeneration to extend the amplification range.

6.2.1 The CS Amplifier with a Source Resistance

Figure 6.47(a) shows an active load CS amplifier with a source resistance R_s . Note that a signal v_{o1} will develop between body and source, and hence the body effect should be taken into account in the analysis. The circuit, prepared for small-signal analysis and with a resistance R_b , shown at the output, is presented in Fig. 6.47(b). To determine the output resistance R_{o1} , we reduce v_i to zero, which makes the circuit identical to that of a CG amplifier. Therefore we can obtain R_{o1} by using (2.10.13) as

$$g_{\mu\nu} = \epsilon^{-1} [1 + (g_{\mu} - g_{\nu})V_{\mu}] \delta \quad (3.142)$$

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$$\beta_{\infty} \approx 1.5 \quad \text{and} \quad \beta_{\infty} \approx 1.6 \quad \text{for } \alpha = 0.113. \quad (3.114)$$

The open-circuit voltage gain can be found from the circuit in Fig. 6.41(c). Notice that the current in N_1 must be zero, the voltage at the source, v_s , will be zero and thus $v_{o1} = v_s$ and $v_{o2} = 0$, resulting in

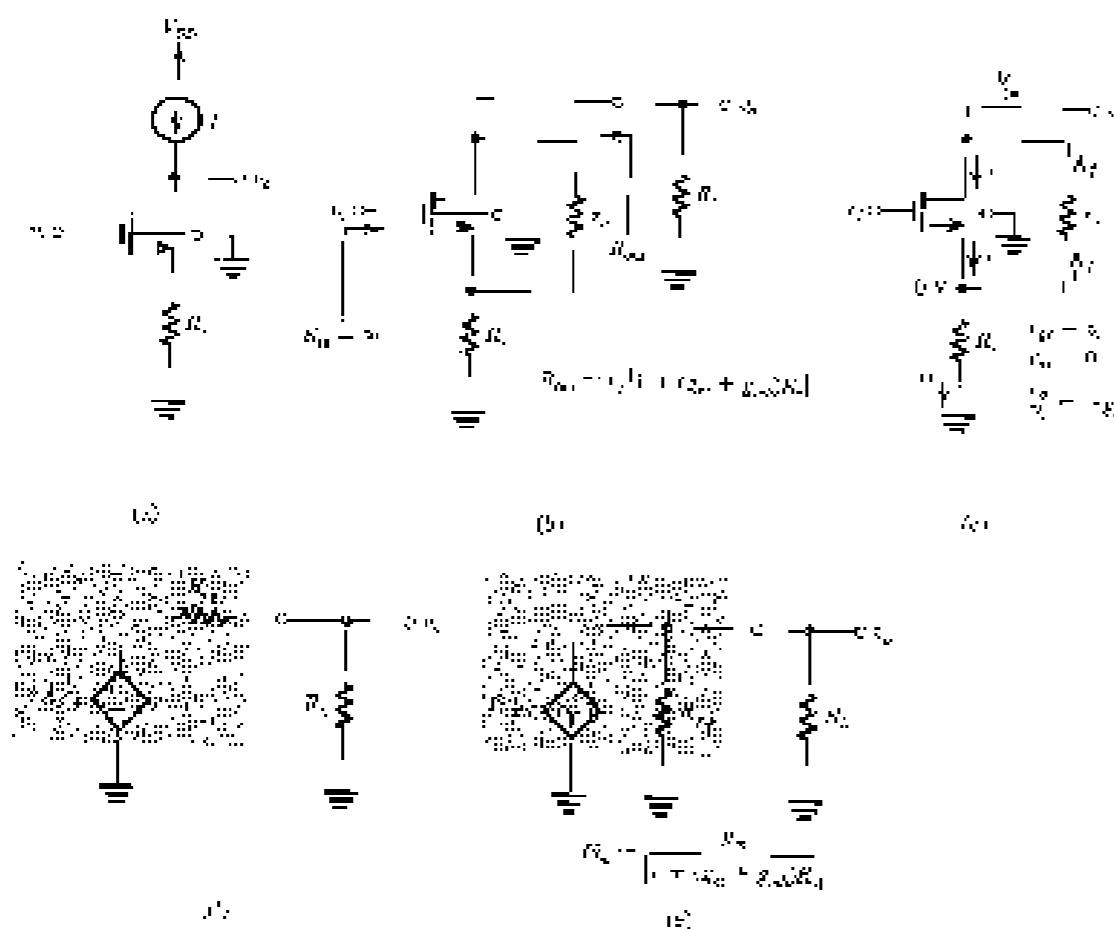


FIGURE 6.47 (a) A CS amplifier with a source degeneration resistor \$R_s\$. (b) Circuit for small-signal analysis. (c) Circuit with the output open-circuited at \$v_o\$. (d) Output equivalent circuit for finding output voltage \$v_o\$ in terms of \$v_i\$.

Since

$$v_o = -v_i \cdot r_o = -g_m r_o v_i = -g_m v_i / r_o$$

Thus,

$$A_{vo} = -g_m r_o = A_0$$

In other words, the resistance \$r_o\$ has no effect on \$A_{vo}\$!

Utilizing \$A_{vo} = A_0\$ and \$R_{vo}\$ from Eq. (6.14-1) enables us to obtain the amplifier output equivalent circuit shown in Fig. 6.48(d). An alternative equivalent circuit in terms of the short-circuit transconductance \$G_m\$ is shown in Fig. 6.49(c), where \$G_m\$ can be found from

$$G_m = \frac{|A_{vo}|}{R_{vo}} = \frac{A_0}{r_o [1 + (g_m + g_{sd})R_s]}$$

Thus,

$$G_m = \frac{A_0}{1 + (g_m + g_{sd})R_s} \quad (6.14-2)$$

The effect of \$R_s\$ is thus obvious: \$R_s\$ reduces the amplifier transconductance and increases its output resistance by the same factor: \$(1 + (g_m + g_{sd})R_s)\$. We will find in Chapter 8 when we study negative feedback formally that this factor is the *loop gain* of negative feedback introduced by \$R_s\$.

The voltage gain \$A_v\$ can be found as

$$A_v = A_{vo} \frac{R_L}{R_L + R_{vo}} \quad (6.14-3)$$

Thus, if \$R_s\$ is kept unchanged, \$A_v\$ will decrease, which is the price paid for the performance improvements obtained when \$R_s\$ is introduced. One such improvement is in the linearity of the amplifier. This comes about because only a fraction \$v_o / v_i\$ of the input signal \$v_i\$ now appears between gate and source. Derivation of an expression for \$v_o / v_i\$ is significantly complicated by the inclusion of \$v_o\$. The derivation should be done with the MOSPET equivalent-circuit model explicitly used. The result is

$$\frac{v_o}{v_i} = \frac{1}{1 + (g_m + g_{sd})R_s} \frac{R_L + R_{vo}}{R_L} \quad (6.14-4)$$

which for \$v_o \gg R_{vo}\$ reduces to the familiar relationship

$$\frac{v_o}{v_i} \approx \frac{1}{1 + (g_m + g_{sd})R_s} \quad (6.14-5)$$

Thus the value of \$R_s\$ can be used to control the magnitude of \$v_o\$, so as to obtain the desired linearity—at the expense, of course, of gain reduction.

Frequency Response. Another advantage of source degeneration is the ability to broaden the amplifier bandwidth. Figure 6.48(a) shows the amplifier with the internal capacitances \$C_{gs}\$ and \$C_{gd}\$ indicated. A capacitance \$C_L\$ that includes the MOSFET capacitance \$C_{ds}\$ is also shown at the output. The method of open-circuit time constants can be employed to obtain an estimate of the 3-dB frequency \$f_B\$. Toward that end we show in Fig. 6.48(b) the circuit for determining \$R_{eq}\$, which is the resistance seen by \$C_{pl}\$. We observe that \$R_{eq}\$ can be determined by simply adapting the formula in Eq. (6.30) to the case with source degeneration as follows:

$$R_{eq} = R_{vo}(1 + (i_o R'_o) + R'_o) \quad (6.14-6)$$

where

$$R'_o = R_o / R_{vo} \quad (6.14-7)$$

The formula for \$R_{eq}\$ can be seen to be simply

$$R_{eq} = R_o \parallel R_{vo} = R'_o \quad (6.14-8)$$

The formula for \$R_{eq}\$ is the most difficult to derive, and the derivation should be performed with the hybrid-\$\pi\$ model explicitly utilized. The result is

$$R_{eq} = \frac{R_{vo} + R_o}{1 + (g_m + g_{sd})R_o \left(\frac{r_o}{r_o + R_s} \right)} \quad (6.14-9)$$

When \$R_{vo}\$ is relatively large, the frequency response will be dominated by the Miller multiplication of \$C_{pl}\$. Another way for saying this is that \$C_{pl} R_{eq}\$ will be the largest of the

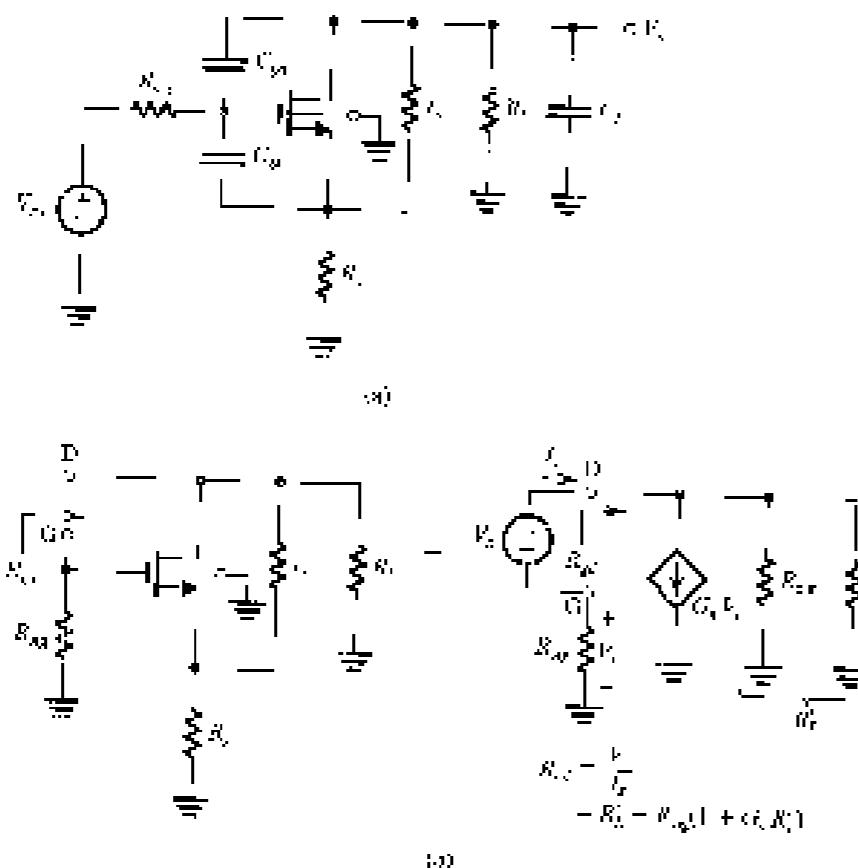


FIGURE 6.46 (a) The CS amplifier circuit with a load resistor R_L prepared for frequency-response analysis. (b) Determining the resistance R_{DS} seen by the capacitance C_F .

three other circuit time constants that make up τ_B :

$$\tau_T = C_{GS}R_{DS} + C_{DS}R_{DS} + C_FR_{DS} \quad (6.52)$$

enabling us to approximate τ_B as

$$\tau_B \approx C_{DS}R_{DS} \quad (6.53)$$

and correspondingly to obtain f_B as

$$f_B \approx \frac{1}{2\pi C_{DS}R_{DS}} \quad (6.54)$$

Now, as R_{DS} is increased, the gain magnitude $|A_{DS}| = G_{DS}R_{DS}$ will decrease, causing R_{DS} to decrease (Eq. 6.148), which in turn causes f_B to increase (Eq. 6.154). To mitigate the trade-off between gain and bandwidth that R_{DS} affords the designer, let us amplify Eq. 6.53 (Eq. 6.148) by assuming that $G_{DS}R_{DS} \gg 1$ and $G_{DS}R_{DS} \gg 1$,

$$R_{DS} \approx G_{DS}R_{DS} = |A_{DS}|R_{DS}$$

which can be substituted in Eq. (6.154) to obtain

$$f_B = \frac{1}{2\pi C_{DS}R_{DS}|A_{DS}|} \quad (6.55)$$

which very clearly shows the gain-bandwidth trade-off. The gain-bandwidth product remains constant:

$$\text{Gain-bandwidth product } f_T = |A_{DS}|f_B = \frac{1}{2\pi C_{DS}R_{DS}} \quad (6.56)$$

In practice, however, the other capacitances will play a role in determining f_B , and f_B will decrease somewhat as R_{DS} is increased.

EXERCISE

- (34) Consider the CS amplifier having the circuit of Fig. 6.46(a), $R_{DS} = 20 \text{ k}\Omega$, $C_{DS} = 10 \text{ pF}$, $C_{GS} = 10 \text{ pF}$, $C_F = 100 \text{ pF}$, $r_s = 10 \text{ M}\Omega$, $r_o = 10 \text{ M}\Omega$, $G_{DS} = 100 \text{ S}$, and $|A_{DS}| = 100$. Using the equations of the text, calculate the gain-bandwidth product f_T (the Report section provides a check), assuming R_{DS} is connected to ground with its value determined from the equation $R_{DS} = r_s(1 + G_{DS})$. Hint: $G_{DS} = 2$.

6.9.2 The CE Amplifier with an Emitter Resistance

Emitter degeneration is even more useful in the CE amplifier than source degeneration is in the CS amplifier. This is because emitter degeneration increases the input resistance of the CE amplifier. The input resistance of the CS amplifier is, of course, practically infinite to start with. Figure 6.49(a) shows an active-loaded CE amplifier with an emitter resistance R_E , usually in the range of 1 to 5 times r_s . Figure 6.49(b) shows the circuit for determining the three circuit time constants that make up τ_B .

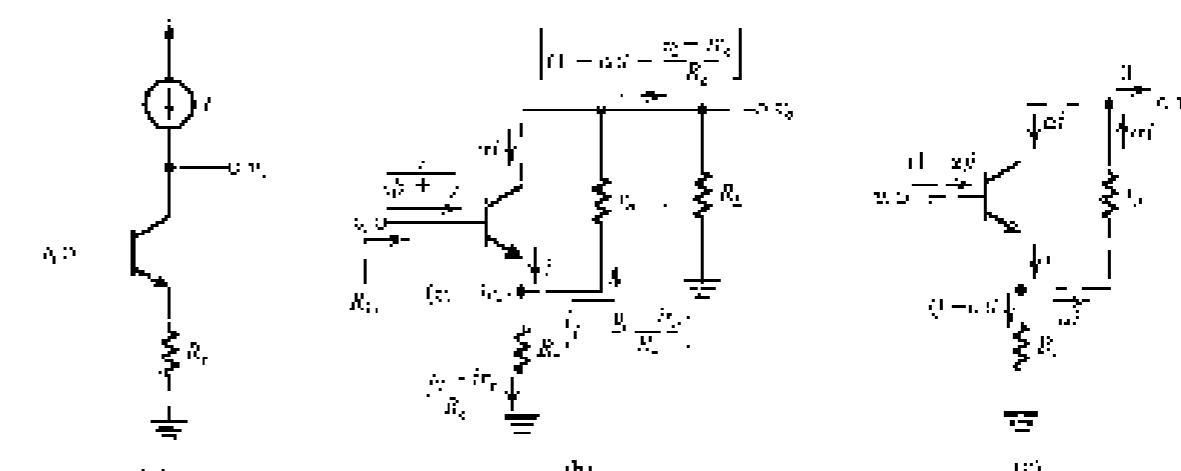


FIGURE 6.49 A CE amplifier with emitter degeneration. (a) circuit; (b) analysis to determine R_E and f_B starting from the other R_{CE} .

input resistance R_{in} , which, due to the presence of r_o , will depend on the value of R_L . With the aid of the analysis shown in Fig. 6.4(b), we can express the output voltage v_o as

$$v_o = (1 + \alpha)\left(\frac{r_o + R_L}{R_o}\right)R_L$$

Alternatively, we can express v_o as

$$v_o = (1 + \alpha)r_o + r_o\left(\frac{R_L + r_o}{R_o}\right)$$

Combining these two expressions of v_o yields an equation in r_o and R_L which can be rearranged to obtain

$$\begin{aligned} R_{in} &= \frac{r_o}{(1 + \beta - 1)} \\ &= (\beta - 1)r_o + (\beta + 1)R_o \frac{r_o + R_L}{r_o + R_o - R_L} \end{aligned} \quad (6.157)$$

Usually R_L is on the order of r_o , thus $R_L/(\beta - 1) \ll r_o$ and $R_L \ll r_o$. Taking account of these two conditions enables us to simplify the expression for R_{in} to

$$R_{in} \approx (\beta - 1)r_o + (\beta - 1)R_o \frac{1}{1 + R_o/r_o} \quad (6.158)$$

This expression indicates that the presence of r_o reduces the effect of R_o on increasing R_{in} . This is because r_o shunts away some of the current that would have flowed through R_o , for example, if $R_o = r_o$, $R_o = 1.0$, $r_o = 0.5R_o$.

To determine the open-circuit voltage gain A_{vo} , we utilize the circuit shown in Fig. 6.4(b). Analysis of this circuit is straightforward and can be shown to yield

$$A_{vo} = -g_m r_o \quad (6.159)$$

That is, the open-circuit voltage gain obtained with a relatively small R_o (i.e., on the order of r_o) remains very close to the value without R_o .

The output resistance R_o is identical to the value of R_{out} that we derived for the CB circuit (Eq. 6.118).

$$R_o = r_o(1 + g_m R_o) \quad (6.160)$$

Since $R_o = R_o/r_o$, since R_o is on the order of r_o , R_o is much smaller than r_o and $R_o \ll R_o$. Thus,

$$R_o \approx r_o(1 + g_m R_o) \quad (6.161)$$

The expressions for R_{in} , A_{vo} , and R_o in Eqs. (6.158), (6.159), and (6.161), respectively, can be used to determine the overall voltage gain for given values of source source and load resistance. Typically, we should mention that r_o and R_o can be used to find the effective short-circuit transconductance (G_{m0}) of the emitter-degenerated CE amplifier as follows:

$$G_{m0} = -\frac{A_{vo}}{R_o}$$

Thus,

$$G_{m0} \approx -\frac{r_o}{g_m R_o} \quad (6.162)$$

which is identical to the expression we found for the discrete case in Section 5.2.

The high-frequency response of the CE amplifier with emitter degeneration can be found in a manner similar to that presented above for the CB amplifier.

In summary, including a relatively small resistance R_o (i.e., a small multiple of r_o) in the emitter of the active-loaded CE amplifier reduces its effective transconductance by the factor $(1 + g_m R_o)$ and increases its output resistance by the same factor, thus leaving the open-circuit voltage gain approximately unchanged. The input resistance R_{in} is increased by a factor $\beta + 1$, depends on R_o , and that is substantially lower than $(1 + g_m R_o)$. Also, including R_o reduces the severity of the Miller effect and correspondingly increases the amplifier bandwidth. Finally, an emitter-degenerate load resistance R_o removes the linearity of the amplifier.

EXERCISE

- E6.10.1 Consider the active-loaded CE amplifier with emitter degeneration shown in Fig. 6.4(b). Let $\beta = 100$, $r_o = 100$ mV, $R_o = 100$ k Ω , $R_L = 100$ k Ω , $V_{CC} = 10$ V, $V_{BE} = 0.7$ V, $I_C = 100$ mA, $R_s = 10$ k Ω , $R_g = 10$ k Ω , and $R_f = 100$ k Ω . Find the open-circuit voltage gain A_{vo} , the input resistance R_{in} , and the output resistance R_o .

6.10 THE SOURCE AND Emitter FOLLOWERS

The discrete-circuit source follower was presented in Section 4.7.5 and the discrete-circuit emitter follower in Section 5.7.6. In the following discussion we consider their IC versions, paying special attention to their high-frequency responses.

6.10.1 The Source Follower

Figure 6.50(a) shows an IC source follower biased by a constant-current source I , which is usually implemented using an NMOS current mirror. The source follower would generally be part of a larger circuit that determines the DC voltage at the transistor gate. We will encounter such circuits in the following chapters. Here we note that v_i is the input signal appearing at the gate and that R_L represents the combination of a load resistance and the output resistance of the current source I .

The low-frequency small-signal model of the source follower is shown in Fig. 6.50(b). Observe that v_i appears in parallel with R_o and that can be evaluated with it. Also, the controlled current-source $I_{ctrl}(v_o)$ feeds its current to the source terminal, where the voltage is $-v_o$. Thus we can use the source-absorption theorem (Appendix C) to replace the current source with a resistance $1/g_m$ between the source and ground. This can then be combined with R_o and r_o . With these two simplifications, the equivalent circuit takes the form shown in Fig. 6.50(c), where

$$R_o' = R_o + r_o \parallel \frac{1}{g_m} \quad (6.163)$$

We now can write for the output voltage v_o ,

$$v_o = g_m v_i R_o' \quad (6.164)$$

and for v_{pi} ,

$$v_{pi} = v_i - v_o \quad (6.165)$$

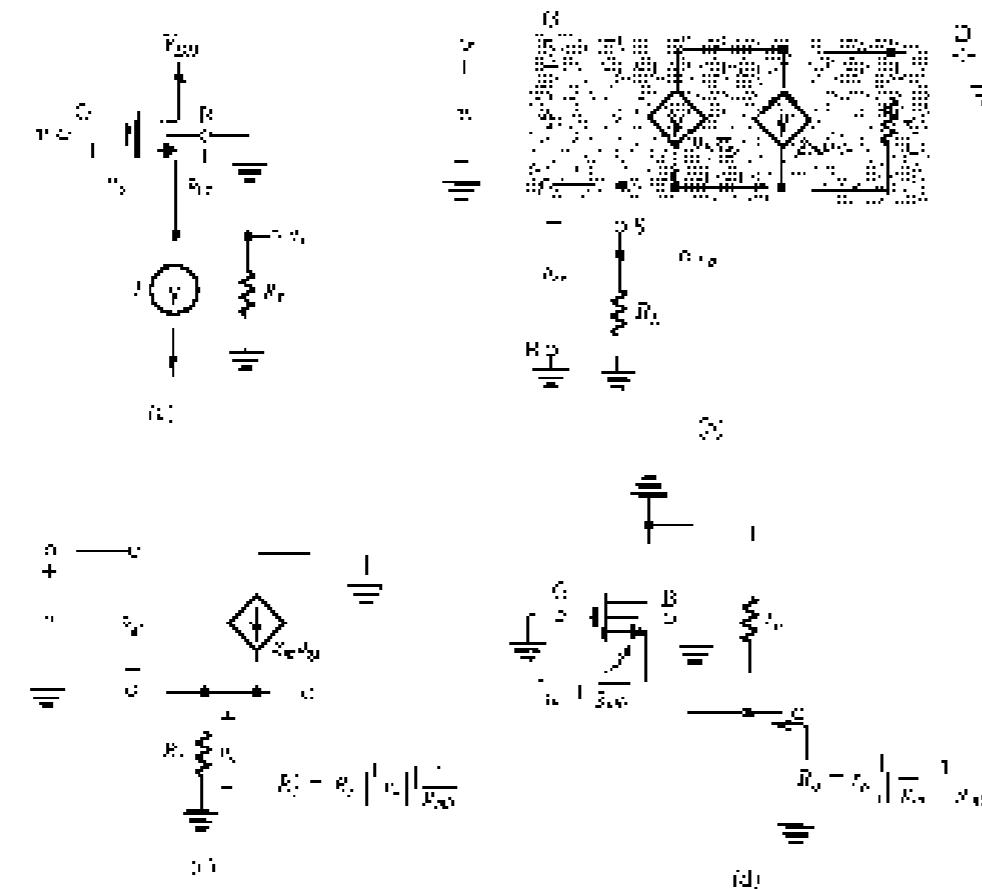


FIGURE 6.50 (a) MOS source follower. (b) Simplified equivalent circuit model of the source follower. (c) Simplified version of the frequency response. (d) Determining the output resistance of the source follower.

Equations (6.164) and (6.165) can be combined to obtain the voltage gain

$$A_v = \frac{V_o}{V_i} = \frac{g_m R'_o}{R'_o + 1/g_m R'_o} \quad (6.166)$$

which, as expected, is less than unity. To obtain the open-circuit voltage gain, we set R'_o in Eq. (6.166) to ∞ , which reduces R'_o to $r_{ds} + 1/g_m r_{ds}$. Substituting this value for R'_o in Eq. (6.166) gives

$$A_{ov} = \frac{g_m r_{ds}}{r_{ds} + g_m r_{ds}} = \frac{1}{1 + g_m} \quad (6.167)$$

which, for the ideal case where $(g_m r_{ds} + g_m^2 r_{ds}) r_{ds} \ll 1$, simplifies to

$$A_{ov} \approx \frac{g_m}{g_m + g_{mss}} = \frac{1}{1 + g_m} \quad (6.168)$$

Thus the highest value possible for the voltage gain of the source follower is limited to $1/(1 + g_m)$, which is typically 0.8 V/V to 0.9 V/V.

Finally, we can find the output resistance R_o of the source follower either using the equivalent circuit of Fig. 6.50(c) or by inspection of the circuit in Fig. 6.50(d) as

$$R_o = \frac{1}{g_m + g_{mss}} \quad (6.169)$$

which can be approximated as

$$R_o \approx 1/(1 + 2g_m) \quad (6.170)$$

Similar to the discrete source follower, the IC source follower can be used as the output stage of a low-voltage amplifier to provide a low output resistance for driving low-impedance loads. It is also used to shift the dc level of the signal by an amount equal to V_{th} .

EXERCISE

A discrete source follower with $V_{th} = -0.2$ V, $r_{ds} = 0.2$ k Ω , $g_m = 20$ mA/V, and $g_{mss} = 1$ mA/V is required to provide a small-signal gain of 0.9 V/V. What must the drain-to-gate bias be? Hint: Use the simplified model of Fig. 6.50(b).

6.10.2 Frequency Response of the Source Follower

A major advantage of the source follower is its excellent high-frequency response. This comes about because, as we shall now see, none of the internal capacitances suffers from the Miller effect. Figure 6.51(a) shows the high-frequency equivalent circuit of a source follower fed with a signal V_{in} from a source having a resistance R_s . In addition to the MOSFET capacitances C_{gs} and C_{gd} , a capacitance C_L is included between the output node and ground to account for the source-to-load capacitance C_{sl} , as well as any actual load capacitance.

The simplification performed above for the low-frequency equivalent circuit can be applied to the high-frequency model of Fig. 6.51(a) to obtain the equivalent circuit in Fig. 6.51(b), where R'_o is given by Eq. (6.163). Although one can derive an expression for the transfer function of this circuit, the resulting expression will be too complicated to yield insight regarding the role that each of the three capacitances plays. Rather, we shall first determine the location of the transmission zeros and then use the method of constant-time analysis to estimate the 3-dB frequency, f_{3dB} .

Although there are three capacitors in the circuit of Fig. 6.51(b), the transfer function is of the second order. This is because the three capacitors form a continuous loop. To determine the location of the two transmission zeros, refer to the circuit in Fig. 6.51(b) and note that V_o is zero at the frequency at which C_L has a zero impedance and thus acts as a short circuit across the output, which is open to ground. V_o will be zero at the value of s that causes the current into the impedance $R'_o + C_L$ to be zero. Since this current is $(g_m + g_{mss})V_{in}$, the transmission zero will be at $s = s_{T1}$, where

$$s_{T1} = -\frac{R'_o}{C_L} \quad (6.171)$$

Hence the zero will be on the negative real axis of the s -plane with a frequency

$$\omega_2 = \frac{R'_o}{C_L} \quad (6.172)$$

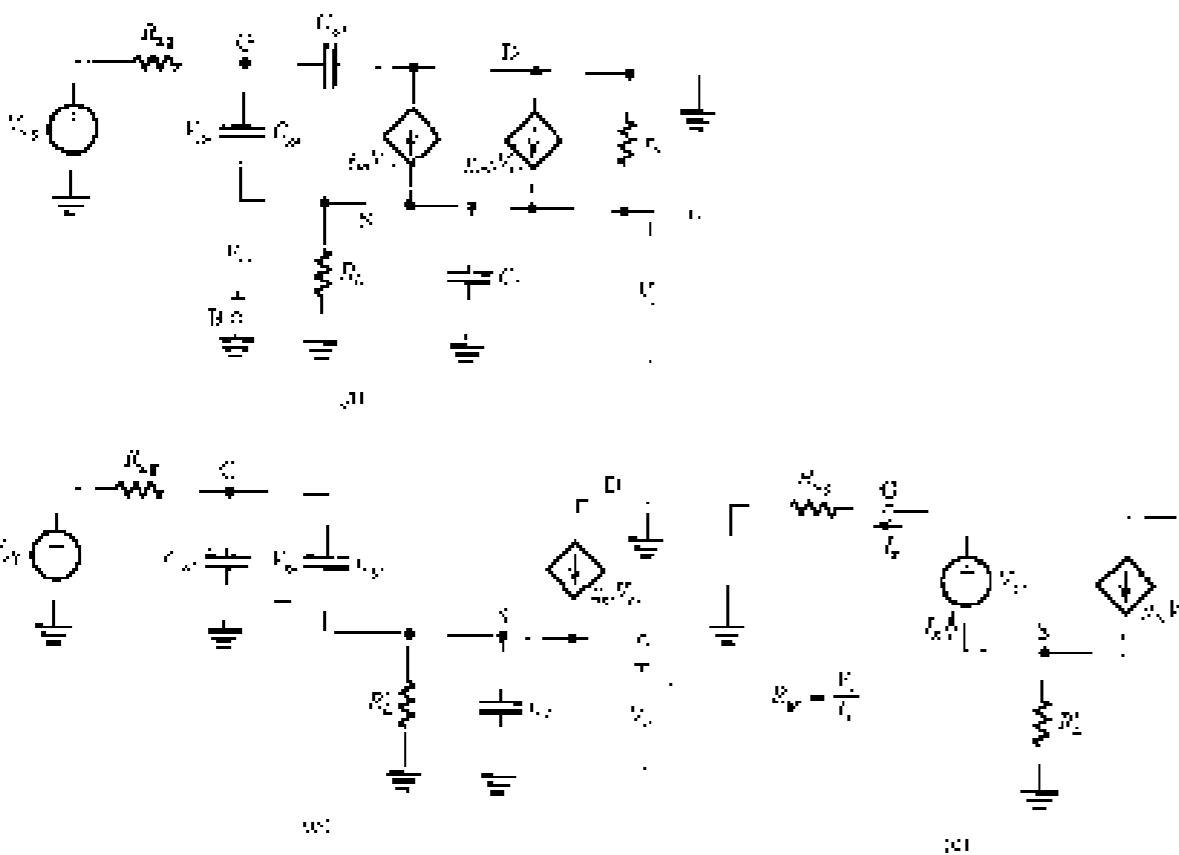


FIGURE 6.51 Analysis of the low-frequency response of the source follower in Fig. 6.50 by simplifying circuit (a) and (b) letting the resistance R_1 , R_2 , and R_3 to zero.

Recalling that the MOSFET's $\omega_T = g_m/(C_{gs} + C_{gd})$ and that $C_{gs} \ll C_{gd}$, we see that ω_2 will be very close to ω_T ,

$$\omega_2 \approx \omega_T. \quad (6.123)$$

Next, we turn our attention to the poles. Specifically, we will find the resistance seen by each of three capacitors C_{gs} , C_{gd} , and C_2 , and then compute the time constant associated with each. With V_{DS} set to zero and C_{gs} and C_2 assumed to be open circuited, we find by inspection that the resistance R_{eq} seen by C_{gd} is given by

$$R_{eq} = R_{ds}. \quad (6.124)$$

This is intuitively obvious: Because of the ground at the drain terminal, the input capacitance of the source follower, in the absence of C_{gs} and C_2 , is equal to C_{gd} . Thus, R_{eq} and C_{gd} form a high-frequency pole.

Next, we consider the effect of C_2 . The resistance R_{eq} seen by C_{gd} can be determined by straightforward analysis of the circuit in Fig. 6.51(c) to obtain

$$R_{eq} = \frac{R_{ds} + R_1}{1 + g_m R_1} \quad (6.125)$$

We note that the factor $(1 + g_m R_1)$ in the denominator will result in reducing the effective resistance with which C_2 interacts. In the absence of the two other capacitors, C_2 , together with R_{ds} , introduce a pole with frequency $1/2\pi C_2 R_{ds} = \omega_2$.

Finally, it is easy to see from the circuit in Fig. 6.51(b) that C_2 intersects with R_1 , R_3 that is,

$$R_{eq} = R_1 \parallel R_3$$

Usually, R_1 (Eq. 6.74b) is low. Thus, R_{eq} will be low, and the effect of C_2 will be small. Nevertheless, all three time constants can be added to obtain τ_0 and hence f_2 ,

$$f_2 = \frac{1}{2\pi\tau_0} = 1/2\pi(C_{gs}R_{ds} + C_{gd}R_{eq} + C_2R_{ds}). \quad (6.126)$$

EXERCISE

For the circuit in Fig. 6.51(a), calculate the value of R_1 if $V_{DS} = 2.2$ volt, $V_{GS} = 1.5$ volt, $I = 10$ microampere, $R_{ds} = 20$ kilohm, $R_2 = 10$ kilohm, $C_{gs} = 70$ pF, $C_{gd} = 15$ pF, and $C_2 = 15$ pF. Assume $R_3 = R_4 = 0$, and hence the time constants associated with the three capacitors C_{gs} , C_{gd} , and C_2 feed into and the appropriate weights to determine each of the three poles.

6.10.3 The Emitter Follower

Figure 6.52(a) shows an emitter follower suitable for IC fabrication. It is biased by a constant-current source I . However, the circuit that sets the dc voltage of the base is not shown. The emitter follower is fed with a signal V_{in} from a source with resistance R_{in} . The resistance R_{out} shown at the output, includes the output resistance of current source I as well as any load resistance.

Analysis of the emitter follower of Fig. 6.52(a) to determine its low-frequency gain, input resistance, and output resistance is identical to that performed on the capacitive-coupled version in Section 5.7.4. To load the terminals given in Table 5.6 can be easily adapted for the circuit in Fig. 6.52(a). Therefore we shall concentrate here on the analysis of the high-frequency response of the circuit.

Figure 6.52(b) shows the high-frequency equivalent circuit. Lumping r_e together with R_1 and r_s together with R_{in} and making a slight change in the way the circuit is drawn results in the simplified equivalent circuit shown in Fig. 6.52(c). We will follow a procedure for the analysis of this circuit similar to that used above for the source follower. Specifically, we obtain the location of the transmission zeros; note that V_o will be zero at the frequency f_2 for which the current fed to k'_1 is zero.

$$g_m V_{in} + \frac{V_o}{r_s} + k'_1 C_o = 0$$

Thus,

$$k'_1 = -\frac{R_1 + 1/g_m}{r_s} = -\frac{1}{C_o r_s}. \quad (6.127)$$

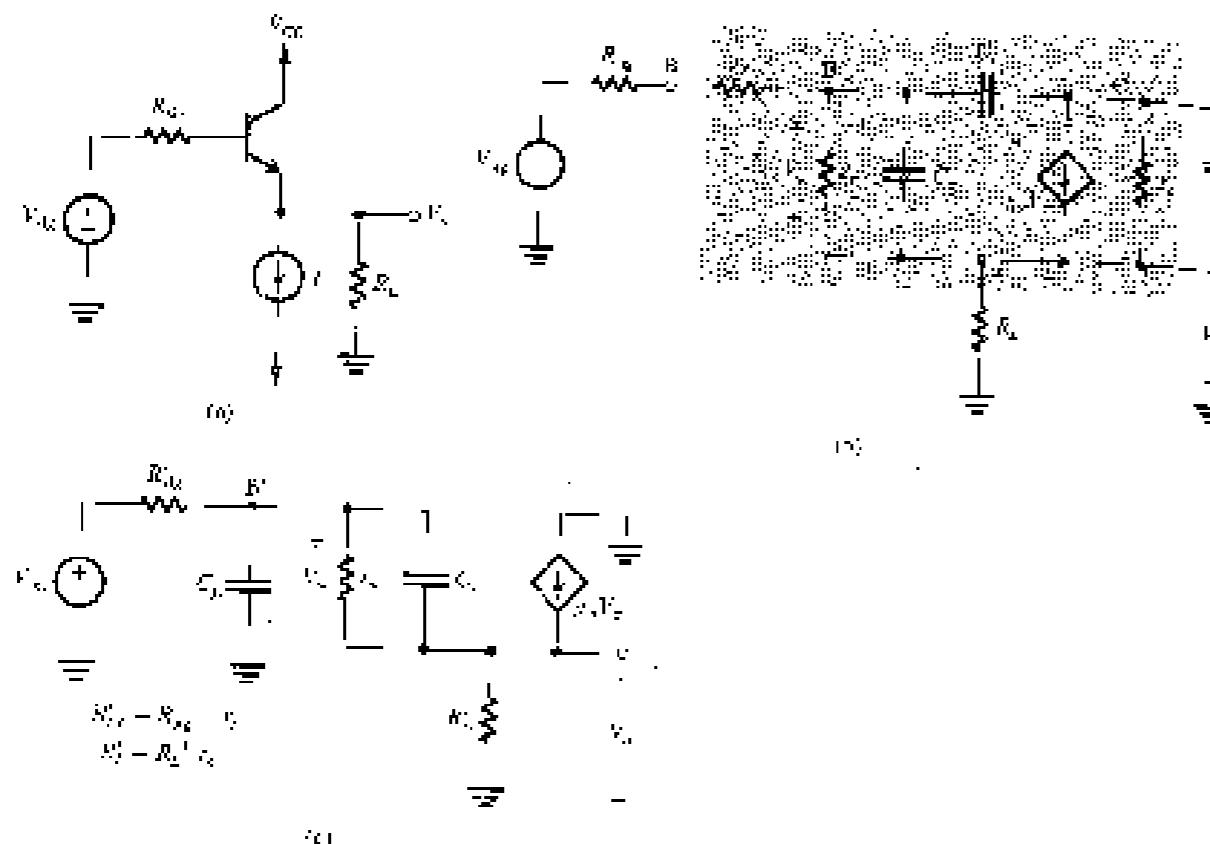


FIGURE 6.52 (a) Lower voltage, (b) High resistance equivalent circuit, (c) Simplified equivalent circuit which is on the negative real-axis of the s -plane, and (d) the step response.

$$\theta_j = \frac{1}{C_{ij}} \quad (6.173)$$

This frequency is very close to the unity-gain frequency, ω_0 , of the transistor. The other term, $\omega_{\text{low}} \omega_0$, is at $\gamma = \infty$. This is because at this frequency, C_0 acts as a short circuit, making V_C zero, and hence V_L will be zero.

Next, we determine the resistances seen by C_1 and C_2 . For C_1 , the reader should be able to show that the resistance it sees, R_{eq}^1 , is the parallel equivalent of R'_{out} and the input resistance looking into R_1^1 ; that is,

$$R_{\beta} = R_{\beta,0} \parallel \gamma_{\beta} = (\beta + 1) R_0] \quad (b=20)$$

Equation (6.19) indicates that θ_d will be smaller than R_{sp}^2 , and since C_p is usually very small, the time constant $C_p \theta_d$ will be correspondingly small.

The resistance R_2 seen by C_4 can be determined using an analysis similar to that employed for the determination of R_1 in the 1000EFT case. The result:

$$R_{\pi} = \frac{R'_{4\pi}}{1 + \frac{R'_{2\pi}}{R'_{4\pi}}} \quad (6.130)$$

We observe that the term R_1^2/C_{μ} will usually make the denominator much greater than unity, thus rendering S_1 rather low. Then, the time constant $C_{\mu} R_1$ will be small. The end result is that the A-dB frequency f_0 of the circuit follows:

$$f_0 = 1/(2\pi) [C_\mu S_\mu - C_\nu R_\nu] \quad (6.181)$$

will usually be very high. We urge the reader to solve the following exercise to gain familiarity with typical values of the various parameters that determine f_{in} .

22 ERGHS

- Fig. 35. Mean daily number of birds per m² and density (λ) for each frequency class ($\lambda = 100$). The width of each bar is 100 ha and the low-frequency class ($\lambda < 100$) includes all areas with less than 100 ha.

6.11 SOME USEFUL TRANSISTOR PAIRINGS

The cascode configuration studied in Section 6.8 combines CS and CG MOS transistors (CT) and CB bipolar transistors to great advantage. The key to the superior performance of the resulting combination is that the transistor pairing is done in a way that maximizes the advantages and minimizes the shortcomings of each of the two individual configurations. In this section we study a number of other such transistor pairings. In each case the transistor pair can be thought of as a compound device; thus the resulting amplifier may be considered as a single stage.

8.1.1 The CD-CS, CC-CE and CD-CE Configuration

Figure 6.55(a) shows an amplifier formed by cascading a common-emitter (source-follower) transistor Q_1 with a common-source transistor Q_2 . As should be expected, the voltage gain of this circuit will be $1/k$ times greater than that of the CS preamplifier. The advantage of this circuit

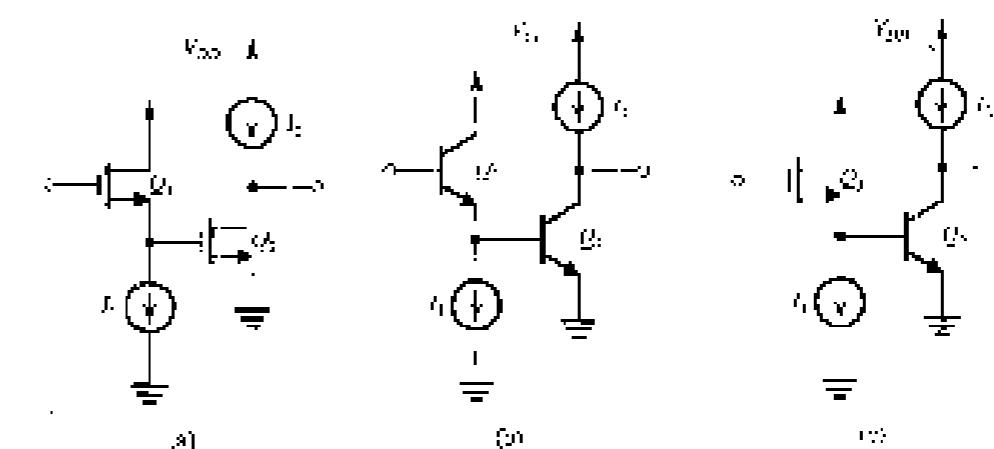


FIGURE 6.53 (a) CO2CS coupling; (b) CC CS coupling; (c) CO2CF coupling.

configuration, however, lies in its bandwidth, which is much wider than that obtained in a CS amplifier. To see how this comes about, note that the CS transistor (Q_2) will still exhibit a Miller effect that results in a large input capacitive, C_{i2} , between its gate and ground. However, the resistance that this capacitance interacts with will be much lower than R_{o2} . The buffering action of the source follower causes a relatively low resistance, approximately equal to $1/(f_{T2} \cdot 1.625)$, to appear between the source of Q_1 and ground across C_{i2} .

The bipolar counterpart of the CD-CS circuit is shown in Fig. 6.53(c). Beside achieving a wider bandwidth than that obtained with a CE amplifier, the CC-CE configuration has an important additional advantage: The input resistance is increased by a factor equal to $(\beta + 1)$. Finally, we show in Fig. 6.53(g) the BiCMOS version of this circuit type. Observe that Q_2 provides the amplifier with an infinite input resistance. Also, note that Q_2 provides the amplifier with a high r_{ce} , as ascribed to that obtained in the MOSFET circuit in Fig. 6.53(a) and hence high gain.

Example 6.13

Consider a CC-CE amplifier such as that in Fig. 6.53(b) with the following specifications: $f_T = f_{T2} = 1$ mA and identical transistors with $\beta = 100$, $f_T = 100$ MHz, and $C_J = 2$ pF. Let the amplifier be fed with a source V_{in} having a resistance $R_{in} = 2$ k Ω , and assume a load resistance of 4 k Ω . Find the voltage gain, A_V , and estimate the 3-dB frequency, f_T . Compare the results with those obtained with a CE amplifier operating under the same conditions. For simplicity, neglect r_o and r_s .

Solution

At an emitter bias current of 1 mA, Q_1 and Q_2 have

$$r_{ce} = 40 \text{ mV/V}$$

$$r_s = 25 \text{ M}\Omega$$

$$r_g = \frac{\beta}{f_T} = \frac{100}{100} = 2.5 \text{ k}\Omega$$

$$C_J = C_J = \frac{R_{in}}{r_{ce}} = \frac{2}{2.5 \times 10^{-3}} = 15.5 \text{ pF}$$

$$C_{i2} = 2 \text{ pF}$$

$$C_{o2} = 12.9 \text{ pF}$$

The voltage gain, A_V , can be determined from the circuit shown in Fig. 6.54(j) as follows:

$$R_{in} = r_{ce} = 2.5 \text{ k}\Omega$$

$$R_{in} = (\beta + 1)r_{ce} + R_{in}$$

$$= 100(0.025 + 2.5) = 255 \text{ k}\Omega$$

$$\frac{V_{o2}}{V_{in}} = \frac{R_{in}}{R_{in} + R_{o2}} = \frac{255}{255 + 4} = 0.98 \text{ V/V}$$

$$\frac{V_{o2}}{V_{in}} = \frac{R_{in}}{R_{in} + r_s} = \frac{2.5}{2.5 + 0.025} = 0.99 \text{ V/V}$$

$$\frac{V_{o2}}{V_{in}} = -r_{ce}R_{in} = -4 \times 0.98 = -160 \text{ V/V}$$

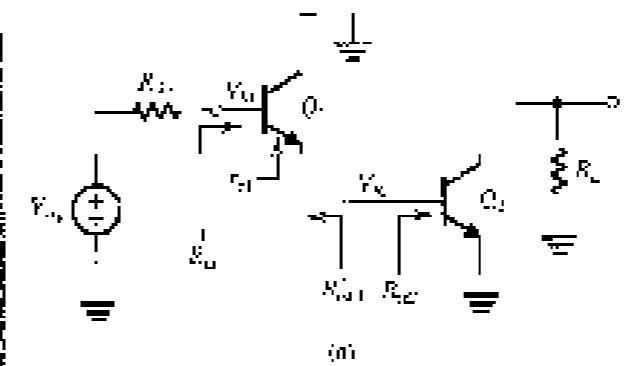
Thus,

$$A_{V2} = \frac{V_{o2}}{V_{in}} = -160 \times 0.98 \times 0.98 = -155 \text{ V/V}$$

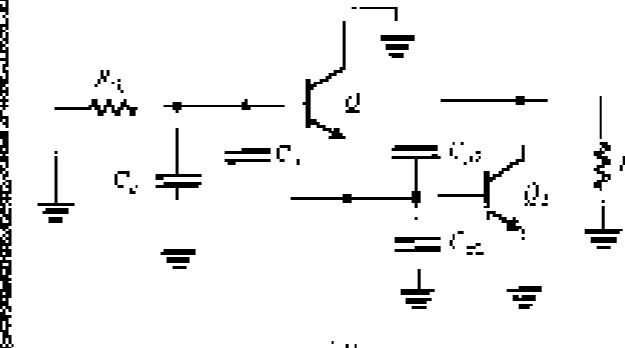
To determine f_T , we use the method of open-circuit time constants. Figure 6.54(i) shows the circuit with V_{in} set to zero and the AC voltages indicated. Capacitor C_{in} sees a resistance R_{in} :

$$R_{in} = R_{in} + R_{o2}$$

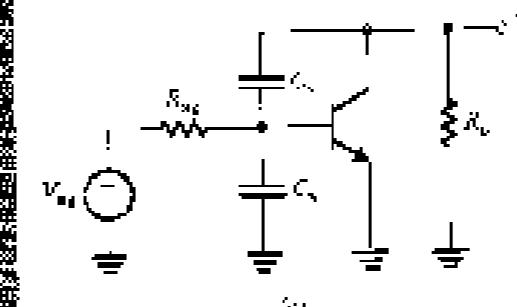
$$= 4 \parallel 255 = 3.61 \text{ k}\Omega$$



(a)



(b)



(c)

FIGURE 6.54 Circuits for Example 6.13: (a) The CC-CE circuit prepared for low-frequency small-signal analysis; (b) the circuit at high frequencies, with V_{in} set to zero, to determine of the open-circuit time constant; and (c) a CE amplifier for comparison.

To find the resistance R_{in} seen by capacitance C_{in} , we refer to the analysis of the high-frequency response of the emitter follower in Section 6.10.3. Specifically, we adapt Eq. (6.180) to the situation here as follows:

$$\begin{aligned} R_{\text{in}} &= \frac{R_{\text{in}} + R_{\text{in},\text{C}}}{1 + \frac{R_{\text{in}} + R_{\text{in},\text{C}}}{r_{\text{in}}} \cdot \frac{1}{f_{\text{c}}} \\ &= \frac{4000 + 2500}{1 + \frac{4000 + 2500}{2500} \cdot \frac{1}{25}} = 65.4 \text{ M} \end{aligned}$$

Capacitance C_{in} seen at collector is $R_{\text{in},\text{C}}$:

$$\begin{aligned} R_{\text{in},\text{C}} &= R_{\text{in}} + R_{\text{in},\text{C}} \\ &\approx r_{\text{in}} \left[1 + \frac{R_{\text{in}}}{\beta_1 + 1} \right] \\ &= 2500 \left[1 + \frac{4000}{101} \right] = 62 \text{ M} \end{aligned}$$

Capacitance C_{in} seen a resistor $R_{\text{in},\text{C}}$. To determine $R_{\text{in},\text{C}}$ we refer to the analysis of the high-frequency response of the CT amplifier in Section 6.9 to obtain

$$\begin{aligned} R_{\text{in},\text{C}} &= (1 + g_{\text{m},1} R_{\text{in}})(R_{\text{in},\text{C}} + R_{\text{in},\text{C},\text{C}}) + R_{\text{in},\text{C}} \\ &= (1 + 10 \times 4) 2500 \left(25 + \frac{4000}{101} \right) + 4000 \\ &= 14,143 \text{ }\Omega = 14.1 \text{ k}\Omega \end{aligned}$$

We now can determine r_{in} from

$$\begin{aligned} r_{\text{in}} &= C_{\text{in}} R_{\text{in}} + C_{\text{in}} R_{\text{in},\text{C}} + C_{\text{in}} R_{\text{in},\text{C},\text{C}} + C_{\text{in}} R_{\text{in},\text{C},\text{C}} \\ &\approx 2 \times 9.6 \times 15.0 \times 0.0534 + 2 \times 14.1 = 15.9 + 0.063 \\ &= 15.9 + 0.06 + 25.2 + 0.88 = 57.9 \text{ m}\Omega \end{aligned}$$

We observe that C_{in} and $C_{\text{in},\text{C}}$ play a very important role in determining the high-frequency response. As expected, C_{in} through the Miller effect plays the most significant role. Note, $C_{\text{in},\text{C}}$, which interacts directly with $(R_{\text{in},\text{C}} + R_{\text{in},\text{C},\text{C}})$, also plays an important role. The 3-dB frequency f_3 can be found as follows:

$$f_3 = \frac{1}{2\pi r_{\text{in}}} = \frac{1}{2\pi \times 17.9 \times 10^{-3}} = 4.2 \text{ MHz}$$

For comparison, we calculate r_{in} and r_{in} of a CT amplifier operating under the same conditions, refer to Fig. 6.54(a). The voltage gain A_{v} is given by

$$\begin{aligned} A_{\text{v}} &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{in},\text{C}}} \cdot g_{\text{m},1} R_{\text{in}} \\ &= \frac{1}{1 + R_{\text{in}}/R_{\text{in},\text{C}}} (g_{\text{m},1} R_{\text{in}}) \\ &= \frac{(1 - 0.5)}{(1.25 + 0.5)} (-10 \times 4) \\ &= -61.5 \text{ V/V} \end{aligned}$$

$$R_2 = r_{\text{in}} | R_{\text{in},\text{C}} = 2.5 | = -1.54 \text{ k}\Omega$$

$$\begin{aligned} R_3 &= (1 + g_{\text{m},1} R_{\text{in}})(R_{\text{in},\text{C}} + R_{\text{in},\text{C},\text{C}}) + R_{\text{in},\text{C}} \\ &= (1 + 10 \times 4)(1 + 1.25) + 4 \\ &= 251.7 \text{ k}\Omega \end{aligned}$$

Thus,

$$\begin{aligned} Z_{\text{in}} &= C_{\text{in}} R_{\text{in}} + C_{\text{in}} R_{\text{in},\text{C}} \\ &\approx 12.9 \times 1.54 + 12 \times 251.7 \\ &= 21.4 + 503.4 = 524.8 \text{ n}\Omega \end{aligned}$$

Observe the dominant role played by C_{in} . The 3-dB frequency f_3 is

$$f_3 = \frac{1}{2\pi r_{\text{in}}} = \frac{1}{2\pi \times 524.8 \times 10^{-3}} = 100 \text{ MHz}$$

Thus, including the buffering transistor Q_1 increases the gain, A_{v} , from 61.5 V/V to 155 V/V—a factor of 2.6—and increases the bandwidth from 203 kHz to 100 MHz—a factor of 149. The gain-bandwidth product is increased from 15.63 MHz to 631 MHz—a factor of 41.5.

6.11.2 The Darlington Configuration

Figure 6.55(a) shows a popular BJT circuit known as the **Darlington configuration**. It can be thought of as a variation of the OC-CE circuit with the collector of Q_1 connected to that of Q_2 . Alternatively, the Darlington pair can be thought of as a composite transistor with $\beta = \beta_1 \beta_2$. It can therefore be used to implement a high-performance voltage follower, as illustrated in Fig. 6.55(b). Note that in this application the circuit can be considered in the cascade connection of two common-collector transistors (that is, CC-CC configuration).

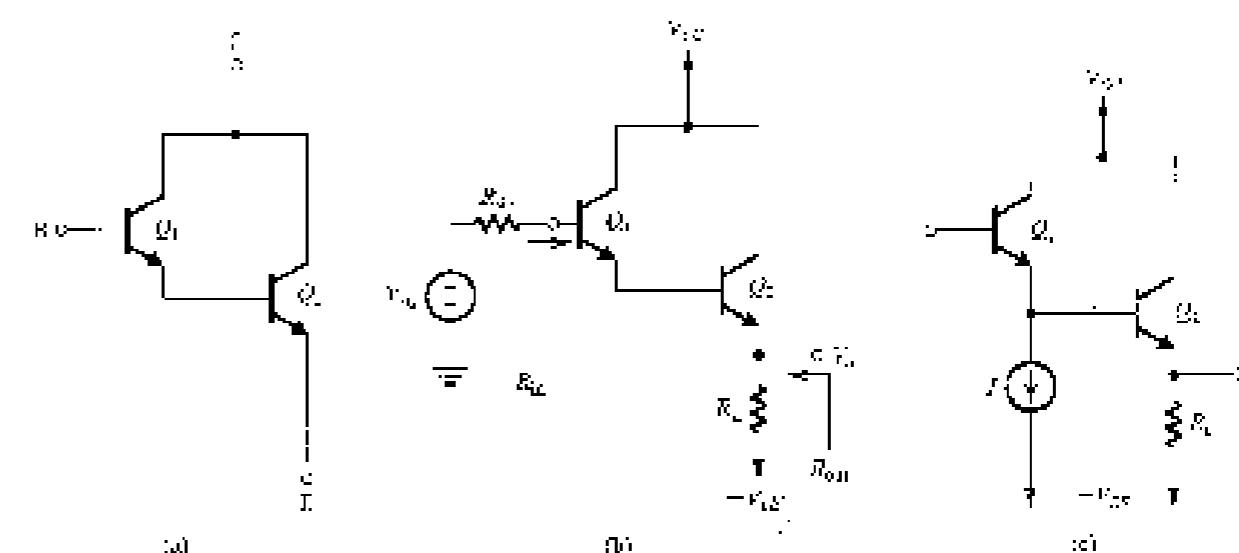
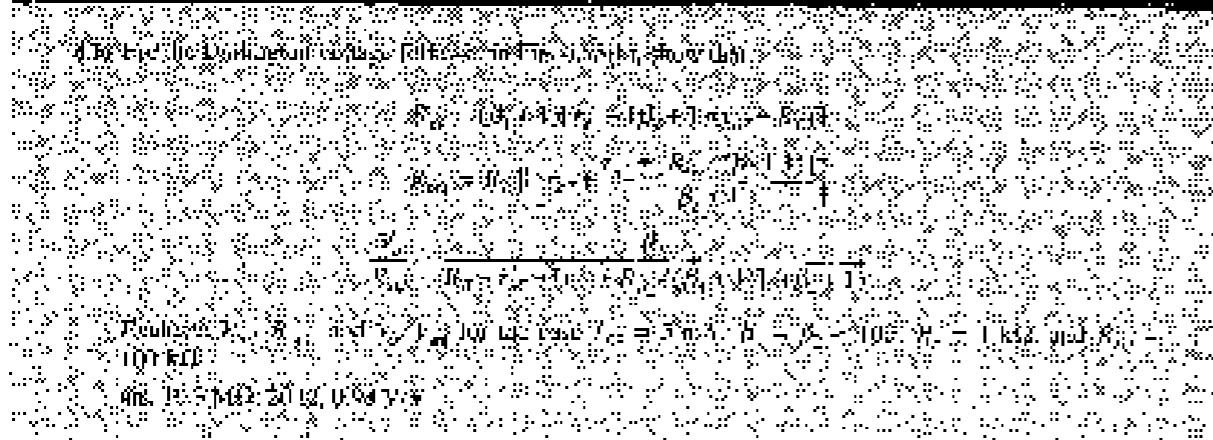


FIGURE 6.55 (a) The Darlington is equivalent to a voltage follower using the Darlington configuration; and (c) a Darlington follower with a low-current demand for Q_1 , assuming that its β is not high.

Since the transistor β depends on the dc bias current I , it is possible that Q_1 will be operating at a very low β , rendering the β -multiplication effect of the Darlington pair rather ineffective. A simple solution to this problem is to provide a bias current for Q_1 , as shown in Fig. 6.55(c).

EXERCISE.



6.11.3 The CC-CB and CD-CG Configurations

Considering an emitter follower with a common-base amplifier, as shown in Fig. 6.56(a), results in a circuit with a low-frequency gain approximation equal to that of the CB but with the problem of the low input resistance of the CB caused by the buffering action of the CC stage. Since neither the CC nor the CB amplifier suffers from the Miller effect, the CC-CB

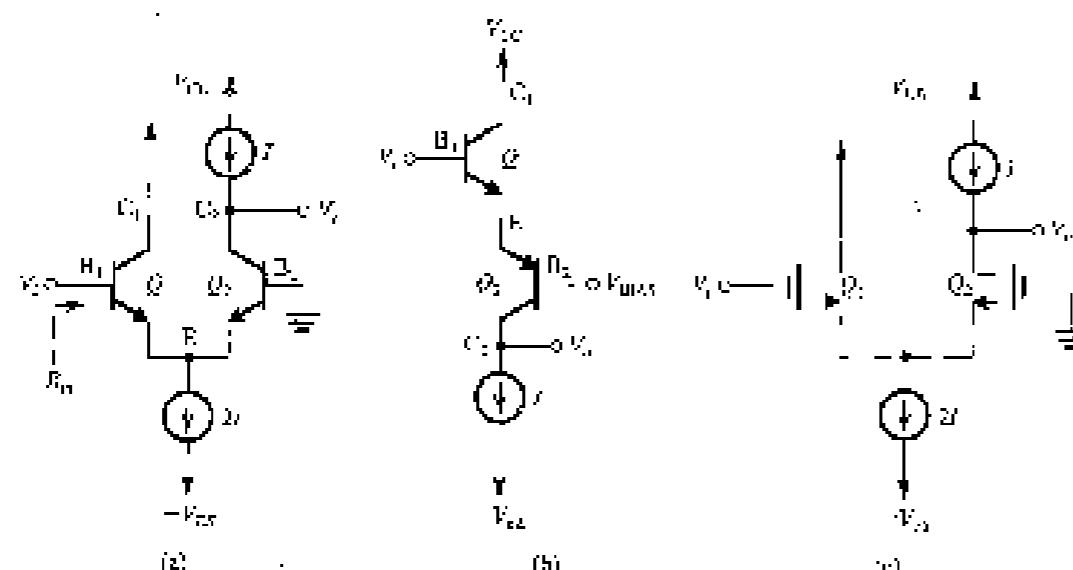


FIGURE 6.56 (a) A CC-CB amplifier. (b) An AC analysis of the CC-CB circuit with Q₁ implemented using a pnp transistor. (c) The VDMOSFET version of the circuit in (a).

configuration has excellent high-frequency performance. Note that the biasing current sources shown in Fig. 6.56(a) ensure that each of Q_1 and Q_2 is operating at a bias current I . We are not showing, however, how the dc voltage at the base of Q_1 is set or the circuit that determines the dc voltage at the collector of Q_2 . Both issues are usually looked after in the larger circuit of which the CC-CB amplifier is part.

An interesting version of the CC-CB configuration is shown in Fig. 6.56(b). Here the CB stage is implemented with a pnp transistor. Although only one current source is now needed, observe that we also need to establish an appropriate voltage at the base of Q_2 . This circuit is part of the internal circuit of the popular 741 op amp, which will be studied in Chapter 9.

The MOSFET version of the circuit in Fig. 6.56(a) is the CD-CG amplifier shown in Fig. 6.56(c).

We now briefly analyze the circuit in Fig. 6.56(a) to determine its gain A_{vA} and its high-frequency response. The analysis applies directly to the circuit in Fig. 6.56(b) and, with appropriate change of component and parameter names, to the NMOSFET version in Fig. 6.56(c). For simplicity we shall neglect r_o and r_s of both transistors. The input resistance R_{in} is given by

$$R_{in} = (\beta_1 + 1)(r_{in} + r_{ds}) \quad (6.182)$$

which for $r_{in} = r_{ds} = r$ and $\beta_1 + \beta_2 = \beta$ becomes

$$R_{in} = 2r \quad (6.183)$$

If a load resistance R_L is connected at the output, the voltage gain V_o/V_i will be

$$\frac{V_o}{V_i} = \frac{\beta_2 R_L}{r_{in} + r_{ds}} = \frac{1}{2} \beta_2 R_L \quad (6.184)$$

Now, if the amplifier is fed with a voltage signal V_{in} from a source with a resistance R_{in} , the overall voltage gain will be

$$\frac{V_o}{V_{in}} = \frac{1}{2} \frac{\beta_2}{R_{in} + R_{in}} R_{in} = \frac{1}{2} \beta_2 R_{in} \quad (6.185)$$

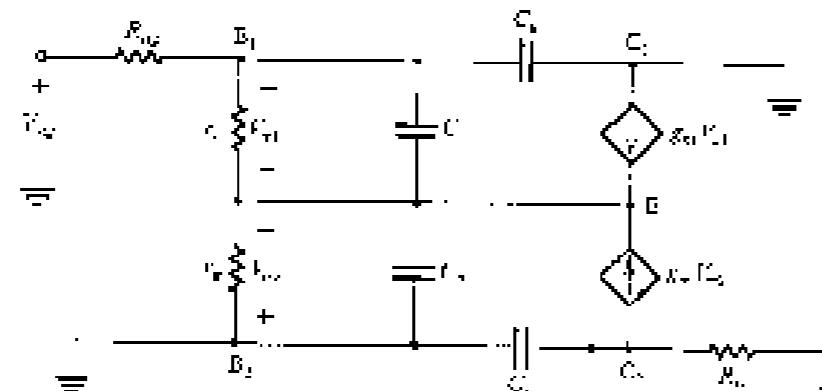
The high-frequency analysis is illustrated in Fig. 6.57(a). Here we have drawn the $1/\omega$ - π equivalent circuit for each of Q_1 and Q_2 . Recalling that the two transistors are operating at equal bias currents, their corresponding model components will be equal (i.e., $r_{in} = r_{ds}$, $C_{in} = C_{ds}$, etc.). With this in mind the reader should be able to see that $V_{in} = V_{in}$ and the horizontal line running through the node labeled B in Fig. 6.57(a) can be deleted. Thus the circuit reduces to that in Fig. 6.57(b). This is a very attractive outcome because the circuit shows clearly the two poles that determine the high-frequency response: the pole at the input, with a frequency f_{p1} , is

$$f_{p1} = \frac{1}{2\pi \left(\frac{C_{in}}{2} + C_{ds} \right) (R_{in} \parallel 2r_{in})} \quad (6.186)$$

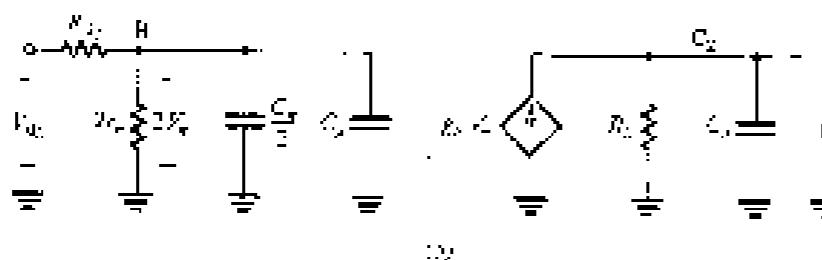
and the pole at the output, with a frequency f_{p2} , is

$$f_{p2} = \frac{1}{2\pi C_{ds} R_L} \quad (6.187)$$

This result is also intuitively obvious: The input impedance at B_1 of the circuit in Fig. 6.57(a) consists of the series connection of r_{in} and r_{ds} in parallel with the series connection of C_{in} and C_{ds} . Then there is C_{ds} in parallel. At the output, we simply have R_L in parallel with C_{ds} .



(a)



(b)

FIGURE 6.57. (a) Equivalent circuit for the amplifier in Fig. 6.63. (b) Simplified equivalent circuit. Note that the equivalent circuits in (a) and (b) also apply to the circuit shown in Fig. 6.63(d). In addition, they can be easily adapted for h-*MOSFET* circuits in Fig. 6.56(d), with 2*n*-channel *MOSFET*s replaced with *p*-channel *MOSFET*s and V_{Tn} replaced with V_{Tp} .

Whether one of the two poles is dominant will depend on the relative values of R_{z1} and R_{z2} . If the two poles are close to each other, then the 3-dB frequency f_3 can be determined either by exact analysis—that is, finding the frequency at which the gain is down by 3 dB—or by using the approximate formula in Eq. (6.16).

$$f_3 = \sqrt{\frac{1}{R_{z1}^2 + R_{z2}^2}} \quad (6.180)$$

Finally, we note that the circuits in Fig. 6.57(a) and (b) are special forms of the differential amplifier, perhaps the most important circuit building block in analog IC design and the major topic of study in Chapter 7.

Example 6.2

Design a single-stage current-mirror circuit with a current ratio of 10. The output resistance is to be $100\text{ k}\Omega$. The input resistance is to be $10\text{ M}\Omega$. The input voltage is to be 1 mV , and the output voltage is to be 10 mV . The circuit is to be implemented in a *MOSFET* technology with $k_n = 10\text{ mA/V}^2$, $k_p = 2\text{ mA/V}^2$, and $V_{Tn} = V_{Tp} = 1\text{ V}$.

6.12 CURRENT-MIRROR CIRCUITS WITH IMPROVED PERFORMANCE

As we have seen throughout this chapter, current sources play a major role in the design of *IC* amplifiers. The constant-current source is used both in biasing and as a load. Simple forms of both *MOSFET* and bipolar current sources and, more generally, current mirrors were studied in Section 6.3. The need to improve the characteristics of the source sources and mirrors has already been demonstrated; specifically, two performance parameters need to be addressed: the accuracy of the current transfer ratio of the mirror and the output resistance of the current source.

The reader will recall from Section 6.3 that the accuracy of the current transfer ratio suffers particularly from the finite *B* of the BJT. The output resistance, as given in the simple circuit, is limited to $1/\beta$ of the *MOSFET* and the BJT, also reduces accuracy and, much more severely, severely limits the gain available from cascode amplifiers. In this section we study *MOS* and bipolar cascode mirrors with more accurate current transfer ratios and higher output resistances.

6.12.1 Cascode MOS Mirrors

A brief introduction to the use of the cascading principle in the design of current sources was presented in Section 6.8.4. Figure 6.58 shows the basic cascode current mirror. Observe that in addition to the diode-connected transistor Q_1 , which forms the basic mirror β_1 , Q_2 , another diode-connected transistor, Q_3 , is used to provide a suitable bias voltage for the gate of the cascode transistor Q_4 . To determine the output resistance of the cascode mirror at the drain of Q_3 , we set I_{DS2} to zero. Also, since Q_1 and Q_3 have a relatively small drain-to-source resistance (each of approximately $1/k_n$), the drain-to-gate voltages across them will be small, and we can assume that the gates of Q_3 and Q_4 are both grounded. Thus the output resistance R_o will be that of the CG transistor Q_4 , which has a resistance r_{ds4} in series. Equation (6.19) can be adapted to obtain

$$R_o = r_{ds4} = 1/(g_{m2} - g_{m3}/(r_{ds3}))r_{ds3} \quad (6.190)$$

As shown in Fig. 6.58, the cascode effect raises the output resistance of the current source by the factor g_{m3}/g_{m2} , which is the intrinsic gain of the cascode transistor.

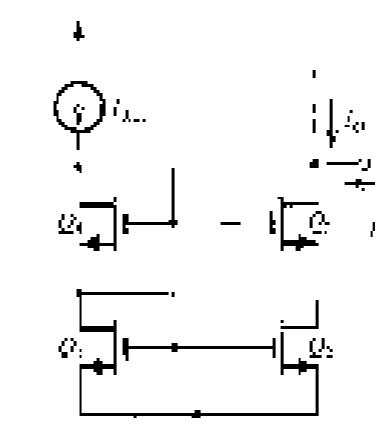


FIGURE 6.58 A cascode *MOS* current mirror.

A disadvantage of the cascode current mirror is that it consumes a relatively large portion of the standby biasing supply voltage V_{DD} . While the simple MOS mirror operates properly with a voltage as low as V_{DD} across its output transistor, the cascode circuit of Fig. 6.58 requires a minimum voltage of $V_{DD} + 2V_{DS}$. This is because the gate of Q_2 is at $2V_{DS} = 2V_{DD}$. Thus the minimum voltage required across the output of the cascode mirror is 1 V (as is). This severely limits the signal swing at the output of the mirror (i.e., at the output of the amplifier that differs this current source as a load). In Chapter 9 we shall study a wide-swing cascode mirror.

EXERCISE

6.58 For a cascode NMOS current mirror design with $V_{DD} = 0.5$ V and $\beta = 10^4$, $r_o = 10^6$ Ω , $V_{DS} = 0.1$ V, $I_{DD} = 10 \mu A$, the minimum output voltage required for no clipping is

6.12.2 A Bipolar Mirror with Base-Current Compensation

Figure 6.59 shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of the simple current mirror. The reduced dependence on β is achieved by including transistor Q_3 , the emitter of which supplies the base currents of Q_1 and Q_2 . The sum of the base currents is then provided by $(\beta_1 + 1)$, resulting in a much smaller error current that has to be supplied by Q_{BIP} . Detailed analysis is shown on the circuit diagram; it is based on the assumption that Q_1 and Q_2 are matched and have equal collector currents, I_C . A node equation at the node labeled v gives

$$I_{BIP} = I_C \left[1 + \frac{2}{\beta(\beta - 1)} \right]$$

Since

$$I_B = I_C$$

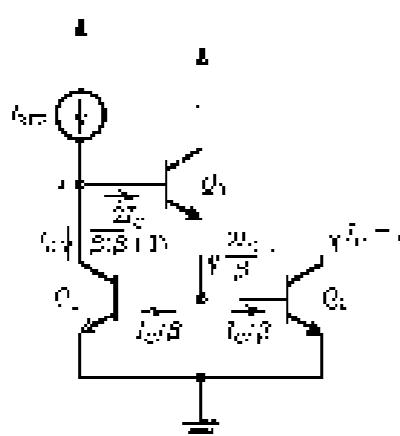


FIGURE 6.59 A current mirror with base-current compensation.

The current transfer ratio of the mirror will be

$$\begin{aligned} \frac{I_O}{I_{BIP}} &= \frac{1}{1 + 2/\beta^2(\beta + 1)} \\ &\approx \frac{1}{1 + 2/\beta^2} \end{aligned} \quad (6.191)$$

which means that the error due to finite β has been reduced from $2/\beta$ in the simple mirror to $2/\beta^2$,... tremendous improvement! Unfortunately, however, the output resistance remains approximately equal to that of the simple mirror, namely r_o . Finally, note that if a reference current I_{REF} is not available, we simply connect node v to the power supply V_{DD} through a resistance R . The result is a reference current given by

$$I_{REF} = \frac{V_{DD} - V_{BE1} - V_{BE2}}{R} \quad (6.192)$$

6.12.3 The Wilson Current Mirror

A simple but ingenious modification of the basic bipolar mirror results in both reducing the β dependence and increasing the output resistance. The resulting circuit, known as the Wilson mirror after its inventor, George Wilson, an IC design engineer working for Tektronix, is shown in Fig. 6.60(a). The analysis to determine the effect of finite β on the current transfer

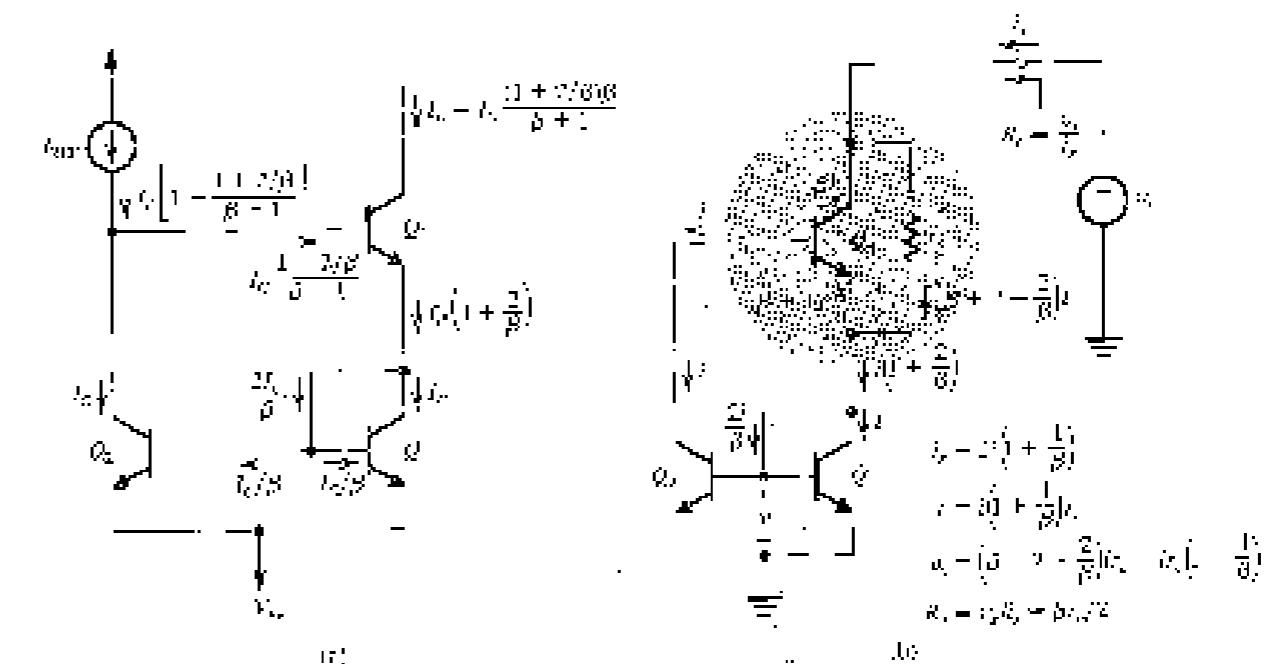


FIGURE 6.60 The Wilson bipolar current mirror: (a) circuit; (b) circuit analysis to determine (b) current transfer ratio and (c) determining the output resistance. Note that the current I_o that enters Q_4 must equal the sum of the currents that leave it. 27

ratio is shown in Fig. 6.60(a), from which we can write

$$\begin{aligned} \frac{i_c}{i_{\text{out}}} &= \frac{i_c \left(1 + \frac{\beta}{\beta+1}\right) (\beta+1)}{i_c \left[1 + \left(\frac{\beta}{\beta+1}\right)^2 / (\beta+1)\right]} \\ &= \frac{\beta+2}{\beta+1 + \frac{\beta^2}{\beta}} = \frac{\beta+2}{\beta+1 + \frac{2}{\beta}} \\ &= \frac{1}{1 - \frac{2}{\beta(\beta+2)}} \\ &\approx \frac{1}{1 + 2/\beta^2} \end{aligned} \quad (6.193)$$

This analysis assumes that Q_1 and Q_2 conduct equal collector currents. There is, however, a slight inaccuracy with this assumption: The collector-to-emitter voltages of Q_1 and Q_2 are not equal, which introduces a current offset or a systematic error. This problem can be solved by adding a diode-connected transistor in series with the collector of Q_2 , as we shall shortly show for the MOS version.

Analysis to determine the output resistance of the Wilson mirror is illustrated in Fig. 6.61(b), from which we see that

$$R_o = \beta r_{\pi}/2 \quad (6.194)$$

Finally, we note that the Wilson mirror is preferred over the cascade mirror because the latter has the same dependence on β as the single mirror. However, like the cascade mirror, the Wilson mirror requires an additional V_{BE} drop for its operation; that is, for proper operation we must allow for 1 V or so across the Wilson mirror output.

EXERCISE 6.12

1. Derive the expression for the output resistance of the Wilson mirror.
2. Derive the expression for the output resistance of the Wilson mirror if the two transistors have different β values.
3. Derive the expression for the output resistance of the Wilson mirror if the two transistors have different V_{BE} drops.
4. Derive the expression for the output resistance of the Wilson mirror if the two transistors have different r_{π} values.

6.12.4 The Wilson MOS Mirror

Figure 6.61(a) shows the MOS version of the Wilson mirror. Obviously there is no β to reduce here, and the advantage of the MOS Wilson lies in its enhanced output resistance. The analysis shown in Fig. 6.61(b) provides

$$R_o = \frac{1}{2} \left(\frac{r_{\pi} \beta (\beta+2)}{\beta+1} \right) = \frac{1}{2} \beta r_{\pi} \beta^2$$

where we have neglected, for simplicity, the body effect in Q_1 . We observe that the output resistance is approximately the same as that achieved in the cascade mirror. Finally, to balance

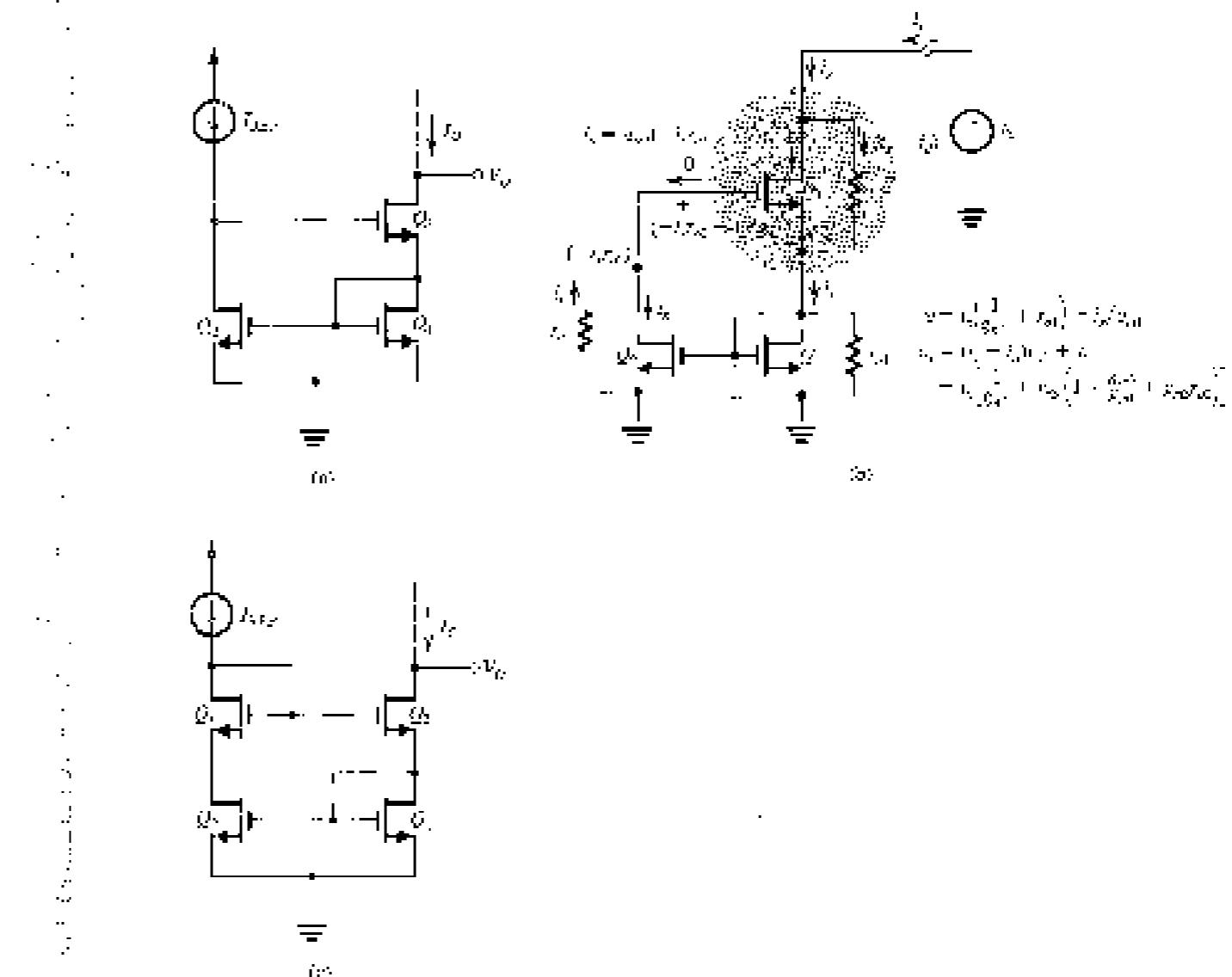


FIGURE 6.61 The Wilson MOS mirror. (a) Circuit; (b) analysis to determine output resistance; and (c) modified circuit.

the two branches of the mirror and thus avoid the systematic current error resulting from the difference in V_{BE} between Q_1 and Q_2 , the circuit can be modified as shown in Fig. 6.61(c).

6.12.5 The Widlar Current Source

A final current-source circuit, known as the Widlar current source, is shown in Fig. 6.62. It differs from the basic current driver circuit in an important way: A resistor R_E is included in the emitter lead of Q_2 . Neglecting base currents we can write

$$I_{\text{dc}} = V_{\text{BE}} \ln \left(\frac{I_{\text{REF}}}{I_b} \right) \quad (6.195)$$

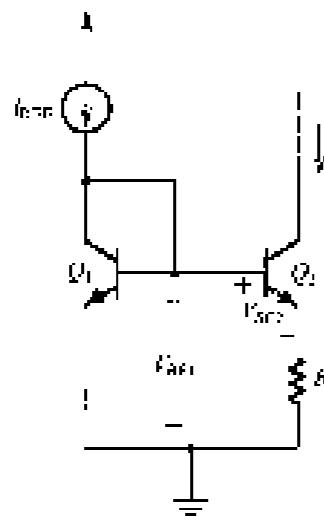


FIGURE 6.62 The Widlar current source.

and

$$V_{BE1} = V_{T\ln}\left(\frac{I_{BIPOLAR}}{I_0}\right) \quad (6.196)$$

where we have assumed that Q_1 and Q_2 are matched correctly. Combining Eqs. (6.195) and (6.196) gives

$$V_{BE1} = V_{BE2} = V_T \ln\left(\frac{I_{BIPOLAR}}{I_0}\right) \quad (6.197)$$

But from the circuit we see that

$$V_{BE1} = V_{BE2} + I_E R_E \quad (6.198)$$

Thus,

$$I_E R_E = V_T \ln\left(\frac{I_{BIPOLAR}}{I_0}\right) \quad (6.199)$$

The design and advantages of the Widlar current source are illustrated in the following example.

Example 6.6 Figure 6.63 shows two circuits for generating a constant current $I_0 = 10 \mu\text{A}$ which comes from a 10-V supply. Determine the values of the required resistors assuming that V_T is 0.7 V at a current of 1 mA and neglecting the effect of finite β .

Solution

For the basic current source circuit in Fig. 6.63(a) we choose a value for R_1 to result in $I_{BIPOLAR} = 10 \mu\text{A}$. At this current, the voltage drop across Q_1 will be

$$V_{BE1} = 0.7 - V_T \ln\left(\frac{10 \mu\text{A}}{1 \mu\text{A}}\right) = 0.54 \text{ V}$$

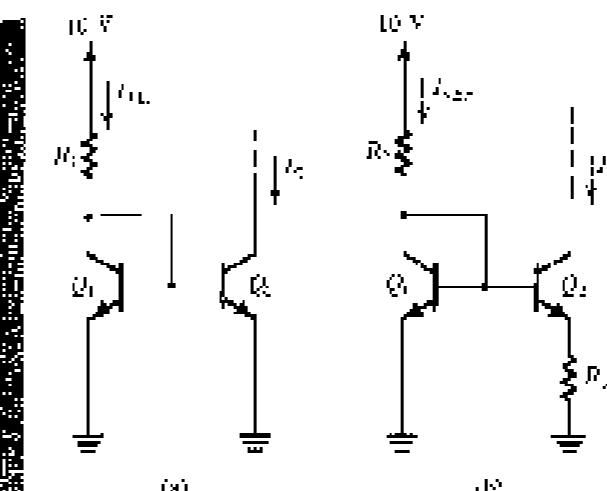


FIGURE 6.63 Circuits for Example 6.12.

Thus,

$$R_1 = \frac{10 - 0.54}{0.001} = 942 \text{ k}\Omega$$

For the Widlar current source of Fig. 6.63(b) we must first decide on a suitable value for $I_{BIPOLAR}$. If we select $I_{BIPOLAR} = 2 \mu\text{A}$, then $V_{BE1} = 0.7 \text{ V}$ and R_1 is given by

$$R_1 = \frac{10 - 0.7}{0.002} = 9.3 \text{ k}\Omega$$

The value of R_2 can be determined using Eq. (6.199) as follows:

$$10 \times 10^{-6} R_2 = 0.025 \ln\left(\frac{1 \mu\text{A}}{10 \mu\text{A}}\right)$$

$$R_2 = 11.5 \text{ k}\Omega$$

From the above example we observe that using the Widlar circuit allows the generation of a much constant current using relatively small resistors. This is an important advantage that results in considerable savings in chip area. In fact the circuit of Fig. 6.63(a), requiring a 942-k Ω resistance, is totally impractical for implementation in IC form.

Another important characteristic of the Widlar current source is that its output resistance, r_o , is high. The increase in the output resistance, above that achieved in the basic current source, is due to the emitter degeneration resistance r_E . To determine the output resistance of Q_2 , we assume that since the base of Q_2 is connected to ground via the small resistance r_E of Q_1 , the input-referred voltage at the base will be small. Thus we can use the formula derived in Section 6.7.2 for the CB amplifier, namely Eq. (6.118), and adapt it for our purposes here as follows:

$$r_o = (1 + \beta_{12}) R_E \parallel r_{e2}(V_o) \quad (6.200)$$

Thus the output resistance is increased above r_E by a factor that can be significant.

EXERCISE

- 6.40 Find the output resistance of each of the two current sources designed in Example 6.4. Let $V_{DD} = 5\text{ V}$ and $\beta = 10^4/\text{V}^2$.
ANSWER 1.24 M Ω .

6.13 SPICE SIMULATION EXAMPLES

We conclude this chapter by presenting two SPICE simulation examples. In the first example, we will use SPICE to investigate the operation of the CS amplifier circuit (studied in Section 6.5.2). In the second example, we will use SPICE to compare the high-frequency response of the CN amplifier (studied in Section 6.6) to that of the folded-cascode amplifier (studied in Section 6.8.6).

EXAMPLE 6.15**THE CMOS CS AMPLIFIER**

In this example, we will use PSpice to compute the dc transfer characteristic of the CS amplifier whose Capture schematic is shown in Fig. 6.61. We will assume a 5- μm CMOS technology for the MOSFETs and use parts NMOS5P0 and PMOS5P0 whose SPICE-level i -parameters are listed in Table 4.8. To specify the dimensions of the MOSFETs in PSpice, we will use the multipligate factor m together with the channel length L and the channel width W . The MOSFET parameter m ,

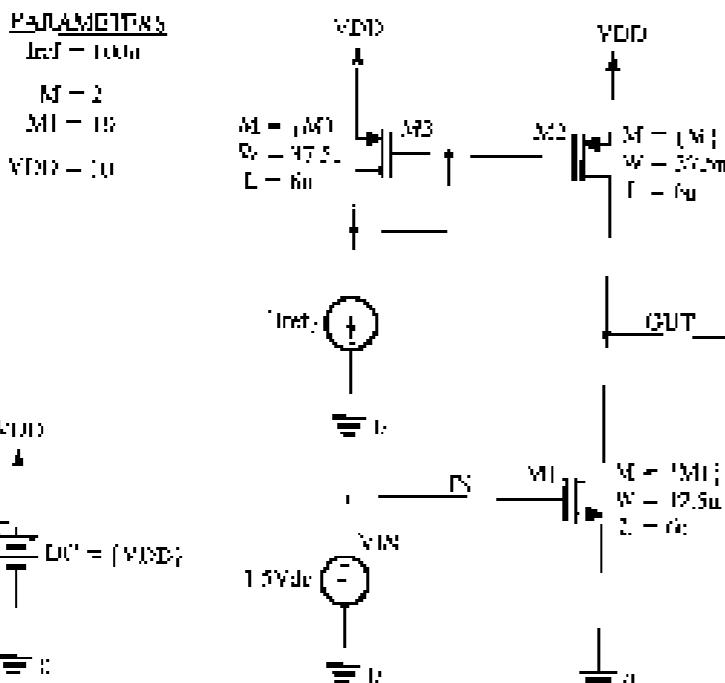


FIGURE 6.61 Capture schematic of the CS amplifier (Example 6.15).

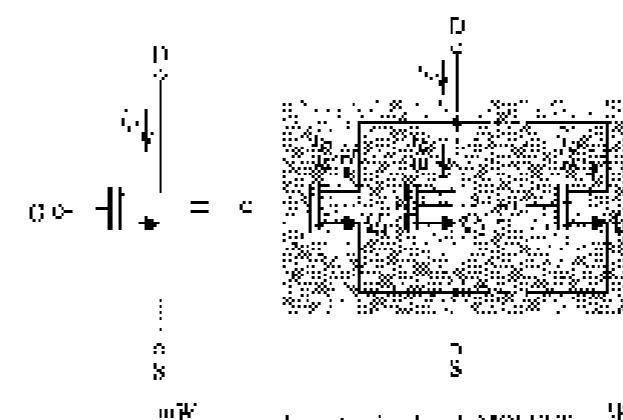


FIGURE 6.65 Transfer equivalence.

whose default value is 1, is used in SPICE to specify the number of MOSFETs connected in parallel. As depicted in Fig. 6.65, a wide transistor with channel length L and channel width $w \times W$ can be implemented using m transistors in parallel, each having a channel length l and a channel width W . Thus, neglecting the channel-length modulation effect, the drain current of a MOSFET operating in the saturation region can be expressed as

$$I_D = \frac{m}{2} \mu C_{ox} \rho \frac{W}{L} V_{DS}^2 \quad (6.201)$$

where C_{ox} rather than C_s is used to more accurately estimate the drain current (refer to Section 4.1.2.2).

The CS amplifier in Fig. 6.61 is designed for a bias current of 100 μA , assuming a drain current $I_D = 100 \mu\text{A}$ and $V_{DD} = 5\text{ V}$. The current-mirror transistors M_2 and M_4 are sized for $V_{DS2} = V_{DS4} = 1\text{ V}$, while the input transistor M_1 is sized for $V_{DS1} = 0.5\text{ V}$. Note that a smaller overdrive voltage is selected for M_1 to achieve a larger voltage gain G_v for the CS amplifier, since

$$G_v = g_m R'_v = g_m (r_{ds1} + r_{ds2}) = \frac{1}{V_{DS1}} \left(\frac{V_{A1} V_{A2}}{V_{DS1} + V_{A1}} \right) \quad (6.202)$$

where V_{A1} and V_{A2} are the magnitudes of the early voltages of, respectively, the NMOS and PMOS transistors. Unit ϕ_{eq} transistors are used with $W/L = 12.5 \mu\text{m}/6 \mu\text{m}$ for the NMOS devices and $W/L = 37.5 \mu\text{m}/6 \mu\text{m}$ for the PMOS devices. Thus, using Eq. (6.201) together with the 5- μm CMOS process parameters in Table 4.8, we find $m_1 = 10$ and $m_2 = m_4 = 2$ (rounded to the nearest integer). Furthermore, Eq. (6.202) gives $G_v = 40\text{ V/V}$.

To compute the dc transfer characteristic of the CS amplifier, we perform a dc analysis in PSpice with V_{IN} swept over the range 0 to V_{DD} and plot the corresponding output voltage V_{GOUT} . Figure 6.66(a) shows the resulting transfer characteristic. The slope of this characteristic (i.e., dV_{GOUT}/dV_{IN}) corresponds to the gain of the amplifier. The high-gain segment is clearly visible for V_{IN} around 1.5 V. This corresponds to an overdrive voltage for M_1 of $V_{DS1} = V_{IN} - V_{A1} = 0.5\text{ V}$, as desired. To examine the high-gain region more closely, we repeat the dc sweep for V_{IN} between 1.5 V and 1.7 V. The resulting transfer characteristic is plotted in Fig. 6.66(b) (middle curve). Using the Probe graphical interface of PSpice, we find that the linear region of this dc transfer characteristic is bounded approximately by $V_{IN} = 1.465\text{ V}$ and $V_{IN} = 1.549\text{ V}$. The corresponding values of V_{DS1} are 3.838 V and 3.739 V. These results are close to the expected values. Specifically, transistors M_1 and M_2 will remain in the saturation region, and, hence, the amplifier will operate in its linear region if $V_{DS1} \leq V_{DS1} \leq V_{DS1} = V_{DS2} = 0.5\text{ V} \leq V_{DS1} \leq 1.5\text{ V}$. From the results above,

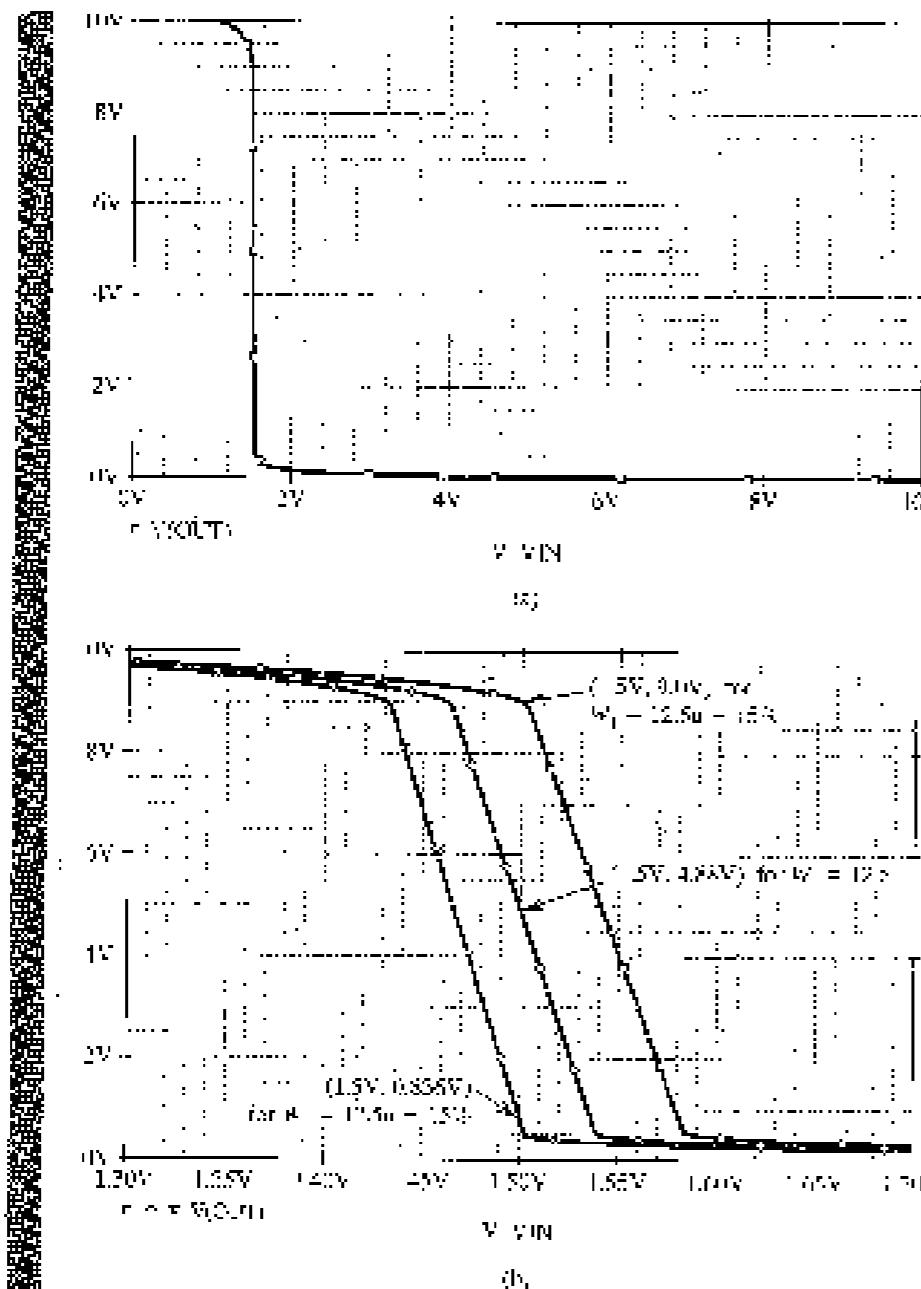


FIGURE 6.66 (a) Transfer characteristics of the CS amplifier in Example 6.15. (b) Expanded view of the transfer characteristic in the high-gain region. All three curves for different process realizations cause the width of transistor M_1 to change by $\pm 25\%$ and its original value of $W = 12.5 \mu\text{m}$.

The voltage $g_{\text{m}} \propto V_{\text{G}}$ (i.e., the slope of the linear segment of the dc transfer characteristic) is approximately -1.2 mV/V , which is reasonably close to the value obtain by hand analysis.

Note, from the dc transfer characteristic in Fig. 6.66(b), that for an input dc bias of $V_{\text{IN}} = 1.5 \text{ V}$, the output dc bias is $V_{\text{OBIAS}} = 0.88 \text{ V}$. This choice of V_{G} maximizes the available signal swing in the output by setting V_{OBIAS} at the middle of the linear segment of the dc transfer characteristic.

However, because of the high resistance of the output node (or, equivalently, because of the high voltage gain), this value of V_{OBIAS} is highly sensitive to the effect of process and temperature variations on the characteristics of the transistors. To illustrate this point, consider what happens when the width of M_1 (i.e., W_1 , which is normally $12.5 \mu\text{m}$) changes by $\pm 25\%$. The curves regarding the transfer characteristics are shown in Fig. 6.66(b). Accordingly, when $V_{\text{IN}} = 1.5 \text{ V}$, V_{O} will drop to 0.84 V if W_1 increases by 15% and will rise to 0.92 V if W_1 decreases by 15%. In practical circuit implementations, this problem is circumvented by using negative feedback to normalize all the dc bias voltage at the output of the amplifier and, hence, to reduce the sensitivity of the circuit to process variations. The topic of negative feedback will be studied in Chapter 8.

FREQUENCY RESPONSE OF THE CS AND THE FOLDED-GASCODE AMPLIFIERS

In this example, we will use PSpice to compute the frequency response of both the CS and the folded-gascode amplifiers whose Capture schematics are given in Figs. 6.67 and 6.69, respectively. We will assume that the dc bias levels at the output of the amplifiers are stabilized using negative feedback. However, before performing a small-signal analysis (or, more precisely, simulation) in SPICE to measure the frequency response, we will perform dc analysis (a 3000-point simulation) to verify that all MOSFETs are operating in the saturation region and, hence, ensure that the amplifiers are operating in its linear region.

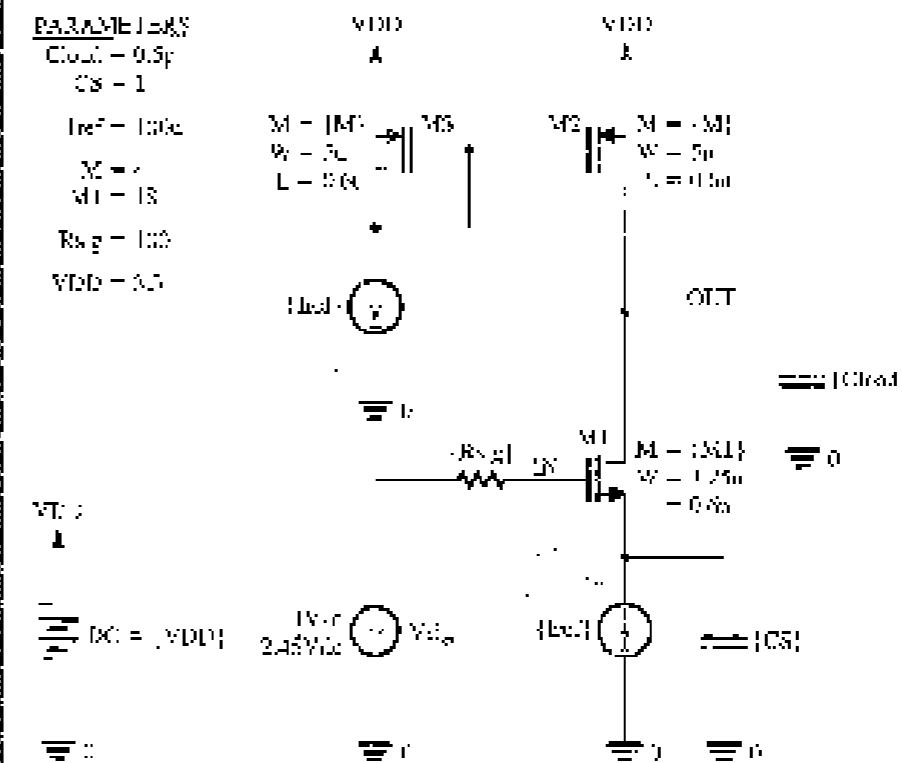


FIGURE 6.67 Capture schematic of the CS amplifier in Example 6.16.

In the following, we will assume a 0.5 μm CMOS technology for the NMOSFETs and two pairs NMOSFET and PMOSFET whose SPICE-level model parameters are listed in Table 4.5. To specify the dimensions of the MOSTFs in PSPice, we will use the *ltx* and *lx* parameters together with the channel length *L* and channel width *W* (as we did in Example 6.15).

THE CS AMPLIFIER

The CS amplifier circuit in Fig. 6.67 is identical to the one shown in Fig. 6.10, except that a current source is connected to the source of the input transistor M_1 to set its drain current I_D independently of its drain voltage V_{DS} . Furthermore, in our PSPice simulations we keep an intentionally large bypass capacitor C_2 of 1 F . This sets the source of M_1 at a sufficiently high ground during the ac-analysis simulation. Accordingly, the CS amplifier circuits in Figs. 6.13 and 6.67 are equivalent for the purpose of frequency-domain analysis. In Chapter 7, we will find out in the context of *c*, *short-circuit* the differential pair. Low-frequency biasing approach for the CS amplifier are discussed in practical IC implementations.

The CS amplifier in Fig. 6.67 is designed assuming a reference current $I_{D0} = 100 \mu\text{A}$ and $V_{DD} = 3.3 \text{ V}$. The current mirror transistors, M_2 and M_3 , are sized for $V_{DS2} = V_{DS3} = 0.3 \text{ V}$, while the input transistor M_1 is sized for $V_{DS1} = 0.5 \text{ V}$. Unit-size transistors are used with $W_{M1} = 1.25 \text{ nm} \times 0.6 \mu\text{m}$ for the NMOS devices and $W_{M2} = 5 \text{ nm} \times 0.6 \mu\text{m}$ for the PMOS devices. Thus, using Eq. (8.22) together with the 0.5- μm CMOS process parameters in Table 4.3, we find $\omega_1 = 18$ and $\omega_2 = \omega_3 = 4$. Furthermore, Eq. (6.202) gives $G_0 = -3.4 \text{ V/V}$ for the CS amplifier.

In the PSPice calculations of the CS amplifier in Fig. 6.67, the V_{GS} bias voltage of the signal source is set such that the voltage at the source terminal of M_1 is $V_{GS} = 1.3 \text{ V}$. This requires the dc level of V_{DS} to be $V_{DS1} = V_{GS} - V_{DD} = 2.45 \text{ V}$ because $V_{DS1} = 1 \text{ V}$ is a result of the body effect on M_1 . The reasoning behind this choice of V_{GS} is that, in a practical circuit implementation, the current source that feeds the source of M_1 is most probably a current-controlled current source, such as the one in Fig. 6.58. In this case, the minimum of the expected voltage across the current source (i.e., the minimum V_{GS}) is $V_{GS} + 2V_{DS} = 3.3 \text{ V}$, assuming $V_{GS} = 0.3 \text{ V}$ for the current mirror transistors.

A biasing verification is performed in PSPice to verify that all MOSFETs are biased in the saturation region. Next, to compute the frequency response of the amplifier, we set the dc voltage of the signal source to 1 V , perform an ac-analysis simulation, and plot the output voltage magnitude versus frequency. Figure 6.68(a) shows the resulting frequency response for $R_{L1} = 0 \Omega$ and $R_{L2} = 1 \text{ M}\Omega$. In both cases, a load capacitor of $C_{L1,2} = 0.5 \text{ pF}$ is used. The corresponding values of the 3-dB frequency f_0 of the amplifier are given in Table 6.4.

Observe from Fig. 6.68 when R_{L2} is increased. This is anticipated from our study of the high-frequency response of the CS amplifier in Section 6.6. Specifically, as R_{L2} increases, the pole

$$f_0 = \frac{1}{2\pi R_{L2} C_{L2}} \quad (6.203)$$

located at the amplifier input will have an increasingly significant effect on the overall frequency response of the amplifier. As a result, the effective time constant τ_R in Eq. (6.57) increases and f_0 decreases. When R_{L2} becomes very large, as it is when $R_{L2} = 1 \text{ M}\Omega$, a dominant pole is formed by R_{L2} and C_{L2} . This results in

$$f_0 = f_{L2,C} \quad (6.204)$$

To estimate $f_{L2,C}$, we need to calculate the input capacitance C_{in} of the amplifier. Using Miller's theorem, we have

$$\begin{aligned} C_{in} &= C_{DS1} + C_{DS2}(1 + g_m R_L^*) \\ &= (g_m R_L^*) C_{DS1} + C_{DS2} + (C_{DS1} + C_{DS2}) (1 + g_m R_L^*) \end{aligned} \quad (6.205)$$

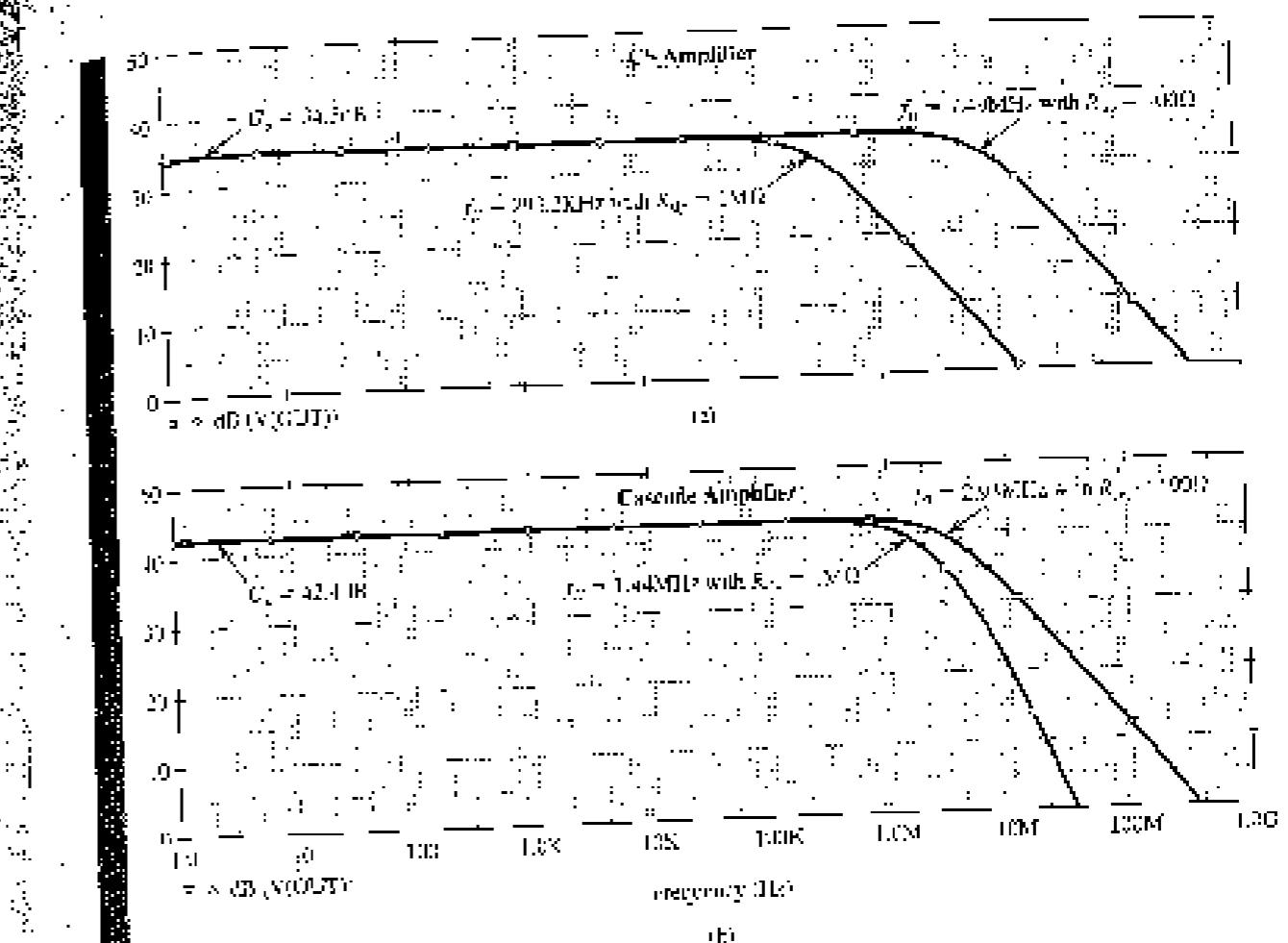


FIGURE 6.68 Frequency response of (a) the CS amplifier and (b) the folded-cascode amplifier in Example 6.16, with $R_{L1} = 100 \Omega$ and $R_{L2} = 1 \text{ M}\Omega$.

TABLE 6.4 Dependence of the 3-dB frequency f_0 on the load of the FCA

R_{L2}	CS Amplifier	Folded-Cascode Amplifier
100 Ω	-7.40 MHz	2.02 MHz
∞	-3.42 MHz	1.14 $\times f_0$
1000 Ω	-	-

$$R_L^* = r_o || R_L \quad (6.206)$$

Thus, C_{in} can be calculated using the values of C_{DS1} and C_{DS2} , which are computed by PSPice and can be found in the output file of the bias-point simulation. Alternatively, C_{in} can be found using Eq. (6.205) with the values of the on-chip capacitances C_{DS1} and C_{DS2} calculated using the

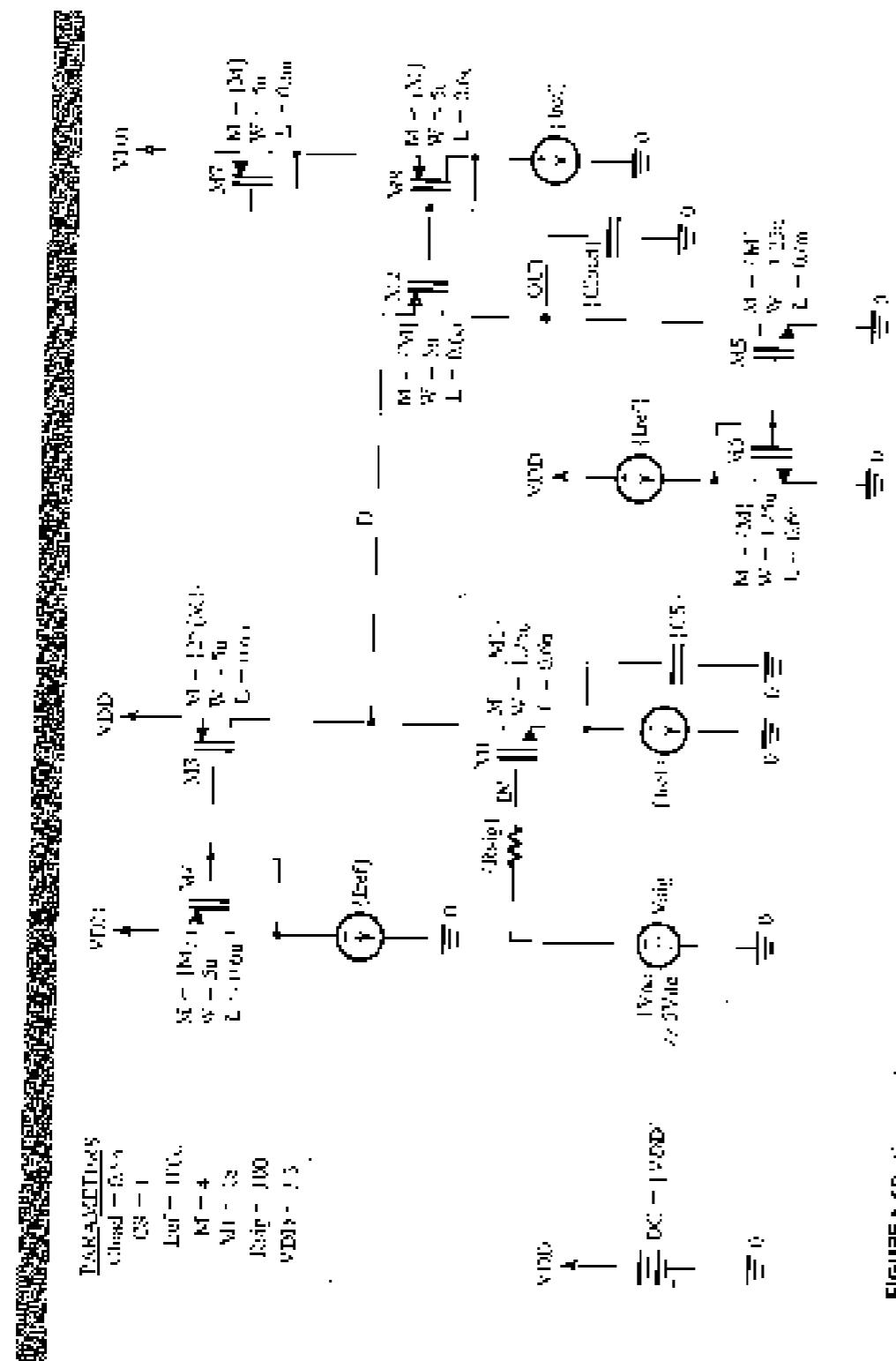


FIGURE 6.69 Circuit diagram of the folded cascode amplifier in Fig. 6.19.



device parameters in Table 6.8 (as described in Eqs. 4.170 and 4.171), that is,

$$C_{N_{M1}} = \mu_C W_1 C_{ox} S_1 \quad (6.207)$$

$$C_{N_{M2}} = \mu_C W_2 C_{ox} S_2 \quad (6.208)$$

This results in $C_N = 0.53$ pF when $|G_D| = \sqrt{S_L} = 53.3$ V/V. Accordingly, using Eqs. 6.206 and 6.208, $f_T = 300.3$ MHz, where $R_{DS} = 1$ M Ω , which is close to the value computed by PSPice.

THE FOLDED-CASCODE AMPLIFIER

The folded-cascode amplifier circuit in Fig. 6.69 is equivalent to the one in Fig. 6.45, except that a current source is placed in the source of the input transistor M_1 for the same dc biasing purpose as in the case of the CS amplifier. Note that in Fig. 6.69, the PMOS current mirror M_6-M_7 and the NMOS current mirror M_2-M_3 are used to obtain large negative current sources i_1 and i_2 in the circuit of Fig. 6.45. Furthermore, the current transfer ratio of mirror M_2-M_3 is set to 2, i.e., $i_2 = i_1/2$. This results in $I_{DS2} = 2I_{DS1}$. Hence, transistor M_2 is biased at $i_{DS2} = I_{DS1} = I_A$. The gate bias voltage of transistor M_3 is generated using the diode-connected transistors M_4 and M_5 . The saturation drain currents of these transistors are set equal to those of transistor M_2 . Therefore, ignoring the body effect,

$$V_{DS2} = V_{DS1} - V_{DS3} = V_{DS1} - 2(V_{DS1} - V_{DS2}) \quad (6.209)$$

where V_{DS2} is the drain-to-source voltage of the PMOS transistors in the input PMOS circuit. These two circuits have the same drain-to-source voltage because their I_{DS}/m is the same. Then, such a biasing configuration results in $V_{DS2} = (V_{DS1} + V_{DS3})$ as desired, while setting $V_{DS1} = (V_{DS1} + V_{DS2})/2$ to achieve the bias matching between M_2 and M_3 .

The folded-cascode amplifier in Fig. 6.69 is designed assuming a reference current $I_A = 50$ μ A and $V_{DD} = 6.0$ V (as in the case of the CS amplifier). All transistors are sized for an operating voltage of 0.3 V, except for the input transistor M_1 , which is sized for $V_{GS1} = 0.25$ V. Thus, using Eq. 6.130, all the MOSFETs in the amplifier circuit are designed using $m = 1$, except for $m_1 = 16$.

The midband voltage gain of the folded-cascode amplifier in Fig. 6.69 can be expressed using Eq. 6.130 as

$$G_v = g_{m1} R_{DS2} \quad (6.210)$$

where

$$R_{DS2} = R_{DS1} \parallel R_{DS3} \quad (6.211)$$

is the output resistance of the amplifier. Here, R_{DS1} is the resistance seen looking into the drain of the source-transistor M_1 , while R_{DS3} is the resistance seen looking into the drain of the cascode-mirror transistor M_3 . Using Eq. 6.127, we have

$$R_{DS2} = (g_{m1} r_{DS1}) R_{DS3} \quad (6.212)$$

where

$$R_{DS} = r_{DS} \parallel r_{DS} \quad (6.213)$$

is the effective resistance of the source of M_1 . Furthermore

$$\Delta R_{DS} = r_{DS} \quad (6.214)$$

Hence for the folded-cascode amplifier in Fig. 6.69,

$$R_{DS2} = r_{DS} \quad (6.215)$$

END

$$C_{\text{in}} = R_{\text{in}} C_{\text{os}} = \frac{R_{\text{in}}}{V_{\text{DD}}} \quad (6.215)$$

Using the 0.5-μm CMOS parameters, this gives $R_{\text{in}} = 100 \text{ k}\Omega$ and $V_{\text{DD}} = +5 \text{ V/V}$. Therefore, R_{in} , and, hence, C_{in} of the folded-cascade amp (Fig. 6.68) are larger than those of the CS amplifier in Fig. 6.67 by a factor of 3.

Figure 6.68(b) shows the frequency response of the folded-cascade amplifier at a supply voltage of the cases $V_{\text{DD}} = 100 \text{ mV}$ and $R_{\text{in}} = 1 \text{ M}\Omega$. The corresponding values of the 3-dB frequency f_3 of the amp (noted as given in Table 6.4). Observe that when R_{in} is small, f_3 of the folded-cascade amplifier is lower than that of the CS amplifier by a factor of approximately 2.6, approximately equal to the factor by which the gain is increased. This is because, when R_{in} is small, the low-frequency response of both amplifiers is dominated by the pole located at the source node, that is,

$$f_3 = f_{\text{CS}} = \frac{1}{2\pi R_{\text{in}} C_{\text{os}}} \quad (6.216)$$

Since the output resistance of the folded-cascade amp¹⁷ is larger than that of the CS amplifier by a factor of approximately 3, as found through the load analysis above, while their output capacitances are approximately equal, the folded-cascade amp¹⁷ has a lower f_3 in this case.

On the other hand, when R_{in} is large, f_3 of the folded-cascade amplifier is much higher than that of CS amplifier. This is because, in this case, the effect of the pole at f_{CS} on the overall frequency response of the amplifier becomes significant. Since, due to the Miller effect, C_{in} of the CS amp (Eq. 6.205) is much larger than that of the folded-cascade amplifier¹⁸, it is much lower in this case. To confirm this point, observe that C_{in} of the folded-cascade amplifier can be estimated by replacing R_{in} in Eq. (6.205) with the total resistance R_{in} between the drain of M_2 and ground. Here,

$$R_{\text{in}} = r_{\text{ds}} \| r_{\text{ds}} \| R_{\text{out}} \quad (6.217)$$

where r_{ds} is the input resistance of the common-gate transistors M_2 and can be obtained using the approximation of the relationship (a) Eq. (6.82) as

$$r_{\text{ds}} = \frac{V_{\text{DD}} + V_{\text{DS}}}{{g}_{\text{m}}^2} \quad (6.218)$$

Thus,

$$R_{\text{in}} = r_{\text{ds}} \| r_{\text{ds}} \| \frac{C_{\text{os}} + C_{\text{in}}}{C_{\text{in}}^2} = \frac{2}{C_{\text{in}}^2} \quad (6.219)$$

Therefore, R_{in} must satisfy that $R_{\text{in}} > \text{Eq. (6.205)}$. Hence, C_{in} of the folded-cascade amplifier in Fig. 6.68 is indeed much smaller than C_{in} of the CS amplifier in Fig. 6.67. This confirms that the folded-cascade amplifier is much less impacted by the Miller effect and, therefore, can achieve a much higher f_3 when R_{in} is large.

The bandwidth gain of the folded-cascade amplifier can be significantly increased by replacing the current mirror M_3, M_4 with a current mirror having a larger output resistance, such as the cascode current mirror in Fig. 6.38 whose output resistance is approximately $g_{\text{m}}^2 r_{\text{ds}}$. In this case, however, R_{in} and, hence, R_{in} , increase, causing an increased Miller effect and a corresponding reduction in f_3 .

Finally, it is interesting to observe that the low-frequency response of the folded-cascade amp of Fig. 6.68(b), drawn several dBs approximately, 20 dB down from a value $R_{\text{in}} = 100 \text{ k}\Omega$ and an approximately -10 dB corner, is at $R_{\text{in}} = 1 \text{ M}\Omega$. This is because, when R_{in} is small, low-frequency response is dominated by the pole at f_{CS} . However, when R_{in} is increased, f_{CS} is moved closer to f_{L} and both poles contribute to the gain fall-off.

SUMMARY

- Integrated circuit fabrication technology allows the size of a Miller network to be approximated by the total input capacitance C_{in} of the respective small-signal MOS transistors. An averaging coefficient for IC design is α , where α is the ratio of the drain current of a p-channel transistor to its drain current when it is connected in the circuit. If the circuit shows that $\alpha < 1$, then calculate $R_{\text{in}} = C_{\text{in}}/\alpha$.
 - Kirchhoff's theorem states that an impedance Z connected between two circuit nodes 1 and 2 when voltage is applied by $V_1 - V_2$ can be replaced by two impedances $Z_1 = Z/2 + jZ\beta$ between node 1 and ground and $Z_2 = Z/2 - jZ\beta$ between node 2 and ground. Miller's theorem is only useful in the analysis of the high-frequency response of the CS and CB amplifiers.
 - DC voltage control by constant-current sources in addition to the load resistors $R_{\text{D}}/R_{\text{G}}$ has reduced the drain-to-ground voltage of these audio levels and the realization of reasonably large voltage gains while using low-voltage supplies, say, ±1 V each.
 - The largest voltage gain realizable from a CS or a CB amplifier is equal to the intrinsic gain of the transistor $A_{\text{v}} = g_{\text{m}} r_{\text{ds}}$, which for a BJT is 2000 to 4000 V/V and for a MOSFET is 30 to 100 V/V. Recall, however, that the CS amplifier has an infinite input resistance while the input resistance of the CB amplifier is limited by the finite drain-to-gate voltage. Both CS and CB amplifiers have output resistances equal to the transistor r_{ds} .
 - The high-frequency response of the CS amplifier is usually limited by the Miller effect. Therefore, αC_{in} does not result in anti-phase feedback $C_{\text{in}} \beta$.
- $$C_{\text{in}} = C_{\text{os}} + C_{\text{in}}(1 + g_{\text{m}} R_{\text{in}}^2)$$
- For a transistor with the resistance R_{in} of the signal source, we form a dominant pole thus $f_3 = 1/(2\pi R_{\text{in}} C_{\text{in}})$. Alternatively, the method of open-circuit poles, consisting of the effective load of the output node, can be used to obtain an estimate of f_3 as $f_3 = \sqrt{2\pi f_{\text{L}} C_{\text{in}}}$, where $f_{\text{L}} = C_{\text{os}} R_{\text{in}} + C_{\text{in}}(1 + g_{\text{m}} R_{\text{in}}^2)$.
- Load analysis of the low-frequency response of the CS amplifier yields the second-order transfer function given by Eq. (6.60), which can be used to determine the poles and zeros and hence f_3 .
 - The high-frequency response of the CB amplifier can be found by solving the CS equations as follows: Replace R_{in} by $R_{\text{in}} + R_{\text{in}} \| 1 + g_{\text{m}} r_{\text{ds}}$ and C_{in} by $C_{\text{in}} + C_{\text{in}}(1 + g_{\text{m}} r_{\text{ds}})^2$.
 - When the CS amplifier is fed with a low-resistance signal source, then the frequency response shown in Fig. 6.26(c)

- 6.1** The CG and CB amplifiers act as current followers. Their impedance transformation properties are displayed in Fig. 6.28 (6.3C) and Fig. 6.47 (6.3B).
- 6.2** The CG and CB amplifiers do not suffer from the Miller capacitive-coupling effect and as a result, have excellent high-frequency response. This is due to the fact that β can be neglected. The CG amplifier has two poles: one produced at the input node with a frequency $f_p = 1/(2\pi\sqrt{C_{in}(R_{in} + g_{m1})})$ and the other formed at the output node with a frequency $f_{po} = 1/(2\pi\sqrt{C_{out}(R_{out} + g_{o1})})$. The 3-dB frequency f_{po} can be determined using $f_{po} = f_p \cdot C_{in}/C_{out}$. When r_o is taken into account, the location of f_{po} can be determined from
- $$f_{po} = 1/(2\pi\sqrt{C_{in}(R_{in} + g_{m1}) + C_{in}R_{out} + R_{out}C_{out}})$$
- 6.3** In the cascode amplifier, the CG (CB) stage drives the drain (collector) of Q₂ (Q₁) as load. The result is a smaller gain than the drain-coupled (CB) and hence a reduced Miller effect in the cascode sandwich. Alternatively, note that while the CG (CB) transistors act as voltage-controlled voltage source and hence the output current is β times gain by a factor of $\mu_{eff}(\beta)$ for the A₁, refer to the output equivalent circuits shown in Fig. 6.37(a) and (b) for the MOS cascode and in Fig. 6.47(a) and (b) for the bipolar cascode.

PROBLEMS

SECTION 6.1: COMPARISON OF THE MOSFET AND THE BJT

- 6.1** Find the ratio of I_{ds} obtained in a particular NMOS transistor to its drain voltage if it increases from 0.5 V to 0.4 V. If the same current range is required in a BJT, what's the corresponding change in V_{BE} ?
- 6.2** What value of I_{ds} is obtained in a p-type transistor as a result of changing the area of the collector-base junction by a factor of 10 while keeping the drain current I_{ds} to be kept constant by other mechanisms? β is constant.
- 6.3** For each of the 7 MOSFET technologies specified in Table 6.1, find the V_{GS} and hence the V_{GS} required to operate with a β of 1000 if a drain current $I_{ds} = 100 \mu A$ is to be kept constant by other mechanisms. β is constant.
- 6.4** Consider NMOS and PMOS devices fabricated in the 0.18- μm process specified in Table 6.1. If the two devices are to be separated in equal drain areas, what must the ratio of $(W/L)_N$ to $(W/L)_P$ be to match the equal values of β_N ?
- 6.5** Consider NMOS and PMOS transistors fabricated in the 0.18- μm process specified in Table 6.1. If the two devices are to be separated in equal drain areas, what must the ratio of $(W/L)_N$ to $(W/L)_P$ be to match the equal values of β_N ?
- 6.6** An NMOS transistor represented in the 0.18- μm CMOS process specified in Table 6.1 is operated at $V_{GS} = -0.2$ V. Find the required V_{DS} and I_{DS} to obtain a g_{m1} of -10 mA/V . At what value of V_{DS} must the transistor be operated to achieve this value of g_{m1} ?
- 6.7** For each of the CMOS processes test voltages as listed in Table 6.1, find the g_m of an NMOS and a PMOS transistor with $R_{DS} = 10$ ohms at $I_{DS} = 100 \mu A$.
- 6.8** An NMOS transistor operated with a drain voltage of 0.25 V is required to have a g_m equal to 100 $\mu A/V$

- at transistor operating at $I_{DS} = 1 \text{ mA}$. What V_{GS} to be? What is the V_{DS} at breakdown?

- 6.9** It is required to find the incremental (i.e., small-signal) resistance of each of the three-connected transistors shown in Fig. 6.9. Assume that the bias current is 0.1 mA for the NMOSFET, let $\mu_F C_{ox} = 200 \text{ picoF}$ and $R_{DS} = 10$.

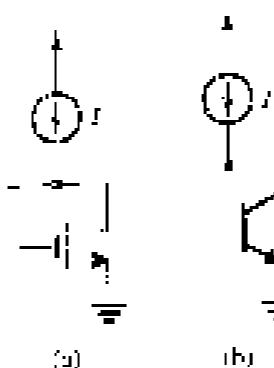


FIGURE 6.9

- 6.10** For an NMOS transistor with $L = 1 \mu m$ fabricated in the 0.18- μm process specified in Table 6.1, find β_N , β_P , β_{NP} , and β_{PN} if the device is operated with $V_{GS} = -0.5$ V and $I_D = 100 \mu A$. Also, find the required device width W .

- 6.11** For an NMOS transistor with $L = 0.2 \mu m$ fabricated in the 0.18- μm process specified in Table 6.1, find β_N , β_P , β_{NP} , and β_{PN} when the device is operated at $I_D = 100 \mu A$ with $V_{GS} = -0.2$ V. Also, find W .

- 6.12** From the table below, for the HBT let $\beta = 100$ and $V_{BE} = 100$ mV. For the NMOSFET, let $\mu_F C_{ox} = 300 \text{ picoF}$, $R_{DS} = 40$ ohms, and $V_{DS} = 10$ V. Note that, in order to find the input resistance at the external input terminal (gate), assume that the drain current is grounded.

Device	β	V_{BE}	R_{in}	R_{out}
NMOSFET	100	100 mV	300 picoF	40 ohms
Current-mirror	100	100 mV	300 picoF	40 ohms
HBT	100	100 mV	300 picoF	40 ohms

- 6.13** For an NMOS transistor fabricated in the 0.18- μm process specified in Table 6.1 with $L = 0.3 \mu m$ and $W = 6 \mu m$, find the value of V_{GS} required when the transistor is operated at $V_{DS} = 0.5$ V. Use both the formula in terms of I_{DS} and C_{ox} , and the approximate formula. Why does the approximate formula overestimate V_{GS} ?

- 6.14** An NMOS transistor fabricated in the 0.18- μm process specified in Table 6.1 and having $L = 102 \mu m \times 0.3 \mu m$ is operated at $V_{GS} = 0.2$ V and has a drain load of 100 ohms. Find A_{v1} , f_T , f_{po} , f_{p1} , and f_{s1} . At what I_D value is the transistor operating? If it is required to couple f_{s1} which is 0.1 to become 10, what is required A_{v2} ? Why is f_{p2} low in this case?

- 6.15** Consider a transistor fabricated in the high-voltage process specified in Table 6.2, assume $L = 1 \mu m$, $W = 100 \mu m$, and $I_{DS} = 100 \mu A$. Assume $\beta_N = \beta_P$. Repeat for the low-voltage process.

- 6.16** Consider an NMOS transistor fabricated in the 0.18- μm process specified in Table 6.1. Let the transistor be operated at $I_D = 100 \mu A$.

- (a) For $V_{GS} = 0.25$ V, let W , β_N , β_P , β_{NP} , β_{PN} , and f_T . Find the I_D value and V_{DS} be changed to a value I_D' . Find the new values of V_{GS} , β_N , β_P , β_{NP} , β_{PN} , and f_T .

- 6.17** For a lateral p-n-p transistor fabricated in the high-voltage process specified in Table 6.2, let I_{DS} be increased if the transistor is operated at a collector bias current of 1 mA. Compare to the value obtained for a vertical p-n-p.

- 6.18** Show that in a MOSTET the solution of I_D and V_{GS} determines A_{v1} and f_{p1} . In other words, show that A_{v1} and f_{p1} will not depend on I_{DS} and V_{DS} .

- 6.19** Consider an NMOS transistor fabricated in the 0.18- μm technology specified in Table 6.1. Let the transistor be operated at $I_D = 0.2$ V. Find β_N and f_T for $L = 0.2 \mu m$, $0.3 \mu m$, and $0.4 \mu m$.

- 6.20** Consider an NMOS transistor fabricated in the 0.18- μm process specified in Table 6.1, let $L = 0.5 \mu m$ and $V_{GS} = 0.5$ V. If the NMOSFET is connected as a common-source amplifier with a load capacitance $C_L = 3 \text{ pF}$ (see Fig. 6.22), find the required transistor width W and bias current I_D to obtain a unity-gain bandwidth of 10 MHz. Also, find A_{v1} and f_{p1} .

SECTION 6.3: IC BIASING, CURRENT SOURCES, CURRENT MIRRORS, AND CURRENT-STEERING CIRCUITS

- 6.21** For $V_{GS} = 1.5$ V and using $I_{DSR} = 50 \mu A$, it is required to design the circuit of Fig. 6.1 to obtain an output current with a nominal value of 50 μA . Note: If Q_1 and Q_2 are matched in the channel lengths to 0.8 μm , the drain widths of 5 μm , $V_{DS} = 0.5$ V, and $I_D = 250 \mu A/\mu m^2$. What is the low-current bias value of V_{GS} ? Assuming that for this geometry the drain voltage V_{DS} is 20 V, find the output resistance of the current source. Also, find the change in output resistance if there is a 10% change in V_{GS} .

- 6.22** Using $V_{GS} = 1.5$ V and a pair of matched NMOSFETs, design a current source circuit with $C_{in} = 6.4 \text{ pF}$ and $I_{DSR} = 0.2 \mu A$.

current, $\phi = 100 \mu\text{A}$, $2000 \times$ value. To simplify matters, assume that the nominal value of the output current is obtained at $V_T = V_{DD}$. It is further required that the circuit operate in V_T in the range of $1.25 \text{ V} \leq V_T \leq 1.5 \text{ V}$, so that the change in I_o over this range be limited to 5% of the required value of I_o . Then the requirement is that R and the device dimensions. For the fabrication-process technology utilized, $n_i C_{ox} = 250 \text{ m}\text{A/V}^2$, $R_s = 20 \text{ k}\Omega/\text{cm}^2$, and $V_A = 0.6 \text{ V}$.

6.23 Sketch the π -equivalent of the current source circuit of Fig. 6-4. Note that while the circuit of Fig. 6-4 should more appropriately be called a current sink, the corresponding PSpice circuit is a current source. Let $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, I_D and g_2 be measured and $\mu_nC_{ox} = 100\text{ }\mu\text{A/V}^2$. Find the device (BJT) value and the value of the resistor that sets the load condition that a minimum 80 μA output current is obtained. The current source is required to operate at V_D as high as 1.6 V (negative channel-length modulation).

6.24 Consider the current mirror circuit of Fig. 6.5 with two transistors having equal channel lengths but with $\beta_1 > \beta_2$, having a width ratio W_1/W_2 that is $\beta_1/\beta_2 = 10$. $V_{BE1} = 20$ mV and the transistors are operating at an overriding voltage of 0.1 V. What is I_0 resulting? What is the minimum allowable value of V_{BE2} for proper operation of the current source? If $V_{BE1} = 0.5$ V, what value of V_{BE2} will the nominal value of I_0 be obtained? If V_{BE1} increases by 1 V, what is the corresponding increase in I_0 ? Let $V_T = 25$ mV.

6.25 For the Zener-diode circuit of Fig. P6.25, find I_L , in terms of I_{in} , and derive the ZD bias.

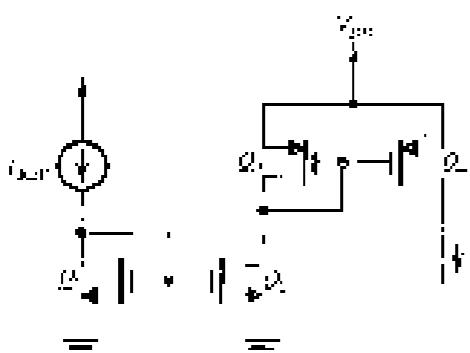


FIGURE PR.19

06.26 The var-cut-switching circuit of Fig. P6.26 is formed in nMOS technology for which $\mu_nC_{ox} = 200 \text{ aF/V}^2$, $\mu_pC_{ox} = 80 \text{ pF/V}^2$, $V_{th} = 0.6 \text{ V}$, $n_A = 100 \text{ V}/\mu\text{A}$, $p_A = 10 \text{ V}/\mu\text{A}$, and $V_{FB} = 12 \text{ V}$. If all resistors have $R = 3k\Omega$, design the circuit so that $I_{D1} = 31 \mu\text{A}$, $I_2 = 200 \mu\text{A}$, $I_3 = I_4 = 20 \mu\text{A}$, and $I_{D2} = 21 \mu\text{A}$. Use the minimum possible device widths while achieving proper operation of the current source Q_1 for voltages v_1 as high as $+1.2 \text{ V}$ and proper operation of the current sink Q_2 with voltages v_2 as high as -0.8 V . Specify the widths of all devices and

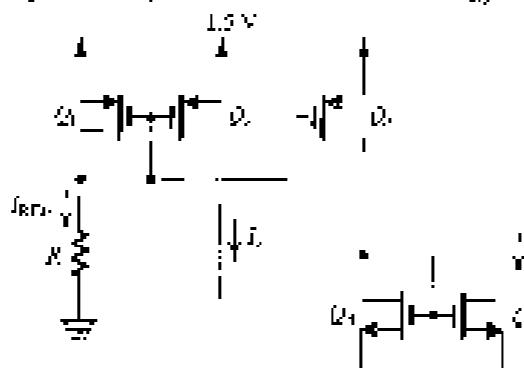
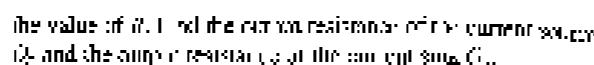


FIGURE P6.26

***6.27** A PMSOS current mirror consists of three PMSOS transistors, one diode connected and two used as current mirrors. All transistors have $|V_t| = 10^3 \text{ V}$, $V_A = 80 \mu\text{A/V}^2$, and $L = 1.0 \mu\text{m}$ with drain-to-source widths, namely, 10 μm , 20 μm , and 40 μm . When the diode-connected transistor is supplied from a 100 μA source, how many different output currents are available? Repeat with one of the transistors diode connected and the third used as possible current output. For each case do the post-layout simulation, give the values of the output current I_o and of transistors' bias results.

6.28 Although thus far we have focused only on the application of op-amp filters in dc blocking, they can also be used as signal-current amplifiers. One such application is illustrated in Fig. PS.28. There v_x is a common-mode input voltage fed with $v_y = V_{DD}/2 - v_x$, where V_{DD} is the voltage source on one terminal of Q_1 , and v_y is a small signal to be amplified. Find the signal component of the output voltage v_O and express the small-signal current gain A_{vO} .

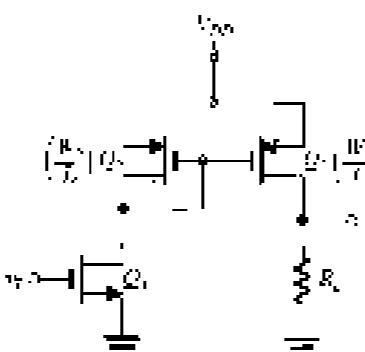


FIGURE P6.28

6.29 Consider the basic bipolar current mirror of Fig. 6.8 (i.e., the top N channel Q_1 and Q_2 are identical devices having $L = 10 \mu\text{m}$).

(c) Assuming the transconductance is very high, find the values of V_{CE} and I_C corresponding to I_{BE} increasing from 10 nA to 100 nA. Assume that Q is zero in the reverse mode, and neglect the base effect.

(g) Find the range of i_0 corresponding to i_{FET} in the range of 0.25 mA to $0.1 \mu\text{A}$, taking into account the small β_A and the β_A being constant at 100 over the current range of 0.1 mA to 0.25 mA and the $\beta_F = 10^{-3} \text{ mA}$, $\mu = 10$. Specify i_0 corresponding to $i_{\text{FET}} = 10^{-3} \text{ mA}$, 0.1 mA , 1 mA , and 10 mA . Note that β_A increases with current because the contact becomes more ohmic.

6.30 Consider the basic BJT current mirror of Fig. 6.6 for the case in which β_2 has 10 times the area of β_1 . Show that the current增益 ratio is given by Eq. (6.19). If β_1 is specified to be a minimum of 80, what's the largest current ratio α possible while keeping the current increased by one time β_2 turned to 32?

6.31 Give the circuit and the *one* equation for the steady current in each of Fig. 6.8. If R_1 of the pipe network is 20, what is the current of 10 A after switch 1 is closed, realizing the Tandy? See Fig. 6.8.

6.32 Consider the basic E-T current mixer of Fig. 6.8 where Ω_1 and Δ_2 are matched and $f_{AT} = 2$ in A. Neglecting the effect of finite β , find the change in I_2 , both in absolute value and as a percentage, corresponding to V_T changing from $+5 \times 10^{-3}$ V to -5×10^{-3} V. The Early voltage is 50 V.

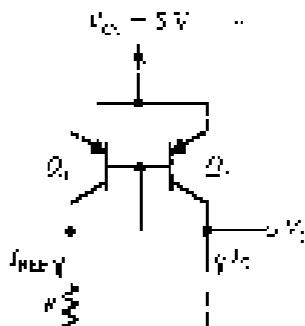
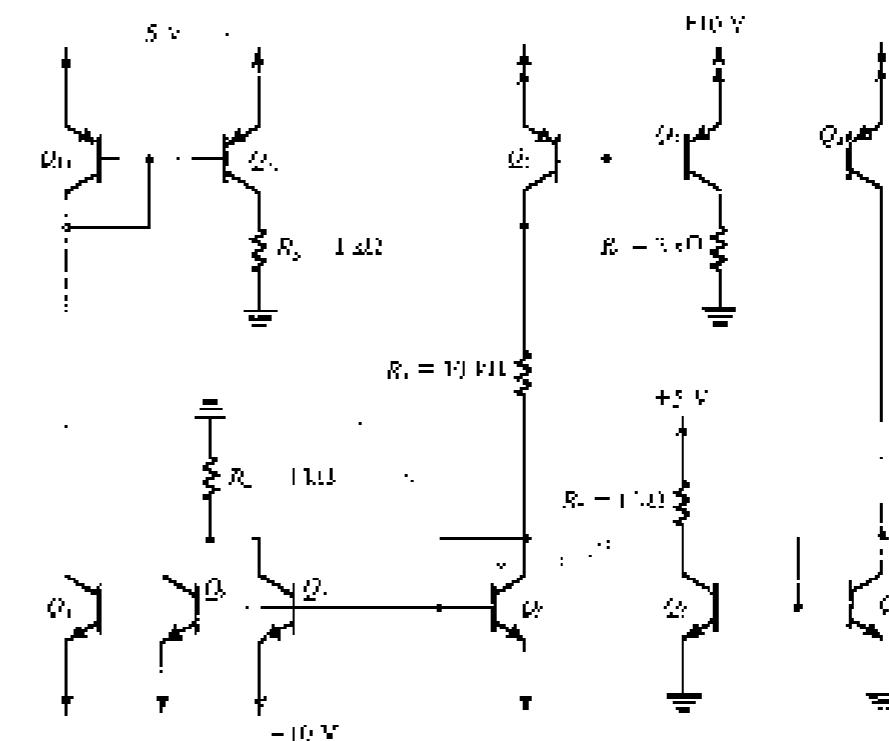


FIGURE P6.3

E3.4 Find the voltages v_a , all currents and the currents through the branches in the circuit of Fig. E3.1. Assume $|V_{AB}| = 0.2$ V and $d = \infty$.



PGWARE Pg.34

6.51 Consider a voltage amplifier with a gain of -100 V/V and a feedback -100 dB connected in the feedback path, that is, between the output and input terminals. Use Miller's theorem to find the input resistance of this circuit.

6.52 An ideal voltage amplifier with a voltage gain of -1000 V/V has a $0.1-\text{pF}$ shunt capacitor connected between its output and input terminals. What is the input capacitance of the amplifier? If the amplifier is fed from a voltage source V_s having a resistance $R_{v_s} = 1 \text{ k}\Omega$, find the intrinsic transconductance g_{m1} as a function of the small-signal frequency variables and hence the 3-dB frequency f_3 and the unity-gain frequency f_1 .

6.53 The air-vortex diode shown is characterized by the description (A, C) , where A is the voltage gain from input to output and C is an internal capacitor connected between input and output. For each, find the equivalent capacitance at the input and the output as provided by the law of Miller's theorem:

- 1000 V/V , $1 \mu\text{s}$
- -10 V/V , 10 pF
- -1 V/V , 10 pF
- -1 V/V , 10 pF
- $+1 \text{ V/V}$, 10 pF

Note that the internal capacitance C can in some cases be used to cancel the effect of a shunt capacitor connected from input to ground. In (c), what capacitance can be cancelled?

6.54 Figure P6.54 shows an ideal voltage amplifier with a gain of -1 V/V (neglecting the effect of the load) connected with an input shunt capacitor and a resistance R_i connected between output and input.

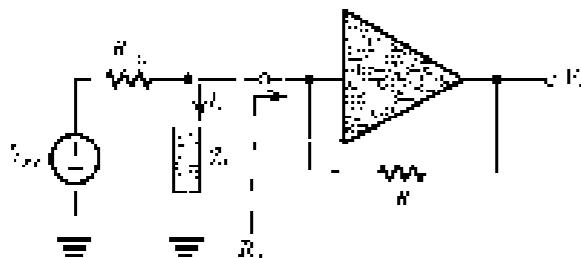


FIGURE P6.54

- Using Miller's theorem, show that the input resistance $R_{in} = -R_i$.
- Using Norton's theorem, replace V_{out} , R_{out} , and R_i with a signal current source and an equivalent voltage source. Show that, by selecting $R_{out} = R_i$, the equivalent parallel resistance becomes infinite, and the circuit has an ideal input voltage V_i (that is, $V_i = V_{out}/2$), with this, their AV ratio is:
- Consider the CMOS amplifier of Fig. 6.18(a) with a process for which $V_t = 1.5 \text{ V}$, $250 \mu\text{A}/\text{V}^2$, $|V_g| = 0.6 \text{ V}$, and $|V_d| = 10 \text{ V}$. Find I_{D1} and $|I_{D2}|$ to obtain a voltage gain of -40 V/V and an output resistance of $100 \text{k}\Omega$. If Q_1 and Q_2 are to be operated at 0.5 mA , the drain-to-source voltage is 2 V , with this, their AV ratio is:
- Consider the CMOS amplifier analyzed in Example 6.6. If V_s consists of two sinusoidal signals, one with no effect imposed on the other (i.e., one that the other does not affect), will V_{out} be the same two sinusoidal signals?
- If V_s is a capacitor, C , find the transfer function V_o/V_s and show it is the desired noninverting integrator.

SECTION 6.5: THE COMMON-SOURCE AND COMMON-EMITTED AMPLIFIERS WITH ACTIVE LOADS

6.55 Find the intrinsic gain of an NMOS transistor fabricated in a process for which $V_t = 125 \mu\text{A}/\text{V}^2$ and $|V_g| = 10 \text{ V}$. The transistor has a 1- μm channel length and is operated at $V_{ds} = 0.2 \text{ V}$. If a $2-\text{nA}/\text{V}$ transconductance is required, what must I_D and R_L be?

6.56 An NMOS transistor fabricated in a certain process is found to have an intrinsic gain of 100 V/V when operated at $I_D = 100 \mu\text{A}$. Find the intrinsic gain for $I_D = 25 \mu\text{A}$ and $I_D = 400 \mu\text{A}$. For each of these currents, find the transconductance changes from its estimate $g_m = 100 \mu\text{A}$.

6.57 The NMOS transistor in the circuit of Fig. P6.57 has $V_t = 0.5 \text{ V}$, $|g_m| = 2 \text{ mA}/\text{V}^2$, and $V_{ds} = 20 \text{ V}$.

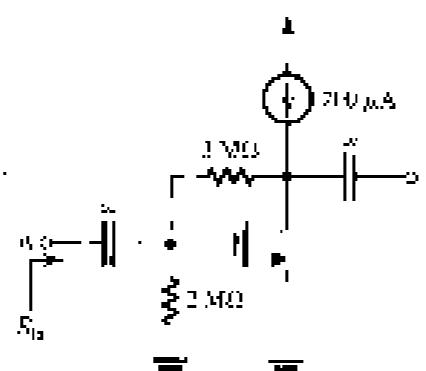


FIGURE P6.57

(a) Neglecting the drain-to-source voltage effect and the effect of r_{ds} and V_{ds} , and V_{gs} , find the drain current in the transistor Q_1 , and verify that you were justified in neglecting it.

(b) Find the small-signal voltage gain, V_o/V_s . When is the peak of the largest component of V_o close to that possible while the NMOS transistor is saturated? What is the maximum V_s input signal?

(c) Find the small-signal input resistance R_{in} .

6.58 Consider the CMOS amplifier of Fig. 6.18(b) with a process for which $V_t = 1.5 \text{ V}$, $250 \mu\text{A}/\text{V}^2$, $|V_g| = 0.6 \text{ V}$, and $|V_d| = 10 \text{ V}$. Find I_{D1} and $|I_{D2}|$ to obtain a voltage gain of -40 V/V and an output resistance of $100 \text{k}\Omega$. If Q_1 and Q_2 are to be operated at 0.5 mA , the drain-to-source voltage is 2 V , with this, their AV ratio is:

- (d) Consider the CMOS amplifier analyzed in Example 6.6. If V_s consists of two sinusoidal signals, one with no effect imposed on the other (i.e., one that the other does not affect), will V_{out} be the same two sinusoidal signals?
- (e) If V_s is a capacitor, C , find the transfer function V_o/V_s and show it is the desired noninverting integrator.

the output with alternative current inversion. What is the magnitude of the current i_{DS} resulting from V_{out} ? To provide the gain, this circuit has a feedback circuit that enables it to operate in a constant-current mode of its linear region.

6.59 The power supply voltage of the CMOS amplifier analyzed in Example 6.8 is increased to 5 V . What is the extent of the linear region of the output voltage?

6.60 Figure P6.60 shows an NMOS amplifier formed by cascading two common-source stages. Assuming the $V_t = 100 \mu\text{A}$, and the biasing current sources to be comparable to those of Q_1 and Q_2 . Find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2 .

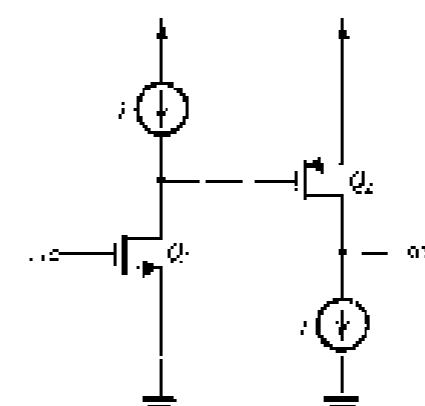


FIGURE P6.60

6.61 Figure P6.61 shows an NMOS amplifier formed by cascading two common-emitter stages. Assuming the $V_t = 100 \mu\text{A}$, and the biasing current sources to be comparable to those of Q_1 and Q_2 . Find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2 .

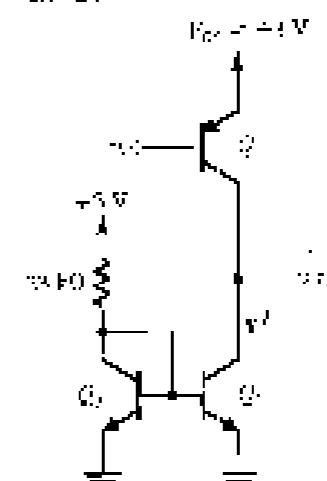


FIGURE P6.61

6.62 Consider the circuit shown in Fig. 6.18(c), using a $\pm 4 \text{ V}$ supply and transistors for which $V_t = 0.8 \text{ V}$ and $|V_g| = 1 \mu\text{m}$. For Q_1 , $|V_d| = 100 \text{ V}$, and $|V_s| = 20 \text{ nm}$; for Q_2 and Q_3 , $|V_d| = 50 \mu\text{m}/\text{V}$ and $V_s = 20 \text{ V}$. For Q_4 , $V_s = 0 \text{ nm}$. For Q_5 , $|V_d| = 10 \mu\text{m}$.

(a) Let Q_2 be n -biased at 100 pA (neglect V_{ds}). For simplicity, ignore the effect of V_{ds} .

(b) What are the extreme values of q_{D2} at which Q_2 and Q_3 just remain in saturation?

(c) What is the biasing and storage point?

(d) Find the slope of the transfer characteristic at $V_{ds} = V_{ds,ss}/2$.

(e) For operation as a small-signal amplifier around a bias point at $V_s = V_{ds,ss}/2$, find the small-signal voltage gain V_o/V_s over V_{ds} resistance.

6.63 The NMOS M_1 in the circuit of Fig. P6.63 is replaced, leaving $V_{ds,ss} = V_{ds}/W/L = 100 \mu\text{A}/\text{V}^2$ and $V_s = 0 \text{ nm}$. The resistor is $R = 1 \text{ M}\Omega$.

- (a) For $V_s = 0 \text{ nm}$, assume the drain current I_{D1} and I_{D2} (M_1 to $\text{M}_2 = n$), what is the voltage gain of the amplifier from G_1 to D_2 ?

- (c) Negating the bias node currents of β_1 and β_2 and assuming that their $V_{BE} = 0.7\text{ V}$ and $r_{DS} \gg R_{DS}$, find the value of β_0 . Find the value of β_0 .
- (d) If β_1 and β_2 are specified to have $V_{BE} = 50\text{ mV}$, find r_{DS} and r_{DS} and hence the load resistance at the collector of β_0 . Find r_{DS} and r_{DS} assuming that $\beta_0 = 50$.
- (e) Find R_{DS} , β_0 , and R_L .

SECTION 6.6: HIGH-FREQUENCY RESPONSE OF THE CS AND CE AMPLIFIERS

- 6.66** A CS amplifier that can be represented by the equivalent circuit of Fig. 6.20 has $C_{1s} = 2\text{ pF}$, $C_{1d} = 0.1\text{ pF}$, $C_2 = 1\text{ pF}$, $\beta_1 = 50\text{ mA/V}$, and $R_{DS} = R'_1 = 20\text{ k}\Omega$. Find the midband gain, the input capacitance C_{in} , using the Miller equivalence, and hence an estimate of the 3-dB frequency f_B .

- 6.67** A CS amplifier can be represented by the equivalent circuit of Fig. 6.20 has $C_{1s} = 2\text{ pF}$, $C_{1d} = 0.1\text{ pF}$, $C_2 = 1\text{ pF}$, $\beta_1 = 50\text{ mA/V}$, and $R_{DS} = R'_1 = 20\text{ k}\Omega$. Find the midband gain, and C_{in} from the 3-dB frequency using the method of open-loop, line constants. Also, give the percentage contribution to f_B by each of three capacitances. (Note that this is the same amplifier considered in Problem 6.66; if you have solved Problem 6.66, compare your results.)

6.68 A CS amplifier represented by the equivalent circuit of Fig. 6.20 has $C_{1s} = 2\text{ pF}$, $C_{1d} = 0.1\text{ pF}$, $C_2 = 1\text{ pF}$, $\beta_1 = 50\text{ mA/V}$, and $R_{DS} = R'_1 = 20\text{ k}\Omega$. Find the exact values of f_B , C_{in} , and A_m using Eq. (6.60). Hence estimate C_{in} . Compare the values of f_B and C_{in} to the approximate values obtained using Eqs. (6.65) and (6.67). (Note that this is the same amplifier considered in Problems 6.66 and 6.67; if you have solved either or both of those problems, compare your results.)

6.69 A CS amplifier represented by the equivalent circuit of Fig. 6.20 has $C_{1s} = 2\text{ pF}$, $C_{1d} = 0.1\text{ pF}$, $C_2 = 1\text{ pF}$, $\beta_1 = 50\text{ mA/V}$, and $R_{DS} = R'_1 = 20\text{ k}\Omega$. It is required to find A_m , f_B , and the gain-bandwidth product for each of the following values of R_L : 5 k Ω , 10 k Ω , and 20 k Ω . Use the approximate expression for f_B in Eq. (6.64). However, in each case also evaluate f_{AB} and f_B to ensure that a minimum pole exists, and in each case, note whether the unity-gain frequency is equal to the gain-bandwidth product. Present your results in tabular form and comment on the gain-bandwidth trade-off.

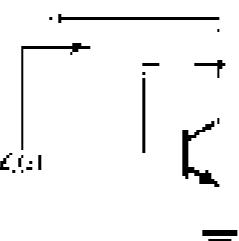


FIGURE P6.72

6.73 For the circuit model in Fig. 6.72, derive an expression for the current transfer function I_2/I_1 (1) taking into account the BJT internal capacitances and neglecting r_e and r_{DS} . Assume the DUTs to be identical. (Note that a signal appears at the collector of Q_2 if the current is larger than I_1 and the HTR is not operating.) Find the characteristics by $f_T = 200\text{ MHz}$, $C_1 = 2\text{ pF}$, and $\beta_0 = \infty$. Find the frequencies of the pole and zero of the transfer function.

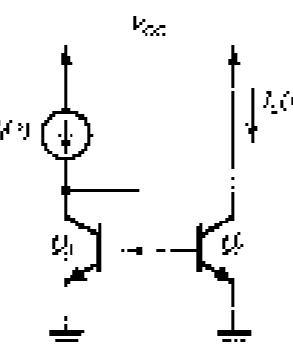


FIGURE P6.73

6.74 A CS amplifier modeled with the equivalent circuit of Fig. 6.20 is specified to have $C_{1s} = 2\text{ pF}$, $C_{1d} = 0.1\text{ pF}$, $C_2 = 1\text{ pF}$, $\beta_1 = 50\text{ mA/V}$, $\beta_2 = 100$, $r_{DS} = 200\text{ M}\Omega$, $R_{DS} = 5\text{ k}\Omega$, and $R'_1 = 1\text{ k}\Omega$. Find the midband gain A_m and an estimate of the 3-dB frequency f_B using the Miller equivalence.

6.75 A common-emitter amplifier that can be represented by the equivalent circuit of Fig. 6.20 is specified $C_{1s} = 10\text{ pF}$, $C_{1d} =$

0.5 pF , $\beta_1 = 2\text{ pA}$, $\beta_2 = 20\text{ mA/V}$, $\beta_0 = 100$, $r_{DS} = 200\text{ M}\Omega$, and $R_{DS} = 5\text{ k}\Omega$. Find the midband gain A_m and the 3-dB frequency f_B . Hence estimate the 3-dB frequency achieved.

6.76 It is required to analyze the high-frequency response of the CMOS amplifier shown in Fig. 19.75. The dc bias current is 100 nA . For β_1 , β_2 , $\beta_0 = 100$ and $V_t = 13.6\text{ mV}$, $W_1 = 100\text{ }\mu\text{m}$, $L_1 = 0.2\text{ }\mu\text{m}$, $C_{1s} = 0.6\text{ pF}$, $C_{1d} = 0.05\text{ pF}$, and $C_2 = 20\text{ fF}$. For β_2 , $C_{2s} = 0.015\text{ pF}$, $C_{2d} = 26\text{ fF}$, and $V_d = 19.2\text{ V}$. Assume that the resistance of the input signal generator is negligibly small. Also, let's implicitly assume that the signal voltage at the gate of D_1 is zero. Find the low-frequency gain, the frequency of the pole, and the frequency of the zero.

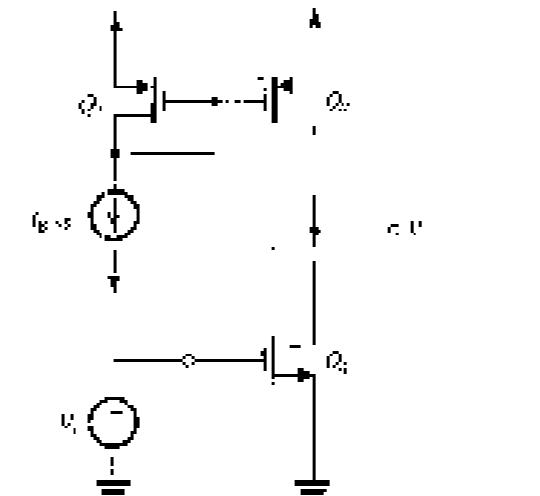


FIGURE P6.76(a)

6.77 Consider an n -channel common-emitter amplifier. Let the amplifier be fed with an ideal voltage source V_s , and neglect the effect of r_e . Assume that the bias or test source has a very high resistance and connects to a common-emitter MOSFET through its output node to ground. This configuration approximates the sum of the input capacitance of the subsequent stage and the inevitable parasitic capacitance between collector and ground. Show that the voltage gain is given by

$$\frac{V_o}{V_s} = \frac{1 - e^{(C_{in}/L_1)}}{1 + C_{in}f_T} \quad (1)$$

$$\approx \frac{R_{DS}}{1 + C_{in}f_T} \quad \text{for small } f_T$$

If the condition is maintained $f_T = 200\text{ }\mu\text{A}$ and $V_t = 100\text{ mV}$, $C_{in} = 0.2\text{ pF}$, and $r_{DS} = 1\text{ pF}$, find the 3-dB frequency, and the frequency at which the gain reduces to unity. Sketch a Bode plot for the gain magnitude.

6.78 A n -channel CS amplifier is fed with a low-resistance signal source and operating with $g_{ds} = 1\text{ mA/V}$. Its 3-dB frequency is of 2 GHz. What additional capacitive load must be connected to the drain to reduce f_B to 1 GHz?

SECTION 6.7: THE COMMON-GATE AND COMMON-BASE AMPLIFIERS WITH ACTIVE LOADS

6.78 Consider a CG amplifier Q_1 which $\beta = 100$, $\lambda = 0.1 \text{ V}^{-2}$, $R_{\text{ds}} = 20 \text{ m}\Omega$, $x = 0.2$, $\rho = 0.8 \text{ m}\Omega$, and $R_{\text{L}} = R_{\text{d}} = r_{\text{d}}$. Find $r_{\text{in}}, r_{\text{out}}, R_{\text{in}}, R_{\text{out}}, R_{\text{ds}}, r_{\text{ds}}$, and f_{c} . In the amplifier, a current fed voltage-controlled voltage source V_{ctrl} provides resistance R_{ctrl} equal to $r_{\text{d}} + R_{\text{L}} + r_{\text{ds}}$, and I_{ctrl} denotes the current in input R_{ctrl} .

6.79 Consider an NMOS CG amplifier for which the current-source load is implemented with a PMOS transistor having an output voltage V_{ctrl} equal to that of Q_1 in NMOS mode. Design circuit so that $r_{\text{ds}}/r_{\text{d}} = 100 \text{ mV/V}$ and $R_{\text{ctrl}} = 2 \text{ k}\Omega$. Assume $|V_{\text{ctrl}}| = 20 \text{ V}$, $\rho = 0.2$, and $R_{\text{L}} = 100 \text{ m}\Omega$. Specify I_{ctrl} and V_{ctrl} of the NMOS transistors.

6.80 Derive an expression for the overall voltage gain A_{v} of a CG amplifier, $G_1 = 1/r_{\text{in}}$, in terms of $A_{\text{v}1}, R_{\text{ctrl}}$, and r_{ds} . Under what condition does G_1 become close to unity? Refer to the equivalent circuit in Fig. 6.5(b).

6.81 What is the aggregate input resistance R_{in} of a CG amplifier, given by its resistance $R_{\text{in}} = r_{\text{in}} + r_{\text{ds}}$?

6.82 In the MOSFET voltage source shown in Fig. 6.82, a required drain-to-source current of 1.14 mA with $V_{\text{ctrl}} = 2.0 \text{ V}$, the MOSFET has $V_t = 0.55 \text{ V}$, $V_{\text{ds}} = 20 \text{ V}$, and the body transconductance G_{m} is $x = 0.2$. Find the value of R_{ctrl} that results in a current r_{ds} and a drain resistance of $200 \text{ m}\Omega$. Also, determine the required gate voltage V_{ctrl} .

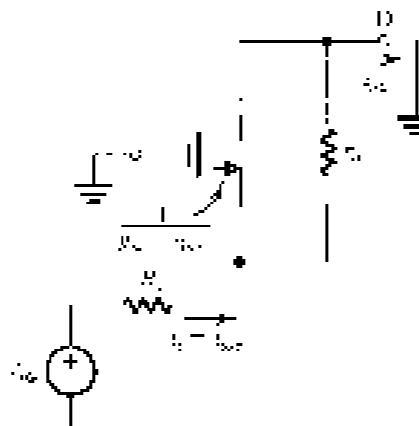


FIGURE P6.84

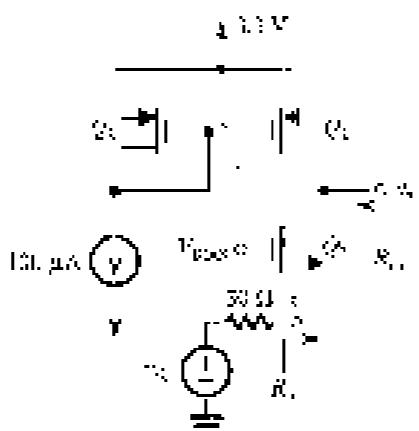


FIGURE P6.85

Transistor Q_1 has $x = 0.2$. The signal v_{ctrl} is a small-signal with no dc component.

- Neglecting the effect of r_{ds} , find the drain current of Q_1 and the required value of V_{ctrl} .
- Find the values of r_{in} and r_{out} and r_{ds} for ω frequencies.
- Find the value of R_{ctrl} .
- Find the value of R_{in} .
- Calculate the voltage ratios v_{ctrl}/v_t and $v_{\text{ctrl}}/v_{\text{ds}}$.
- How large can v_{ctrl} be (peak-to-peak) while maintaining saturation-mode operation for Q_1 and Q_2 ?

6.86 A CG amplifier is specified to have $r_{\text{in}} = 5 \text{ pF}$, $C_{\text{g}} = 0.1 \text{ pF}$, $C_{\text{d}} = 2 \text{ pF}$, $\rho = 5 \text{ m}\Omega/\text{V}$, $\beta = 100$, $R_{\text{ds}} = 1 \text{ m}\Omega$, and $R_{\text{L}} = 20 \text{ k}\Omega$. Neglecting the effect of r_{ds} (and the low-frequency approximation), the frequencies of the poles f_p and f_{c} and hence an estimate of f_{c} at the frequency f_p .

6.87 For the CG amplifier considered in Problem 6.86, we wish to determine the low-frequency voltage gain v_{ctrl}/v_t and all resistances (now $|V_{\text{ctrl}}| = 0.3 \text{ V}$ and $V_{\text{ctrl}} = 20 \text{ V}$,

an estimate of r_{in} , the drain-to-gate voltage V_{ctrl} , the drain-to-source voltage V_{ctrl} , and feeding a load resistance R_{L} in parallel with a capacitance C_L .

6.88 Use Fig. 6.84(a) together with Eq. (6.1.9) to derive the expression in Eq. (6.111).

6.89 Use Eq. (6.112) to explore the variation of the input resistance R_{in} with the load resistor R_{L} . Specifically, for $\beta = 100$ and $r_{\text{ds}} = 1 \text{ m}\Omega$, let $R_{\text{L}}/r_{\text{ds}} = 0, 1, 10, 100, 1000$, and so on, $\beta = 200$. Present your results in tabular form.

6.90 Consider an active-loaded BJT configuration, i.e., the common-base configuration with $\beta = 100$. If the intrinsic gain of the BJT is 2000, what value of r_{ds} causes the drain resistance R_{d} to be exactly the value of r_{ds} ?

6.91 Use Fig. 6.37 to derive the expression in Eq. (6.1.11).

6.92 Use Eq. (6.1.18) to explore the variation of the output resistance of the CB amplifier with the signal generator resistance r_{ds} . First, derive an expression for $r_{\text{out}}/r_{\text{ds}}$ as a function of β and m , where $m = R_{\text{L}}/r_{\text{ds}}$. Then use this expression to generate curves for $r_{\text{out}}/r_{\text{ds}}$ versus R_{L} with values for $R_{\text{L}} = r_{\text{ds}}/2$, $2r_{\text{ds}}$, $4r_{\text{ds}}$, $8r_{\text{ds}}$, $16r_{\text{ds}}$, and $32r_{\text{ds}}$ for $\beta = 100$.

6.93 As is pictured in the text, the CBJ can either be used as a common-emitter. That is, when fed with a constant signal, it passes it to the collector and it makes the output collector current at a high current resistance. Figure P6.93 shows a CBJ amp, fed with a signal current i_{sig} having a source resistance $R_{\text{in}} = 10 \text{ k}\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 50 \text{ V}$. Note that the bias arrangement is not shown (i.e., point at the collector is represented by its Norton equivalent circuit). Find the value of the output gain k and the output resistance R_{out} .

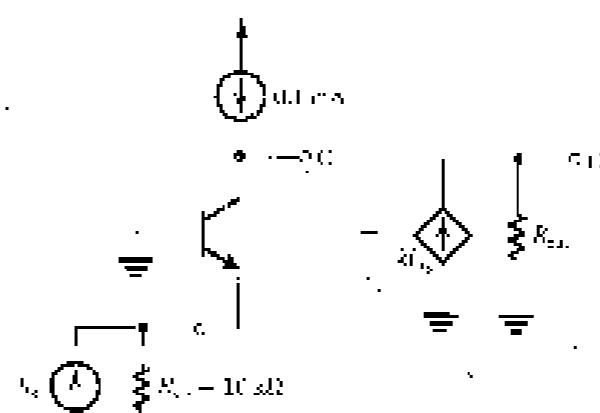


FIGURE P6.93

and R_{L} and feeding a load resistance R_{L} in parallel with a capacitance C_L .

6.94 Show that for $r_{\text{ds}} \rightarrow \infty$ the circuit can be simplified into two parallel input port that produces a pole at

$$f_{\text{c}} = \frac{1}{2\pi C_{\text{g}}(R_{\text{in}} + r_{\text{ds}})}$$

and an output port that forms a pole at

$$f_{\text{c}} = \frac{1}{2\pi(C_{\text{d}} + C_{\text{L}})R_{\text{L}}}$$

Note that these are the bipolar counterparts of the MOS expressions in Probs. 6.105 and 6.106.

(b) Furthermore, r_{ds} and r_{in} , and hence r_{out} are given in the case $R_{\text{in}} = 10 \text{ k}\Omega$, $C_{\text{g}} = 2 \text{ pF}$, $C_{\text{d}} = 1 \text{ pF}$, $C_{\text{L}} = 1 \text{ nF}$, $R_{\text{L}} = 1 \text{ k}\Omega$, and $R_{\text{ds}} = 10 \text{ k}\Omega$. Also, find y of the transistor.

6.95 Adapt the expressions in Probs. 6.107, 6.108, and 6.109 for the case of the CB amplifier.

6.96 For the constant-current source circuit shown in Fig. 6.96, find the collector current I and the current resistance. The BJTs are operated to have $\beta = 100$ and $\rho = 100 \text{ m}\Omega$. If the collector voltage undergoes a change of $+10 \text{ V}$ while the HBT remains in the active mode, what's the corresponding change in collector current?

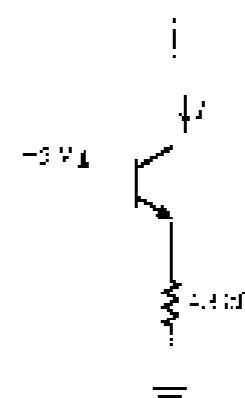


FIGURE P6.96

SECTION 6.8: THE CASCODE AMPLIFIER

6.97 For the cascade amplifier of Fig. 6.86(a), let Q_1 and Q_2 be germanium with $V_t = 0.5 \text{ V}$, $\rho = 60 \text{ m}\Omega/\text{V}$, $\lambda = 0.05 \text{ V}^{-2}$, $\beta = 50$, $R_{\text{ds}} = 100$, and $V_{\text{ctrl}} = 0.2 \text{ V}$.

(a) What's m in the bias circuit?

(b) Calculate the values of r_{in} , r_{out} , r_{ds} , r_{in} , R_{in} , and R_{out} .

(c) Find the open-circuit voltage v_{ctrl}/v_t .

(d) Calculate the value of Q_3 to feed the cascode circuit.

(e) Sketch the low-frequency equivalent circuit of a CS amplifier fed with a signal generated via a voltage-controlled voltage source V_{ctrl} .

(a) If the common-emitter source J_1 is implemented with a cascode circuit like that in Fig. 6.13 with an output resistance of βR_D , find the voltage gain A_{v1} .

(b) Ignoring the small signal swing at the input and at the drain of Q_1 , find the lowest value that R_{L1} should have in order to ensure Q_1 and Q_2 are silencing.

6.98 The cascode transistor can be thought of as providing a "shield" for the input transistor from the voltage variations in the source. To verify this "shielding" property of the cascode, consider the situation in Fig. P6.98. Here we have grounded the input terminal (i.e., reduced it to zero), applied a small change δv to the output node, and denoted the voltage change that results at the drain of Q_1 by δv_1 . By what factor is δv_1 smaller than δv ?

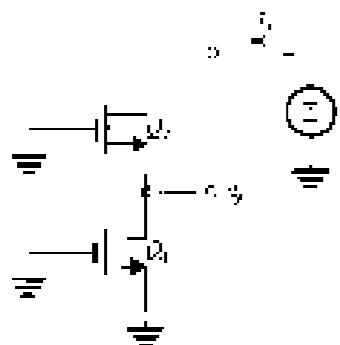


FIGURE P6.98

6.99 In this problem we investigate whether, in a transconductance cascading, we can simply increase the drain of chapter 6 of the FETs (Fig. 6.7). Specifically, we wish to compare the two circuits shown in Fig. P6.99(b) and (c). The circuit in Fig. P6.99(b) is a CS amplifier in which the channel length has been quadrupled relative to that of the original CS amplifier in Fig. P6.99(c) while the drain bias current (see Item 2a) is constant.

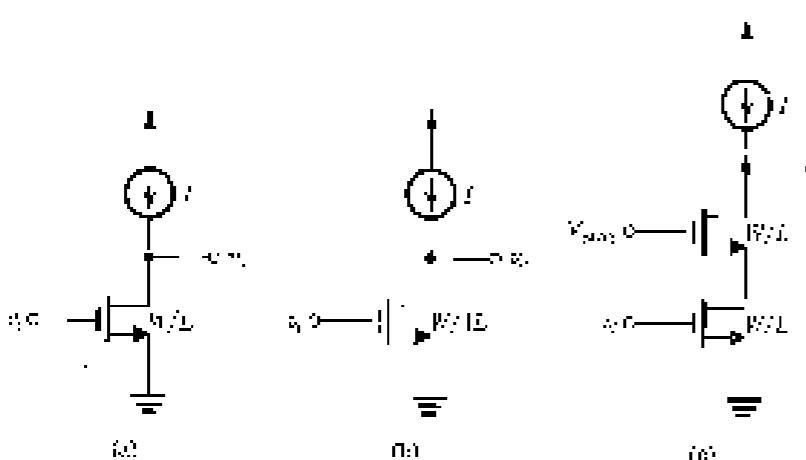


FIGURE P6.99

(a) Show that for the drain of Q_2 it is possible that if the aging current η_2 is half that of the original chapter 6, and β_2 is double that of the initial condition.

(b) Compute these values in terms of the cascade current J_1 (Fig. 6.99(c)), which is operating at the same drain current as the same minimum voltage requirement of the drain in the circuit of Fig. P6.99(b).

6.100 (a) Consider a CS stage having $C_{gs} = 0.2 \text{ pF}$, $R_{ds} = R_s = 20 \text{ k}\Omega$, $\eta_1 = 2 \text{ mV/V}$, $C_{ss} = 3 \text{ pF}$, C_s (including $C_{gd} = 1 \text{ pF}$, $C_{ds} = 0.2 \text{ pF}$, and $r_o = 20 \text{ k}\Omega$). Find the low-frequency gain A_{v1} and estimate f_a using open-circuit time constants. Hence determine the gain-bandwidth product.

(b) The CG stage is cascaded with the CS in series in (a) to create a cascade amplifier. Use the new values of A_{v1} , f_a , and f_{ad} to calculate the product. Assume R_L remains unchanged and $\beta = 10$.

6.101 It is required to design a cascode amplifier to provide a gain of 50 dB when driven with a low-noise source (generator) and utilizing NMOS transistors for which $V_g = 10 \text{ V}$, $n_s C_{ss} = 100 \text{ pF/V}^2$, $W/L = 10$, $C_{gd} = 0.1 \text{ pF}$, and $C_{ds} = 1 \text{ pF}$. Assuming that $R_s = R_{ds}$, determine the drain-to-gate voltage and the drain current at which the NMOSFETs should be operated. Neglect the body effect. Is the drain-to-gate voltage and the drain current. If the cascode capacitor is removed and its voltage unchanged, what will the drain become? The result is different than what can be inferred from Fig. 6.28. Be sure to show.

6.102 Consider a bipolar cascode amplifier in which the current-sink load is implemented with a circuit having an output resistance of βR_D . Let $\beta = 100$, $|V_g| = 100 \text{ V}$, and $I = 0.1 \text{ mA}$. Find R_{L1} , G_{v1} , ω_{ad} , and ω_{ad} . Also, find the gain of the CG stage.

6.103 Consider a bipolar cascode amplifier biased at a current of 1 mA. The transistor model has $\beta = 100$, $r_o = 100 \text{ k}\Omega$, $C_{gd} = 14 \text{ pF}$, $C_{ds} = 2 \text{ pF}$, $C_{ss} = 0$, and $r_s = 50 \text{ }\Omega$. The amplifier

is fed with a signal source having $R_{in} = 5 \text{ }\Omega$. The load is a resistor $R_L = 5 \text{ k}\Omega$. Find the low-frequency gain A_{v1} and estimate the value of the 3-dB corner frequency f_a .

6.104 (a) It is possible to obtain the frequency response of a bipolar cascode amplifier in the case that r_s can be neglected.

(a) Redraw Fig. 6.42 and use the sum-of-the-squares formula to estimate ω_a for the amplifier with $I = 1 \text{ mA}$, $C_{gd} = 1 \text{ pF}$, $C_{ds} = 1 \text{ pF}$, $C_{ss} = C_{gd} = 0$, $\beta = 100$, and $r_s = 0$ in the following two cases:

- (i) $R_{L1} = 1 \text{ k}\Omega$,
- (ii) $R_{L1} = 50 \text{ }\Omega$.

6.105 Design the circuit in Fig. 6.44 to provide an output current of $100 \mu\text{A}$. Use $V_{DD} = 3 \text{ V}$, and assume the PMOS transistors to have $n_s C_{ss} = 50 \text{ pF/V}^2$, $V_g = 6.5 \text{ V}$, and $V_{th} = 5 \text{ V}$. The central source is to have the widest possible bandwidth and thus will have negligible effect on ω_a . It also follows that at the frequencies of interest, the gain from the base to the collector of Q_1 will be $-n_s \beta_1 \approx -1$. Use this to find the resistance to the input of Q_1 and hence show that the gain measured at the input node will vary at frequency

$$\omega_a = \frac{2 \pi V_{DD}}{I_{SS} (C_{ss} + C_{gd})}$$

Then show that the pole introduced at the output node will have a LC quality.

$$\omega_p = \frac{1}{I_{SS} R_{L1} (C_{ss} + C_{gd})}$$

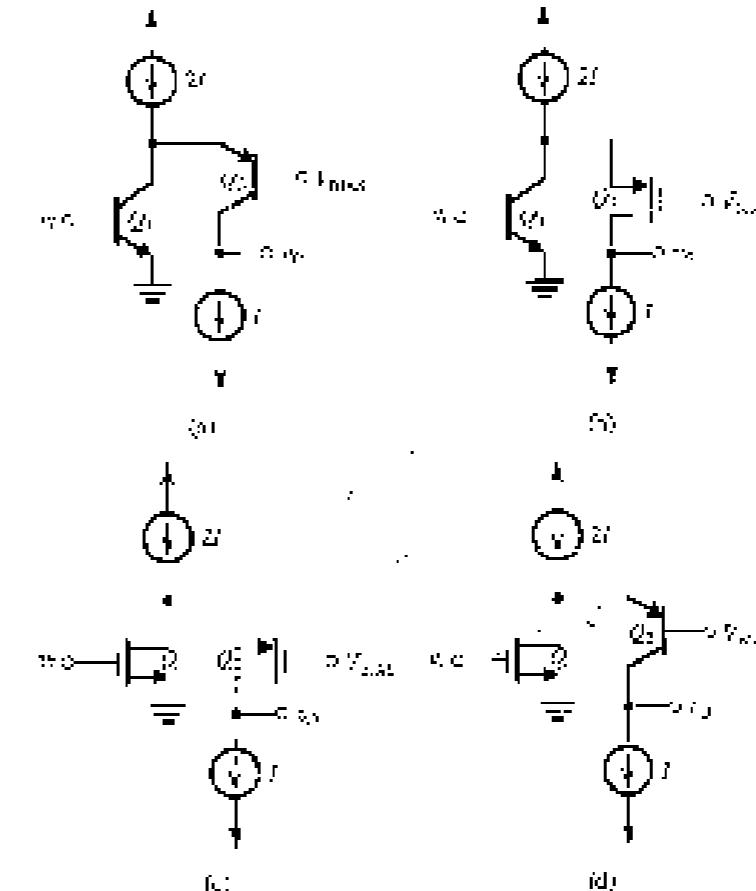


FIGURE P6.107

$V_{DD} = 5 \text{ V}$, and $|V_{GS}| = 0.6 \text{ V}$. Assume $I = 100 \mu\text{A}$ and $V_{DS} = -1 \text{ V}$. To assume that the output is a dependent current source, it is equal to the input current i_1 with a connected diode. Current-source β should be assumed to be ideal. For which results find:

- the bias current i_1 .
- the voltage at the node between Q_1 and Q_2 (assume $V_{DD} = 5.7 \text{ V}$).
- g_m and r_o for each device.
- the maximum allowable value of R_1 .
- the output resistance.
- the output current.
- the voltage gain.

Does the current-source β have to be a sophisticated one? For this example, what output resistance would reduce the overall gain by 10%?

SECTION 6.6: THE CS AND CE AMPLIFIERS WITH SOURCE (EMITTER) DEGENERATION

6.6.10 A common-source amplifier with $g_m = 2 \text{ mA/V}$, $r_o = 50 \text{ k}\Omega$, $x = 0.2$, and $R_1 = 50 \text{ k}\Omega$ has a 3-dB corner frequency $f_c = 100 \text{ Hz}$. If the source lead, bias R_1 , A_{CS} , A_{CE} , C_s , and the feedback β , that appears between gate and source.

6.6.11 A common-source amplifier has $g_m = 2 \text{ mA/V}$, $r_o = 50 \text{ k}\Omega$, $x = 0.2$, and $R_1 = 50 \text{ k}\Omega$. Find the value of the resistance R_s that is Δ -connected in the source, reduces the 3-dB f_c by a factor of 2 (i.e., which, if connected, $A_{CS}/A_{CE} = \frac{1}{2}$). What is the corresponding value of voltage gain A_{CS}/A_{CE} ?

6.6.12 A CS β -follower is specified to have $g_m = 5 \text{ mA/V}$, $r_o = 50 \text{ k}\Omega$, $C_{os} = 2 \text{ pF}$, $C_{ss} = 0.1 \text{ pF}$, $\beta = 1 \text{ pF}$, $R_{SD} = 20 \text{ k}\Omega$, and $R_s = 40 \text{ k}\Omega$.

(a) Find the low-frequency gain A_{CS} and use operational time constants to estimate the 3-dB frequency f_c . Hence determine the gain-bandwidth product.

(b) If the 3dB-BW is shunted on the source lead, find the new values of $|A_{CS}|$, f_c , and the gain-bandwidth product. Assume $g_{mN} = 2 \text{ mA/V}$.

6.6.13 For the CS amplifier with a source-dependent resistance R_s , show that $R_{SD} \approx R_s$ and $X_1 \approx r_o$.

$$\frac{C_{os}R_s}{k + (k/2)} + C_{os}R_{SD} \left(1 + \frac{r_o}{2 + k} \right) = (k + C_{os})r_o \frac{1 + k}{2 + k}$$

where $k = C_{os} + C_{ss}/R_{SD}$.

6.6.14 It is required to generate both the i^2R_{SD}/R_s and i^2 versus $i = (V_{GS} - g_{mN})R_s$ for a CS amp to be used as a source-degenerated current source R_s . The table shows four series load $\beta = 1, 2, \dots, 10$. The transistor is specified to have $g_m = 2 \text{ mA/V}$, $r_o = 2 \text{ M}\Omega$, $f_c = 40 \text{ Hz}$, $R_2 = 40 \text{ k}\Omega$,

$R_{SD} = 20 \text{ k}\Omega$, $C_{os} = 2 \text{ pF}$, $C_{ss} = 0.1 \text{ pF}$. Use the formula for r_o given in the statement for Problem 6.10, if $f_c = 2 \text{ MHz}$ is required. Find the values needed for R_s and the corresponding r_o value of $|A_{CS}|$.

6.6.15 (a) Use the approximate expression in Eq. 6.159 to determine the gain-bandwidth product of a CS amplifier with a source-dependent resistance. Assume $r_o = 0.1 \text{ pF}$ and $R_{SD} = 10 \text{ k}\Omega$.

(b) If a low-frequency gain of 20 V/V is required, what R_s corresponds?

(c) For $g_m = 5 \text{ mA/V}$, $x = 0.2$, $A_{CS} = 100 \text{ V/V}$, and $R_1 = 20 \text{ k}\Omega$, find the maximum value of R_s .

6.6.16 A CS amplifier has a collector bias current of 0.5 mA and an emitter-collector resistance of 100Ω . If $\beta = 100$, $V_{BE} = 0.2 \text{ V}$, and $R_s = r_o$, determine R_{SD} , R_1 , A_{CS} , C_s , f_c , and the overall voltage gain A_{CS}/f_c , when $V_{DD} = 10 \text{ V}$.

6.6.17 In this problem, we investigate the effect of emitter degeneration on the frequency response of a common-emitter amplifier.

(a) Only consider small-signal MOSFET formulas in Equations 6.148 through 6.152 can be adapted to the P-T case to obtain the following:

$$\begin{aligned} R_p &= [(R_2 + 1/k)R_{SD}(1 + G_{os}R_{SD}) + R_1] \\ R_{SD}' &= R_{SD} + R_{SD} \\ R_{SD} &= R_{SD} + R_{SD} + R_{SD}' \\ R_{SD} &= r_o + \frac{R_{SD} + R_{SD}'}{1 + \frac{r_o}{2 + k}} \\ &= r_o \left[\frac{r_o + R_{SD}'}{r_o + R_{SD}'} \right] \end{aligned}$$

(b) Find A_{CS} and f_c of a common-emitter amplifier having $G_{os} = 0.1 \text{ pF}$, $C_{os} = 0.5 \text{ pF}$, $C_{ss} = 2 \text{ pF}$, $g_m = 20 \text{ mA/V}$, $\beta = 100$, $r_o = 200 \text{ k}\Omega$, $r_{SD} = 100 \text{ k}\Omega$, $R_1 = 5.4 \text{ k}\Omega$, and $R_{SD} = 1 \text{ k}\Omega$.

(c) For the following two cases:

- $R_s = 0$.
- $R_s = 200 \text{ }\Omega$.

For simplicity, assume $R_{SD} = R_{SD}'$.

SECTION 6.10: THE SOURCE AND Emitter FOLLOWERS

6.10.16 Consider a source follower for which the NMOS transistor has $I_D = 160 \text{ }\mu\text{A}/\text{V}^2$, $A = 50 \text{ eV}^{-1}$, $x = 0.1$, $R_sL = 100$, and $V_{DD} = 0.5 \text{ V}$.

- What is now the bias current I_D ?
- Calculate the values of V_{GS} , V_{DS} , and V_{SS} .
- Find A_{SF} and R_o .
- What does the voltage gain become when a $1\text{-M}\Omega$ load resistor is connected?

6.11.7 Assume that $g_m = 2 \text{ mA/V}$, $r_o = 1 \text{ M}\Omega$, $V_{DD} = 20 \text{ V}$, $R_{SD} = 20 \text{ k}\Omega$, $R_1 = 20 \text{ k}\Omega$, $C_{os} = 2 \text{ pF}$, $C_{ss} = 0.1 \text{ pF}$, and $f_c = 100 \text{ Hz}$. Find the values needed for R_s and the corresponding r_o value of $|A_{SF}|$.

6.11.8 For the source follower, the term $C_{os}(V_{GS} - V_{DS})$ is usually very small and can be neglected in its determination. If this is true, is the new value of r_o when $R_{SD} \ll R_s$ given that

$$r_o \approx \sqrt{2.5R_{SD}} \sqrt{1 + \frac{C_{os}}{1 + g_m R_{SD}}}$$

where $R_{SD} \ll R_s$ (neglect r_{SD}). For given values of C_{os} , C_{ss} , and R_{SD} , r_o can be increased by reducing the drain-loading R_{SD} . This can be done by increasing $g_m R_{SD}$. Note, however, that $g_m R_{SD}$ cannot exceed $1/g$. Why? What is the corresponding maximum for f_c ? Calculate the value of the maximum f_c for the source follower specified in Problem 6.11.1.

6.11.9 For an emitter follower biased at $I_C = 5 \text{ mA}$ and having $R_{SD} = 10.162$, $R_1 = 1 \text{ k}\Omega$, $V_{DD} = 20 \text{ V}$, $\beta = 100$, $C_{os} = 2 \text{ pF}$, $r_o = 300 \text{ k}\Omega$, and $f_c = 800 \text{ MHz}$, find the low-frequency gain A_{SF} , r_o , and f_c .

6.11.10 For an emitter follower biased at $I_C = 1 \text{ mA}$ and having $R_{SD} = R_1 = 1 \text{ k}\Omega$, and using a transistor specified as the $\beta = 5.0 \times 10^3$, $C_{os} = 0.1 \text{ pF}$, $r_o = 100 \text{ k}\Omega$, $f_c = 100 \text{ Hz}$, and $V_{DD} = 20 \text{ V}$, evaluate the low-frequency A_{SF} , r_o , and the 3-dB frequency f_c .

6.11.11 For the emitter follower shown in Fig. 6.21, find the low-frequency gain and the 3-dB frequency f_c for the following three cases:

- $R_{SD} = 1 \text{ k}\Omega$.
- $R_{SD} = 10 \text{ k}\Omega$.
- $R_{SD} = 100 \text{ k}\Omega$.

(a) $f_c = 100$, $r_o = 10^6 \text{ M}\Omega$, and $C_{os} = 2 \text{ pF}$.

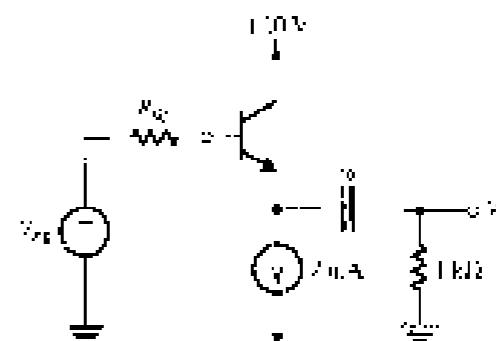


FIGURE PS.121

SECTION 6.11: SOME USEFUL TRANSISTOR PAIRINGS

6.11.22 The transistor in the circuit of Fig. PS.22 has $\beta = 100$, $V_{BE} = 0.2 \text{ V}$, $C_{os} = 0.2 \text{ pF}$, and $C_{ss} = 0.3 \text{ pF}$. At a bias current of $100 \mu\text{A}$, $f_c = 400 \text{ MHz}$. Note that the bias resistors are not shown.

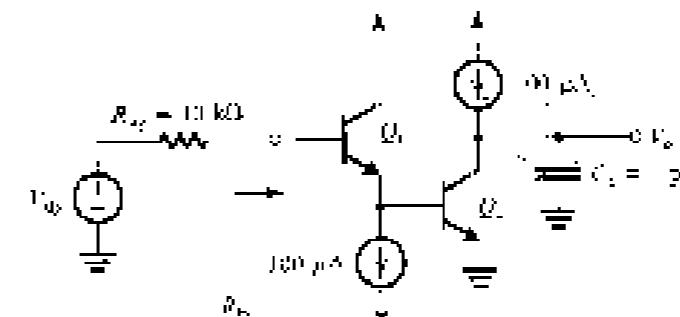
- Find R_{SD} and the drain gain.
- Find an estimate of the upper 3-dB frequency f_c . Which capacitor dominates? Which one is the second dominant signal source?
- What are the effects of increasing the bias currents by a factor of 10?

6.11.23 Consider the BiCMOS structure shown in Fig. PS.23. For HBT, $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, $\beta = 200$, $C_{os} = 0.8 \text{ pF}$, and $C_{ss} = 0.6 \text{ pF}$. The NMOS transistor has $V_t = 1 \text{ V}$, $C_{os} = 2 \text{ mV/V}^2$, and $C_{ss} = 1 \text{ pF}$.

(a) Consider the drain circuit. Neglect the bias current of Q_2 in determining the drain in Q_1 , find the dc bias currents in Q_1 and Q_2 , and show that they are approximately $130 \mu\text{A}$ and $1 \mu\text{A}$, respectively.

(b) Evaluate the total signal parameters of Q_1 and Q_2 at these bias points.

(c) Consider the source, at the dc frequencies, first determine the small-signal voltage gain A_{SF} . (Note that R_s can be



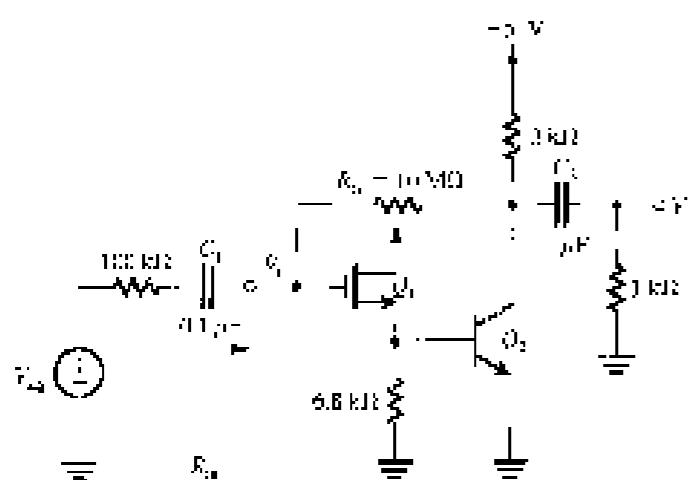


FIGURE P6.123

decreased in this process). Then use Miller's theorem on R_{in} , as done for the amplifier input resistance R_{in} . Finally, determine the overall voltage gain $A_v = V_O/V_{A1}$.

(c) Consider the effect at low frequencies. Determine the frequency of the poles due to C_1 and C_2 , and hence estimate the low-cut frequency f_c .

(d) Consider the circuit at higher frequencies. Use Miller's theorem to replace R_{in} with a resistance of the form β ; the value of the stage will be too large to measure. Use a plotter or the constants to estimate β .

(e) To considerably reduce the effect of R_{in} on R_{in} and hence on amplifier performance, consider the effect of adding another 10-MΩ resistor in series with the existing one and placing a large bypass capacitor between their joint node and ground. What will R_{in} , A_v , and f_c become?

P6.124 The NPNs in the Darlington follower of Fig. P6.124 have $\beta_1 = 100$. If the follower is fed with a source having a

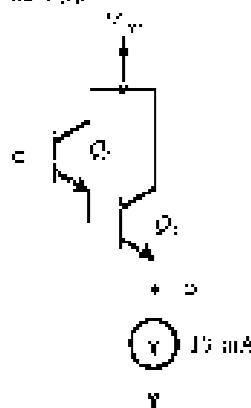


FIGURE P6.124

100-kΩ resistance and a load with > 100 , find the input resistance and the amplifier transistor current (I_A) for best. Also find the overall voltage gain, both theoretical and estimated.

S6.125 For the amplifier in Fig. 6.5(a), let $\beta = 100$, $f_c = 300$ Hz, and $C_1 = 0.5 \mu\text{F}$, and neglect r_s and r_o . Assume that a load resistance of 10 kΩ is connected to the output terminal. If the amplifier is fed with a signal V_{A1} having a source resistance $R_{\text{in}} = 20 \text{ k}\Omega$, find A_v and f_c .

S6.126 Consider the CC-CG amplifier of Fig. 6.5(b); the biasing is $V_b = 5 \text{ mA}$, $C_{11} = 2 \text{ pF}$, $C_{21} = 0.1 \text{ pF}$, $C_{22} = 0.01 \text{ pF}$, $r_s = 1 \text{ pF}$, and $R_{\text{in}} = R_{\text{out}} = 20 \text{ k}\Omega$. Neglecting r_o , the frequency effect and $A_{\text{dc}} = 1/\beta$.

S6.127 In each of the six circuits in Fig. 6.17, let $\beta = 100$, $C_1 = 2 \text{ pF}$, and $f_c = 30$ MHz, and neglect r_s and r_o . Calculate the midband gain A_v and the 3-dB frequency f_c .

SECTION 6.124: CURRENT-MIRROR CIRCUITS WITH IMPROVED PERFORMANCE

S6.128 For the class-A current mirror of Fig. 5.58 with $V_s = 0.5 \text{ V}$, $n_1R_1 = 1 \text{ mV}/\text{A}$, $V_1 = 2 \text{ V}$, $I_{D1} = 30 \mu\text{A}$, and $V_2 = 4.5 \text{ V}$, what value of I_2 results? Specify the output resistance and the minimum overshoot voltage at the output.

S6.129 In a particular cascode current mirror such as that shown in Fig. 5.58, all transistors have $V_s = 0.4 \text{ V}$, $n_1I_{D1} = 200 \mu\text{A}/\text{V}$, $\beta = 1/\mu\text{A}$, and $V_1 = 20 \text{ V}$, while $V_2 = 0.5 \text{ V}$, and $W_1 = W_2 = 40 \mu\text{m}$. The reference current I_{D1} is 25 μA. With output current reversal, what are the voltages at the gates of Q_1 and Q_2 ? What is the lowest voltage at the output for which current mirror operation is possible? What are the values of β_{on} and β_{off} at Q_1 and Q_2 ? What is the output resistance at 1% current?

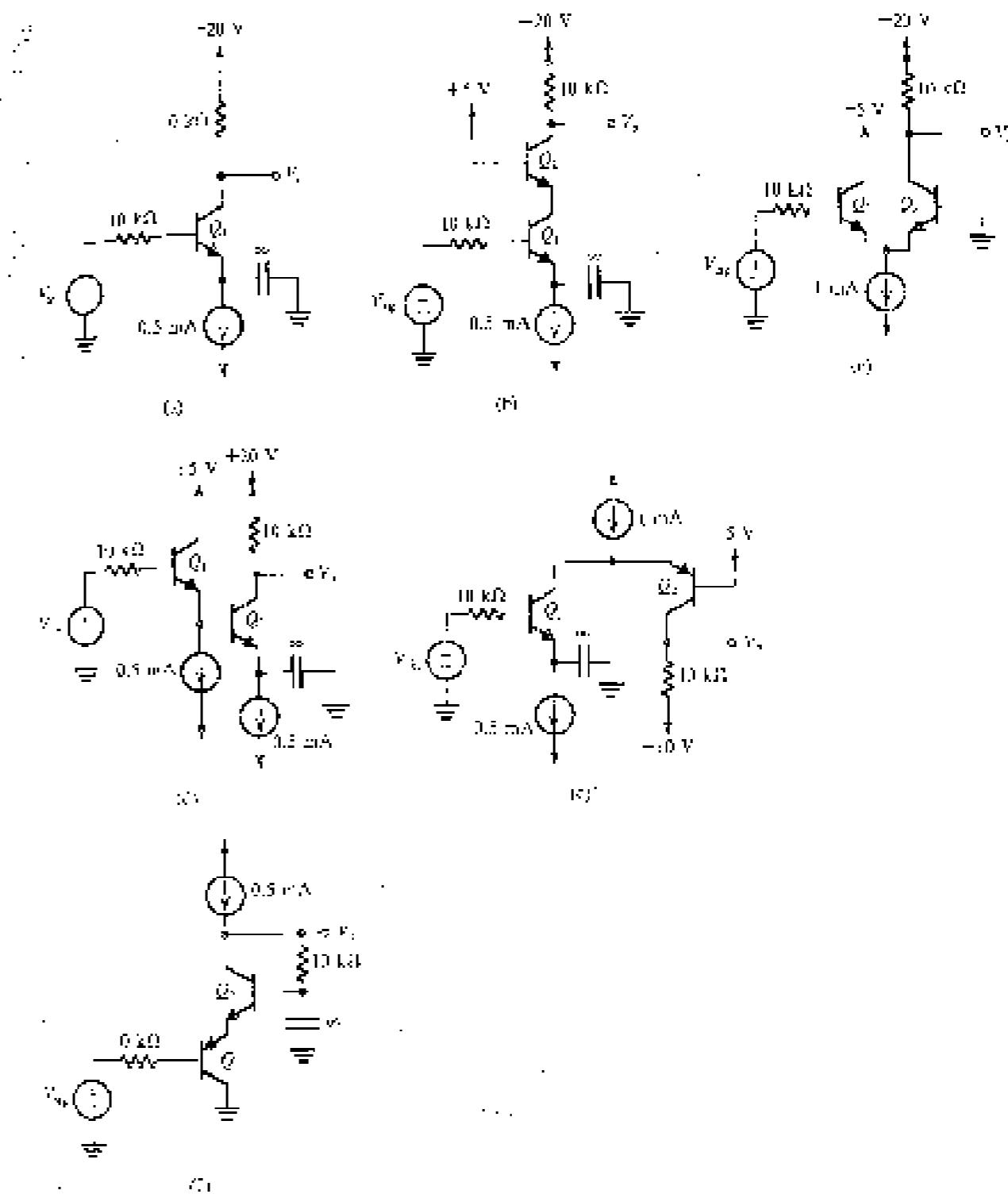


FIGURE P6.127

6.130 If the output resistance of the double cascode can be made to be $R_{\text{out}} = 50$,

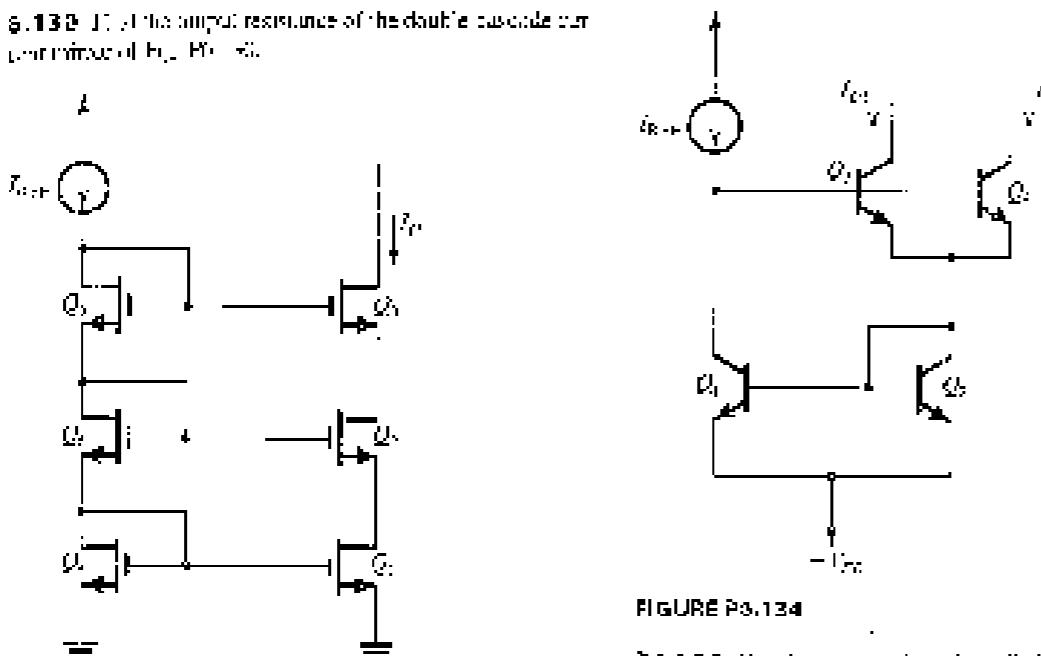


FIGURE P6.130

6.131 For the heterojunction current source of Fig. 6.40, let the bias voltages be matched and supplied by two collector currents of 1 mA at $V_{\text{bb}} = 0.7$ V. The β 's of 1000, and assuming $\beta = 200$, what will the voltage at node 2 be? If $I_{\text{bb}} = 1$ mA, what is the change in V_2 ? What is the value of R_s obtained with $V_b = V_2$? What current I_s is the percentage difference between the required and real values of I_s ? What is the lowest voltage at which p-type current source operation is maintained?

6.132 Extend the current-mirror concept of Fig. 6.9 to n outputs. What is the resulting current transfer ratio between the inputs to each output, I_o/I_{in} ? If the deviation from unity is to be kept at 1%, for best results, what is the maximum possible number of outputs? At $\beta = 100$, $\beta = 10$?

6.133 For the base-emitter-current-mirror circuit of Fig. 6.50, show that the increment in output voltage seen by the reference current source is approximately $3V_{\text{bb}}$. Evaluate R_s for $I_{\text{bb}} = 100 \mu\text{A}$.

6.134 (a) The circuit in Fig. P6.134 is a modified version of the Wilson current mirror. Here the output transistor is split into two matched transistors, Q_1 and Q_2 . Find I_{out} and I_{bb} in terms of I_{bb} . Assume all transistors have $\beta = 100$ and $\beta = 10$.

(b) Use this idea to design a circuit that generates currents of 1 mA, 2 mA, and 4 mA using a reference current source of 2 mA. What are the actual values of the currents generated for $\beta = 50$?

$V_1 = 20$ V, $I_{\text{bb}} = 100 \mu\text{A}$. Neglect V_{bb} (by result 6.1), the circuit is modified as shown in Fig. 6.61(c), what value of I_s yields?

6.141 (a) Utilizing a reference current of 100 μA , design a Wilson current source to provide an output current of 10 μA . Let the BJTs have $V_{\text{bb}} = 0.7$ V at 1 mA current, and assume $\beta = 100$.

(b) If $\beta = 200$ and $V_1 = 100$ V, find the value of the output resistance, and find the change in output current corresponding to a 5-V change in output voltage.

6.142 Design three Wilson current sources, each having a 100- μA reference current, one with a current transfer ratio of 0.8, one with a ratio of 1.0, and one with a ratio of 1.01 \pm 1% for high β . For each, find the output resistance and compare with r_s of the basic unity gain source for which $R_s = 6$ k Ω , $\beta = \infty$ and $V_{\text{bb}} = 0.0$ V.

6.143 The JFET is the circuit of Fig. 26.1-3 has $V_{\text{GS}} = 0.7$ V, $I_s = 100$ and $V_A = 100$ V. Find R_s .

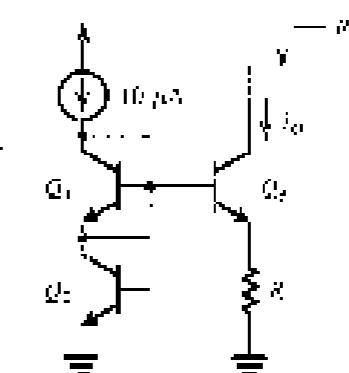


FIGURE P6.143

6.145 (a) The jFET transistor in the circuit of Fig. P6.145 is characterized by its exponential relationship with a drain current I_d , shown for the drain voltage V_d determined by $0.7 = V_d - V_{\text{GS}} - R_s$. Assume Q_1 and Q_2 to be matched and Q_3 ($Q_1 \neq Q_2$) be matched. Find the value of R_s that yields a current $I_d = 10 \mu\text{A}$. For the JFET, $V_{\text{GS}} = 0.7$ V at $I_d = 1 \text{ mA}$.

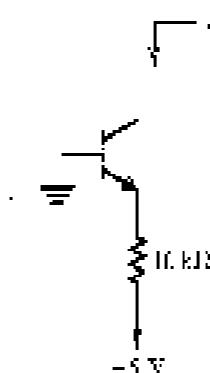


FIGURE P6.145

6.146 (a) For the circuit in Fig. P6.146, assuming BJTs with high β and $V_{\text{bb}} = 0.7$ V at 1 mA. Find the value of R_s that will result in $I_s = 10 \mu\text{A}$.

(b) For the design in (a), find R_s assuming $\beta = 100$ and $V_1 = 100$ V.

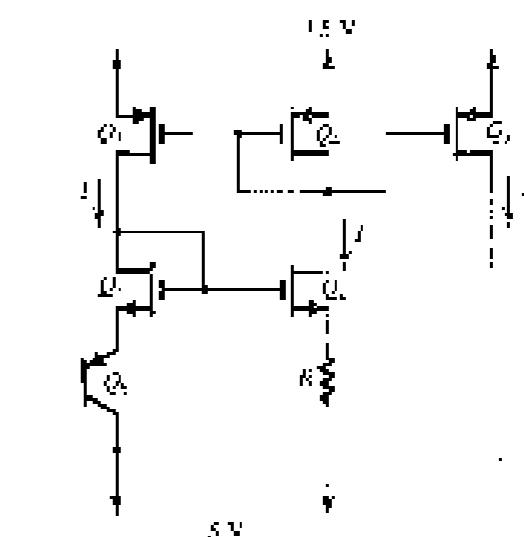


FIGURE P6.146

CHAPTER 7

Differential and Multistage Amplifiers

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INTRODUCTION

The differential-pair or differential-amplifier configuration is the most widely used building block in analog integrated-circuit design. For instance, the input stage of every op-amp is a differential amplifier. Also, the BJT differential amplifier is the basis of a very-high-speed logic circuit family, studied briefly in Chapter 11, called emitter-coupled logic (ECL).

Initially invented for use with vacuum tubes, the basic differential amplifier configuration was subsequently implemented with discrete bipolar transistors. However, it was the advent of integrated circuits that has made the differential pair extremely popular in both bipolar and MOS technologies. There are two reasons why differential amplifiers are so well suited for IC fabrication. First, as we shall shortly see, the performance of the differential pair depends critically on the matching between the two sides of the circuit. Integrated-circuit fabrication is capable of providing matched processes whose parameters track over wide ranges of changes in environmental conditions. Second, by their very nature, differential amplifiers utilize more components (approximately twice as many) than single-ended circuits. Here again, the reader will recall from the discussion in Section 6.1 that a significant

advantage of integrated circuit technology is the availability of large numbers of transistors at relatively low cost.

We assume that the reader is familiar with the basic concept of a differential amplifier as presented in Section 2. Nevertheless, it is worthwhile to re-visit the question: Why differential? Basically, there are two reasons for using differential or difference in single-ended amplifiers. First, differential circuits are much less sensitive to noise and interference than single-ended circuits. To appreciate this point, consider two wires carrying a small differential signal as the voltage difference between the two wires. Now, assume that there is an interference signal that is coupled to the two wires, either capacitively or inductively. As the two wires are physically close together, the interference voltage on the two wires (i.e., here equal) of the two wires and ground will be equal. Since, in a differential system, only the difference signal between the two wires is sensed, it will contain no interference component!

The second reason for preferring differential amplifiers is that the differential configuration enables us to mix the amplifier and its coupled amplifier stages together without the need for bypass and coupling capacitors such as those utilized in the design of discrete-circuit amplifiers (Sections 4.7 and 5.7). This is another reason why differential circuits are also suited for IC fabrication where these capacitors are impossible to fabricate exponentially.

The major topic of this chapter is the differential amplifier in both the MOS and bipolar implementations. As we will see, the design and analysis of differential amplifiers make extensive use of the material on single-stage amplifiers presented in Chapter 6. We will follow the study of differential amplifiers with examples of multistage amplifiers again in both MOS and bipolar technologies. The chapter concludes with two SPICE circuit simulation examples.

7.1 THE MOS DIFFERENTIAL PAIR

Figure 7. shows the basic MOS differential pair configuration. It consists of two matched transistors, Q_1 and Q_2 , whose sources are joined together and biased by a constant-current source I . The latter is usually implemented by a MOSFET circuit of the type studied in Sections 6.3 and 6.12. For the time being, we assume that the current source is ideal and does not influence output resistance. Although each L_{out} is shown connected to the positive output,

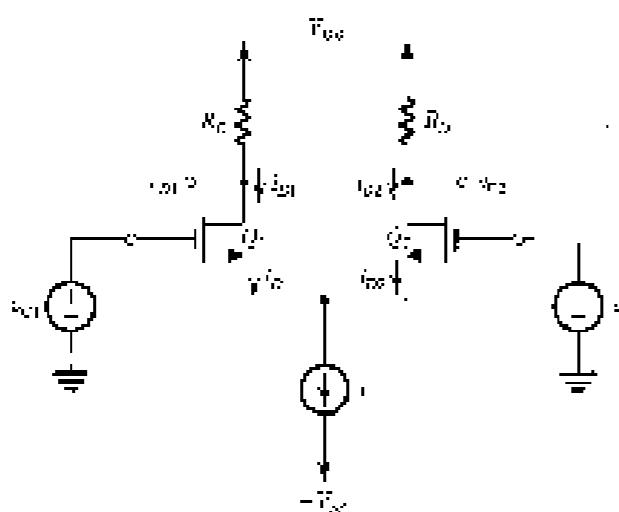


FIGURE 7.1 The basic MOS differential pair circuit.

through a resistor R_{in} to mostextrême current source). Loads are not played, as will be seen shortly. For the time being, however, we will explain the essence of the different load gain operation utilizing simple resistive loads. Whatever type of load is used, it is easier to find the MOSFET's bias under the steady state of operation.

7.1.1 Operation with a Common-Mode Input Voltage

To see how the differential pair works, consider first the case of the two yoke terminals joined together and connected to a voltage v_{cm} , called the common-mode voltage. That is, as shown in Fig. 7.2(a), $v_{\text{in}} = v_{\text{out}} = v_{\text{cm}}$. Since O_1 and O_2 are matched, it follows from symmetry that the current I_{cm} will divide equally between the two transistors. Thus, $i_{\text{D1}} = i_{\text{D2}} = I_{\text{cm}}/2$, and the voltage at the sources, v_{s} , will be

$$D = D_{\text{eff}} - D_{\text{ex}} \quad (7.1)$$

where V_{GS} is the gate-to-source voltage corresponding to a drain current of $I/2$. Neglecting channel-length modulation, V_{GS} and $I/2$ are related by

$$J = \sum_{ij} \rho_{ij}^2 \left(V_{i\mu\nu} - V_{j\mu\nu} \right)^2 \quad (7.21)$$

Fig. 1. Locals of the overdriven voltage V_{over}

$$V_{\text{ext}} = V_{\text{ext}}(r) \quad (1.4)$$

$$\frac{f}{\lambda} = \frac{1}{2} K \left(\frac{F}{f} \right) + \frac{1}{2} \lambda_0 \quad (7.2)$$

$$f_{\text{obs}} \equiv \sqrt{f_{\text{obs}}(1) f_{\text{obs}}(2)} \quad (7.5)$$

the voltage at each alarm will

$$v_{\mu_1} - v_{\mu_2} = V_{\mu\alpha} - \frac{1}{c} S_\alpha \quad (6.6)$$

Thus, the difference in voltage between the two drains will be zero.

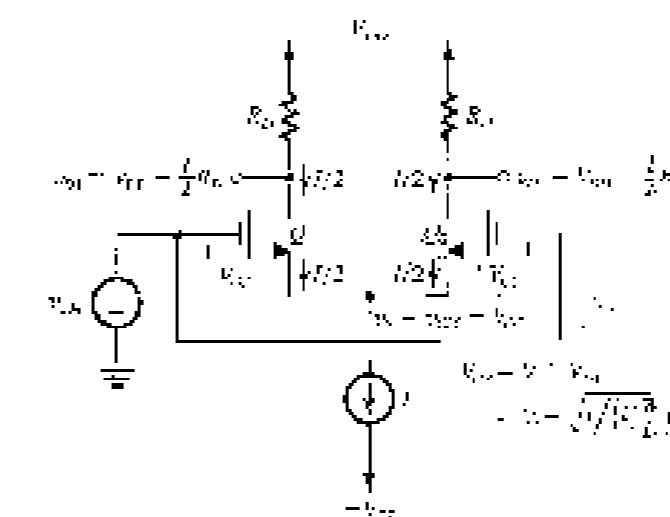


FIGURE 7.2 The NDS differential air velocity approach. A 110 ft/min air flow rate is required.

Now, let us vary the value of the common-mode voltage v_{CM} . Obviously, as long as Q_1 and Q_2 remain in the saturation region, the current I will divide equally between Q_1 and Q_2 and the voltages at the drains will not change. Thus the differential pair does not respond to v_{CM} , it rejects common-mode input signals.

An important specification of a differential amplifier is its input common-mode range, that is, the range of v_{CM} over which the differential pair operates properly. The highest value of v_{CM} is limited by the requirement that Q_1 and Q_2 remain in saturation, thus

$$v_{CM_{max}} = V_s - V_{DS} - \frac{I}{2}R_D \quad (7.1)$$

The lowest value of v_{CM} is determined by the need to allow for a sufficient voltage across the current source for it to operate properly. If a voltage V_{DS} is measured across the current source, then

$$v_{CM_{min}} = -V_{DS} + U_{DS} + V_s + V_{DS} \quad (7.2)$$

EXERCISE

7.1 For the circuit with the drain resistors shown in Fig. 7.3, assume $V_s = 1.57$ V, $V_{DD} = 4.75$ V, $V_{GS1} = 0.2$ mA, and $N_A = 2.5$ kA, and neglect channel length modulation. Find the drain current I and the output voltage v_{DS} .

7.2 Repeat Exercise 7.1.

7.3 Repeat Exercise 7.1.

7.4 What is the highest voltage v_{CM} for which Q_1 and Q_2 remain in saturation?

7.5 Suppose one of the transistors in Fig. 7.3 has a drain-to-source voltage of -0.4 V. Recalculate the drain current I and the output voltage v_{DS} .

7.6 Repeat Exercise 7.1.

7.7 Repeat Exercise 7.1.

7.8 What is the highest voltage v_{CM} for which Q_1 and Q_2 remain in saturation?

7.9 Suppose one of the transistors in Fig. 7.3 has a drain-to-source voltage of -0.4 V. Recalculate the drain current I and the output voltage v_{DS} .

7.10 Repeat Exercise 7.1.

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7.151 Repeat Exercise 7.1.

7.152 Repeat Exercise 7.

will be greater than i_R and the difference output voltage ($v_{O2} - v_{O1}$) will be positive. On the other hand, when i_{R2} is negative, i_{R1} will be lower than i_{R2} , i_{O1} will be smaller than i_{O2} , and correspondingly v_{O1} will be higher than v_{O2} ; in other words, the difference or differential output voltage ($v_{O2} - v_{O1}$) will be negative.

From the above, we see that the differential pair responds to difference-mode or differential input signals by providing a corresponding differential output signal between the two drains. At this point, it is useful to inquire about the value of v_2 that causes the entire drain current $I_{D1} + I_{D2}$ to flow in one of the two transistors. In the positive direction, the happens when v_{21} reaches the value that corresponds to $I_{D1} = I_D$, and v_{22} is reduced to a value equal to the threshold voltage V_T , at which point $v_2 = \pm V_T$. The value of v_2 can be found as:

$$I = \frac{V'_{\text{in}}}{V_{\text{in}}} \frac{W'}{W} \cdot (R_{\text{load}} - R_{\text{in}})$$

$$\begin{aligned} \rho_{\text{eff}} &= V_0 - \sqrt{2}E_0/\Omega_0(2\Omega_0) \\ &\equiv V_0 + \sqrt{2}V_{\text{osc}} \end{aligned} \quad (1.9)$$

where V_{Dg} is the overdrive voltage corresponding to a drain current of $I_D/2$ (Eq. 7.5). Thus, the value of v_g at which the cell bias current I is stepped into Q_1 is

$$\begin{aligned} \text{Polaris } V &= V_{\text{max}} = V_0 \\ &= V_0 + \beta \partial V_{\text{ext}} = V_0 \\ &= \sqrt{2} V_{\text{ext}} \end{aligned} \quad (7.10)$$

If ω_0 is increased beyond $\sqrt{2}\nu_{01}$, β_0 reaches a value equal to 1, ν_{01} remains equal to $(V_1 + \sqrt{2}\nu_{01})$, and ω_0 rises correspondingly, thus keeping Q_1 off. In a similar manner we can show that in the negative direction, as ω_0 reaches $-\sqrt{2}\nu_{01}$, β_0 assumes and Q_2 exhausts the entire time currency. Thus the equilibrium can be located from one transition to the other by varying ω_0 in the range

$$-\sqrt{2} v_{\text{eff}} \leq v_x \leq \sqrt{2} v_{\text{eff}}$$

which defines the range of differential-mode operation. Finally, observe that we have assumed the Q_1 - and Q_2 regions in saturation even when one of them is conducting the entire current [1].

EXERCISE

To use the differential pair as a logic amplifier, we keep the differential input signal v_{in} small. As a result, the current in one of the transistors (i_Q , when v_{in} is positive) will increase by an increment Δi proportional to v_{in} , to $(1/2 + \Delta)$. Simultaneously, the current in the other transistor will decrease by the same amount to become $(1/2 - \Delta)$. A voltage signal $-AV_{in}$ develops across one of the drains and an opposite-polarity signal AV_{in} develops at the other drain. Thus the output voltage taken between the two drains will be $2AV_{in}$, which is an inverted

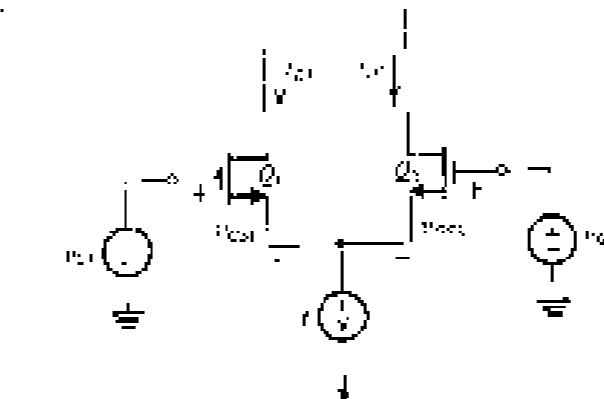


FIGURE 7.5 The ADOS-ETI developmental path for the purpose of deriving the normative standards. Step 1: $\alpha_1 = \alpha_2 = \alpha_3 = 0.5$

the differential input signal v_{D1} . The small-signal operation of the differential pair will be studied in detail in section 3.2.

3.1.3 Large-Signal Operation

We shall now derive expressions for the drain currents i_{D1} and i_{D2} in terms of the input differential signal $v_{D1} = v_{D2} - v_{D3}$. Since these expressions do not depend on the details of the circuit to which the drains are connected, we do not allow these connections in Fig. 7.3; we simply assume that the circuit maintains Q_1 and Q_2 out of the dead region of operation at all times. The following derivation assumes that the dielectric plate is perfectly matched and neglects the self-mixing modulation ($\lambda = \infty$) and the noisy effect.

Table 1: 3D geometric features for drawn symmetric \mathcal{C}^2 Q_1 and $Q_{1,0}$.

$$I_{\text{eff}} = \frac{1}{2} k_s^2 \left(V_0 \cos(\pi x) - V_0 \right)^2 \quad (7.11)$$

$$v_{\text{eff}} = \frac{1}{2} k \zeta \left(\frac{W}{\epsilon} (v_{\text{eff}})^2 - v_{\text{eff}}^2 \right) \quad (7.12)$$

Dividing the square roots of both sides of each of Eqs. (7.11) and (7.12), we obtain

$$\phi_{j,k} = \frac{1}{\sqrt{2}} e^{i \frac{W_j^k}{2} (\alpha_k - \beta_k)} \phi_{j,k} \quad (7.15)$$

$$j_{\alpha}^{\pm} = \frac{i}{\sqrt{2}} \sqrt{\frac{q}{2}} (\psi_{\alpha R} - \psi_{\alpha L}) \quad (3.11)$$

subject to a T(1, 7, 14) [Poisson Eq. (7.13); and subject to

$$B_{\text{eff}} = B_{\text{ext}} + B_{\text{m}} - B_{\text{g}} \approx B_{\text{ext}}$$

Results

$$\sqrt{g_{\mu\nu}} = \sqrt{g_{\mu_1\mu_2}} = \sqrt{\frac{1}{2} k_F \frac{\partial^2 F}{\partial p_1 \partial p_2}} \quad (7.1)$$

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$$(\omega_0 - \omega_0) = 0$$

Equations (7.16) and (7.17) are two equations in the two unknowns i_{Q1} and i_{Q2} and can be solved as follows. Squaring both sides of (7.16) and substituting for $i_{Q1} + i_{Q2} = I$ gives

$$2i_{Q1}i_{Q2} = I - \frac{1}{2}k_s \frac{R_s}{L} V_{DS}$$

Substituting for i_{Q2} from Eq. (7.17) in $i_{Q1} = I - i_{Q2}$ and squaring both sides of the resulting equation provides a quadratic equation in i_{Q1} that can be solved to yield

$$i_{Q1} = \frac{I}{2} \pm \sqrt{\frac{k_s R_s}{L} \left(\frac{V_{DS}}{2} \right)^2 \left[1 - \frac{(V_{DS}/2)^2}{I/k_s R_s} \right]}$$

Now since the increment in i_{Q1} above the bias value of $I/2$) must have the same polarity as the only the root with the "+" sign in the second term is physically meaningful; thus

$$i_{Q1} = \frac{I}{2} + \sqrt{\frac{k_s R_s}{L} \left(\frac{V_{DS}}{2} \right)^2 \left[1 - \frac{(V_{DS}/2)^2}{I/k_s R_s} \right]} \quad (7.18)$$

The corresponding value of i_{Q2} is found from $i_{Q1} + i_{Q2} = I$ as

$$i_{Q2} = \frac{I}{2} - \sqrt{\frac{k_s R_s}{L} \left(\frac{V_{DS}}{2} \right)^2 \left[1 - \frac{(V_{DS}/2)^2}{I/k_s R_s} \right]} \quad (7.19)$$

At the bias (quiescent) point, $V_{DS} = 0$, leading to

$$i_{Q1} = i_{Q2} = \frac{I}{2} \quad (7.20)$$

Correspondingly,

$$V_{GS1} = V_{GS2} = V_{GS} \quad (7.21)$$

where

$$\frac{I}{2} = k_s \frac{R_s}{L} (V_{GS} - V_{GS})^2 = k_s \frac{R_s}{L} V_{GS}^2 \quad (7.22)$$

This relationship enables us to replace $k_s(R_s/L)$ in Eqs. (7.18) and (7.19) with I/V_{GS}^2 to express i_{Q1} and i_{Q2} in the alternative form

$$i_{Q1} = \frac{I}{2} + \left(\frac{I}{V_{GS}} \right) \frac{\sqrt{V_{GS}}}{\sqrt{2}} \left(1 - \frac{\sqrt{V_{GS}/2}}{V_{GS}} \right)^2 \quad (7.23)$$

$$i_{Q2} = \frac{I}{2} - \left(\frac{I}{V_{GS}} \right) \frac{\sqrt{V_{GS}}}{\sqrt{2}} \left(1 - \frac{\sqrt{V_{GS}/2}}{V_{GS}} \right)^2 \quad (7.24)$$

These two equations describe the effect of applying a differential input signal, v_{GS} , on the currents i_{Q1} and i_{Q2} . They can be used to obtain the normalized plots i_{Q1}/I and i_{Q2}/I versus v_{GS}/V_{GS} , shown in Fig. 7.6. Note that at $v_{GS} = 0$, the two currents are equal to $I/2$. Making v_{GS} positive causes i_{Q1} to increase and i_{Q2} to decrease by equal amounts so as to keep the sum constant, $i_{Q1} + i_{Q2} = I$. The current is steered entirely into Q_1 when v_{GS} reaches the value $\sqrt{2}V_{GS}$, as we found out earlier. For v_{GS} negative, identical statements can be made by interchanging i_{Q1} and i_{Q2} . In this case, $v_{GS} = -\sqrt{2}V_{GS}$ steers the current entirely into Q_2 .

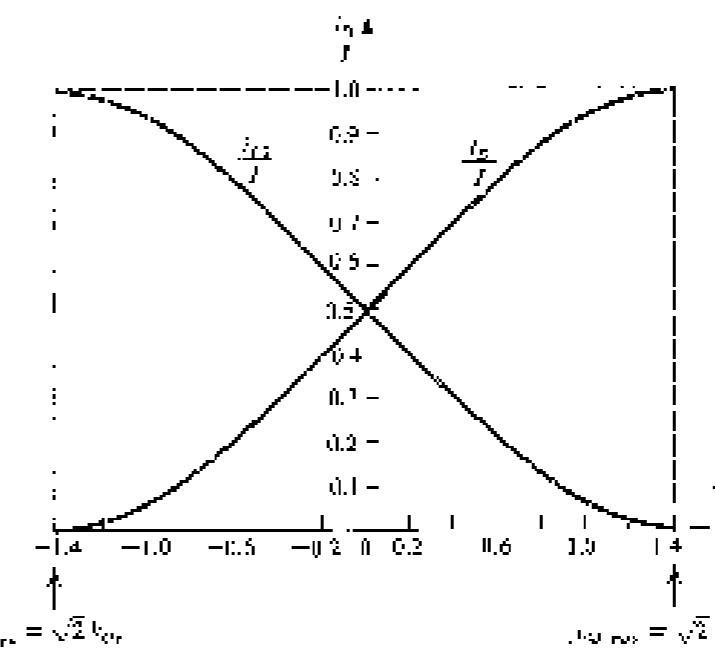


FIGURE 7.6 Normalized plots of the currents in a MOSFET differential pair. Note that V_{GS} is the overdrive voltage at which Q_1 and Q_2 operate when v_{GS} is being varied from its value at $I/2$.

The transfer characteristics of Eqs. (7.23) and (7.24) and Fig. 7.6 are obviously nonlinear. Due to due to the term involving v_{GS} , since we are interested in obtaining linear amplification from the differential pair, we will strive to make this term as small as possible. For a given value of V_{GS} , the only thing we can do is keep $(V_{GS}/2)$ much smaller than V_{GS} , which is the condition for the small-signal approximation. It results in

$$i_{Q1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS}} \right) \frac{\sqrt{V_{GS}}}{\sqrt{2}} \quad (7.25)$$

$$i_{Q2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS}} \right) \frac{\sqrt{V_{GS}}}{\sqrt{2}} \quad (7.26)$$

which, as expected, indicate that i_{Q1} increases by an increment i_1 and i_{Q2} decreases by the same amount $-i_1$, where i_1 is proportional to the differential input signal v_{GS} .

$$i_1 = \left(\frac{I}{V_{GS}} \right) \frac{\sqrt{V_{GS}}}{\sqrt{2}} \quad (7.27)$$

Recalling from our study of the MOSFET in Chapter 4 and Section 6.2 (refer to Table 6.3), that a MOSFET biased at a current I_0 has a transconductance $g_m = 2I_0/V_{GS}$, we recognize the factor $(2I_0/V_{GS})$ in Eq. (7.27) as g_m of each of Q_1 and Q_2 , which are biased at $I_0 = I/2$. Now, why $i_1 \ll I$? Simply because i_{Q1} divides equally between the two devices with $i_{Q1} = i_1/\sqrt{2}$ and $i_{Q2} = -i_1/\sqrt{2}$, which causes Q_1 to have a current increment i_1 and Q_2 to have a current decrement i_1 . We shall return to the small-signal operation of the MOS differential pair shortly. At this time, however, we wish to return to Eqs. (7.23) and (7.24) and note that linearity can be increased by increasing the overdrive voltage V_{GS} at which each of Q_1 and Q_2 is operating. This can be done by using smaller (M_1/M_2) ratios. The price paid for the increased linearity is a reduction in g_m and hence a reduction in gain. In this regard, we observe that the

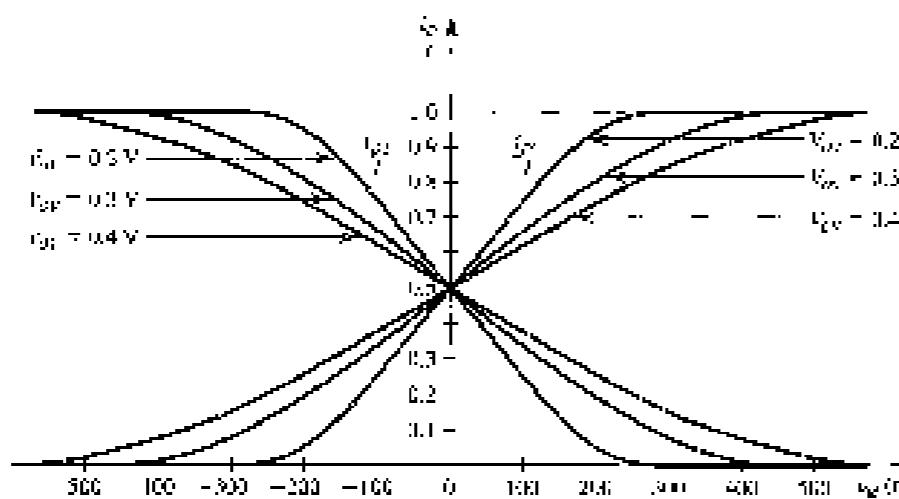
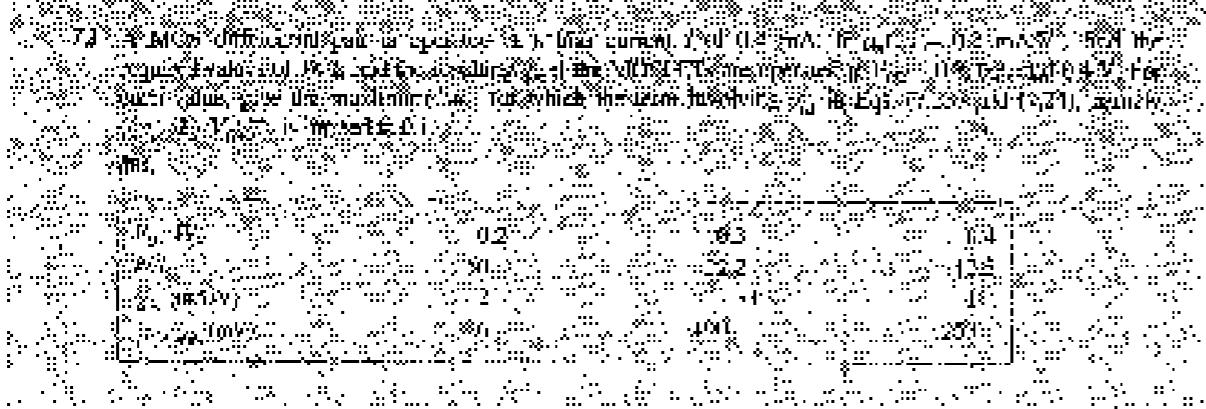


FIGURE 7.7 The linear range of operation of the MOS differential pair can be extended by operating the transistors at higher values of V_{GS} .

uncalibrated plot of Fig. 7.6, though compact, masks this design degree-of-freedom. Figure 7.7 shows plots of the transfer characteristics $I_D/g_s V$ versus v_D for various values of V_{GS} assuming that the current I is kept constant. These graphs clearly illustrate the linearity-transconductance trade-off obtained by changing the value of V_{GS} . The linear range of operation can be extended by operating the MOSFETs at a higher V_{GS} (by using smaller R_{DS} ratios) at the expense of reducing g_s and hence the gain. This trade-off is based on the assumption that the bias current I is kept constant. The bias current can, of course, be increased to obtain a higher g_s . The expense for doing this, however, is increased power dissipation, a serious limitation in IC design.

EXERCISE



7.2 SMALL-SIGNAL OPERATION OF THE MOS DIFFERENTIAL PAIR

In this section we build on the understanding gained of the basic operation of the differential pair and consider in some detail its operation as a linear amplifier.

7.2.1 Differential Gain

Figure 7.8(a) shows the MOS differential amplifier with input voltages

$$v_{in} = v_{GS1} - v_{GS2} \quad (7.28)$$

$$v_{out} = V_{CM} + \frac{1}{2} v_{in} \quad (7.29)$$

Here, V_{CM} denotes a common-mode dc voltage within the linear conduct-mode range of the differential amplifier. It is needed in order to set the dc voltage of the MOSFET gates.

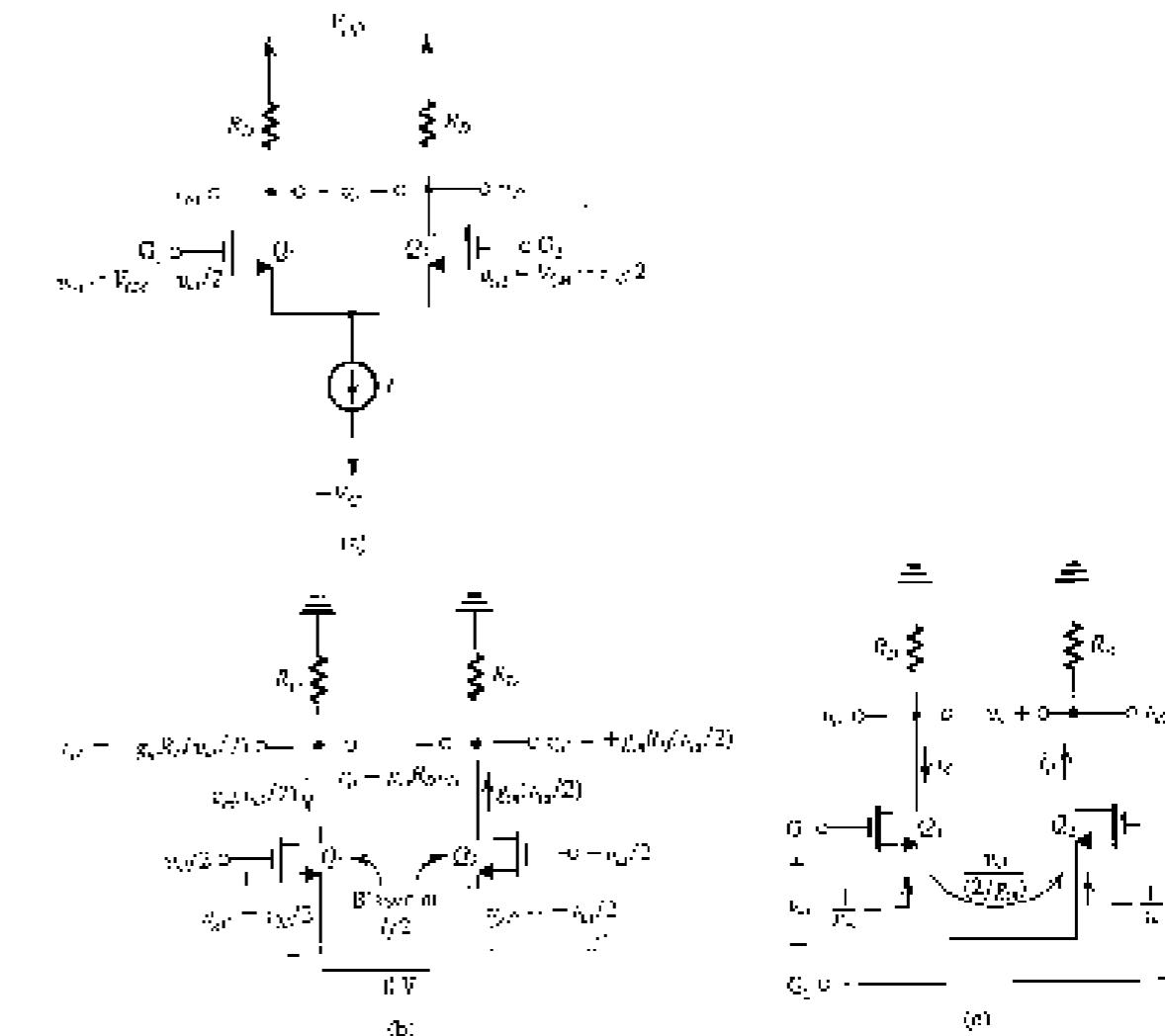


FIGURE 7.8 Small-signal analysis of the MOS differential pair amplifier. (a) The circuit with a common-mode voltage applied to set the dc bias voltage of the gates and $v_{in} = v_1 - v_2$ applied in a 1:1 (differential or balanced) manner. (b) The circuit required for small-signal analysis. (c) An alternative way of looking at the small-signal model of the circuit.

Typically V_{DD} is at the middle value of the power supply. Thus, for our case, where two complementary supplies are utilized, V_{DD} is typically 0 V.

The differential input signal v_{in} is applied in a complementary (or balanced) manner; that is, v_{in} is increased by $v_{in}/2$ and v_{in} is decreased by $-v_{in}/2$. This would be the case, for instance, if the differential amplifier were fed from the output of another differential amplifier stage. Sometimes, however, the differential input is applied in a single-ended fashion, as we saw earlier in Fig. 7.4. The difference in the performance resulting is too subtle a topic for our current needs.

As indicated in Fig. 7.8(a) the amplifier output can be taken either between one of the drain nodes or between the two drains. In the latter case, the resulting single-ended outputs v_{o1} and v_{o2} will be twice the sum of the dc voltages at the drains ($V_{DD} - R_D$). This is not the case when the output is taken between the two drains; the resulting differential output v_o having a 0 V dc component will be entirely a signal component. We will see later that there are other significant advantages to taking the output voltage differentially.

Our objective now is to analyze the small-signal operation of the differential amplifier of Fig. 7.8(a) to determine its voltage gain in response to the differential input signal v_{in} . Toward this end we show in Fig. 7.8(b) the circuit with the power-supply terminals and V_{DD} eliminated. For the time being we will neglect the effect of the MOSFET's r_o , which we have been doing since the beginning of this chapter, amounts to neglecting the body effect (i.e., continue to assume that $\chi = 0$). Finally note that each of Q_1 and Q_2 is biased at a dc current of $I/2$ and is operating at an overdrive voltage V_{ov} .

From the symmetry of the circuit as well as because of the balanced manner in which v_{in} is applied, we observe that the signal voltage at the gate-source connection must be zero acting as a sort of virtual ground. Thus Q_1 has a gate-to-source voltage signal $v_{g1s} = v_{in}/2$ and Q_2 has $v_{g2s} = -v_{in}/2$. Assuming $r_{ds}/2 \ll V_{ov}$, the condition for the small-signal approximation, the changes resulting in the drain currents of Q_1 and Q_2 will be proportional to v_{g1s} and v_{g2s} , respectively. Thus Q_1 will have a drain current increment $i_{d1}(v_{in}/2)$ and Q_2 will have a drain current decrement $i_{d2}(v_{in}/2)$, where g_s denotes the equal transconductances of the two devices.

$$g_s = \frac{2I}{V_{ov}} = \frac{2(I/2)}{V_{ov}} = \frac{I}{V_{ov}} \quad (7.30)$$

These results correspond to those obtained earlier using the large-signal transfer characteristics and imposing the small-signal condition [Eqs. (7.25) to (7.27)].

It is useful at this point to observe again that a signal ground is established at the source terminals of the transistors without resorting to the use of a large bypass capacitor, clearly a major advantage of the differential-pair configuration.

The essence of differential-pair operation is that it provides complementary current signals in the drains; what we do with the resulting pair of complementary current signals is, in a sense, a separate issue. Here, of course, we are simply passing the two current signals through a pair of matched resistors, R_D , and thus obtaining the drain voltage signals

$$v_{o1} = -i_{d1} \frac{R_D}{2} \quad (7.31)$$

and

$$v_{o2} = +i_{d2} \frac{R_D}{2} \quad (7.32)$$

If the output is taken in a single-ended fashion, the resulting gain becomes

$$\frac{v_o}{v_{in}} = \frac{1}{2} g_s R_D \quad (7.33)$$

or

$$\frac{v_o}{v_{in}} = \frac{1}{2} g_s R_D \quad (7.34)$$

Alternatively, if the output is taken differentially, the gain becomes

$$a_{12} = \frac{v_{o1} - v_{o2}}{v_{in}} = g_s R_D \quad (7.35)$$

Thus, another advantage of taking the output differentially is an increase in gain by a factor of 2 (0 dB). It should be noted, however, that although differential outputs are preferred, a single-ended output is needed in some applications. We will have more to say about this later.

An alternative and useful way of viewing the operation of the differential pair in response to a differential input signal v_{in} is illustrated in Fig. 7.8(c). Here we are making use of the fact that the resistance between gate and source of a MOSFET, looking into the source, is $1/g_s$. As a result between G_1 and G_2 we have a total resistance, in the source shunt, of $2/g_s$. It follows that we can obtain the current i_o simply by dividing v_o by $2/g_s$, as indicated in the figure.

Effect of the MOSFET's r_o . Next we refine our analysis by considering the effect of the finite output resistance r_o of each of Q_1 and Q_2 . As well, we make the realistic assumption that the drain current source I has a finite output resistance R_{DS} . The resulting differential-pair circuit, prepared for small-signal analysis, is shown in Fig. 7.9(a). Observe that the circuit remains perfectly symmetric, and as a result the voltage signal at the common source terminal is zero.

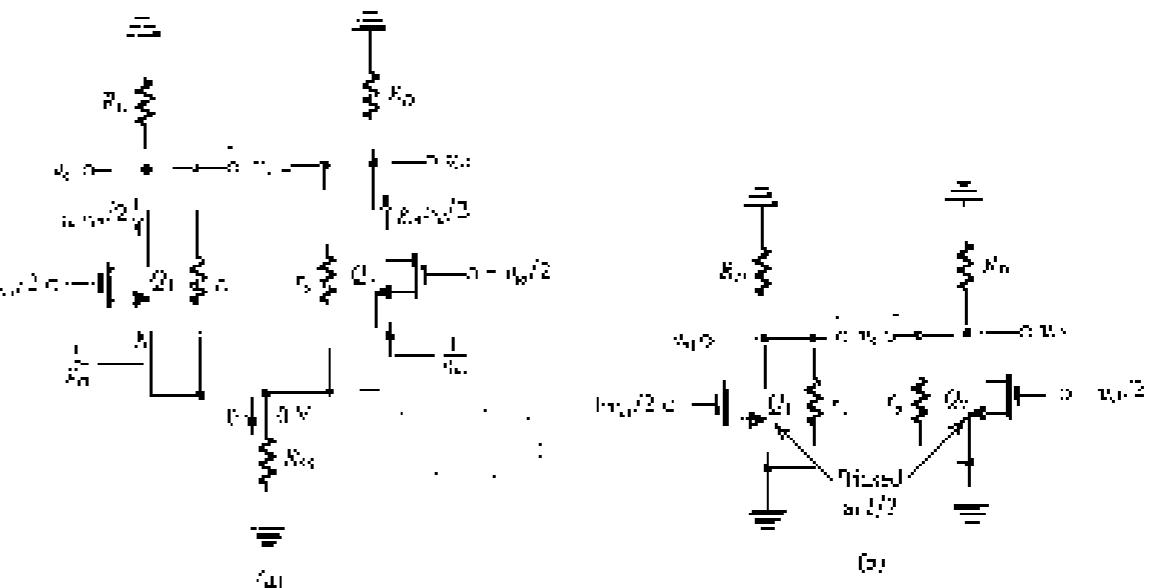


FIGURE 7.9 (a) MOS differential amplifier with r_o and R_{DS} taken into account. (b) Equivalent circuit for determining the differential gain. Both of the two halves of the differential amplifier circuit is a common source amplifier, known as a differential half circuit.

In other words, the mismatch in R_D causes the common-mode input signal v_{in} to be converted into a small output signal; clearly an undesirable situation. Equation (7.49) indicates that the common-mode gain will be

$$A_{CM} = -\frac{\Delta R_D}{2R_M} \quad (7.51)$$

which can be expressed in the alternative form

$$A_{CM} = -\frac{K_1}{2R_M} \left(\frac{\Delta R_D}{R_D} \right) \quad (7.52)$$

Since the mismatch in R_D will have a negligible effect on the differential gain, we can write

$$A_d = A_d R_D \quad (7.53)$$

and combining Eqs. (7.51) and (7.53) to obtain the CMRR resulting from a mismatch ($\Delta R_D/R_D$) is

$$CMRR = \frac{A_d}{A_{CM}} = (2R_M R_D) \left(\frac{\Delta R_D}{R_D} \right) \quad (7.54)$$

EXERCISE 7.10

Derive the expression for the CMRR resulting from a mismatch in the drain resistances R_D .

Effect of g_m Mismatch on CMRR. Next we inquire into the effect of a mismatch between the values of the transconductances g_m of the two MOSFETs on the CMRR of the differential pair. Since the circuit is no longer matched, we cannot employ the common-mode half-circuit. Rather, we refer to the circuit shown in Fig. 7.11, and write:

$$i_{S1} = g_m v_{DS1} \quad (7.55)$$

$$i_{S2} = g_m v_{DS2} \quad (7.56)$$

Since $v_{DS} = v_{DS1}$ we can combine Eqs. (7.54) and (7.55) to obtain

$$\frac{i_{S1}}{i_{S2}} = \frac{g_{m1}}{g_{m2}} \quad (7.57)$$

The two drain currents sum together at R_D to provide

$$v_{DS} = i_{S1} + i_{S2} R_D$$

Thus

$$i_{S1} + i_{S2} = \frac{v_{DS}}{R_D} \quad (7.58)$$

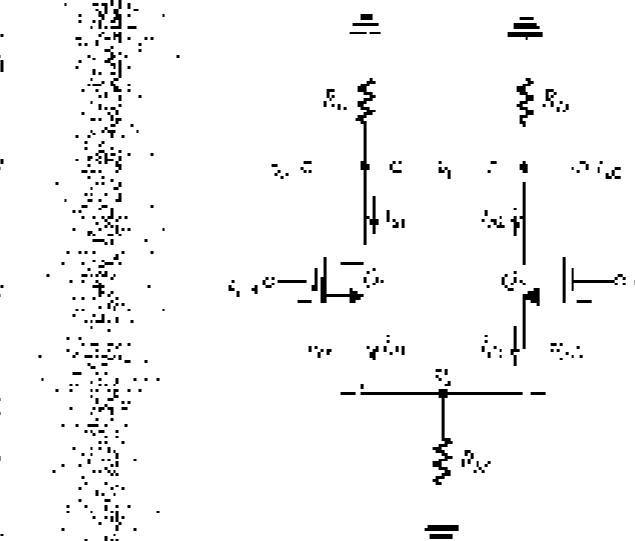


FIGURE 7.18 Analysis of the MOS Differential pair to determine the common-mode gain resulting from a mismatch in the g_m values of Q_1 and Q_2 .

Since Q_1 and Q_2 are in effect operating as source followers with a source resistance R_{DS} that is typically much larger than R_D ,

$$i_{S1} \approx i_{DS1} \quad (7.59)$$

leading us to write Eq. (7.57) as

$$i_{S1} = i_{DS1} = \frac{v_{DS1}}{R_{DS}} \quad (7.60)$$

We can now combine Eqs. (7.56) and (7.60) to obtain

$$i_{DS1} = \frac{g_{m1} v_{DS1}}{(g_{m1} + g_{m2}) R_{DS}} \quad (7.61)$$

$$i_{DS2} = \frac{g_{m2} v_{DS1}}{(g_{m1} + g_{m2}) R_{DS}} \quad (7.62)$$

If g_{m1} and g_{m2} exhibit a small mismatch Δg_{m1} (i.e., $g_{m1} - g_{m2} = \Delta g_{m1}$), we can assume that $|g_{m1} - g_{m2}| \leq 2g_{m0}$, where g_{m0} is the nominal value of g_{m1} and g_{m2} , thus

$$i_{DS1} = \frac{g_{m1} v_{DS1}}{2g_{m0} R_{DS}} \quad (7.63)$$

$$i_{DS2} = \frac{g_{m2} v_{DS1}}{2g_{m0} R_{DS}} \quad (7.64)$$

The differential output voltage can now be found as

$$\begin{aligned} v_{DS} - v_{DS1} &= -i_{DS1} R_D - i_{DS2} R_D \\ &= R_D (i_{DS1} - i_{DS2}) = \frac{\Delta g_{m1} K_1}{2g_{m0} R_{DS}} v_{DS1} \end{aligned}$$

from which the common-mode gain can be obtained as

$$A_{cm} = \frac{g_f R_D}{1 + g_f R_D} \left(\frac{R_{2L}}{R_{2U}} \right) \quad (7.64)$$

Since the g_m mismatch will have a negligible effect on A_{cm} ,

$$\phi_0 = g_f R_D \quad (7.65)$$

and the CMRR resulting will be

$$CMRR = \frac{A_d}{A_{cm}} = (2g_m R_{2L}) / (\phi_0) \quad (7.66)$$

The similarity of this expression to that resulting from the R_{2L} mismatch rule (Eq. 7.53) should be noted.

EXERCISE

- 7.10. An NMOS differential-pair circuit has two matched transistors, Q_1 and Q_2 , whose emitters are joined together and biased by a constant-current source I . The latter is usually implemented by a transmission-gate circuit of the type studied in Sections 6.3 and 6.12. Although each collector is shown connected to the positive supply voltage V_{DD} , through a resistance R_C , this connection is not essential to the operation of the differential pair. That is, in some implementations the two collectors may be connected to other transistors rather than to resistive loads. This is essential, however, that the collector circuits be such that Q_1 and Q_2 never enter saturation.

7.3 THE BJT DIFFERENTIAL PAIR

Figure 7.12 shows the basic BJT differential-pair configuration. It is very similar to the MOSFET circuit and consists of two matched transistors, Q_1 and Q_2 , whose emitters are joined together and biased by a constant-current source I . The latter is usually implemented by a transmission-gate circuit of the type studied in Sections 6.3 and 6.12. Although each collector is shown connected to the positive supply voltage V_{DD} , through a resistance R_C , this connection is not essential to the operation of the differential pair. That is, in some implementations the two collectors may be connected to other transistors rather than to resistive loads. This is essential, however, that the collector circuits be such that Q_1 and Q_2 never enter saturation.

7.3.1 Basic Operation

To see how the BJT differential pair works, consider first the case of the two bases joined together and connected to a common-mode voltage v_{cm} . That is, as shown in Fig. 7.13(a),

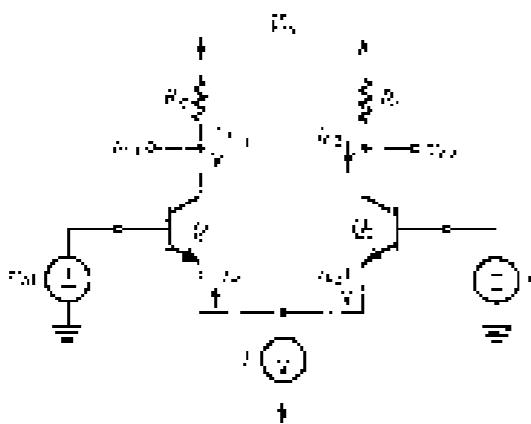


FIGURE 7.12 The basic BJT differential pair circuit.

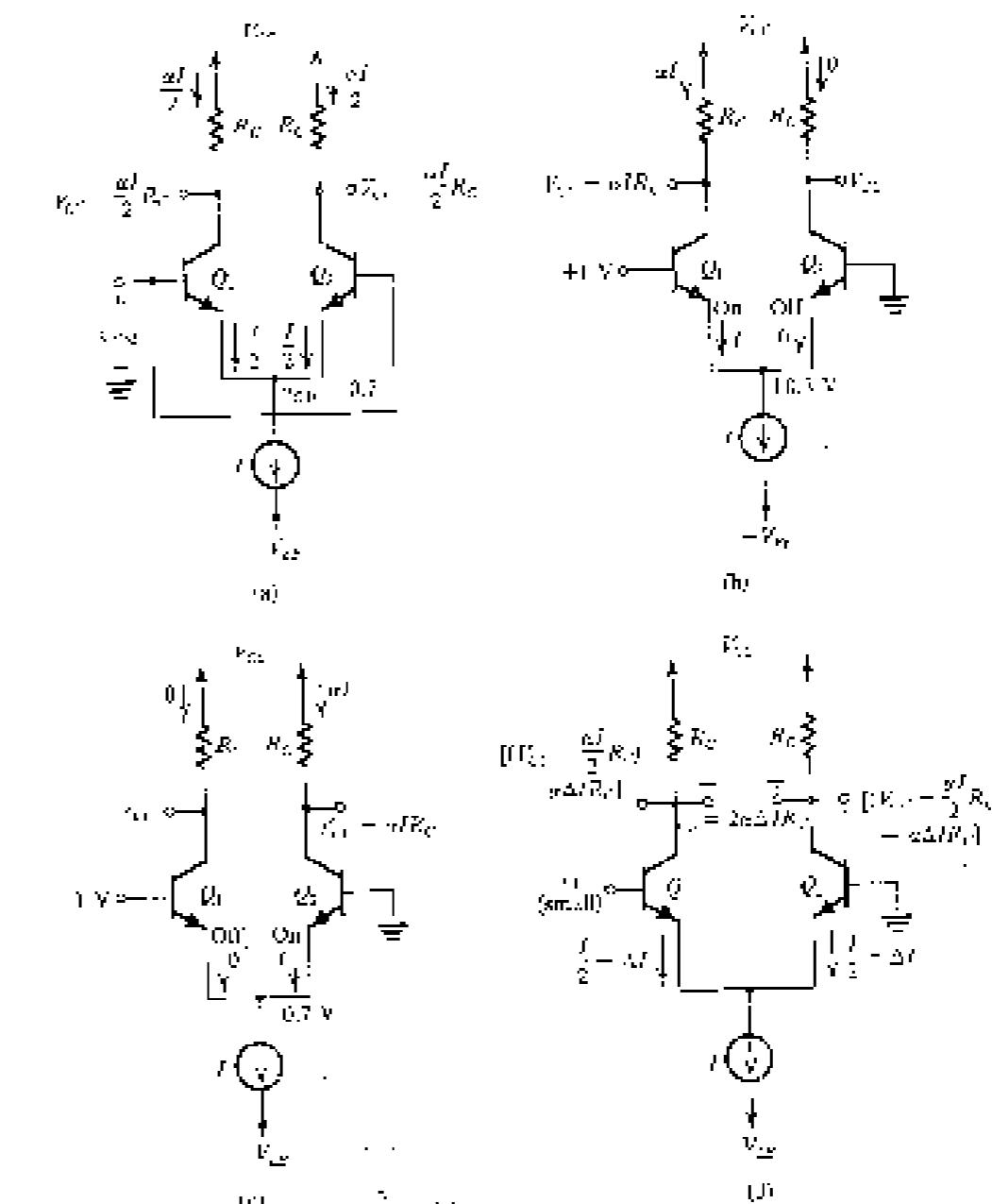


FIGURE 7.13 BJT-level nodes representation of the BJT differential pair. (a) The differential pair with a common-emitter input signal v_{cm} . (b) The differential pair with a charge-difference mode signal. (c) The differential pair with a large difference mode signal of relatively moderate magnitude. (d) The differential pair with a small differential input signal. Note that we have assumed the bias current source I to be ideal (i.e., zero internal resistance). Thus $i_{cm} = I$ is constant with the current i_{Q1} .

$i_{Q1} = i_{Q2} = i_{cm}$. Since Q_1 and Q_2 are matched, and assuming an ideal bias current source I with a finite output resistance, it follows that the current I will remain constant and from symmetry the I 's will divide equally between the two devices. Thus $i_{Q1} = i_{Q2} = I/2$, and the voltage at the emitters will be $v_{ce} = V_{BE}$, where V_{BE} is the base-emitter voltage (assumed in Fig. 7.13a to be

approximately 0.7 V corresponding to an emitter current of $50\text{ }\mu\text{A}$. The voltage across R_{E} will be $V_{\text{CE}} = \frac{1}{2}V_{\text{DD}}$, and the difference in voltage between the two collectors will be zero.

Now let us vary the value of the common-emitter input signal v_{in} . Obviously, so long as Q_1 and Q_2 remain in the active region the current I will still divide equally between Q_1 and Q_2 , and the voltages at the collectors will not change. Thus the differential pair does not respond to (i.e., it rejects) common-mode input signals.

As another experiment, let the voltage v_{in} be set to a constant value, say, zero, by grounding v_{in} , and let $v_{\text{cc}} = -1\text{ V}$ (see Fig. 7.13b). With a bit of reasoning it can be seen that Q_1 will be on and conducting all of the current I and that Q_2 will be off. For Q_1 to be on (with $V_{\text{BE}} = 0.7\text{ V}$), the emitter has to be at approximately 40.3 V , which keeps the EBO of Q_2 reverse-biased. The collector voltages will be $v_{\text{c}_1} = V_{\text{CC}} - \text{e}^{\beta V_{\text{BE}}}$ and $v_{\text{c}_2} = V_{\text{CC}}$.

Let us now change v_{in} to -1 V (Fig. 7.13c). Again with some reasoning it can be seen that Q_2 will turn off, and Q_1 will carry all the current I . The common-emitter will be at -0.7 V , which means that the EBO of Q_1 will be reverse-biased by 0.3 V . The collector voltages will be $v_{\text{c}_1} = V_{\text{CC}}$ and $v_{\text{c}_2} = V_{\text{CC}} + \text{e}^{\beta V_{\text{BE}}}$.

From the foregoing, we see that the differential pair certainly responds to large differential-mode (or differential) signals. In fact, with relatively small difference voltages we are able to steer the entire bias current from one side of the pair to the other. This current-steering property of the differential pair allows it to be used in logic circuits, as will be demonstrated in Chapter 11. Indeed, the reader can easily see that the differential pair implements the single-pole double-throw switch that we employed in the realization of the current-mode inverter of Fig. 1.33.

To use the BJT differential pair as a linear amplifier we apply a very small differential signal (in few millivolts), which will result in one of the transistors conducting a current of $52 \pm 5\text{ }\mu\text{A}$; the current in the other transistor will be $48 \pm 5\text{ }\mu\text{A}$, with β being proportional to the difference input voltage (see Fig. 7.13d). The output voltage taken between the two collectors will be $2\text{mV}/R_{\text{L}}$, which is proportional to the differential input signal v_{d} . The small-signal operation of the differential pair will be studied next in Section 7.3.

EXERCISE

- 7.7 Consider the circuit of Fig. 7.12. Assume that v_{in} is applied to the midpoint of R_{E} .



FIGURE 7.7

7.3.2 Large-Signal Operation

We now present a general analysis of the BJT differential pair of Fig. 7.12. If we denote the voltage at the common-emitter by v_{ce} , the exponential relationship applied to each of the two transistors may be written:

$$i_{\text{c}_1} = \frac{I}{2} e^{\frac{v_{\text{ce}} - V_{\text{BE}}}{2kT}} \quad (7.67)$$

$$i_{\text{c}_2} = \frac{I}{2} e^{\frac{v_{\text{ce}} + V_{\text{BE}}}{2kT}} \quad (7.68)$$

These two equations can be combined to obtain

$$\frac{i_{\text{c}_1}}{i_{\text{c}_2}} = e^{\frac{2(V_{\text{BE}} - v_{\text{ce}})}{kT}} \quad (7.69)$$

which can be manipulated to yield

$$\frac{i_{\text{c}_1}}{i_{\text{c}_1} + i_{\text{c}_2}} = \frac{1}{1 + e^{\frac{2(V_{\text{BE}} - v_{\text{ce}})}{kT}}} \quad (7.70)$$

$$\frac{i_{\text{c}_2}}{i_{\text{c}_1} + i_{\text{c}_2}} = \frac{1}{1 + e^{\frac{2(V_{\text{BE}} - v_{\text{ce}})}{kT}}} \quad (7.71)$$

The circuit imposes the additional constraint

$$i_{\text{c}_1} + i_{\text{c}_2} = I \quad (7.72)$$

Using Eq. (7.72) together with Eqs. (7.69) and (7.70) and substituting $v_{\text{c}_1} = v_{\text{c}_2} = v_{\text{ce}}$ gives

$$i_{\text{c}_1} = \frac{I}{1 + e^{\frac{2(V_{\text{BE}} - v_{\text{ce}})}{kT}}} \quad (7.73)$$

$$i_{\text{c}_2} = \frac{I}{1 + e^{\frac{2(V_{\text{BE}} - v_{\text{ce}})}{kT}}} \quad (7.74)$$

The collector currents i_{c_1} and i_{c_2} can be obtained simply by multiplying the emitter currents (Eq. 7.73) and (7.74) by α , which is normally very close to unity.

The fundamental operation of the differential amplifier is illustrated by Eqs. (7.73) and (7.74). First, note that the amplifier responds only to the difference voltage v_{d} . That is, if $v_{\text{c}_1} = v_{\text{c}_2} = v_{\text{ce}}$ the current I divides equally between the two transistors irrespective of the value of the common-mode voltage v_{cm} . This is the essence of differential-mode operation, which also gives rise to the name.

Another important observation is that relatively small difference voltage v_{d} will cause the current I to flow almost entirely in one of the two transistors. Figure 7.14 shows a plot of the two collector currents (assuming $\alpha = 1$) as a function of the differential input signal. This is a normalized plot that can be used universally. Note that a difference voltage of about 4% ($1-100\text{ mV}$) is sufficient to switch the current almost entirely to one side of the BJT pair. Note that this is much smaller than the corresponding voltage for the MOS pair, 42 mV . The fact that even a small signal can switch the current from one side of the BJT differential pair to the other means that the BJT differential pair can be used as a fast switch. Another reason for the high speed of operation of the BJT differential device as a switch is the nature of the transition saturations. The reader will recall from Chapter 5 that a saturated junction stores charge in its base that must be removed before the device can turn off. Generally it takes several nanoseconds

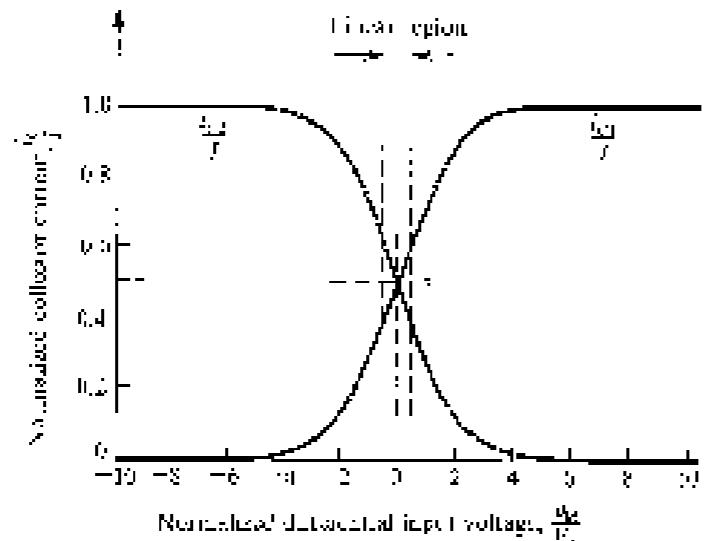


FIGURE 7.14 Transfer characteristics of the BJT differential pair of Fig. 7.12 assuming $\alpha = 1$.

slow inverter. The absence of saturation¹ in the normal operation of the BJT differential pair limits the logic family based on it the fastest form of logic circuits available (see Chapter 11).

The nonlinear transfer characteristics of the differential pair shown in Fig. 7.14 will not be utilized any further in this chapter. Rather, in the following we shall be interested specifically in the application of the differential pair as a small-signal amplifier. For this purpose the difference input signal is limited to less than about $v_{xy}/V_T \approx 1$ (note that we may operate on a linear segment of the characteristics around the midpoints in Fig. 7.14).

Before leaving the large-signal operation of the differential BJT pair we wish to point out an effective technique frequently employed to extend the linear range of operation. It consists of introducing two equal resistances R_s in series with the emitters of Q_1 and Q_2 , as shown in Fig. 7.15(a). The resulting transfer characteristics for three different values of R_s are sketched in Fig. 7.15(b). Observe that expansion of the linear range is obtained at the expense of reduced g_m (which is the slope of the transfer curve at $v_{xy} = 0$) and hence reduced gain. This result should come as no surprise; R_s here is performing in exactly the same way as the emitter resistance R_e does in the CE amplifier with emitter degeneration (see Sect. 6.9.2). Finally, we also note that this linearization technique is in effect the singular counterpart of the technique employed for the MOS differential pair (Fig. 7.7). In the latter case, however, V_{DD} was varied by changing the transistors' V_T /L ratio—a design tool with no counterpart in the BJT

EXERCISE

For the BJT differential pair of Fig. 7.12 find the linearity range if $\alpha = 0.95$ and $R_s = 10\text{ k}\Omega$.

Ans.: $v_{xy}/V_T \in [-1.5, 1.5]$. Hint: The saturation regions are now shifted to $v_{xy}/V_T = \pm 1.5$.

¹ Recall that saturation in a BJT means something completely different than saturation of a MOSFET.

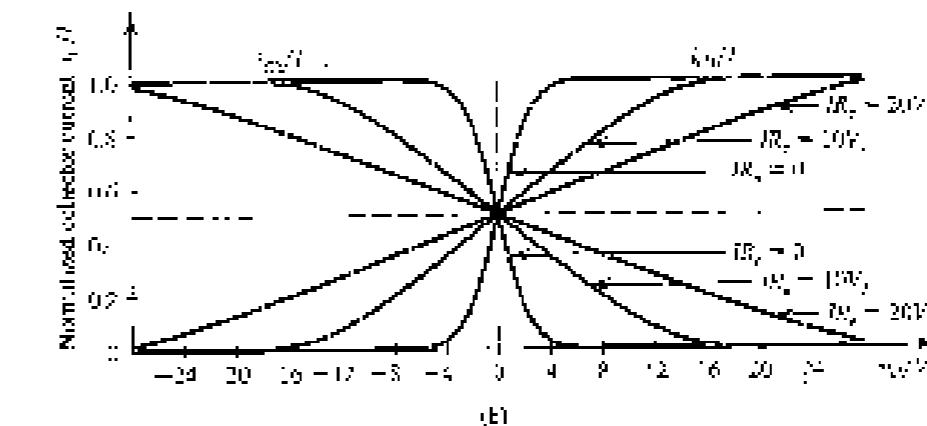
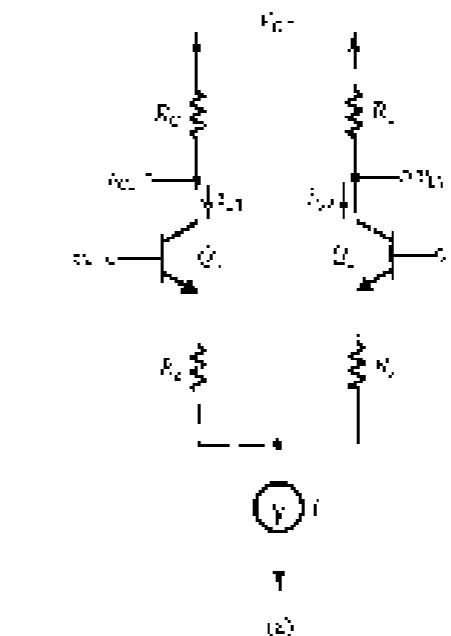


FIGURE 7.15 (a) The circuit characteristics of the BJT differential pair can be linearized (i.e., the linear range of operation can be extended) by inserting resistances in the emitters.

7.3.3 Small-Signal Operation

In this section we shall study the application of the BJT differential pair in small-signal amplification. Figure 7.16 shows the BJT differential pair with a difference voltage signal v_{xy} applied between the two bases. Assumed is that the dc level in the inputs—that is, the common-mode input voltage—has been somehow established. For instance, one of the two input terminals can be grounded and v_{xy} applied to the other input terminal. Assuming, for y , the differential amplifier may be fed from the output of another differential amplifier. In the latter case, the voltage at one of the input terminals will be $v_{xy} + v_o/2$ while at the other input terminal will be $v_{xy} - v_o/2$. We will consider common-mode operation subsequently.

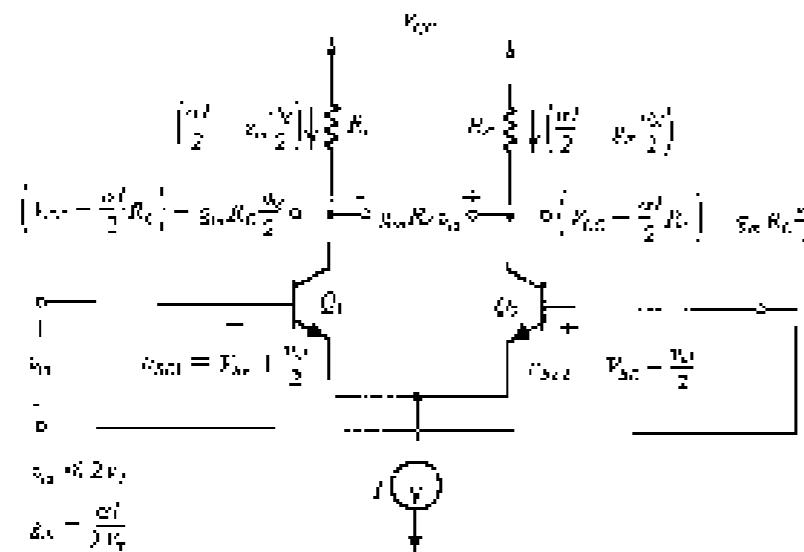


FIGURE 7.16 The currents and voltages in the differential amplifier when a small differential input signal v_{in} is applied.

The Collector Currents When v_{in} Is Applied. For the circuit of Fig. 7.16, we may use Eqs. (7.72) and (7.73) to write

$$i_{C1} = \frac{\alpha I}{1 + e^{-\alpha(V_{be} - i_C)/kT}} \quad (7.74)$$

$$i_{C2} = \frac{\alpha I}{1 + e^{-\alpha(V_{be} + i_C)/kT}} \quad (7.75)$$

Multiplying the numerator and the denominator of the right-hand side of Eq. (7.74) by $e^{\alpha(V_{be} - i_C)/kT}$ gives

$$i_{C1} = \frac{\alpha I e^{\alpha(V_{be} - i_C)/kT}}{e^{\alpha(V_{be} - i_C)/kT} + e^{-\alpha(V_{be} + i_C)/kT}} \quad (7.76)$$

Assume that $V_{be} \approx 2V_T$. We may thus expand the exponential $e^{\alpha(V_{be} - i_C)/kT}$ in a series, and retain only the last two terms:

$$i_{C1} = \frac{\alpha I (1 - \alpha i_C / 2V_T)}{1 - \alpha i_C / 2V_T + 1 - \alpha i_C / 2V_T}$$

Thus

$$i_{C1} = \frac{\alpha I}{2} - \frac{\alpha I \cdot \alpha i_C}{2V_T} \quad (7.77)$$

Similar manipulations can be applied to Eq. (7.75) to obtain

$$i_{C2} = \frac{\alpha I}{2} + \frac{\alpha I \cdot \alpha i_C}{2V_T} \quad (7.78)$$

Equations (7.77) and (7.78) tell us that when $v_{in} = 0$, the bias current I divides equally between the two transistors of the pair. The α -circuit transistor is biased at an emitter current of

$i_1 = \frac{\alpha I}{2} - \frac{\alpha^2 I \cdot \alpha i_C}{2V_T}$ and the β -circuit transistor is biased at an emitter current of $i_2 = \frac{\alpha I}{2} + \frac{\alpha^2 I \cdot \alpha i_C}{2V_T}$. When a "small signal" v_{in} is applied differentially (i.e., between the two bases), the collector current of Q_1 increases by an increment i_1 and that of Q_2 decreases by an equal amount. This ensures that the sum of the total currents in Q_1 and Q_2 remains constant, as constrained by the emitter-current bias. The incremental (or signal) current component i_s is given by

$$i_s = \frac{\alpha I \cdot \alpha i_C}{2V_T} \quad (7.79)$$

Equation (7.79) has an easy interpretation. First, note from the symmetry of the circuit (Fig. 7.16) that the differential signal v_{in} should divide equally between the base-emitter junctions of the two transistors. Thus the total base-emitter voltages will be

$$v_{base1} = V_{be} + \frac{v_{in}}{2}$$

$$v_{base2} = V_{be} - \frac{v_{in}}{2}$$

where V_{be} is the dc BE voltage corresponding to no emitter current of $I/2$. Therefore, the collector current of Q_1 will increase by $\alpha g_m v_{in}/2$ and the collector current of Q_2 will decrease by $\alpha g_m v_{in}/2$. Here g_m denotes the transconductance of Q_1 and of Q_2 , which are equal and given by

$$g_m = \frac{i_C}{V_T} = \frac{\alpha I/2}{V_T} \quad (7.80)$$

Thus Eq. (7.79) simply states that $i_s = g_m v_{in}/2$.

An Alternative Viewpoint. There is an extremely useful alternative interpretation of the result above. Assume the current source I to be ideal, its incremental resistance then will be infinite. Thus the voltage v_{in} appears across a total resistance of $2R_e$, where

$$r_e = \frac{V_T}{I_e} = \frac{V_T}{E/2} \quad (7.81)$$

Correspondingly there will be a signal current i_s as illustrated in Fig. 7.17, given by

$$i_s = \frac{v_{in}}{2r_e} \quad (7.82)$$

Hence the collector of Q_1 will exhibit a current increment i_1 and the collector of Q_2 will exhibit a current decrement i_2 :

$$i_1 = \alpha i_s = \frac{\alpha v_{in}}{2r_e} = g_m \frac{v_{in}}{2} \quad (7.83)$$

Note that in Fig. 7.17 we have shown signal quantities only. It is implied, of course, that each transistor is biased at an emitter current of $I/2$.

This method of analysis is particularly useful when resistances are included in the emitters, as shown in Fig. 7.18. For this circuit we have

$$i_s = \frac{v_{in}}{2r_e + 2R_e} \quad (7.84)$$

Input Differential Resistance. Unlike the MOS differential amplifier, which has an infinite input resistance, the BJT differential pair exhibits a finite input resistance, a result of the finite β of the BJT

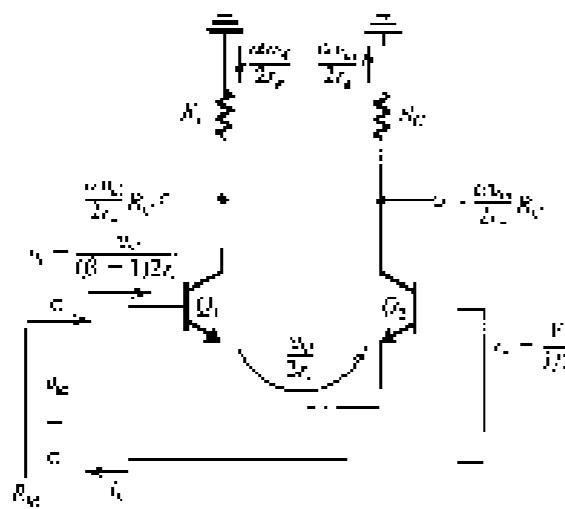


FIGURE 7.17 A simple bipolar circuit showing the signal connection to a differential amplifier excited by a differential voltage signal \$v_d\$. The output voltages are not shown.

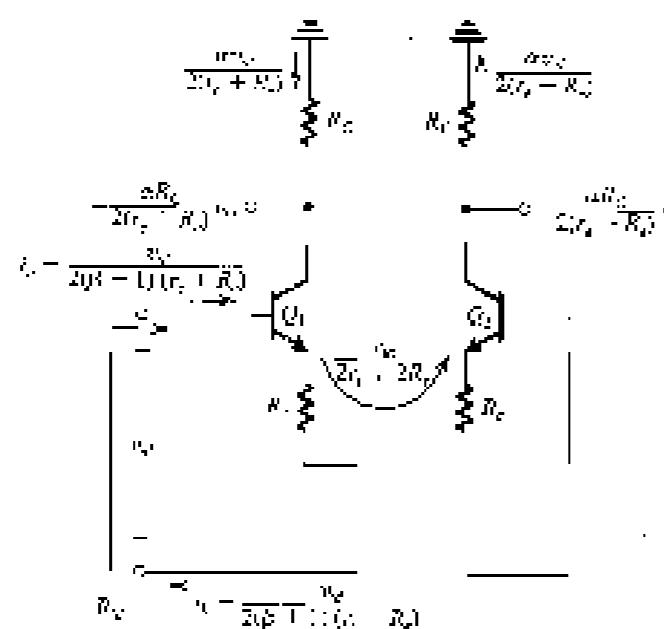


FIGURE 7.18 A differential amplifier with unequal resistances. Only signal quantities are shown in bold.

The input differential resistance is the resistance seen between the two bases; that is, it is the resistance seen by the differential input signal \$v_d\$. For the differential amplifier in Figs. 7.16 and 7.17 it can be seen that the base current of \$Q_1\$ shows an increment \$\delta_i\$ and the base current of \$Q_2\$ shows no equal decrement,

$$\delta_i = \frac{i_b}{\beta + 1} = \frac{v_d / 2r_e}{\beta + 1} \quad (7.85)$$

Thus the differential input resistance \$R_{dI}\$ is given by

$$R_{dI} = \frac{v_d}{\delta_i} = (\beta + 1)2r_e = 2r_e \quad (7.86)$$

This result is just a restatement of the familiar resistor-reflection rule; namely, the resistance seen between the two bases is equal to the load resistance in the emitter (increased by a factor \$(\beta + 1)\$). We can employ this rule to find the input differential resistance for the circuit in Fig. 7.18 as

$$R_{dI} = (\beta + 1)(2r_e + 2R_E) \quad (7.87)$$

Differential Voltage Gain. We have established that for small difference input voltages (\$v_d \ll 2V_T\$, i.e., \$A_d\$ small; less than about 20 mV) the collector currents are given by

$$i_{C1} = i_C - g_m \frac{v_d}{2} \quad (7.88)$$

$$i_{C2} = i_C + g_m \frac{v_d}{2} \quad (7.89)$$

where

$$i_C = \frac{v_T}{2} \quad (7.90)$$

Thus the total voltages at the collectors will be

$$v_{C1} = (V_{CC} - i_C R_C) - g_m R_C \frac{v_d}{2} \quad (7.91)$$

$$v_{C2} = (V_{CC} - i_C R_C) + g_m R_C \frac{v_d}{2} \quad (7.92)$$

The quantities in parentheses are simply the dc voltages at each of the two collectors.

As in the MOS case, the output voltage signal of a bipolar differential amplifier can be taken either differentially (i.e., between the two collectors) or single-endedly (i.e., between one collector and ground). If the output is taken differentially, then the differential gain (as opposed to the common-mode gain) of the differential amplifier will be

$$A_d = \frac{v_{C2} - v_{C1}}{v_d} = \beta_r R_C \quad (7.93)$$

On the other hand, if we take the output single-endedly (say, between the collector of \$Q_1\$ and ground), then the differential gain will be given by

$$A_d = \frac{v_{C1}}{v_d} = -\frac{1}{2} g_m R_C \quad (7.94)$$

For the differential amplifier with resistances in the emitter leads (Fig. 7.16) the differential gain with the output taken单endedly is given by

$$A_d = \frac{i_C(2R_E)}{2r_e + 2R_E} = -\frac{R_E}{r_e + R_E} \quad (7.95)$$

This equation is a familiar one. It states that the voltage gain is equal to the ratio of the total resistance in the collector circuit (\$2R_E\$) to the total resistance in the emitter circuit (\$2r_e + 2R_E\$).

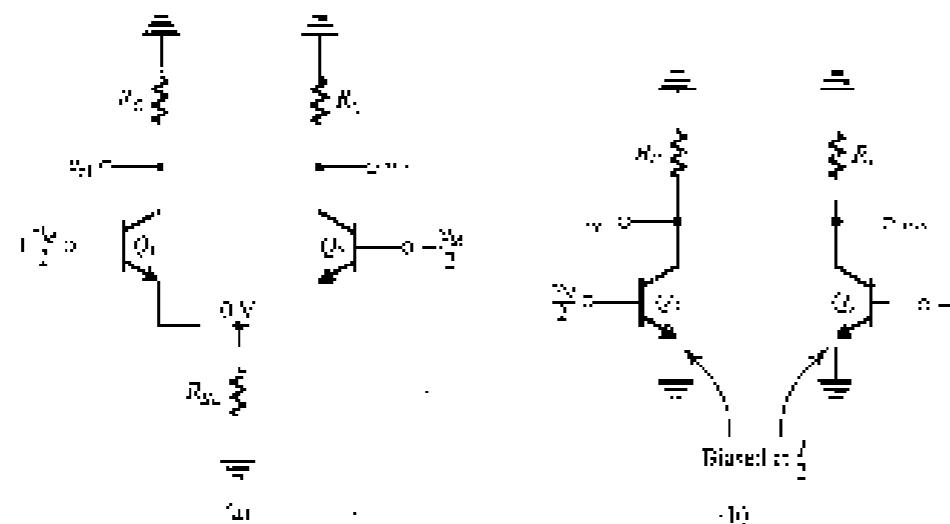


FIGURE 7.19 Equivalent circuit of the BJT differential amplifier. (a) Full circuit; (b) common-mode input to the amplifiers in (b). This analysis applies only for differential input signals. Since in (b) the common-emitter amplifier in (b) can be used to find the differential gain, differential input resistance, frequency response, and so on, of the differential amplifier.

Equivalence of the Differential Amplifier to a Common-Emitter Amplifier The analysis and results on the previous page are quite similar to those obtained in the case of a common-emitter amplifier stage. Thus the differential amplifier is in fact equivalent to a common-emitter amplifier circuit illustrated in Fig. 7.18. Figure 7.19(a) shows a differential amplifier fed by a differential signal v_D , which is applied in a complementary (push-pull or balanced) manner. That is, while the base of Q_1 is raised by $v_D/2$, the base of Q_2 is lowered by $v_D/2$. We have also included the output resistance $R_{L\text{eq}}$ of the load as current source. From symmetry, it follows that the signal voltage at the emitters will be zero. Thus the circuit is equivalent to the two common-emitter amplifiers shown in Fig. 7.19(b), where each of the two transistors is biased at an emitter current of $I/2$. Note that the finite output resistance $R_{L\text{eq}}$ of the current source will have no effect on the operation. The equivalent circuit at Fig. 7.19(b) is valid for differential operation only.

In many applications the differential amplifier is not fed in a complementary fashion; rather, the input signal may be applied to one of the input terminals while the other terminal is grounded, as shown in Fig. 7.20. In this case the signal voltage at the emitters will not be zero, and thus the resistance $R_{L\text{eq}}$ will have an effect on the operation. Nevertheless, if $R_{L\text{eq}}$ is large ($R_{L\text{eq}} \gg r_o$), as is usually the case,² then v_D will still divide equally (approximately) between the two junctions, as shown in Fig. 7.20. Thus the operation of the differential amplifier in this case will be almost identical to that in the case of symmetric load, and the common-emitter equivalence can still be employed.

Since in Fig. 7.19 $v_{D1} = v_{D2}$, the two common-emitter transistors in Fig. 7.19(b) yield similar result³ when the performance of the differential amplifier. Thus only one is needed to analyze for differential small-signal operation of the differential amplifier, and it is known as the **differential half-circuit**. If we take the common-emitter transistor fed with $+v_D/2$ as the differential half-circuit and replace the resistors with its low-frequency equivalents,

² Note that $R_{L\text{eq}}$ appears in parallel with the much smaller r_o of Q_1 .

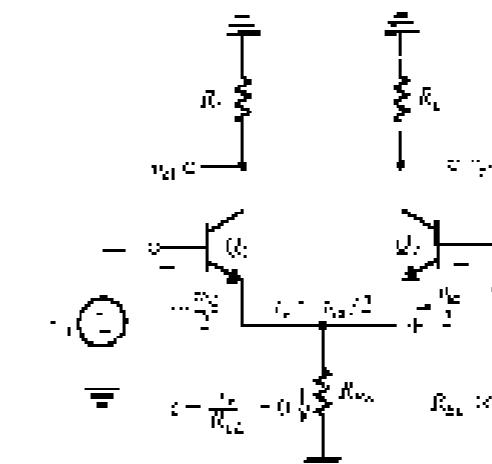


FIGURE 7.20 The BJT differential amplifier fed in a single-ended manner.

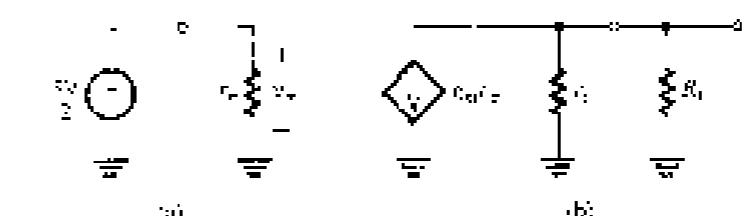


FIGURE 7.21 (a) The differential half-circuit model; (b) its equivalent circuit model.

current mode, the circuit in Fig. 7.21 results. In evaluating the model parameters v_{D1} , v_{D2} , and v_p , we must recall that the half-circuit is biased at $I/2$. The voltage gain of the differential amplifier (with the output taken differentially) is equal to the voltage gain of the half-circuit—that is, $v_{O1}/(v_{D1}/2)$. Hence we note that including r_o will modify the gain expression in Eq. (7.91) to

$$A_{v1} = g_m(R_{L\text{eq}}r_o) \quad (7.96)$$

The input differential resistance of the differential amplifier is twice that of the half-circuit ($\approx 2r_o$). Finally, we note that the differential half-circuit of the amplifier of Fig. 7.18 is a common-emitter transistor with a resistance R_2 in the emitter lead. Thus the common-mode output voltage v_O will be

$$v_O = -\frac{\partial R_{L\text{eq}}}{\partial v_{D1}} \frac{v_{D1}}{2R_{L\text{eq}}} = \frac{g_m R_{L\text{eq}}}{2R_{L\text{eq}}} v_{D1} \quad (7.97)$$

At the other collector we have an equal common-mode signal v_{O2} ,

$$v_{O2} = -\frac{\partial R_{L\text{eq}}}{\partial v_{D2}} \frac{v_{D2}}{2R_{L\text{eq}}} \quad (7.98)$$

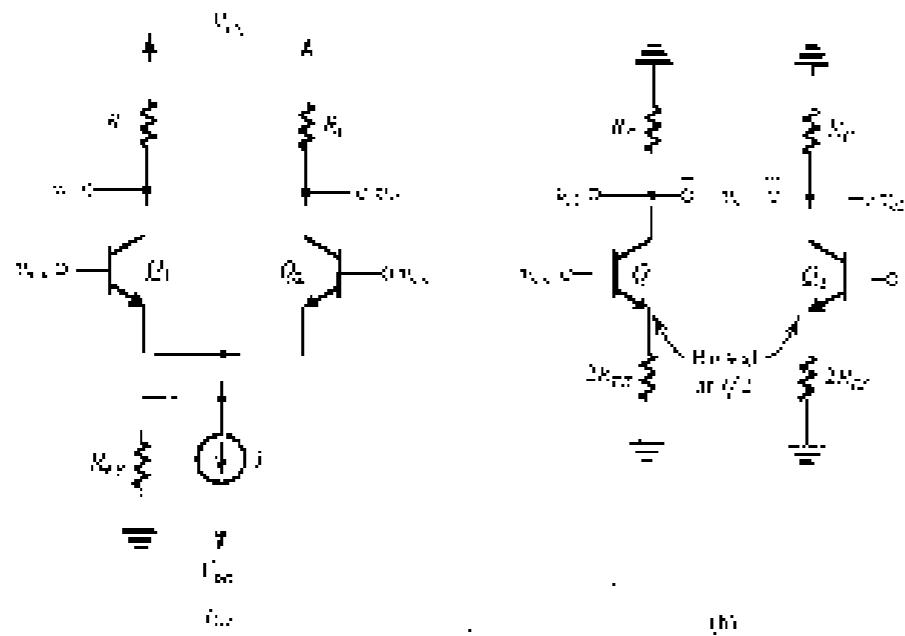


FIGURE 7.22 (a) The operational amplifier fed by a common-mode voltage signal v_0 . (b) A typical "differential-to-single-ended converter."

Now, if the output is taken differentially, then the output common-mode voltage $v_{oC} = (v_{1o} + v_{2o})/2$ will be zero and the common-mode gain also will be zero. On the other hand, if the output is taken single-endedly, the common-mode gain A_{oC} will be finite and given by⁷

$$A_{oC} = \frac{v_{oC}}{v_0} = \frac{\Delta R_C}{2R_{in}} \quad (7.99)$$

Since in this case the differential gain is

$$A_{od} = \frac{1}{2}g_m R_C \quad (7.100)$$

The common-mode rejection ratio (CMRR) will be

$$\text{CMRR} = \left| \frac{A_{od}}{A_{oC}} \right| = g_m R_{in} \quad (7.101)$$

Normally the CMRR is expressed in decibels,

$$\text{CMRR} = 20 \log \left| \frac{A_{od}}{A_{oC}} \right| \quad (7.102)$$

Each of the circuits in Fig. 7.22(b) is called the common-mode null circuit.

⁷ The expressions in Eqs. (7.97) and (7.98) were obtained by neglecting r_o . A detailed derivation using the results of Section 6.1 shows that $v_{oC} = v_0$ and $A_{oC} \approx 0$ approximately.

$$\frac{\Delta R_C}{2R_{in}} \approx \frac{2g_m r_o}{\beta r_s} \quad (7.98)$$

where it is assumed that $R_C \gg r_o$ and $2R_{in} \gg r_s$. This expression reduces to those in Eqs. (7.97) and (7.98) when $2R_{in} \gg r_o$.

The analysis on the facing page assumes that the circuit is perfectly symmetrical. However, practical circuits are not perfectly symmetrical, with the result that the common-mode gain A_{oC} may not be zero even if the output is taken differentially. To illustrate, consider the case of perfect symmetry except for a mismatch ΔR_C in the collector resistances. That is, let the collector of Q_1 have a load resistance R_{1L} and Q_2 have a load resistance $R_{2L} \neq \Delta R_C$. It follows that

$$v_{1o} = -v_{2o} = \frac{\Delta R_C}{2R_{in} + r_o}$$

$$v_{oC} = -v_{1o} = \frac{\Delta R_C + \Delta R_C}{2R_{in} + r_o}$$

Thus the signal at the output due to the common-mode input signal will be

$$v_{oC} = v_{1o} - v_{2o} = v_{1o} \frac{2g_m r_o}{2R_{in} + r_o}$$

and the common-mode gain will be

$$A_{oC} = \frac{\Delta R_C}{2R_{in} + r_o} \approx \frac{\Delta R_C}{2R_{in}}$$

This expression can be rewritten as

$$A_{oC} = \frac{R_C}{2R_{in}} \frac{\Delta R_C}{R_C} \quad (7.103)$$

Compare the common-mode gain in Eq. (7.103) with that for single-ended output in Eq. (7.99). We see that the common-mode gain is much smaller in the case of differential output. Therefore the input differential mode of an op amp, for example, is almost always a balanced one, with the output taken differentially. This ensures that the op amp will have the lowest possible common-mode gain and, therefore, a high CMRR.

The input signals v_1 and v_2 to a differential amplifier usually contain a common-mode component, v_{10} ,

$$v_{10} = \frac{v_1 + v_2}{2} \quad (7.104)$$

and a differential component v_{1d} ,

$$v_{1d} = v_1 - v_2 \quad (7.105)$$

Thus the output signal will be given in general by

$$v_o = A_{od} v_{1d} + A_{oC} \left(\frac{v_1 + v_2}{2} \right) \quad (7.106)$$

Input Common-Mode Resistance. The definition of the common-mode input resistance R_{inC} is illustrated in Fig. 7.23(a). Figure 7.23(b) shows the z-parameter common-mode self-circuit; its input resistance is $2R_{inC}$. The value of $2R_{inC}$ can be determined using the expression we derived in Section 5.9 for the input resistance of a CF amplifier with a resistance R in the emitter. Specifically, we can use Eq. (6.157) and substitute $R_1 = 2R_{inC}$ and $R_2 = R_C$ to obtain for the case $R_2 \gg r_o$ and $2R_{inC} \gg r_s$ the approximate expression

$$2R_{inC} \approx (3 - 1)(2R_{inC} + r_o)$$

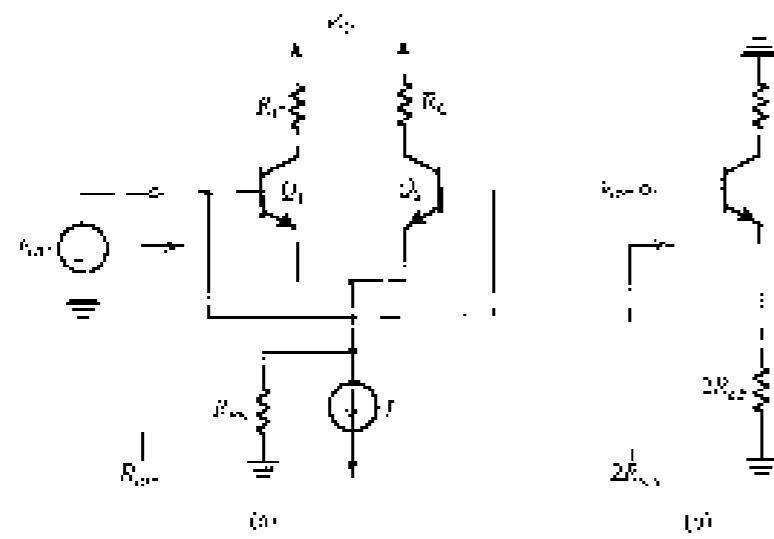


FIGURE 7.23 (a) Definition of the input common-mode resistance $R_{in,CM}$. (b) The equivalent common-mode differential voltage source.

Thus,

$$R_{in,CM} = (\beta + 1) \left(R_{in,CM} \parallel \frac{r_o}{2} \right) \quad (7.107)$$

Equation (7.107) indicates that since $R_{in,CM}$ is typically of the order of r_o , $R_{in,CM}$ will be very large.

- The differential amplifier in Fig. 7.24 uses transistors with $\beta = 100$. To calculate the following:
- The input differential resistance $R_{in,D}$.
 - The overall differential voltage gain A_{vD} .
 - The worst-case common-mode gain if the two collector resistances are assumed $\pm 7\%$.
 - The CMRR, in dB.
 - The input common-mode resistance (assuming that the bias voltage $V_B = 100$ V).

Solution

- (a) Each transistor is biased at an emitter current of 0.5 mA . Thus

$$r_{o1} = r_{o2} = \frac{V_B}{I_E} = \frac{25 \text{ mV}}{0.5 \text{ mA}} = 50 \Omega$$

The input differential resistance is calculated as

$$\begin{aligned} R_{in,D} &= \lambda(\beta + 1)(r_o + R_C) \\ &= 2 \times 10^4 \times (50 + 150) = 40 \text{ k}\Omega \end{aligned}$$

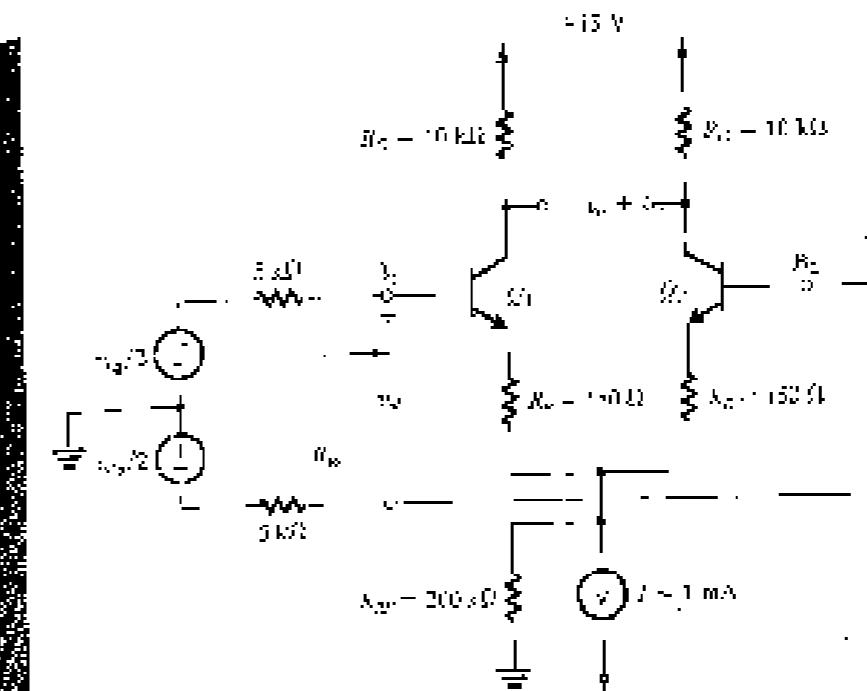


FIGURE 7.24 Circuit for Example 7.1.

- (b) The voltage gain from the signal source to the bases of Q_1 and Q_2 is

$$\begin{aligned} \frac{v_B}{v_{A1}} &= \frac{R_{in,D}}{R_{in,D} + R_{in,CM}} \\ &= \frac{40}{40 + 40} = 0.5 \text{ V/V} \end{aligned}$$

The voltage gain from the bases to the outputs is

$$\begin{aligned} \frac{v_O}{v_B} &= \frac{\text{Total resistance in the collector}}{\text{Total resistance in the emitter}} \\ &= \frac{2R_C}{2(r_o + R_C)} = \frac{2 \times 15}{2(50 + 150) \times 10^{-3}} = 50 \text{ V/V} \end{aligned}$$

The overall differential voltage gain can now be calculated as

$$A_{vD} = \frac{v_O}{v_{A1}} = \frac{v_O v_B}{v_{A1} v_B} = 50 \times 50 = 2500 \text{ V/V}$$

- (c) Using Eq. (7.106),

$$A_{vCM} = \frac{R_C}{2R_{in,D}} \frac{\Delta R_C}{R_C}$$

where $\Delta R_C = 0.07R_C$, in the worst case, 7%.

$$A_{vCM} = \frac{10}{2 \times 40} \times 0.07 = 5 \times 10^{-4} \text{ V/V}$$

$$\begin{aligned}
 & \text{Q.} \\
 & \text{CMRR} = 20 \log \frac{A_d}{A_{11}} \\
 & = 20 \log \frac{40}{5 \times 10^3} = 98 \text{ dB} \\
 & \text{Ans.} \\
 & R_{11} = \frac{V_o}{I_{D2}} = \frac{100}{0.5} = 200 \text{ k}\Omega \\
 & \text{Using Eq. (7.102),} \\
 & R_{\text{out}} = (1 + 1/g_m) R_{11} \left(\frac{g_m}{2} \right) \\
 & = (1 + 230) \text{ k}\Omega \parallel (70 \text{ k}\Omega) = 5.7 \text{ M}\Omega
 \end{aligned}$$

EXERCISE

7.8. For the differential pair of Fig. 7.35(a), if $V_{DD} = 10 \text{ V}$, $R_{11} = 100 \text{ k}\Omega$, and the drain-to-source voltage drop is 0.5 V at 2 mA drain current, and $I_{DSS} = 10 \text{ mA}$ at 2 V drain-to-source voltage, and the transistors are matched, find the output voltage V_o for the following input voltages: (a) $V_{in1} = 0.5 \text{ V}$, $V_{in2} = 0.4 \text{ V}$; (b) $V_{in1} = 0.5 \text{ V}$, $V_{in2} = 0.6 \text{ V}$; (c) $V_{in1} = 0.4 \text{ V}$, $V_{in2} = 0.5 \text{ V}$; (d) $V_{in1} = 0.6 \text{ V}$, $V_{in2} = 0.5 \text{ V}$. Hint: Assume $R_{DS} = 10 \text{ M}\Omega$.

(a) $V_o = 0.5 \text{ V}$; (b) $V_o = 0.5 + 0.05 \ln(2) \times 10 \text{ mV}$; (c) $V_o = 0.5 - 0.05 \ln(2) \times 10 \text{ mV}$; (d) $V_o = 0.5 + 0.05 \ln(2) \times 10 \text{ mV}$. Hint: $V_o = V_{DD}/2 + (V_{in1} - V_{in2})/2 + (V_{in1} - V_{in2})^2/(2R_{DS})$.

7.4 OTHER NONIDEAL CHARACTERISTICS OF THE DIFFERENTIAL AMPLIFIER

7.4.1 Input Offset Voltage of the MOS Differential Pair

Consider the basic MOS differential amplifier with both inputs grounded, as shown in Fig. 7.25(a). If the two sides of the differential pair were perfectly matched (i.e., Q_1 and Q_2 identical and $R_{D1} = R_{D2} = R_D$), then current I would split equally between Q_1 and Q_2 , and V_D would be zero. Practical circuits exhibit imbalances that result in a dc output voltage V_o even with both inputs grounded. We call V_o the output dc offset voltage. More conveniently, we divide V_o by the differential gain of the amplifier, A_d , to obtain a quantity known as the input offset voltage, V_{IO} :

$$V_{IO} = V_o / A_d. \quad (7.108)$$

Obviously, if we apply a voltage V_{IO} between the inputs terminals of the differential amplifier, then the output voltage will be reduced to zero (see Fig. 7.35(b)). This observation gives rise to the usual definition of the input offset voltage. It should be noted, however, that since the offset voltage is a result of device mismatches, its polarity is not known a priori.

Three factors contribute to the dc offset voltage of the MOS differential pair: mismatch in drain resistances, mismatch in $2g_m$, and mismatch in V_t . We shall consider the first contributing factor at this time.

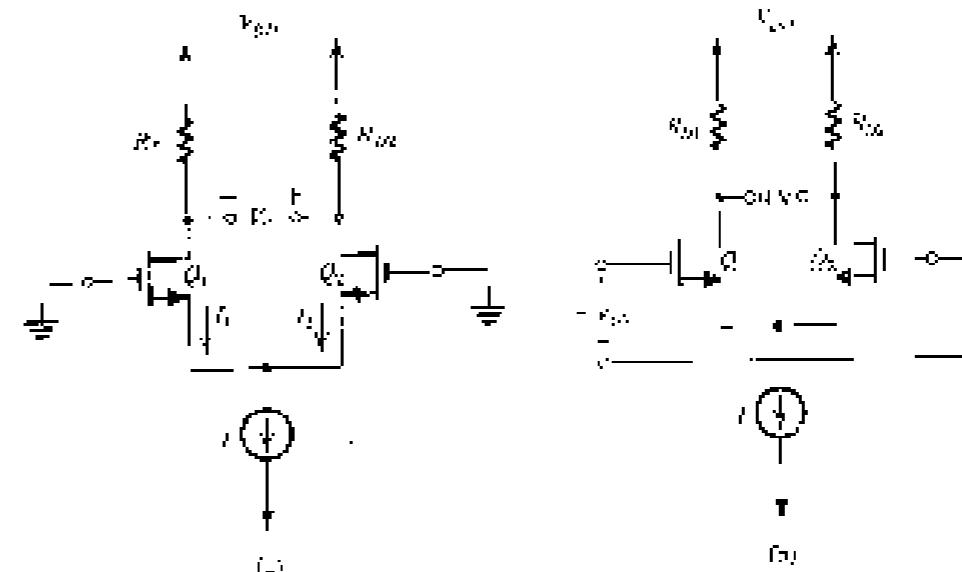


FIGURE 7.25 (a) The MOS differential pair with both inputs grounded. (b) The circuit of part (a) with an input offset voltage V_{IO} applied. (c) Application of a voltage input to the input of the second stage. (d) The input terminal with input biasing voltage V_{IO} to zero.

For the differential chain shown in Fig. 7.25(a), consider first the case where Q_1 and Q_2 are perfectly matched but R_{S1} and R_{S2} show a mismatch ΔR_S ; that is,

$$R_{S1} = R_S + \frac{\Delta R_S}{2} \quad (7.109)$$

$$R_{S2} = R_S - \frac{\Delta R_S}{2} \quad (7.110)$$

Because Q_1 and Q_2 are matched, the currents I will still be equal to each other. Nevertheless, because of the mismatch in load resistances, the output voltages V_{o1} and V_{o2} will be less, because

$$V_{o1} = V_{DD} - \frac{I}{2} (R_D + \frac{\Delta R_S}{2})$$

$$V_{o2} = V_{DD} - \frac{I}{2} (R_D - \frac{\Delta R_S}{2})$$

Thus, the differential output voltage V_o will be

$$\begin{aligned}
 V_o &= V_{o2} - V_{o1} \\
 &= \left(\frac{I}{2} \right) \Delta R_S. \quad (7.1.1)
 \end{aligned}$$

The corresponding input offset voltage is obtained by dividing V_o by the gain $g_m R_D$ and substituting for g_m from Eq. (7.20). The result is

$$V_{IO} = \left(\frac{V_o}{2} \right) \frac{\Delta R_S}{g_m R_D}. \quad (7.1.2)$$

Thus the offset voltage is directly proportional to V_{DD} and, of course, to $\Delta R_2/R_2$. As an example, consider a differential pair in which the two transistors are operating at an over-drive voltage of 0.2 V and each drain resistance is accurate to within $\pm 1\%$. It follows that the worst-case resistor mismatch will be

$$\frac{\Delta R_2}{R_2} = 0.02$$

and the resulting input offset voltage will be

$$V_{IO} = 0.1 \times 100 = 2 \text{ mV}$$

Now, consider the effect of a mismatch in the W/L ratios of Q_1 and Q_2 , expressed as

$$\left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2} \Delta \left(\frac{W}{L}\right) \quad (7.113)$$

$$\left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2} \Delta \left(\frac{W}{L}\right) \quad (7.114)$$

Such a mismatch causes the current I to no longer divide equally between Q_1 and Q_2 . Rather, it can be shown that the currents I_1 and I_2 will be

$$I_1 = I + I \left(\frac{\Delta (W/L)}{2 \times 2^0 W/L} \right) \quad (7.115)$$

$$I_2 = I - I \left(\frac{\Delta (W/L)}{2 \times 2^0 W/L} \right) \quad (7.116)$$

Dividing the current increment

$$\frac{I \Delta (W/L)}{2 \times 2^0 W/L}$$

by R_2 gives half the input offset voltage (due to the mismatch in W/L values). Thus

$$V_{IO} = \left(\frac{R_2}{2} \right) \left(\frac{\Delta (W/L)}{2^0 W/L} \right) \quad (7.117)$$

Here again we note that V_{IO} , resulting from a W/L mismatch, is proportional to V_{DD} and, as expected, $\propto W/L$.

Finally, we consider the effect of a mismatch ΔV between the two drain-to-source voltages.

$$V_1 = V_i + \frac{\Delta V}{2} \quad (7.118)$$

$$V_2 = V_i - \frac{\Delta V}{2} \quad (7.119)$$

The current I_1 will be given by

$$I_1 = \frac{1}{2} k_s \frac{W}{L} (V_{DS1} - V_i) \left(1 - \frac{\Delta V}{2(V_{DS1} - V_i)} \right)^2$$

which, for $\Delta V \ll 2(V_{DS1} - V_i)$ (that is, $\Delta V \ll 2V_{DS1}$), can be approximated as

$$I_1 \approx \frac{1}{2} k_s \frac{W}{L} (V_{DS1} - V_i)^2 \left(1 - \frac{\Delta V}{V_{DS1}} \right)^2$$

similarly,

$$I_2 = \frac{1}{2} k_s \frac{W}{L} (V_{DS2} - V_i)^2 \left(1 - \frac{\Delta V}{V_{DS2} - V_i} \right)^2$$

It follows that

$$\frac{1}{2} k_s \frac{W}{L} (V_{DS1} - V_i)^2 = \frac{1}{2}$$

and the current mismatch (decrement) in Q_1 / Q_2 is

$$\Delta I \equiv \frac{I_1 - I_2}{2(V_{DS1} - V_i)} = \frac{I}{2} \frac{\Delta V}{V_{DS1}}$$

Dividing ΔI by R_2 gives half the input offset voltage (due to ΔV). Thus

$$V_{IO} = \Delta V \quad (7.120)$$

a very logical result! For modern MOS technology ΔV can be easily as high as 2 mV.

Finally, we note that since the three sources for offset voltage are not correlated, an estimate of the total input offset voltage can be found as

$$V_{IO} = \sqrt{\left(\frac{R_2}{2} \right) \frac{\Delta R_2 W^2}{R_2 L} + \left(\frac{V_{DD}}{2} \right) \frac{\Delta (\beta_1 \beta_2 L)^2}{W^2 L^2} + (\Delta V)^2} \quad (7.121)$$

EXERCISE

7.10 Consider a CMOS differential pair with $V_{DD} = 10 \text{ V}$ and $R_2 = 10 \text{ k}\Omega$. If the drain resistances are $R_{D1} = 10 \text{ k}\Omega$ and $R_{D2} = 12 \text{ k}\Omega$, calculate the input offset voltage. Assume $k_s = 100 \mu\text{A}/\text{V}^2$, $L = 1 \mu\text{m}$, $W = 10 \mu\text{m}$, $\beta_1 = 100$, $\beta_2 = 120$, $V_{DS1} = V_{DS2} = 0.2 \text{ V}$, and $V_i = 0$.

7.4.2 Input Offset Voltage of the Bipolar Differential Pair

The offset voltage of the bipolar differential pair shown in Fig. 7.26(a) can be determined in a manner analogous to that used above for the MOS pair. Note, however, due to the bipolar case there is no scaling to the V_i mismatch of the MOSFET pair. Here the output offset results from mismatch in the load resistances R_{L1} and R_{L2} and β junction area, β , and other factors, when in Q_1 and Q_2 . Consider first the effect of the load mismatch, i.e.

$$R_{L1} = R_{L2} = \frac{\alpha R_L}{2} \quad (7.122)$$

$$R_{L2} = R_L + \frac{\Delta R_L}{2} \quad (7.123)$$

and assume that Q_1 and Q_2 are perfectly matched. It follows that current I will divide equally between Q_1 and Q_2 , and thus

$$V_{O1} = V_{O2} = \left(\frac{g_f}{2} \right) R_{L1} = \frac{\alpha R_L}{2}$$

$$V_{O2} = V_{O1} = \left(\frac{g_f}{2} \right) R_{L2} = \frac{\alpha R_L}{2}$$

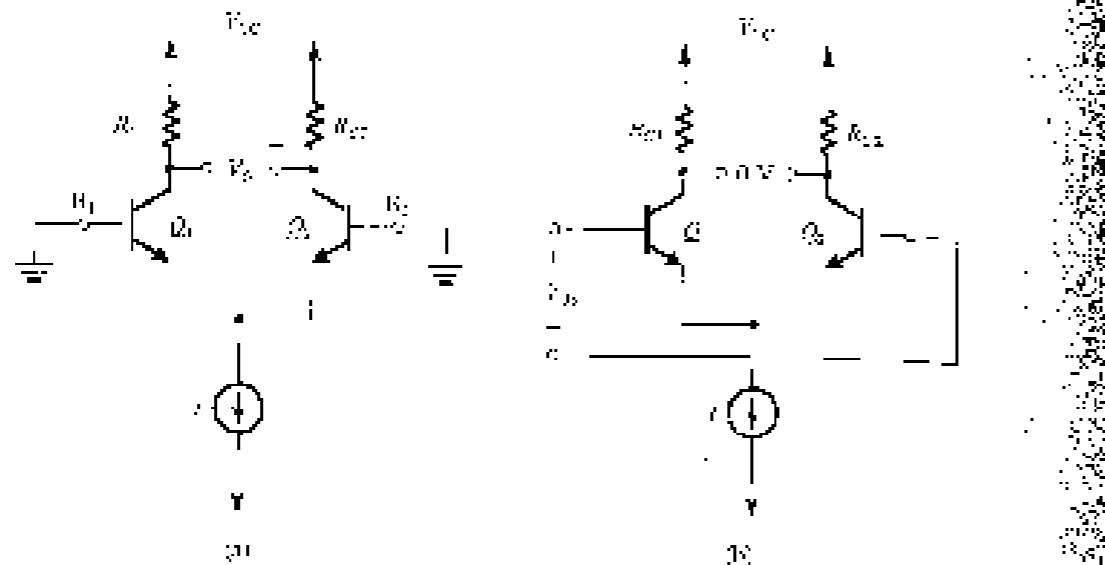


FIGURE 7.2d (a) The DIF differential amplifier with both inputs active. (b) Device connections used to obtain dc output V_o . (c) A connection of the input offset voltage V_{IO} = V_{IO1} to the top terminals over appropriate resistor values R_{IO1} gives:

Then the output voltage will be

$$V_o = V_{o1} - V_{o2} = \alpha \left(\frac{I_s}{\lambda} \right) \Delta R_{IO}$$

and the input offset voltage will be

$$V_{IO} = \frac{\alpha (I_s / \lambda) \Delta R_{IO}}{I_s} \quad (7.127)$$

Substituting $\alpha_s = \alpha_s R_C$ and

$$\beta_s = \frac{\alpha_s R_C}{V_T}$$

gives

$$|V_{IO}| = V_T \left(\frac{\Delta R_{IO}}{R_C} \right) \quad (7.128)$$

An important point to note is that in comparison to the corresponding expression for the MOS pair (Eq. 7.115), here the offset is proportional to V_T rather than $V_{DD}/2$. V_T at 25 mV is 4 to 10 times lower than $V_{DD}/2$. Hence bipolar differential pairs exhibit lower offsets than their MOS counterparts. As an example, consider the situation where the collector resistors are equal up to within $\pm 5\%$. Then the worst-case mismatch will be

$$\frac{\Delta R_C}{R_C} = 0.02$$

and the resulting input offset voltage will be

$$|V_{IO}| = 25 \times 0.02 = 0.5 \text{ mV}$$

Next consider the effect of mismatches in transistors Q_1 and Q_2 . In particular, let the transistors have a mismatch in their active-base junction areas, which are unequal.

gives α_s a proportional mismatch to the same currents I_s

$$I_{s1} = I_s + \frac{\Delta I_s}{2} \quad (7.129)$$

$$I_{s2} = I_s - \frac{\Delta I_s}{2} \quad (7.130)$$

Refer to Fig. 7.2d(a) and note that $V_{o1} = V_{o2}$. Thus, the current I will split between Q_1 and Q_2 in proportion to their I_s values, resulting in

$$I_{s1} = \frac{I_s}{2} \left(1 + \frac{\Delta I_s}{2 I_s} \right) \quad (7.126)$$

$$I_{s2} = \frac{I_s}{2} \left(1 - \frac{\Delta I_s}{2 I_s} \right) \quad (7.127)$$

It follows that the output offset voltage will be

$$V_o = 2 \left(\frac{1}{2} \right) \frac{\Delta I_s}{I_s} R_C$$

and the corresponding input offset voltage will be

$$|V_{IO}| = V_T \left(\frac{\Delta I_s}{I_s} \right) \quad (7.130)$$

As an example, an area mismatch of 4% gives rise to $\Delta I_s/I_s = 0.04$ and an input offset voltage of 1 mV. Here again we note that the offset voltage is proportional to V_T rather than to the much larger V_{DD} , which determines the offset of the MOS pair (in AOPC) mismatch.

Since the two contributions to the input offset voltage are not correlated, an estimate of the total input offset voltage can be found as

$$V_{IO} = \sqrt{V_T^2 \frac{\Delta R_{IO}^2}{R_C^2} + \left(V_T \frac{\Delta I_s}{I_s} \right)^2} \\ = V_T \sqrt{\frac{\Delta R_{IO}^2}{R_C^2} + \left(\frac{\Delta I_s}{I_s} \right)^2} \quad (7.131)$$

There are other possible sources for input offset voltage such as mismatches in the values of β and v_T . Some of these are investigated in the end-of-chapter problems. Finally, it should be noted that there is a popular scheme for compensating for the offset voltage; it involves introducing a feedback mechanism at the values of the two collector resistors such that the differential output voltage is reduced to zero when both input terminals are grounded. Such an offset-nulling scheme is explained in Problem 7.57.

7.4.3 Input Bias and Offset Currents of the Bipolar Pair

In a perfectly symmetric differential pair the two input terminals carry equal dc currents. That is,

$$I_{p1} = I_{p2} \approx \frac{I_D}{2} \quad (7.132)$$

This is the input bias current of the differential amplifier.

Mismatches in the amplifier circuit and most importantly a mismatch in β underlie the two input-drain currents mismatch. The resulting difference is the input offset current, I_{os} , given as

$$I_{os} = |I_{s1} - I_{s2}| \quad (7.133)$$

Let

$$\beta_1 = \beta + \frac{\Delta\beta}{2}$$

$$\beta_2 = \beta - \frac{\Delta\beta}{2}$$

Then

$$I_{s1} = \frac{I}{2\beta_1 + \Delta\beta/2} = \frac{I}{2\beta + 1} \left(1 + \frac{\Delta\beta}{2\beta}\right) \quad (7.134)$$

$$I_{s2} = \frac{I}{2\beta_2 + \Delta\beta/2} = \frac{I}{2\beta + 1} \left(1 - \frac{\Delta\beta}{2\beta}\right) \quad (7.135)$$

$$I_{os} = \frac{I}{2(\beta + 1)} \left(\frac{\Delta\beta}{\beta}\right) \quad (7.136)$$

Finally, the gain-bandwidth product I_g is defined as follows:

$$I_g = \frac{I_g - I_{os}}{2} = \frac{I}{2(\beta + 1)} \quad (7.137)$$

Thus

$$I_{os} = I_g \cdot \frac{\Delta\beta}{\beta} \quad (7.138)$$

As, for example, a 10% β mismatch results in an offset that is current one-tenth the value of the input bias current.

Finally note that obviously a great advantage of the MOS differential pair is that it does not suffer from finite input bias current or from mismatch thereof.

7.4.4 Input Common-Mode Range

As mentioned earlier, the input common-mode range of a differential amplifier is the range of the input voltage v_{cm} over which the differential pair behaves as a linear amplifier for differential input signals. The upper limit of the common-mode range is determined by Q_1 and Q_2 leaving the active mode and entering the saturation mode of operation in the BJT case or the triode mode of operation in the MOS case. Thus, for the bipolar case the upper limit is approximately equal to 0.4 V above the dc collector voltage of Q_1 and Q_2 . For the MOS case, the upper limit is equal to V , so is above the voltage at the drains of Q_1 and Q_2 . The lower limit is determined by the transistor that supplies the biasing current I leaving its active region of operation and thus no longer functioning as a constant current source. Current source circuits were studied in Sections 6.3 and 6.12.

7.4.5 A Concluding Remark

We conclude this section by noting that the definitions presented here are identical to those presented in Chapter 4 for op amps. In fact, as will be seen in Chapter 9, it is the input

differential voltage in an op-amp circuit that primarily determines the op-amp's dc offset voltage, input bias and offset currents, and input common-mode range.

EXERCISE

For a BJT differential amplifier design, the following parameters are required: $V_{DD} = 10$ V, $R_L = 100 \Omega$, $\beta = 100$, $\beta_0 = 100$, $\lambda = 0.01$, $\Delta\beta = 10$, $I = 10 \mu A$, $V_{BE} = 0.7$ V, $I_{os} = 10 \mu A$, and $f_T = 100$ Hz. Find V_{os} , I_g , and I_{os} . (The dc bias current is 200 μA .)

7.5 THE DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

As we learned in Chapter 6, replacing the linear load resistor R_L with a constant-current source results in much higher voltage gain as well as savings in components. The same, of course, applies to the differential amplifier. In this section we study an important circuit for implementing an active-load differential amplifier and at the same time converting the output from differential to single-ended. We shall study both the MOS and bipolar forms of this particular circuit.

7.5.1 Differential-to-Single-Ended Conversion

In the previous sections we found that taking the output of the differential amplifier as the voltage between the two drivers (emitters), results in double the value of the differential gain as well as a much reduced common-mode gain. In fact, the only reason a small fraction of the input common-mode signal appears between the differential output terminals is the transients inevitably present in the circuit. Thus if a real integrator (such as an op-amp) is to achieve a high CMRR, the output of its first stage must be taken differentially. Beyond the first stage, however, unless the system is fully differential, the signal is converted from differential to single-ended.

Figure 7.27 illustrates the simplest most basic approach for differential-to-single-ended conversion. It consists of simply bypassing the drain current signal of Q_1 and eliminating its drain

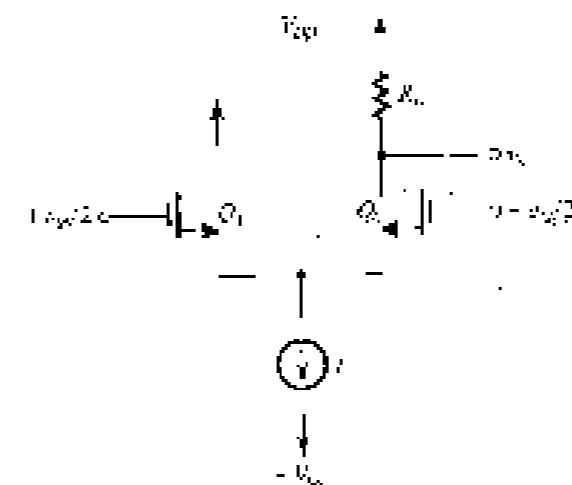


FIGURE 7.27 A simple (but efficient) approach for differential-to-single-ended conversion.

resistor degeneration and taking the output between the drains of Q_1 and ground. The obvious disadvantage of this scheme is that we lose a factor of 2 for G_{dA} in gain as a result of "biasing" the drain signal current of Q_1 . A much better approach would be to find a way of utilizing the drain-current signal of Q_1 , and that is exactly what the circuit we are about to discuss accomplishes.

7.5.2 The Active-Loaded MOS Differential Pair

Figure 7.28(a) shows a MOS differential pair formed by transistors Q_1 and Q_2 , loaded in a current mirror formed by transistors Q_3 and Q_4 . To see how the circuit operates consider first the quiescent state with the two input terminals connected to a dc voltage equal to the common-mode equilibrium value, in this case 0 V, as shown in Fig. 7.28(b). Assuming perfect matching, the bias current I_b divides equally between Q_1 and Q_2 . The drain current of Q_3 , $I/2$, is fed to the input transistor of the mirror, Q_4 . Thus, a replica of this current is provided by the output transistor of the mirror, Q_3 . Observe that at the output node the two currents $I/2$ balance each other out, leaving a zero current to flow out to the next stage or to a load (not shown). If Q_3 is perfectly matched to Q_4 , its drain voltage will track the voltage at the drain

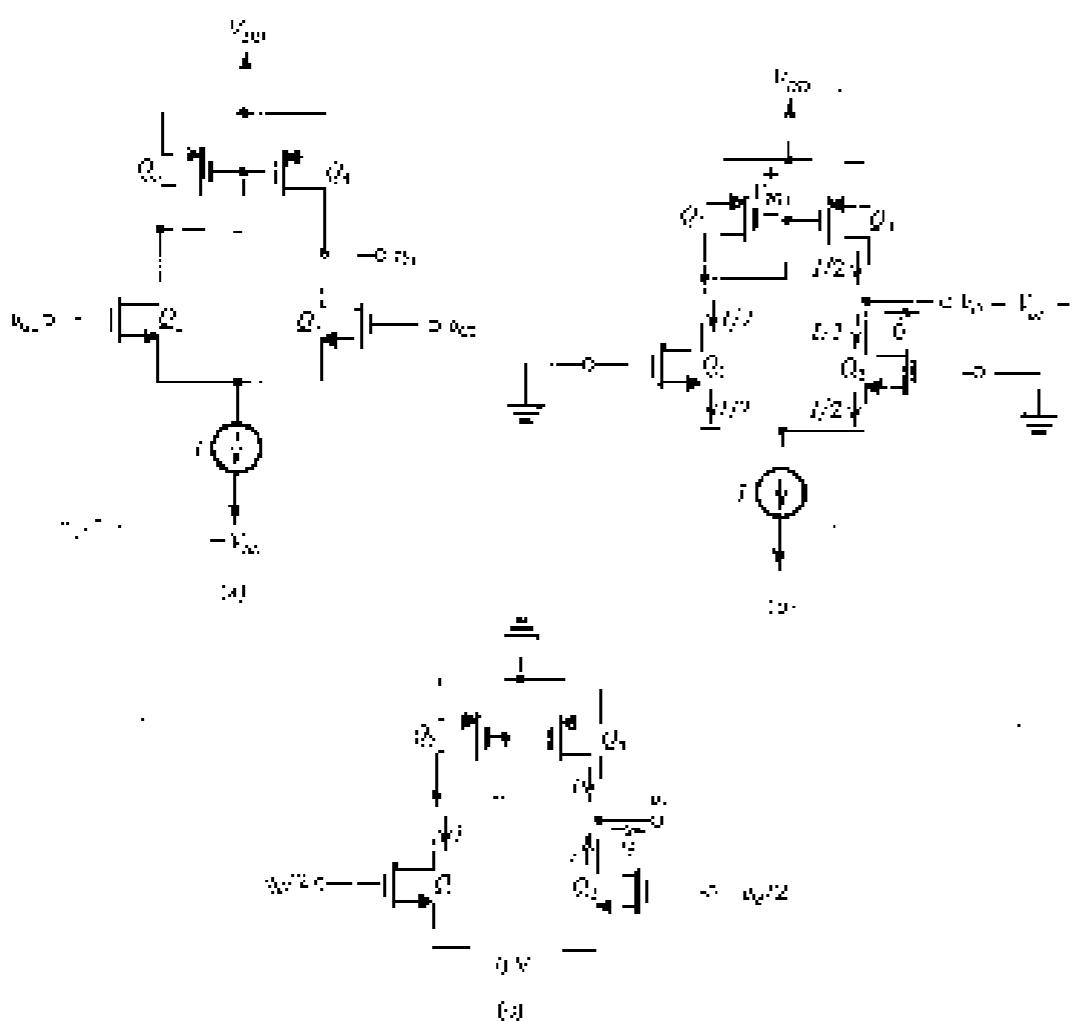


FIGURE 7.28 (a) The active-loaded MOS differential pair; (b) the circuit at equilibrium; (c) the small-signal equivalent circuit applied, neglecting the r_s of the transistors.

of Q_3 ; thus, in equilibrium the voltage at the output will be $V_{DQ} = V_{SDQ}$. It should be noted, however, that in practical implementations, there will always be mismatch errors, resulting in a dc current at the output. In the absence of a load connection, this current will flow into the output resistances of Q_2 and Q_3 and thus can cause a large deviation in the output voltage from the ideal value. Therefore, this circuit is always designed so that the dc bias voltage at the output node is determined by a feedback circuit rather than by simply relying on the matching of Q_3 and Q_4 . We shall see how this is done later.

Next, consider the circuit with a differential input signal v_{in} applied to the inputs, as shown in Fig. 7.28(c). Since we are now investigating the small-signal operation of the circuit, we have removed the dc supplies (including the current source I_b). Also, for the time being let us ignore r_s of all transistors. As Fig. 7.28(c) shows, a virtual ground will develop at the common-source terminal of Q_1 and Q_2 . Transistor Q_4 will conduct a drain signal current $i = g_m v_{in}$, and transistor Q_3 will conduct an equal but opposite current i . The drain signal current of Q_3 is fed to the input of the Q_1-Q_2 mirror, which functions by inverting (i) replicating the drain of Q_4 . Now, at the output node we have two currents, each equal to i , which sum together to provide an output current $2i$. It is this factor of 2, which is a result of the current mirror action, that makes it possible to convert the signal to single ended form (i.e., between the output node and ground) with no loss of gain. If a load resistance is connected to the output node, the current $2i$ flows through it and thus determines the output voltage v_{out} . In the absence of a load resistance, the output voltage is determined by the output current $2i$ and the output resistance of the circuit, as we shall shortly see.

7.5.3 Differential Gain of the Active-Loaded MOS Pair

As we have learned in Chapter 6, the output resistance r_o of the transistor plays a significant role in the operation of active-loaded amplifiers. Therefore, we shall now take r_o into account and derive an expression for the differential gain v_{out}/v_{in} of the active-loaded MOS differential pair. Unfortunately, because the circuit is non-symmetrical we will not be able to use the differential half-circuit technique. Rather, we shall perform the derivation from first principles. We will first find the short-circuit transconductance G_m and the output resistance R_o . Then, the gain will be determined in $G_m R_o$.

Determining the Transconductance G_m . Figure 7.29(a) shows the circuit prepared for determining G_m . Note that we have short-circuited the output to ground in order to find G_m as i_{DQ}/v_{DSQ} . Although the original circuit is not perfectly symmetrical, when the output is shorted to ground, the circuit becomes almost symmetrical. This is because the voltage between the drain of Q_1 and ground is very small. This in turn is due to the low resistance between that node and ground, which is assumed equal to r_{oQ_1} . Thus, we can ignore symmetry and assume that a virtual ground will appear at the source of Q_2 and Q_3 and in this way obtain the equivalent circuit shown in Fig. 7.29(b). Here we have replaced the diode-connected transistor Q_3 by its equivalent resistance $(1/g_m)(r_{oQ_1})$. The voltage v_{DSQ} that develops at the collector-gate line of the mirror can be found as

$$v_{DSQ} = -g_m \left(\frac{V_{SDQ}}{2} \right) \left[\frac{1}{r_{oQ_1}} + r_{oQ_2} + r_{oQ_3} \right] \quad (7.139)$$

which for the usual case of $r_{oQ_1} \gg r_{oQ_2}, r_{oQ_3}$ reduces to

$$v_{DSQ} \approx -\left(\frac{g_m}{2} \right) \frac{V_{SDQ}}{r_{oQ_1}} \quad (7.140)$$

This voltage controls the drain current of Q_3 , resulting in a current of $g_m v_{DSQ}$. Note that the ground at the output node causes the currents in r_{oQ_2} and r_{oQ_3} to be zero. Thus the output current

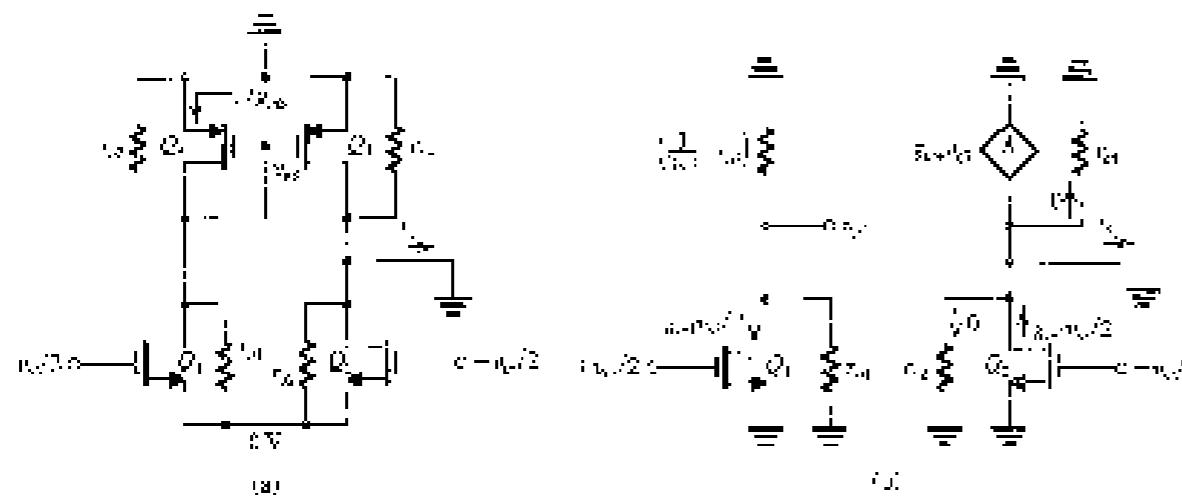


FIGURE 7.29 Determining the three-neuron transconductance $G_3 = i_3/i_{in}$ of the voltage-gated Na⁺ channel/pair.

i will be

$$L = -\lambda_1 v_x + \lambda_2 v_y + \frac{(\lambda_3)}{2} \quad (2.14)$$

Substitution for ρ_1 , from (7.140), give

$$Q_1 = g_{11} \left(\frac{g_{22}}{g_{11}} \right) \left(\frac{g_{33}}{g_{11}} \right) + g_{12} \left(\frac{g_{22}}{g_{11}} \right)$$

More, since $y_{ij} = x_{ij}$ and $g_{ij} = b_{ij} - s_{ij}$, the current ℓ becomes

$$j_1 = j_2$$

↳ [View details](#)

$$G_{ij} \equiv g_{ij} \quad (7.14)$$

Thus the short-circuit transconductance of the silicon is equal to g_m of each of the two transistors at the differential pair. Here we should note that in the absence of the current minimization, g_m would be equal to $k_T/\sqrt{2}$.

Determining the Output Resistance R_o . Figure 7.30 shows the circuit for determining R_o . Observe that the current in the collector of Q_1 must exit its source. It then enters (g_1) , exists at the drain, to feed the $(g_2 - g_3)$ Miller. Since for the diode-connected transistor Q_2 , $|g_{21}|$ is much smaller than r_{ds} , most of the current i will flow into the drain of Q_2 . The miller responds by providing an equal current i in the drain of Q_2 . It now remains to determine the relationship between i and v_{os} . From Fig. 7.30 we see that

where R_o is the output resistance of Q_1 . Now, Q_1 is a CG transistor and has in its source lead the input resistance of Q_1 . The latter is connected in the CG configuration with a small resistor and is therefore far from unity ($\approx 1/\alpha$), thus its input resistance is given roughly by $1/\alpha$.

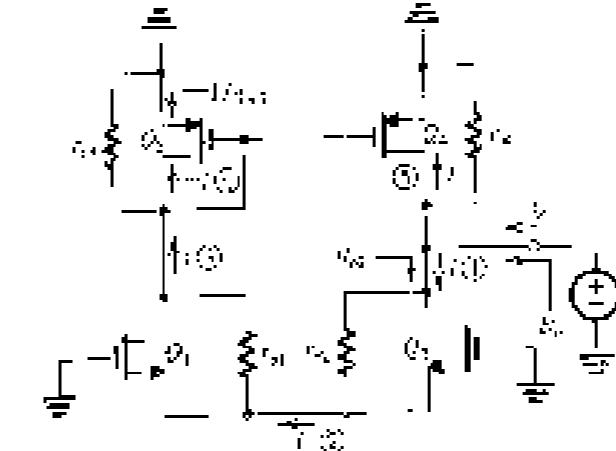


FIGURE 7.30: Flowchart for determining Δ . The nodes numbered 1 through 6 are the ends of the newly-discovered edges.

we now use Eq. (6.161) to determine R_{12} by substituting $\rho_{12} = 0$ and $R_1 = 1\%$, to obtain

$$R_{\mu\nu} = T_{\mu\nu} + \Lambda^2 - g_{\mu\nu} R(\lambda)/\lambda^2$$

which for $\rho_{\text{ex}} = \rho_{\text{ext}} = \rho_0$ and $\rho_{\text{ext}}r_{\infty} \ll 1$ yields

$$\delta_{\alpha} \leq 2r_{\alpha} \quad (7.144)$$

Revising the code in Fig. 7.30, we can write at the output rate

$$\begin{aligned} f_1 &= (1 + \frac{1}{n})^{\frac{n}{2}} \\ &= 2^n \cdot \frac{3^n}{2^n} = 2^{\frac{1}{2}} \cdot 3^{\frac{1}{2}} \end{aligned}$$

Substituting for $R_{\alpha\beta}$ from Eq. (7.146) we obtain

$$k_2 = \frac{c_1}{c_{\text{tot}}} = \frac{c_1}{1 + c_1}$$

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$$R_{ij} = \frac{d_i}{r_j} = r_{ij}/(r_A) \quad (7.145)$$

which is an intuitively appealing result.

Determining the Differential Gain: Equations (7.142) and (7.143) can be combined to obtain the differential gain $A_{differential}$:

$$A_3 \equiv {}^{\text{v}_2} = G_\alpha R_\beta = g_{\alpha\beta}(r_{\text{ad}}) \quad (7.145)$$

For the case $\mu = \sigma < 2$

$$A_0 = \frac{1}{2} \sin \theta_0 = \frac{A_0}{2} \quad (7.47)$$

Figure 1 The behaviour of the NDS transistor

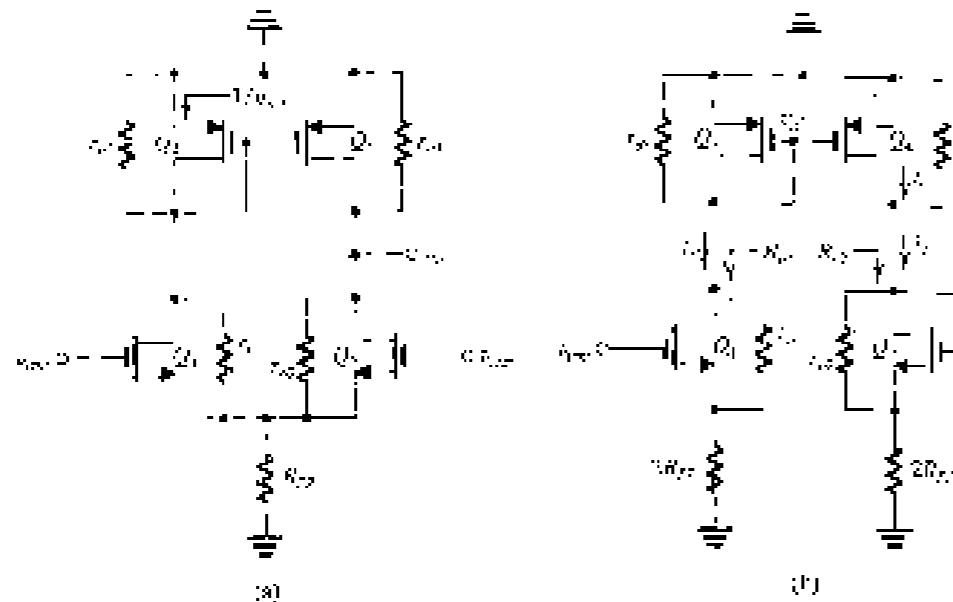


FIGURE 7.31 Analysis of the active-loaded MOS differential amplifier to determine its common-mode gain.

7.5.4 Common-Mode Gain and CMRR

Although its output is single ended, the active-loaded MOS differential amplifier has a low common-mode gain and, correspondingly, a high CMRR. Figure 7.31(a) shows the circuit with v_{in} applied and with the power supplies eliminated except, of course, for the input resistance R_{in} of the bias-current source I . Although the circuit is not symmetrical and hence we cannot use the common-mode null method, we can split R_{in} equally between Q_1 and Q_2 as shown in Fig. 7.31(b). It can now be seen that each of Q_1 and Q_2 is a CS transistor with a large source degeneration resistance $2R_S$. We can use the formulas derived in Section 6.9 to determine the currents i_1 and i_2 that result from the application of a single signal v_{in} . Alternatively, we observe that since $2R_S$ is usually much larger than $1/g_m$ of each of Q_1 and Q_2 , the signals at the source terminals will be approximately equal to v_{in} . Also, the effect of r_{ds} and r_{os} can be shown to be negligible. Thus, we can write

$$i_1 = i_2 = \frac{v_{in}}{2R_S} \quad (7.148)$$

The output resistance of each of Q_1 and Q_2 is given by Eq. 6.101 which, for $R_s \gg 1/g_m$ and $g_{os} = 0$ yields

$$r_{os} = R_{os} = r_s + 2R_S + 2g_{os}r_sR_S \quad (7.149)$$

where $r_{os} = r_{os} = r_s$ and $g_{os} = g_{os} = g_m$. Note that R_{os} will be much greater than the parallel resistance introduced by Q_2 , namely $(1/g_m)(1/g_{os})$. Similarly, R_{os} will be much greater than r_s . Thus, we can easily neglect R_{os} and A_{os} in finding the total resistance between the drains of the drain nodes and ground.

The current i_1 is passed through $(1/g_{os}) \parallel r_s$ which in turn produces a voltage v_{os} .

$$v_{os} = -i_1 \left(\frac{1}{g_{os}} \parallel r_s \right) \quad (7.150)$$

Transistor Q_1 carries this voltage and hence provides a drain current i_2

$$i_2 = -g_{os}v_{os} \\ = \frac{-g_{os}^2}{(1/g_{os}) \parallel r_s} \parallel r_s \quad (7.151)$$

Now, at LDO output node the current difference between i_2 and i_1 passes through r_{os} (since $R_{os} \gg r_{os}$) to provide v_{os}

$$v_{os} = (i_2 - i_1)r_{os} \\ = \left[\frac{1}{g_{os}} \frac{1}{\frac{1}{g_{os}} \parallel r_s} \parallel r_s \right] - i_1 r_{os}$$

Simplifying for i_1 and i_2 from Eq. (7.148) and setting $v_{in} = 4.0$ we obtain after some straightforward manipulations

$$A_{os} = \frac{r_s}{2R_S} = -\frac{r_s}{2R_S(1 - g_{os}r_s)} \quad (7.152)$$

Finally, $i_{os} \gg 1$ and $i_{os} = r_{os}$ yielding

$$A_{os} = \frac{1}{1 + g_{os}R_S} \quad (7.153)$$

Since R_S is usually large, at least equal to r_s , A_{os} will be small. The common-mode rejection ratio (CMRR) can now be obtained by utilizing Eqs. (7.146) and (7.153).

$$\text{CMRR} = \frac{|A_{os}|}{|A_{cm}|} = (g_{os}r_{os}) \parallel r_s \parallel 2R_S \parallel r_s \quad (7.154)$$

which for $r_{os} = r_{os} \gg r_s$ and $R_S \gg r_s$ simplifies to

$$\text{CMRR} = (g_{os}r_{os})(g_{os}R_S) \quad (7.155)$$

We observe that to obtain a large CMRR we select an implementation of the biasing current source I that features a high output resistance. Such circuits include the cascode current source and the Wilson current source studied in Section 6.12.

EXERCISE

7.5.1. Design a single-supply CMOS differential amplifier with a typical output voltage of $V_{out} = 10V$ and a load of 200Ω . If $C_{in} = 100 \text{ pF}$, $C_{load} = 100 \text{ pF}$, $f_c = 100 \text{ Hz}$, and $f_{ul} = 100 \text{ kHz}$, calculate C_{os} , R_{os} , and CMRR.

7.5.2. In the design of the CMOS differential amplifier of Exercise 7.5.1, if $C_{in} = 100 \text{ pF}$, $C_{load} = 100 \text{ pF}$, $f_c = 100 \text{ Hz}$, and $f_{ul} = 100 \text{ kHz}$, calculate C_{os} , R_{os} , and CMRR.

7.5.3. In the design of the CMOS differential amplifier of Exercise 7.5.1, if $C_{in} = 100 \text{ pF}$, $C_{load} = 100 \text{ pF}$, $f_c = 100 \text{ Hz}$, and $f_{ul} = 100 \text{ kHz}$, calculate C_{os} , R_{os} , and CMRR.

7.5.5 The Bipolar Differential Pair with Active Load

The bipolar version of the active-loaded differential pair is shown in Fig. 7.32(a). The circuit structure and operation are very similar to those of the MOS counterpart, except that here we have to contend with the effects of finite β and the resulting finite load resistance at the

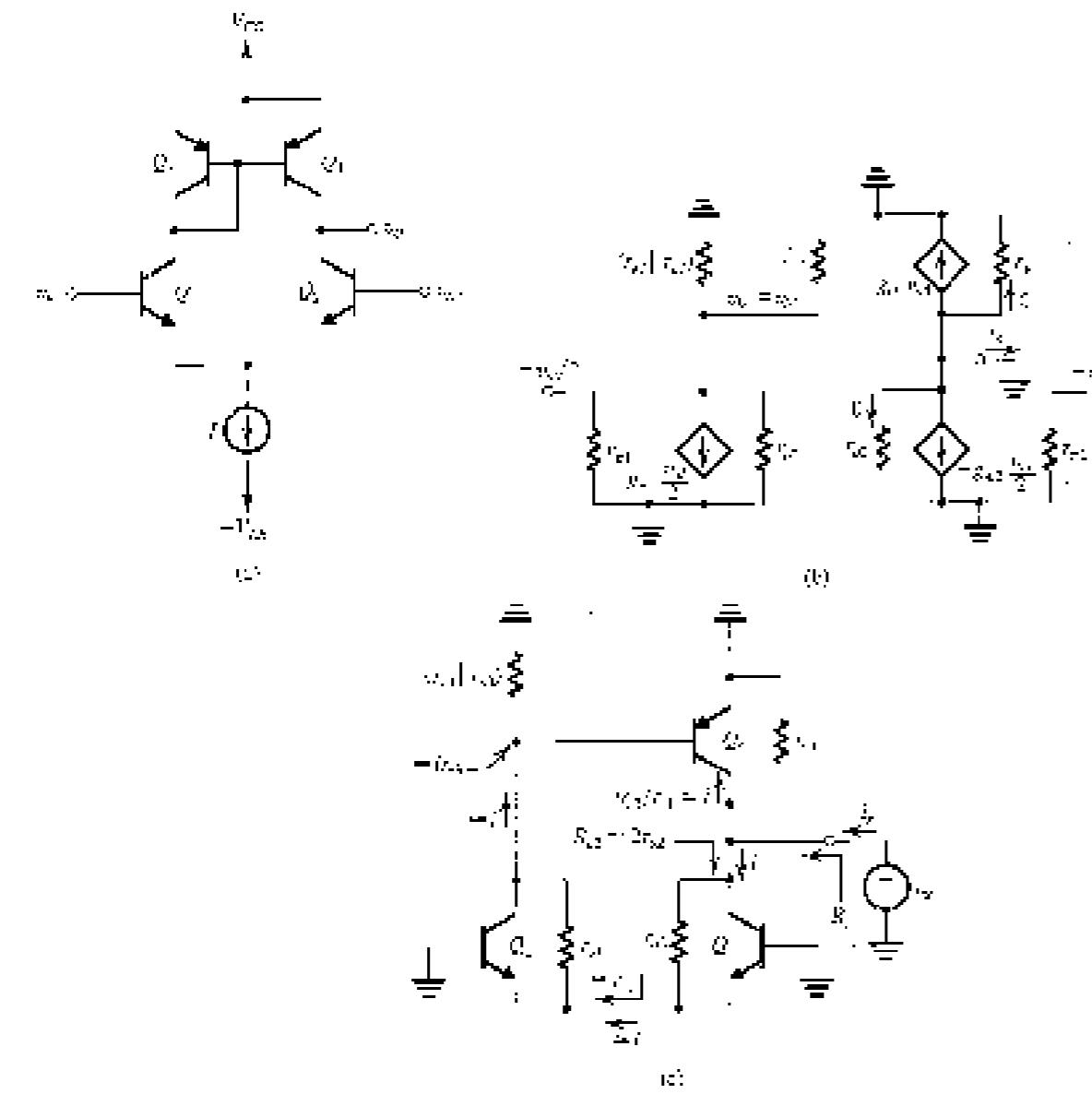


FIGURE 7.32 (a) Active-loaded bipolar differential pair; (b) Small-signal equivalent circuit for determining \$G_d = v_{os}/(v_{in1} - v_{in2})\$; (c) Equivalent circuit for determining the output resistance \$R_o = v_{os}/i\$.

case, \$r_{o1}\$ for the time being, however, we shall ignore the effect of finite \$\beta\$ on the analysis of the four-transistor case and assume that at equilibrium all transistors are operating in the current of \$I/2\$.

Differential Gain To obtain an expression for the differential gain, we apply an input differential signal \$v_{in1} - v_{in2}\$ shown in the equivalent circuit in Fig. 7.32(b). Note that the output is connected to ground in order to determine the overall short-circuit transconductance \$G_d = v_{os}/(v_{in1} - v_{in2})\$. Also, as in the MOS case, we have assumed that the circuit is sufficiently linear so that a virtual ground develops at the common-emitter terminal. This assumption is predicated on the fact

the line voltage signal at the collector of \$Q_1\$ will be small as a result of the low resistance between its emitter and ground (approximately equal to \$r_{o1}\$). The voltage \$v_{os}\$ can be found from

$$\begin{aligned} v_{os} &= -g_{m1}\left(\frac{r_{o2}}{2}\right)(v_{in1} - v_{in2})\parallel r_{o1} \parallel r_{o2} \\ &= g_{m1}r_{o1}\left(\frac{r_{o2}}{2}\right) \end{aligned} \quad (7.156)$$

Since \$r_{o1} = r_{o2}\$, the collector current of \$Q_1\$ will be

$$g_{m1}r_{o1} = -g_{m1}g_{m2}r_{o2}\left(\frac{r_{o2}}{2}\right) \quad (7.157)$$

The output current \$i_o\$ can be found from a node equation at the outputs:

$$i_o = g_{m2}\left(\frac{r_{o1}}{2}\right) = g_{m2}r_{o1} \quad (7.158)$$

Using Eq. (7.157) we obtain

$$i_o = g_{m1}\left(\frac{r_{o2}}{2}\right) = g_{m1}g_{m2}(r_{o1}\parallel\frac{r_{o2}}{2}) \quad (7.159)$$

Since all devices are operating at the same bias current, \$g_{m1} = g_{m2} = g_{mH} = g_m\$, where

$$g_m \triangleq \frac{I/2}{V_T} \quad (7.160)$$

and \$r_{o1} = \alpha_1/g_{m1} = \alpha_2/g_{m2} = 1/g_m\$. Thus, for \$G_d\$, Eq. (7.157) yields

$$G_d = g_m \quad (7.161)$$

which is identical to the result found for the MOS pair.

Next we determine the output resistance of the amplifier utilizing the equivalent circuit shown in Fig. 7.32(c). We urge the reader to carefully examine this circuit and to note that the analysis is very similar to that for the MOS pair. The output resistance \$R_o\$ of transistor \$Q_1\$ can be found using Eq. (6.160) by noting that the resistance \$R_1\$ in the emitter of \$Q_1\$ is approximately equal to \$r_{o1}\$, thus

$$\begin{aligned} R_o &= r_{o1}\parallel(g_{m1}(r_{o2}\parallel r_{o1})) \\ &\approx r_{o1}\parallel r_{o2} = r_{o1}r_{o2} \\ &= 2r_{o1} \end{aligned} \quad (7.162)$$

where we made use of the fact that corresponding parameters of all four transistors are equal.

The current \$i_o\$ can now be found as

$$i_o = \frac{R_o}{R_{o1}} = \frac{R_o}{2r_{o1}} \quad (7.163)$$

and the current \$i_1\$ can be obtained from a node equation at the output:

$$i_1 = 2i_o - \frac{v_{os}}{r_{o1}} = \frac{v_{os}}{r_{o1}} + \frac{v_{os}}{r_{o2}}$$

Thus,

$$R_o = \frac{v_{os}}{i_1} = r_{o1}\parallel r_{o2} \quad (7.164)$$

This expression simply says that the output resistance of the amplifier is equal to the parallel equivalent of the output resistance of the differential pair and the output resistance of the current source, a result identical to that obtained for the MOS pair.

Equations (7.161) and (7.162) can now be combined to obtain the differential gain,

$$A_d = \frac{v_o}{v_{in}} = g_{m1} R_o = g_{m1}(r_{ds1} \parallel r_{ds2}) \quad (7.163)$$

and since $r_{ds1} = r_{ds2} = r_{ds}$, we can similarly Eq. (7.163) to:

$$A_d = \frac{g_{m1}}{r_{ds}} v_{in} \quad (7.164)$$

Although this expression is identical to that found for the MOS circuit, the gain here is much larger because g_{m1} for the BJT is more than an order of magnitude greater than g_{m1} in MOSFET. The downside, however, lies in the low input resistance of BJT amplifiers. Indeed, the equivalent circuit of Fig. 7.32(b) indicates that, as expected, the differential input resistance of the differential amplifier is equal to $2r_{ds}$,

$$R_{in} = 2r_{ds} \quad (7.165)$$

In sharp contrast to the infinite input resistance of the MOS amplifier. Thus, while the voltage gain realized in a source-loaded amplifier stage is large, when a subsequent stage is connected to the output, its inevitably low input resistance will drastically reduce the overall voltage gain.

Common-Mode Gain and CMRR The common-mode gain A_{cm} and the common-mode rejection ratio (CMRR) can be found following a procedure identical to that utilized in the MOS case. Figure 7.33 shows the circuit prepared for common-mode signal analysis. The collector currents of Q_1 and Q_2 are given by

$$i_1 = i_2 = \frac{v_{cc}}{2R_{in}} \quad (7.166)$$

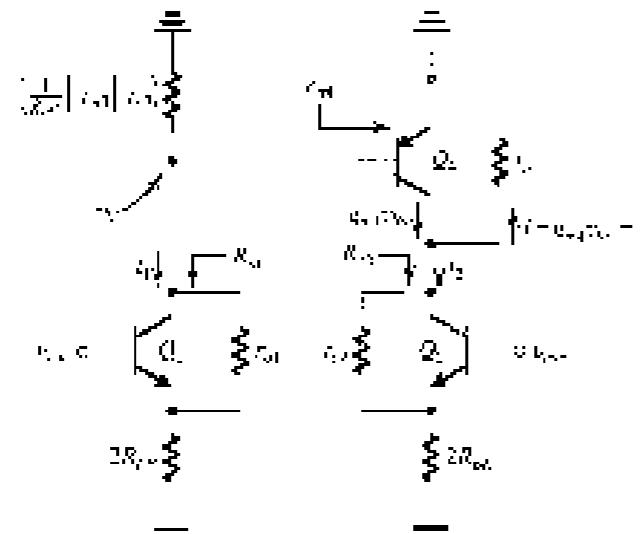


FIGURE 7.33 Analysis of the bipolar source-loaded differential amplifier for the common-mode gain.

It can be shown that the output resistances of Q_1 and Q_2 , R_{ds1} and R_{ds2} , are very large and hence can be neglected. Then, the voltage v_{ce} at the common-base connection of Q_1 and Q_2 can be found by multiplying i_1 by the total resistance between the common-base node and ground as

$$v_{ce} = -i_1 \left(\frac{1}{2r_{ds1}} + r_{ds2} + r_{ds1} \right) \quad (7.167)$$

In response to v_{ce} , transistor Q_2 provides a collector current $g_{m2} v_{ce}$. At the output node we have

$$i_o = (-g_{m2} v_{ce} - i_1) R_{ds2} \quad (7.168)$$

Substituting for v_{ce} from Eq. (7.167) and the i_1 and i_2 from Eq. (7.166) gives

$$\begin{aligned} A_{cm} &= \frac{i_o}{v_{in}} = \frac{r_{ds1}}{2R_{in}} \left[2 + \left(\frac{1}{2r_{ds1}} + r_{ds2} + r_{ds1} \right) - 1 \right] \\ &= \frac{r_{ds1}}{2R_{in}} \frac{\frac{1}{2} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}}{\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}} \end{aligned} \quad (7.169)$$

where we have assumed $g_{m2} = g_{m1}$. Now, for $r_{ds1} = r_{ds2} = r_{ds}$, Eq. (7.169) gives

$$\begin{aligned} A_{cm} &= \frac{r_{ds1}}{2R_{in} g_{m1}} \frac{\frac{1}{2}}{\frac{1}{r_{ds1}}} \\ &= -\frac{r_{ds1}}{2R_{in} g_{m1}} \frac{2}{3} = -\frac{r_{ds1}}{3R_{in} g_{m1}} \end{aligned} \quad (7.170)$$

Using A_d from Eq. (7.164) enables us to obtain the CMRR as

$$\text{CMRR} = \frac{A_d}{A_{cm}} = g_{m1} r_{ds1} \parallel r_{ds2} \left(\frac{R_{ds1} R_{ds2}}{r_{ds1} + r_{ds2}} \right) \quad (7.171)$$

For $r_{ds1} = r_{ds2} = r_{ds}$

$$\text{CMRR} = \frac{1}{3} g_{m1} R_{ds} \quad (7.172)$$

from which we observe that to obtain a large CMRR, the circuit implementing the bias current source should have a large output resistance R_{ds} . This is possible with, say, a Wilson current mirror (Section 6.12.3).

EXERCISE

- 7.13. Design a source-loaded differential amplifier with a differential gain of $A_d = 100$ and a CMRR of $\text{CMRR} = 100$. Assume that the transistors have a $f_T = 100$ MHz and a $g_m = 10 \mu\text{A/V}$.

- 7.14. Design a source-loaded differential amplifier with a differential gain of $A_d = 100$ and a CMRR of $\text{CMRR} = 100$. Assume that the transistors have a $f_T = 100$ MHz and a $g_m = 10 \mu\text{A/V}$.

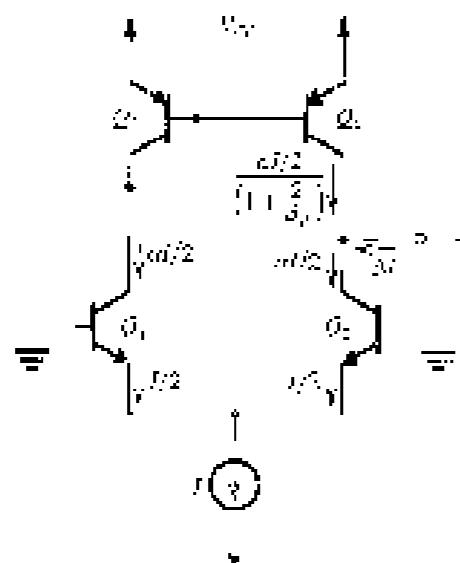


FIGURE 7.34 The two-balanced HBT differential pair. V_{in} is the system-wide input offset voltage resulting from the error in the current-mirror ratio of the current mirror.

Systematic Input Offset Voltage. In addition to the random offset voltages that result from the transistors inevitably present in the differential amplifier, the active-loaded bipolar differential pair suffers from a systematic offset voltage. This is due to the error in the current transfer ratio of the current-mirror load caused by the finite β of the pnp transistors that make up the mirror. To see how this occurs about, refer to Fig. 7.34. Here the inputs are symmetrized and the transistors are assumed to be perfectly matched. That is, the bias current I will divide equally between Q_1 and Q_2 with the result that their two collectors conduct equal currents of $\alpha I/2$. The collector current of Q_1 is fed to the input of the current mirror. From Section 6.3 we know that the current-transfer ratio of the mirror is

$$\frac{I_1}{I_2} = \frac{1}{1 + \frac{2}{\beta_p}} \quad (7.170)$$

where β_p is the value of β of the pnp transistors Q_3 and Q_4 . Thus the collector current of Q_2 will be

$$I_2 = \frac{\alpha I/2}{1 + \frac{2}{\beta_p}} \quad (7.171)$$

which does not exactly balance the collector current of Q_1 . It follows that the current difference ΔI will flow into the output terminal of the amplifier with

$$\begin{aligned} \Delta I &= \frac{\alpha I}{2} - \frac{\alpha I/2}{1 + \frac{2}{\beta_p}} \\ &= \frac{\alpha I \cdot 2 \cdot \beta_p}{2 + \frac{2}{\beta_p}} \\ &= \frac{\alpha I}{\beta_p} \end{aligned} \quad (7.172)$$

To reduce this output current to zero, an input voltage V_{in} has to be applied with a value of

$$V_{in} = \frac{\Delta I}{G_v} \quad (7.173)$$

Substituting for ΔI from Eq. (7.172) and for $G_v \approx g_m = (\alpha I/2)/V_T$, we obtain for the input offset voltage the expression

$$V_{in} = \frac{\alpha I/\beta_p}{\alpha I/2 V_T} = \frac{2 V_T}{\beta_p} \quad (7.174)$$

As an example, let $\beta_p = 50$, $V_T = -1$ mV. To reduce V_{in} , an improved current mirror such as the Wilson circuit studied in Section 6.12 should be used. Such a circuit provides the added advantage of increased output resistance and hence voltage gain. However, to realize the full advantage of the higher output resistance of the active load, the output resistance of the differential pair should be raised by utilizing a cascode stage. Figure 7.35 shows such an arrangement. A folded cascode stage formed by pnp transistors Q_3 and Q_4 is utilized to raise the output resistance looking into the collector of Q_1 to R_{out} . A Wilson mirror formed by transistors Q_5 , Q_6 , and Q_7 is used to implement the active load. From Section 6.12.3 we know that the output resistance of the Wilson mirror (i.e., looking into the collector of Q_8) is $\beta_w(r_o/2)$. Thus the output resistance of the amplifier

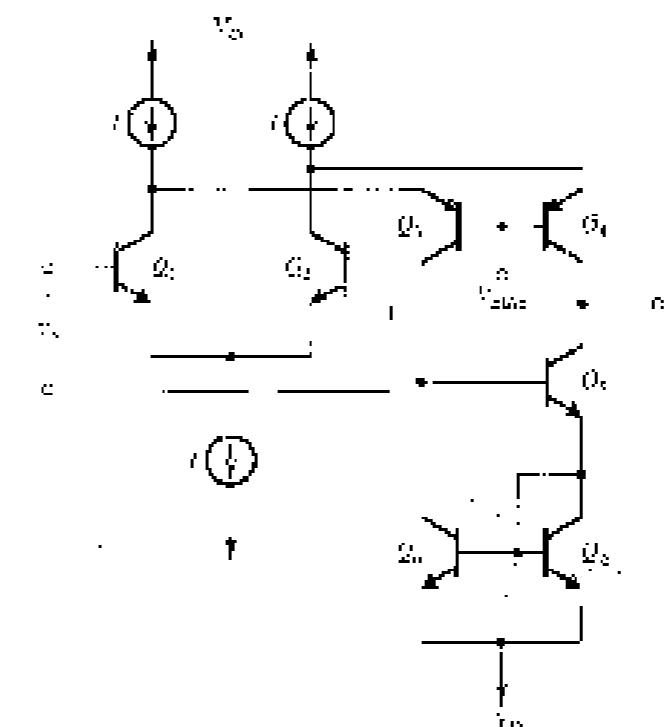


FIGURE 7.35 A balanced bipolar differential amplifier employing a folded cascode stage (Q_3 and Q_4) and a Wilson mirror active load (Q_5 , Q_6 , and Q_7).

is given by

$$R_o = \left(\beta_2 r_{ds} + \beta_1 \frac{r_{ds}}{2} \right) \quad (7.17b)$$

The transconductance G_m remains same as r_{ds} of Q_2 and Q_1 due the differential voltage gain becomes

$$A_d = g_m \left(\beta_2 r_{ds} + \beta_1 \frac{r_{ds}}{2} \right) \quad (7.18b)$$

which can be very large. Further examples of improved performance circuit architectures will be studied in Chapter 9.

EXERCISE

- 7.14. Consider the differential pair of Fig. 7.15(b) with the following parameters:
 $\beta_1 = \beta_2 = 100$,
 $V_{DD} = 10$,
 $V_{SS} = -10$,
 $r_{ds1} = r_{ds2} = 100$,
 $C_{gs1} = C_{gs2} = 100$,
 $C_{gd1} = C_{gd2} = 10$,
 $C_{ds1} = C_{ds2} = 10$,
 $C_{od} = 10$.
 Find the differential gain A_d and CMRR.

7.6 FREQUENCY RESPONSE OF THE DIFFERENTIAL AMPLIFIER

In this section we study the frequency response of the differential amplifier. We will consider the variation with frequency of both the differential gain and the common-mode gain and hence of the CMRR. We will rely heavily on the study of frequency response of single-ended amplifiers presented in Chapter 6. Also, we will only consider MOS circuits. The bipolar case is straightforward extension, as we saw on a number of occasions in Chapter 6.

7.6.1 Analysis of the Resistively Loaded MOS Amplifier

We begin with the basic, resistively loaded MOS differential pair shown in Fig. 7.36(a). Note that we have explicitly shown the transistor Q_3 that supplies the bias current I . Although we are showing a dc bias voltage V_{bias} at the gate, usually Q_3 is part of a current mirror. This detail, however, is of no consequence to our present needs. Most importantly, we are interested in the load impedance between node S and ground, Z_{WS} . As we shall shortly see, this impedance plays a significant role in determining the common-mode gain and the CMRR of the differential amplifier. Resistance R_{DS} is simply the output resistance of current source Q_2 . Capacitance C_{WS} is the total capacitance between node S and ground and includes C_{ds2} and C_{od} of Q_2 , as well as C_{gs1} and C_{gd1} .

The differential half-circuit shown in Fig. 7.36(b) can be used to determine the frequency dependence of the differential gain V_o/V_{ds} . Indeed the gain function $A_d(s)$ of the differential amplifier will be identical to the transfer function of this common-source amplifier. We studied the frequency response of the common-source amplifier at great length in Section 6.6 and will not repeat this material here.

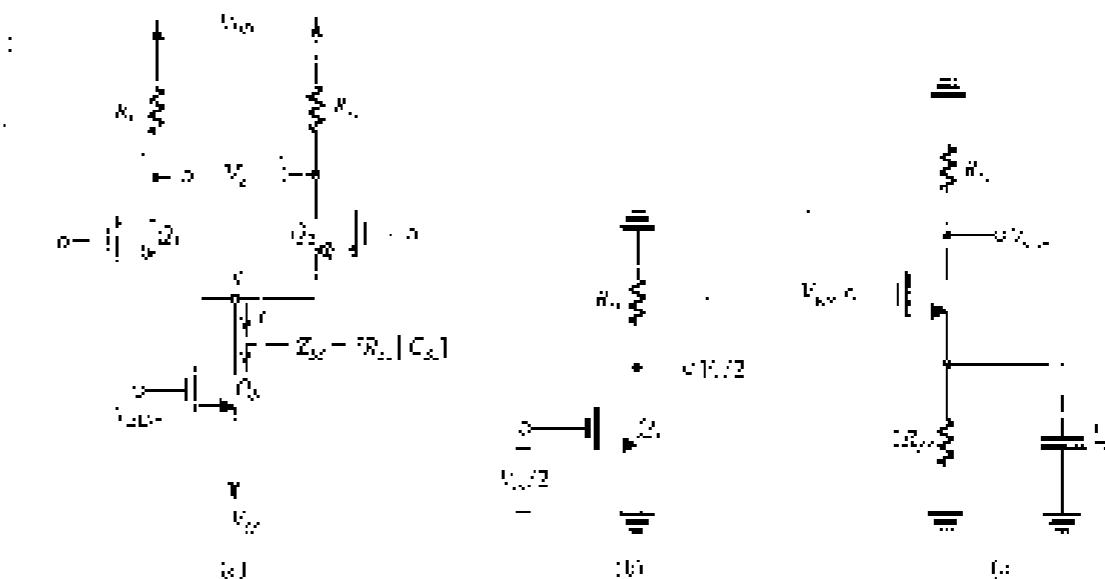


FIGURE 7.36 (a) Resistively loaded MOS differential pair with the bias star supplying the bias current explicitly shown. It is assumed that the drain–source voltage between node S and \$Q_2\$ is \$V_{ds2} = V_{bias} - I R_{DS}\$. (b) Differential half-circuit. (c) Common-mode half-circuit.

EXERCISE

- 7.15. Consider the differential pair of Fig. 7.36(a) with the following parameters:
 $\beta_1 = \beta_2 = 100$,
 $V_{DD} = 10$,
 $V_{SS} = -10$,
 $r_{ds1} = r_{ds2} = 100$,
 $C_{gs1} = C_{gs2} = 100$,
 $C_{gd1} = C_{gd2} = 10$,
 $C_{ds1} = C_{ds2} = 10$,
 $C_{od} = 10$.
 Find the differential gain A_d and CMRR.

The common-mode half-circuit is shown in Fig. 7.36(c). Although this circuit has other capacitances, namely C_{gs3} , C_{gd3} , and C_{od} of the transistor in addition to other stray capacitances, we have chosen to show only $C_{od}/2$. This is because $(C_{od}/2)$ together with (CR_s) forms a real-axis zero in the common-mode gain function at a frequency much lower than those of the other poles and zeros of the circuit. This zero then dominates the frequency dependence of the CMRR.

If the output of the differential amplifier is taken single-endedly, then the common-mode gain of interest is V_{o1}/V_{ds1} . More typically, the output is taken differentially. Nevertheless,

as we have seen in Section 7.3, V_{GS1}/V_{GS2} still plays a major role in determining the common-mode gain. To be specific, consider what happens when the output is taken differentially and there is a mismatch ΔR_D between the two drain resistances. The resulting common-mode gain is found in Section 7.3 to be (Eq. 7.51)

$$A_{CM} = \frac{R_D (\Delta R_D)}{2(R_{DS1} + R_{DS2})} \quad (7.81)$$

which is simply the product of V_{GS1}/V_{GS2} and the per-unit mismatch ($\Delta R_D/R_{DS}$). Similar expressions can be found for the effects of other circuit imbalances. The important point to note is that the factor $R_D/(2R_{DS})$ is always present in these expressions. Thus, the frequency dependence of A_{CM} can be obtained by simply replacing R_{DS} by Z_{DS} in this factor. Doing so for the expression in Eq. 7.181 gives

$$\begin{aligned} A_{CM}(s) &= \frac{R_D (\Delta R_D)}{2Z_{DS1} + R_D} \\ &= \frac{1}{2} \frac{R_D (\Delta R_D)}{R_D + R_{DS}} Y_{DS} \\ &= \frac{1}{2} \frac{R_D (\Delta R_D)}{R_D + R_{DS}} \left(1 + sC_{DS} \right)^{-1} \\ &= \frac{R_D (\Delta R_D)}{2R_{DS}} \left(1 + sC_{DS}R_{DS} \right)^{-1} \end{aligned} \quad (7.82)$$

from which we see that A_{CM} acquires a zero on the negative real-axis of the s -plane with frequency ω_2 ,

$$\omega_2 = \frac{1}{C_{DS}R_{DS}} \quad (7.83)$$

or in terms,

$$\omega_2 = \frac{\omega_2}{2\pi} = \frac{1}{2\pi C_{DS}R_{DS}} \quad (7.84)$$

As mentioned above, usually ω_2 is much lower than the frequencies of the other poles and zeros. As a result, the common-mode gain increases at the rate of -6 dB/octave (20 dB decade) starting at a relatively low frequency, as indicated in Fig. 7.37(a). Of course, A_{CM} drops off at high frequencies because of the other poles of the common-mode h_{FE} circuit. It is, however, f_2 that is significant for it is the frequency at which the CMRR of the differential amplifier begins to decrease, as indicated in Fig. 7.37(c). Note that if both A_V and A_{CM} are expressed and plotted in dB, then CMRR in dB is simply the difference between A_V and A_{CM} .

Although in the foregoing we considered only the common-mode gain resulting from an R_D mismatch, it should be obvious that the results apply to the common-mode gain resulting from any other mismatch. For instance, it applies equally well to the case of r_{DS} mismatch, multiplying Eq. 7.61 by replacing R_{DS} by Z_{DS} and so on.

Before leaving this section, it is interesting to point out an important trade-off involved in the design of the current-source transistors (Q_3): in order to operate this current source with a small V_{GS3} to conserve the already low V_{GS1} , we desire to operate the transistor in a low-overdrive voltage V_{OD} . For a given value of the current I , however, this means using a large W/L ratio (i.e., a wide transistor). This in turn increases C_{GS} and hence lowers f_2 with the result that the CMRR degrades (i.e., decreases) at relatively low frequency. Thus there is

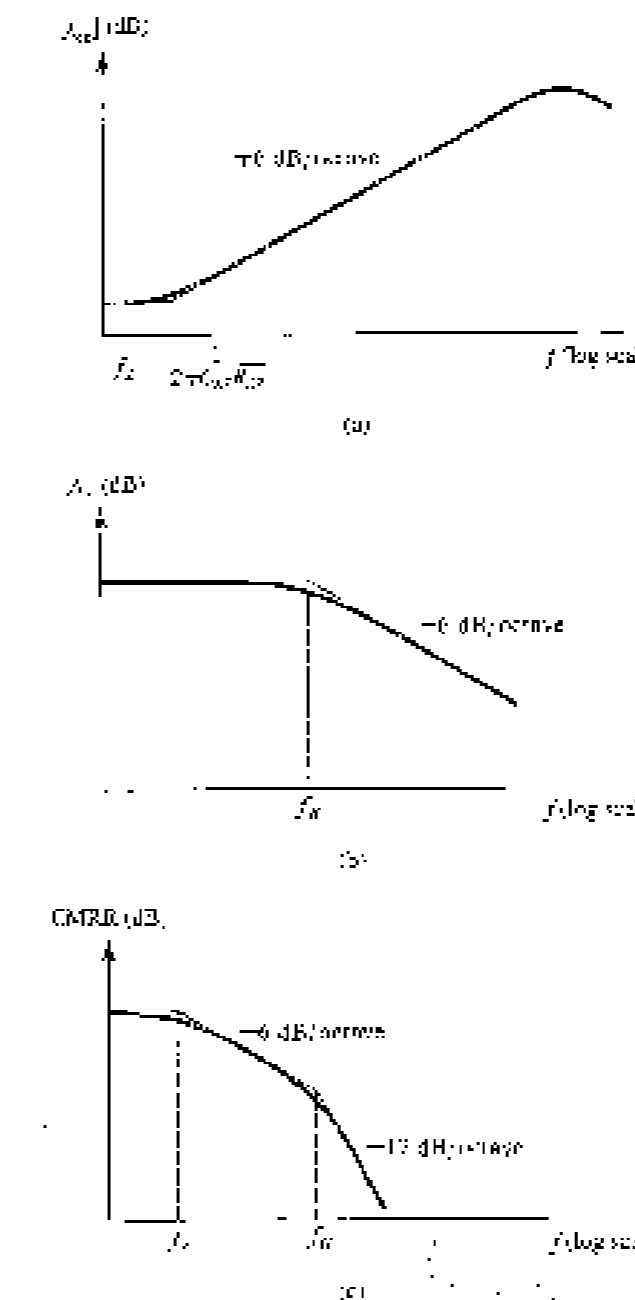


FIGURE 7.37 Variation of (a) open-circuit gain, (b) differential gain, and (c) common-mode rejection ratio with frequency.

trade-off between the need to reduce the dc voltage across Q_3 and the need to keep the CMRR reasonably high at higher frequencies.

To appreciate the need for high CMRR at higher frequencies, consider the situation illustrated in Fig. 7.38. We show two stages of a differential amplifier whose power-supply voltage V_{DD} is corrupted with high-frequency noise. Since the crossover voltage of each of

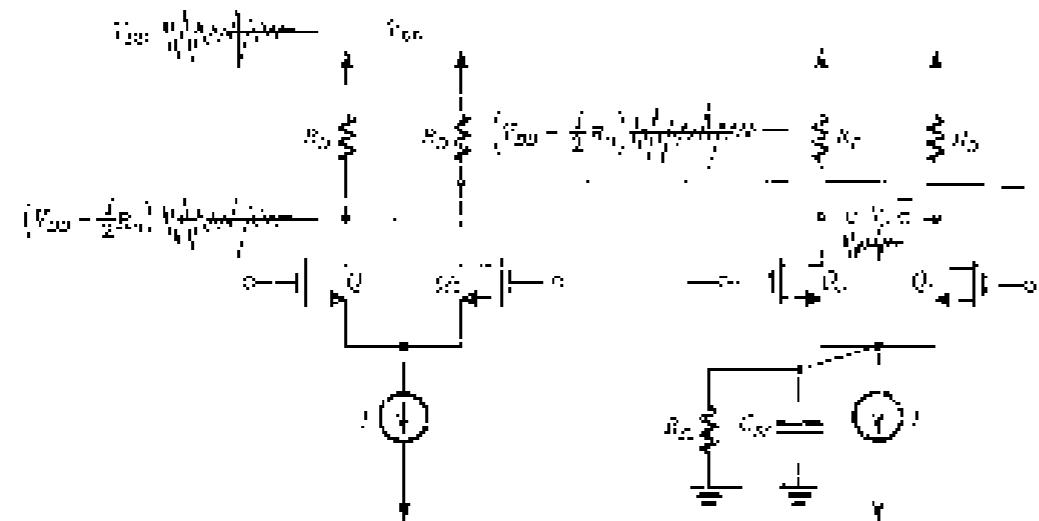


FIGURE 7.38 The second stage in a direct-coupled amplifier is related to the suppression of high-frequency noise caused by the power supply of the first stage, and its other main function is high CMRR at high frequencies.

the drains of Q_1 and Q_2 is $[V_{DD} - (1/2)R_S]$, we see that Q_1 and Q_2 will have the same high-frequency noise as V_{DD} . This high-frequency noise then constitutes a common-mode input signal to the second differential stage, formed by Q_3 and Q_4 . If the second differential stage is perfectly matched, its differential output voltage V_o should be free of high-frequency noise. However, in practice there is no such thing as perfect matching and the second stage will have a finite common-mode gain. Furthermore, because of the zero formed by R_{SD} and C_{SS} at the second stage, the common-mode gain will increase with frequency, causing some of the noise to track its way to V_o . With careful design, this undesirable component of V_o can be suppressed.

EXERCISE

- 7.16. इन्हें लाने की जगह तो आपका विकास करने की जगह है। यह एक अच्छी बात है। लेकिन यह लापता की जगह नहीं।

7.6.2 Analysis of the Active-Loaded MOS Amplifier

We next consider the frequency response of the current-mirror-loaded MOS differential pair circuit for f_{RF} in Section 7.5. The circuit is shown in Fig. 7.36(a) with two capacitances indicated: C_{in} , which is the total capacitance at the input node of the current mirror, and C_{out} , which is the total capacitance at the output node. Capacitance C_{in} is mainly formed by C_{gnd} and C_{in} , but also includes C_{gg} , C_{gm} , and C_{gd} .

$$C_{\text{st}} = C_{\text{st}1} + C_{\text{st}2} - C_{\text{st}3} + C_{\text{st}4} - C_{\text{st}5} \quad (3.18)$$

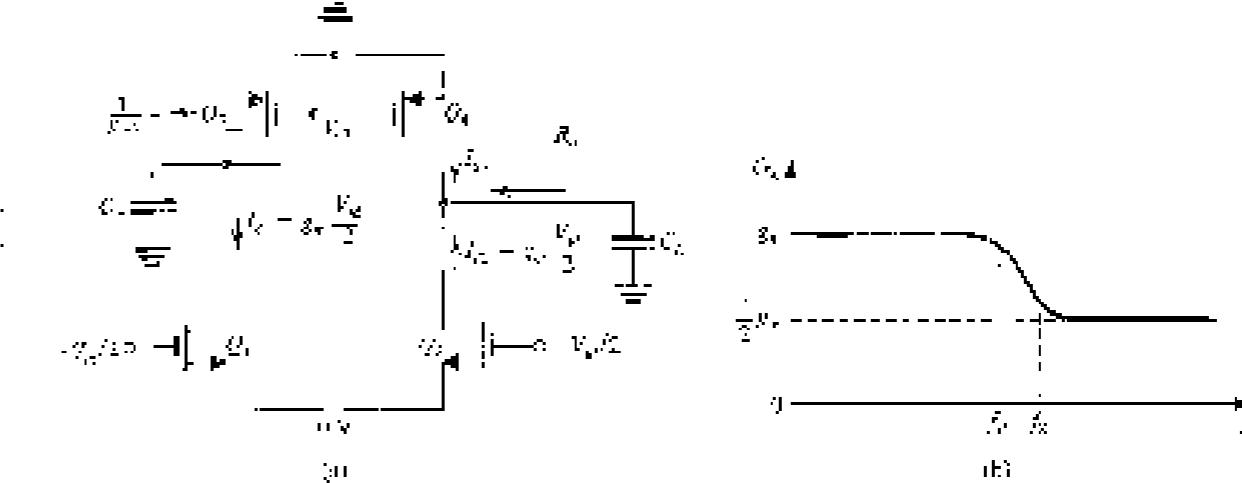


FIGURE 7.35 (a) Frequency-response analysis of the active-loaded MOS differential pair (b) T₁ vs. full transconductance G_m over the initial frequency.

Capacitance C_2 includes C_{in} , C_{out} , C_{load} and the input capacitance and/or the input capacitance of a subsequent stage (C_3).

$$C_1 = C_{\text{exp}} + C_{\text{opt}} + C_{\text{err}} - C_{\text{sys}} - C_s \quad (7.46)$$

These two capacitances primarily determine the dependence of the differential gain of this amplifier on frequency.

As indicated in Fig. 11.39(a) the input differential signal V_{in} is applied in a balanced fashion. Transistor Q_1 will conduct a drain current signal of $v_o / V_{DD} / 2$, which flows through the diode connected transistor Q_2 and then through the parallel combination of $1/(2g_m)$ and C_{in} , where we have replaced the resistances r_o and c_o which are given after Eq. (11.1). This

$$V_{\text{eff}} = \frac{E_0 N_0 / 2}{\pi^2 \tau^2 \delta C} \quad (1.187)$$

En revanche, le $V_{\text{d}} \cdot \text{projet}_1$ (\mathcal{Q} , symétrique à \mathcal{P}) n'est pas un \mathcal{L} .

$$J_{xz} = -g_{eA} V_{xz} + \frac{g_{eA} g_A V_{xz}}{g_{eA} + g_A}$$

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$$J_{\zeta} = \frac{q_0 B_0 / 2}{1 + r \frac{C_0}{B_0}} \quad .1186$$

Note: at the annual rate for total current assets.

$$\frac{Z_0 E_{12}/2}{C} = E_{11}(E_{12}/2) \quad (7.186)$$

which flows through the parallel combination of $R_s = r_{sd}||r_{sd}$ and C_2 , thus

$$I_s = I_d \frac{1}{1 + sC_2R_s} \quad (7.189)$$

Substituting for I_s from Eq. (7.189) gives

$$V_o = R_s R_{cs} \frac{V_{DD}}{2} \left[1 + \frac{1}{1 + s\frac{C_2}{R_s}} \right] \frac{1}{1 + sC_1R_s}$$

which can be manipulated to yield

$$A_v(s) = \frac{V_o}{V_{in}} = (R_s R_{cs}) \frac{1}{(1 + sC_1R_s)} \frac{-s \frac{C_2}{R_s}}{1 + s \frac{C_2}{R_s}} \quad (7.191)$$

We recognize the first factor on the right-hand side as the dc gain of the amplifier. The second factor indicates that C_2 and R_s form a pole with frequency f_{p2} .

$$f_{p2} = \frac{1}{2\pi C_2 R_s} \quad (7.192)$$

This, of course, is a entirely expected result, and in fact this corner pole is often dominant, especially when a large load capacitance is present. The third factor on the right-hand side of Eq. (7.191) indicates that the capacitance C_1 at the input of the current mirror gives rise to a pole with frequency f_{p1} ,

$$f_{p1} = \frac{R_{cs}}{2\pi C_1} \quad (7.193)$$

and a zero with frequency f_{z1} ,

$$f_z = \frac{2R_{cs}}{2\pi C_1} \quad (7.194)$$

That is, the zero frequency is twice that of the pole. Since C_1 is approximately $C_{es} = \Gamma_{gsd}/2M_{1,2,3}$,

$$f_z = \frac{\Gamma_{gsd}}{2\pi(2M_{1,2,3})} = f_p f_c/2 \quad (7.195)$$

and

$$f_p > f_c \quad (7.196)$$

where f_c is the frequency at which the magnitude of the high-frequency current gain of the MOSFET becomes unity (see Sections 4.8 and 6.2). Thus, the multiple pole and zero occur at very high frequencies. Nevertheless, their effect can be significant.

It is interesting and useful to observe that the pole of the signal current produced by Q_1 has a transfer function different from that of the signal current produced by Q_2 . It is the first signal that encounters C_{1a} and experiences the major pole. This observation leads to an interesting view of the effect of C_{1a} on the overall transconductance G_{av} of the differential amplifier. As we learned in Section 7.5, at low frequencies f_{p1} is replicated by the minor Q_2 . Q_2 is the collector of Q_1 , so f_{p1} which adds to f_{p2} to provide a factor-of-2 increase in G_{av} (thus making G_{av} equal

to \tilde{g}_{m2} , which is double the value available without the current mirror). Now, at high frequency C_{1a} acts as a short circuit causing V_{o2} to be zero and hence I_{d2} will be zero, reducing G_{av} to $\tilde{g}_{m2}/2$. Thus, if the output is short-circuited to ground and the short-circuit transconductance G_{av} is plotted versus frequency, the plot will have the shape shown in Fig. 7.56(b).



Consider an active-loaded MOS differential amplifier of the type shown in Fig. 7.28(a). Assume the two NMOS transistors, $M1 = M2 = 7.2 \text{ } \mu\text{m} \times 36 \text{ } \mu\text{m}$, $C_{gs} = 20 \text{ fF}$, $C_{gd} = 5 \text{ fF}$, and $C_{ds} = 5 \text{ fF}$. Also, let $\mu_n C_{ss} = 387 \text{ } \mu\text{A/V}^2$, $\mu_p C_{ss} = 46 \text{ } \mu\text{A/V}^2$, $V_{th} = 5 \text{ V}/\mu\text{A}$, $V_{DD} = 6 \text{ V}/\mu\text{A}$. The bias current $I = 0.2 \text{ mA}$, and the bias current source has an output resistance $R_{os} = 25 \text{ k}\Omega$ and an output conductance $G_{os} = 0.2 \text{ S}$. In addition to the capacitances introduced by the transistors at the output node, there is a capacitance C_L of 35 pF . It is required to determine the low-frequency values of A_{vL} , A_{vH} , and CMRR. It is also required to find the poles and zeros in A_{vL} and the dominant pole of CMRR.

Solution

Since $I = 0.2 \mu\text{A}$, each of the two transistors is operating in a bias current of $100 \mu\text{A}$. Thus, for Q_1 and Q_2 ,

$$\tilde{g}_{m1} = \frac{1}{2} \times 387 \times \frac{7.2}{0.1} \times 100 \text{ } \mu\text{A} \text{,}$$

which leads to

$$V_{DD} = 0.16 \text{ V}$$

Thus,

$$g_{m1} = g_{m2} = g_{os} = \frac{2 \times 0.1}{0.16} = 1.25 \text{ mA/V}$$

$$r_{sd} = r_{os} = \frac{5}{0.1} = 50 \text{ k}\Omega$$

For Q_3 and Q_4 we have

$$\tilde{g}_{m3} = \frac{1}{2} \times 36 \times \frac{7.2}{0.1} \times 100 \text{ } \mu\text{A} \text{,}$$

thus,

$$V_{O3,4} = 0.34 \text{ V}$$

and

$$g_{m3} = g_{m4} = \frac{2 \times 0.1}{0.34} = 0.6 \text{ mA/V}$$

$$r_{sd} = r_{os} = \frac{6 \times 0.1}{0.1} = 21.6 \text{ k}\Omega$$

The low-frequency value of the differential gain can be determined from

$$A_{vL} = g_{m1}(r_{sd} + r_{os}) \\ \approx 1.25(50 + 50) = 12.5 \text{ V/V}$$

The low-frequency value of the common-mode gain can be determined from Eq. (7.152) as

$$\begin{aligned} A_{cm} &= \frac{1}{2R_{in}R_{out}} \\ &= \frac{1}{2 \times 0.6 \times 24} = -0.033 \text{ V/V} \end{aligned}$$

The low-frequency value of the CMRR can be determined as

$$\text{CMRR} = \frac{|A_v|}{|A_{cm}|} = \frac{12.2}{0.033} = 369$$

or

$$20 \log 369 = 51.2 \text{ dB}$$

To determine the poles and zero of A_v , we first compute the values of the non-potential bypass capacitors C_2 and C_3 . Using Eq. (7.184),

$$\begin{aligned} C_2 &= C_{2d1} + C_{2d2} + C_{2s1} + C_{2s2} \\ &= 5 + 5 + 20 + 20 = 50 \text{ pF} \end{aligned}$$

Similarly, C_3 is found using Eq. (7.184) as

$$\begin{aligned} C_3 &= C_{3d1} + C_{3d2} + C_{3s1} + C_{3s2} + C_s \\ &= 5 + 5 + 5 + 20 + 45 = 70 \text{ pF} \end{aligned}$$

Now, the poles and zero of A_v can be found from Eqs. (7.192) and (7.197) as

$$\begin{aligned} f_p &= \frac{1}{2\pi C_2 R_{out}} \\ &= \frac{1}{2\pi \times 50 \times 24 \times 10^6} \\ &= \frac{1}{2\pi \times 15 \times 10^{-12} \times 24 \times 10^6} \\ &= 330 \text{ MHz} \\ f_{z1} &= \frac{f_{p1}}{\frac{A_{v1}}{2\pi C_s}} = \frac{0.6 \times 10^{-3}}{2\pi \times 25 \times 10^{-12}} = 3.7 \text{ GHz} \\ f_z &= 2f_{z1} = 7.4 \text{ GHz} \end{aligned}$$

Thus, the dominant pole is not produced by C_s at the output node. As expected, the pole and zero of the circuit are all under the influence.

The dominant pole of the CMRR is at the location of the conductance-mode-zero introduced by C_{2s} and R_{out} (Eq. 7.184).

$$\begin{aligned} f_p &= \frac{1}{2\pi C_{2s} R_{out}} \\ &= \frac{1}{2\pi \times 0.2 \times 10^{-3} \times 25 \times 10^6} \\ &= 31.8 \text{ MHz} \end{aligned}$$

Thus, the CMRR begins to decrease at 31.8 MHz, which is much lower than f_p .

EXERCISE

- 7.7.1 Design a two-stage CMOS op-amp with a total voltage gain of 1000. The input stage uses a PMOS differential pair with a transconductance of $10 \mu\text{A}/\text{V}$ and a Miller compensation capacitor of 100 pF . The second stage uses a NMOS differential pair with a transconductance of $10 \mu\text{A}/\text{V}$ and a Miller compensation capacitor of 100 pF . The output stage uses a current mirror with a transconductance of $10 \mu\text{A}/\text{V}$ and a load resistor of $10 \text{ k}\Omega$. The biasing network is to be designed using the current mirror technique. The total power consumption is to be limited to 1 mW .

7.7 MULTISTAGE AMPLIFIERS

Practical transistor amplifiers usually consist of a number of stages connected in cascade. In addition to providing gain, the first (or input) stage is usually required to provide a high input resistance in order to avoid a loss in signal level when the amplifier is fed from a high-resistance source. In a differential amplifier the input stage must also provide large common-mode rejection. The function of the middle stages of an amplifier cascade is to provide the bulk of the voltage gain. In addition, the middle stages provide such other functions as the conversion of the signal from differential mode to single-ended mode (mixing, of course). The output stage also is differentially fed, the shifting of the dc level of the signal is often used to allow the output signal to swing low, positive and negative. These two functions and others will be illustrated later in this section and in greater detail in Chapter 9.

Finally, the main function of the last (or output) stage of an amplifier is to provide a low output resistance in order to avoid loss of gain when a low-impedance load resistance is connected to the amplifier. Also, the output stage should be able to supply the current required by the load in an efficient manner—that is, without dissipating an unneeded large amount of power in the output resistors. We have already studied one type of amplifier configuration suitable for implementing output stages, namely, the source follower and the emitter follower. It will be shown in Chapter 14 that the source and emitter followers are not optimum from the point of view of power efficiency and that other more appropriate circuit configurations exist for output stages that are required to supply large amounts of output power. In fact, we will encounter some such output stages in the op-amps given in Examples 7.10 through 7.12.

To illustrate the circuit structure and the method of analysis of multistage amplifiers, we will present two examples: a two-stage CMOS op-amp and a four-stage bipolar op-amp.

7.7.1 A Two-Stage CMOS Op Amp

Figure 7.17 shows a popular structure for CMOS op-amps known as the two-stage configuration. The circuit utilizes two power supplies, which can range from -2.5 V to the 0.5 V rail with an integrated $+0.9 \text{ V}$ to the 0.18 \mu m technology. A reference bias current I_{ref} is generated either externally or using on-chip circuitry. One such circuit will be discussed shortly. The current mirror formed by Q_1 and Q_2 supplies the differential pair (Q_3, Q_4) with bias current. The W/L ratio of Q_2 is selected to yield the desired value for the input-stage bias current ($I_{ref}/3$) for each of Q_1 and Q_2 . The input differential pair is actively loaded with the current mirror formed by Q_3 and Q_4 . Thus the input stage is identical to that studied in Section 7.2 (except that here the differential pair is implemented with PMOS transistors and the current mirror with NMOS).

The second stage consists of Q_5 , which is a common-source stage differentially loaded with the other source-follower Q_6 . A capacitor C_2 is included in the negative-feedback path of the second stage. Its function is to enhance the Miller effect already present in Q_5 (the effect of the action of $I_{ref} \times C_{ref}$) and thus provide the op-amp with a dominant pole. By the careful placement of

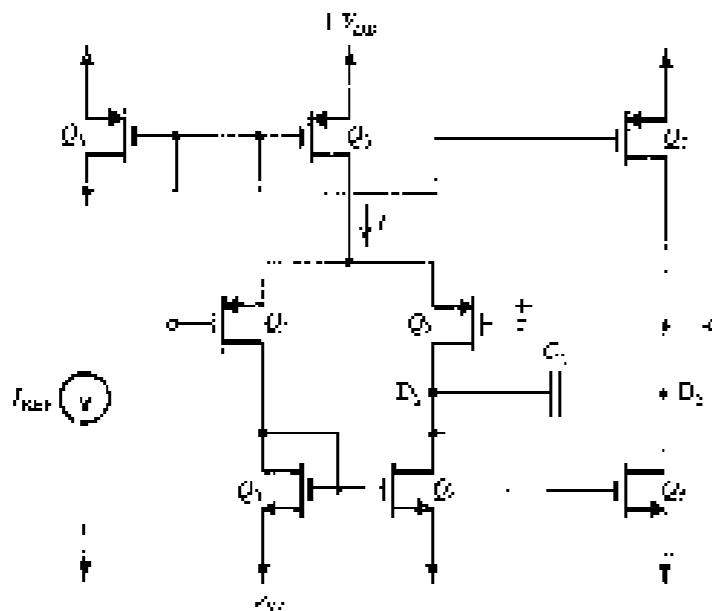


FIGURE 7.40 Two-stage CMOS op-amp configuration.

In this p–n–n op-amp, it can be shown that the gain that decreases with frequency at the rate of $\rightarrow 6$ dB/octave, i.e., equivalently, -20 dB/octade down to unity gain (0 dB). Op-amps with such a gain function are guaranteed to operate in a stable fashion, as opposed to oscillating, with nearly all possible feedback configurations. Such op-amps are said to be *frequency compensated*. We shall study the subject of frequency compensation in Chapters 8 and 9. Here, we will simply take C_f into account in the analysis of the frequency response of the circuit in Fig. 7.40.

A striking feature of the circuit in Fig. 7.40 is that it does not have a low-output resistance stage. In fact, the output resistance of the circuit is equal to $(r_{ds1} \parallel r_{ds2})$ and is thus rather high. This circuit, therefore, is not suitable for driving low-impedance loads. Nevertheless, the circuit is very popular, and is used frequently for implementing op-amps in VLSI circuits where the op-amp needs to drive only a small capacitive load. For example, in switched-capacitor circuits (Chapter 12), the simplicity of the circuit results in an op-amp of reasonably good quality realized in a very small chip area.

Voltage Gain The voltage gain of the first stage was found in Section 7.5 to be given by

$$A_1 = g_{m1}(r_{ds1} + r_{ds2}) \quad (7.197)$$

where g_{m1} is the transconductance of each of the two transistors of the first stage, that is, Q_1 and Q_2 .

The second stage is an inverting \pm loaded common-source amplifier whose low-frequency voltage gain is given by

$$A_2 = -g_{m2}(r_{ds3} + r_{ds4}) \quad (7.198)$$

The dc open-loop gain of the op-amp is the product of A_1 and A_2 ,

* Readers who have studied Chapter 2 will recognize that commercially available op-amps with this uniform gain roll-off of -6 dB/octade are said to be *internally compensated*. The “internal” means that the frequency compensation network is integrated to the package (i.e., chip) and need not be supplied externally by the user. The LM741 op-amp is an example of an internally compensated op-amp.

Consider the circuit in Fig. 7.40 with the following device geometries (in μm):

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
I_{DN}	40.0	30.0	5.0	5.0	40.0	10.0	10.0	40.0
V_{GS}	—	—	—	—	—	—	—	—
V_{DS}	—	—	—	—	—	—	—	—

Let $I_{DN} = 90\ \mu\text{A}$, $V_{GS} = 0.7\ \text{V}$, $V_{DS} = 3.8\ \text{V}$, $\mu_n C_{ox} = 100\ \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 40\ \mu\text{A}/\text{V}^2$, V_{th} (for all devices) = $1.0\ \text{V}$, $V_{DD} = V_{SS} = 2.5\ \text{V}$. For all devices evaluate $|V_{GS}|$, V_{DS} , i_{DS} , and i_{DS} . Also find A_1 , A_2 , the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of C_f on i_{DS} 's current.

Solution

Refer to Fig. 7.40. Since Q_1 and Q_2 are matched, $I = I_{DN}$. Thus, Q_1 , Q_2 , Q_3 , and Q_4 each could draw a current equal to $5.0 \times 45 = 45\ \mu\text{A}$. Since Q_5 is matched to Q_2 and Q_6 , the current in Q_5 is equal to $I_{DN} = 90\ \mu\text{A}$. Finally, Q_7 conducts an equal current of $90\ \mu\text{A}$.

With I_{DN} of each device known, we use

$$I_D = \frac{1}{2} \mu n C_{ox} (W/L) V_{GS}^2$$

to determine V_{GS} for each transistor. From we find $|V_{GS}|$ from $|V_{GS}| = |V_G| + |V_{GS}|$. The results are given in Table 7.1.

The transconductance of each device is estimated from

$$i_D = 2I_D / V_{GS}$$

The value of r_{ds} is determined from

$$r_{ds} = V_{DS} / i_{DS}$$

The resulting values of i_D and r_{ds} are given in Table 7.1.

The voltage gain of the first stage is determined from

$$\begin{aligned} A_1 &= g_{m1}(r_{ds1} + r_{ds2}) \\ &= -0.5(232 \parallel 232) = -32.5\ \text{V/V} \end{aligned}$$

The voltage gain of the second stage is determined from

$$\begin{aligned} A_2 &= -g_{m2}(r_{ds3} + r_{ds4}) \\ &= -0.5(111111) = -55.5\ \text{V/V} \end{aligned}$$

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
$ V_{GS} $ (V)	45	45	45	45	90	10	10	90
V_{DS} (V)	0.3	1.0	0.5	0.5	0.3	0.3	0.3	0.3
V_{DD} (V)	1.0	1.1	1	1	1.1	1	1	1.1
i_{DS} (μA)	0.3	1.0	0.5	0.5	0.3	0.6	0.6	0.3
r_{ds} (Ω)	232	232	232	232	111	111	111	111

Thus the overall dc gain-loop ratio is

$$A_0 = A_1 A_2 = (32.3) \times (-25.9) = -1000 \text{ V/V}$$

or

$$20 \log |A_0| = 60 \text{ dB}$$

The lower limit of the input common-mode range is the value of input voltage at which Q_1 and Q_2 leave the saturation region. This occurs when the input voltage falls below the voltage at the drain of Q_1 by $|V_{th}|$ volts. Since the drain of Q_1 is at $-2.5 + 1 = -1.5$ V, then the lower limit of the input common-mode range is -0.9 V.

The upper limit of the input common-mode range is the value of input voltage at which Q_2 leaves the saturation region. Since for Q_2 to operate in saturation, the voltage across it (i.e., V_{ds}) should at least be equal to the overdrive voltage at which it is operating (i.e., 0.5 V), the highest voltage permitted at the drain of Q_2 should be -2.2 V. It follows that the higher value of v_{in} , denoted as

$$v_{in,high} = -2.2 + 1.1 = -1.1 \text{ V}$$

The highest allowable output voltage is the value at which Q_2 leaves the saturation region, which is $V_{dd} - |V_{th}| = 0.5 - 0.1 = 0.4$ to 0.5 V. The lowest allowable output voltage is the value at which Q_1 leaves saturation, which is $-V_{dd} + |V_{th}| = -2.5 + 0.3 = -2.2$ V. Thus, the output voltage range is 0.4 V to 1.2 V.

Input Offset Voltage The device mismatches inevitably present in the input stage give rise to an input offset voltage. The components of this input offset voltage can be calculated using the methods developed in Section 7.4.1. Because device mismatches are random, the resulting offset voltage is referred to as **random offset**. This is to distinguish it from another type of input offset voltage that can be present even if all appropriate devices are perfectly matched. This predictable or **systematic offset** can be minimized by careful design. Although it occurs also in BJT op amps, and we have encountered it in Section 7.5.5, it is usually much more pronounced in CMOS op amps because their gain-per-stage is rather low.

To see how systematic offset can occur in the circuit of Fig. 7.40, i.e., the two inputs terminals be grounded. If the input stage is perfectly balanced, then the voltage appearing at the drain of Q_4 will be equal to that at the drain of Q_3 , which is $(-V_{gg} - V_{gs2})$. Now this is also the voltage that is fed to the gate of Q_6 . In other words, a voltage equal to V_{gs2} appears between gate and source of Q_6 . Thus the drain current of Q_6 , I_6 , will be related to the drain current of Q_4 , which is equal to $I/2$, by the relationship

$$I_6 = \frac{(W/L)_6}{(W/L)_4} (I/2) \quad (7.193)$$

In order for no offset voltage to appear at the output, this current must be exactly equal to the current supplied by I_5 . The latter current is related to the current I of the parallel source for Q_5 by

$$I_5 = \frac{(W/L)_5}{(W/L)_3} I \quad (7.194)$$

Now, the condition for making $I_6 = I_5$ can be found from Eqs. (7.193) and (7.194) as

$$\frac{(W/L)_6}{(W/L)_4} = \frac{2(W/L)_5}{(W/L)_3} \quad (7.195)$$

If this condition is not met, a systematic offset will result. From the specifications of the devices in Example 7.3, we can verify that condition (7.195) is not met, and, therefore, the op amp analyzed in that example should not exhibit a systematic input offset voltage.

EXERCISE

- 1.7 Consider the CMOS op amp shown in Fig. 7.40. Assume all n-channel devices are identical with $L = 1 \mu\text{m}$, $W_1 = W_2 = 10 \mu\text{m}$, $W_3 = W_4 = 20 \mu\text{m}$, $W_5 = W_6 = 10 \mu\text{m}$, $R_1 = R_2 = 100 \text{ k}\Omega$, $R_3 = R_4 = 10 \text{ M}\Omega$, $R_5 = 10 \text{ k}\Omega$, and $R_6 = 100 \text{ M}\Omega$. Find the overdrive voltage required to drive each of Q_1 , Q_2 , and Q_3 respectively.
2. Find $v_{in,high}$ for Q_1 , Q_2 , and Q_3 .
3. Find the output voltage range if $V_{dd} = 10$ V, $V_{gg} = 0$ V, and $V_{ss} = -10$ V.
4. Find the voltage gains A_1 , A_2 , and the output resistance R_o .
5. Find the input resistance R_i if $R_{in} = 200 \text{ G}\Omega$, $R_1 = 100 \text{ k}\Omega$, $R_2 = 10 \text{ M}\Omega$, $R_3 = 10 \text{ M}\Omega$, $R_4 = 10 \text{ M}\Omega$, $R_5 = 10 \text{ k}\Omega$, and $R_6 = 100 \text{ M}\Omega$.

Frequency Response To determine the frequency response of the two-stage CMOS op amp of Fig. 7.40, consider its simplified small-signal equivalent circuit shown in Fig. 7.41. Here G_{in} is the transconductance of the input stage ($G_{in} = g_{in} = g_{sd1}$), R_1 is the output resistance of the first stage ($R_1 = r_{ds1} \parallel r_{ds2}$), and C_{in} is the total capacitance at the interface between the first and second stages

$$C_{in} = C_{in1} + C_{in2} + C_{in3} + C_{in4} + C_{in5}$$

G_{out} is the transconductance of the second stage ($G_{out} = g_{out} = g_{sd2}$), R_2 is the output resistance of the second stage ($R_2 = r_{ds3} \parallel r_{ds4}$), and C_{out} is the total capacitance at the output node of the op amp

$$C_{out} = C_{out1} + C_{out2} + C_{out3} = C_{in}$$

where C_{in} is the load capacitance. Usually C_{in} is much larger than the transistor capacitances, with the result that C_{in} is much larger than C_{in} . Finally, note that in the equivalent circuit of Fig. 7.41, we should have included C_{in} in parallel with C_{in} . Usually, however, $C_{in} \gg C_{in}$, which is the reason we have neglected C_{in} .

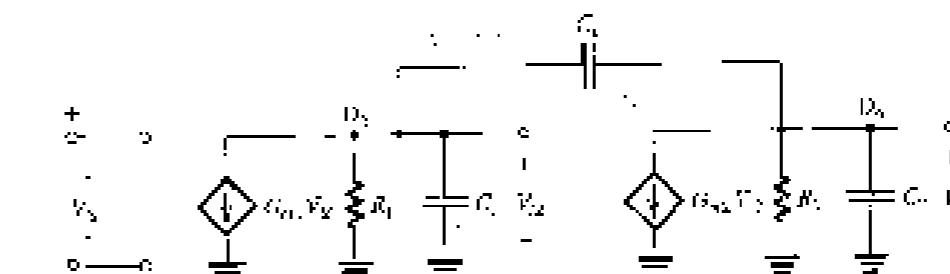


FIGURE 7.41 Equivalent circuit of the op amp in Fig. 7.40.

To determine V_{o2} , analysis of the circuit in Fig. 7.41 proceeds as follows. Writing a node equation at node V_2 yields

$$G_{o2}V_{o2} + \frac{V_o}{R_2} + sC_1V_2 + sC_2(V_2 - V_o) = 0 \quad (7.202)$$

Writing a node equation at node V_3 yields

$$G_{o3}V_{o3} + \frac{V_o}{R_3} + sC_3V_3 + sC_4(V_3 - V_o) = 0 \quad (7.203)$$

To eliminate V_{o2} and thus determine V_o in terms of V_{in} , we use Eq. (7.203) to express V_3 in terms of V_o and substitute the result into Eq. (7.202). After some straightforward manipulation we obtain the amplifier transfer function

$$\frac{V_o}{V_{in}} = \frac{\frac{V_o}{R_3} + sC_3V_3 + sC_4(V_3 - V_o)}{1 + r(C_1R_1 + C_2R_2 + C_3(G_{o3}R_3 + R_1 + R_2) + s^2(C_1C_2 + C_3(C_1 + C_2))R_3R_4)} \quad (7.204)$$

First we note that for $r = 0$ (i.e., dc), Eq. (7.204) gives $V_o/V_{in} = -(G_{o3}R_3)/(C_3R_3R_4)$, which is what we should have expected. Second, the transfer function in Eq. (7.204) indicates that the amplifier has a transmission zero at $s = s_0$, which is determined from

$$G_{o3} + s_0C_3 = 0$$

Thus,

$$s_0 = -\frac{G_{o3}}{C_3} \quad (7.205)$$

In other words, the zero is on the positive real axis with a frequency of

$$\omega_0 = \frac{G_{o3}}{C_3} \quad (7.206)$$

Also, the amplifier has two poles that are the roots of the denominator polynomial of Eq. (7.204). If the frequencies of the two poles are denoted ω_{p1} and ω_{p2} , then the denominator polynomial can be expressed as

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) + 1 + r\left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right) + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

Now if one of the poles, say that with frequency ω_{p1} , is dominant, then $\omega_{p1} \gg \omega_{p2}$ and $D(s)$ can be approximated by

$$D(s) \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \quad (7.207)$$

The frequency of the dominant pole, ω_{p1} , can now be determined by equating the coefficients of the s terms in the denominator in Eq. (7.204) and in Eq. (7.207).

$$\begin{aligned} \omega_{p1} &= \frac{1}{C_1R_1 + C_2R_2 + C_3(G_{o3}R_3 + R_1 + R_2 + R_4)} \\ &= \frac{1}{R_1[C_1 + C_2(1 + G_{o3}R_3)] + R_2(C_1 + C_3)} \end{aligned} \quad (7.208)$$

We recognize the first term in the denominator as arising at the interface between the first and second stages. Here, R_1 , the output resistance of the first stage, is interacting with the total capacitive load in the interface. The latter is the sum of C_1 and the Miller capacitance $C_2(1 + G_{o3}R_3)$, where resistive load connecting C_1 is the negative-feedback path of the second stage whose gain is $G_{o3}R_3$. Now, since R_1 and R_2 are usually of megaparsec value, we see that the first term in the denominator will be much larger than the second and we can approximate ω_{p1} as

$$\omega_{p1} \approx \frac{1}{R_1[C_1 + C_2(1 + G_{o3}R_3)]} \quad (7.209)$$

A further approximation is possible because C_1 is usually much smaller than the Miller capacitance and $G_{o3}R_3 \gg 1$, thus

$$\omega_{p1} \approx \frac{1}{R_1C_1G_{o3}R_3} \quad (7.209)$$

The frequency of the second, nondominant, pole can be found by equating the coefficients of the s^2 terms in the denominator of Eq. (7.204) and in Eq. (7.207) and substituting for ω_{p1} from Eq. (7.209). The result is

$$\omega_{p2} = \frac{G_{o3}C_3}{C_1C_2 + C_3(C_1 + C_2)} \quad (7.210)$$

Since $C_1 \ll C_2$ and $C_1 \ll C_3$, ω_{p2} can be approximated as

$$\omega_{p2} \approx \frac{G_{o3}}{C_3} \quad (7.210)$$

In order to provide the op amp with a uniform gain roll-off of -20 dB/decade down to 0 dB, the value of the compensation capacitor C_3 is selected so that the resulting value of ω_{p2} (Eq. 7.209) when multiplied by the dc gain ($G_{o3}R_3/G_{o2}R_2$) results in a unity-gain frequency ω_u lower than ω_0 and ω_{p1} . Specifically

$$\omega_u = (G_{o3}R_3G_{o2}R_2)\omega_{p2}$$

$$\omega_u = \frac{G_{o3}}{C_3} \quad (7.210)$$

which must be lower than $\omega_0 = \frac{G_{o3}}{C_3}$ and $\omega_{p1} = \frac{G_{o3}}{C_1}$. We will have more to say about this point in Section 9.

EXERCISE

- 7.19 Consider the response of the op amp shown in Fig. 7.40. Let $V_{in} = 0$, $V_{cc} = 10$ V, and $V_{ee} = 0$ V. Plot the value of C_3 that results in $\omega_u = 2$ rad/s and recall that ω_u is given by $\omega_u = 2\pi/\omega_{p2}$.

A Bias Circuit That Stabilizes g_m . We conclude this section by presenting a bias circuit for the two-stage CMOS op amp. The circuit presented has the interesting and useful property of providing a bias current whose value is independent of both the supply voltage and the

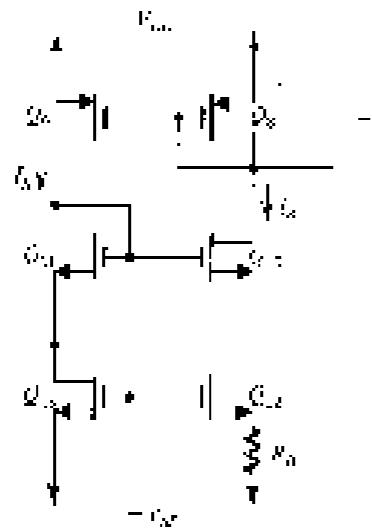


FIGURE 7.42 Bias circuit for the CMOS op-amp.

MOSFET threshold voltage. Furthermore, the transconductances of the transistors based on this circuit have values that are determined only by a single resistor and the device dimensions.

The bias circuit, as shown in Fig. 7.42, is composed of two deliberately mismatched transistors, Q_2 and Q_3 , with Q_2 usually about four times wider than Q_3 (Sotzing et al., 1990; Johns and Martin, 1987). A resistor R_B is connected in series with the source of Q_2 . Since, as will be shown, R_B determines both the bias current I_B and the transconductance g_{m2} , its value should be accurate and stable; in most applications, R_B will be an on-chip resistor. In order to minimize the channel-length modulation effect on Q_{10} , a source follower transistor Q_{11} and a matched diode-connected transistor Q_{12} provide a bias voltage for Q_{10} ; V_B is included. Finally, a p -channel current mirror formed by a pair of matched resistors, Q_4 and Q_5 , replicates the current I_B back to Q_{10} and Q_{11} , as well as providing a bias line for Q_1 and Q_2 of the CMOS op-amp circuit of Fig. 7.40.²

The circuit operates as follows. The current mirror (Q_4 , Q_5) causes Q_{10} to conduct a current equal to that in Q_{12} , that is, I_B . Thus,

$$I_B = \frac{1}{2} g_m C_{SD} \left(\frac{W}{L} \right) (V_{GS2} - V_T)^2 \quad (7.212)$$

and

$$I_B = \frac{1}{2} g_m C_{SD} \left(\frac{W}{L} \right) (V_{GS2,0} - V_T)^2 \quad (7.213)$$

From the circuit, we see that the gate-source voltages of Q_{12} and Q_1 are related by

$$V_{GS1} = V_{GS2} + I_B R_S$$

Subtracting V_T from both sides of the equation and using Eqs. (7.212) and (7.213) we replace $V_{GS1} = V_{GS2} + (V_{GS2,0} - V_T)$ resulting in

$$\frac{1}{2} g_m \frac{C_{SD}}{R_S} = \frac{1}{2} g_m \frac{C_{SD}}{\left(\frac{W}{L} \right)_2} + I_B R_S \quad (7.214)$$

²We denote the bias current of this circuit by I_B . If the value of I_B is set to bias the CMOS op-amp at $V_{GS} = 0$, then I_B becomes the reference current for I_{GS1} .

This equation can be rearranged to yield

$$I_B = \frac{2}{\alpha_s C_{SD} (W/L)_2 R_S} \left[\frac{g_m W L}{2} \left(\frac{W}{L} \right)_2 - 1 \right]^2 \quad (7.215)$$

from which we observe that I_B is determined by the dimensions of Q_2 and the value of R_S and by the ratio of the dimensions of Q_1 and Q_2 . Furthermore, Eq. (7.215) can be rearranged to the form

$$R_S = \frac{2}{\sqrt{2} \mu_n C_{SD} (W/L)_2 I_B} \left[\frac{g_m W L}{2} \left(\frac{W}{L} \right)_2 - 1 \right] \quad (7.216)$$

in which we recognize the factor $\sqrt{2} \mu_n C_{SD} (W/L)_2 I_B$ as g_{m2} . Thus,

$$R_S = \frac{2}{R_{SD}} \left[\frac{g_m W L}{2} \left(\frac{W}{L} \right)_2 - 1 \right] \quad (7.216)$$

This is a very interesting result since it determines R_S by the value of I_B and the ratios of the dimensions of Q_1 and Q_2 . Furthermore, since g_m of a MOSFET is proportional to $\sqrt{I_B (\lambda V_T)}$, each transistor creates by the circuit of Fig. 7.42, that is, each transistor whose bias current is derived from I_B will have a g_m value that is a multiple of g_{m2} . Specifically, the n -channel MOSFET will have

$$g_{mn} = R_{SD} \frac{I_B (\lambda V_T)}{\sqrt{I_B (\lambda V_T)}} \quad (7.217)$$

and the p -channel device will have

$$g_{mp} = 3 \times R_{SD} \frac{I_B (\lambda V_T)}{\sqrt{I_B (\lambda V_T)}} \quad (7.218)$$

Finally, it should be noted that the bias circuit of Fig. 7.42 employs positive feedback, and thus care should be exercised in its design to avoid unstable performance. Instability is avoided by making Q_2 wider than Q_3 , as has already been pointed out. Nevertheless, some form of instability may still occur; in fact, the circuit can operate in a stable state in which all currents are zero. To get it out of this state, current needs to be injected into one of its nodes, to "kick start" its operation. Feedback and stability will be studied in Chapter 8.

EXERCISES

- 7.7.1 Consider the bias circuit of Fig. 7.42, with $R_S = 100 \Omega$, $R_D = 100 \Omega$, $R_B = 100 \Omega$, $C_{SD} = 100 \text{ pF}$, $\mu_n C_{SD} = 100 \text{ nA}$, $\mu_p C_{SD} = 10 \text{ nA}$, $V_B = 1.5 \text{ V}$, $V_{GS1} = 0$, $V_{GS2} = 0$, $V_{GS1,0} = 0.5 \text{ V}$, $V_{GS2,0} = 0.2 \text{ V}$, $V_T = 0.2 \text{ V}$, $\lambda = 0.01$, $I_B = 10 \text{ nA}$, $I_{GS1} = 10 \text{ nA}$, $I_{GS2} = 100 \text{ nA}$, $I_{DS1} = 0$, $I_{DS2} = 0$, $I_{D1} = 0$, $I_{D2} = 0$, $I_{D3} = 0$, $I_{D4} = 0$, $I_{D5} = 0$, $I_{D6} = 0$, $I_{D7} = 0$, $I_{D8} = 0$, $I_{D9} = 0$, $I_{D10} = 0$, $I_{D11} = 0$, $I_{D12} = 0$, $I_{D13} = 0$, $I_{D14} = 0$, $I_{D15} = 0$, $I_{D16} = 0$, $I_{D17} = 0$, $I_{D18} = 0$, $I_{D19} = 0$, $I_{D20} = 0$, $I_{D21} = 0$, $I_{D22} = 0$, $I_{D23} = 0$, $I_{D24} = 0$, $I_{D25} = 0$, $I_{D26} = 0$, $I_{D27} = 0$, $I_{D28} = 0$, $I_{D29} = 0$, $I_{D30} = 0$, $I_{D31} = 0$, $I_{D32} = 0$, $I_{D33} = 0$, $I_{D34} = 0$, $I_{D35} = 0$, $I_{D36} = 0$, $I_{D37} = 0$, $I_{D38} = 0$, $I_{D39} = 0$, $I_{D40} = 0$, $I_{D41} = 0$, $I_{D42} = 0$, $I_{D43} = 0$, $I_{D44} = 0$, $I_{D45} = 0$, $I_{D46} = 0$, $I_{D47} = 0$, $I_{D48} = 0$, $I_{D49} = 0$, $I_{D50} = 0$, $I_{D51} = 0$, $I_{D52} = 0$, $I_{D53} = 0$, $I_{D54} = 0$, $I_{D55} = 0$, $I_{D56} = 0$, $I_{D57} = 0$, $I_{D58} = 0$, $I_{D59} = 0$, $I_{D60} = 0$, $I_{D61} = 0$, $I_{D62} = 0$, $I_{D63} = 0$, $I_{D64} = 0$, $I_{D65} = 0$, $I_{D66} = 0$, $I_{D67} = 0$, $I_{D68} = 0$, $I_{D69} = 0$, $I_{D70} = 0$, $I_{D71} = 0$, $I_{D72} = 0$, $I_{D73} = 0$, $I_{D74} = 0$, $I_{D75} = 0$, $I_{D76} = 0$, $I_{D77} = 0$, $I_{D78} = 0$, $I_{D79} = 0$, $I_{D80} = 0$, $I_{D81} = 0$, $I_{D82} = 0$, $I_{D83} = 0$, $I_{D84} = 0$, $I_{D85} = 0$, $I_{D86} = 0$, $I_{D87} = 0$, $I_{D88} = 0$, $I_{D89} = 0$, $I_{D90} = 0$, $I_{D91} = 0$, $I_{D92} = 0$, $I_{D93} = 0$, $I_{D94} = 0$, $I_{D95} = 0$, $I_{D96} = 0$, $I_{D97} = 0$, $I_{D98} = 0$, $I_{D99} = 0$, $I_{D100} = 0$, $I_{D101} = 0$, $I_{D102} = 0$, $I_{D103} = 0$, $I_{D104} = 0$, $I_{D105} = 0$, $I_{D106} = 0$, $I_{D107} = 0$, $I_{D108} = 0$, $I_{D109} = 0$, $I_{D110} = 0$, $I_{D111} = 0$, $I_{D112} = 0$, $I_{D113} = 0$, $I_{D114} = 0$, $I_{D115} = 0$, $I_{D116} = 0$, $I_{D117} = 0$, $I_{D118} = 0$, $I_{D119} = 0$, $I_{D120} = 0$, $I_{D121} = 0$, $I_{D122} = 0$, $I_{D123} = 0$, $I_{D124} = 0$, $I_{D125} = 0$, $I_{D126} = 0$, $I_{D127} = 0$, $I_{D128} = 0$, $I_{D129} = 0$, $I_{D130} = 0$, $I_{D131} = 0$, $I_{D132} = 0$, $I_{D133} = 0$, $I_{D134} = 0$, $I_{D135} = 0$, $I_{D136} = 0$, $I_{D137} = 0$, $I_{D138} = 0$, $I_{D139} = 0$, $I_{D140} = 0$, $I_{D141} = 0$, $I_{D142} = 0$, $I_{D143} = 0$, $I_{D144} = 0$, $I_{D145} = 0$, $I_{D146} = 0$, $I_{D147} = 0$, $I_{D148} = 0$, $I_{D149} = 0$, $I_{D150} = 0$, $I_{D151} = 0$, $I_{D152} = 0$, $I_{D153} = 0$, $I_{D154} = 0$, $I_{D155} = 0$, $I_{D156} = 0$, $I_{D157} = 0$, $I_{D158} = 0$, $I_{D159} = 0$, $I_{D160} = 0$, $I_{D161} = 0$, $I_{D162} = 0$, $I_{D163} = 0$, $I_{D164} = 0$, $I_{D165} = 0$, $I_{D166} = 0$, $I_{D167} = 0$, $I_{D168} = 0$, $I_{D169} = 0$, $I_{D170} = 0$, $I_{D171} = 0$, $I_{D172} = 0$, $I_{D173} = 0$, $I_{D174} = 0$, $I_{D175} = 0$, $I_{D176} = 0$, $I_{D177} = 0$, $I_{D178} = 0$, $I_{D179} = 0$, $I_{D180} = 0$, $I_{D181} = 0$, $I_{D182} = 0$, $I_{D183} = 0$, $I_{D184} = 0$, $I_{D185} = 0$, $I_{D186} = 0$, $I_{D187} = 0$, $I_{D188} = 0$, $I_{D189} = 0$, $I_{D190} = 0$, $I_{D191} = 0$, $I_{D192} = 0$, $I_{D193} = 0$, $I_{D194} = 0$, $I_{D195} = 0$, $I_{D196} = 0$, $I_{D197} = 0$, $I_{D198} = 0$, $I_{D199} = 0$, $I_{D200} = 0$, $I_{D201} = 0$, $I_{D202} = 0$, $I_{D203} = 0$, $I_{D204} = 0$, $I_{D205} = 0$, $I_{D206} = 0$, $I_{D207} = 0$, $I_{D208} = 0$, $I_{D209} = 0$, $I_{D210} = 0$, $I_{D211} = 0$, $I_{D212} = 0$, $I_{D213} = 0$, $I_{D214} = 0$, $I_{D215} = 0$, $I_{D216} = 0$, $I_{D217} = 0$, $I_{D218} = 0$, $I_{D219} = 0$, $I_{D220} = 0$, $I_{D221} = 0$, $I_{D222} = 0$, $I_{D223} = 0$, $I_{D224} = 0$, $I_{D225} = 0$, $I_{D226} = 0$, $I_{D227} = 0$, $I_{D228} = 0$, $I_{D229} = 0$, $I_{D230} = 0$, $I_{D231} = 0$, $I_{D232} = 0$, $I_{D233} = 0$, $I_{D234} = 0$, $I_{D235} = 0$, $I_{D236} = 0$, $I_{D237} = 0$, $I_{D238} = 0$, $I_{D239} = 0$, $I_{D240} = 0$, $I_{D241} = 0$, $I_{D242} = 0$, $I_{D243} = 0$, $I_{D244} = 0$, $I_{D245} = 0$, $I_{D246} = 0$, $I_{D247} = 0$, $I_{D248} = 0$, $I_{D249} = 0$, $I_{D250} = 0$, $I_{D251} = 0$, $I_{D252} = 0$, $I_{D253} = 0$, $I_{D254} = 0$, $I_{D255} = 0$, $I_{D256} = 0$, $I_{D257} = 0$, $I_{D258} = 0$, $I_{D259} = 0$, $I_{D260} = 0$, $I_{D261} = 0$, $I_{D262} = 0$, $I_{D263} = 0$, $I_{D264} = 0$, $I_{D265} = 0$, $I_{D266} = 0$, $I_{D267} = 0$, $I_{D268} = 0$, $I_{D269} = 0$, $I_{D270} = 0$, $I_{D271} = 0$, $I_{D272} = 0$, $I_{D273} = 0$, $I_{D274} = 0$, $I_{D275} = 0$, $I_{D276} = 0$, $I_{D277} = 0$, $I_{D278} = 0$, $I_{D279} = 0$, $I_{D280} = 0$, $I_{D281} = 0$, $I_{D282} = 0$, $I_{D283} = 0$, $I_{D284} = 0$, $I_{D285} = 0$, $I_{D286} = 0$, $I_{D287} = 0$, $I_{D288} = 0$, $I_{D289} = 0$, $I_{D290} = 0$, $I_{D291} = 0$, $I_{D292} = 0$, $I_{D293} = 0$, $I_{D294} = 0$, $I_{D295} = 0$, $I_{D296} = 0$, $I_{D297} = 0$, $I_{D298} = 0$, $I_{D299} = 0$, $I_{D300} = 0$, $I_{D301} = 0$, $I_{D302} = 0$, $I_{D303} = 0$, $I_{D304} = 0$, $I_{D305} = 0$, $I_{D306} = 0$, $I_{D307} = 0$, $I_{D308} = 0$, $I_{D309} = 0$, $I_{D310} = 0$, $I_{D311} = 0$, $I_{D312} = 0$, $I_{D313} = 0$, $I_{D314} = 0$, $I_{D315} = 0$, $I_{D316} = 0$, $I_{D317} = 0$, $I_{D318} = 0$, $I_{D319} = 0$, $I_{D320} = 0$, $I_{D321} = 0$, $I_{D322} = 0$, $I_{D323} = 0$, $I_{D324} = 0$, $I_{D325} = 0$, $I_{D326} = 0</$

7.7.2 A Bipolar Ob Amo

Our second example of multistage amplifiers is the four-stage bipolar op amp shown in Fig. 7.4A. The circuit consists of four stages. The input stage is differential-in, differential-out and consists of transistors Q_1 and Q_2 , which are biased by current source Q_3 . The second stage is also a differential-input amplifier, but its output is taken single-endedly at the collector of Q_5 . This stage is formed by Q_4 and Q_5 , which are biased by the current source Q_6 . Note that the conversion from differential to single-ended is performed by the second stage resulting in a loss of gain by a factor of 2. A more elaborate method for accomplishing this conversion was studied in Section 7.5; it involves using a current mirror as active load.

In addition to providing some voltage gain, the taild stage, consisting of the pnp transistor Q_1 , provides the essential function of shifting the dc level of the signal. Thus while the signal at the collector of Q_1 is not allowed to swing below the voltage at the base of Q_2 , i.e. 10 V, the signal at the collector of Q_1 can swing negatively (and positively, of course). From our study of op-amps in Chapter 2 we know that the output terminal of the op-amp should be capable of both positive and negative voltage swings. Therefore every op-amp circuit includes a level-shifting arrangement. Although the use of the complementary pair transistors

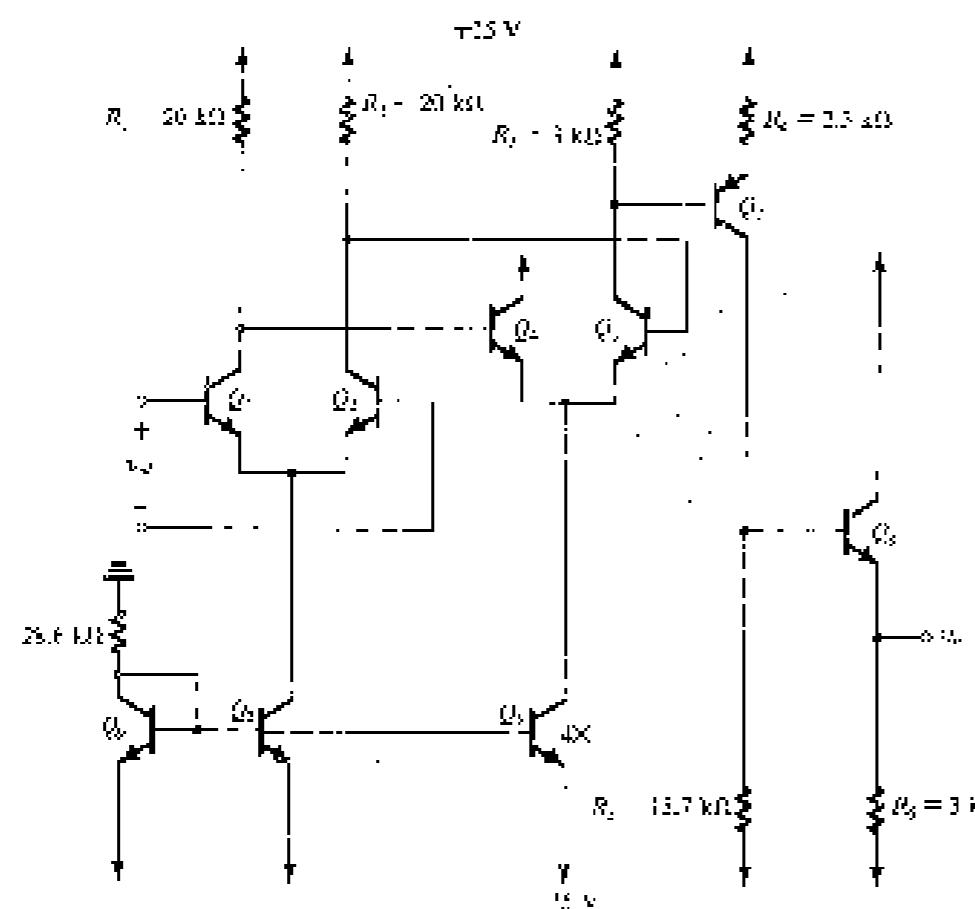


FIGURE 7.43 A three-stage bipolar op amp.

provide a simple solution to the level-shifting problem, other form of level shifter exist (see 3) which will be discussed in Chapter 9. Furthermore, note that level-shifting is more pushed in the CMOS op-amp we have been studying by using complementary devices for the bias stages. That is, a current for the first stage is also obtained for the second stage.

The output stage of the op amp consists of a current follower Q_1 . As we know from our study of op amps in Chapter 2, the output operates ideally around zero volts. This and other features of the BJT op amp will be illustrated in Example 7-4.

In this example, we analyze the de nites of the loop gain amplitude of Fig. 7.15. Toward this end, Fig. 7.14 shows the circuit, where two input terminals connected to ground

- (a) Perform an approximate dc analysis assuming $\beta \gg 1$, $V_{BE} = 0.7\text{ V}$, and neglecting the Early effect. Calculate the dc currents and voltages everywhere in the circuit. Note that C_{BE} is $\sim 10\text{ pF}$; the area of each of Ω_1 and Ω_2

 - Calculate the quiescent power dissipation in the circuit.
 - If transistors Ω_1 and Ω_2 have $\beta = 100$, calculate the input bias current of the op-amp.
 - What is the input common-mode range of the op-amp?

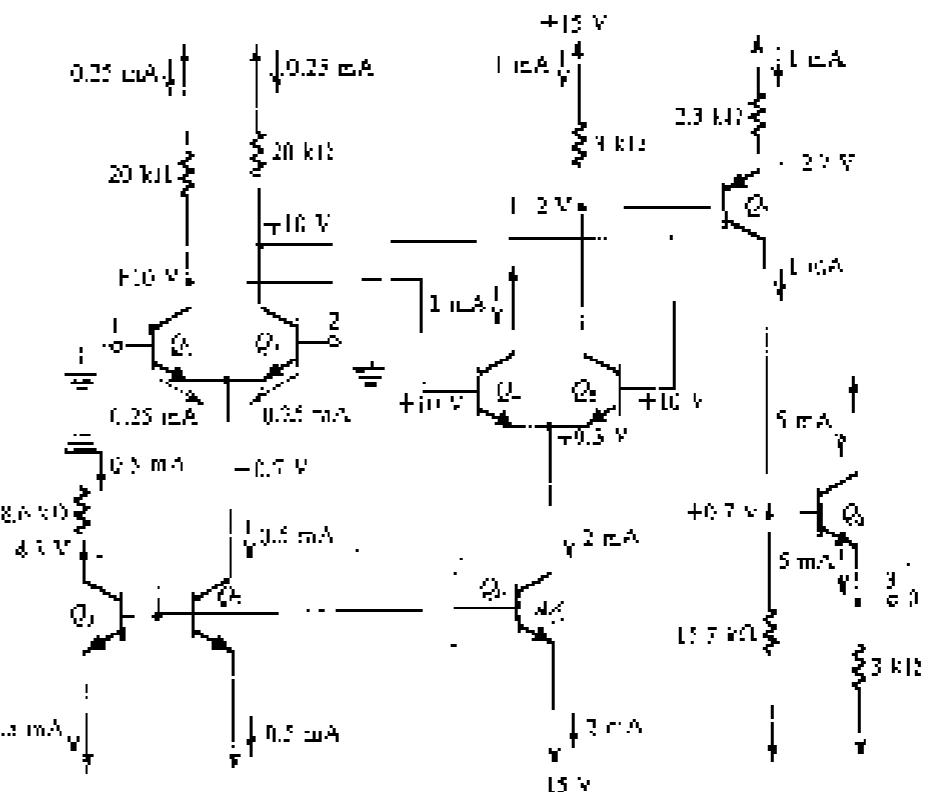


FIGURE 7.44 Circuit for Example 7.

Solution

(a) The values of all dc currents and voltages are indicated on the circuit diagram. These values were calculated by ignoring the base current of every transistor—that is, by assuming β to be very high. The analysis starts by determining the current through the current-controlled transistor Q_1 , which is 0.25 mA . Then we see that since Q_1 conducts 1.25 mA and has a $\beta = 100$, $I_{C1} = 2 \text{ mA}$. Thus, current-controlled resistor R_1 (across the differential pair (Q_1, Q_2)) will be 0.25 mA . Thus each of Q_1 and Q_2 will be biased at 0.25 mA . The collector of Q_1 and Q_2 will be at $-10 - 0.25 \times 20^{\circ} = -10 \text{ V}$.

Proceeding to the second differential stage formed by Q_3 and Q_4 , we find the voltage at the emitters to be $|-10 - 0.2| = 9.8 \text{ V}$. This differential pair is biased by the current-source transistor Q_5 , which supplies a current of 2 mA ; thus Q_3 and Q_4 will each be biased at 1 mA . We can now calculate the voltage at the collector of Q_3 as $[(15 - 1) \times 2] + 12 = 14 \text{ V}$. This will cause the voltage at the emitter of the pnp transistor Q_6 to be -12 V ; and the emitter current of Q_6 will be $(15 - (-12)) / 2 = 1.0 \text{ A}$.

The collector current of Q_6 , 1 A , causes the voltage at the collector to be $(15 - 1 \times 15 \%) = 14.2 \text{ V}$. The emitter of Q_6 will be 0.2 V below the base; thus output terminal 3 will be at 0 V . Finally, the emitter current of Q_3 can be calculated to be $[0 - (15)/3] = 5 \text{ mA}$.

(b) To calculate the power dissipated in the circuit in the quiescent state (i.e., with zero input signal), we simply evaluate the dc current that the circuit draws from each of the two power supplies. From the -15 V supply the dc current is $I^+ = 0.25 + 0.25 + 1 + 1 + 1 + 2 = 8.2 \text{ mA}$. Thus the power supplied by the positive power supply is $P^+ = 15 \times 8.2 = 123 \text{ mW}$. The -12 V supply provides a current I^- given by $I^- = 0.2 + 1.0 + 2 + 1 + 3 = 6.5 \text{ mA}$. Thus the power provided by the negative supply is $P^- = 15 \times 6.5 = 132 \text{ mW}$. Adding P^+ and P^- provides the total power dissipated in the circuit, $P_{\text{tot}} = P^+ + P^- = 255.5 \text{ mW}$.

(c) The input bias current of the op-amp is the average of the dc currents that flow in the two input terminals (i.e., in the bases of Q_1 and Q_2). These two currents are equal (because we have assumed matched devices); thus the bias current is given by

$$I_B = \frac{I_B}{\beta + 1} = 0.5 \text{ }\mu\text{A}$$

(d) The upper limit on the input common-mode voltage is determined by the voltage at which Q_1 and Q_2 leave the active mode and enter saturation. This will happen if the input voltage exceeds the collector voltage, which is -10 V , by about 0.4 V . Thus the upper limit of the common-mode range is $+10.4 \text{ V}$.

The lower limit of the input common-mode voltage is determined by the voltage at which Q_1 leaves the active mode and thus ceases to act as a constant-current source. This will happen if the collector voltage of Q_1 goes below the voltage at its base, which is -14.2 V , by more than 0.4 V . It follows that the input common-mode voltage should not go lower than $-14.2 + 0.4 = -14 \text{ V}$. Thus the common-mode range is -14 V to $+10.4 \text{ V}$.

Example 7.4

Use the dc bias quantities evaluated in Example 7.1 to analyze the circuit in Fig. 7.41 to determine the input resistance, the voltage gain, and the output resistance.

Solution

The input differential resistance R_{in} is given by

$$R_{in} = r_{in} + r_{ce}$$

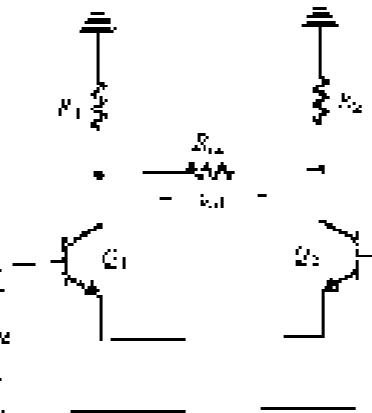


FIGURE 7.45 Equivalent circuit for calculating the gain of the first stage of the circuit in Fig. 7.41.

Since Q_1 and Q_2 are each operating at an emitter current of 0.25 mA , it follows that

$$r_{ce} = r_{in} = \frac{25}{0.25} = 100 \Omega$$

Assume $\beta = 100$; then

$$r_{ce} = r_{in} = 0.1 \times 100 = 10 \text{ k}\Omega$$

Thus

$$R_{in} = 20 \text{ k}\Omega$$

To calculate the gain of the first stage we first find the input resistance of the second stage, R_{in2} ,

$$R_{in2} = r_{in2} + r_{ce}$$

Q_4 and Q_5 are each operating at an emitter current of 1 mA ; thus

$$r_{ce} = r_{in2} = 25 \Omega$$

$$r_{in2} = r_{ce} = 0.1 \times 25 = 2.525 \text{ k}\Omega$$

Thus $R_{in2} = 2.525 \text{ k}\Omega$. This resistance appears between the collectors of Q_1 and Q_2 , as shown in Fig. 7.45. Thus the g_{in} of the first stage will be

$$\begin{aligned} g_{in} &= \frac{r_{in}}{r_{in} + r_{in2}} = \frac{100}{100 + 2.525} = 97.5 \text{ mV/V} \\ &= \frac{(R_{in} + R_{in2})}{r_{in} + r_{in2}} \\ &= \frac{(5.05 \text{ k}\Omega + 40 \text{ k}\Omega)}{2.525 \text{ k}\Omega} = 22.4 \text{ mV/V} \end{aligned}$$

Figure 7.46 shows an equivalent circuit for calculating the gain of the second stage. As indicated, the input voltage to the second stage is the output voltage of the first stage, v_{o1} . Also shown is the resistance R_{in3} , which is the input resistance of the third stage formed by Q_6 . The value of R_{in3} can be found by multiplying the total resistance in the emitter of Q_5 by $(\beta + 1)$:

$$R_{in3} = (\beta + 1)(R_{in} + r_{ce})$$

Since Q_5 is operating at an emitter current of 1 mA ,

$$r_{ce} = \frac{25}{1} = 25 \Omega$$

$$R_{in3} = 0.1 \times 2.525 = 254.8 \text{ k}\Omega$$

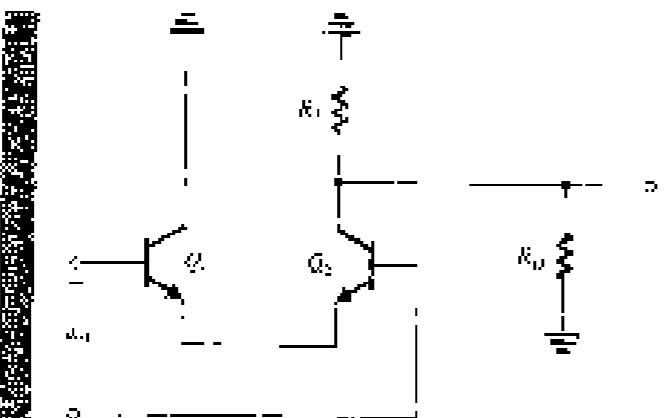


FIGURE 7.46 Equivalent circuit for calculating the gain of the second stage of the amplifier in Fig. 7.43.

We can now find the gain A_2 of the second stage as the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit:

$$\begin{aligned} A_2 &\equiv \frac{v_{o2}}{v_{i2}} = \frac{(R_C2 \parallel R_{L2})}{r_{ce2} + r_{e2}} \\ &= \frac{(5\text{k}\Omega \parallel 234.8\text{k}\Omega)}{50\Omega} = -59.2\text{V/V} \end{aligned}$$

To obtain the gain of the third stage we refer to the equivalent circuit shown in Fig. 7.47, where r_{ce3} is the output resistance of the output stage terminated by Q_3 . Using the transmission-reflection rule, we calculate the value of r_{ce3} as

$$r_{ce3} = (\beta + 1)(r_{ex3} + R_{L3})$$

where

$$r_{ex3} \approx \frac{25}{3} = 5\Omega$$

$$R_{L3} = 101(5 + 50\Omega) = 303.5\text{k}\Omega$$

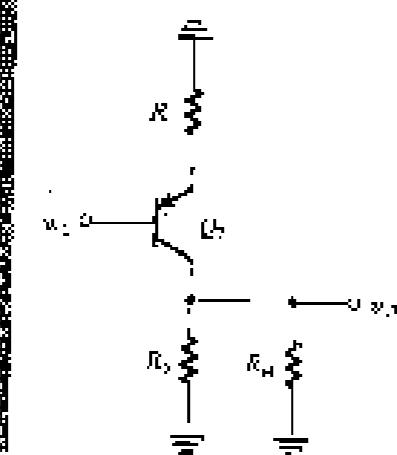


FIGURE 7.47 Equivalent circuit for evaluating the gain of the third stage in the amplifier circuit of Fig. 7.43.

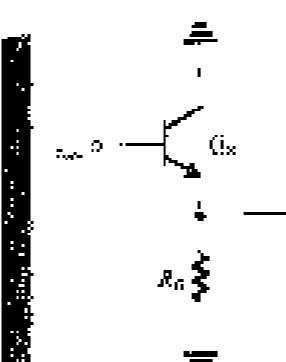


FIGURE 7.48 Equivalent circuit of the output stage of the amplifier circuit of Fig. 7.43.

The gain of the third stage is given by

$$\begin{aligned} A_3 &\equiv \frac{v_o}{v_{o3}} = \frac{(R_C3 \parallel R_{L3})}{r_{ce3} + R_{L3}} \\ &= \frac{(15.7\text{k}\Omega \parallel 303.5\text{k}\Omega)}{2.325\text{k}\Omega} = -642\text{V/V} \end{aligned}$$

Finally, to obtain the gain A_4 of the output stage we refer to the equivalent circuit in Fig. 7.48 and write

$$\begin{aligned} A_4 &\equiv \frac{v_o}{v_{o3}} = \frac{R_L}{R_C3 + r_{ce3}} \\ &= \frac{3000}{3000 + 5} = 0.798 = 1 \end{aligned}$$

The overall voltage gain of the amplifier can then be obtained as follows:

$$\frac{v_o}{v_{i2}} \equiv A_1 A_2 A_3 A_4 = 65.3\text{V/V}$$

or 73.6 dB.

To obtain the output resistance R_o we "ground" the output terminal in Fig. 7.49 and look back into the circuit. By inspection we find

$$R_o = R_C3 \parallel r_{ce3} + R_{L3}/(\beta + 1)$$

which gives

$$R_o = 152\Omega$$

EXERCISE

7.72 Use the equivalent circuit of the output stage of the amplifier in Fig. 7.43 to determine the output resistance of the output stage of the amplifier in Fig. 7.43.

ANS. 49.3 kΩ

7.73 The output resistance of the output stage of the amplifier in Fig. 7.43 is 49.3 kΩ. If the output voltage is 10 mV, what is the output current?

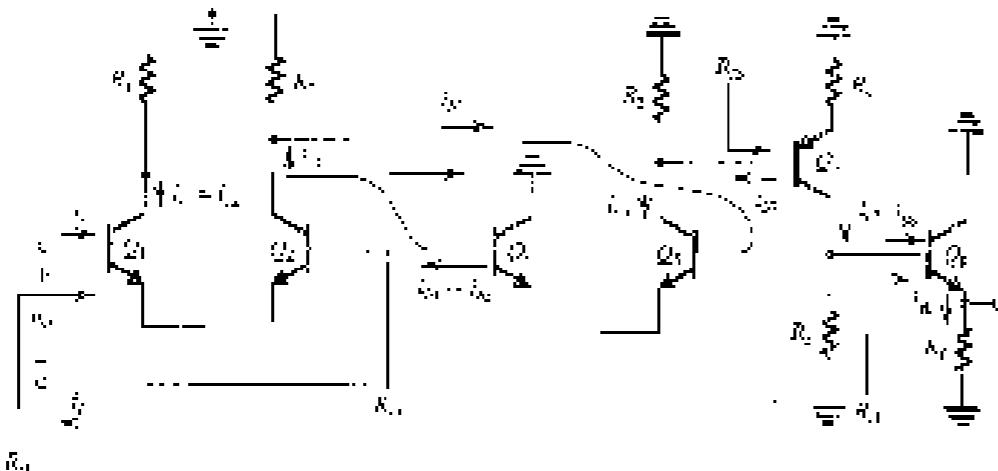


FIGURE 7-49 The result of the recordings made at 1 s of the 200- μ prepulse in the electrical analysis. The currents of depolarizing currents throughout the prepulse and the repolarizing currents of the following spikes.

Analysis Using Current Gains. There is an alternative method for the analysis of bipolarmatching amplifiers that can be somewhat easier to perform in some cases. The method makes use of current gains or more appropriately current transmission factors. In effect, it traces the transmission of the signal current throughout the amplifier cascade, evaluating at the outset the transistor factors in play. We shall illustrate the method by using it to analyze the equivalent circuit of the preceding example.

Figure 7-49 shows the amplifiers circuit prepared for small-signal analysis. We have indicated both the current directions of the signal currents through all the circuit branches. Also indicated are the input resistances of all four stages of the amplifier. These should be evaluated before proceeding with the following analysis.

The purpose of the analysis is to determine the overall voltage gain (v_o/v_s). Toward that end, we express v_o in terms of the signal current in the emitters of Q_1 , Q_2 , and Q_3 in terms of the input voltage v_s as follows:

$$z_i = \delta_{ij} z_j$$

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Thus, the voltage gain can be expressed in terms of a current gain (I_{out}/I_{in}) as

$$\frac{v_i}{v_j} = \frac{R_i}{R_j} \frac{I_j}{I_i}$$

Next, we expand the current gain β_{dc}/β in terms of d.c. signal currents throughout the circuit as follows:

$$\frac{f_{1,2}}{f_1} = \frac{1}{2} \times \frac{f_{2,2}}{f_2} \times \frac{1}{2} \times \frac{f_{2,2}}{f_2} \times \frac{1}{2} \times \frac{f_{2,2}}{f_2} \times \frac{1}{2}$$

Each of the current matrix factor on the right-hand side is either the current gain of a transistor or the ratio of a current divider. Thus, reference to Fig. 7.49 enables us to find these factors by inspection.

$$\lim_{n \rightarrow \infty} \beta_n = \beta_0$$

$$\frac{I_{\text{in}}}{I_{\text{out}}} = \frac{R_s}{R_o + R_s}$$

$$\frac{I_{\text{in}}}{I_{\text{out}}} = \beta_2$$

These ratios can be easily evaluated and their values used to determine the voltage gain.

With a little practice, it is possible to carry out steady-state analysis very quickly, forgoing explicitly labeling the signal currents on the circuit diagram. One simply "walks through" the circuit, from input to output, or vice versa, determining the current through each factor one at a time, in a chainlike fashion.

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Frequency Response The bipolar op-amp circuit of Fig. 7.43 is neither complete. Nevertheless, it is possible to obtain an approximate estimate of its high-frequency response. Figure 7.50(c) shows an approximate equivalent circuit for this purpose. Note that we have utilized the equivalent differential test-circuit concept, with Q_1 representing the first stage and Q_2 representing the second stage. We observe, of course, that the second stage is non-symmetrical, and strictly speaking the equivalent $1:1$ circuit does not apply. Nevertheless, we use it as an approximation since it retains a quick pencil-and-paper estimate of the dominant high-frequency pole of the amplifier. More precise results can, of course be obtained using computer simulation with SPICE (Sec. 12.6).

Examination of the equivalent circuit in Fig. 2.50(a) reveals that if the resistance of the source of signal V_2 is small, the high-frequency limitation will not occur at the input by earlier at the interface between the first and the second stages. This is because the total capacitance at node A will be high as a result of the Miller multiplication of C_{23} . Also, the third stage, formed by transistors Q_3 , should exhibit good high-frequency response, since Q_3 has a large emitter-degeneration resistance, R_3 . The same is also true for the emitted follower stage, Q_4 .

To determine the frequency of the dominant pole that is formed at the interface between G_1 and G_2 , we show in Fig. 7.50(c) the pertinent equivalent circuit. The total resistance

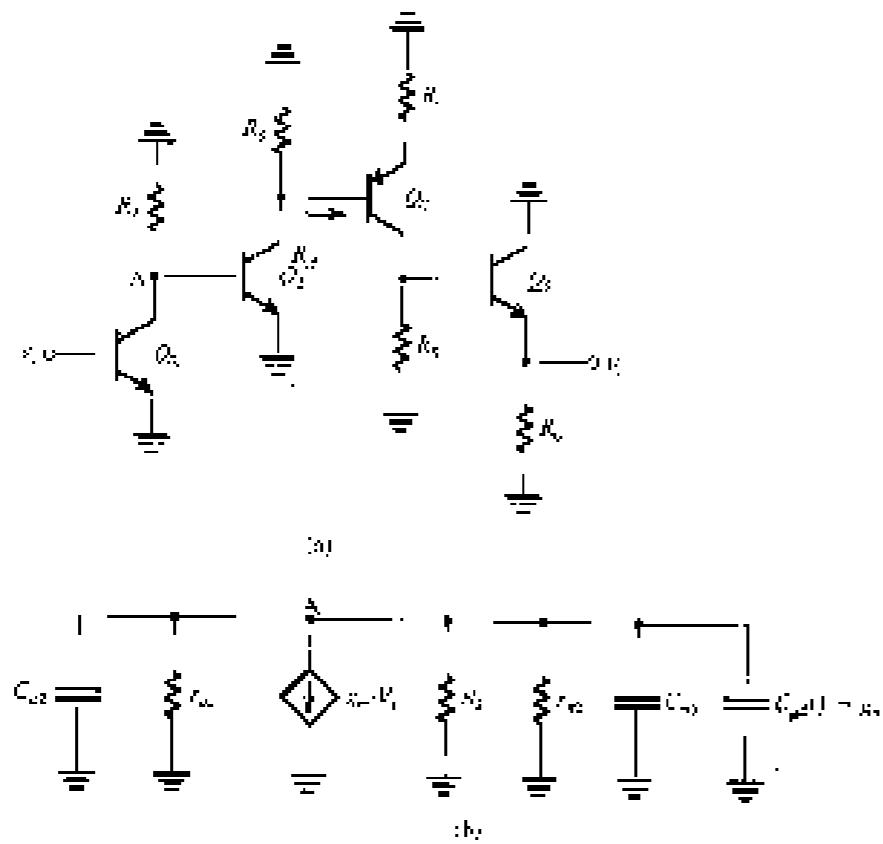


FIGURE 7.50 (a) Application equivalent circuit for determining the high frequency response of the op-amp circuit; (b) the equivalent circuit of the interface between the output of Q3 and the input of Q2.

Between nodes A and ground can now be found as

$$R_{IN} = R_1 \parallel r_{ds1} \parallel r_{ds2}$$

and the total capacitance is

$$C_{IN} = C_{12} + C_{23}(1 + \beta_{Q3}R_{12})$$

where

$$R_{12} = R_1 \parallel r_{ds1} \parallel R_2$$

The frequency of the pole can be calculated from R_{12} and C_{IN} :

$$f_p = \frac{1}{2\pi R_{12} C_{IN}}$$

EXERCISE

7.35 Calculate the frequency of the pole in Figure 7.50(a) for the case where $V_{CC} = 15$ V, $V_{EE} = -15$ V, $V_{REF} = 0$ V, $V_{BL} = -0.5$ V, $V_{BL2} = 0$ V, $V_{BL3} = 0$ V, $V_{BL4} = 0$ V, $V_{BL5} = 0$ V, $V_{BL6} = 0$ V, $V_{BL7} = 0$ V, $V_{BL8} = 0$ V, $V_{BL9} = 0$ V, $V_{BL10} = 0$ V, $V_{BL11} = 0$ V, $V_{BL12} = 0$ V, $V_{BL13} = 0$ V, $V_{BL14} = 0$ V, $V_{BL15} = 0$ V, $V_{BL16} = 0$ V, $V_{BL17} = 0$ V, $V_{BL18} = 0$ V, $V_{BL19} = 0$ V, $V_{BL20} = 0$ V, $V_{BL21} = 0$ V, $V_{BL22} = 0$ V, $V_{BL23} = 0$ V, $V_{BL24} = 0$ V, $V_{BL25} = 0$ V, $V_{BL26} = 0$ V, $V_{BL27} = 0$ V, $V_{BL28} = 0$ V, $V_{BL29} = 0$ V, $V_{BL30} = 0$ V, $V_{BL31} = 0$ V, $V_{BL32} = 0$ V, $V_{BL33} = 0$ V, $V_{BL34} = 0$ V, $V_{BL35} = 0$ V, $V_{BL36} = 0$ V, $V_{BL37} = 0$ V, $V_{BL38} = 0$ V, $V_{BL39} = 0$ V, $V_{BL40} = 0$ V, $V_{BL41} = 0$ V, $V_{BL42} = 0$ V, $V_{BL43} = 0$ V, $V_{BL44} = 0$ V, $V_{BL45} = 0$ V, $V_{BL46} = 0$ V, $V_{BL47} = 0$ V, $V_{BL48} = 0$ V, $V_{BL49} = 0$ V, $V_{BL50} = 0$ V, $V_{BL51} = 0$ V, $V_{BL52} = 0$ V, $V_{BL53} = 0$ V, $V_{BL54} = 0$ V, $V_{BL55} = 0$ V, $V_{BL56} = 0$ V, $V_{BL57} = 0$ V, $V_{BL58} = 0$ V, $V_{BL59} = 0$ V, $V_{BL60} = 0$ V, $V_{BL61} = 0$ V, $V_{BL62} = 0$ V, $V_{BL63} = 0$ V, $V_{BL64} = 0$ V, $V_{BL65} = 0$ V, $V_{BL66} = 0$ V, $V_{BL67} = 0$ V, $V_{BL68} = 0$ V, $V_{BL69} = 0$ V, $V_{BL70} = 0$ V, $V_{BL71} = 0$ V, $V_{BL72} = 0$ V, $V_{BL73} = 0$ V, $V_{BL74} = 0$ V, $V_{BL75} = 0$ V, $V_{BL76} = 0$ V, $V_{BL77} = 0$ V, $V_{BL78} = 0$ V, $V_{BL79} = 0$ V, $V_{BL80} = 0$ V, $V_{BL81} = 0$ V, $V_{BL82} = 0$ V, $V_{BL83} = 0$ V, $V_{BL84} = 0$ V, $V_{BL85} = 0$ V, $V_{BL86} = 0$ V, $V_{BL87} = 0$ V, $V_{BL88} = 0$ V, $V_{BL89} = 0$ V, $V_{BL90} = 0$ V, $V_{BL91} = 0$ V, $V_{BL92} = 0$ V, $V_{BL93} = 0$ V, $V_{BL94} = 0$ V, $V_{BL95} = 0$ V, $V_{BL96} = 0$ V, $V_{BL97} = 0$ V, $V_{BL98} = 0$ V, $V_{BL99} = 0$ V, $V_{BL100} = 0$ V, $V_{BL101} = 0$ V, $V_{BL102} = 0$ V, $V_{BL103} = 0$ V, $V_{BL104} = 0$ V, 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TABLE 7.2 SPICE Model Parameters of the Transistors Used in Discrete BJT

Q2N3904 Discrete BJT					
IS=1.14	XTF=0	DS=1.1	VA=14.8	RB=4.4k	NA=1.250
ICF=400mA	A ₁₁ =1.0	ISB=3.75	VCB=0	ISD=0	RC=1
CO ₁ =3.75pF	MOC ₁ =0.85	V _{CB} =7.5	RD=2	CO ₂ =4.85pF	VO _B =2.0V
TX=281.0u	11=30.2	11B=4	VT _B =4	XTF=2	Re=10

Q2N3906 Discrete BJT					
IS=1.41f	XTF=0	DS=1.1	VA=7.87	RB=4.0k	NA=1.5
ICF=800mA	A ₁₁ =1.0	ISB=3.75	VCB=0	ISD=0	RC=1.5
CO ₁ =5.75pF	MOC ₁ =0.75	V _{CB} =7.5	RD=2	CO ₂ =3.06pF	VO _B =2.0V
TX=33.72n	11=179.3	11B=4	VT _B =1	XTF=5	Re=10

TABLE 7.3 DC Collector Currents of the Op-Amp Circuits in Fig. 7.1 as Computed by PSpice (Hand Analysis Example 7.4) and by PSpice

Transistor	Collector Currents (mA)		
	Hand Analysis (Example 7.4)	PSpice	Error (%)
Q ₁	0.22	0.281	-11.0
Q ₂	0.22	0.281	-11.0
Q ₃	0.5	0.561	11.8
Q ₄	1.3	1.27	-21.1
Q ₅	1.3	1.21	-17.1
Q ₆	2.0	2.50	-20.0
Q ₇	1.0	1.37	-21.3
Q ₈	5.0	6.17	-18.9
Q ₉	0.5	0.18	-4.2

Q2N3908 from Fairchild Semiconductors for the Q_8 and Q_9 BJTs, respectively. The model parameters of these discrete BJTs are listed in Table 7.3 and are available in PSpice.

In PSpice, the ac-coupled input voltage V_{IN} of the op-amp circuit is set to $V_{\text{IN},\text{dc}}$, to the average of the dc power-supply voltages V_{DD} and V_{SS} , to maximize the available input signal swing. A bias-point simulation is performed to determine the dc operating point. Table 7.3 summarizes the values of the dc collector currents as computed by PSpice and as calculated by the hand analysis in Example 7.4. Recall that our hand analysis assumed β and the Early voltage, V_A , of the BJTs to be both infinite. However, our SPICE simulations in Examples 5.2, where we investigated the dependence of β on the collector current I_C , indicate that the Q2N3904 ($\text{v}_t = \beta = 25 - I_C = 0.25 \text{ mA}$). Furthermore, its forward Early voltage (V_A) is given in Table 7.2 ($V_A = 14 \text{ V}$, as given in Table 7.3). Nevertheless, we observe from Table 7.3 that the largest error in the calculation of the dc bias currents is at the order of 20%. Accordingly, we can conclude that a quick hand analysis using gross approximations can still yield reasonable results for a preliminary estimate and, of course, hand analysis yields much insight into the circuit operation. In addition to the dc bias currents listed in Table 7.3, the bias-point simulation in PSpice shows that the current I_{DD} off Q_9 (i.e., $V_{\text{DD}} = 0$) is 3.02 mA and that the input bias current, I_{BI} , is 2.63 μA .

To compute the large-signal differential transfer characteristic of the op-amp circuit, we perform a dc-analysis simulation in PSpice with the differential voltage input V_{d} swept over the range $-V_{\text{DD}} < V_{\text{d}} < V_{\text{DD}}$ and we plot the corresponding output voltage V_{OUT} . Figure 7.52(a) shows the

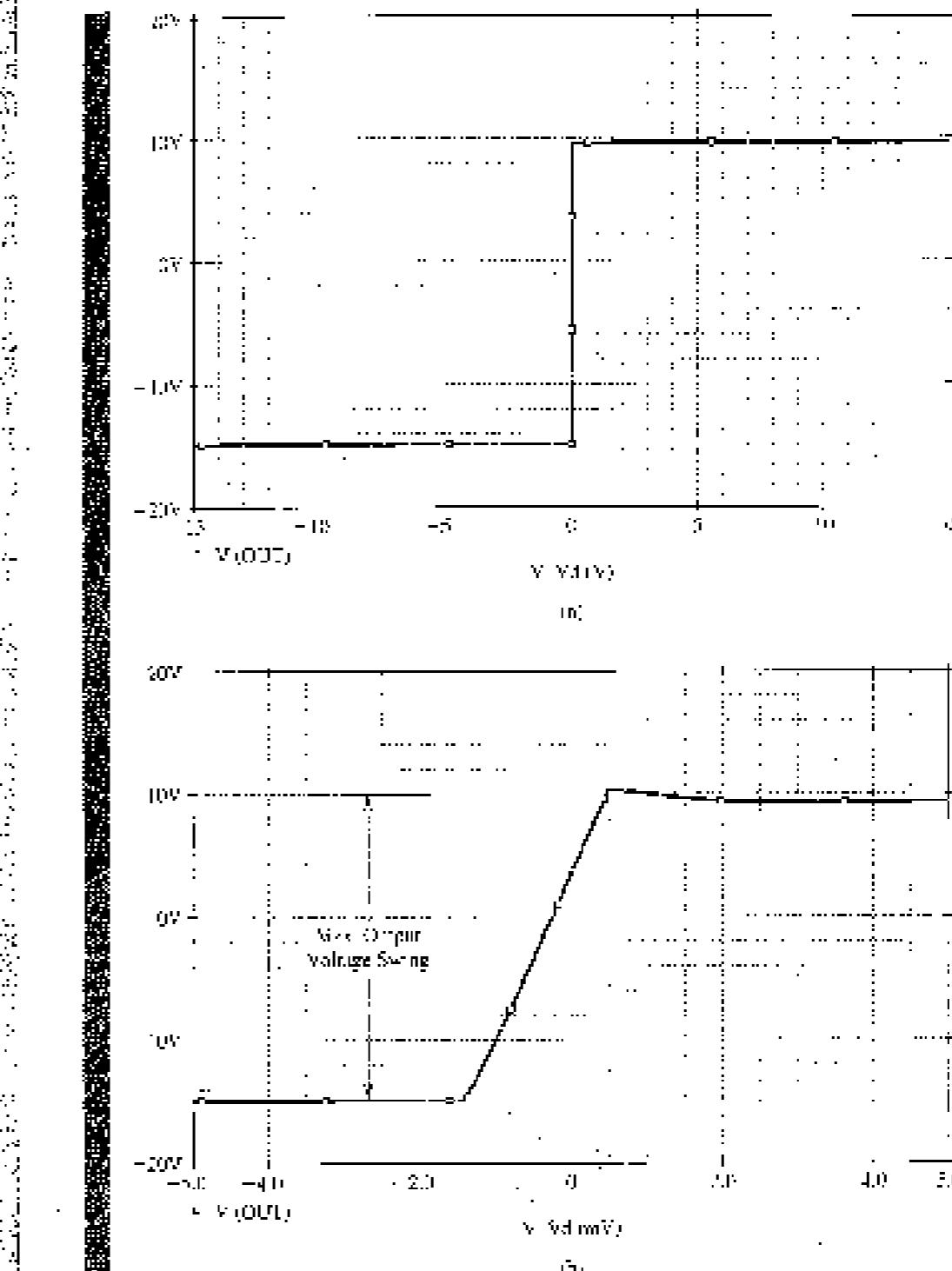


FIGURE 7.52 (a) The large-signal differential transfer characteristics of the op-amp circuit in Fig. 7.1. The common-mode voltage V_{d} is set to 0 V. (b) An expanded view of the transfer characteristic with the x-axis gain 5x.

resulting dc transfer characteristic. The slope of this dc characteristic (*i.e.*, $\partial V_{out}/\partial V_2$) corresponds to the differential gain of the amplifier. Note that, as expected, the high-gain region is the vicinity of $V_2 = 0$ V. However, the regulation of the input-voltage axis is too coarse to yield much information about the details of the high-gain region. Therefore, to examine this region more closely, the dc analysis is repeated with V_2 sweep over the range -5 mV to $+5$ mV at increments of 10 μ V. The resulting differential dc transfer characteristic is plotted in Fig. 7.25(b). Accordingly, the linear region in the large-signal differential characteristic is bounded approximately by $V_2 = -1.5$ mV and $V_2 = +0.5$ mV. Over this region, the output level changes from $V_{out} = -15$ mV to $V_{out} = +15$ mV in a linear fashion. Thus, the output voltage swing for this amplifier is between -15 mV and $+15$ mV, a rather asymmetrical range. A rough estimate for the differential gain of this amplifier can be obtained from the boundaries of the linear region as $A_d = [10 \cdot (-15) \text{ mV} / 2] / [1.5 \text{ mV}] = 10.0 \times 10^3 \text{ V/V}$. We also observe from Fig. 7.25(b) that $V_2 \geq +50$ μ V when $V_{out} = 0$. Therefore, the compliance on an output offset voltage V_{os} of $+50$ μ V (by definition, the negative value of the x -axis intercept of the large-signal differential transfer characteristics). This corresponds to an output offset voltage of $\pm V_{os} = (12.5 \times 10^3)(200 \mu\text{V}) = 3.25$ V, which is close to the value found through the bias-point simulation. It should be emphasized that this offset voltage is inherent in the design and is not the result of component or device mismatch. That is, it is usually referred to as a systematic offset.

Next, to compute the frequency response of the opening circuit and to measure its differential gain A_d and its 3-dB frequency f_T in PSpice, we set the differential input voltage V_2 to be a 1-V ac signal (with 0 V dc level), perform an ac analysis simulation, and plot the output voltage magnitude $|V_{out}|$ versus frequency. Figure 7.25(a) shows the resulting frequency response. Accordingly, $A_d = 13.36 \times 10^3$ V/V or 82.8 dB, and $f_T = 256.9$ kHz. Thus, this value of A_d is closer to the value estimated using the large-signal differential transfer characteristic.

An approximate value of f_T for this is obtained using the approximations derived in Section 7.4.2. Specifically,

$$f_T = \frac{1}{2\pi R_s C_{in}} \quad (7.21)$$

where

$$C_{in} = C_{ds} + C_{ce} + C_{pe} + g_m r_s (R_s \| r_{ce} + (r_{ce} + (\beta + 1)R_s)C_{os})$$

and

$$R_s = R_L + r_{ce} + r_{os}$$

The values of the small-signal parameters as computed by PSpice can be found in the input file of a bias-point (or ac) analysis simulation. Using these values results in $C_{in} = 508$ pF, $R_s = 2.91$ k Ω , and $f_T = 161.71$ Hz. However, the approximate value of f_T is much smaller than the value computed by PSpice. The reason for the disagreement is that the foregoing expression for f_T was developed in Section 7.4.2 using the equivalent differential half-circuit concept. However, the 2000pF is relevant only when it is applied to a symmetrical circuit. The op-amp circuit in Fig. 7.21 is not symmetrical because the second gain stage (formed by the differential pair Q_1-Q_2) has a load resistor R_2 in the collector of Q_2 only. To verify that the expression for f_T in Eq. (7.21) gives a close approximation to f_T in the case of a symmetrical circuit, we insert a resistor R_2' (whose size is equal to R_2) in the collector of Q_1 . More specifically, we will have only a minor effect on the dc operating point. The op-amp circuit with Q_2 having a collector resistor R_2' is then simulated in PSpice. Figure 7.25(c) shows the resulting frequency response of this symmetrical op-amp

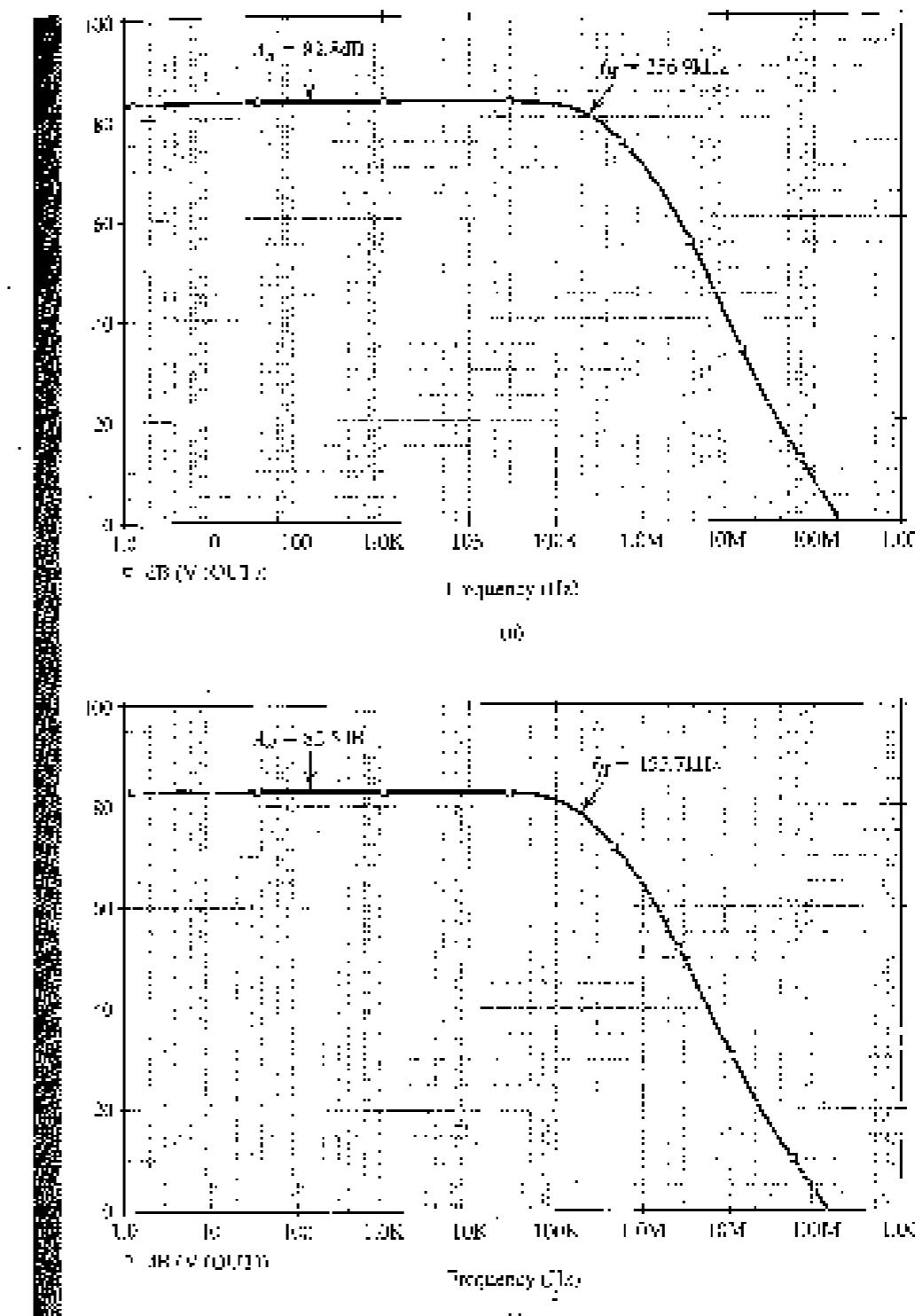


FIGURE 7.25 Frequency response of (a) the op-amp circuit in Fig. 7.21 and (b) the op-amp circuit in Fig. 7.25(b) with resistor $R_2' = R_2$ inserted in the collector of Q_1 to make the $x-y$ circuit symmetrical.

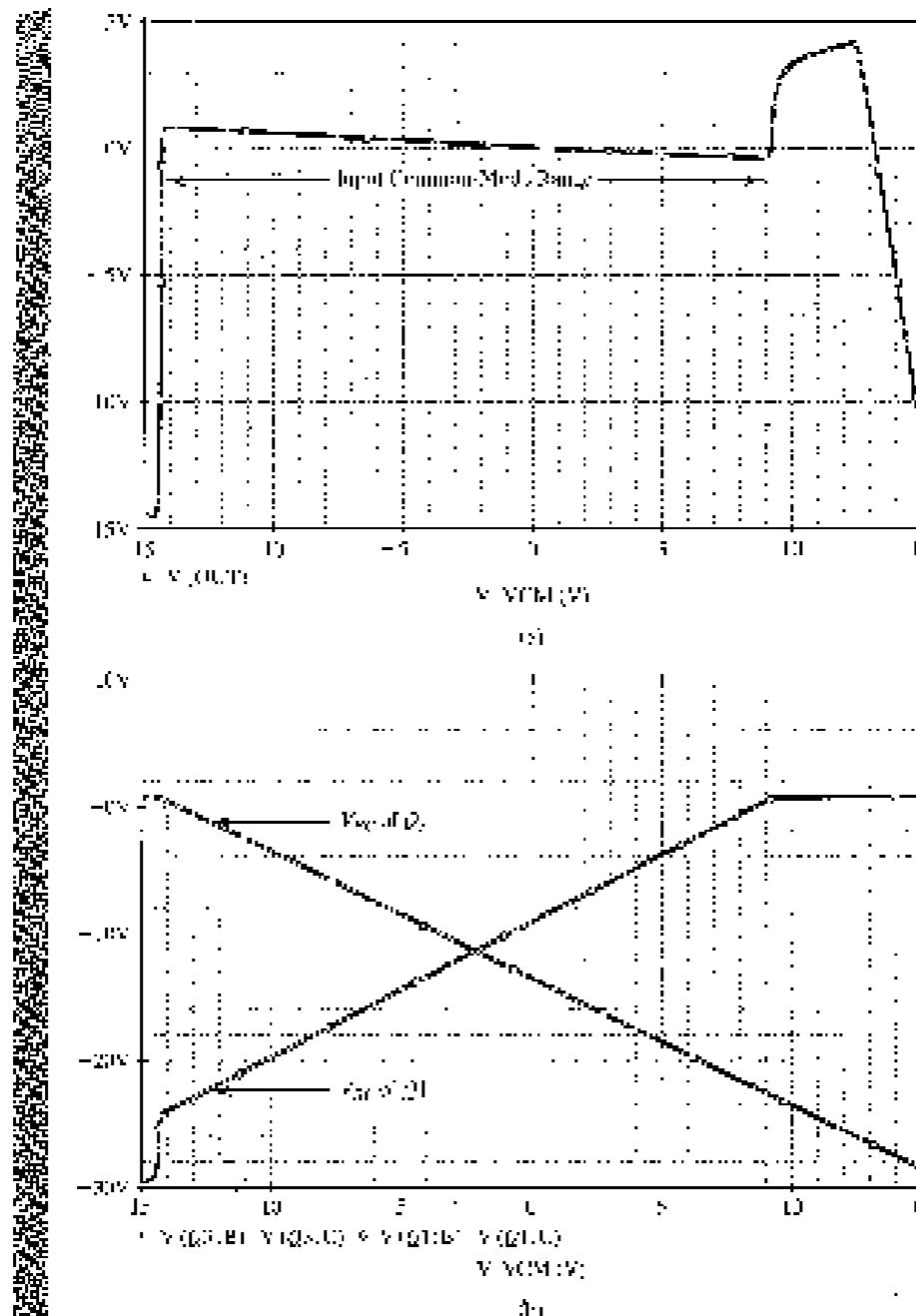


FIGURE 7.54 (a) The large signal common-mode transfer characteristic of the op-amp circuit in Fig. 7.31. The center common voltage V_0 is set to $V_{CC} = 20$ V to prevent saturation. (b) The effect of the common-mode voltage V_{VCM} on the biasing of the input stage of the op-amp. In Fig. 7.31, the above collector voltage of Q_1 and Q_2 is shown as a function of V_{VCM} . The input stage of the op-amp will leave the active region when the base-collector junction of either Q_1 or Q_2 becomes forward biased (i.e., when $V_{BC} \geq 0$).

where $f_a = 155.7$ Hz. Accordingly, in the case of a perfectly symmetric transistor circuit, the value of f_a in Eq. (7.2-7) closely approximates the value computed by PSpice. Considering the frequency response of the noninverting (Fig. 7.59a) and the symmetric (Fig. 7.59b) op-amp circuits, we note that the 3-dB frequency of the op-amp drops from 290.0 kHz to 57 kHz when resistor R_2 is inserted in the collector of Q_2 to make the op-amp a rail-to-rail circuit. This is because, with a resistor R_2 , the collector of Q_2 is no longer at signal ground, hence, C_L experiences the Miller effect. Consequently, the high-frequency response of the op-amp circuit is degraded.

Observe that in the preceding ac-analysis simulation, owing to the systematic offset inherent in the design, the op-amp circuit is operating at an output dc voltage of 3.62 V. However, in the actual circuit implementation (with $V_{DD} = 0$), negative feedback is employed (see Chapters 4 and 8) and the output dc voltage is stabilized at zero. Thus, the small-signal performance of the op-amp circuit can be more accurately simulated by biasing the circuit so as to force operation at this level of output voltage. This can be easily done by applying a differential dc input of $-V_{DD}$. Superimposed on this dc input, we can apply an ac signal to perform an ac-analysis simulation for the purpose of, for example, computing the differential gain and the 3-dB frequency.

Finally, to compute the input common-mode range of the op-amp circuit in Fig. 7.31, we perform a dc-analysis simulation in PSpice with the input common-mode voltage swept over the range $-V_{DD} \leq V_{VCM} \leq V_{CC}$, while maintaining V_0 constant at $-V_{DD}$ in order to cancel the output offset voltage (as calculated earlier) and, thus, prevent premature saturation of the BJTs. The corresponding output voltage V_{OV} is plotted in Fig. 7.54(a). From this common-mode transfer characteristic we find that the amplifier behaves linearly over the V_{VCM} range -11.1 V to $+8.9$ V, which is therefore the input common-mode range. In Example 7.4, we noted that the upper limit of this range is determined by Q_1 and Q_2 saturating, whereas the lower limit is determined by Q_2 saturating. To verify this assertion, we requested PSpice to plot the values of the collector-base voltages of these BJTs versus the input common-mode voltage V_{VCM} . The results are shown in Fig. 7.54(b), from which we note that our assertion is indeed correct (recall that an *npn* BJT enters the saturation region when its base-collector junction becomes forward biased, i.e., $V_{BC} \geq 0$).

SUMMARY

- The differential-gain or differential-mode voltage is the most widely used building block in analog IC design. The input stage of every op amp is a differential amplifier.
- In a MOS (JFET) pair biased by a current source I_b , each device operates at a drain (collector, drain) or $-D$ current I_D^+ / I_D^- and a corresponding oxidative voltage V_{DS} (or analog in JFET). Each device has $I_D = I_D^+ V_{DS} / (2L^2W)$ ($L = 1$ micrometer) and $I_b = V_{GS}/(2L^2)$.
- Transistors and they do not have bypass and coupling capacitors.
- For a MOS (JFET) pair biased by a current source I_b , each device operates at a drain (collector, drain) or $-D$ current I_D^+ / I_D^- and a corresponding oxidative voltage V_{DS} (or analog in JFET). Each device has $I_D = I_D^+ V_{DS} / (2L^2W)$ ($L = 1$ micrometer) and $I_b = V_{GS}/(2L^2)$.

- With the two input terminals connected to a suitable dc voltage V_{dd} , the bias current I of a symmetrically symmetrical differential pair divides equally between the two transistors of the pair, resulting in a zero voltage difference between the two drains (collector). To save the current, connect only to one side of the pair, a difference input voltage v_{in} of at least $\sqrt{2}V_{DD}$ (4V_D for bipolar) is needed.
- Superimposing a differential input signal v_{in} on the common-mode input voltage V_{DD} such that $v_1 = V_{DD} + v_{in}/2$ and $v_2 = V_{DD} - v_{in}/2$ causes a virtual ground to appear on the common-source terminal (emitter). In response to v_{in} , the current in Q_1 increases by $\beta_1 v_{in}/2$ and the current in Q_2 decreases by $\beta_2 v_{in}/2$. Thus, voltage signals of $\beta_1 (R_D/2)v_{in}/2$ develop at V_{DS1} (an output collector) with R_D replaced by R_{DS1} . If the output voltage is taken single-ended, that is, between one of the drains (collectors) and common, a differential gain of $\beta_1 (R_D/2)$ is realized. Taking the output differentially, that is, between the two drains (emitters), the differential gain will be twice as large, $\beta_1 (\beta_1 + \beta_2)$.
- The analysis of a differential amplifier to determine differential gain, differential input resistance, frequency response, and CMRR is facilitated by employing the differential half-circuit, which is a common-source common-emitter (cascode) biased at 1/2.
- An input common-mode signal v_{CM} gives rise to drain (collector) voltage signals that are (ideally) equal and given by $(R_D/2R_{DS1})[-v_{CM}/R_{DS1}/2R_{DS2}]$ for the bipolar case, where R_{DS1} (R_{DS2}) is the output resistance of the current source that supplies the bias current I . When the circuit is taken single-endedly, a common-mode gain of magnitude $A_{CM} = R_D/2R_{DS1}$ ($R_D/2R_{DS2}$ for the bipolar case). Taking the output differentially results in the perfectly matched case in zero A_{CM} (infinite CMRR). Mismatches between the two sides of the pair make A_{CM} finite even when the output is taken differentially. A mismatch ΔR_{DS} causes $|A_{CM}| = (R_D/2R_{DS1})(\Delta R_{DS}/R_{DS})$; a mismatch $\Delta \beta$ causes $|A_{CM}| = (R_D/2R_{DS1})(\Delta \beta_1/\beta_1)$. Corresponding expressions apply for the bipolar pair.
- While the input differential resistance R_{in} of the MOS pair is infinite, that for the bipolar pair is only $2r_s$ but can be increased to $2(\beta_1 + \beta_2) + R_D$ by including resistors R_D of the same value. The latter action, however, lowers A_{in} .

■ Mismatches between the two sides of a differential pair result in a differential output voltage V_{DS} even when the two input terminals are tied together and connected to a dc voltage V_{DD} . This signifies the presence of a common-mode voltage $V_{DD} - V_{DS}$. This MOS pair here has two main sources for V_{DS} :

$$\Delta R_{DS} \rightarrow V_{DS} = \frac{V_{DD}}{2} \frac{\Delta R_{DS}}{R_D}$$

$$\Delta (W/L) \rightarrow V_{DS} = \frac{V_{DD}}{2} \frac{\Delta (W/L)}{WL}$$

$$\Delta V_{GS} \rightarrow V_{DS} = \Delta V_{GS}$$

For the bipolar pair there are two contributors:

$$\Delta R_{DS} \rightarrow V_{DS} = \frac{\Delta R_{DS}}{N}$$

$$\Delta V_{GS} \rightarrow V_{DS} = V_1 \frac{\Delta V_{GS}}{I_0}$$

■ A popular circuit is both MOS and bipolar using W/L s of the emitter-nitter-base (ENB) differential pair. In real v_{in} , a high differential gain, $A_{in} = \mu_n (N_{in1} + 1) R_{in1,1}$ (i.e., a low common-mode gain, $A_{CM} = \frac{1}{2} \mu_n R_{in1}$ for the MOS circuit or $\beta_1 R_{DS1}$ for the bipolar case), as well as performing the differential-to-single-ended conversion with no loss of gain.

■ The common-mode gain in the differential output exhibits a transmission zero caused by the finite output resistance and capacitance of the bias current source; $j\omega = \frac{1}{2}C_{DS}R_{DS} + \frac{1}{2}C_{DS}R_{DS}$ for bipolar. Thus, the CMRR has a pole at this relatively low frequency.

■ A multivoltage amplifier usually consists of three stages: an input stage having a high input resistance, a reasonably high gain, and, if differential, a high CMRR; an intermediate stage that reduces the gain of the pair and an output stage having a low output resistance. Many CMOS amplifiers serve to drive only small on-chip capacitive loads and hence do not need an output stage. In designing multivoltage amplifiers, the loading effect of each stage on the next that precedes it must be taken into account.

PROBLEMS

SECTION 7.1: THE NMOS DIFFERENTIAL PAIR

7.1 For an NMOS differential pair with a common-mode voltage V_{DD} applied as shown in Fig. 7.2, let $V_{DD} = V_D = 2.5$ V, $k^*(W/L) = 400 \mu A/V^2$, $V_t = 0.7$ V, $I = 0.2$ mA, $R_D = 5$ k Ω , and neglect channel-length modulation.

(a) Find V_{GS1} and V_{GS2} for each transistor.

(b) For $v_{in1} = 0$, find v_{in2} , i_{D1} , i_{D2} , and v_{DS1} .

(c) Suppose $v_{in1} = 1.1$ V.

(d) If $v_{in1} = 0$ and $v_{in2} = v_{in}$, find the range of v_{in} required to keep the bias current from one side of the pair to the other. At each end of this range, give the value of the voltage in the common-source terminal and the drain voltages.

7.2 Consider the differential amplifier specified in Problem 7.1 with G produced and $v_{in1} = v_{in2}$. Let v_{in} be adjusted to the value that makes $i_{D1} = 0.1$ mA and $i_{D2} = 0.09$ mA. Find the corresponding values of v_{DS1} , v_{DS2} , and v_{in} . Hence $v_{in} = V_D - 100$ mV. What is the differential output voltage $v_{DS1} - v_{DS2}$? What is the voltage gain $(v_{DS1} - v_{DS2})/v_{in}$? What value of v_{in} results in $i_{D1} = 0.09$ mA and $i_{D2} = 0.1$ mA?

7.3 For the PMOS differential amplifier shown in Fig. P7.2 let $V_D = 0.7$ V and $k^*(W/L) = 3.5 \mu A/V^2$. Neglect channel-length modulation.

(a) For $v_{in1} = v_{in2} = 0$ V, find V_{GS1} and V_{GS2} for each of Q_1 and Q_2 . Also find i_{D1} , i_{D2} , and v_{DS1} .

(b) If the drain source voltage is constant at 0.5 V, find the input common-mode range.

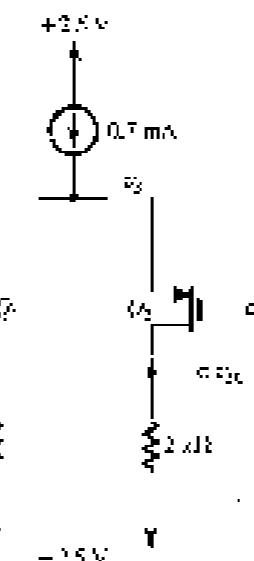


FIGURE P7.2

7.4 For the differential amplifier specified in Problem 7.1 let $v_{in1} = 0$ and $v_{in2} = v_{in}$. Find the value of v_{in} that corresponds to each of the following situations:

(a) $i_{D1} = i_{D2} = 0.1$ mA; (b) $i_{D1} = 0.15$ mA and $i_{D2} = 0.05$ mA; (c) $i_{D1} = 0.1$ mA and $i_{D2} = 0$ (Q₂ just cuts off); (d) $i_{D1} = 0.05$ mA

and $i_{D2} = 0.15$ mA; (e) $i_{D1} = 0$ mA (Q_1 just cuts off) and $i_{D2} = 0.2$ mA. For each case, find v_{GS1} , v_{GS2} , and $v_{DS1} - v_{DS2}$.

7.5 For the differential amplifier specified in Problem 7.1, let $v_{in1} = 0$ and $v_{in2} = v_{in}$. Find the range of v_{in} required to keep the bias current from one side of the pair to the other. At each end of this range, give the value of the voltage in the common-source terminal and the drain voltages.

7.6 Consider the differential amplifier specified in Problem 7.1 with G produced and $v_{in1} = v_{in2}$. Let v_{in} be adjusted to the value that makes $i_{D1} = 0.1$ mA and $i_{D2} = 0.09$ mA. Find the corresponding values of v_{DS1} , v_{DS2} , and v_{in} . Hence $v_{in} = V_D - 100$ mV. What is the differential output voltage $v_{DS1} - v_{DS2}$? What is the voltage gain $(v_{DS1} - v_{DS2})/v_{in}$? What value of v_{in} results in $i_{D1} = 0.09$ mA and $i_{D2} = 0.1$ mA?

7.7 The table providing the answers to Exercise 7.2 shows that as the maximum input signal is applied to the differential pair is increased, linearity is maintained at the same level by increasing v_{in} by $k(v_{in})$. If $|v_{in}|_{max}$ is to be 150 mV, use the data in the table to determine the required V_{DD} and the corresponding values of W/L and g_m .

7.8 Use Eq. (7.23) to show that if the maximum value v_{in} is to be kept to a maximum value of k then the maximum possible fractional change in the transistors currents is given by

$$\left(\frac{\Delta I_{DS}}{I/2} \right) = 2\sqrt{k(1-k)}$$

and the corresponding maximum value of v_{in} is given by

$$v_{in,max} = 2\sqrt{k}V_{DD}$$

Evaluate both expressions for $k = 0.01$, 0.1, and 0.2.

7.9 An NMOS differential amplifier utilizes a bias current of 200 μ A. The devices have $V_t = 0.5$ V, $W = 100 \mu m$, and $L = 1.6 \mu m$, in a technology for which $\mu_n C_{ox} = 90 \mu A/V^2$. Find V_{DD} , A_{in} , and the value of v_{in} for full-current switching. To what value should the bias current be changed in order to double the value of v_{in} for full-current switching?

7.10 Design the MOS differential amplifier of Fig. 7.5 to operate at $V_{DD} = 0.2$ V and to provide a transconductance g_m of 1 m A/V . Specify the W/L ratios and the bias current. The technology available provides $V_t = 0.8$ V and $\mu_n C_{ox} = 90 \mu A/V^2$.

7.11 Consider the NMOS differential pair illustrated in Fig. 7.5 under the conditions that $I = 100 \mu$ A, using H.L.T. for which $k^*(W/L) = 400 \mu A/V^2$, and $V_t = 1$ V. What is the value of the maximum source resistance for $v_{in1} = v_{in2} = 0.2$ V? What is the relation between the drain currents of each

of these situations? Now for $V_{DD} = 0$ V, at what voltages must V_D be placed to reduce I_{DQ} by 10% or increase I_{DQ} by 100%? What is the differential voltage, $V_{DS} = V_{DD} - V_D$, for which the ratio of drain currents in A_{DD} is 1.0? 0.5? 0.9? 1.1? For the constant current $A_{DD} = 30.0$, what differential voltage is required?

SECTION 7.2: SMALL-SIGNAL OPERATION OF THE MOS DIFFERENTIAL PAIR

7.1.1 An NMOS differential amplifier is operated at a bias current, I_D , of 0.5 mA and has a drain ratio of 50, $\mu_C/\mu_B = 250 \mu\text{A/V}^2$, $V_D = 10$ V, and $R_D = 4$ k Ω . From V_{DD} , v_{in} , A_{vD} , and C_L ,

D7.12 It is required to design an NMOS differential amplifier to operate with a differential input voltage that can range from 0.1 V to 1.0 V. The output voltage must be able to swing between 0.1 V and 1.0 V.

At high voltage, the following two conditions must be satisfied:
 The square root of R_2 (7.53) is a maximum of 0.1. A transconductance $\mu_A = 3 \text{ mA/V}$ is needed. Find the required values of V_{DD} , T , and FWL . Assume that the transistors per stage have $\mu_A C_o = 150 \text{ pA/V}^2$. What differentiated gain does this give when $R_2 = 1 \text{ k}\Omega^2$? Assume $A = 0$. What is the resulting output signal voltage according to v_{ds} at its maximum value?

077.13 Figure P7.13 shows a circuit. For a differential amplifier with an active load, there \mathcal{Q}_1 and \mathcal{Q}_2 form the differential pair while the current source transistors \mathcal{Q}_3 and \mathcal{Q}_4 form the active loads for \mathcal{Q}_1 and \mathcal{Q}_2 , respectively. The biasing network consists of resistors R_1 through R_4 and voltage sources V_{B1} and V_{B2} . The output voltage is $V_{O1} = V_{O2}$.

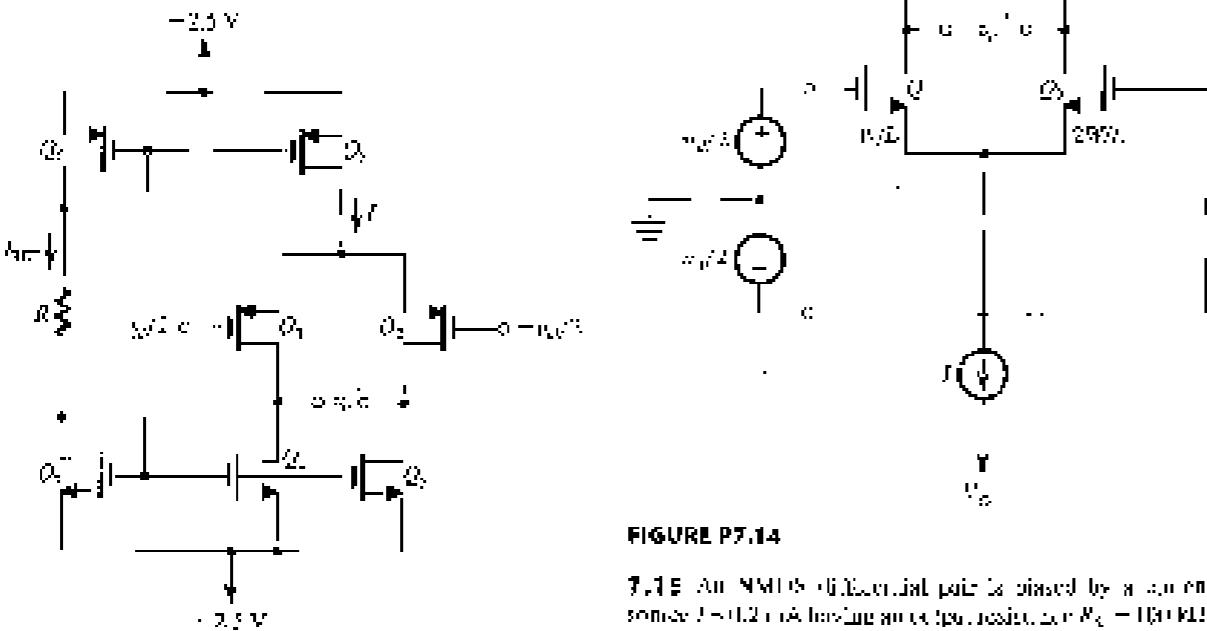


FIGURE P7.14

7.15 An NMOS differential pair is biased by a current source $I = 0.12 \mu\text{A}$ having an output resistance $R_S = 100 \text{ k}\Omega$. The output has drain resistances $R_D = 10 \text{ M}\Omega$, using transistors with $V_{FBV} = 3 \text{ mV/V}^2$, and n_s that is large.

(g) The cultural class displacement, for $|V_0|$, A_{ext} , and C_{MB} .

(g) If the unique solution differentially and there is a 1% mismatch between the true resistances, find $\{R_x\}$, $\{V_{ex}\}$, and G_{ME} .

7.56 For the differential amplifier shown in Fig. P7.5.1, if \mathcal{Q}_1 and \mathcal{Q}_2 have $V_A(1M\Omega) = 100 \text{ mV/V}^2$, and assume that \mathcal{Q}_3 has current source bias at output resistance of $30 \text{ k}\Omega$. Let $V_{IN1} = 10 \mu\text{V}$, $A_{DC1} = 100$, and the CMRR is 60 dB , this is with the output taken differentially. The drain resistances are known to have a mismatch of 2% .

B7.17 The differential amplifier in Fig. B7.17 utilizes a resistor R_{g} to establish a -1mA dc bias current. Note that this amplifier uses a single 5 V supply and thus needs a dc beam-current voltage $V_{\text{B}} = 1\text{ V}$. The transistors P_1 and Q_2 have $\beta = 100$, $-2.5 \mu\text{A/V}^2$, $V_T = 0.7\text{ V}$, and $\lambda = 0$.

- (c) Find the required value of R_2 .
 (d) Find the value of R_1 that results in a differential gain A_{vD} of 8 V/V.
 (e) Determine the no voltage of the circuits.
 (f) Determine the output impedances from A_{V21}/A_{V22} . (Hint: You need to take Fig. 1 into account.)
 (g) Use the common mode gains found in (d) to determine the charge in C_{21} that results in Q_1 and Q_2 entering the block 12000.

$$A_{\text{min}} = \left[\frac{R_0}{\lambda^2} \left(\frac{2g_{\text{eff}}}{\pi} + \frac{\Delta M_0}{\lambda} \right) \right]$$

Note that this equation indicates that R_{p} can be deliberately varied to compensate for the initial variability of y_{p} and R_{m} (see Fig. 10.10 and 10.12).

- (b) In a 3408 differential transformer, the values $R_{A_1} = 3.25\Omega$ and $R_{A_2} = 25.32\Omega$, the secondary-mode voltage measured and found to be 0.002 V/V. Find the percentage change required in one of the resistors to reduce A_{v2} to zero for class A operation.

7.12 Recalling that τ_c of a MOSFET is given by

$$g_i = k_i \left[\sum_{j=1}^W (V_{ij} - V) \right]$$

We observe that there are two potential sources for a mismatch between the y_+ values in a differential pair: a mismatch $\Delta B(B)$ in the $(B(t))$ values and a mismatch ΔV in the transconductance values. Hence, show that

$$\frac{\Delta G_{\text{ex}}}{E_{\text{ex}}} = \frac{\Delta (W/T)}{kT} + \frac{\Delta Y_1}{E_{\text{ex}}}$$

Find the worst-case transient mismatch in g_{m} for a differential pair in which the (V_A) values have a tolerance of $\pm 1\%$ and the largest orientation in V_T is specified to be $\pm 1\%$. Assume that the pair is operating at $V_{DD} = 0.25$ V, if $R_D = 5\text{ k}\Omega$ and $R_{SD} = 15\text{ k}\Omega$, and the worst-case value of α_{DD} . If the bias current $I = 1\text{ mA}$, find the corresponding worst-case CMRR.

SECTION 7.3: THE BJT DIFFERENTIAL PAIR

7.38 For the differential amplifier of Fig. 7.13(a) let $I = 1 \text{ mA}$, $V_{CC} = 5 \text{ V}$, $R_A = 2 \text{ M}\Omega$, $R = 3 \text{ k}\Omega$, and $\beta = 100$. Assume that the BJT's have $\alpha_{FE} = 0.95$ at $I_C = 1 \text{ mA}$. Find the voltage at the output v_o as a function of the input v_i .

2.2.2 For the circuit of Fig. 2.1.1(b) with an input of $+1 \text{ V}_\text{DC}$, find the output voltage and with $C = 1 \text{ nF}$, $V_\text{DD} = 5 \text{ V}$, $R_\text{D} = 4 \text{ k}\Omega$, and $\beta = 100$, find the voltage at the emitters and the collector voltages. Assume that the BJT is in $v_\text{BE} = 0.7 \text{ V}$ at $I = 1 \text{ mA}$.

7.1.2 Repeat for $\alpha = 0.72$, 0.75 , 0.78 (in a range of $-0.3 \leq \chi$,

7.53 For the BJT differential amplifier of Fig. 7.12 (a), if the value of the input differential signal, $v_{o1} - v_{o2}$, is 0.8, what is v_{o1} ?

Q3.24 Consider the differential amplifier of Fig. 3.12 and let the 2.1T rule be assumed.

(a) What is the largest input voltage magnitude signal that can be applied while the DCTs work comfortably on the service account with $\alpha = 0^\circ$?

(b) If an input v_1 reference signal is applied that is large enough to bias the current entirely to one side of the pair, what is the change i_c voltage across collector-emitter resistors for which $v_o = 0$?

(c) If the available power supply V_{cc} is 5 V, what value of R_E should you choose in order to allow a maximum audio input signal of 25 mV?

(d) For the value of R_E found in (c), calculate α and R_o . Use the larger possible value for β subject to the constraint that the base-to-collector voltage in (when divided equally) should not exceed 200 mV. Let $\beta = 100$.

7.45 To provide straightforward possibility of negative differential resistance from large differential input signals applied to their transistors amplifiers, Fig. 7.12 includes a degeneration stage in the output i_{ce} , $\beta = (I_{CQ}/(I/2))/\beta$, i.e., differential input signals v_1 (0.5 , 1.0 , 2.0 , 3.0 , and 4.0 V) provide a calculation of the ratio $(v_{A1} + v_{A2})/v_{A1}$, which represents the proportional transconductance gain of the differential pair, versus v_{A1} (constant) or either the two input signals or output.

7.46 Design the circuit of Fig. 7.12 to provide a differential output voltage (i.e., one taken between the two collectors) of 1 V when the differential input sig $v_1 = 10$ mV. A common-emitter of 100mA and a positive supply of $+10$ V are used. What is the largest possible input common-mode voltage for which operation is as required? Assume $\alpha = 1$.

7.47 One of the trade-offs available to the designer of the basic differential amplifier circuit of Fig. 7.12 is between the value of the voltage gain and the range of common-mode input voltage. The purpose of this problem is to demonstrate this trade-off.

(a) Use Eqs. (7.32) and (7.33) to obtain i_{A1} and i_{A2} corresponding to a differential input signal of 5 mV ($v_{A1} = -v_{A2} = 5$ mV). Assume $\beta = 100$ and $\alpha = 1$. Find the resulting $v_{o1} - v_{o2}$ difference between the two collectors ($v_{o1} = v_{o2}$) and divide this value by 5 mV to obtain the voltage gain in terms of (R_E) .

(b) Find the maximum permitted value for v_{cm} (Fig. 7.11(a)) while the transistors remain in common-mode. In the same mode with $v_{cm} = 0$, Express the maximum in terms of V_{cc} and β . Notice also that for a given value of V_{cc} , the higher the gain achieved, the lower the common-mode range. Use this expression to find values corresponding to a gain margin rate of 100 , 200 , 300 , and 400 mV. For each value also plot the required value of R_E (use the value of $\beta = 100$).

*7.48 For the circuit of Fig. 7.12, assume $\alpha = 1$ and $R_E = 5$ V, use Eqs. (7.32) and (7.33) to find i_{A1} and i_{A2} , and hence determine $v_{o1} = v_{o2}$ ($v_{A1} = -v_{A2}$) of 5 mV, 10 mV, 15 mV, 20 mV, 25 mV, 30 mV, and 40 mV. Plot v_{o1} versus v_{A1} and hence comment on the amplifier's linearity. As another way of evaluating linearity, determine the gain (v_{o1}/v_{A1}) versus v_{A1} . Comment on the resulting graph.

7.49 In a differential amplifier using a common-emitter bias circuit, one of the two BJTs is not well matched. Rather, one has one-half the collector current of the other. For a differential input signal of zero volts, what do the collector currents become? What difference input is needed to equate the collector currents? Assume $\alpha = 1$.

7.50 Figure P7.30 shows a logic inverter based on the differential pair. Here, Q_1 and Q_2 form the differential pair, whereas Q_3 is an emitter follower that performs two functions: it shifts the level of the output voltage v_o relative to V_{cc} and V_{bb} centered on the reference voltage V_{bb} . On enabling v_{bb} with a drive voltage (this point will be explained in detail in Chapter 13), it provides the inverter with a low output resistance. All transistors have $V_{BE} = 0.7$ V at $I_c = 1$ mA and $\beta = 100$.

(a) For v_{bb} sufficiently low so that Q_3 is cut off, find the value of the output voltage v_o (it's $\neq V_{cc}$).

(b) For v_{bb} sufficiently high that Q_3 is conducting at the current I , find the output voltage v_o . This is Fig.

(c) Determine the value of v_{bb} that results in Q_3 conducting 10% of I . This can be taken as V_{bb} .

(d) Determine the value of v_{bb} that has Q_3 conducting $10\% \times I$. This can be taken as V_{bb} .

(e) Sketch and clearly label the hysteresis of the inverter voltage transfer characteristic. Calculate the values of the noise margins NM_H and NM_L . Note the judicious choice of the value of the reference voltage V_{bb} .

For the definitions of the parameters they are used to characterize the inverter VTC, refer to Section 13.3.

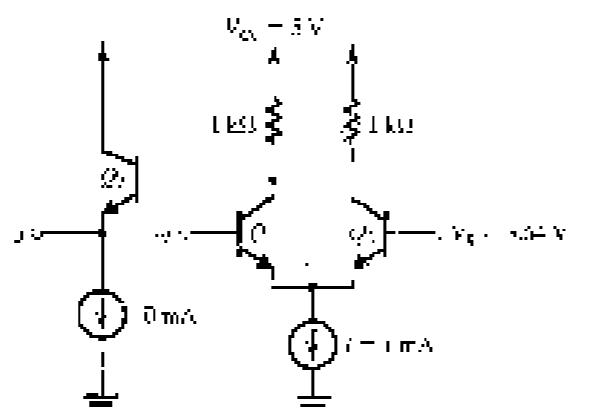


FIGURE P7.30

7.51 A BJT differential amplifier uses a $100\mu\text{A}$ bias current. What is the value of v_o at each device if $\beta = 100$, where is the differential input voltage?

7.52 Design the basic BJT differential amplifier circuit of Fig. 7 to provide a differential input resistance of at least 10 k Ω and a defined (the voltage v_{o1}) (given the input current

(between the two collectors) of 200 mV. The transistor β is specified to be at least 100 . The available power supply is 10 V.

7.53 For a differential amplifier in which a total difference signal of 10 mV is applied, what is the collector signal in its common-emitter output if the emitter current source is 100mA , $v_{bb} = 5$ V, the left circuit? The load resistance of $10\text{k}\Omega$ in each collector, what is the half-circuit gain? What magnitude of signal output voltage would you expect at each collector?

7.54 A BJT differential amplifier is obtained from a 2-mA common-emitter source and includes a $100\mu\text{A}$ resistor to each emitter. The voltage source connected to V_{bb} is 10 mV. A differential input signal of 1 mV is applied between the two bases.

(a) Find the signal current in the emitters (i_b) from the signal voltage v_{bb} for each BJT.

(b) What is the total emitter current in each BJT?

(c) What is signal voltage at output v_o ? Assume $\alpha = 1$.

(d) What is the voltage gain realized when the input is taken between the two collectors?

7.55 Design a BJT differential amplifier to amplify a difference input signal of 0.2 V and provide a differential output signal of 4 V. To ensure a large linear headroom, it is required to limit the signal amplitude whose collector-base junction is a maximum of 0.7 mV. Another design requirement is that the differential input resistance be at least $80\text{k}\Omega$. The BJTs available are specified to have $\beta > 200$. Give the circuit configuration and specify the values of all its components.

7.56 A parasitic differential amplifier operating from an emitter current source whose output resistance is $1\text{M}\Omega$. When source is terminated with each common-emitter half circuit by a load resistor of $20\text{k}\Omega$, what is the resulting common-mode gain for output taken (a) differentially, (b) single-endedly?

7.57 Find the voltage gain and the input resistance of the amplifier shown in Fig. P7.37 assuming $\beta = 100$.

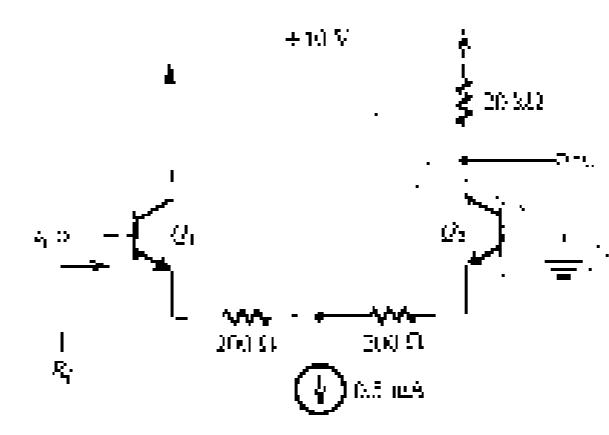


FIGURE P7.37

7.58 Find the voltage gain and input resistance of the amplifier in Fig. P7.38 assuming $\beta = 100$.

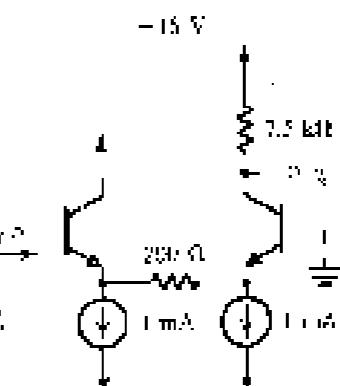


FIGURE P7.38

7.59 Derive an expression for the small-signal voltage gain v_o/v_{in} of the circuit shown in Fig. P7.39 in two different ways.

can as a differential amplifier

(a) as a cascade of a common-emitter stage Q_1 and a common-base stage Q_2

Assume that the BJTs are matched and have a current gain of β . Verify that both approaches lead to the same result.

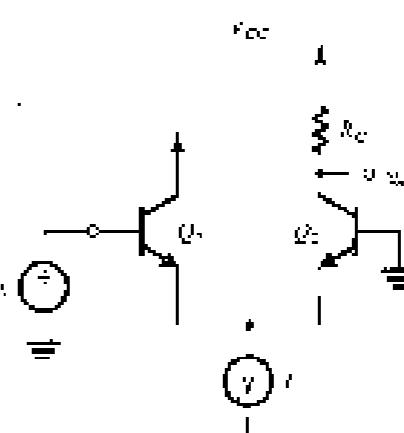


FIGURE P7.39

7.60 The differential amplifier circuit of Fig. P7.40 utilizes a resistor R_1 connected to the negative power supply to establish the bias current.

(a) For $v_{in} = v_{nn}/2$ and $v_{in} = -v_{in}/2$, where v_{in} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{in}|$.

(b) For $v_{in} = v_{nn} = v_{in}$, find the magnitude of the common-mode gain, $|v_o/v_{in}|$.

(c) Calculate the CMRR.

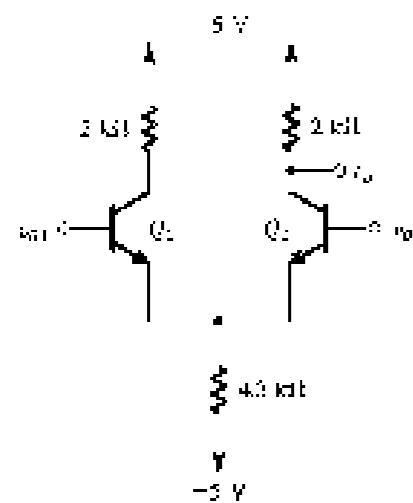


FIGURE P7.40

$$(a) 15 \mu\text{A} + 0.1 \sin 2\pi \times 60t + 0.005 \sin 2\pi \times 1000t \text{ uA}$$

$$v_2 = 0.1 \sin 2\pi \times 60t + 0.15 \times 10^{-6} \sin 1000t \text{ uV}$$

P7.41 For the differential amplifier shown in Fig. P7.41, identify and sketch the differential voltage and the common-mode half-current. Fix the collector load, the differential input resistance, the common-mode gain, and the common-mode input resistance. For these constants, $\beta = 100$ and $V_T = 100$ mV.

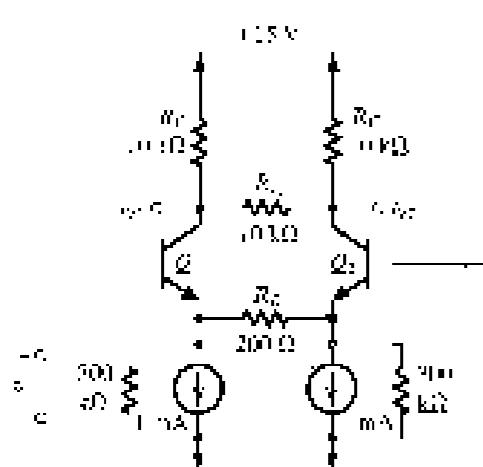


FIGURE P7.41

P7.42 Consider the basic differential circuit in which the transistors have $\beta = 200$ and $V_T = 200$ mV, with $i = 0.7$ mA, $R_{ce1} = 1.4 k\Omega$, and $R_{ce2} = 20 k\Omega$. Then

- (a) the differential gain is a single-ended output
- (b) the differential pair is a differential output

- (c) the differential input resistance
- (d) the common-mode gain is a single-ended output
- (e) the common-mode gain is a differential output

P7.43 In a differential amplifier circuit resembling that shown in Fig. 7.26(a), the current generator represented by β_1 and R_{ce1} consists of a pair of NPN transistors operating at $i_1 = 100 \mu\text{A}$. For this transistor, and also need in the differential pair, $V_T = 200$ mV and $\beta = 50$. With common-mode input resistance would apply?

P7.44 It is required to design a differential amplifier to provide the largest possible signal in a pair of $10 \text{ k}\Omega$ load resistances. The input differential signal is a sine wave of 5-mV peak amplitude which is applied to the input terminals, while the DC input terminal is zero. The power-supply available is 10 V. To determine the bias current required, I , derive an expression for the total voltage at each of the collectors in terms of V_{cc} and I in the presence of the input signal. Then integrate the expression for each voltage, since it must well out of saturation with a maximum value of approximately 0.5 V. Thus determine the required value of I . For this design, what differential gain is achieved? What is the amplitude of the digital voltage obtained between the two collectors? Assume $\beta = 1$.

*P7.45 Design a CMOS differential amplifier that provides two single-ended outputs for the rail-to-rail. The input is to be a 100 pA current source in the middle of the two emitters of a 2×10^4 - pA current mirror. The output resistances R_{ce1} and R_{ce2} are to be equal (so each of the two outputs no greater than 0.1 V/V). Use a 2-mV current source for biasing. Give the complete circuit with component values and variable power supplies not closer than 12 V from a each collector. Specify the minimum value that the output resistance at the bias current source must have. (The BJTs available have $\beta = 200$. What is the value of the input current mode resistance when the bias source set the lowest acceptable resistance?)

P7.46 When the output of a BJT differential amplifier is taken differentially, its CMRR is found to be 40 dB higher than when the output is taken single-ended. If the only source of common-mode gain when the outputs taken differentially is the mismatch in collector resistances, what must this mismatch be (in percent)?

*P7.47 In a particular HBT differential amplifier, a reduction of 10% in one of the transistors' β values causes the base junction current to double that of the other. With the inputs grounded, how will the emitter bias current split between the two transistors? If the output resistance of the current source is $1 \text{ M}\Omega$ and the resistance in each collector (R_{ce}) is $2 \text{ k}\Omega$, find the common-mode gain when the output is taken differentially. Assume $\alpha = 1$.

SECTION 7.4: OTHER NONIDEAL CHARACTERISTICS OF THE DIFFERENTIAL AMPLIFIER

P7.48 An NMOS differential pair is to be used in an amplifier whose drain resistors are $10 \text{ k}\Omega \pm 1\%$. For the pair, $V_{GS} = 0.5 \text{ V}$ and $\beta = 100 \mu\text{A}/\text{V}^2$. A decision is to be made concerning the bias current. It is proposed either $200 \mu\text{A}$ or $400 \mu\text{A}$. For the second output, control the 100% output ground rail offset voltage for the two possibilities.

P7.49 An NMOS amplifier whose designed operating point is at $V_{GS} = 0.5 \text{ V}$, is suspected to have a variability of $\pm 1.5 \text{ mV}$, and $\beta = 100 \pm 1\%$ independently of $\pm 2\%$. What is the worst-case total offset voltage you would expect to find? Note, is the sum of contributions to the total offset? If you used a variation of one of the drain resistors to reduce the output offset to zero and thereby compensate for the uncertainties in V_{GS} , that of the pair, β , what percentage change from around $100 \mu\text{A}$ do you expect? (By selection you can set the contribution of the worst case offset by ± 1 due to $\pm 1\%$; what change in R_d would be needed?)

P7.50 An NMOS differential pair operating at a bias current of $100 \mu\text{A}$ has resistors for which $R_d = 100 \text{ }\mu\text{A}/\text{V}$ and $\beta = 2\%$, with $V = 0.8 \text{ V}$. Find the main components of input offset voltage under the conditions that $\Delta R_d / R_d = 5\%$, $\Delta V_{GS} / V_{GS} = 5\%$, and $\Delta \beta / \beta = 5\%$. In the worst case, what might the total offset be? (For the usual case of the three effects being independent, what is the overall likely $\pm 3\%$ offset?) For the latter situation, use a root sum of squares computation.)

P7.51 A differential amplifier using a $600 \mu\text{A}$ emitter bias and $100 \mu\text{A}$ per transistor matched transistor per collector load resistors that are mismatched by 10% at upper offset voltage, is required to reduce the differential output to 10% of its original value.

P7.52 A differential amplifier using a $600 \mu\text{A}$ emitter bias source uses two transistors whose scale currents β differ by 10%. If the β 's are to be reasonably well matched, find the resulting input offset voltage.

P7.53 Modify Eq. (7.155) for the case of a differential amplifier having a resistance, R , connected to the emitter of each transistor. Let the bias current source be I .

P7.54 A differential amplifier uses two transistors whose β values are β_1 and β_2 . If everything else is matched, (Note that the input offset voltage is approximately $V_T(\beta_1/\beta_2)^2(1/\beta_2)$). Reduce β_2 so that $\beta_1 = 100$ and $\beta_2 = 300$. Assume the differential source resistance to be zero.

*P7.55 A differential amplifier uses two transistors having V_T values of 100 mV and 130 mV. If everything else is matched, the

the resulting input offset voltage. Assume that the two transistors are intended to be biased at V_{GS} of about 100 mV.

*P7.56 A differential amplifier is fed in a balanced-dc pulse-pair source with the source resistance in series with each bias being R . Show that in the small-signal between the values of the two source resistances gives rise to an input offset voltage of approximately $(R/2)/2R$.

P7.57 One approach to "offset cancellation" involves the adjustment of the values of R_{ce1} and R_{ce2} to reduce the differential output voltage to zero when both input terminals are at ground. This offset nulling process can be accomplished by adjusting a potentiometer in the collector circuit, as shown in Fig. P7.57. We wish to find the potentiometer setting, represented by the fraction x , its value requires R_{ce2} in series with R_{ce1} that is required for nulling the output offset voltage that is 10% .

- (a) R_{ce1} being 5% higher than required and R_{ce2} 2% lower than required
- (b) R_{ce1} having an area 1.5% larger than that of R_{ce2}

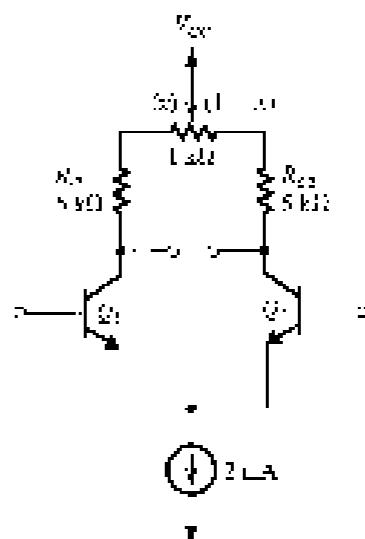


FIGURE P7.57

P7.58 A differential amplifier for which the total emitter bias current is $600 \mu\text{A}$ uses transistors for which β is specified to be between 80 and 200. What is the largest possible input voltage if the smallest possible input bias current is 10% ? The largest possible limit of set current?

*P7.59 A BJT differential amplifier, operating at a bias current of $500 \mu\text{A}$, employs collector resistors of $2 \text{ k}\Omega$ (one-half V_{cc}) assuming a $+1.5 \text{ V}$ supply. The collector current, and the bypassed AC emitter voltage, is 5 V . What is the

positive and negative ends of the input common-mode voltage of the coupled JFET differential signals at $\pm 10\text{ mV}$ peak amplitude, applied in the balanced mode? (Ans.: 1)

- *7.60** In a particular OTI differential amplifier, it is desired to obtain results in one of the transistors having an emitter-base junction area twice that of the other. With both inputs grounded, find the current in each of the two transistors and hence the total output voltage V_o for output, assuming that the collector resistances are unequal. Use small-signal analysis to find the input voltage V_{in} that would restore current balance to the differential pair. Repeat using large-signal analysis and compare results. Also find the input noise and offset currents assuming $I = 0.1\text{ mA}$ and $R_s = 100\text{ k}\Omega$.

7.61 A large fraction of mass-produced differential amplifiers employ 10-k Ω collector resistors to tame the output offset voltage ranging from $\pm 3\text{ mV}$ to $\pm 5\text{ mV}$. If the total dc input differential voltage is 10 mV, by what amount must one collector resistor be adjusted to make the output offset zero? If no adjustment mechanism is desired that raises one collector resistor while lowering the other, what resistance change is needed? Suppose a available circuit using the existing collector resistors and a ground biasing where inverting current I is connected to V_{in} . What value of noninverting resistance (specified to 1 significant digit) is appropriate?

SECTION 7.5: THE DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

- 7.62** In an active-loaded differential amplifier of the form shown in Fig. 7.38(a), if the transistors are characterized by $\beta'W/L = 1.2\text{ mA/V}^2$ and $V_T = -20\text{ V}$, find the bias current I for which the gain $A_{vD} = 20\text{ dB}$.

7.63 Consider an active-loaded differential amplifier such as that shown in Fig. 7.38(b) with the bias current source implemented with the modified Wilson mirror of Fig. P7.62 with $I = 100\text{ nA}$. The transistors have $V_T = 0.1\text{ V}$ and $\beta'W/L = 500\text{ }\mu\text{A/V}^2$. What is the largest value of the total power supply ($V_{DD} + V_{SS}$) that allows both transistors to operate with $|V_{DS}| \geq 2\text{ V}$?

- 7.64** In a version of the active-loaded MOS differential amplifier shown in Fig. 7.39(c), all transistors have $NW/L = 0.2\text{ mA/V}^2$ and $|V_T| = 20\text{ V}$. For $V_{DD} = 2\text{ V}$, with the input bias point at $V_{in} = 100\text{ }\mu\text{V}$ or $I = 100\text{ }\mu\text{A}$, calculate the CMRR values of r_{in} , the r_{oD} of Q_1 and Q_2 , the output resistance of Q_3 and Q_4 , the total output resistance, and the voltage gain.

- 7.65** Consider the active-loaded MOS differential amplifier of Fig. 7.39(d) in two cases:

- (a) The current source I is implemented with a simple constant current.
- (b) The current source I is implemented with the modified Wilson current source shown in Fig. P7.61.

Recalling that for the simple case $r_{in} = r_{oD}$ and for the Wilson current source $r_{in} = g_{m,I}^{-1} \approx r_{oD}$ and assuming that all transistors have the same $|V_T|$ and NW/L , show that for case (a)

$$\text{CMRR} = 2 \frac{|V_{in}|^2}{|V_{in}|^2 + |V_{in}|^2}$$

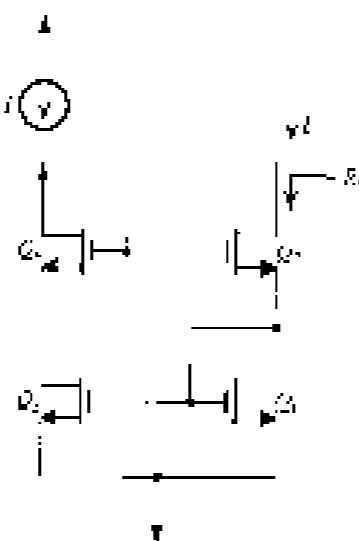


FIGURE P7.64

and for case (b)

$$\text{CMRR} = \sqrt{2} \frac{|V_{in}|^2}{|V_{in}|^2 + |V_{in}|^2}$$

where $|V_{in}|$ is the average dc voltage that corresponds to a drain current of $I/2$. For $NW/L = 1.2\text{ mA/V}^2$, $I = 1\text{ mA}$, and $|V_T| = 20\text{ V}$, find CMRR for both cases.

- *7.66** (a) Sketch the circuit of an active-loaded MOS differential amplifier like — with the input transistors n -channel, and a source current mirror m used for the load. (b) Show that all transistors are connected as an active load, r_{oD} , and have similar drain voltages $|V_{DS}|$; the gain is given by

$$A_{vD} = 2(V_{DD} - V_{SS})/r_{oD}$$

For $|V_{in}| \ll V_{DD}$, the gain for $V_{DD} = 1.25\text{ V}$ is $A_{vD} = 30\text{ V}$.

- 7.67** The differential amplifier in Fig. 7.39(j) is operated with $I = 100\text{ }\mu\text{A}$, with devices for which $V_T = 15\text{ V}$ and $\beta' = 100$. What different r_{in} , load resistance, output resistance, equivalent transconductance, and open-circuit voltage gain would you expect? What will be voltage gain if the input resistance of the subsequent stage is 100 k Ω ?

- *7.68** Design the circuit of Fig. 7.39(m) using a basic current mirror to implement the current source I . It is required that the

equivalent transconductance be 5 mA/V, the DC power supplies and bias current levels $I = 150$ and $V_T = 100\text{ V}$, and the complete circuit, using these values, and specify the DC biasing voltage V_B , the output resistance R_o , the open-circuit voltage gain A_{vD} , the input bias current I_{BIAS} , the common-mode rejection ratio, and the current I_{Q1} (base).

- *7.69** Repeat the design of the amplifier specified in Problem 7.68, using a Wilson current source (Fig. 6.52) to supply the bias current. Assume that the largest resistance available is 2 M Ω .

- 7.70** Modify the design of the amplifier in Problem 7.68 by connecting emitter degeneration resistors of values that result in $R_o = 100\text{ k}\Omega$. What does A_{vD} become?

7.71 An active-loaded bipolar differential amplifier such as that shown in Fig. 7.32(a) is at 3.3 mA, $V_T = 120\text{ mV}$, and $\beta = 100$. The Q_1 , Q_2 , Q_3 , and Q_4 in the differential source is implemented with a suitable low-current source. Let A_{vD} be the CMRR. If the input terminals differentially with a source having a load of 10 k Ω resistors ($\pm 5\text{ k}\Omega$ in series with the base end of each of Q_1 and Q_2), find the overall differential voltage A_{vD} .

- 7.72** Consider the differential amplifier circuit of Fig. 7.39(m) with the two input terminals tied together and an input common-mode signal V_{in} applied. Let the output resistance r_{oD} of this current source be denoted by R_{in} , and let the r_{in} of the input resistors be denoted by r_{in} . Assuming that $r_{in} \gg r_{oD}$, the two transistors Q_1 and Q_2 are the current mirror output of the inverter. Then, show that the common-mode transconductance is $g_{m,Q_1} + g_{m,Q_2}$. Use this result to find the differential conductance r_{oD} (derived in the text) to an alternative measure of the common-mode rejection. Observe that this result differs from the CMRR expression in Eq. (7.17) by a factor of 2, which is simply the ratio of the output resistance to common-mode inputs (r_{oD}) and the output resistance for differential inputs ($r_{oD}/2$).

- 7.73** Repeat Problem 7.72 for the case in which the current mirror is replaced with a Wilson mirror. Show that in this case the output current will be $I_{Q1} = I_{Q2} = I$, and the common-mode input voltage is the ratio r_{in}/r_{oD} .

- 7.74** Figure P7.71 shows a commercial运放 (op-amp) with an active load formed by a Wilson current mirror. Unlike the configurations described in Chapter 6 for the output resistance of a BJT op-amp and the output resistance of the Wilson mirror, and assuming all transistors to be identical, note that the differential voltage gain A_{vD} is given by

$$A_{vD} = \frac{1}{2} \frac{R_o}{r_{in}} I$$

Evaluate A_{vD} for the case $I = 0.4\text{ mA}$, $\beta = 100$, and $V_T = 125\text{ mV}$.

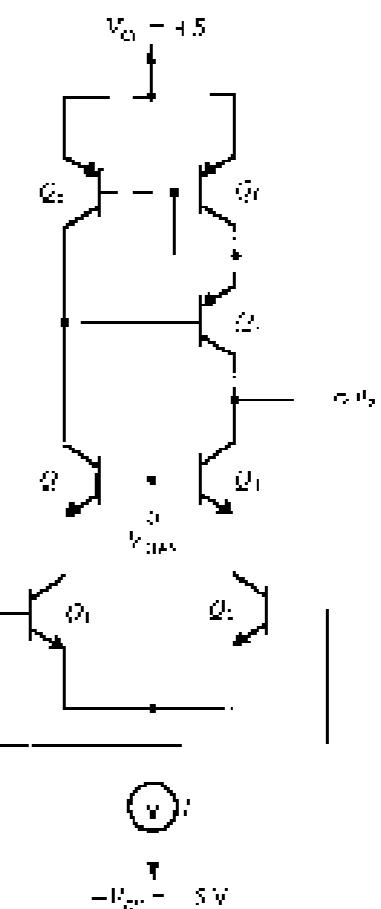


FIGURE P7.74

- 7.75** Consider the bias design of the Wilson loaded cascode JFET op-amp shown in Fig. P7.72.

- (a) What is the largest signal voltage possible at the output without clipping? Assume that the CR junction conductance when the voltage across it exceeds 0.1 V.
- (b) What should the bias voltage established at the output be in arrangement (a) be in order to allow for rail-to-rail output swing of 1.5 V?
- (c) What should the value of V_{DD} be in order to allow for rail-to-rail output swing of 1.5 V?

- (d) What is the upper limit on the input common-mode voltage V_{in} ?

- 7.76** Figure P7.76 shows a typical active-load differential amplifier. Here Q_1 and Q_2 are the cascade transistors. However, we assume in which Q_1 is connected with its base current feeding the common-emitter Q_2 . This results in very interesting input properties. Note that for simplicity the circuit is shown with the base of Q_2 grounded.

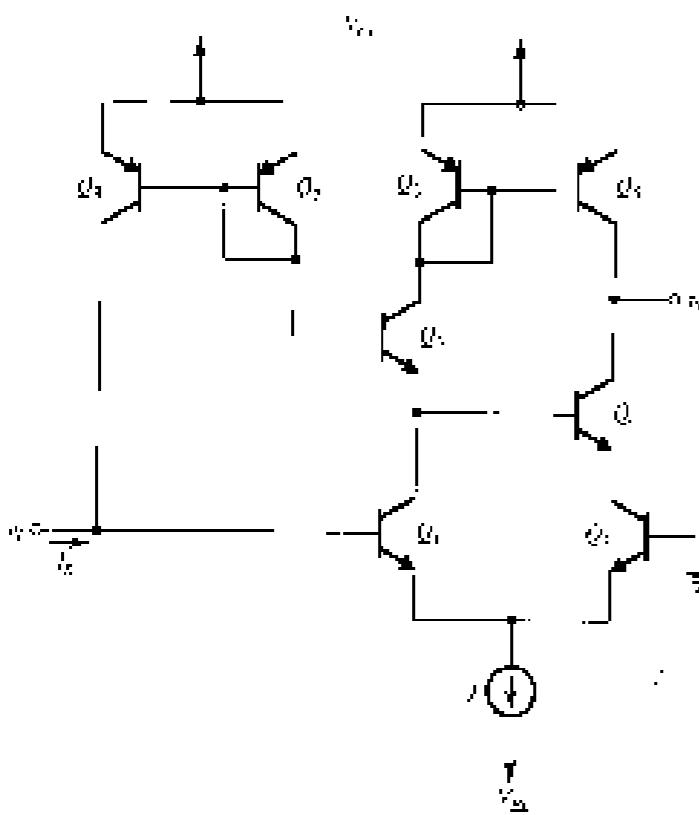


FIGURE P7.76

(a) With $v_s = 0$ V dc, find the total bias current I_B assuming all transistors have equal value of 0. Compare the case with out the Q_3 - Q_4 connection.

(b) With $v_s = 0$ V ($V_D - v_{SD}$), find the input signal current i_s and hence the differential resistance R_{ds} . Compare with the case without the Q_3 - Q_4 connection. (Observe that Q_4 requires that the emitter currents of Q_1 and Q_2 are very nearly the same.)

7.77 Utilizing the expression for the current transfer ratio at the Wilson model derived in Section 6.1.3.3 (Eq. 6.193) derive an expression for the systematic offset voltage of a GTR differential amplifier that utilizes a \pm Wilson current mirror load. Evaluate V_{os} for $f_L = 50$.

7.78 For the folded-cascode differential amplifier of Fig. 7.45, find the value of V_{os} that results in the largest possible gain of g_m swing, while keeping Q_3 , Q_4 , and the p-n junction source, the neutralization source out of saturation. Assume $V_{os} = V_{os}^* = 5$ V. If the dc level at the output is 0 V, find the maximum allowable output signal swing. For $I = 0.4$ mA, $R_S = 50$, $\beta_1 = 100$, and $V_2 = 120$ V. Let G_m , R_{ds} , R_{in} , V_{os} , and A_{os} .

7.79 For the BiCMOS differential amplifier in Fig. P7.79 let $V_{DD} = V_{SS} = 3$ V, $I = 0.4$ mA, $A_{os}W/L = 5.4$ mA/V², V_A

for p-channel MOSFETs ($V_{DD} = 10$ V, V_A for n-pn transistors is 120 V). Find C_{os} , R_{in} , and A_{os} .

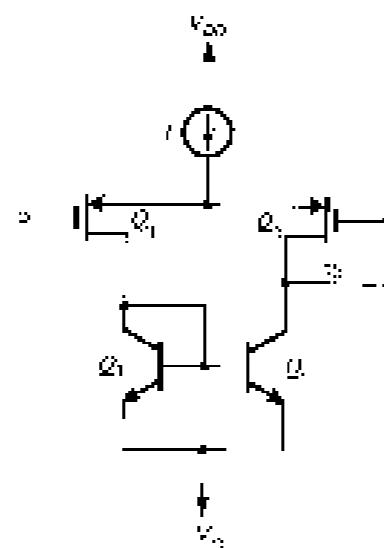


FIGURE P7.79

SECTION 7.6: FREQUENCY RESPONSE OF THE DIFFERENTIAL AMPLIFIER

7.80 A MOSFET differential amplifier such as the one shown in Fig. 7.36(a) is biased with a current source $I = 200$ μ A. The transistors have $100V_A = 25$, $K_n = 128 \mu A/V^2$, $V_T = 20$ mV, $C_{os} = 30$ fF, $C_{gs} = 5$ fF, and $C_{gd} = 5$ fF. The drain resistances are 20 k Ω each. There is a 10-k Ω capacitive load between each drain and ground.

- Find V_{os} and A_{os} for each transistor.
- Find the differential-mode gain A_{os} .
- If the input signal source has a small resistance R_{in} , and thus the frequency response is determined primarily by the output pole, estimate the 3-dB frequency f_L .
- In a different situation, the amplifier is fed symmetrically with a signal source of 40 k Ω resistance ($r_s = 20$ k Ω in series with each gate terminal). Use the open-circuit time constants method to estimate f_L .

7.81 The amplifier specified in Problem 7.80 has $R_{os} = 100$ k Ω and $C_{os} = 0.2$ pF. Find the 3-dB frequency of the CMRR.

7.82 A JFET differential amplifier operating with a 1-mA current source uses transistors for which $\theta = 100$, $I_D = 600$ mV, $C_{os} = 0.5$ pF, and $r_s = 100$ Ω . Each of the collector resistances is 10 k Ω , and C_{gd} is very large. The amplifier is fed in a symmetrical fashion with a source resistance of 10 k Ω in series with each of the two input terminals.

- Sketch the differential-mode small-signal and its high-frequency equivalent circuit.
- Determine the low-frequency value of the overall differential-mode gain A_{os} .
- Use Miller's theorem to determine the input capacitive load and hence estimate the 3-dB frequency f_L and the pole-bandwidth product.

7.83 The differential amplifier circuit specified in Problem 7.82 is modified by including a 10-k Ω resistor in each of the emitters. Determine the low-frequency value of the overall differential-mode voltage gain. Also, use the method of open-circuit time constants to obtain an estimate for f_L . (Hint: In the end, note that the resistance R_E seen by C_{os} is given by

$$R_E = [(\theta + r_s)(R_E + R_{in})] / (1 + C_{os}R_E) + R_{in},$$

where

$$R_E = (\theta + 1)(R_E + r_s)$$

$$C_{os} = \frac{R_E}{1 + \theta R_E}.$$

The resistance R_E seen by C_{os} is given by

$$R_E = r_s + \frac{R_E(\theta + r_s + R_{in})}{1 + C_{os}R_E}.$$

Also determine the pole-bandwidth product.

7.84 It is required to increase the 3-dB frequency of the differential amplifier specified in Problem 7.82 to 1 MHz by adding an emitter resistance R_E . Use the open-circuit time constants method to perform this design. Specifically, use the Jacobian of R_E and R_{in} given in the statement for Problem 7.82 to determine the required value of the factor $(1 + \theta R_E)$ and hence find R_E . Make appropriate approximations to simplify the calculations. What does the dc gain become? Also determine the resulting gain-bandwidth product.

7.85 A current-inverter-loaded MOS differential amplifier is biased with a current source $I = 0.6$ mA. The two NMOS transistors of the differential pair are operating at $V_{DD} = 0.3$ V, and the PMOS devices of the inverter are operating at $V_{DD} = 0.5$ V. The drain voltage $V_{DD} = V_{SS} = 9$ V. The total capacitance to the input node of the inverter is 0.1 pF and that at the output node of the amplifier is 0.2 pF. Find the dc value and the frequencies of the poles and zeros of the differential voltage gain.

7.86 A differential amplifier is biased by a current source having an output resistance of 1 M Ω and an output capacitance of 10 pF. The differential gain exhibits a dominant pole at 500 kHz. What are the poles of the CMRR?

7.87 For the differential amplifier specified in Problem 7.82, find the dc gain and f_L when the circuit is modified by eliminating the collector resistance of the left-hand-side transistor and the input signal is fed to the base of the right-hand-side transistor while the base of the other transistor in the pair is grounded. Turn the source resistance by 20 k Ω and neglect r_s (Refer to Fig. 4.57.)

7.88 Consider the circuit of Fig. P7.88 for the case: $I = 300$ μ A and $V_{DD} = 0.3$ V, $R_{in} = 200$ k Ω , $R_E = 10$ k Ω , $C_{os} = C_{gs} = 1$ pF. Find the dc gain, the high-frequency poles, and an estimate of f_L .

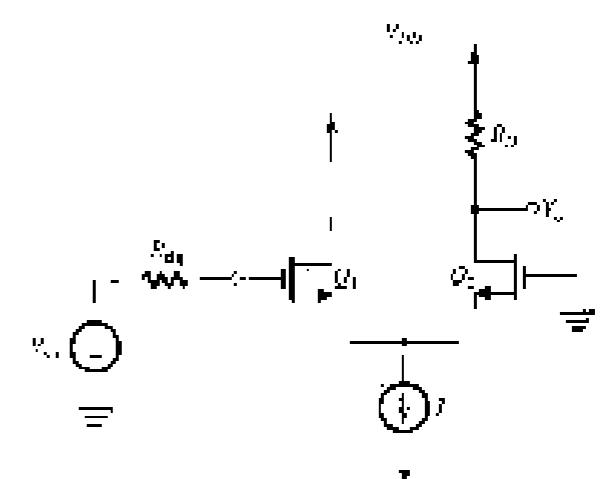


FIGURE P7.88

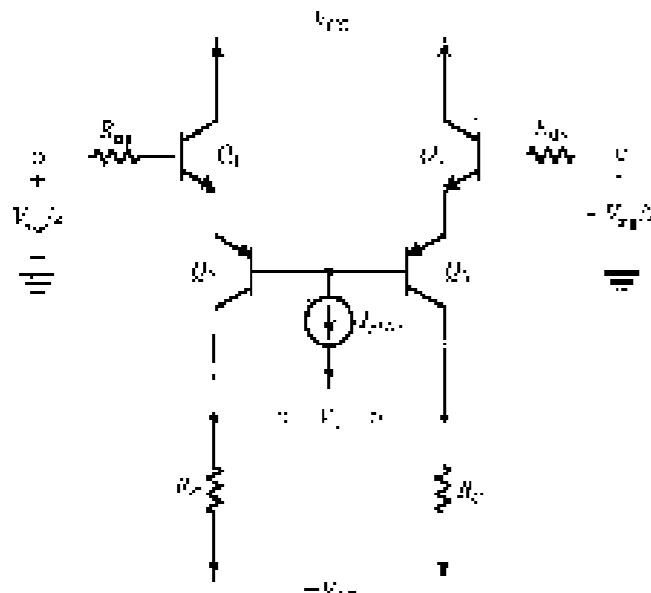


FIGURE P7.89

P7.89 For the circuit in Fig. P7.89, let the bias be such that each transistor is operating at 100 μ A collector current (i.e., the HFEs are $\beta = 200$, $V_A = 3.0$ Vdc, and $r_{ce} = 0.2 \text{ k}\Omega$), and neglect V_{BE} and V_{CE} . Also, $R_{in} = R_{c1} = 50 \text{ k}\Omega$. Find the low-frequency gain, the input differential voltage, the high-frequency poles, and the output voltage.

SECTION 7.7: MULTISTAGE AMPLIFIERS

P7.90 Consider the circuit in Fig. 7.40 with the device parameters (in μ A) shown in the legend of this page.

(a) If $I_{B1} = 125 \mu\text{A}$, $V_A = 0.75 \text{ V}$ for all devices, $\beta C_1 = 180 \mu\text{A}/\text{V}^2$, $\mu C_1 = 60 \mu\text{A}/\text{V}^2$, $|V_A| = 9 \text{ V}$ for all devices, $V_{BE1} = V_{BE2} = 1.5 \text{ V}$. Determine the width of Q_3 , W_3 , that will ensure that the op amp will not have a systematic offset voltage. Hint: Set $V_{out} = 0$ and solve for V_{BE1} , V_{BE2} , V_{c1} , and V_{c2} . Review your results in a table similar to Table 7.1. Also find A_{v1} , A_{v2} , the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on the bias current.

P7.91 In a particular design of the CMOS op-amp of Fig. 7.40, the currents widths are unequal. Show that the two sides of the input stage are perfectly matched if and the threshold voltages of Q_3 and Q_4 have a mismatch of 4 mV . Show

Transistor	I_B	β	μ	V_A	r_{ce}
Q_1	100	200	100	9	0.2
Q_2	100	200	100	9	0.2
Q_3	100	200	100	9	0.2
Q_4	100	200	100	9	0.2

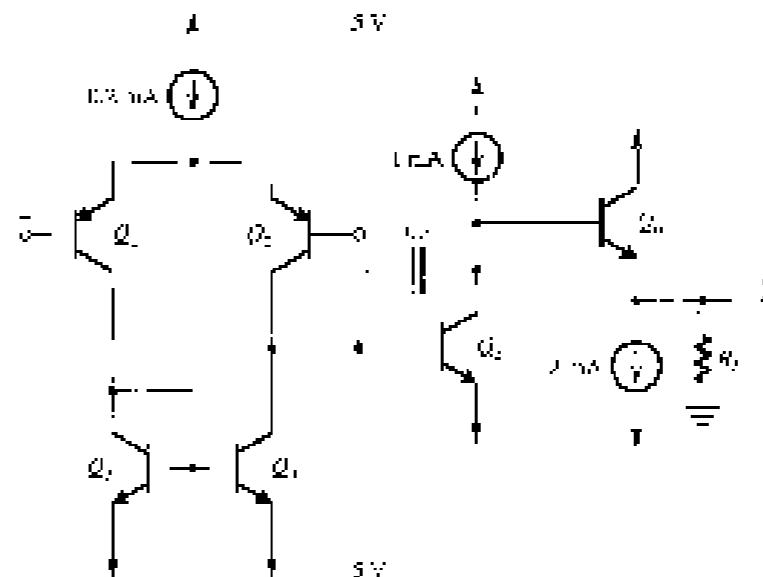


FIGURE P7.95

the resulting gain, appears in the output of the first stage. What is the corresponding input offset voltage before this after setting for the current specified in Example 7.3 for $V_A = 9 \text{ V}$? (Use the results of example 7.3.)

P7.94 A CMOS op-amp with the topology in Fig. 7.40 has $V_A = -100 \text{ V}$, $\mu C_1 = 2 \text{ mA/V}$, the net capacitance between node D and node E is 0.2 pF , and the drain-to-source resistance between the output node and ground is $5 \text{ M}\Omega$. Find the value of C_{FB} that results in $f_T = 10 \text{ MHz}$ and verify that it is lower than $10 \text{ f}\omega_T$.

P7.95 Figure P7.95 shows a basic op-amp circuit that resembles the CMOS op-amp of Fig. 7.40. Here, the ± 100 differential pair Q_1 , Q_2 is biased in a current mirror formed by Q_3 and Q_4 . The current mirror is formed by the current source located between the bases of Q_3 and Q_4 . The CMOS circuit, however, is an output stage formed by the common-emitter stage Q_5 , Q_6 . Capacitor C_E is placed in the negative feedback path of Q_6 , and thus it is transconductanced by the gain of Q_6 . The resulting large capacitive load is dominant at low frequency, but C_E thus provides the required unity-gain bandwidth around 10 Hz . Transistors have $\beta = 100$, $|V_A| = 0.75 \text{ V}$, and $r_{ce} = 0.2 \text{ k}\Omega$.

(a) For $V_{in} = 0$ and $V_{out} = 0$ (no offset voltage), find the output voltage of the first stage.

(b) Calculate the dc gain of the amplifier with $R = 10 \text{ k}\Omega$.

(c) With $R = 10 \text{ k}\Omega$, find the value of C_E at about a 100

frequency of 100 Hz. What is the value of C_E that results?

P7.96 It is required to bias the circuit of Fig. 7.42 to get a bias current $I_B = 25 \mu\text{A}$ with Q_1 and Q_2 as matched devices having $W/L = 600/5$. The biasing Q₃, Q₄, and Q₅

are to be identical and must have the same μ as Q_1 and Q_2 . Let $V_B = 3V$, $V_{DD} = 180 \mu\text{A}/\text{V}^2$, and $V_{SS} = V_{BE} = 1.5 \text{ V}$. Find the required value of R_B . What is the voltage drop across R_B ? Also specify the bias ratios of Q_1 , Q_2 , Q_3 , and Q_4 and give the expected dc voltages at the gates of Q_1 , Q_2 , and Q_3 .

P7.97 A BJT differential amplifier circuit is to have $r_{ce} = 100 \text{ M}\Omega$ and driving two $100 \text{ }\mu\text{A}$ emitter resistors and $2\text{-}\mu\text{A}$ loads, with a second differential stage biased to have $r_{ce} = 20 \text{ M}\Omega$. All BJTs have $f_T = 100 \text{ Hz}$. What is the voltage gain of the first stage? Also find the input resistance of the first stage and the overall gain of the second stage.

P7.98 In the ± 100 -stage amplifier of Fig. 7.43, consider the case to be unbalanced— $10 \text{ }\mu\text{A}$ in the emitter lead of each of the first-stage ± 100 stages and $2\text{-}\mu\text{A}$ in each of the second-stage transistors. What is the effect of r_{ce} on r_{in} , the voltage gain of the first stage, and the overall voltage gain? Use the bias values found in Example 7.4.

P7.99 Consider the circuit of Fig. 7.43 and its input resistance r_{in} with resistor R_1 as the model. Set the output resistance r_{out} to be zero. Should this resistor be changed so the output resistance r_{out} is to be reduced by a factor of 2π ? What will the amplifier gain become after this change? What extra change can you make to restore the amplifier gain to approximately its prior value?

P7.100 (a) If, in the multistage amplifier of Fig. 7.43, the resistor R_2 is replaced by a constant current source of $-10 \text{ }\mu\text{A}$, such that the bias condition is essentially unaffected, what does the overall voltage gain of the amplifier become?

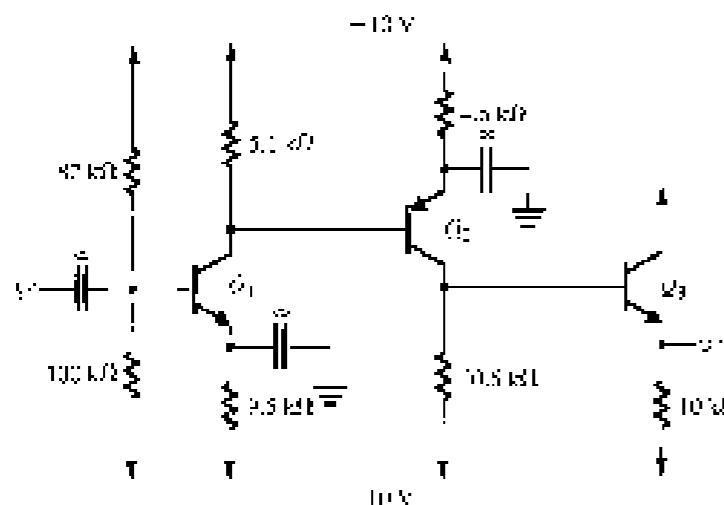


FIGURE P7.101

Assume that the output resistance of the current source is very high. Use the results of Example 7.5.

- (a) When the load is a voltage source, what is the effect of the change in output resistance? What is the overall gain of the amplifier when loaded by $10\text{ k}\Omega$ to ground? The original amplifier (before modification) has an output resistance of $1.18\text{ k}\Omega$ and a voltage gain of 481.9 . What is its gain when loaded by $10\text{ k}\Omega$? (Ans. 466.4, for $\beta = 10$)

*7.101. Figure P7.101 shows a three-stage amplifier in which the stages are directly coupled. The gain, however, utilizes input capacitors, and so such an amplifier response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to be as passive short circuits at all signal frequencies of interest.

- (a) Find the drain current in each of the three transistors. Also find the drain voltage at the output, V_{D2} , if $V_{DD} = 0.7\text{ V}$, $\beta = 100$, and neglect Early effect.

(b) Find the input resistance and the output resistance.

- (c) Use the current-gain method to evaluate the voltage gain A_{vD} .

(d) Find the frequency of the low-frequency pole located at the junction between the first and the second stages. Assume that $C_{12} = 2\text{ pF}$ and $C_{23} = 1.5\text{ pF}$.

- *7.102. For the circuit shown in Fig. P7.102, which uses a load electrode having a transconductance g_m , all nonlinearities are zero, $V_{DD} = 0.7\text{ V}$ for the n -channel devices, $V_A = 100\text{ V}$, and $\beta = 100$. Use a more or less conventional excess factor G_m , which appears in a Class B mode (we will study this in Chapter 12) to provide an increased negative current swing for an n -channel device.

- (a) Perform a bias analysis assuming $|V_{GS1}| = 0.7\text{ V}$, right β , $V_{GS2} = 0$, $v_1 = v_2 = 0\text{ V}$, and v_3 is stabilized by feedback to

about 0.7 V . Find N so that the reference current I_{DSR} is $100\text{ }\mu\text{A}$. What is the voltage v_3 at the bias point?

- (b) Show that the bias currents in the transistors, together with v_1 and v_2 , let the signal transistors (Q_1 , Q_2 , Q_3 , and Q_4) and v_3 for Q_5 , Q_6 , and Q_7 .

(c) Now, using $\beta = 100$, find the voltage gain A_{vD} and v_3 to the previous, verify v_3 voltage at the output terminals.

- (d) Find the input and output resistances.

(e) Find the load resistance-load range for linear operation.

- (f) For now, what is the range of available output voltages assuming $V_{DD} = 0.7\text{ V}$?

(g) Now consider the situation with a load resistance connected to the output. If $v_3 = 4\text{ V}$, prior work suggests that the output signal swing, and the smallest load resistance that can be driven if one of the either of Q_5 or Q_7 is allowed to cutoff.

- D*7.103. In the CMOS op amp shown in Fig. P7.103, all MOS devices have $|V_t| = 1\text{ V}$, $\mu_C = 2\text{ pA/V}^2$, $|V_A| = 50\text{ V}$, and $L = 5\text{ }\mu\text{m}$. Device widths are indicated on the diagram as multiples of W , where $W = 5\text{ }\mu\text{m}$.

(a) Design it to provide a 10-MHz reference current.

- (b) Assuming $v_2 = 0\text{ V}$, as established by external feedback, perform a bias analysis, finding all the inherent node voltages, V_{GS1} and I_{DS1} to all nodes.

(c) Provide it with four load I_{DS} , V_{GS} , g_m , and v_3 for all devices.

- (d) Calculate the voltage gain A_{vD} , R_{in} , the input resistance, and the output resistance.

(e) What is the input bias, voltage-biased input?

- (f) What is the output signal range for no load?

(g) For what load resistance connected to ground is the output negative voltage limited to -1 V before Q_1 begins to conduct?

- (h) For a load resistance one tenth of that found in (g), what is the output signal swing?

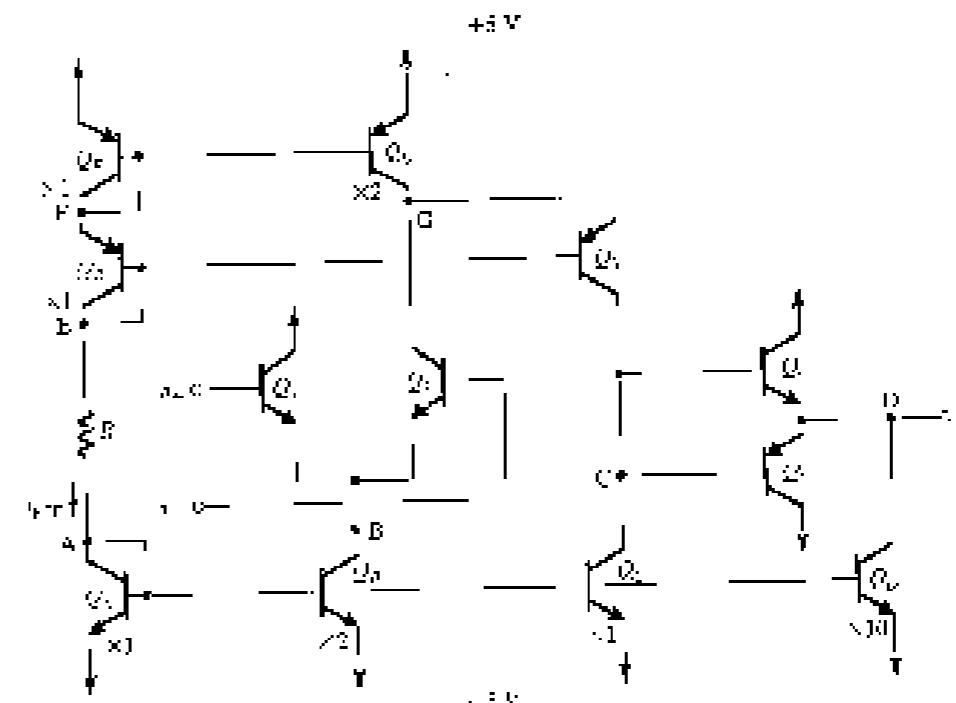


FIGURE P7.102

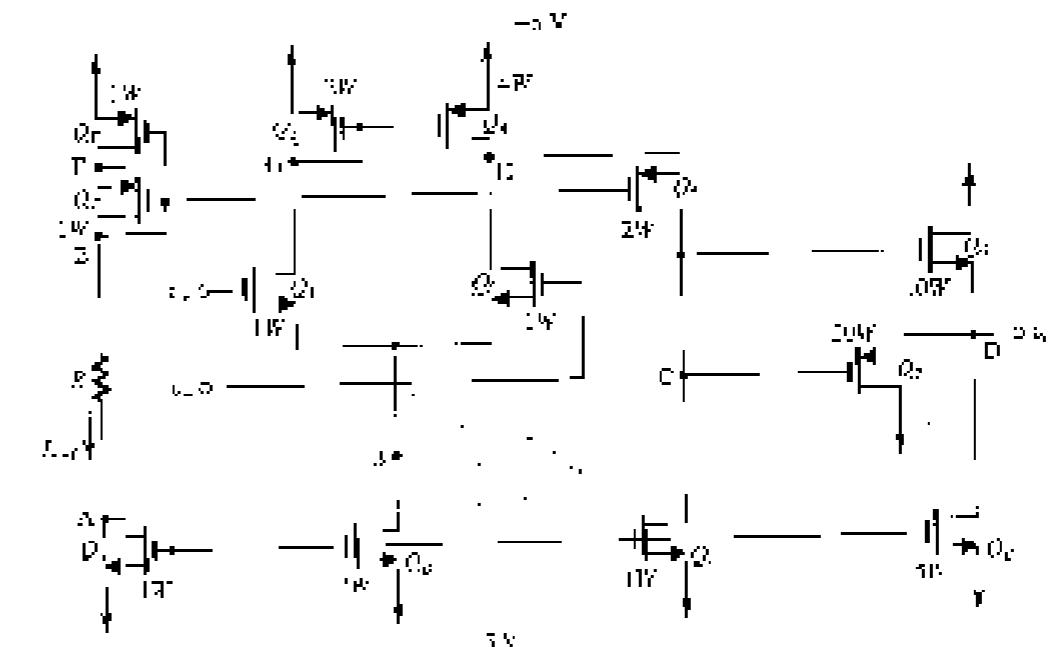


FIGURE P7.103

CHAPTER 8

Feedback

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INTRODUCTION

Most physical systems incorporate some form of feedback. It is interesting to note, though, that the theory of negative feedback has been developed by electronics engineers. In his search for methods for the design of amplifiers with stable gain, for use in telephone repeaters, Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier in 1926. Since then the technique has been so widely used that it is almost impossible to think of electronic circuits without some form of feedback, either implicit or explicit. Furthermore, the concept of feedback and its associated theory are currently used in areas other than engineering, such as in the modeling of biological systems.

Feedback can be either negative (degenerative) or positive (regenerative). In a negative design, negative feedback is applied to effect one or more of the following properties:

1. *Desensitize the gain*: that is, make the value of the gain less sensitive to variations in the value of circuit components, such as might be caused by changes in temperature.
2. *Reduce nonlinear distortion*: that is, make the gain proportional to the input (in other words, make the gain constant, independent of signal level).
3. *Reduce the effect of noise*: that is, minimize the contribution to the output of unwanted electric signals generated either by the circuit components themselves, or by extraneous interference.
4. *Control the input and output impedances*: that is, raise or lower the input and output impedances by the selection of an appropriate feedback topology.
5. *Extend the bandwidth of the amplifier*.

All of the desirable properties above are obtained at the expense of a reduction in gain. It will be shown that the gain factor for the β , called the amount of feedback, is the factor by which the circuit is desensitized, by which the input impedance of a voltage amplifier is increased, by which the bandwidth is extended, and so on. In short, the basic idea of negative feedback is to trade off gain for other desirable properties. This chapter is devoted to the study of negative-feedback amplifiers, their analysis, design, and characteristics.

Under certain conditions, the negative feedback in an amplifier can become positive and of such a magnitude as to cause oscillation. In fact, in Chapter 13 we will study the use of positive feedback in the design of oscillators and switch circuits. Here, in this chapter, however, we are interested in the design of stable amplifiers. We shall therefore study the stability problem of negative-feedback amplifiers and their potential for oscillation.

It should not be implied, however, that positive feedback always leads to instability. In fact, positive feedback is quite useful in a number of nonregenerative applications, such as the design of active filters, which are studied in Chapter 12.

Before we begin our study of negative feedback, we wish to remind the reader that we have already encountered negative feedback in a number of applications. Almost all op-amp circuits employ negative feedback. Another popular application of negative feedback is the use of the emitter resistance R_e to stabilize the bias point of bipolar transistors and to increase the input resistance, bandwidth, and linearity of a B.C. amplifier. In addition, the source follower and the Miller follower both employ a large amount of negative feedback. The question then arises about the need for a formal study of negative feedback, as will be appreciated by the end of this chapter, the formal study of feedback provides an invaluable tool for the analysis and design of electronic circuits. Also, the insight gained by thinking in terms of feedback can be extremely profitable.

8.1 THE GENERAL FEEDBACK STRUCTURE

Figure 8.1 shows the basic structure of a feedback amplifier, rather than showing voltages and currents, Fig. 8.1 is a signal-flow diagram, where each of the quantities x can represent either a voltage or a current signal. The open-loop amplifier voltage gain A from its input x_1 is related to the input x_1 by

$$x_2 = A x_1 \quad (8.1)$$

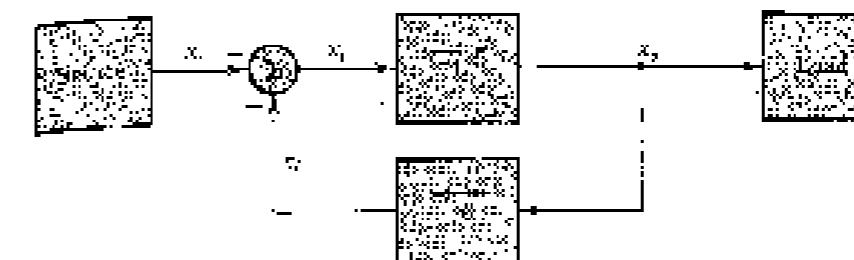


FIGURE 8.1 General structure of the feedback amplifier. This is a signal-flow diagram, and the x 's and B and A are generic symbols for "signals."

The output x_3 is fed to the load as well as to a feedback network, which produces a sample of the output. This sample x_4 is related to x_3 by the feedback factor B :

$$x_4 = B x_3 \quad (8.2)$$

The feedback signal x_4 is subtracted from the source signal x_1 , which is the input to the complete feedback amplifier,¹ to produce the signal x_5 , which is the input to the basic amplifier.

$$x_5 = x_1 - x_4 \quad (8.3)$$

Here we note that it is this subtraction that makes the feedback negative. In essence, negative feedback reduces the signal that appears at the input of the basic amplifier.

In brief, in the description above is that the source, the load, and the feedback network do not load the basic amplifier. That is, the gain A does not depend on any of these three networks. In practice this will not be the case, and we shall have to find a method for casting a real circuit into the ideal structure depicted in Fig. 8.1. Figure 8.1 also implies that the forward transmission occurs entirely through the basic amplifier and the reverse transmission occurs entirely through the feedback network.

The gain of the feedback amplifier can be obtained by combining Eqs. (8.1) through (8.3):

$$A_f = \frac{x_4}{x_1} = \frac{B}{1 + AB} \quad (\text{that})$$

The quantity AB is called the loop gain, a name that follows from Fig. 8.1. For the feedback to be negative, the loop gain AB should be positive; that is, the feedback signal x_4 should have the same sign as x_3 , thus resulting in a smaller difference signal x_5 . Equation (8.4) indicates that for positive AB the gain-with-feedback A_f will be smaller than the open-loop gain A by the quantity $1 + AB$, which is called the *amount of feedback*.

If, as is the case in many circuits, the loop gain AB is large, $AB \gg 1$, then from Eq. (8.4) it follows that $A_f = 1/AB$, which is a very interesting result: *The gain of the feedback amplifier is absolutely determined by the feedback network.* Since the feedback network usually consists of passive components, which usually can be chosen to be as accurate as one wishes, the advantage of negative feedback in obtaining accurate, predictable, and stable

¹ In earlier chapters, we used the subscript "wg" for quantities associated with the signal source, that is, x_{1w} and x_{4w} . We had that to avoid confusion with the subscript "g," which is usually used with PCTs. It seems quite reasonable with the course content of this chapter. At this point, however, it is suggested that readers have some settling early familiarity with this distinction, that the possibility of confusion is minimal. Therefore, we will now be using the simpler subscript "1" for right-source quantities.

gain should be apparent. In other words, the overall gain will have very little dependence on the gain of the basic amplifier, A_0 , inevitable property because the gain A is usually a function of many manufacturing and application parameters, some of which might have wide tolerances. We have seen a dramatic illustration of all of these effects in op-amp circuits, where the closed-loop gain (which is another name for the gain-with-feedback) is almost entirely determined by the feedback elements.

Equations (8.1) through (8.3) can be combined to obtain the following expression for the feedback signal x_f :

$$x_f = \frac{A\beta}{A + \beta} x_i \quad (8.5)$$

Thus, for $A\beta \gg 1$, we see that $x_f \approx x_i$, which implies that the signal at the input of the basic amplifier is reduced to almost zero. Thus if a large amount of negative feedback is employed, the feedback signal x_f becomes an almost identical replica of the input signal x_i . An outcome of this property is the tracking of the two output terminals of an op-amp. The difference between x_{o1} and x_{o2} , which is x_o , is sometimes referred to as the "error signal." Accordingly, the input differencing circuit often also called a comparitor circuit (it is also known as a mixer). An expression for x_o can be easily determined as

$$x_o = \frac{1}{1 + A\beta} x_i \quad (8.6)$$

from which we can verify that for $A\beta \gg 1$, x_o becomes very small. Observe that negative feedback reduces the signal that appears at the output terminals of the basic amplifier by the amount of feedback, $(1 + A\beta)x_i$.

EXERCISE

The differential voltage-controlled voltage source shown in Fig. 8.1-1 provides a direct implementation of the feedback loop of Fig. 8.1. Suppose that the open-loop gain of the basic amplifier is $A_0 = 10^4$ and $\beta = 0.99$. To obtain a closed-loop gain of $A = 10^3$, what is the required value of feedback? What is the corresponding value of β ?



FIGURE 8.1-1

8.2 SOME PROPERTIES OF NEGATIVE FEEDBACK

Key

The properties of negative feedback were mentioned in the Introduction. In the following, we shall examine some of these properties in more detail.

8.2.1 Gain Desensitivity

The effect of negative feedback on desensitizing the closed-loop gain was demonstrated in Example 8.1, where we saw that a 20% reduction in the gain A of the basic amplifier gave rise to only a 0.72% reduction in the gain of the closed-loop amplifier. This sensitivity reduction property can be analytically established as follows:

Assume that β is constant. Taking differentials of both sides of Eq. (8.4) results in

$$\frac{dA_f}{A_f} = \frac{dA}{(1 + A\beta)^2} \quad (8.7)$$

Dividing Eq. (8.7) by Eq. (8.4) yields

$$\frac{dA_f}{A_f} = \frac{1}{(1 + A\beta)} \frac{dA}{A} \quad (8.8)$$

which says that the percentage change in A_f due to variations in some circuit parameter is small for less than 100% feedback. For this reason the amount of feedback, $1 + A\beta$, is also known as the desensitivity factor.

8.2.2 Bandwidth Extension

Consider an amplifier whose high-frequency response is characterized by a single pole. Its gain at low and high frequencies can be expressed as

$$A(\omega) = \frac{A_M}{1 + \omega/\omega_h} \quad (8.9)$$

where A_M denotes the midband gain and ω_h is the upper 3-dB frequency. Application of negative feedback, with a frequency-independent factor β , around this amplifier results in a closed-loop gain $A_f(\omega)$ given by

$$A_f(\omega) = \frac{A(\omega)}{1 + \beta A(\omega)}$$

Substituting for $A(\omega)$ from Eq. (8.9) results after a little manipulation to

$$A_f(\omega) = \frac{A_M/(1 + A_M\beta)}{1 + \omega/\omega_h(1 + A_M\beta)} \quad (8.10)$$

Thus the feedback amplifier ψ has a midband gain of $A_M/(1 + A_M\beta)$ and an upper 3-dB frequency ω_{hf} given by

$$\omega_{hf} = \omega_h(1 + A_M\beta) \quad (8.11)$$

It follows that the upper 3-dB frequency is increased by a factor equal to the amount of feedback.

Similarly, it can be shown that if the open-loop gain is characterized by a dominant low-frequency pole ω_L at a low 3-dB frequency ω_L , then the feedback amplifier will

involves a lower S-CH frequency error.

$$\omega_{ch} = \frac{\omega_0}{1 + A_{ch}\beta} \quad (8.12)$$

Note that the angular bandwidth is increased by the same factor by which its midband gain is decreased, maintaining the gain-bandwidth product at a constant value.

EXERCISE

8.2.1 Consider the circuit in Fig. 8.2(a). If the open-loop gain of the basic amplifier is $A_1 = 10^4$, the feedback factor is $\beta = 0.01$, and the input voltage is $V_i = 1\text{ mV}$, calculate the output voltage V_o . Assume that the noise voltage at the input is $V_n = 1\text{ nV}$.

8.2.3 Noise Reduction

Negative feedback can be employed to reduce the noise or interference in an amplifier or, more precisely, to increase the ratio of signal to noise. However, as we shall now explain, the noise-reduction process is possible only under certain conditions. Consider the situation illustrated in Fig. 8.2. Figure 8.2(a) shows an amplifier with gain A_1 , an input signal V_i , and noise, or interference, V_n . It is assumed that for some reason this amplifier suffers from noise and that the noise can be assumed to be introduced at the input of the amplifier. The

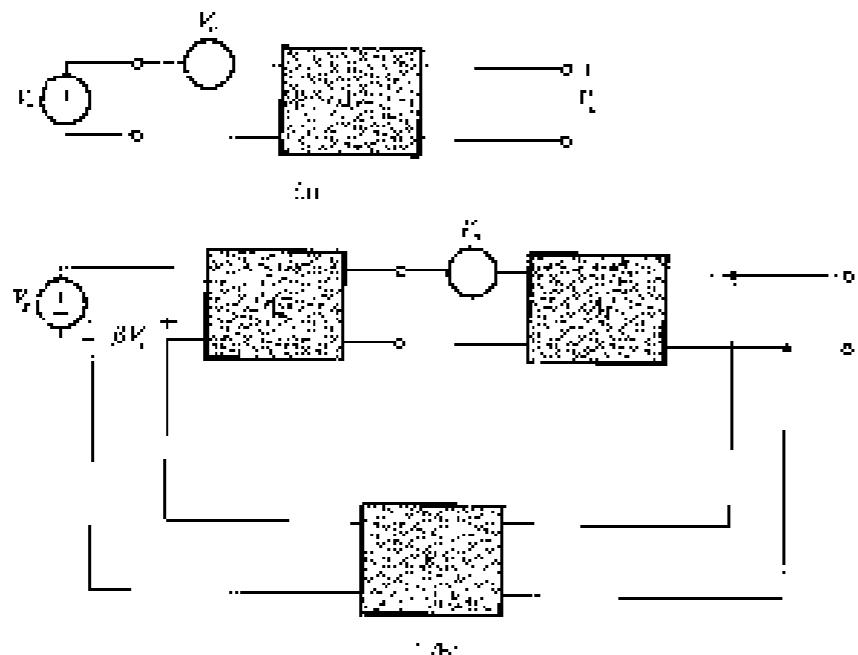


FIGURE 8.2 Illustrating the application of negative feedback to improve the signal-to-noise ratio of an amplifier.

signal-to-noise ratio for this amplifier is

$$S/N = V_o/V_n \quad (8.13)$$

Consider next the circuit in Fig. 8.2(b). Here we assume that it is possible to build another amplifier stage with gain A_2 that does not suffer from the noise problem. If this is the case, then we may precede our original amplifier A_1 by the clean amplifier A_2 and apply negative feedback around the overall cascade of such an amount as to keep the overall gain constant. The output voltage of the circuit in Fig. 8.2(b) can be found by superposition:

$$V_o = V_i \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta} \quad (8.14)$$

Thus the signal-to-noise ratio at the output becomes

$$\frac{S}{N} = \frac{V_o}{V_n} A_2 \quad (8.15)$$

which is A_2 times higher than in the original case.

We emphasize once more that the improvement in signal-to-noise ratio by the application of feedback is possible only if one can precede the noisy stage by a relatively noise-free stage. This situation, however, is not uncommon in practice. The best example is found in the output power-amplifier stage of an audio amplifier. Such a stage usually suffers from a problem known as power-supply hum. The problem arises because of the large currents that this stage draws from the power supply and the difficulty in providing adequate power-supply filtering inexpensively. The power-output stage is required to provide large power gain but little or no voltage gain. We may therefore precede the power-output stage by a small-signal amplifier that provides large voltage gain and apply a large amount of negative feedback, thus reducing the voltage gain to its original value. Since the small-signal amplifier can be fed from another, less noisy (and hence better regulated) power supply, it will not suffer from the hum problem. The hum at the output will then be reduced by the amount of the voltage gain of this added preamplifier.

EXERCISE

8.3 Consider the system shown in Fig. 8.2(b). An input signal of $V_i = 1\text{ mV}$ and noise $V_n = 1\text{ nV}$ are applied to the inverting input of the first stage. Assume that the output voltage of the first stage is $V_o = 100\text{ mV}$. The inverting input of the second stage is connected to the output of the first stage. The non-inverting input of the second stage is connected to ground. The overall gain of the system is $A = 1000$. Find the output voltage V_o and the signal-to-noise ratio.

8.2.4 Reduction in Nonlinear Distortion

Curve (a) in Fig. 8.3 shows the transfer characteristic of an amplifier. As indicated, the characteristic is piecewise linear, with the voltage gain changing from 1000 to 100 and then to 0. The nonlinear transfer characteristic will result in the amplifier generating a large amount of nonlinear distortion.

The amplifier transfer characteristic can be considerably linearized (i.e., made less nonlinear) through the application of negative feedback. That this is possible should not be too surprising, since we have already seen that negative feedback reduces the dependence of the overall closed-loop amplifier gain on the open-loop gain of the basic amplifier. Thus large

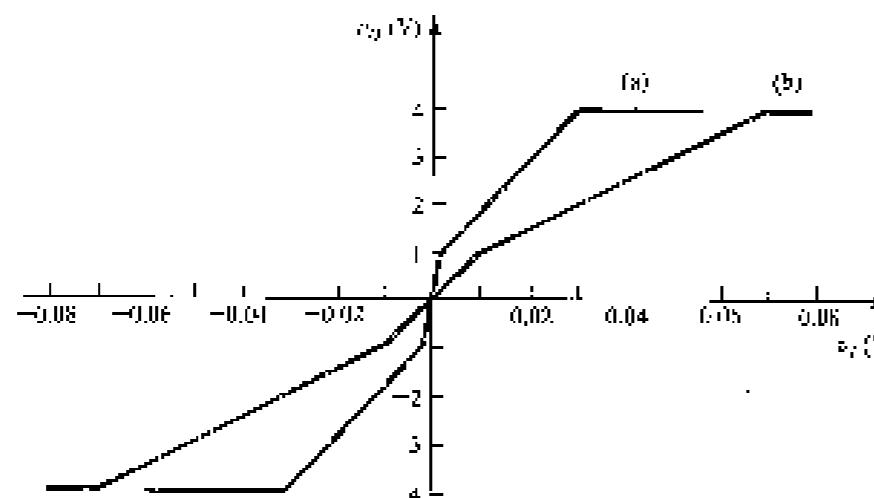


FIGURE 8.3 Illustrating the application of negative feedback to reduce the nonlinearity of voltage amplifiers. Curve (a) shows the amplifier transfer characteristic without feedback. Curves (b) show the characteristic with negative feedback ($\beta = 0.01$) up to $v_i \approx \pm 0.01$ V.

changes in open-loop gain (1000 to 100 in this case) give rise to much smaller corresponding changes in the closed-loop gain.

To illustrate, let's apply negative feedback with $\beta = 0.01$ to the amplifier whose open-loop voltage transfer characteristic is depicted in Fig. 8.3. The resulting transfer characteristic of the closed-loop amplifier is shown in Fig. 8.3 as curve (b). Here the slope of the steepest segment is given by

$$A_{v_f} = -\frac{1000}{1000 + 0.01} = -99.9$$

and the slope of the next segment is given by

$$A_{v_f} = -\frac{100}{1 + 100 + 0.01} = -99$$

Thus the order-of-magnitude change in slope has been considerably reduced. The price paid, of course, is a reduction in voltage gain. Thus if the overall gain has to be restored, then a preamplifier should be added. This preamplifier should not present a severe nonlinear-distortion problem, since it will be dealing with smaller signals.

Finally, it should be noted that negative feedback can do nothing at all about amplifier saturation, since in saturation the input is very small (almost zero) and hence the amount of feedback is also very small (nearly zero).

8.3 THE FOUR BASIC FEEDBACK TOPOLOGIES

Based on the quantity to be amplified (voltage or current) and on the degree form of output feedback (voltage or current), amplifiers can be classified into four categories. These categories were discussed in Chapter 1. In the following, we shall review this amplifier classification and point out the feedback topologies appropriate in each case.

8.3.1 Voltage Amplifiers

Voltage amplifiers are intended to amplify an input voltage signal and provide an output voltage signal. The voltage amplifier is essentially a voltage-controlled voltage source. The input impedance is required to be high, and the output impedance is required to be low. Since the signal source is essentially a voltage source, it is convenient to represent it in terms of a Thévenin equivalent circuit. In a voltage amplifier the output quantity of interest is the output voltage. It follows that the feedback network should sample the output voltage. Also, because of the Thévenin representation of the source, the feedback signal(s) should be a voltage that can be mixed with the source voltage in series.

A suitable feedback topology for the voltage amplifier is the voltage-mixing voltage-sampling one shown in Fig. 8.4(a). Because of the series connection of the input and the parallel or shunt connection of the output, this feedback topology is also known as series-shunt feedback. As will be shown, this topology not only stabilizes the voltage gain but also results in a higher input voltage (naturality), a result of the series connection at the input and a lower output resistance (intuitively, a result of the parallel connection of the output), which are desirable properties for a voltage amplifier. The noninverting op-amp configuration of Fig. 8.4 is an example of series-shunt feedback.

8.3.2 Current Amplifiers

The input signal in a current amplifier is essentially a current, and thus the signal source is most conveniently represented by its Norton equivalent. The output quantity of interest is current, hence the feedback network should sample the output current. The feedback signal should be in current form so that it may be summed with the source current. Thus the feedback topology suitable for a current amplifier is the current-mixing current-sampling topology, illustrated in Fig. 8.4(b). Because of the parallel (or shunt) connection at the input and the series connection at the output, this feedback topology is also known as shunt-series feedback. As will be shown, this topology not only stabilizes the current gain but also results in a lower input resistance and a higher output resistance. Both desirable properties for a current amplifier.

An example of the shunt-series feedback topology is given in Fig. 8.5. Note that the bias details are not shown. Also note that the current being sampled is not the output current, but the equal current flowing from the source of Q_2 . This use of a shunt-gate is done for circuit design convenience and is quite usual in circuits involving current sampling.

The reference direction indicated in Fig. 8.5 for the feedback current i_f is such that it subtracts from i_d . This reference notation will be followed in all circuits in this chapter, since it is consistent with the notation used in the general feedback structure of Fig. 8.1. In all circuits, therefore, for the feedback to be negative, the loop gain $A\beta$ should be positive. The reader is urged to verify, through qualitative analysis, that in the circuit of Fig. 8.5, A is negative and β is negative.

It is of utmost importance to be able to ascertain (qualitatively) from quick β , the feedback polarity (positive or negative). This can be done by "following the signal around the loop." For instance, let the current i_f in Fig. 8.5 increase. We see that the gate voltage of Q_1 will increase, and thus its drain current will also increase. This will cause the drain voltage of Q_2 (and the gate voltage of Q_1) to decrease, and thus the drain current of Q_2 , i_d , will decrease. Thus the source current of (Q_2, i_d) decreases. From the feedback network we see that if i_f increases, then i_d in the direction shown will increase. The increase in i_d will subtract from i_d , causing a small increment to be seen by the amplifier. Hence the feedback is negative.

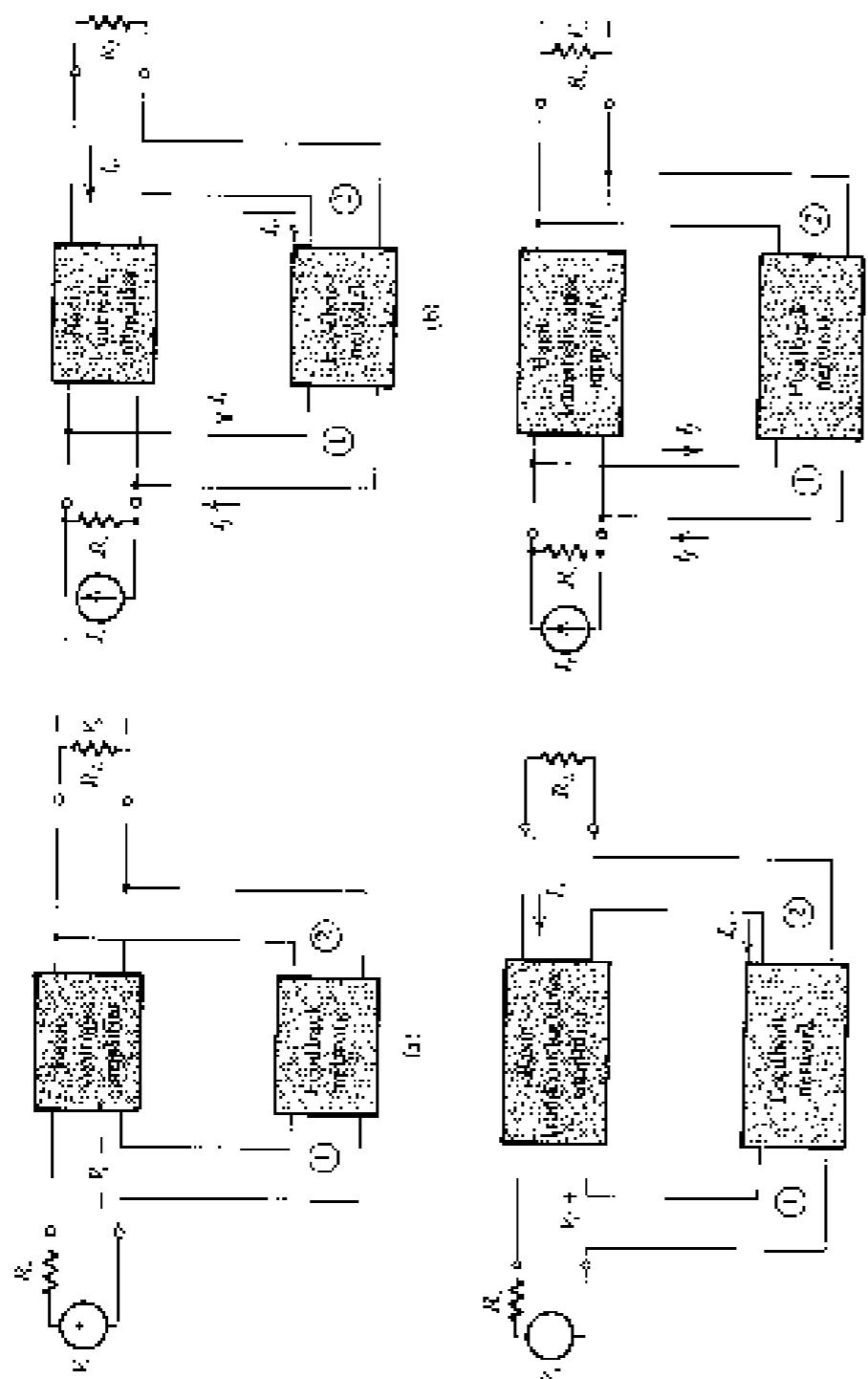


FIGURE 8.4 The four basic feedback topologies: (a) current-mixing voltage-sampling topology; (b) current-mixing current-sampling topology; (c) voltage-mixing current-sampling topology; (d) voltage-mixing voltage-sampling topology.

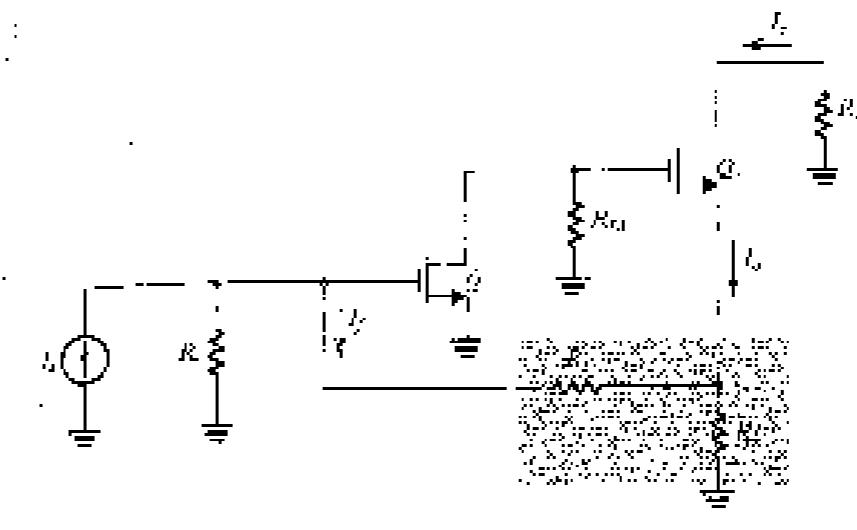


FIGURE 8.5 A complete example of a transconductance amplifier using a current-mixing voltage-sampling topology.

8.3.3 Transconductance Amplifiers

In transconductance amplifiers the input signal is a voltage and the output signal is a current. It follows that the appropriate feedback topology is the voltage-mixing current-sampling topology, illustrated in Fig. 8.4(c). The presence of the series connection at both the input and the output gives this feedback topology the alternative name series-series feedback.

An example of this feedback topology is given in Fig. 8.6. Here, note that as in the circuit of Fig. 8.5 the current sampled is not the output current but the almost equal emitter current of Q_1 . In addition, the mixing loop is not a conventional one; it is not a simple series connection, since the feedback signal developed across R_{B2} is in the emitter circuit of Q_1 , while the source is in the base circuit of Q_1 . These two approximations are done for convenience of circuit design.

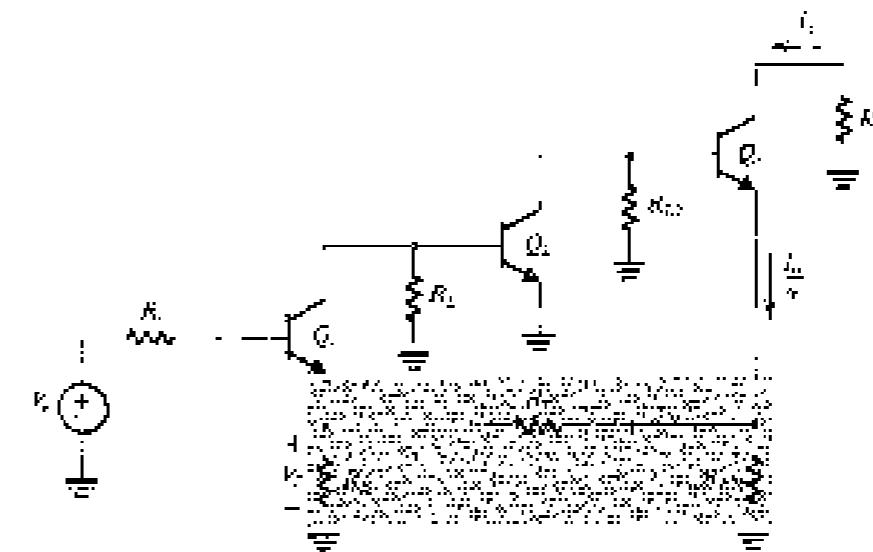


FIGURE 8.6 A complete example of the series-series feedback topology. (Biasing not shown.)

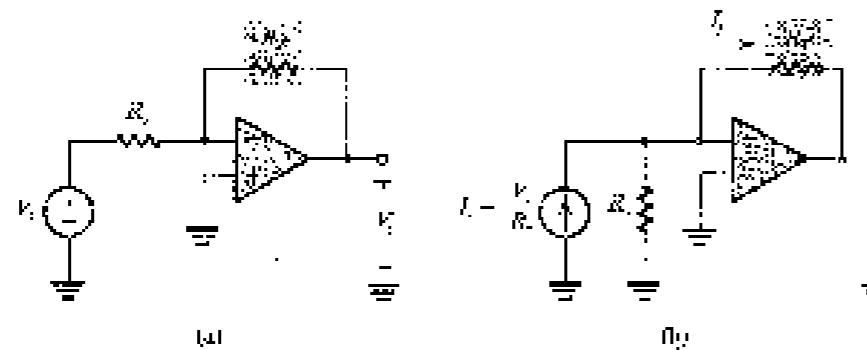


FIGURE 8.7 (a) The inverting op-amp circuit with current feedback; (b) its current feedback model.

8.3.4 Transresistance Amplifiers

In transresistance amplifiers the input signal is current and the output signal is voltage. It follows that the appropriate feedback topology is of the current-feeding voltage-sampling type, shown in Fig. 8.8(a). The presence of the parallel (or shunt) connection at both the input and the output makes this feedback topology also known as shunt-shunt feedback.

An example of this feedback topology is found in the inverting op-amp circuit of Fig. 8.7(b) with the source converted to Norton's form.

8.4 THE SERIES-SHUNT FEEDBACK AMPLIFIER

8.4.1 The Ideal Situation

The ideal structure of the series-shunt feedback amplifier is shown in Fig. 8.8(a). It consists of a unilateral open-loop amplifier (the A circuit) and an ideal voltage-voltage voltage-sampling feedback network (the β circuit). The A circuit has an input resistance R_i , a voltage gain A , and an output resistance R_o . It is assumed that the sources and load resistances have been included inside the A circuit (more on this point later). Furthermore, note that the β circuit does not load the A circuit; that is, connecting the β circuit it does not change the value of A (defined as $A = V_o / V_i$).

The circuit of Fig. 8.8(a) exactly follows the ideal feedback model of Fig. 8.1. Therefore the closed-loop voltage gain A_β is given by

$$A_\beta = \frac{V_o}{V_i} = \frac{A}{1 + A\beta} \quad (8.16)$$

Note that A and β have reciprocal units. This in fact is always the case, resulting in a dimensionless loop gain $A\beta$.

The equivalent circuit model of the series-shunt feedback amplifier is shown in Fig. 8.8(b). Here R_β and R_o denote the input and output resistances with feedback. The relationship between R_β and R_o can be established by considering the circuit in Fig. 8.8(a).

$$\begin{aligned} R_\beta &= \frac{V_i}{I_i} = \frac{V_i}{V_o / R_o} \\ &= R_o \cdot \frac{V_i}{V_o} = R_o \cdot \frac{A(1 + A\beta)}{A} \end{aligned}$$

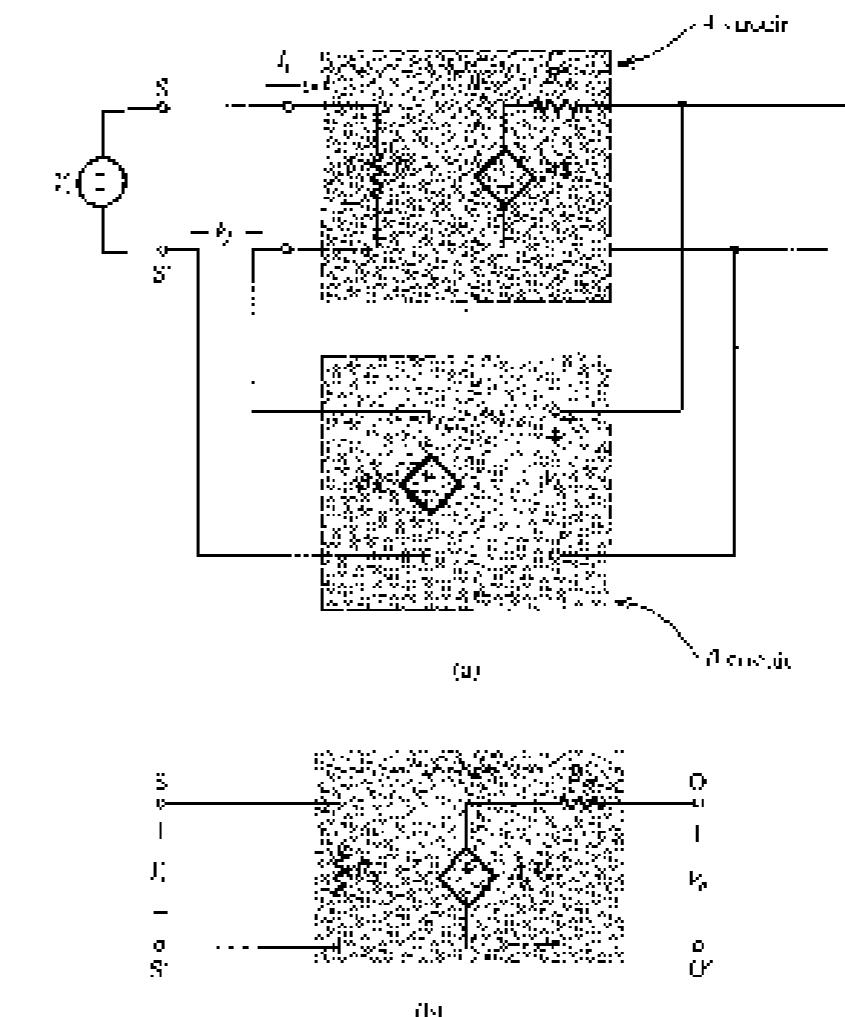


FIGURE 8.8 The series-shunt feedback amplifier: (a) ideal structure and (b) equivalent circuit.

Thus,

$$R_\beta = R_o / (1 + A\beta) \quad (8.17)$$

That is, in this case the negative feedback lowers the input resistance by a factor equal to the amount of feedback. Since the derivation above does not depend on the method of sampling (shunt or series), it follows that the relationship between R_β and R_o is independent of the method of mixing. We shall discuss this point further in later sections.

Note, however, that this result is not surprising and is physically intuitive: Since the feedback voltage V_β subtracts from V_o , the voltage that appears across R_o (that is, V_o) becomes quite small ($|V_o| = V_o / (1 + A\beta)$). Thus the input current, I_i , becomes correspondingly small and the resistance seen by V_i becomes large. Finally, it should be pointed out that Eq. (8.17) can be generalized to the form

$$Z_\beta(s) = Z_o(s) / (1 + A(s)\beta(s)) \quad (8.18)$$

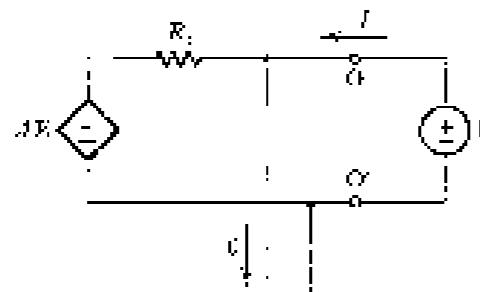


FIGURE 8.9 Measuring the output resistance of the feedback amplifier of Fig. 8.8(a); $y_{oi} = V_o/I_o$.

To find the output resistance, R_{oi} , of the feedback amplifier in Fig. 8.8(a) we reduce V_i to zero and apply a test voltage V_t at the output, as shown in Fig. 8.9.

$$R_{oi} = \frac{V_t}{I}$$

From Fig. 8.9 we can write

$$I = \frac{V_t - \beta V_o}{R_o}$$

and since $V_t = 0$ it follows from Eq. 8.8(a) that

$$V_o = -V_F = -\beta V_o = -\beta V_t$$

Thus

$$I = \frac{V_t + \beta V_o}{R_o}$$

leading to

$$R_{oi} = \frac{R_o}{1 + \beta}$$
(8.19)

That is, the negative feedback in fact *does* reduce the output resistance by a factor equal to the amount of feedback. With a little thought one can see that the derivation of Eq. 8.19 does not depend on the method of coupling. Thus the relationship between R_{oi} and R_o depends only on the method of sampling. Again, this result is not surprising and is physically intuitive. Since the feedback samples the output voltage V_o , it acts to stabilize the value of V_o ; that is, to reduce changes in the value of V_o , including changes due to load, to be brought about by changing the current drawn from the amplifier output terminals. This, in effect, means that voltage sampling feedback reduces the output resistance. Finally, we note that Eq. 8.19 can be generalized to

$$Z_{oi}(s) = \frac{Z_o(s)}{1 + A(s)\beta(s)}$$
(8.20)

8.4.2 The Practical Situation

In a practical series-voltage feedback amplifier, the feedback network will not be an ideal voltage-controlled voltage source. Rather, the feedback network is usually resistive and hence will load the basic amplifier and thus affect the values of A , R_o , and R_{oi} . In addition, the source and load resistances will affect these three parameters. Thus the problem we face is as follows: Given a series-voltage feedback amplifier represented by the block's diagram of Fig. 8.10(a), find the α circuit and the β circuit.

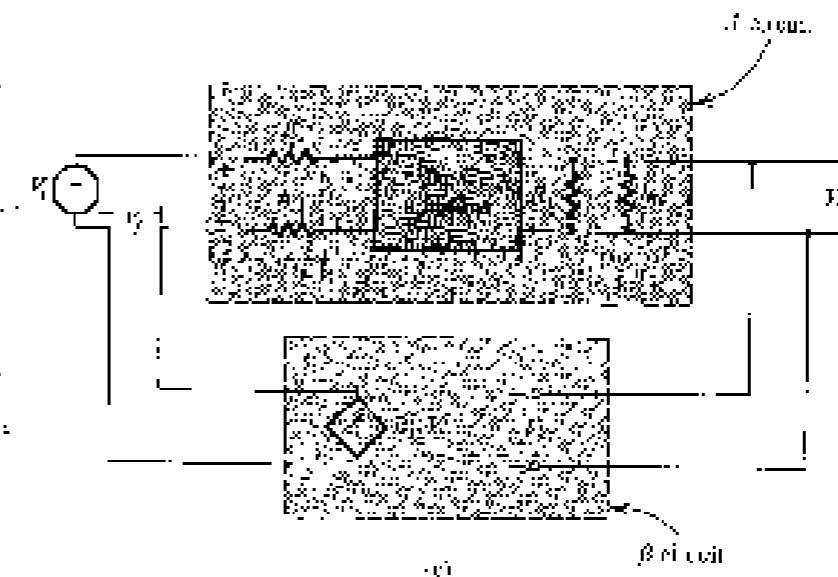
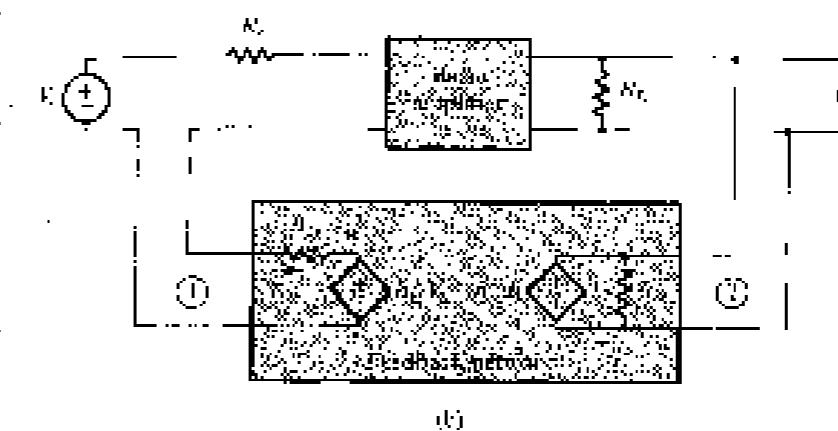
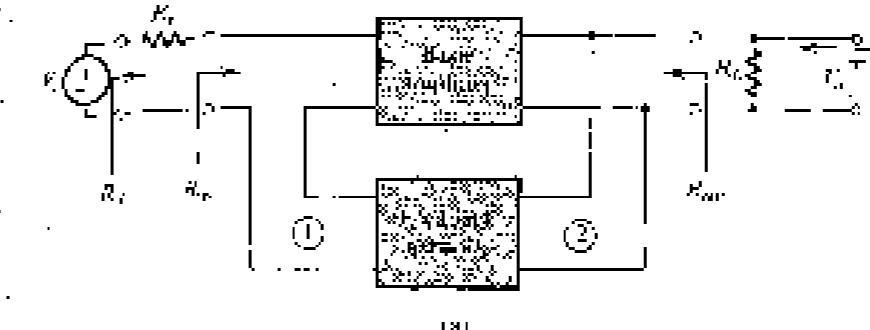


FIGURE 8.10 Practical series-voltage feedback amplifier: (a) block diagram; (b) practical series-voltage feedback amp.; (c) the circuit in (b) with the feedback network represented by two parallel branches. (d) the circuit in (c) with R_o neglected.

Our problem essentially involves representing the amplifier of Fig. 8.10(a) by the ideal structure of Fig. 8.8(b). As a first step toward this end we observe that the source and load resistances should be merged with the basic amplifier. This, together with representing a two-port feedback network in terms of its \hat{h} parameters (see Appendix B), is illustrated in Fig. 8.10(b). The choice of \hat{h} parameters is based on the fact that this is the only parameter set that represents the feedback network by a series network (port 1) and a parallel network at port 2. Such a representation is obviously convenient in view of the series connection of the input and the parallel connection at the output.

Preamplifier of the circuit in Fig. 8.10(b) reveals that the current source $b_2 h_2$ represents the forward transmission of the feedback network. Since the feedback network is usually passive, its forward transmission can be neglected in comparison to the much larger forward transmission of the basic amplifier. We will therefore assume that $b_2 \ll 1$ ($|b_2| \ll |h_{21}|$) and thus omit the controlled source $b_2 h_2$ altogether.

Compare the circuit of Fig. 8.10(b) (after eliminating $b_2 h_2$) with the ideal circuit of Fig. 8.8(a). We see that by including b_1 and b_2 with the basic amplifier we obtain the circuit shown in Fig. 8.10(c), which is very similar to the ideal circuit. Now, if the basic amplifier is unilateral (or almost unilateral), a situation that prevails when

$$|b_1|_{\text{actual}} \gg |b_1|_{\text{ideal}}, \quad (8.23)$$

then the circuit of Fig. 8.10(c) is equivalent (or approximately equivalent) to the ideal circuit. It follows then that the A circuit is obtained by augmenting the basic amplifier at the input with the source impedance R_s and the impedance b_{12} of the feedback network, and at the output with the load impedance R_L and the admittance b_{21} of the feedback network.

We conclude that the loading effect of the feedback network on the basic amplifier is represented by the components b_{12} and b_{21} . From the definitions of the \hat{h} parameters in Appendix B we see that b_{12} is the impedance looking into port 1 of the feedback network with port 2 short-circuited. Since port 2 of the feedback network is connected in shunt with the output port of the amplifier, short-circuiting port 2 destroys the feedback. Similarly, b_{21} is the admittance looking into port 2 of the feedback network with port 1 open-circuited. Since port 1 of the feedback network is connected in series with the output port, open-circuiting port 1 destroys the feedback.

These observations suggest a simple rule for finding the loading effects of the feedback network on the basic amplifier: The loading effect is found by looking into the appropriate port of the feedback network while the other port is open-circuited or short-circuited to destroy the feedback. If the connection is a shunt one, we short-circuit the port; if it is a series one, we open-circuit it. In Sections 8.5 and 8.6 it will be seen that this simple rule applies also to the other three feedback topologies.³

We next consider the determination of β . From Fig. 8.10(c), we see that β is equal to b_{12} of the feedback network:

$$\beta = b_{12} = \frac{V_2}{V_{212}} \quad (8.24)$$

Thus to measure β , one applies a voltage to port 2 of the feedback network and measures the voltage that appears at port 1 while the latter port is open-circuited. This result is intuitively appealing because the object of the feedback network is to supply the output voltage ($V_2 = V_{212}$) and provide a voltage signal ($V_1 + V_2$) that is mixed in series with the input source. The voltage

³ A simple rule to remember is: If the connection is a shunt, short it; if series, open it.

connection at the input suggests that (as in the case of finding the loading effects of the feed-back network) β should be found with port 1 open-circuited.

8.4.3 Summary

A summary of the rules for finding the A circuit and β for a given series-shunt feedback amplifier of the form in Fig. 8.10(a) is given in Fig. 8.11. As for using the feedback formulas in Eqs. (8.17) and (8.18) to determine the input and output resistances, it is important to note that

1. R_s and R_L are the input and output resistances, respectively, of the A circuit (see Fig. 8.10(a)).
2. R_{12} and R_{21} are the input and output resistances, respectively, of the feedback amplifier, including R_s and R_L (see Fig. 8.10(a)).
3. The actual input and output resistances of the feedback amplifier usually exclude R_s and R_L . These are denoted R_{12}' and R_{21}' in Fig. 8.10(a) and can be easily determined as

$$R_{12}' = R_{12} - R_s \quad (8.25)$$

$$R_{21}' = 1 / \left(\frac{1}{R_{21}} - \frac{1}{R_L} \right) \quad (8.26)$$

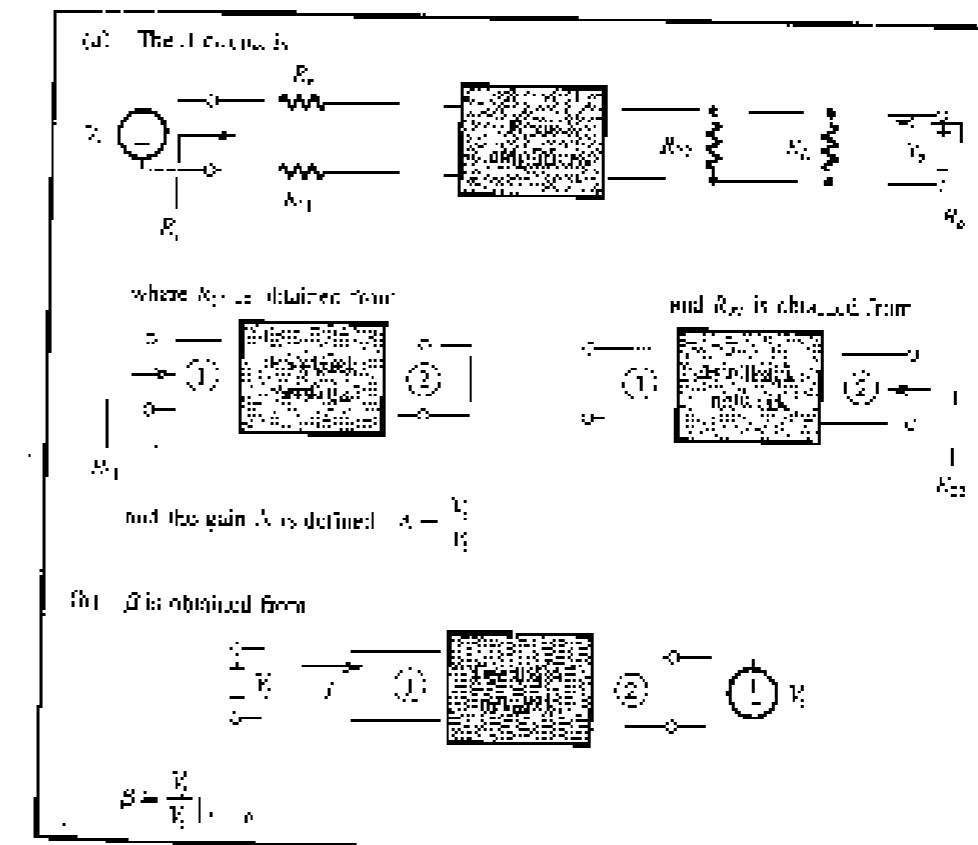


FIGURE 8.11 Summary of the rules for finding the A circuit and β for a given series-shunt feedback amplifier of the form in Fig. 8.10(a).

Figure 8.12(c) shows an op-amp connected in the noninverting configuration. The op-amp has an open-loop gain A and a feedback input resistance R_f , and an output resistance r_o . Recall that in the analysis of op-amp circuits in Chapter 2, we neglected the effects of R_f (assumed it to be infinite) and of r_o (assumed it to be zero). Here we wish to use the feedback method to analyze the circuit, taking both R_f and r_o into account. First express the closed-loop gain V_o/V_i , the input resistance R_i (see Fig. 8.12(a)), and the output resistance R_{oL} . Also find numerical values, given $\mu = 10^3$, $R_1 = 100\text{ k}\Omega$, $r_o = 1\text{ M}\Omega$, $R_2 = 2\text{ k}\Omega$, $K_1 = 1\text{ M}\Omega$, $R_3 = 1\text{ M}\Omega$, and $R_4 = 10\text{ k}\Omega$.

Solution

We observe that the feedback network consists of R_f and R_i . This network samples the output voltage V_o and provides a voltage signal (across R_i) that is mixed in series with the input source V_i .

The Δ circuit can be easily obtained following the rules of Fig. 6.1.1, and is shown in Fig. 8.12(b). For this circuit we can write by inspection

$$\Delta = \frac{V_o}{V_i} = \frac{(R_f R_i R - R_f)}{R_f [R_i(R_1 + R_2) + r_o R_{oL} - R_f \sqrt{R_i R_o}]} = \frac{R_f}{R_f + R_i(R_1 + R_2) + r_o R_{oL} - R_f \sqrt{R_i R_o}}$$

For the values given, we find that $\Delta = 0.001\text{ MV}$.

The circuit for obtaining β is shown in Fig. 8.12(a), from which we obtain

$$\beta = \frac{V_o}{V_i} = \frac{R_f}{R_f + R_i} \approx 10^{-3} \text{ MV/V}$$

The voltage gain with feedback is now obtained as

$$A_f = \frac{V_o}{V_i} = \frac{\Delta}{1 - A\beta} = \frac{0.0001}{1 - 10^{-3}} = 250 \text{ V/V}$$

The input resistance R_i determined by the feedback equations is the resistance seen by the external source (see Fig. 8.12(c)), and is given by

$$R_i = R_f(1 + A\beta)$$

where R_f is the input resistance of the Δ circuit in Fig. 8.12(b).

$$R_f = R_1 + R_2 + R_o R_{oL}$$

For the values given, $R_f = 11\text{ k}\Omega$, resulting in

$$R_i = 11 \times 10^3 = 777 \text{ k}\Omega$$

This, however, is not the resistance asked for. What is required is R_{iL} indicated in Fig. 8.12(a). To obtain R_{iL} we subtract R_i from R_f :

$$R_{iL} = R_f - R_i$$

For the values given, $R_{iL} = 339\text{ k}\Omega$. The resistance R_{iL} given by the feedback equations is the output resistance of the feedback amplifier, including the load resistance R_o , as indicated in Fig. 8.12(a). R_{oL} is given by

$$R_{oL} = \frac{R_o}{1 + A\beta}$$

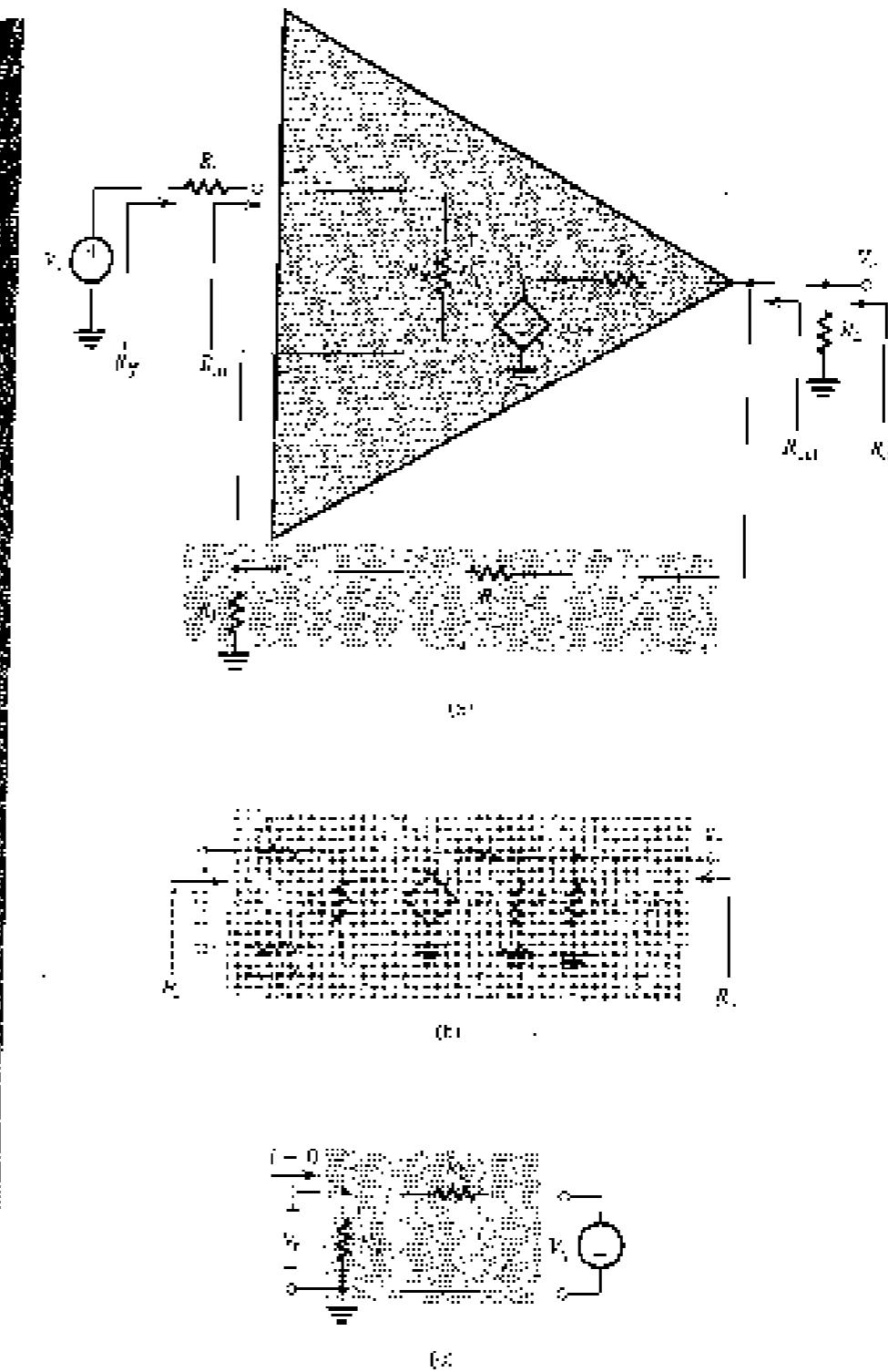


FIGURE 8.13 (continued) Example 8.1

where R_2 is the output resistance of the A circuit. R_2 can be obtained by inspection of Fig. 8.12(a) as

$$R_2 = r_o \parallel R_{\text{in}} \parallel (R_1 + R_f)$$

For the values given, $R_2 = 667 \Omega$, and

$$R_{\text{out}} = \frac{667}{7} = 95.1 \Omega$$

The resistance asked for, R_{out} , is the output resistance of the feedback amplifier excluding R_f . From Fig. 8.12(a) we see that

$$R_{\text{out}} = R_{\text{in}} \parallel R_2$$

Thus

$$R_{\text{out}} = 100 \Omega$$

EXERCISES

4.4 The load of Exercise 8.1 has a negative feedback loop load impedance of $-1 \text{ k}\Omega$. Find the 3 dB frequency of the closed-loop system.

4.5 $\beta = 1/2$

4.5 The input voltage to the FET source follower differential stage defined by the simulation diagram is $v_s = 10 \text{ mV}$. Assume $R_f = 10 \text{ k}\Omega$, $R_{\text{in}} = 10 \text{ M}\Omega$, $R_{\text{out}} = 10 \text{ k}\Omega$, and $V_{GS} = -0.5 \text{ V}$. The load is a $10 \text{ k}\Omega$ resistor. The output voltage is measured at node 1. The output voltage is approximately zero. Then find the values of A , B , and C if $V_{GS} = -0.5 \text{ V}$ and $R_{\text{out}} = 10 \text{ k}\Omega$. Assume that the transistors have 10^{-12} A .

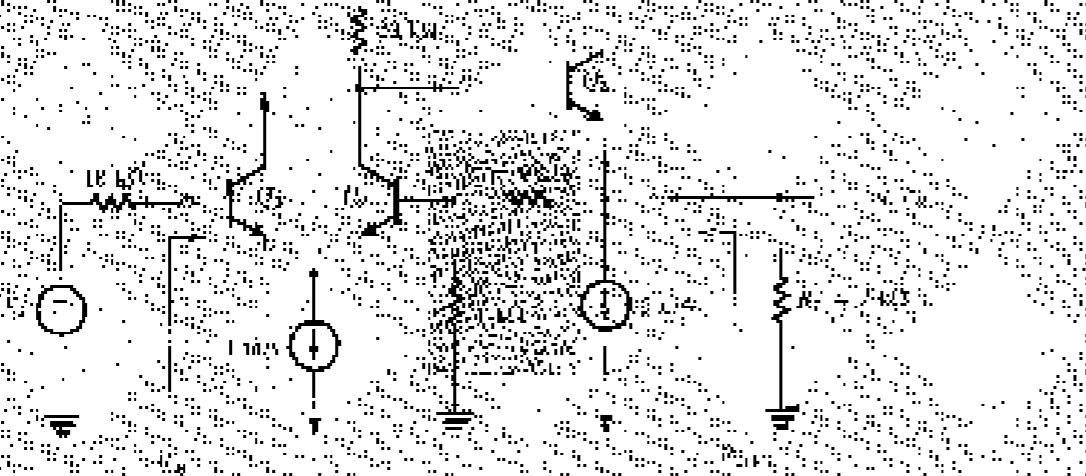


FIGURE 8.5

An. 82.7 $V(v_s, 0)$; $V(v_s, 8.96 \text{ V})$; $V(v_s, 19.1 \text{ V})$

8.5 THE SERIES-SERIES FEEDBACK AMPLIFIER

8.5.1 The Ideal Case

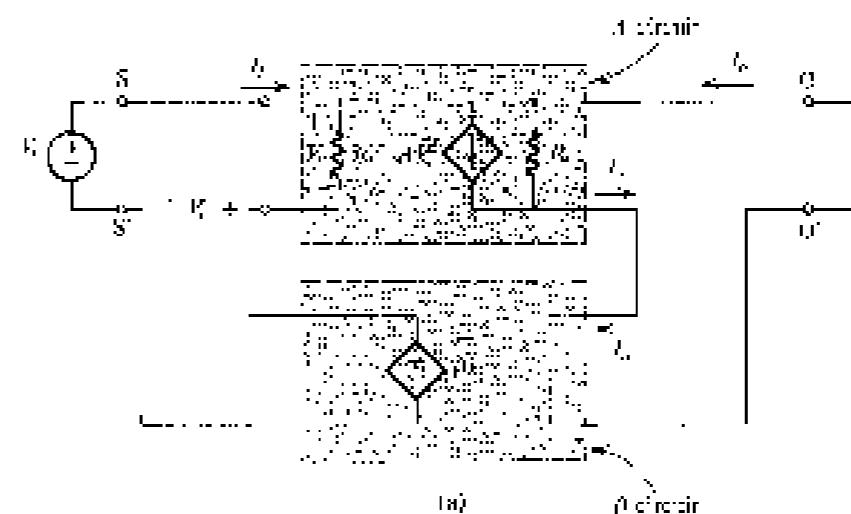
As mentioned in Section 8.2, the series-series feedback topology stabilizes $A_c v_o$ and is therefore best suited for transconductance amplifiers. Figure 8.17(a) shows the ideal structure for the series-series feedback amplifier. It consists of a unilateral open-loop amplifier (the A circuit) and an ideal feedback network. Note that in this case A is a transconductance.

$$A = \frac{I_o}{V_s} \quad (8.23)$$

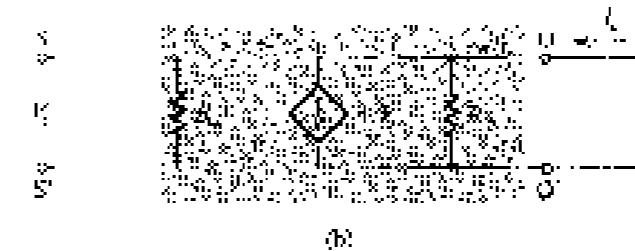
while β is a transresistance. Thus the loop gain $A\beta$ remains a dimensionless quantity, as it should always be.

In the ideal structure of Fig. 8.17(a), the load and source resistances have been absorbed inside the A circuit, and the β circuit does not load the A circuit. Thus the circuit follows the dual feedback model of Fig. 8.1, and we can write

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + A\beta} \quad (8.24)$$



(a) A circuit



(b)

FIGURE 8.13 The series-series feedback amplifier in ideal structure and the equivalent circuit.

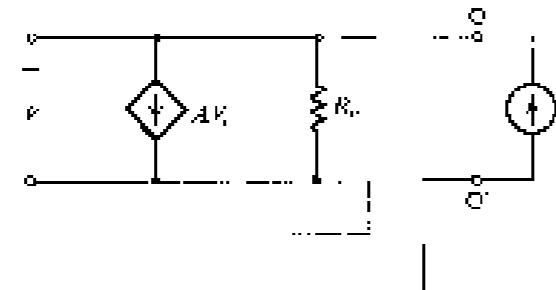


FIGURE 8.14 Measuring the input resistance R_s of a series-series feedback amplifier.

This transconductance-with-feedback is included in the equivalent circuit model of the feedback amplifier, shown in Fig. 8.17(b). In this model, R_s is the input resistance with feedback. Using an analysis similar to that in Section 8.4, we can show that

$$R_s = R_i(1 + A\beta) \quad (8.27)$$

This relationship is identical to that obtained in the case of source-shunt feedback. This confirms our earlier observation that the relationship between R_s and R_i is a function only of the method of mixing. Voltage (or series) mixing therefore always increases the input resistance.

To find the output resistance R_o of the series-series feedback amplifier of Fig. 8.13(a) we reduce V_i to zero and break the output circuit to apply a test current I_t , as shown in Fig. 8.14;

$$R_o = \frac{V}{I_t} \quad (8.28)$$

In this case, $V_i = V_f = -\beta I_o = -\beta I_t$. Thus for the circuit in Fig. 8.14 we obtain

$$V = (I_t - A V_i) R_s = (I_t - A\beta I_t) R_s$$

Hence

$$R_o = (1 + A\beta) R_s \quad (8.29)$$

That is, in this case the negative feedback increases the output resistance. This should have been expected, since the negative feedback tries to make I_t constant in spite of changes in the output voltage, which means increased output resistance. This result also confirms our earlier observation. The relationship between R_o and R_i is a function only of the method of mixing. While voltage (shunt) sampling reduces the output resistance, current (series) sampling increases it.

8.5.2 The Practical Case

Figure 8.15(a) shows a block diagram for a practical series-series feedback amplifier. To be able to apply the feedback equations to this amplifier, we have to represent it by the ideal structure of Fig. 8.13(a). Our objective therefore is to derive a simple method for finding A and β . Observe the definition of the amplifier input resistance R_{in} and output resistance R_{out} . It is important to note that these are different from R_s and R_o , which are determined by the feedback equations, as will become clear shortly.

The series-series amplifier of Fig. 8.15(a) is redrawn in Fig. 8.15(b) with R_s and R_o shown closer to the basic amplifier, and the two-port feedback network represented by its z -parameters (Appendix B). This parameter set has been chosen because it is the only one that provides a representation of the feedback network with a series circuit on the input and a

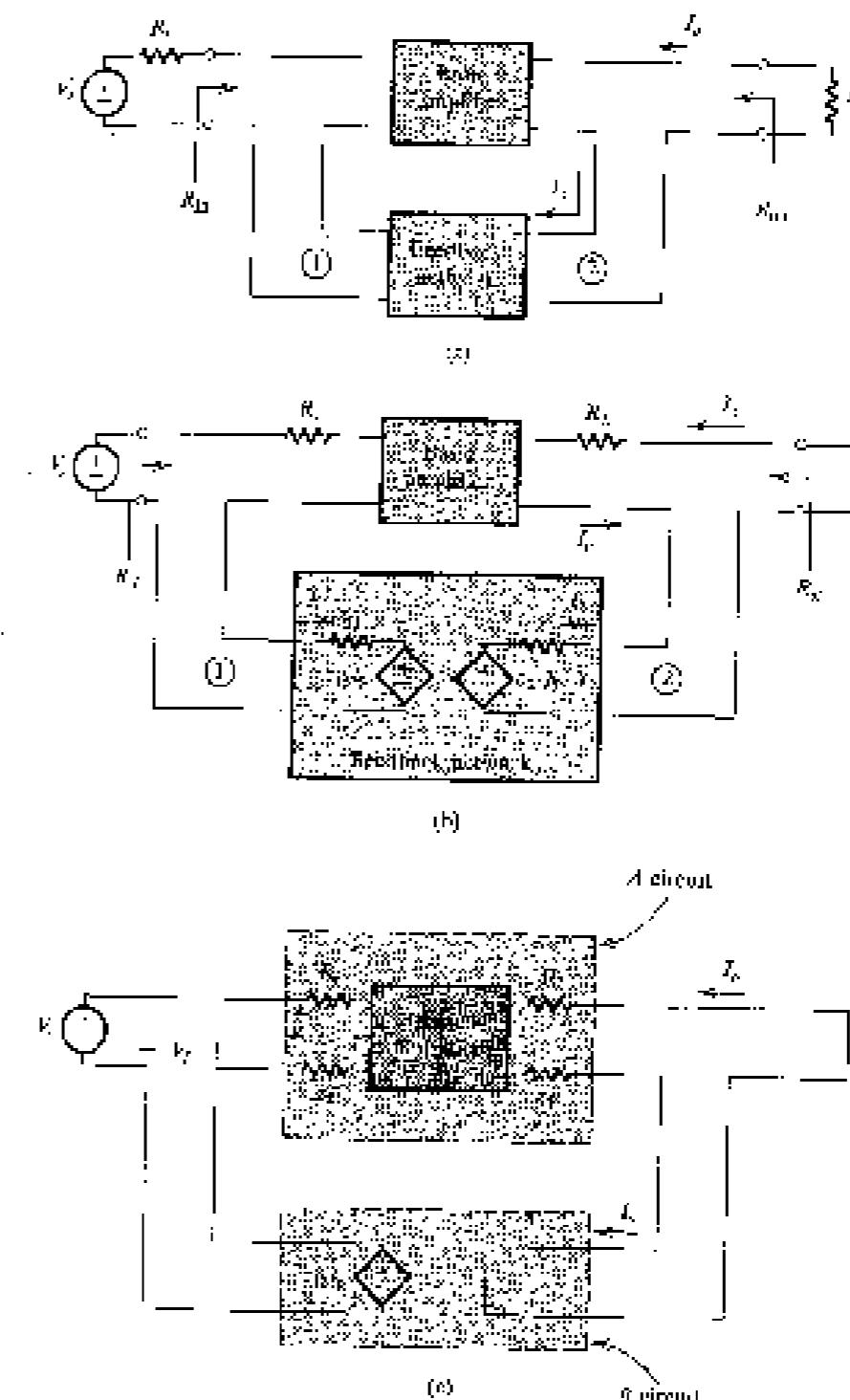


FIGURE 8.15 (a) Block diagram of a practical series-series feedback amplifier; (b) The circuit of (a) with the feedback network represented by its z -parameters, (1, 2), following (c) the circuit of (b) with z -parameters (1, 2) replaced.

series circuit at the output. This is obviously convenient in view of the series connections at input and output. The input and output resistances with feedback, R_f and R_{out} , are indicated on the diagram.

As we have done in the case of the series-shunt amplifier, we shall assume that the feed-forward term due to the feedback network is negligible in comparison to that through the basic amplifier; that is, the condition:

$$|\beta_1| \ll 1 \quad (\text{Series-shunt case}) \quad (8.20)$$

is satisfied. We can then do so with the voltage source $\beta_2 I_2$ in Fig. 8.15(a). Doing this, and reducing the circuit to include β_{11} and β_{12} with the basic amplifier, results in the circuit in Fig. 8.15(b). Now if the basic amplifier is nonlinear (for current limitation), a situation can be obtained where

$$\beta_1 R_{\text{in}} \gg \beta_2 R_{\text{out}} \quad (\text{Series-shunt case}) \quad (8.21)$$

then the circuit in Fig. 8.15(b) is equivalent (or almost equivalent) to the ideal circuit of Fig. 8.13(a).

It follows that the A circuit is composed of the basic amplifier augmented at the input with R_i and β_{11} and augmented at the output with R_o and β_{12} . Since β_{11} and β_{12} are the impedances looking between 1 and 2, respectively, at the feedback network with the other port open-circuited, we see that finding the leading effects of the feedback network on the basic amplifier follows the rule formulated in Section 8.4. That is, we look into one port of the feedback network while the other port is open-circuited or short-circuited so as to destroy the feedback loop if series and short if shunt.

From Fig. 8.15(b) we see that β is equal to β_2 of the feedback network,

$$\beta = \beta_2 = \frac{V_2}{I_2} \quad (8.22)$$

This result is interestingly appealing. Recall that in this case the feedback network samples the output current ($I_2 = I_1$) and provides a voltage ($V_2 = V_1$) that is mixed in series with the input source. Again, the series connection at the input suggests that β is measured with port 1 open.

8.5.3 Summary

For future reference we present in Fig. 8.16 a summary of the rules for finding A and β for a given series-series feedback amplifier of the type shown in Fig. 8.15(a). Note that R_i is the input resistance of the A circuit, and its output resistance is R_o , which can be determined by breaking the output loop and looking between 1 and V' . R_f and R_{out} can be used in Eqs. (8.27) and (8.29) to determine R_g and R_{in} (see Fig. 8.15(a)). The input and output resistances of the feedback amplifier can then be found by subtracting R_i from R_g and R_o from R_{out} :

$$R_g = R_f + R_i \quad (8.23)$$

$$R_{\text{in}} = R_g' - R_i \quad (8.24)$$

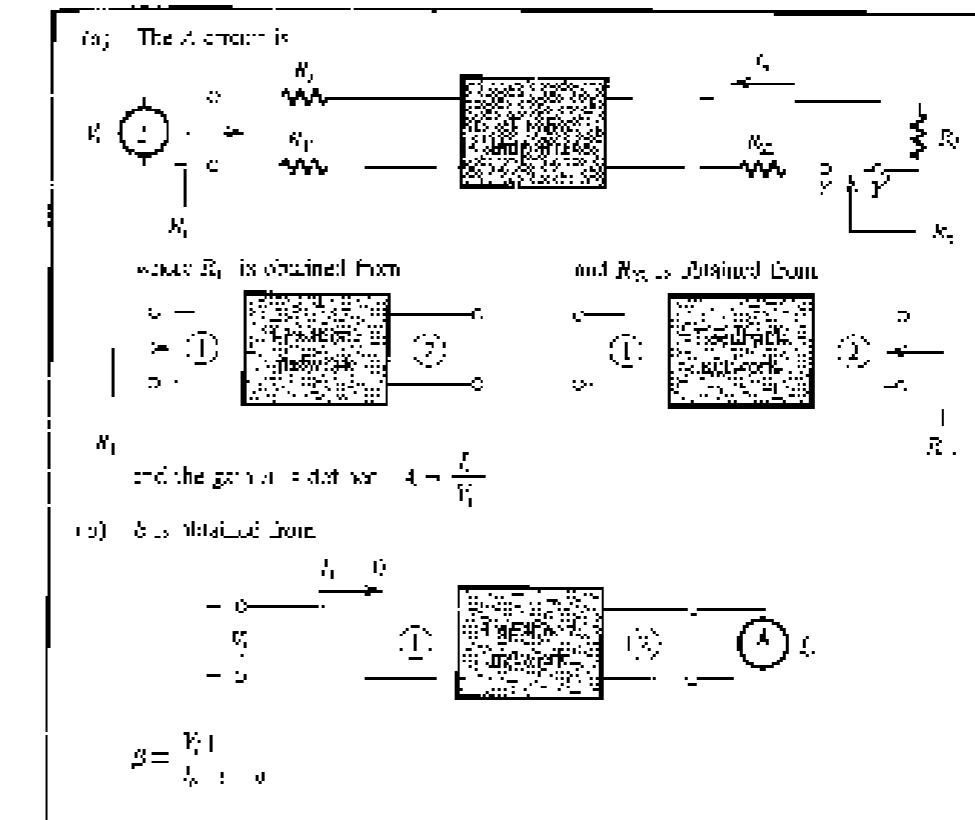


FIGURE 8.16 Finding the A circuit and β for the voltage-mixing current-coupling (series-series) case.

Recently, negative feedback extends the amplifier bandwidth, as commonly used in the design of broadband amplifiers. One such amplifier is the MC1553. Part of the circuit of the MC1553 is shown in Fig. 8.17(a). The circuit shown (called a feedback opamp) is composed of three gain stages with series-series feedback provided by the network composed of R_{fb} , R_f , and R_{in} . Assume that the bias circuit, which is not shown, causes $I_{C1} = 0.6 \text{ mA}$, $I_{C2} = 1 \text{ mA}$, and $I_{C3} = 1 \text{ mA}$. Using these values and assuming $R_f = 100$ and $r_{\text{in}} = \infty$, find the open-loop gain A , the feedback factor β , the closed-loop gain $A_{\text{cl}} = I_{C2}/V_1$, the voltage gain V_o/V_1 , the output resistance $R_o = R_{\text{fb}}$, and the output resistance R_g (between nodes 1 and V'), as indicated. Now, if r_o of Q_2 is $25 \text{ k}\Omega$, estimate an appropriate value of the output resistance R_g .

Solution

Employing the leading rules given in Fig. 8.16, we obtain the A circuit shown in Fig. 8.17(b). To find $A = V_2/V_1$, we first compute the gain of the first stage. This can be written by inspection as

$$\frac{V_{21}}{V_1} = \frac{-\alpha_1 (R_{\text{fb}}/R_{\text{in}})}{r_{\text{in}} + (R_{\text{fb}}/\alpha_1 (R_f - R_{\text{fb}}))}$$

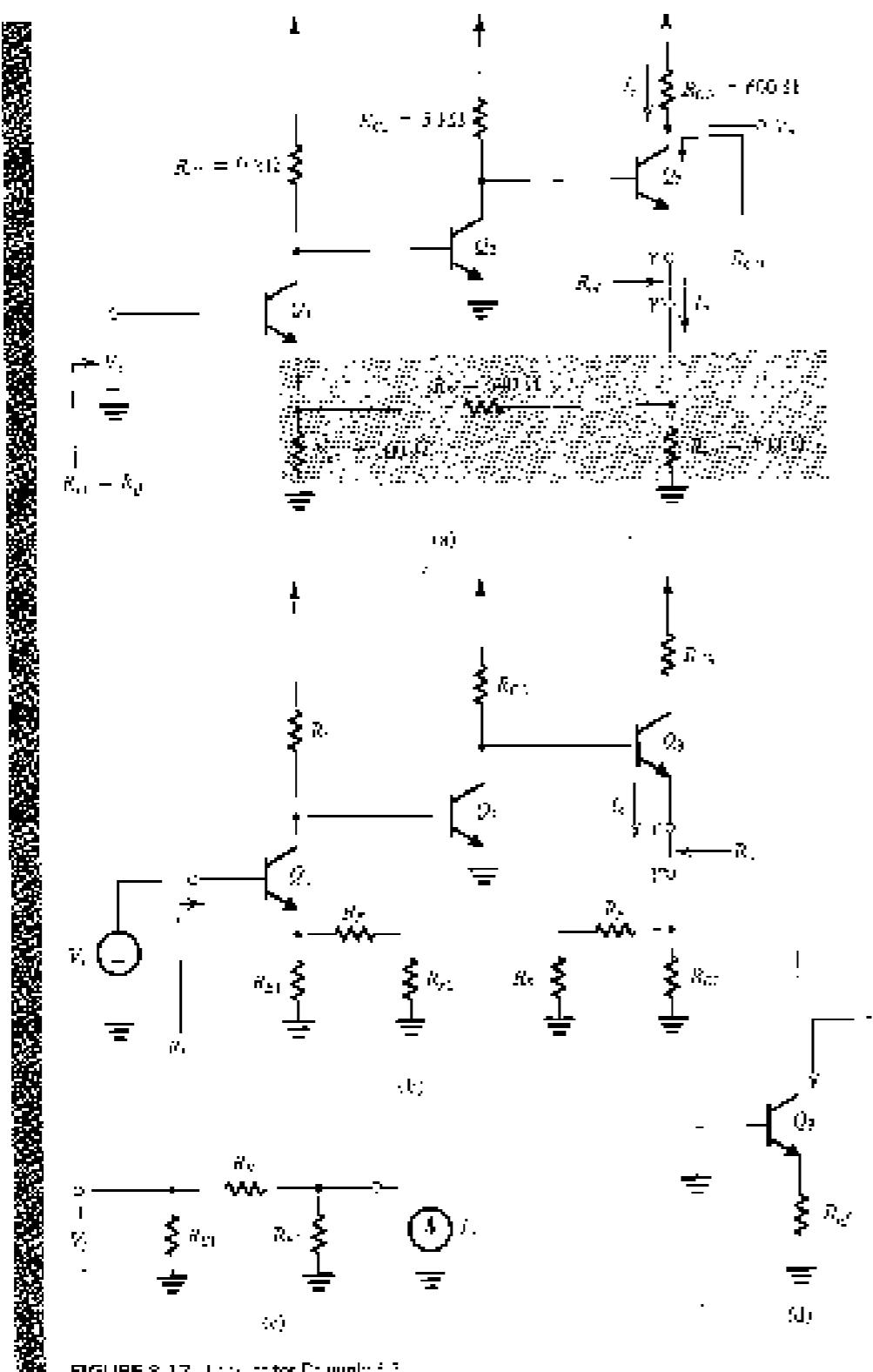


FIGURE 8.17 Unvoltor Example 8.2.

Since Q_1 is biased at 0.6 mA , $\alpha = 41.7 \Omega$. Transistor Q_2 is biased so that $i_{\text{C2}} = i_{\text{C1}}/\beta_{\text{M2}} = 10.5/40 = 2.5 \text{ mA}$. Substituting these values together with $\alpha = 0.98$, $R_{\text{C1}} = 9 \text{ k}\Omega$, $R_{\text{L}} = 100 \text{ k}\Omega$, $R_{\text{F2}} = 420 \text{ }\Omega$, and $R_{\text{F3}} = 100 \text{ }\Omega$ results in

$$\frac{V_{\text{O1}}}{V_{\text{I}}} = -14.92 \text{ V/V}$$

Next we determine the gain of the second stage, which can be written by inspection as (note that $V_{\text{O2}} = V_{\text{O1}}$)

$$\frac{V_{\text{O2}}}{V_{\text{I}}} = -g_{\text{m2}}(R_{\text{C2}})\beta/\beta_{\text{M2}} = -(1/r_{\text{e2}} + (R_{\text{C2}}/\beta(R_{\text{L}} + R_{\text{C2}}))V_{\text{I}})$$

Substituting $g_{\text{m2}} = 40 \text{ mA/V}$, $R_{\text{C2}} = 5 \text{ k}\Omega$, $\beta_{\text{M2}} = 100$, $r_{\text{e2}} = 25.64 = 6.25 \text{ }\Omega$, $R_{\text{L}} = 100 \text{ k}\Omega$, and $R_{\text{C2}} = 100 \text{ }\Omega$, results in

$$\frac{V_{\text{O2}}}{V_{\text{I}}} = -131.2 \text{ V/V}$$

Finally, for the third stage we obtain by inspection

$$\begin{aligned} \frac{V_{\text{O3}}}{V_{\text{I}}} &= \frac{i_{\text{C3}}}{V_{\text{I}}} = \frac{1}{r_{\text{e3}} + (R_{\text{C3}}/\beta(R_{\text{L}} + R_{\text{C3}}))} \\ &= \frac{1}{6.25 + (100/710)} = 99.6 \text{ mA/V} \end{aligned}$$

Combining the gains of the three stages results in

$$\begin{aligned} A &= \frac{V_{\text{O}}}{V_{\text{I}}} = -4.92 \times -131.2 \times 10.6 \times 10^{-3} \\ &= 20.7 \text{ A/V} \end{aligned}$$

The circuit for determining the feedback factor β is shown in Fig. 8.7(b), from which we find

$$\begin{aligned} \beta &\equiv \frac{V_{\text{I}}}{I_{\text{f}}} = \frac{R_{\text{F1}}}{R_{\text{F1}} + R_{\text{F2}} + R_{\text{F3}}} \times R_{\text{F1}} \\ &= \frac{10}{10 + 640 + 10} \times 10 = 11.9 \text{ }\Omega \end{aligned}$$

The closed-loop gain is given now by found from

$$\begin{aligned} A_f &= \frac{A}{1 + \beta A} = \frac{A}{1 + \beta F} \\ &= \frac{20.7}{1 + 20.7 \times 1.9} = 32.7 \mu\text{A/V} \end{aligned}$$

The voltage gain is found from

$$\begin{aligned} \frac{V_{\text{O}}}{V_{\text{I}}} &= \frac{-I_{\text{f}}R_{\text{C2}}}{V_{\text{I}}} = \frac{-I_{\text{f}}R_{\text{C2}}}{V_{\text{I}}} = -A_f R_{\text{C2}} \\ &= -32.7 \times 10^{-6} \times 100 = -3.27 \text{ V/V} \end{aligned}$$

The output resistance of the feedback amplifier is given by

$$R_{\text{O}} = R_{\text{L}}(1 + \beta F)$$

where R_i is the input resistance of the A circuit. The value of R_i can be found from the circuit in Fig. 8.17(b) as follows:

$$R_i = (R_{A2} + 1)(r_{e1} + (R_{A1}/\beta)(R_2 + R_{A2})) \\ = 15.65 \text{ k}\Omega$$

Thus,

$$R_o = 10.05(1 - 20.5 \times 11.9) = 3.31 \text{ M}\Omega$$

To find the output resistance R_o of the A circuit in Fig. 8.17(b), we break the circuit between y and y' . The resistance looking between these two nodes can be found to be

$$R_o = [R_{A2}/(\beta R_1 + R_{A2})] + r_{e2} + \frac{R_{A2}}{\beta_r + 1}$$

which, for the values given, yield $R_o = 143.9 \Omega$. The output resistance R_o of the feedback amplifier can now be found as

$$R_o = R_o(1 + A\beta) = 143.9(1 - 20.7 \times 11.9) = 35.6 \text{ k}\Omega$$

Note that the feedback stabilizes the collector current of Q_2 , and thus the output resistance, that is determined by the feedback formula, is the resistance of the emitter loop (i.e., between V_b and V_{o2}), which we have just found, and not the resistance looking into the collector³ of Q_2 . This is because the output resistance r_o of Q_2 is in effect outside the feedback loop. We can, however, use the value of R_o to obtain an approximate value for R_{o2} . To do this, we assume that the effect of the feedback is to place a resistance $R_{o2}(15.6 \text{ k}\Omega)$ in the emitter of Q_2 , and find the output resistance from the equivalent circuit shown in Fig. 8.17(d). Using Eq. (6.1-1), R_{o2} can be found as

$$R_{o2} = r_o + (1 + \beta_r/\beta)(R_{o2}/\beta r_{e2}) \\ = 35.6(1 - 160 \times 25)(35.6/0.625) = 2.0 \text{ M}\Omega$$

Thus, the output resistance in the collector increases, but not by $(1 + A\beta)$.

EXERCISE

- 8.10 A feedback circuit has a gain of $A = 10^4$, a load resistance of $R_L = 10 \text{ k}\Omega$, and a feedback factor of $\beta = 0.1$. The input resistance is $R_i = 10 \text{ k}\Omega$. The forward gain is considered to be of the voltage-controlled voltage-controlled type. Note, however, that the load gain is not the same as the forward gain. Find the values of V_b , V_{o1} , V_{o2} , V_{o3} , V_{o4} , V_{o5} , V_{o6} , V_{o7} , and V_{o8} in volts.

8.6 THE SHUNT-SHUNT AND SHUNT-SERIES FEEDBACK AMPLIFIERS

In this section we shall extend "without proof" the method of Sections 8.4 and 8.5 to the two remaining feedback topologies.

³This important point was first brought to the author's attention by Gustav Robert von Koenigs / C. Scirra, 1992.

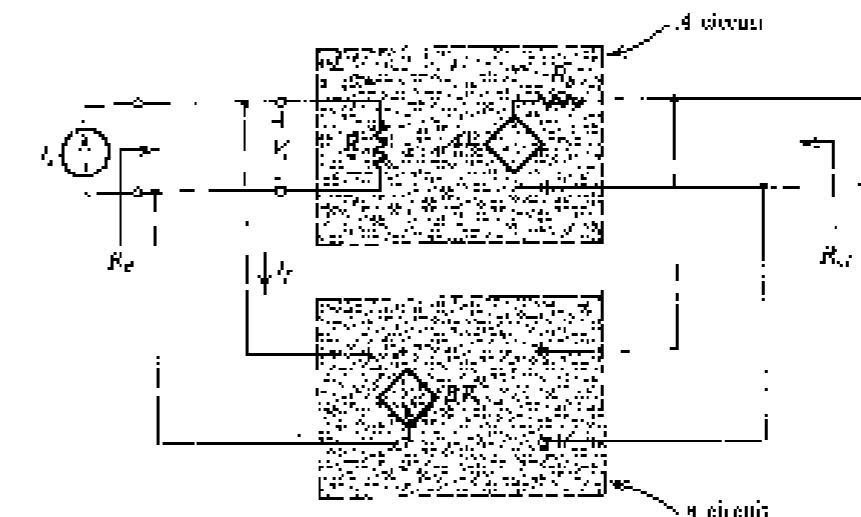


FIGURE 8.18 Ideal structure for the shunt-shunt feedback amplifier.

8.6.1 The Shunt-Shunt Configuration

Figure 8.18 shows the ideal structure for a shunt-shunt feedback amplifier. Here the A circuit has an input resistance R_i , a transresistance A , and an output resistance R_o . The β circuit is a voltage-controlled current source, and β is a transconductance. The closed-loop gain A_f is defined

$$A_f = \frac{V_o}{V_i} \quad (8.65)$$

and is given by

$$A_f = \frac{A}{1 + A\beta}$$

The input resistance with feedback is given by

$$R_{i_f} = \frac{R_i}{1 + A\beta} \quad (8.66)$$

where we note that the shunt connection at the input results in a reduced input resistance. Also note that the resistance R_i is the resistance seen by the source I_i , and it includes any source resistance.

The output resistance with feedback is given by

$$R_{o_f} = \frac{R_o}{1 + A\beta} \quad (8.67)$$

where we note that the shunt connection at the output results in a reduced output resistance. This resistance includes any load resistance.

Given a practical shunt-shunt feedback amplifier having the block diagram of Fig. 8.19, we use the method given in Fig. 8.20 to obtain the A circuit and the circuit for determining β . As in Sections 8.4 and 8.5, the method of Fig. 8.20 assumes that the basic amplifier is almost unilateral and that the forward transmission through the feedback network is negligibly small.

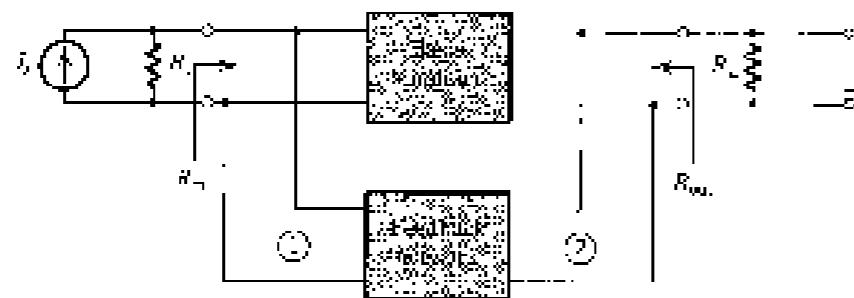
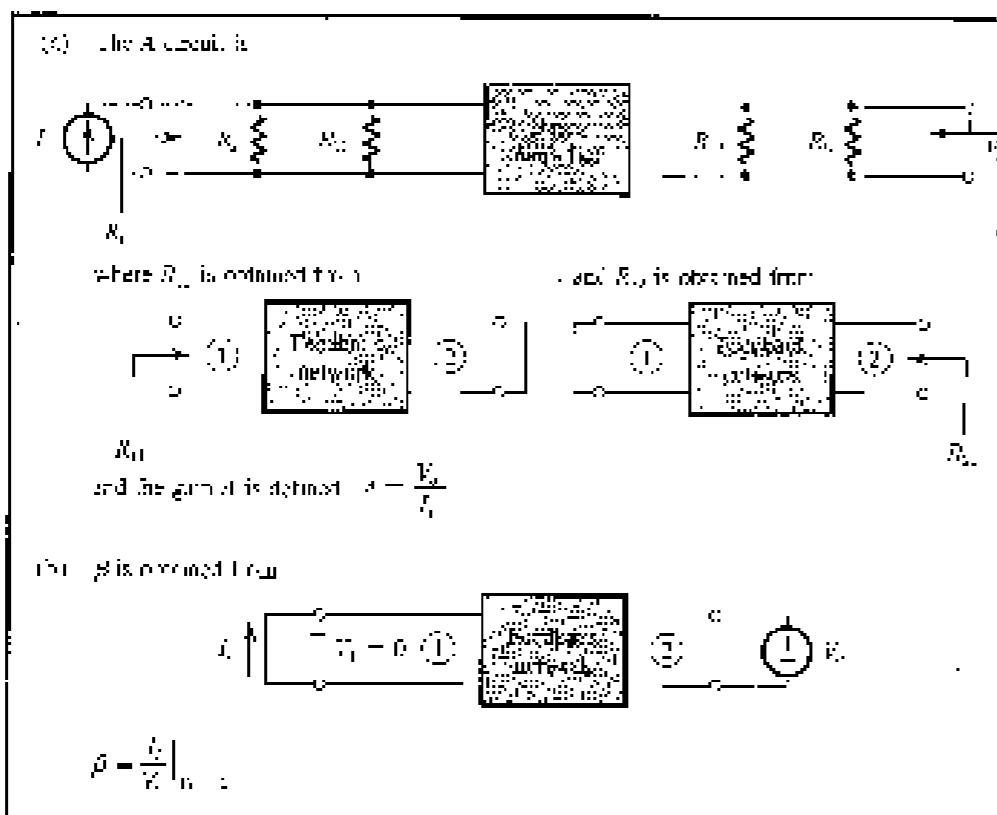


FIGURE 8.19 Block diagram for a practical shunt-shunt feedback amplifier.

FIGURE 8.20 Finding the A circuit and β for the current-mixing voltage-coupling (current-voltage) feedback amplifier in Fig. 8.19.

The first assumption is justified when the α parameters⁶ of the basic amplifier and of the feedback network satisfy the condition

$$|\beta| \ll |\alpha_{11}| \ll |\alpha_{12}| \alpha_{22} \quad (8.38)$$

⁶For e, the α parameters (Appendix B) are used because this is the only two-port parameter set that provides a representation of the feedback network with a parallel load at the input and a parallel circuit at the output.

The second assumption is justified when the forward α parameters satisfy the condition

$$|\alpha_{11}| \gg |\alpha_{12}| \alpha_{22} \quad (8.39)$$

Finally, we note that once R_f and R_{in} have been determined using the feedback formulas (Eqs. 8.36 and 8.37), the input and output resistances of the cascaded stages (see definitions in Fig. 8.19) can be obtained as

$$R_{in} = \frac{1}{\beta_1 \alpha_{11} + \alpha_{22}} \quad (8.40)$$

$$R_{out} = \frac{1}{\beta_2 \alpha_{11} + \alpha_{22}} \quad (8.41)$$

Example 8.2

We want to analyze the circuit of Fig. 8.21(a) to determine the small-signal voltage gain V_o/V_{in} , the input resistance R_{in} , and the output resistance $R_{out} = R_{fb}$. The transistor has $\beta = 100$.

Solution

First, we determine the transistor dc operating point. The dc analysis is illustrated in Fig. 8.21(b); from which we can write

$$V_t = 0.7 + (I_b - 0.07)12 = 5.89 + 12I_b \quad \text{and} \quad \frac{12 - V_t}{4.7} = (\beta + 1)I_E + 0.07$$

These two equations can be solved to obtain $I_b = 0.015 \text{ mA}$, $I_E = 1.5 \text{ mA}$, and $V_t = 5.2 \text{ V}$.

To carry out small-signal analysis we first recognize that the feedback is provided by R_f , which samples the output voltage V_o and feeds back a current that is mixed with the source current. Thus it is convenient to use the Norton source representation, as shown in Fig. 8.21(c). The A circuit can be easily obtained using the rules of Fig. 8.20, and it is shown in Fig. 8.21(d). For the A circuit we can write by inspection

$$V_o = I_o(R_f R_f / R_{fb})$$

$$V_i = -g_m V_o (R_f / R_{fb})$$

Thus

$$A = \frac{V_o}{V_i} = -g_m (R_f / R_{fb})(R_f / R_f / g_m) \\ = -75 \times 7 \text{ k}\Omega$$

The input and output resistances of the A circuit can be obtained from Fig. 8.21(d) as

$$R_i = R_f / R_f / g_m = 1.4 \text{ k}\Omega$$

$$R_o = R_f / R_f = 4.7 \text{ k}\Omega$$

The circuit for determining β is shown in Fig. 8.21(e), from which we obtain

$$\beta = \frac{I_c}{V_o} = \frac{1}{R_f} = \frac{1}{4.7 \text{ k}\Omega}$$

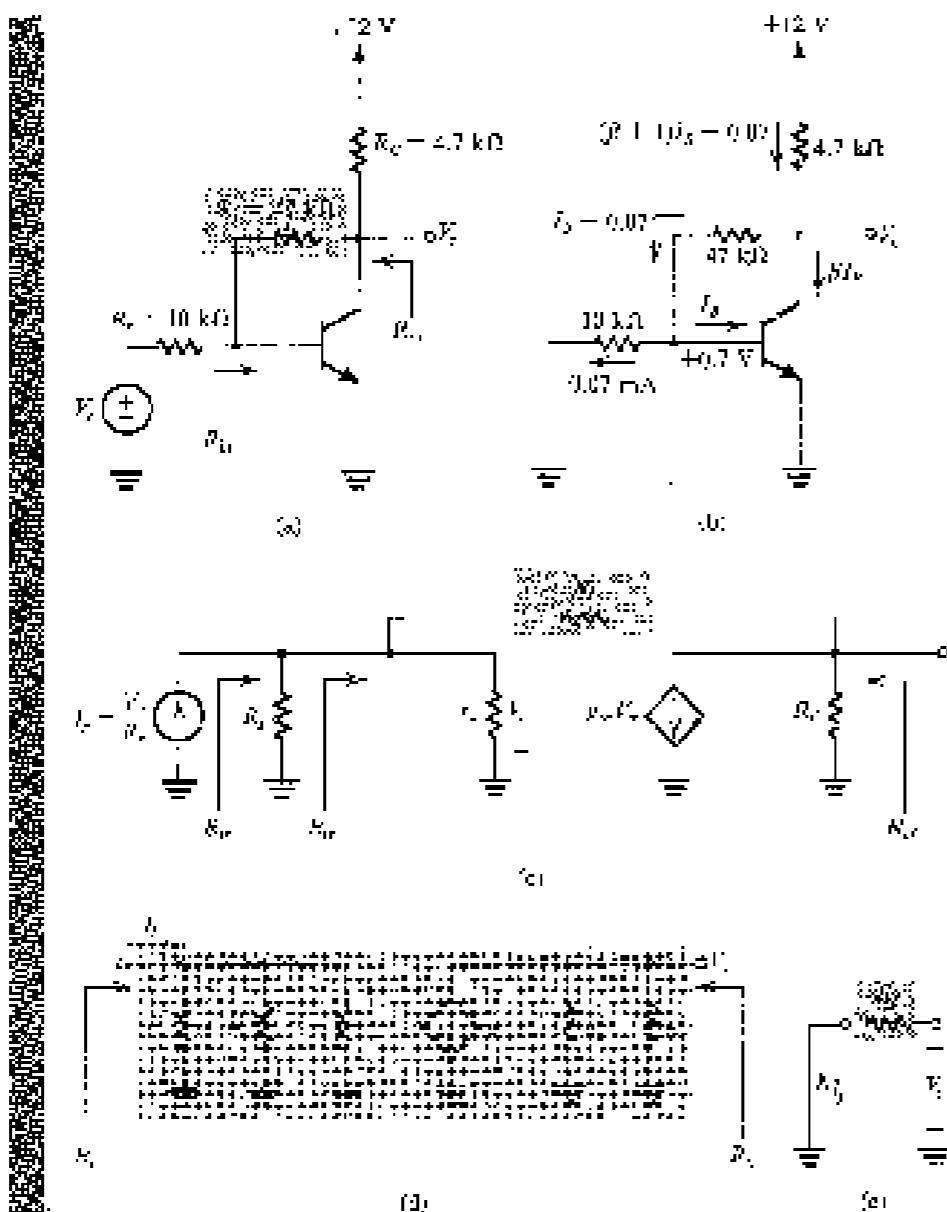


FIGURE 8.21 Circuits for Example 8.2.

Now let us recall the negative action for β has been selected so that I_f subtracts from I_o . The resulting negative sign of β should cause no concern, since A is also negative, keeping the loop gain $A\beta$ positive, as it should be for the feedback to be negative.

We can now obtain A_f for the circuit in Fig. 8.21(c) as

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

$$\frac{V_o}{I_s} = \frac{-358.7}{1 + 358.7/47} = \frac{-358.7}{8.85} = -40.5 \text{ mV}$$

To find the voltage gain V_o/V_s , we note that

$$V_o = I_o R_o$$

Thus

$$\frac{V_o}{V_s} = \frac{I_o}{I_s R_f} = \frac{A/8}{1 + A\beta} = -4.5 \text{ mV}$$

The input resistance with feedback (see Fig. 8.21(b)) is given by

$$R_{in} = \frac{R_i}{1 + A\beta}$$

Thus

$$R_{in} = \frac{10}{8.65} = 1000 \Omega$$

This is the resistance seen by the current source I_f in Fig. 8.21(c). To obtain the input resistance of the feedback amplifier excluding R_f (i.e., the required resistance R_{in}) we subtract $1/R_f$ from $1/R_{in}$ and hence the result gives $R_{in} = 165 \Omega$. Finally, the amplifier output resistance R_{out} is evaluated using

$$R_{out} = \frac{R_o}{1 + A\beta} = \frac{4.7}{8.65} = 0.5 \Omega$$

8.6.2 An important Note

The method we have been employing for the analysis of feedback amplifiers is predicated on two premises: Most of the forward transmission occurs in the basic amplifier, and most of the reverse transmission (feedback) occurs in the feedback network. For each of the three topologies considered thus far, these two assumptions were mathematically expressed as conditions on the relative magnitudes of the forward and reverse two-port parameters of the basic amplifier and the feedback network. Since the circuit considered in Example 8.2 is simple, we have a good opportunity to check the validity of these assumptions.

Reference to Fig. 8.21(d) indicates clearly that the basic amplifier is unilateral; thus all the reverse transmission takes place in the feedback network. The case with forward transmission, however, is not so clear, and we must evaluate the forward γ parameter. For the circuit in Fig. 8.21(b), $\gamma_{21} = g_{se}$ for the feedback network is easily shown to be $\gamma_{21} = -1/R_f$. Thus for our analysis method to be valid we must have $\gamma_{21} \ll 1/R_f$. For the numerical values in Example 8.2, $g_{se} = 60 \text{ mV/V}$ and $1/R_f = 0.02 \text{ mA/V}$, indicating that this assumption is more than justified. Nevertheless, in designing feedback amplifiers, care should be taken in choosing component values to ensure that the two basic assumptions are valid.

8.6.3 The Shunt-Series Configuration

Figure 8.22 shows the ideal structure of the shunt-series feedback amplifier. It is a current amplifier whose gain with feedback is defined as

$$A_f = \frac{I_o}{I_s} = \frac{A}{1 + A\beta} \quad (8.42)$$

The input resistance with feedback is the resistance seen by the current source I_s and is given by

$$R_{in} = \frac{R_i}{1 + A\beta} \quad (8.43)$$

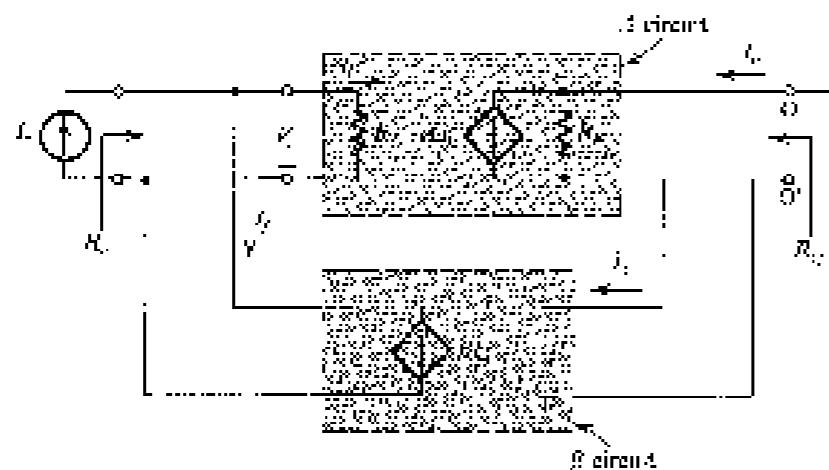


FIGURE 8.22 Ideal structure for the shunt-series feedback amplifier.

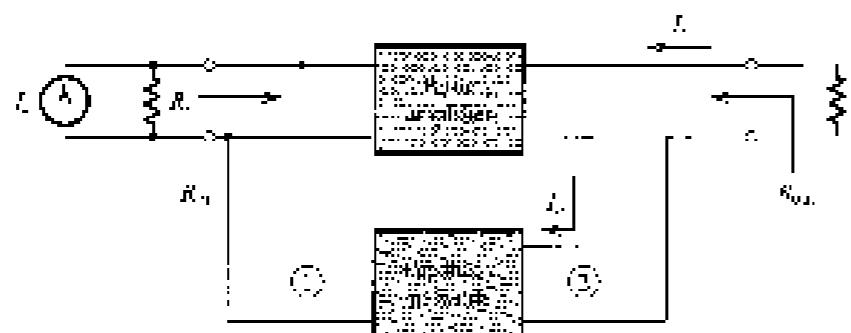


FIGURE 8.23 Block diagram of a practical shunt-series feedback amplifier.

Again we note that the shunt connection at the input reduces the input resistance. The output resistance with feedback is the resistance seen by breaking the output circuit, such as between O and O', and looking between the two terminals thus generated (i.e., between O and O'). This resistance, R_{oF} , is given by

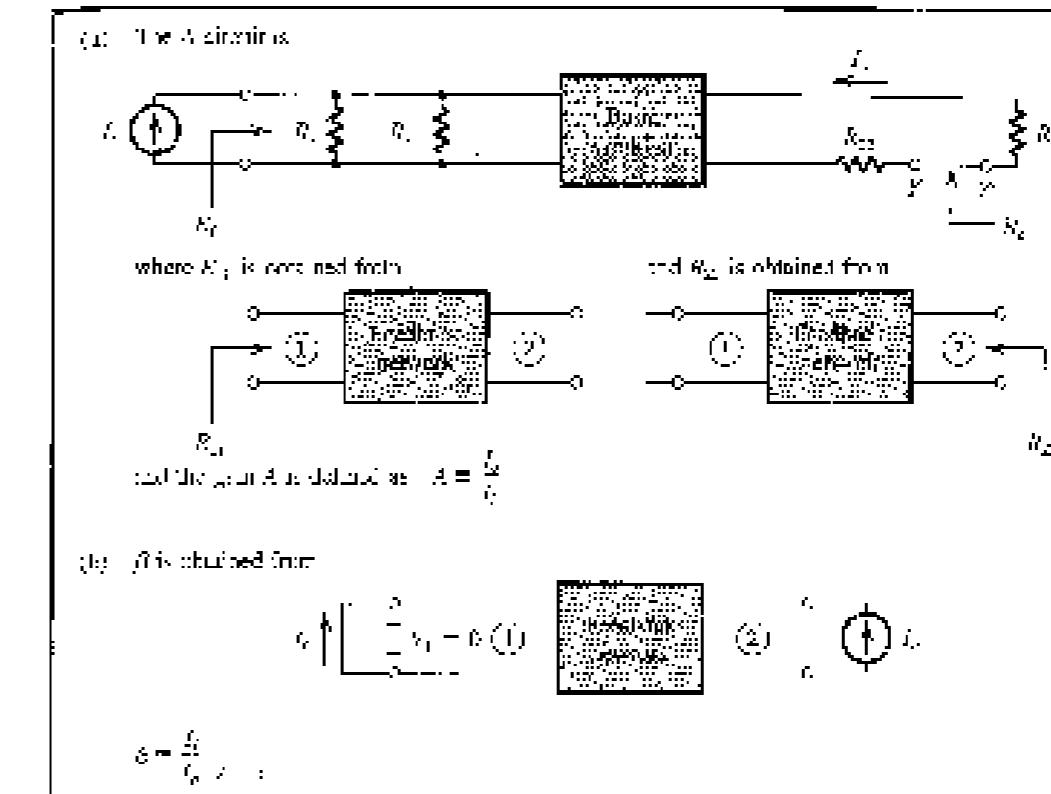
$$R_{oF} = R_o(1 + A\beta) \quad (8.42)$$

where we note that the increase in output resistance is due to the current (series) sampling.

Given a practical shunt-series feedback amplifier, such as the one represented by the block diagram of Fig. 8.23, we follow the method given in Fig. 8.24 in order to obtain α and β . Here again the analysis method is predicated on the assumption that most of the forward transmission occurs in the basic amplifier.²

$$\left. g_{\pi}\right|_{\text{input}} \ll \left. g_{\pi}\right|_{\text{output}} \quad (8.43)$$

² For this coupling topology, the more convenient set of two-port parameters to use is the set of β parameters; it is the only set that provides a representation that is composed of a parallel of one of the input and a series of one of the outputs (see Appendix B).

FIGURE 8.24 Finding the equivalent α -beta circuit for the current-mirror current-sampling shunt-series feedback amplifier of Fig. 8.23.

and most of the inverse transmission takes place in the feedback network;

$$\left. g_{\pi}\right|_{\text{output}} \ll \left. g_{\pi}\right|_{\text{input}} \quad (8.45)$$

Finally, we note that once R_A and R_B have been determined using the feedback equations (Figs. 8.43 and 8.44), the input and output resistances of the amplifier proper, R_i and R_o (Fig. 8.23), can be found as

$$R_i = \left[\frac{1}{\beta} \frac{1}{R_A} \frac{1}{R_B} \right] \quad (8.46)$$

$$R_{oF} = R_o - R_i \quad (8.47)$$

Example 8.10
Figure 8.25 shows a feedback circuit of the shunt-series type. Find I_{oL} , V_{oL} , R_i , and R_{oF} . Assume the transistors to have $\beta = 100$ and $V_A = 75$ V.

Solution

We begin by determining the dc operating points. In this regard, we note that the feedback signal is capacitively coupled; thus the feedback has no effect on dc bias. Neglecting the effect

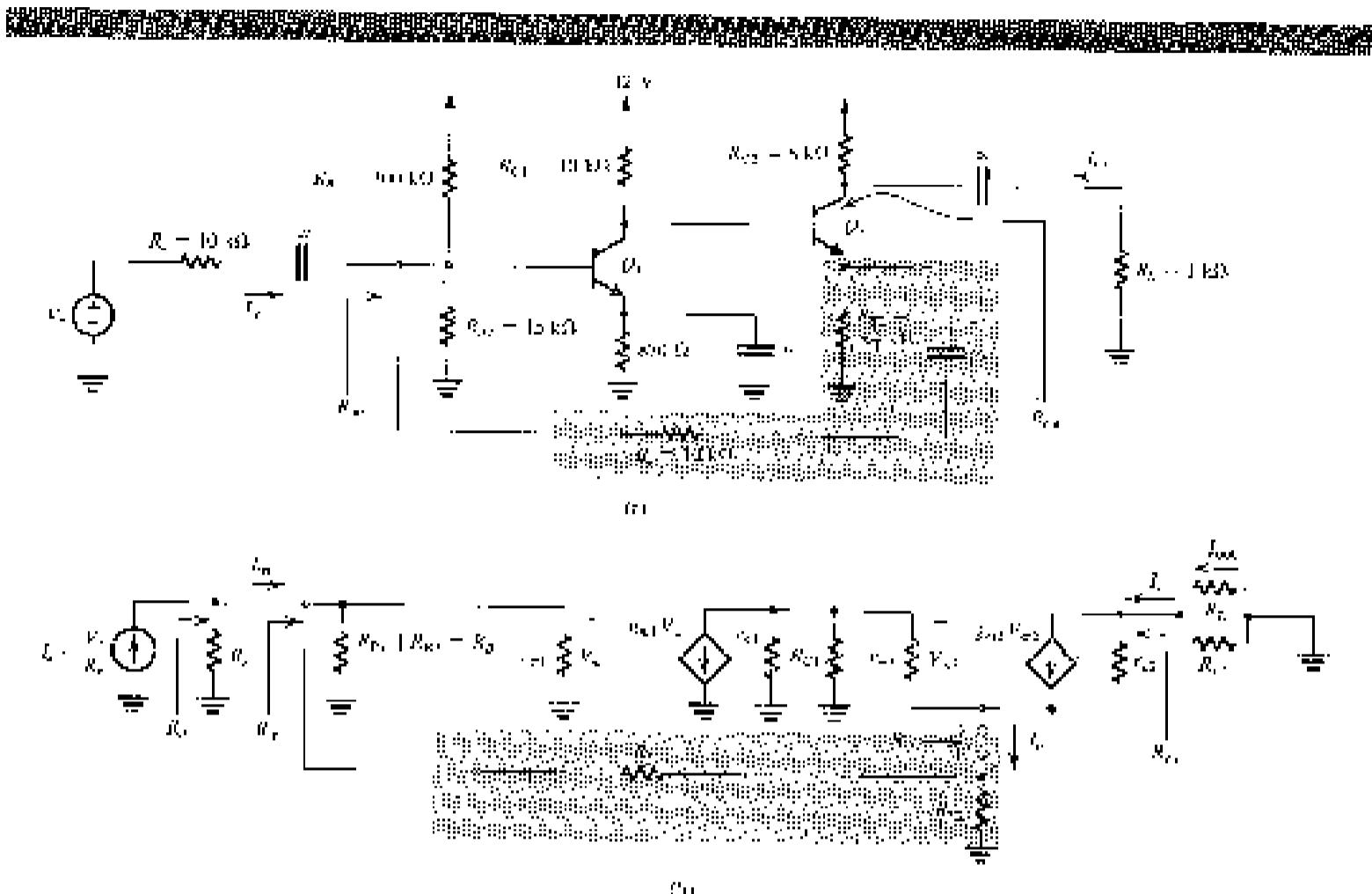


FIGURE 8.25 Circuits for Example 8.4

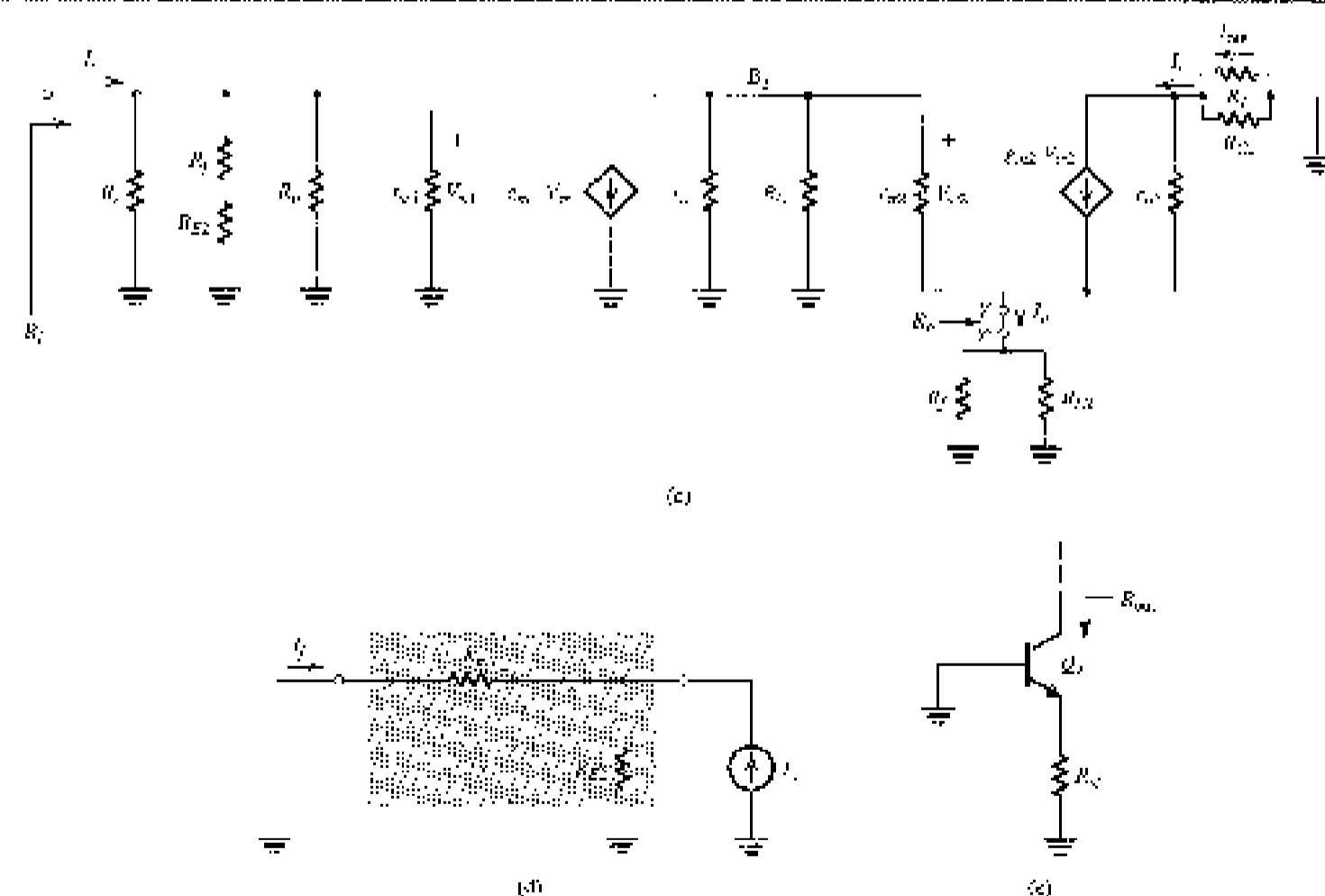


FIGURE 8.25 (Continued)



Feedback Amplifier	A_f	β	$A_f \beta$	Form	At Input	At Output	Feedback Network	I_o	β_f	$\frac{Z_f}{A_f + \beta_f}$	Notes
Series-shunt feedback amplifier	V_o / V_i	$-V_o / I_o$	$-V_o^2 / I_o$	The voltage gain V_o / V_i is negative.	V_o	$-V_o$	By open-circuiting port 2 of feedback network	$I_o = -V_o / R_o$	$\beta_f = -V_o / V_i$	$\frac{R_o}{V_o / V_i + -V_o / V_i}$	V_o / V_i
Shunt-series feedback amplifier	I_o / V_i	$-I_o / V_o$	$-I_o^2 / V_o$	The current gain I_o / V_i is negative.	V_o	$-V_o$	By short-circuiting port 2 of feedback network	$V_o = -I_o R_o$	$\beta_f = -V_o / V_i$	$\frac{R_o}{I_o / V_i + -V_o / V_i}$	I_o / V_i
Shunt-shunt feedback amplifier	V_o / I_o	$-V_o / V_i$	$-V_o^2 / I_o$	The voltage gain V_o / I_o is negative.	V_o	$-V_o$	By short-circuiting port 1 of feedback network	$I_o = -V_o / R_o$	$\beta_f = -V_o / V_i$	$\frac{R_o}{V_o / I_o + -V_o / V_i}$	V_o / I_o

8.6.4 Summary of Results

Table 8.1 provides a summary of the rules and relationships employed in the analysis of the four types of feedback amplifier.

8.7 DETERMINING THE LOOP GAIN

We have already seen that the loop gain $A\beta$ is a very important quantity that characterizes a feedback loop. Furthermore, in the following sections it will be shown that $A\beta$ determines whether the feedback amplifier is stable (as opposed to oscillatory). In this section, we shall describe an alternative approach to the determination of loop gain.

8.7.1 An Alternative Approach for Finding $A\beta$

Consider first the general feedback amplifier shown in Fig. 8.1. Let the external source v_i be set to zero. Open the feedback loop by breaking the connection of x_o to the feedback network and apply a test signal x_t . We see that the signal at the output of the feedback network is $x_o = \beta x_t$, that is, the input of the basic amplifier is $x_i = \beta x_t$, and the signal at the output of the amplifier, where the loop was broken, will be $x_o = -A\beta x_t$. It follows that the loop gain $A\beta$ is given by the negative of the ratio of the reflected signal to the applied test signal; that is, $A\beta = -x_o / x_t$. It should also be obvious that this applies regardless of where the loop is broken.

However, in breaking the feedback loop of a practical amplifier circuit, we must ensure that the conditions that existed prior to breaking the loop are not changed. This is achieved by terminating the loop where it is opened with an impedance equal to that seen before the loop was broken. To be specific, consider the conceptual feedback loop shown in Fig. 8.26(a). If we break the loop at XX' and apply a test voltage V_t to the remainder (thus created to the left of XX'), the terminals at the right of XX' should be loaded with an impedance Z_t , as shown in Fig. 8.26(b). The impedance Z_t is equal to that previously seen looking to the left of XX' . The loop gain $A\beta$ is then determined from

$$A\beta = -\frac{V_t}{V_i} \quad (8.49)$$

Finally, it should be noted that in some cases it may be convenient to determine $A\beta$ by applying a test current I_t and finding the reflected current signal I_o . In this case, $A\beta = -I_o / I_t$.

An alternative equivalent method for determining $A\beta$ (see Rosenstark, 1986) that is particularly convenient to employ, especially in SPICE simulations, is as follows: As before, the loop is broken at a convenient point. Then the open-circuit transfer function T_{oc} is determined as indicated in Fig. 8.26(c), and the short-circuit transfer function T_{sc} is determined as shown in Fig. 8.26(d). These two transfer functions are then combined to obtain the loop gain $A\beta$:

$$A\beta = -\sqrt{\frac{1}{T_{oc}} + \frac{1}{T_{sc}}} \quad (8.50)$$

This method is particularly useful when it is not easy to determine the termination impedance Z_t .

To illustrate the process of determining loop gain, we consider the feedback loop shown in Fig. 8.27(a). This feedback loop represents both the inverting and the non-inverting op-amp

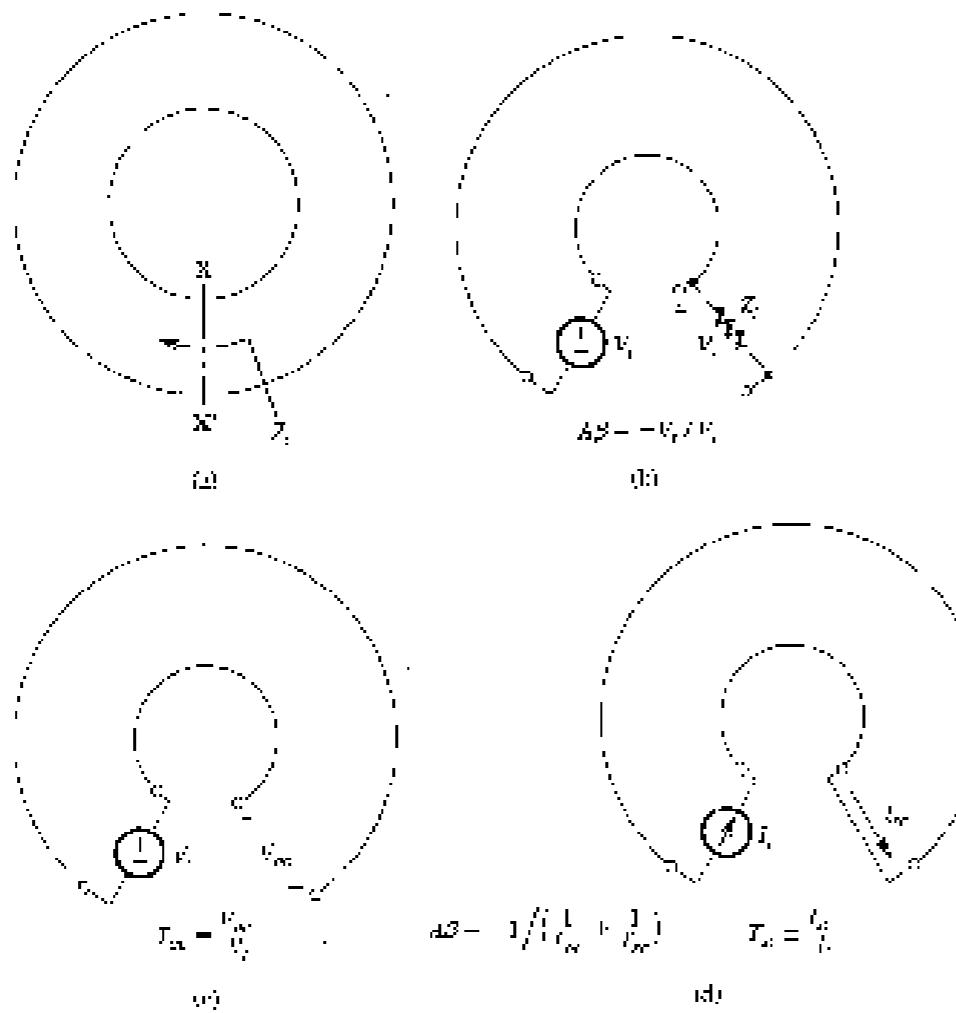


FIGURE 8.26 A negative feedback loop is broken at XX' and a test voltage V_t is applied. The impedance Z_1 is equal to the open-loop voltage looking in the left of XX' . The loop gain $A_0 = -V_o/V_i$, where V_o is the output voltage. As an alternative, after the loop is closed by closing the open terminal, the loop gain is T_{in} , as in (c), and the error-element transfer function T_{err} , as in (d), if you examine them as indicated.

configurations. Using a simple equivalent circuit model for the op-amp we obtain the circuit of Fig. 8.27(b). Examination of this circuit reveals that a convenient place to break the loop is at the input terminals of the op-amp. The loop breaker in this instance is shown in Fig. 8.27(c) with a test signal V_t applied to the right-hand-side terminals and a resistor R_t terminating the left-hand-side terminals. The returned voltage V_r is found by inspection as

$$V_r = -V_t \frac{R_2(R_1 + R_3(R_2 + R_4 + R))}{(R_1(R_2 + R_3(R_2 + R))) + r_s} \frac{1}{1 + R_2(R_2 + R_3) + R_3R_4 + R} = \frac{R_2}{R_1 + R_3 + R_4 + R} V_t \quad (8.51)$$

This equation can be used directly to find the loop gain $L = A_0 = -V_o/V_i = -V_r/V_t$.

Since the loop gain L is generally a function of frequency, it is usual to call it loop transmission and denote it by $L(\omega) \approx L(j\omega)$.

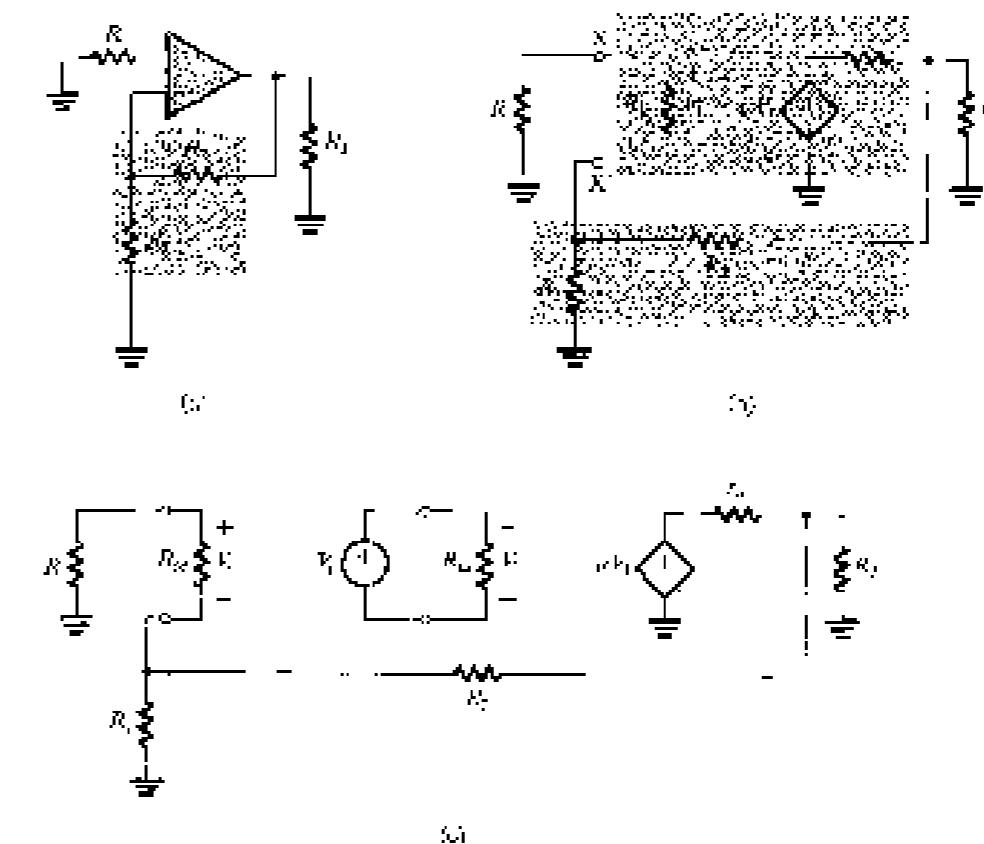


FIGURE 8.27 The loop gain of the feedback loop in (a) is determined in (b) and (c).

8.22 Equivalence of Circuits from a Feedback-Loop Point of View

In the study of circuit theory we know that the poles of a circuit are independent of the external excitation. In fact the poles, or the natural modes (which is a more appropriate name), are determined by setting the external excitation to zero. It follows that the poles of a feedback amplifier depend only on the feedback loop. This will be confirmed in a later section, where we show that the characteristic equation (whose roots are the poles) is completely determined by the loop gain. Thus, a given feedback loop may be used to generate a number of circuits having the same poles but different transmission zeros. The closed-loop gain and the transmission zeros depend on how and where the input signal is injected into the loop.

As an example consider the feedback loop of Fig. 8.27(a). This loop can be used to generate the noninverting op-amp circuit by feeding the input voltage signal to the terminal of R_t that is connected to ground; that is, we lift this terminal off ground and connect it to V_t . The same feedback loop can be used to generate the inverting op-amp circuit by feeding the input voltage signal to the terminal of R_t that is connected to ground.

Recognition of the fact that two or more circuits are equivalent from a feedback-loop point of view is very useful, because it will be shown in Section 8.61 stability is a function of the loop. Thus one needs to perform the stability analysis only once for a given loop.

In Chapter 12 we shall employ the concept of loop equivalence in the synthesis of active filters.

EXERCISES

- 8.1 Consider the feedback amplifier with equivalent circuit as shown in Fig. 8.1. Assume the feedforward network has a gain of 1. Calculate the closed-loop gain $A_f(j\omega)$ at low frequencies, and determine whether the feedback factor is positive or negative. Thus show that the feedback is negative in the analysis.

$$A_f(j\omega) = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)}$$

Using the component values in Example 8.1 and the value of desired output voltage with the value found in Example 8.4, calculate the magnitude of the open-loop gain at low frequencies ($\omega = 10^3 \text{ rad/s}$, Fig. 8.3 versus 8.2),

and for the momentary value of the open-loop gain at break-up ($\omega = 10^5 \text{ rad/s}$, Fig. 8.3 versus 8.2).

By using the momentary value of the open-loop gain at break-up, calculate the magnitude of the closed-loop gain at the frequency of break-up ($\omega = 10^5 \text{ rad/s}$, Fig. 8.3 versus 8.2).

8.6 THE STABILITY PROBLEM**8.6.1 Transfer Function of the Feedback Amplifier**

In a feedback amplifier such as that represented by the general structure of Fig. 8.1, the open-loop gain A is generally a function of frequency, and it should therefore be quite accurately called the **open-loop transfer function**, $A(j\omega)$. Also, we have been assuming for the most part that the feedback network is resistive and hence that the feedback factor β is constant, but this need not be always the case. We shall therefore assume that in the general case the **feedback transfer function** is $\beta(j\omega)$. It follows that the **closed-loop transfer function**, $A_f(j\omega)$, is given by

$$A_f(j\omega) = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)} \quad (8.52)$$

To focus attention on the points central to our discussion in this section, we shall assume that the amplifier is direct-coupled with constant dc gain A_0 and with poles and zeros occurring in the high-frequency band. Also, for the time being let us assume that, at low frequencies, $\beta(j\omega)$ reduces to a constant value. Thus at low frequencies the loop gain $A(j\omega)\beta(j\omega)$ becomes a constant, which should be a positive number; otherwise the feedback would not be negative. The question then is: What happens at higher frequencies?

For very low frequencies $\omega = j\omega_0$, Eq. (8.52) becomes

$$A_f(j\omega_0) = \frac{A(j\omega_0)}{1 + A(j\omega_0)\beta(j\omega_0)} \quad (8.53)$$

Thus the loop gain $A(j\omega)\beta(j\omega)$ is a complex number that can be represented by its magnitude and phase:

$$\begin{aligned} L(j\omega_0) &= A(j\omega_0)\beta(j\omega_0) \\ &= |A(j\omega_0)\beta(j\omega_0)| e^{j\phi(\omega_0)} \end{aligned} \quad (8.54)$$

It is the manner in which the loop gain varies with frequency that determines the stability or instability of the feedback amplifier. To appreciate this fact, consider the frequency at which the phase angle $\phi(j\omega)$ becomes 180° . At this frequency, since the loop gain $A(j\omega)\beta(j\omega)$ will be a real number with a negative sign, thus at this frequency the feedback will become positive. If at $\omega = \omega_{\text{un}}$, the magnitude of the loop gain is less than unity, then from Eq. (8.53) we see that the closed-loop gain $A_f(j\omega)$ will be greater than the open-loop gain $A(j\omega)$, since the denominator of Eq. (8.52) will be smaller than unity. Nevertheless, the feedback amplifier will be stable.

On the other hand, if at the frequency ω_{un} the magnitude of the loop gain is equal to unity, it follows from Eq. (8.53) that $A_f(j\omega)$ will be infinite. This means that the amplifier will have an output for zero input; this is by definition an oscillator. To visualize how this feedback loop may oscillate, consider the general form of Fig. 8.1 with the external input x set to zero. Any disturbance in the circuit such as the closure of the power-supply switch, will generate a signal, x_1 , at the input to the amplifier. Such a noise signal usually contains a wide range of frequencies, and we shall now concentrate on the component with frequency $\omega = \omega_{\text{un}}$, that is, the signal $X_1 \sin(\omega_{\text{un}}t)$. This input signal will result in a feedback signal given by

$$A_f = A(j\omega_{\text{un}})\beta(j\omega_{\text{un}})X_1 = -X_1$$

Since X_1 is further multiplied by -1 in the inverter block of the input, we see that the feedback causes the signal X_1 at the amplifier input to be reinforced. That is, from this point on, there will be sinusoidal signals at the amplifier input and output of frequency ω_{un} . Thus the amplifier is said to oscillate at the frequency ω_{un} .

The question now is: What happens if at ω_{un} the magnitude of the loop gain is greater than unity? We shall answer this question, not in general, but for the restricted yet very important class of circuits in which we are interested here. The answer, which is not obvious from Eq. (8.53), is that the circuit will oscillate, and the oscillations will grow in amplitude until some nonlinearity (which is always present in some form) reduces the magnitude of the loop gain to exactly unity, at which point sustained oscillations will be obtained. This mechanism for starting oscillations by using positive feedback with a loop gain greater than unity, and then using a nonlinearity to reduce the loop gain to unity at the desired amplitude, will be exploited in the design of sinusoidal oscillators in Chapter 13. Our objective here is just the opposite: Now that we know how oscillations could occur in a negative-feedback amplifier, we wish to find methods to prevent their occurrence.

8.6.2 The Nyquist Plot

The Nyquist plot is a normalized approach for testing for stability based on the discussion above. It is simply a polar plot of loop gain with frequency used as a parameter. Figure 8.28 shows such a plot. Note that the radial distance is $|A(j\omega)|$ and the angle is the phase angle ϕ . The solid-line plot is for positive frequencies. Since the loop gain—not for that matter any gain function of a physical network—has a magnitude that is an even function of frequency and a phase that is an odd function of frequency, the $A(j\omega)$ plot for negative frequencies (shown in Fig. 8.28 as a broken line) can be drawn as a mirror image through the $\text{Re}\omega$ axis.

The Nyquist plot intersects the negative real axis at the frequency ω_{un} . Thus, if this intersection occurs to the left of the point $(-1, 0)$, we know that the magnitude of loop gain at this frequency is greater than unity and the amplifier will be unstable. On the other hand, if the intersection occurs to the right of the point $(-1, 0)$ the amplifier will be stable. It follows that if the Nyquist plot encircles the point $(-1, 0)$ then the amplifier will be

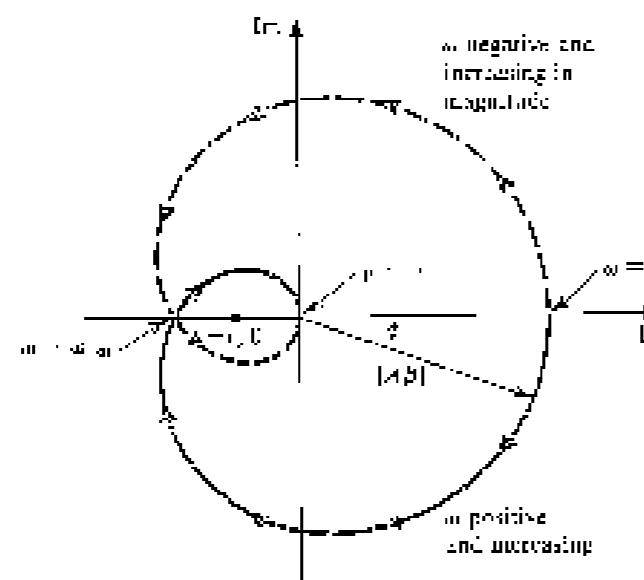


FIGURE 8.28 The Nyquist plot of an unstable amplifier.

instability. It should be mentioned, however, that this statement is a simplified version of the Nyquist criterion; nevertheless, it applies to all the circuits in which we are interested. For the full theory behind the Nyquist method and its details of its application, see Bell (1970).

EXERCISE

A feedback circuit has a gain that is proportional to the frequency, $A(\omega) = \omega^2$. If the feedback factor is constant independent of frequency, find the frequency at which the phase shift is 180°, assuming the feedback will start to oscillate when the phase shift reaches 180°. Assume the feedback factor is +1, and the output voltage is zero at $\omega = 0$. The output voltage is given by $V_o = V_i e^{j\omega t} / (1 + A(\omega))$.

8.9 EFFECT OF FEEDBACK ON THE AMPLIFIER POLES

The amplifier frequency response and stability are determined directly by its poles. We shall therefore investigate the effect of feedback on the poles of the amplifier.⁶

⁶ For a short review of poles and zeros and related concepts, refer to Appendix A.

8.9.1 Stability and Pole Location

We shall begin by considering the relationship between stability and pole location. For an amplifier or any other system to be stable, its poles should lie in the left half of the s plane. A pair of complex-conjugate poles on the σ axis gives rise to sustained sinusoidal oscillations. Poles in the right half of the s plane give rise to growing oscillations.

To verify the statement above, consider an amplifier with a pole pair at $\sigma = \sigma_c, \pm j\omega_c$. If this amplifier is subjected to a disturbance, such as the caused by a noise of the power-supply switch, its transient response will contain terms of the form

$$v(t) = e^{\sigma_c t} [e^{j\omega_c t} + e^{-j\omega_c t}] = 2e^{\sigma_c t} \cos(\omega_c t) \quad (8.57)$$

This is a sinusoidal signal with an envelope $e^{\sigma_c t}$. Now if the poles are in the left half of the s plane, then σ_c will be negative and the oscillations will decay exponentially toward zero, as shown in Fig. 8.29(a), indicating that the system is stable. If, on the other hand, the poles are in the right half-plane, then σ_c will be positive, and the oscillations will grow exponentially,

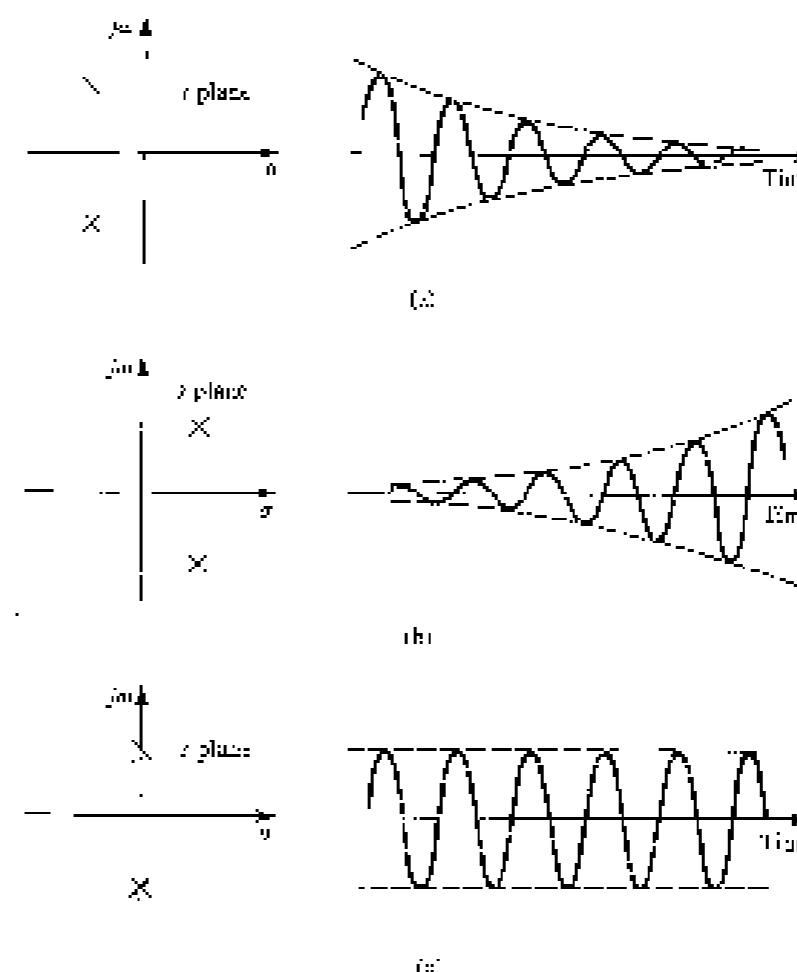


FIGURE 8.29 The relationship between pole location and transient response.

until some nonlinearity limits their growth, as shown in Fig. 8.26(c). Finally, if the poles are on the $j\omega$ axis, then σ_c will be zero and the oscillations will be sustained, as shown in Fig. 8.26(e).

Although the discussion above is in terms of complex-conjugate poles, it can be shown that the existence of any right-half-plane poles results in instability.

8.9.2 Poles of the Feedback Amplifier

From the closed-loop transfer function in Eq. (8.52), we see that the poles of the feedback amplifier are the zeros of $1 + A(s)\beta(s)$. That is, the feedback-amplifier poles are obtained by solving the equation

$$1 + A(s)\beta(s) = 0 \quad (8.56)$$

which is called the characteristic equation of the feedback loop. It should therefore be apparent that applying feedback to an amplifier changes its poles.

In the following, we shall consider how feedback affects the amplifier poles. For this purpose we shall assume that the open-loop amplifier has real poles and no finite zeros (i.e., all the zeros are at $s = \infty$). This will simplify the analysis and enable us to focus our attention on the fundamental concepts involved. We shall also assume that the feedback factor β is independent of frequency.

8.9.3 Amplifier with a Single-Pole Response

Consider first the case of an amplifier whose open-loop transfer function is characterized by a single pole:

$$A(s) = \frac{A_0}{1 + s/\omega_p} \quad (8.57)$$

The closed-loop transfer function is given by

$$A_c(s) = \frac{A_0/(1 + A_0\beta)}{1 + s/\omega_p(1 + A_0\beta)} \quad (8.58)$$

Thus the feedback moves the pole along the negative real axis to a frequency ω_{pf} ,

$$\omega_{pf} = \omega_p(1 + A_0\beta) \quad (8.59)$$

This process is illustrated in Fig. 8.30. Figure 8.30(a) shows Bode plots for A_0 and A_c . Note that while at low frequencies the difference between the two plots is $20 \log(1 + A_0\beta)$, the two curves coincide at high frequencies. One can show that this indeed is the case by approximating Eq. (8.58) for frequencies $\omega \gg \omega_p(1 + A_0\beta)$:

$$A_c(s) \approx \frac{A_0\beta}{s} \approx A(s) \quad (8.60)$$

Physically speaking, at such high frequencies the loop gain is much smaller than unity and the feedback is ineffective.

Figure 8.30(b) clearly illustrates the fact that applying negative feedback to an amplifier results in extending its bandwidth at the expense of a reduction in gain. Since the poles of the closed-loop amplifier never enter the right half of the s -plane, the single-pole amplifier is stable for any value of β . Thus this amplifier is said to be unconditionally stable. This

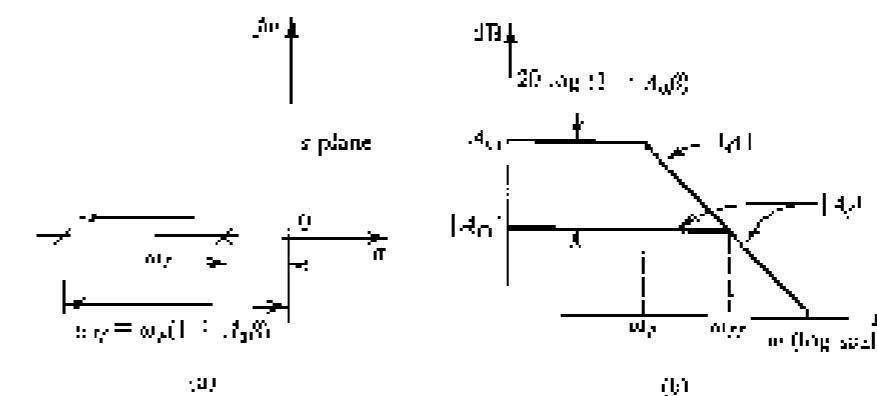


FIGURE 8.30 Effect of feedback on (a) the pole locus and (b) the frequency response of an amp with a single-pole open-loop response.

result, however, is mainly surprising, since the phase lag associated with a single-pole response can never be greater than 90° . Thus the loop gain never achieves the 180° phase shift required for the feedback to become positive.

EXERCISE

- 8.11 An open-loop $A(s) = 10^4/s$ single-pole system (Fig. 8.30) is fed back with $\beta = 0.7$. What is the factor by which feedforward shifts the pole? To what frequency is β increased so that the $20 \log(1 + A_0\beta)$ value that results in delayed onset of saturation frequency decreases in half?

8.9.4 Amplifier with Two-Pole Response

Consider next an amplifier whose open-loop transfer function is characterized by two real poles:

$$A(s) = \frac{A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \quad (8.61)$$

In this case, the closed-loop poles are obtained from $1 + A(s)\beta = 0$, which leads to

$$s^2 + s(\omega_{p1} + \omega_{p2}) + (1 + A_0\beta)\omega_{p1}\omega_{p2} = 0 \quad (8.62)$$

Thus the closed-loop poles are given by

$$s = -\frac{1}{2}(\omega_{p1} + \omega_{p2}) \pm \frac{1}{2}\sqrt{(\omega_{p1} - \omega_{p2})^2 + 4(1 + A_0\beta)\omega_{p1}\omega_{p2}} \quad (8.63)$$

From Eq. (8.63) we see that as the loop gain $A_0\beta$ is increased from zero, the poles are brought closer together. When a value of loop gain is reached at which the poles become coincident, if the loop gain is further increased, the poles become complex conjugate and move along a vertical line. Figure 8.31 shows the locus of the poles for increasing loop gain. This plot is called a root-locus diagram, where "root" refers to the fact that the poles are the roots of the characteristic equation.

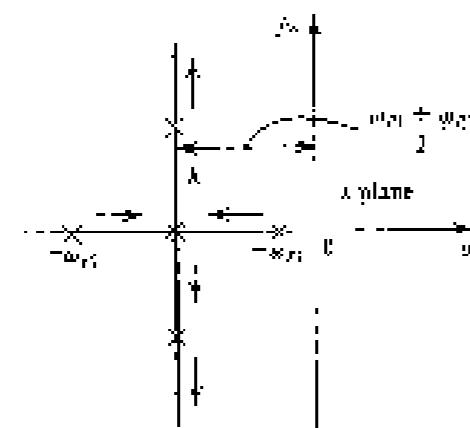


FIGURE 8.31 Root-locus diagram for a feedback amplifier where the open-loop transfer function has no real poles.

From the root-locus diagram of Fig. 8.31 we see that this feedback amplifier also is unconditionally stable. Again this result should come as no surprise; the maximum phase shift of 45° in this case is 180°/200° per pole, but this value is reached at $\omega = \infty$. Thus there is no finite frequency at which the phase shift reaches 180°.

Another observation to make on the root-locus diagram of Fig. 8.31 is that the open-loop amplifier might have a dominant pole, but this is not necessarily the case for the closed-loop amplifier. The response of the closed-loop amplifier can, of course, always be plotted once the poles have been found from Eq. (8.67). As is the case with second-order responses generally, the closed-loop response can show a peak (see Chapter 12). To be more specific, the characteristic equation of a second-order network can be written in the standard form

$$s^2 + s \frac{\omega_0}{Q} + \omega_0^2 = 0 \quad (8.68)$$

where ω_0 is called the pole frequency and Q is called pole Q factor. The poles are complex if Q is greater than 0.5. A geometric interpretation for ω_0 and Q of a pair of complex-conjugate poles is given in Fig. 8.32, from which we note that ω_0 is the radial distance of the poles from the origin and that Q indicates the distance of the poles from the $j\omega$ axis. Poles on the $j\omega$ axis have $Q = \infty$.

By comparing Eqs. (8.67) and (8.68) we obtain the Q factor for the poles of the feedback amplifier as

$$Q = \frac{\sqrt{1 + A_{\text{fb}}(\beta)} \omega_p \omega_z}{\omega_p - \omega_z} \quad (8.69)$$

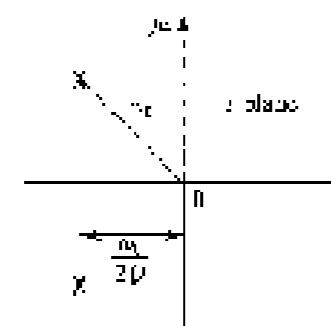


FIGURE 8.32 Definition of λ and Q of a pair of complex-conjugate poles.

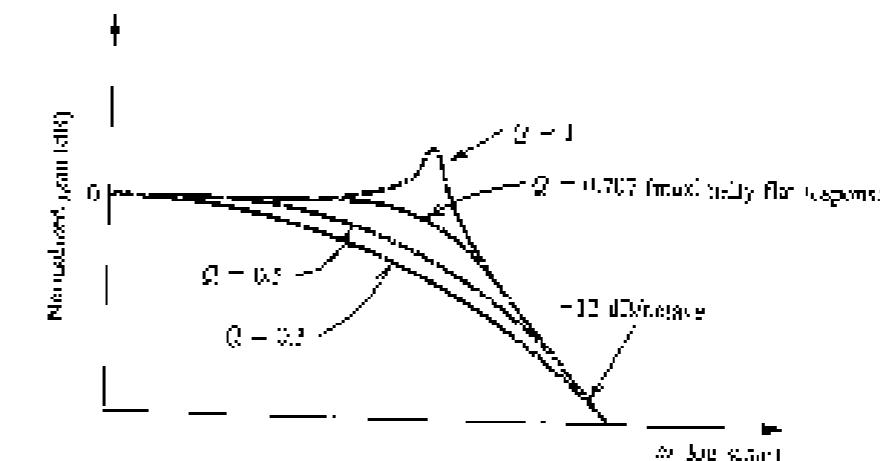


FIGURE 8.33 Normalized gain of a two-pole feedback amplifier for various values of Q . Note that Q is determined by the loop gain according to Eq. (8.69).

From the study of second-order network responses in Chapter 12, it will be seen that the response of the feedback amplifier under consideration shows no peaking for $Q \leq 0.707$. The boundary case corresponding to $Q = 0.707$ (poles at 45° angles) results in the maximally flat response. Figure 8.33 shows a number of possible responses obtained for various values of Q (or, correspondingly, various values of $A_{\text{fb}}(\beta)$).

EXERCISE

8.12 Consider a circuit with voltage-controlled voltage source V_{ctrl} and two dependent current-controlled voltage sources V_{ctrl} and V_{ctrl} , as shown in Fig. 8.34(a). Find the loop transmission $A_{\text{fb}}(\beta)$ and the characteristic equation. Sketch a root-locus diagram for varying K_{ctrl} and find the value of K_{ctrl} at which the circuit oscillates, and the value of K_{ctrl} at which the circuit oscillates. Assume that the amplifier has infinite input impedance and zero output impedance.

As an illustration of some of the ideas just discussed, we consider the positive-feedback circuit shown in Fig. 8.34(c). Find the loop transmission $A_{\text{fb}}(\beta)$ and the characteristic equation. Sketch a root-locus diagram for varying K_{ctrl} and find the value of K_{ctrl} at which the circuit oscillates, and the value of K_{ctrl} at which the circuit oscillates. Assume that the amplifier has infinite input impedance and zero output impedance.

Solution

To obtain the loop transmission we short-circuit the signal source and break the loop at the amplifier input. We then apply a test voltage V_i and find the internal voltage V_o , as indicated in

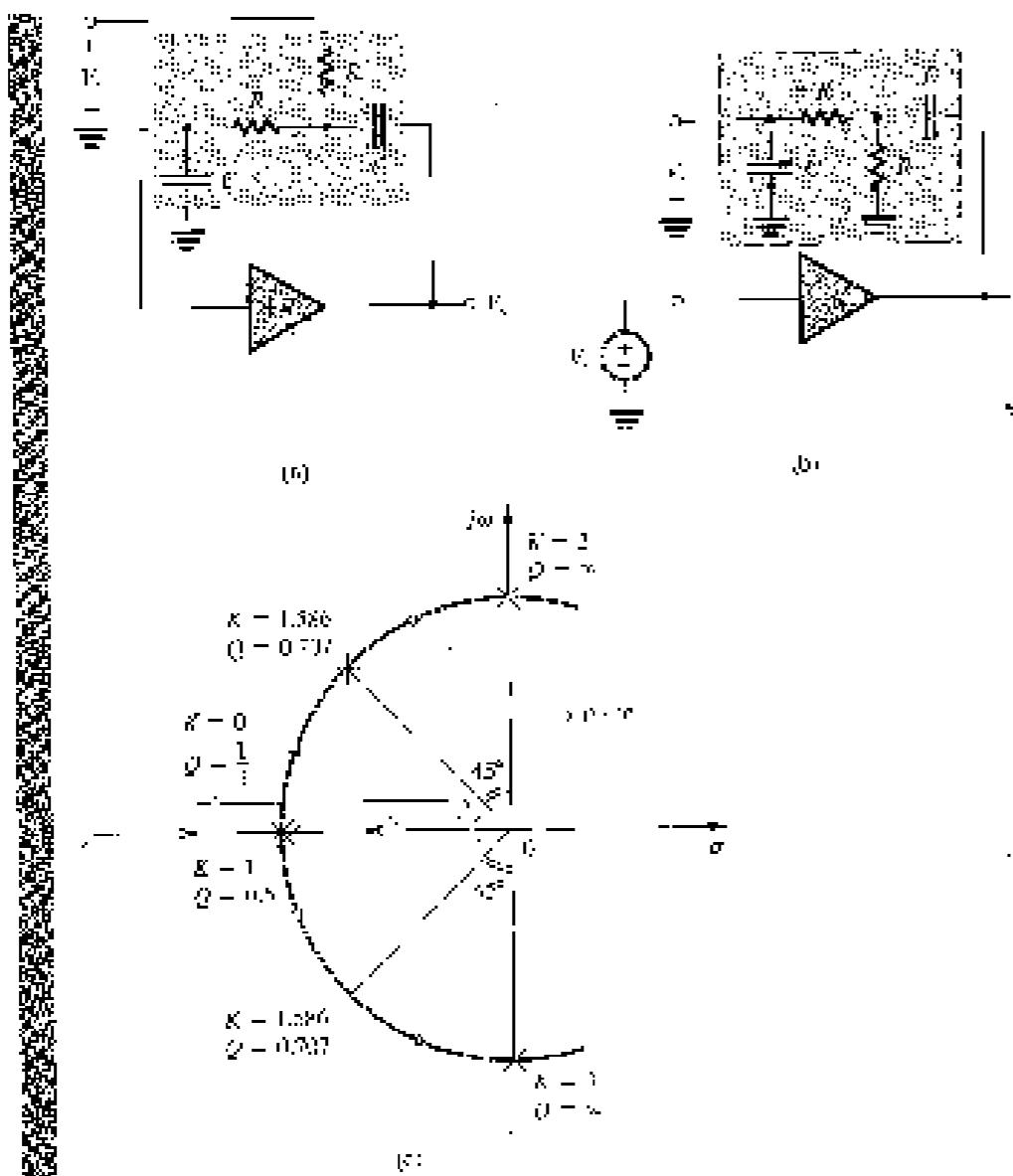


FIGURE 8.34 Circuit and plot for Example 8.5.

(Fig. 8.31(b)). The loop transmission $L(s) = A(s)\beta(s)$ is given by

$$L(s) = -\frac{V_o}{V_i} = -\beta T(s) \quad (8.66)$$

where $T(s)$ is the transfer function of the two-part RC network shown inside the broken-line box in Fig. 8.34(b).

$$T(s) = \frac{V_o}{V_i} = \frac{\alpha(1/sC)}{s^2 + s(\beta/C) + (1/\alpha R)} \quad (8.67)$$

Topic:

$$L(s) = \frac{\alpha R/(CR)}{s^2 + s(\beta/C) + (1/\alpha R)} \quad (8.68)$$

The characteristic equation is

$$(1) L(s) = 0 \quad (8.69)$$

that is,

$$\begin{aligned} s^2 + s(\beta/C) + \frac{\alpha R}{CR} + \frac{1}{\alpha R} &= 0 \\ s^2 + \frac{\beta}{CR} + \frac{1}{\alpha R} &= 0 \end{aligned} \quad (8.70)$$

By comparing this equation to the standard form of the second-order characteristic equation (Eq. 8.64) we see that the pole frequency ω_0 is given by

$$\omega_0 = \frac{1}{CR} \quad (8.71)$$

and the Q factor is

$$Q = \frac{1}{\beta - \alpha} \quad (8.72)$$

Thus, for $K = 0$ the poles have $Q = \frac{1}{2}$ and are therefore located on the negative real axis. As K is increased, the poles are brought closer together and eventually collide ($Q = 0.5$, $K = 1$). Further increasing K results in the poles becoming complex and conjugate. The pole locus is then a circle because the radial distance ω_0 remains constant (Eq. 8.71) independent of the value of K .

The maximally flat response is obtained when $Q = 0.707$, which results when $K = 1.386$. In this case the poles are at 45° angles, as indicated in Fig. 8.34(c). The poles cross the $j\omega$ -axis into the right half of the s -plane at the value of K that results in $Q = \infty$, that is, $K = 3$. Thus for $K > 3$ this circuit becomes unstable. This might appear to contradict our earlier conclusion that the feedback amplifier with a second-order response is inherently stable. Well, however, the circuit in this example is quite different from the negative-feedback amplifier that we have been studying. Here we have an amplifier with a positive gain K and a feedback network whose transfer function $T(s)$ is frequency dependent. The feedback is in fact positive, and the circuit will oscillate at the frequency for which the phase of $A(s)$ is zero.

Example 8.5 illustrates the use of feedback (positive feedback in this case) to move the poles of an I_C network from their negative real-axis locations to complex-conjugate locations. One can accomplish the same task using negative feedback, as the two-loop diagram of Fig. 8.31 demonstrates. The process of pole control is the essence of active filter design, as will be discussed in Chapter 12.

8.9.5 Amplifiers with Three or More Poles

Figure 8.35 shows the two-loop diagram for a feedback amplifier whose open-loop response is characterized by three poles. As indicated, increasing the loop-gain term $\alpha\beta$ moves the highest-frequency pole outward while the two other poles are brought closer together. As $\alpha\beta$ is increased further, the two poles become coincident and then become complex and conjugate. A value of $\alpha\beta$ exists at which this pair of complex-conjugate poles enters the right half of the s -plane, thus causing the amplifier to become unstable.

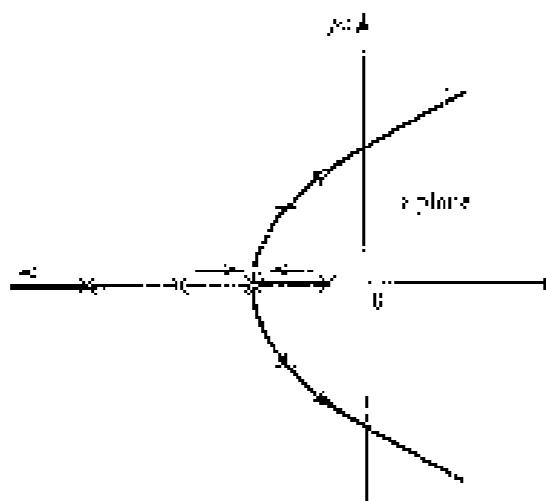


FIGURE 8.35 Root locus diagram in the complex plane with three poles. The locus indicates the pole locations as A_B is increased.

This result is not entirely unexpected, since an amplifier with three poles has a phase shift that reaches -270° as ω approaches ω_c . Thus there exists a finite frequency ω_{inst} at which the loop gain has 180° phase shift.

From the root locus diagram of Fig. 8.35, we observe that one can always maintain amplifier stability by keeping the loop gain A_B smaller than the value corresponding to the poles entering the right half-plane. In terms of the Nyquist diagram, the critical value of A_B is that for which the diagram passes through the $(-1, 0)$ point. Reducing A_B below this value causes the Nyquist plot to shift and thus intersect the negative real axis to the right of the $(-1, 0)$ point, indicating unstable amplifier performance. On the other hand, increasing A_B above the critical value causes the Nyquist plot to expand, thus encircling the $(-1, 0)$ point and indicating unstable performance.

For a given open-loop gain A_0 , the conclusions above can be stated in terms of the feedback factor β . That is, there exists a maximum value for β above which the feedback amplifier becomes unstable. Alternatively, we can state that there exists a minimum value for the closed-loop gain A_L below which the amplifier becomes unstable. To obtain lower values of closed-loop gain one needs, therefore, to filter the loop transfer function, $L(j\omega)$. This is the process known as *frequency compensation*. We shall study the theory and techniques of frequency compensation in Section 8.11.

Before leaving this section we point out that construction of the root locus diagram for amplifiers having four or more poles as well as finite zeros is an involved process for which a systematic procedure exists. However, such a procedure will not be presented here, and the interested reader should consult Haykin (1970). Although the root-locus diagram provides the amplifier designer with considerable insight, other, simpler techniques based on Bode plots can be effectively employed, as will be explained in Section 8.10.

In this section we shall study the stability of feedback amplifiers using Bode plots. We shall also discuss the effect of frequency-dependent feedback devices such as showband oscillators in detail. Next, we shall show how the value of β at which the amplifier becomes unstable varies with the number of poles. Finally, we shall introduce the margins considered in Fig. 8.36.

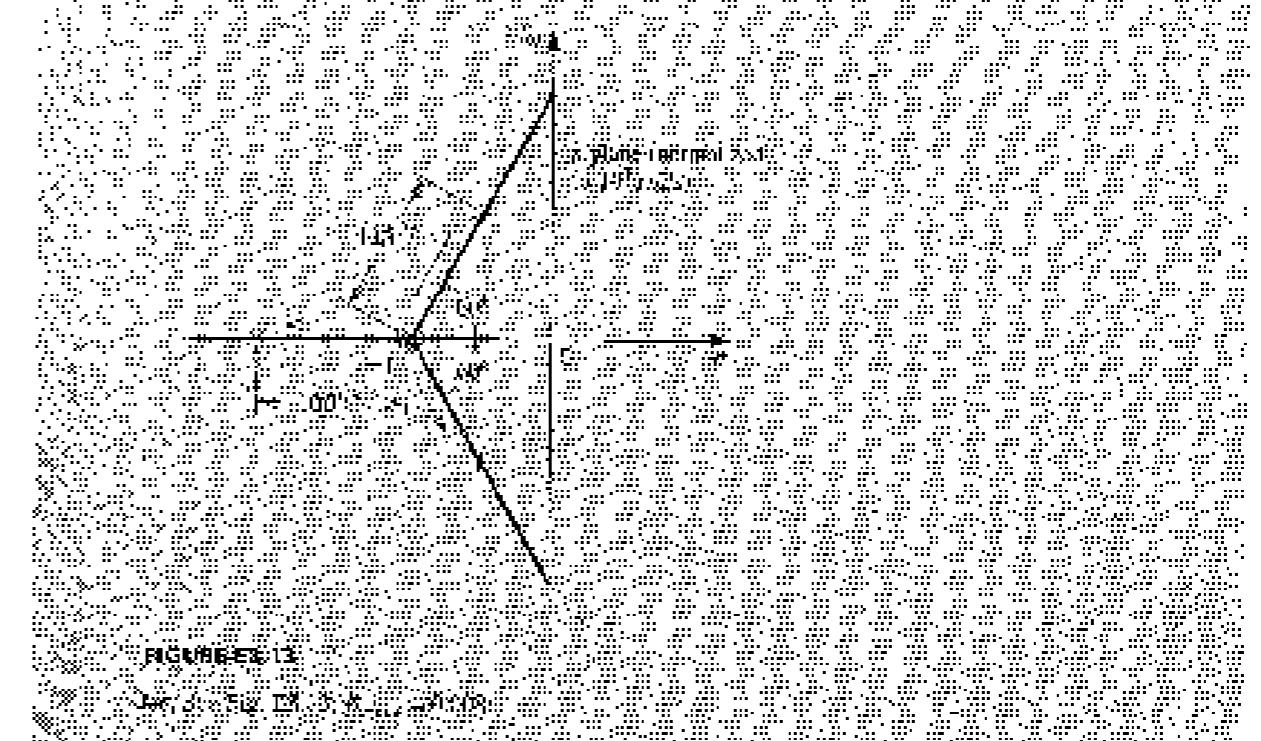


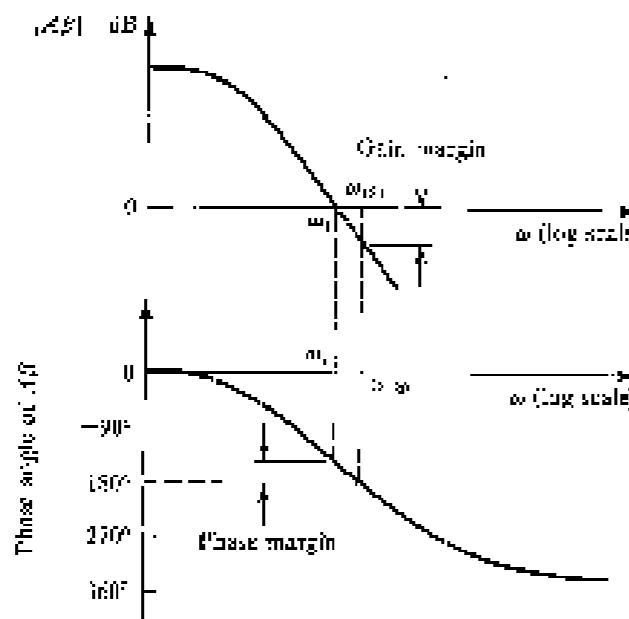
FIGURE 8.36

8.10 STABILITY STUDY USING BODE PLOTS

8.10.1 Gain and Phase Margins

From Sections 8.8 and 8.9 we know that one way to determine whether a feedback amplifier is or is not stable is by examining its loop gain A_B as a function of frequency. One of the simplest and most effective means for doing this is through the use of a Bode plot for A_B , such as the one shown in Fig. 8.36. Note that, because the phase approaches -270° , the network examined is a fourth-order one. The feedback amplifier whose loop gain is plotted in Fig. 8.36 will be stable, since at the frequency of 180° phase shift, ω_5 , the magnitude of the loop gain is less than unity (negative dB). The difference between the value of $|A_B|$ at ω_5 , and unity, called the *gain margin*, is usually expressed in decibels. The gain margin represents the amount by which the loop gain can be increased while stability is maintained. Feedback amplifiers are usually designed to have sufficient gain margin to allow for inevitable changes in loop gain with temperature, time, and so on.

Another way to investigate the stability and to express its degree is to examine the bode plot at the frequency for which $|A_B| = 1$, which is the point at which the magnitude plot crosses the 0-dB line. If at this frequency the phase angle is less than a magnitude that 180° , then the amplifier is stable. This is the situation illustrated in Fig. 8.36. The difference between the phase angle at this frequency and 180° is termed the *phase margin*. On the

FIGURE 8.56 Bode plots for the loop gain $A(j\omega)$ illustrating the definitions of the gain and phase margins.

other hand, if at the frequency of unity-loop-gain magnitude, the phase lag is in excess of 180° , the amplifier will be unstable.

EXERCISE

- E.14 Consider an amplifier with a single-pole open-loop transfer function $A(j\omega) = 10 \cdot 0.1 \omega_1^2 / (j\omega + \omega_1^2)$, where $\omega_1 = 10 \text{ rad/s}$. At what value of the input signal current i_{in} does the amplifier become unstable? Assume the noninverting terminal has a nominal low-frequency open-loop gain of 1000, and the feedback voltage amplitude is 14.0 mV . Also, find the closed-loop gain.

8.10.2 Effect of Phase Margin on Closed-Loop Response

Feedback amplifiers are normally designed with a phase margin of at least 45° . The amount of phase margin has a profound effect on the shape of the closed-loop step response. To see this relationship, consider a feedback amplifier with a large low-frequency loop gain, $A(j\omega) \gg 1$. It follows that the closed-loop gain at low frequencies is approximately $1/\beta$. Denoting the frequency at which the magnitude of loop gain is unity by ω_1 , we have (refer to Fig. 8.36)

$$|A(j\omega_1)\beta| = 1 \times 10^{-6} \quad (8.73a)$$

where

$$\theta = -60^\circ - \text{phase margin} \quad (8.73b)$$

At ω_1 the closed-loop gain is

$$A_L(j\omega_1) = \frac{A(j\omega_1)}{1 + A(j\omega_1)\beta} \quad (8.74)$$

Substituting from Eq. (8.73b) gives

$$A_L(j\omega_1) = \frac{(1/\beta)e^{j\theta}}{1 + e^{j\theta}} \quad (8.75)$$

Hence the magnitude of the gain at ω_1 is

$$|A_L(j\omega_1)| = \frac{1/\beta}{1 + e^{j\theta}} \quad (8.76)$$

Next phase margin $\theta = 60^\circ$, $\theta = 135^\circ$, and we obtain

$$|A_L(j\omega_1)| = 1.3 \frac{1}{\beta} \quad (8.77)$$

This is the gain peaks by a factor of 1.3 above the low-frequency value of $1/\beta$. This means the required phase margin is reduced, eventually reaching ω_1 when the phase margin is zero. Zero phase margin, of course, implies that the amplifier can't satisfy specifications (poles on the j-axis; Nyquist plot passing through $(-1, 0)$).

EXERCISE

- E.15 Using the closed-loop gain $A_L(j\omega)$ evaluate the low-frequency gain margin for the circuit of Fig. 8.36, assuming $\omega_1 = 10 \text{ rad/s}$, $\beta = 1000$, and $A(j\omega) = 10^6$.

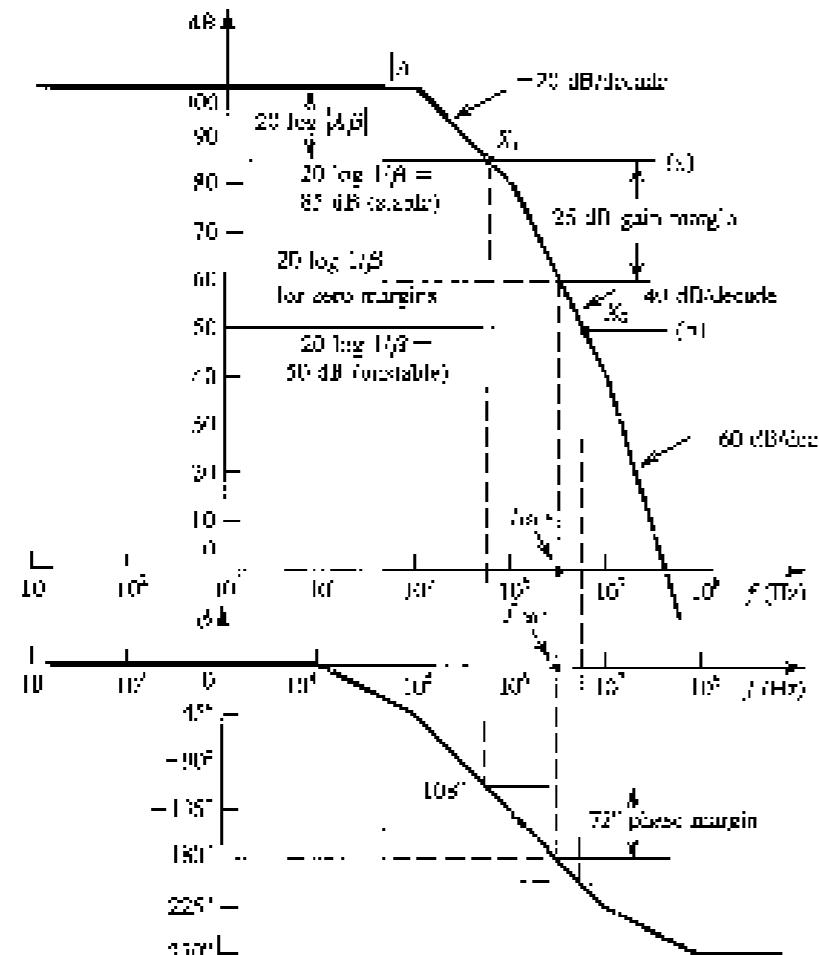
8.10.3 An Alternative Approach for Investigating Stability

Investigating stability by constructing Bode plots for the loop gain $A(j\omega)$ can be a tedious and time-consuming process, especially if we have to investigate the stability of a given amplifier for a variety of feedback networks. An alternative approach, which is much simpler, is to construct a Bode plot for the open-loop gain $A(j\omega)$ only. Assuming for the time being that β is independent of frequency, we can plot $20 \log(1/\beta)$ as a horizontal straight line on the same plane used for $20 \log(A(j\omega))$. The difference between the two curves will be

$$20 \log(A(j\omega)) - 20 \log \frac{1}{\beta} = 20 \log(1/\beta) \quad (8.78)$$

which is the loop gain (in dB). We may therefore study stability by examining the difference between the two plots. If we wish to evaluate stability for a different feedback factor we simply draw another horizontal straight line at the level $20 \log(1/\beta)$.

To illustrate, consider an amplifier whose open-loop transfer function is characterized by three poles. For simplicity let the three poles be widely separated—say, at 0.1 MHz, 1 MHz, and 10 MHz, as shown in Fig. 8.37. Note that because the poles are widely separated, the phase is approximately -15° at the first pole frequency, -145° at the second, and -225° at the third. The frequency at which the phase of $A(j\omega)$ is -180° lies on the -40 -dB/decade segment, as indicated in Fig. 8.37.

FIGURE 8.37 Stabilization using Bode plot of $A(j)$.

The over-loop gain of this amplifier can be expressed as

$$A = \frac{-\beta}{(1 + \beta/10^3)(1 - jf/10^6)(1 + jf/10^3)} \quad (8.79)$$

from which $|A|$ can be easily determined for any frequency f in Hz, and the phase can be obtained as

$$\phi = -\tan^{-1}(j/f \cdot 10^3) + \tan^{-1}(f/10^6) + \tan^{-1}(j/f \cdot 10^3) \quad (8.80)$$

The magnitude and phase graphs shown in Fig. 8.37 are obtained using the method for constructing Bode plots (Appendix E). These graphs provide approximate values for imperfect amplifier parameters, with more exact values obtainable from Eqs. (8.79) and (8.80). For example, the frequency f_{ph} at which the phase angle is -180° can be found from Fig. 8.37 to be approximately 3.2×10^6 Hz. Using this value as a starting point, a more exact value can be found by trial and error using Eq. (8.80). The result is $f_{\text{ph}} = 3.34 \times 10^6$ Hz. At this

frequency, Eq. (8.79) gives a gain magnitude of 58.2 dB, which is reasonably close to the approximate value of 60 dB given by Fig. 8.37.

Consider next the straight line labeled (a) in Fig. 8.37. This line represents a feedback factor β for which $20 \log |1/\beta| = 85$ dB, which corresponds to $\beta = 5.623 \times 10^{-3}$ and a closed-loop gain of 81.6 dB. Since the loop gain is the difference between the $|A|$ curve and the $20 \log |1/\beta|$ line, the point of intersection X_1 corresponds to the frequency at which $|\beta| = 1$. Using the graph of Fig. 8.37, this frequency can be found to be approximately 3.6×10^6 Hz. A more exact value of 4.936×10^6 rad/s can be obtained using the transfer function equations. At this frequency the phase angle is approximately -108° . Thus the closed-loop amplifier, for which $20 \log |1/\beta| = 85$ dB, will be stable with a phase margin of 72° . The gain margin can be easily obtained from Fig. 8.37; it is 25 dB.

Next, suppose that we wish to use this amplifier to obtain a closed-loop gain of 50-dB nominal value. Since $A_{\text{ph}} = 100$ dB, we see that $A_{\text{ph}}\beta < 1$ and $20 \log |A_{\text{ph}}\beta| = 50$ dB, resulting in $20 \log |1/\beta| = 50$ dB. To see whether this closed-loop amplifier is or is not stable, we draw line (b) in Fig. 8.37 with a height of 50 dB. This line intersects the open-loop gain curve at point X_2 , where the corresponding phase is greater than 180° . Thus the closed-loop amplifier with 50-dB gain will be unstable.

In fact, it can easily be seen from Fig. 8.37 that the minimum value of $20 \log |1/\beta|$ that can be used, with the resulting amplifier being stable, is 60 dB. In other words, the minimum value of stable closed-loop gain obtainable with this amplifier is approximately 60 dB. At this value of gain, however, the amplifier may still oscillate, since no margin is left for possible changes in gain.

Since the 180° -phase point always occurs on the -20 -dB/decade segment of the Bode plot for $|A|$, a rule of thumb to guarantee stability is as follows: The closed-loop amplifier will be stable if the $20 \log |1/\beta|$ line intersects the $20 \log |A|$ curve at a point on the -20 -dB/decade segment required. Following this rule ensures that a phase margin of at least 15° is obtained. For the example of Fig. 8.37, the rule implies that the maximum value of $|\beta|$ is 10^{-1} , which corresponds to a closed-loop gain of approximately 80 dB.

The rule of thumb above can be generalized for the case in which β is a function of frequency. The general rule states that at the intersection of $20 \log |1/\beta(f)|$ and $20 \log |A(f)|$ the difference of slopes (called the rate of closure) should not exceed 20 dB/decade.

EXERCISE

8.11 Consider an op-amp-based circuit having a unity-gain feedback. The open-loop gain is $A_{\text{OL}} = 10^5$ dB, and the corner frequencies are $f_1 = 10^3$ Hz and $f_2 = 10^6$ Hz. The feedback factor is $\beta = 10^{-3}$. The output voltage is $V_o = 10V_{\text{in}}$. The input voltage is $V_{\text{in}} = 10^{-3}V_o$. The load resistance is $R_L = 10^3$ ohms. The power supply is ± 15 V. The circuit is to be compensated using a single pole. The corner frequency of the compensation is to be $f_c = 10^4$ Hz. The desired closed-loop gain is $A_{\text{CL}} = 10^4$ dB. The desired phase margin is 72° . The desired gain margin is 25 dB. The desired corner frequency of the closed-loop system is $f_1 = 10^3$ Hz. The desired corner frequency of the closed-loop system is $f_2 = 10^6$ Hz. The desired corner frequency of the closed-loop system is $f_3 = 10^4$ Hz. The desired corner frequency of the closed-loop system is $f_4 = 10^5$ Hz. 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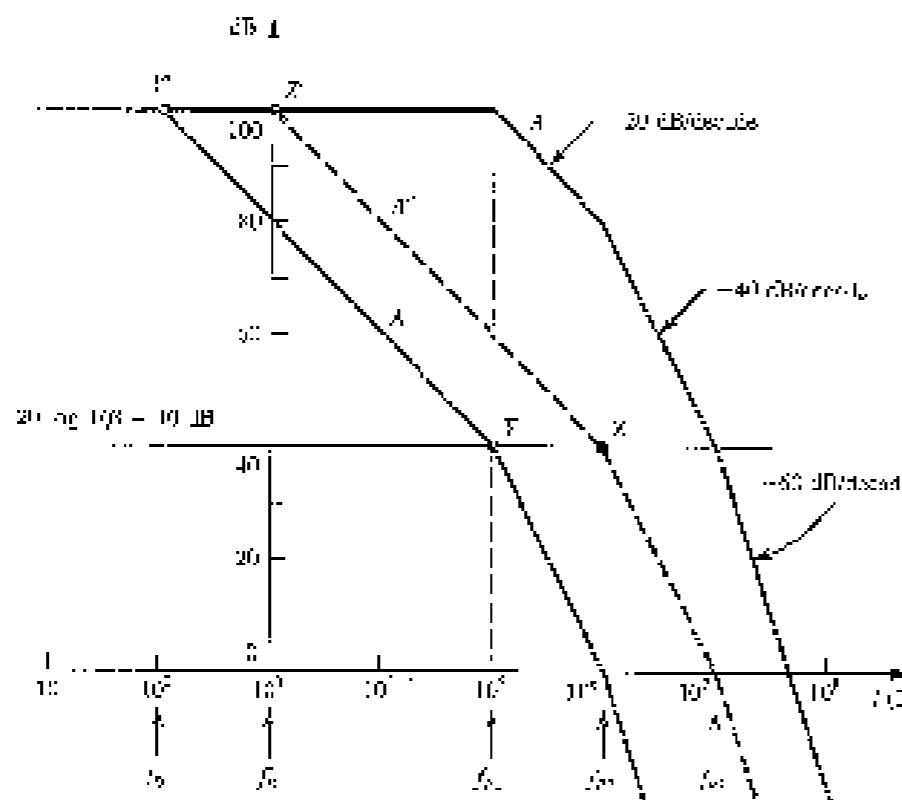


FIGURE 8.38 Frequency compensation for $\beta = 10^{-2}$. The response is obtained by introducing an additional pole at f_c . The A' response is obtained by moving the original low-frequency pole at f_p .

8.11.1 Theory

The simplest method of frequency compensation consists of introducing a new pole in the function $A(s)$ at a sufficiently low frequency, f_p , such that the modified open-loop gain, $A'(s)$, intersects the $20 \log(1/\beta)$ curve with a slope difference of 20 dB/decade. As an example, let's assume we want to compensate the amplifier whose $A(s)$ is shown in Fig. 8.38 such that closed-loop amplifiers with β as high as 10^{-2} (i.e., closed-loop gains as low as approximately 10 dB) will be stable. First, we draw a horizontal straight line at the 10-dB level to represent $20 \log(1/\beta)$, as shown in Fig. 8.38. We then locate point Y on this line at the frequency of the first pole, f_p . From Y we draw a line with a -20-dB/decade slope and determine the point X at which this line intersects the $A(s)$ gain line. Point P is the frequency f_p of the new pole that has to be introduced in the open-loop transfer function.

The compensated open-loop response $A'(s)$ is indicated in Fig. 8.38. It has two poles at f_p , f_{p+} , and f_{p-} . Thus $A'(s)$ begins to roll off with a slope of -20 dB/decade at f_p . At f_{p+} the slope changes to -40 dB/decade, at f_{p-} it changes to +40 dB/decade, and so on. Since the $20 \log(1/\beta)$ line intersects the $20 \log(A')$ curve at point X on the -20-dB/decade segment, the closed-loop amplifier with this β value (or lower values) will be stable.

A serious disadvantage of this compensation method is that at most frequencies the open-loop gain has been drastically reduced. This means that at most frequencies the amount of feedback available will be small. Since all the advantages of negative feedback are directly proportional to the amount of feedback, the performance of the compensated amplifier has been impaired.

Careful examination of Fig. 8.38 shows that the gain $A'(s)$ is low because of the pole at f_p . If we can somehow eliminate this pole, then—rather than locating point Y , drawing PP' , and so on—we can just move Z far to the frequency of the second pole and draw the line ZZ' . This would result in the open-loop curve $A''(s)$, which shows considerably higher gain than $A'(s)$.

Although it is not possible to eliminate the pole at f_p , it is usually possible to shift that pole from $f = f_p$ to $f = f_{p'}$. This makes the pole dominant and eliminates the need for introducing an additional lower-frequency pole, as will be explained next.

8.11.2 Implementation

We shall now address the question of implementing the frequency-compensation scheme discussed above. The amplifier circuit normally consists of a number of cascaded gain stages, with each stage responsible for one or more of the transfer function poles. Through your usual analog computer analysis of the circuit, one identifies which stage it introduces each of the important poles f_{p1}, f_{p2} , and so on. For the purpose of our discussion, assume that the first pole f_{p1} is introduced in the interface between the two cascaded differential stages shown in Fig. 8.39(a). In Fig. 8.39(b) we show a simple small-signal model of the circuit at this interface. Current source I_1 represents the output signal current of the Q_1-Q_2 stage. Resistance R_1 and capacitance C_1 represent the total resistance and capacitance between the two nodes B and D . It follows that the pole f_{p1} is given by

$$f_{p1} = \frac{1}{2\pi C_1 R_1} \quad (8.41)$$

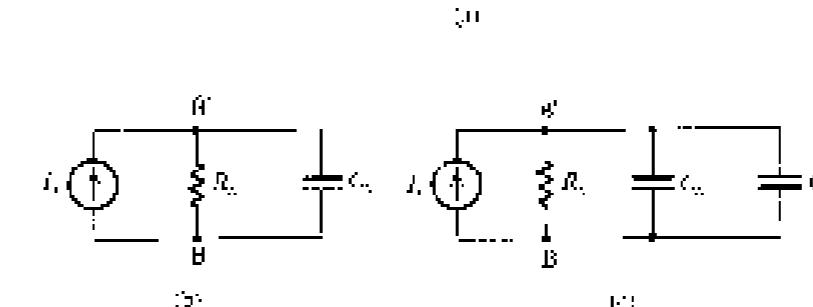
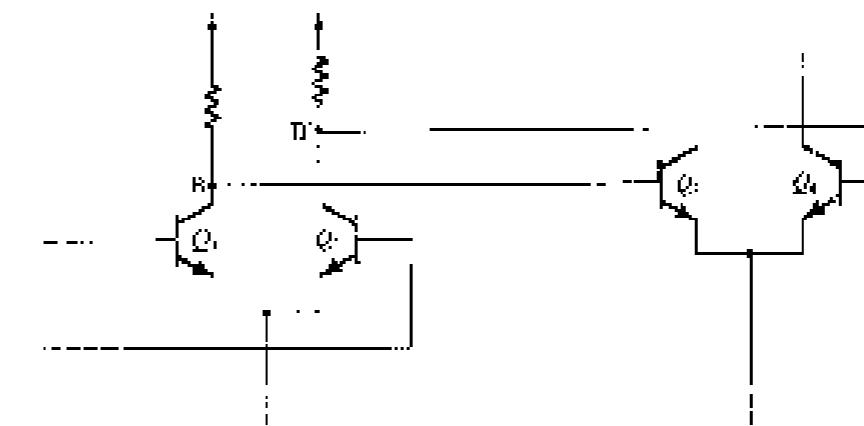


FIGURE 8.39 (a) Two cascaded gain stages of an inverting amplifier. (b) Equivalent circuit for the interface between the two stages. (c) The same circuit as in (b) with a compensation capacitor C_p added. Note that this analysis also applies equally well to MOS amplifiers.

Let us now connect the compensating capacitor C_2 between nodes B and B' . This will result in the modified equivalent circuit shown in Fig. 8.39(a) from which we see that the pole introduced will no longer be at f_{p1} ; rather, the pole can be at any desired lower frequency f_p :

$$f_p = \frac{1}{2\pi(C_1 + C_2)R_1} \quad (8.82)$$

We thus conclude that one can select an appropriate value for C_2 so that the pole frequency from f_{p1} to the value f_p determined by prior Z in Fig. 8.38.

At this juncture it should be pointed out that adding the capacitor C_2 will usually result in changes in the location of the other poles (those at f_{p2} and f_{p3}). One might therefore need to calculate the new location of f_p and perform a few iterations to arrive at the required value for C_2 .

A serious danger of this implementation method is that the required value of C_2 is usually quite large. Thus if the amplifier to be compensated is a JFET op-amp, it will be difficult and probably impossible, to include the compensating capacitor on the IC chip. As pointed out in Chapter 6 and in Appendix A, the maximum practical size of a monolithic capacitor is about 100 pF. An elegant solution to this problem is to connect the compensating capacitor in the feedback path of an amplifying stage. Because of the Miller effect, the compensating capacitance will be multiplied by the stage g_m , resulting in a much larger effective capacitance. Furthermore, as explained later, another unexpected benefit accrues.

8.11.3 Miller Compensation and Pole Splitting

Figure 8.40(a) shows one gain stage of a multistage amplifier. For simplicity, the stage is shown as a common-emitter amplifier, but in practice it can be a more elaborate circuit. In the feedback path of this common-emitter stage we have placed a compensating capacitor C_2 .

Figure 8.40(b) shows a simplified equivalent circuit of the gain stage of Fig. 8.40(a). Here R_1 and C_1 represent the total resistance and total capacitance between node B and ground. Similarly, R_2 and C_2 represent the total resistance and total capacitance between node C and ground. Furthermore, it is assumed that C_1 includes the Miller component due to capacitors C_{o1} and C_3 includes the input capacitance of the succeeding amplifier stage. Finally, I represents the output signal current of the preceding stage.

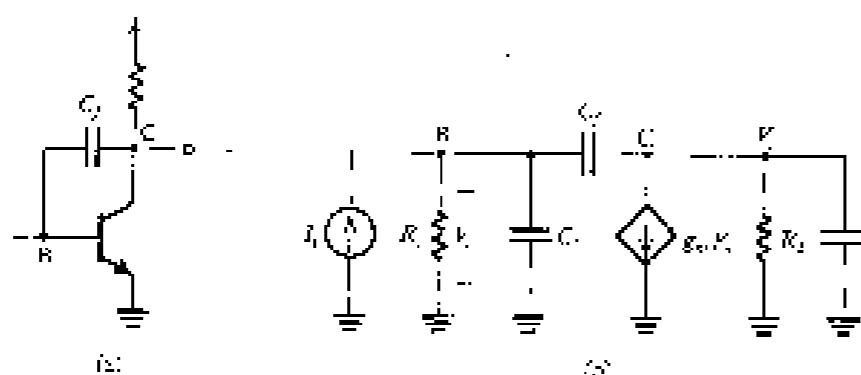


FIGURE 8.40 (a) A gain stage in a multistage amplifier with a compensating capacitor connected in the feedback path and (b) an equivalent circuit. Note that although a JFET is shown, the analysis in this section applies to the MOSFET case.

In the absence of the compensating capacitor C_2 , we can see from Fig. 8.40(b) that there are two poles—one at the input and one at the output. Let us assume that these two poles are f_{p1} and f_{p2} in Fig. 8.38; thus,

$$f_{p1} = \frac{1}{2\pi C_1 R_1} \quad f_{p2} = \frac{1}{2\pi C_3 R_3} \quad (8.83)$$

With C_1 given, analysis of the circuit yields the transfer function

$$\frac{V_o}{V_i} = \frac{\frac{(sC_2 + g_m)R_2 R_3}{1 + s(C_1 R_1 + C_3 R_3) + C_1 C_3 R_1 R_3 + R_1 + R_3} + s^2[C_1 C_3 + C_1 C_2 + C_2 C_3]R_1 R_3}{1 + s[C_1 R_1 + C_3 R_3] + C_1 C_3 R_1 R_3 + R_1 + R_3} \quad (8.84)$$

The zero is usually at a much higher frequency than the dominant pole, and we shall neglect it. The denominator polynomial $D(s)$ can be written in the form

$$D(s) = \left(1 + \frac{s}{\omega_{p1}'}\right)\left(1 + \frac{s}{\omega_{p2}'}\right) = 1 + \left(\frac{1}{\omega_{p1}'} + \frac{1}{\omega_{p2}'}\right)s + \frac{s^2}{\omega_{p1}' \omega_{p2}'} \quad (8.85)$$

where ω_{p1}' and ω_{p2}' are the new frequencies of the two poles. Normally one of the poles will be dominant; $\omega_{p1}' \gg \omega_{p2}'$. Thus,

$$D(s) \approx 1 + \frac{s}{\omega_{p1}'} + \frac{s^2}{\omega_{p1}' \omega_{p2}'} \quad (8.86)$$

Equating the coefficients of s in the denominators of Eq. (8.84) and in Eq. (8.86) results in

$$\omega_{p1}' = \frac{1}{C_1 R_1 + C_3 R_3 + C_1 C_3 R_1 R_3 + R_1 + R_3} \quad (8.87)$$

which can be approximated by

$$\omega_{p1}' \approx \frac{1}{g_m R_1 C_1 R_3} \quad (8.88)$$

To obtain ω_{p1}' , we equate the coefficients of s^2 in the denominators of Eq. (8.84) and in Eq. (8.86) and use Eq. (8.87):

$$\omega_{p2}' = \frac{g_m C_1}{C_1 C_3 + C_3 (C_1 + C_2)} \quad (8.89)$$

From Eqs. (8.87) and (8.89), we see that as C_2 is increased, ω_{p1}' is reduced and ω_{p2}' is increased. This scheme is referred to as pole splitting. Note that the increase in ω_{p2}' is highly beneficial; it allows us to move pole Z (see Fig. 8.38) further to the right, thus resulting in a higher compensated open-loop gain. Finally, note from Eq. (8.89) that C_2 is multiplied by the Miller-effect factor $g_m R_3$, thus resulting in a much larger capacitance, $g_m R_3 C_2$. In other words, the required value of C_2 will be much smaller than that of C_3 in Fig. 8.39.



Consider an op-amp whose open-loop transfer function is identical to that shown in Fig. 8.37. We wish to compensate this op-amp so that the closed-loop amplifier with resistive feedback is stable for any gain (*i.e.*, for β up to infinity). Assume that the op-amp circuit includes a stage such as that of Fig. 8.40 with $C_1 = 100 \text{ pF}$, $C_3 = 5 \text{ pF}$, and $g_m = 10 \text{ mA/V}$. Let the pole at f_{p1} be caused by the input circuit of that stage, and that the pole at f_{p2} is introduced by the output circuit. Find the value of the compensating capacitor for two cases: either if it is connected between the input node B and ground or in the feedback path of the transistor.

Solution

First we determine R_1 and R_2 from

$$f_{p1} = 0.1 \text{ MHz} = \frac{1}{2\pi C_1 R_1}$$

Thus,

$$R_1 = \frac{10^7}{3C_1} \Omega$$

$$f_{p2} = 1 \text{ MHz} = \frac{1}{2\pi C_2 R_2}$$

Thus,

$$R_2 = \frac{10^7}{3C_2} \Omega$$

If a compensating capacitor C_3 is connected across the input terminals of the transistor, then the frequency of the first pole changes from f_{p1} to f'_{p1} :

$$f'_{p1} = \frac{1}{2\pi(C_1 + C_3)R_1}$$

The second pole remains unchanged. The required value for C_3 is determined by drawing a 20-dB decade line from the 1-MHz frequency point on the $20 \log(1/\beta) - 20 \log 1 = 0$ dB line. This line will intersect the 100-dB dc gain line at 10 Hz. Thus,

$$f'_{p1} = 10 \text{ Hz} = \frac{1}{2\pi(C_1 + C_3)R_1}$$

which results in $C_3 = 1 \mu\text{F}$, which is quite large and certainly cannot be included on the IC chip.

Now, if a compensating capacitor C_3 is connected in the feedback path of the transistor, the two poles change location to the values given by Eqs. (8.87) and (8.88):

$$f'_{p1} = \frac{1}{2\pi g_m R_1 C_2 R_1} \quad f'_{p2} = \frac{\omega_t C_2}{2\pi(C_1 C_2 + C_1(C_1 + C_2))} \quad (8.89)$$

To determine where we should locate the first pole, we need to know the value of f'_{p2} . As an approximation, let's assume that $C_f \gg C_2$, which enables us to obtain

$$f'_{p2} = \frac{\omega_t}{2\pi(C_1 + C_2)} = 60.6 \text{ MHz}$$

Thus it appears that this pole will move to a frequency higher than f_{p1} (which is 10 MHz). Let us therefore assume that the second pole will be at f_{p2} . This requires that the first pole be located at

$$f'_{p1} = \frac{f_{p2}}{A_2} = \frac{10^7 \text{ Hz}}{10^4} = 100 \text{ Hz}$$

Thus,

$$f'_{p1} = 100 \text{ Hz} = \frac{1}{2\pi g_m R_1 C_2 R_1}$$

which results in $C_2 = 78.5 \text{ pF}$. Although this value is indeed much greater than C_1 , we can determine the location of the pole f'_{p1} from Eq. (8.89), which yields $f'_{p1} = 77.2 \text{ MHz}$, confirming that this pole has indeed been moved past f_{p2} .

We conclude that using Miller compensation not only results in a more slender compensating capacitor but, owing to pole splitting, also enables us to place the dominant pole a decade higher in frequency. This results in a wider bandwidth for the compensated op-amp.

EXERCISES

8.12.1 A two-pole circuit has the following corner frequencies: $f_{p1} = 100 \text{ Hz}$ and $f_{p2} = 10 \text{ MHz}$. If the load resistance is 100Ω , find the loop gain magnitude at the frequency at which the two poles interlace to reduce the magnitude of the output voltage by 50%.

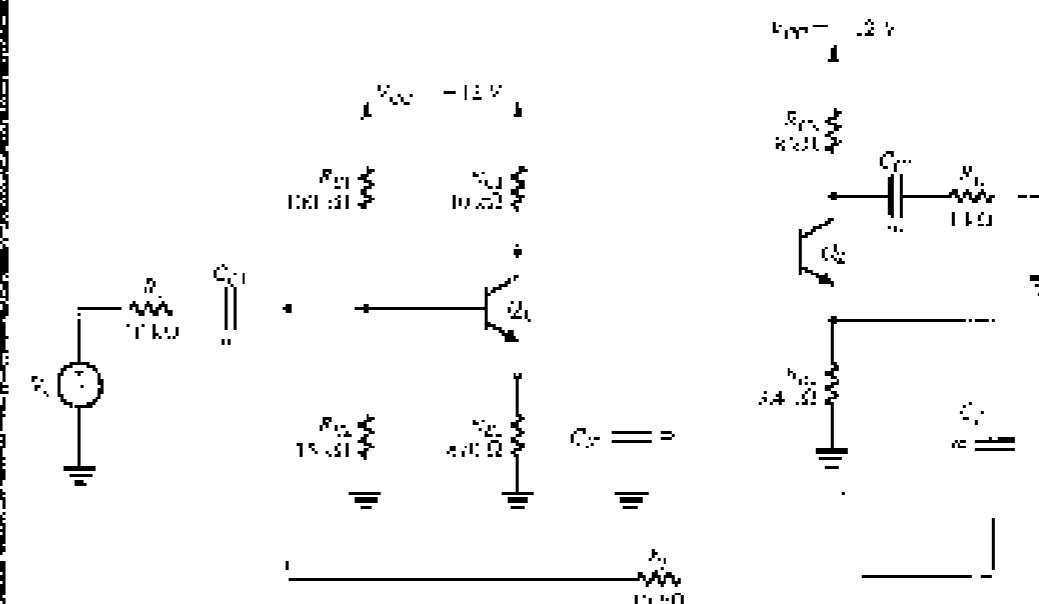
8.12.2 Consider the circuit described in Example 8.12. Calculate the magnitude of the output voltage at the frequency at which the two poles interlace to reduce the magnitude of the output voltage by 50%. If the frequency of the second pole is at 1 MHz and the second-magnitude value is unchanged as required, find the frequency at which the first pole must be lowered so that the resulting single-pole low-pass loop-gain value is 20 dB. By what frequency is the magnitude of the control line inside the inverter increased?

8.12 SPICE SIMULATION EXAMPLE

We conclude this chapter by presenting an example that illustrates the use of SPICE in the analysis of feedback circuits.

DETERMINING THE LOOP GAIN USING SPICE

This example illustrates the use of SPICE to compute the loop gain ω_L . To be able to compare results, we shall use the same short-series feedback amplifier considered in Example 8.2 and shown in Fig. 8.11. This, however, does not limit the generality of the method described.



To compute the loop gain, we set the input signal V_{in} to zero, and we choose to break the feedback loop between the collector of Q_1 and the base of Q_2 . However, to break the feedback loop, we must ensure that the following two conditions that existed prior to breaking the feedback loop do not change: (1) the dc bias condition and (2) the no signal current I_{Q1} .

To view the feedback loop without disturbing the dc bias conditions of the circuit, we inject a large voltage V_{inj} at V_{in} , as shown in Fig. 8.42(a). The no-value of, say, $I_{inj} = -10\text{ mA}$ will ensure that the loop is opened for no signals while keeping dc bias conditions unchanged.

To break the feedback loop without disturbing the signal-current conditions, we must load the loop output at the collector of Q_1 with a termination impedance Z_t whose value is equal to the impedance seen looking into the loop input at the base of Q_2 . Furthermore, to avoid disturbing the dc bias conditions, Z_t must be connected to the collector of Q_1 via a large coupling capacitor. However, it is not always easy to determine the value of the termination impedance Z_t . So, we will describe two simulation methods to compute the loop gain without really determining Z_t .

Method 1 Using the open-circuit and short-circuit transfer functions

As described in Section 8.7, the loop gain can be expressed as

$$\text{dB} = -10 \left(\frac{V_{out}}{V_{in}} + \frac{1}{T_{\infty}} \right)$$

where T_{∞} is the open-circuit voltage transfer function and T_s is the short-circuit voltage transfer function.

The circuit for determining T_{∞} is shown in Fig. 8.42(b). Here, an ac test signal voltage V_{in} is applied to the loop input at the base of Q_2 via a large coupling capacitor (having a value of, say, 1 kF) to avoid disturbing the dc bias conditions. Then,

$$T_{\infty} = \frac{V_{out}}{V_{in}}$$

where V_{out} is the ac open-circuit output voltage at the collector of Q_1 .

In the circuit for determining T_s (Fig. 8.42(b)), an ac test signal current I_{inj} is applied to the loop input at the base of Q_2 . Note that a coupling capacitor is not needed in this case because the ac current source appears as an open-circuit source, and, hence, does not disturb the dc bias conditions.

The loop output at the collector of Q_1 is dc short-circuited to ground via a large capacitor C_{L1} . Then,

$$T_s = \frac{I_{Q1}}{I_{inj}}$$

where I_{Q1} is the ac short-circuit output current at the collector of Q_1 .

Method 2 Using a replica circuit

As shown in Fig. 8.42(c), a replica of the feedback amplifier circuit can be simply used as a terminated impedance. Here, the feedback loops in both the amplifier circuit and the replica circuit are broken using a large inductor L_{rep} , to avoid disturbing the dc bias conditions. The loop output at the collector of Q_1 in the amplifier circuit is then connected to the loop input at the base of Q_2 in the rep circuit via a large coupling capacitor C_{L1} (again, to avoid disturbing the dc bias conditions). Thus, to set signals, the loop output at the collector of Q_1 in the amplifier circuit has an impedance equal to the Z_t value before the feedback loop is broken. Accordingly, we have ensured that the conditions that existed in the amplifier circuit prior to breaking the loop have not changed.

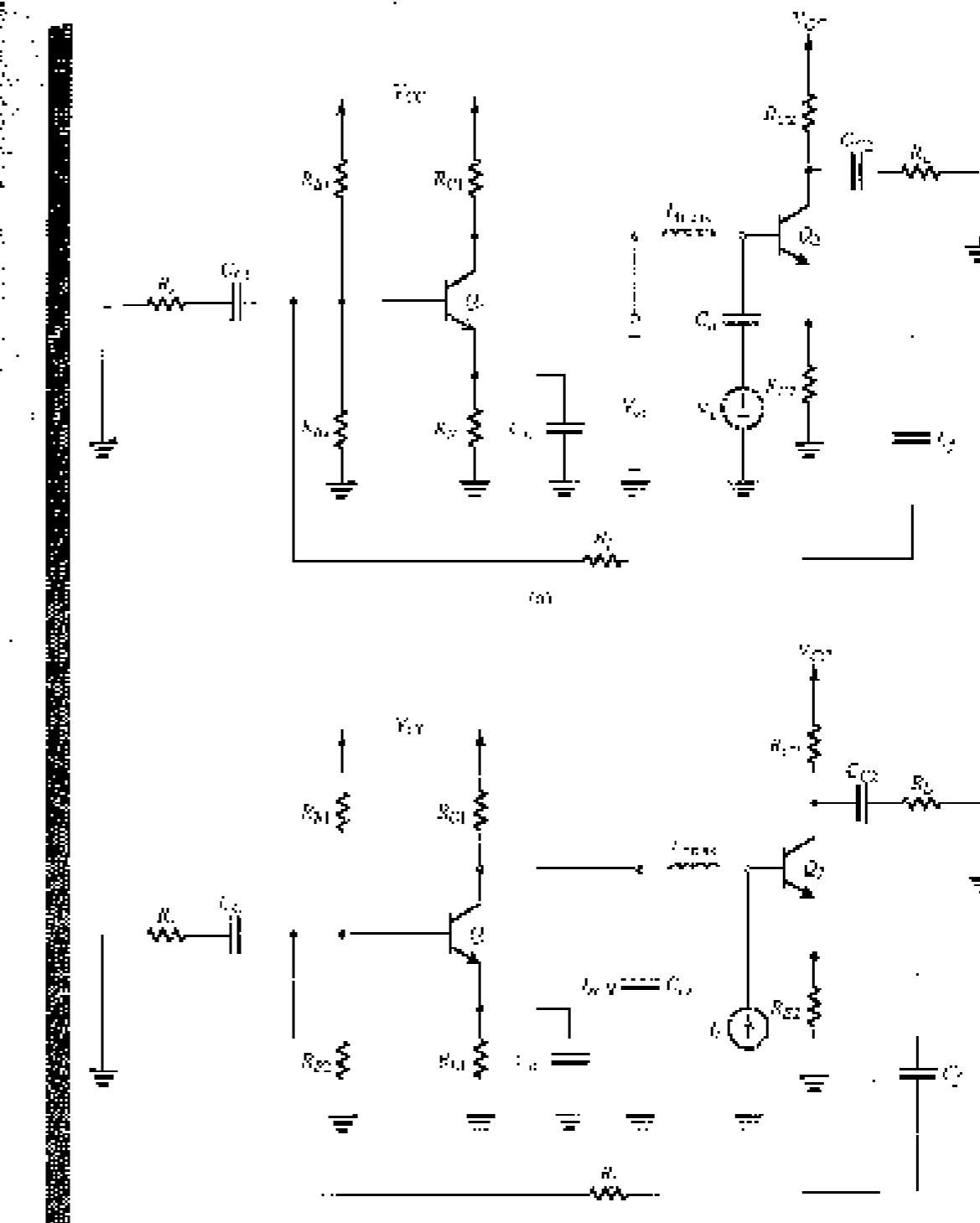


FIGURE 8.42 Circuits for simulating (a) the open-circuit voltage transfer function T_{∞} and (b) the short-circuit voltage transfer function T_s of the feedback amplifier in Fig. 8.41 for the purpose of coupling the loop gain.

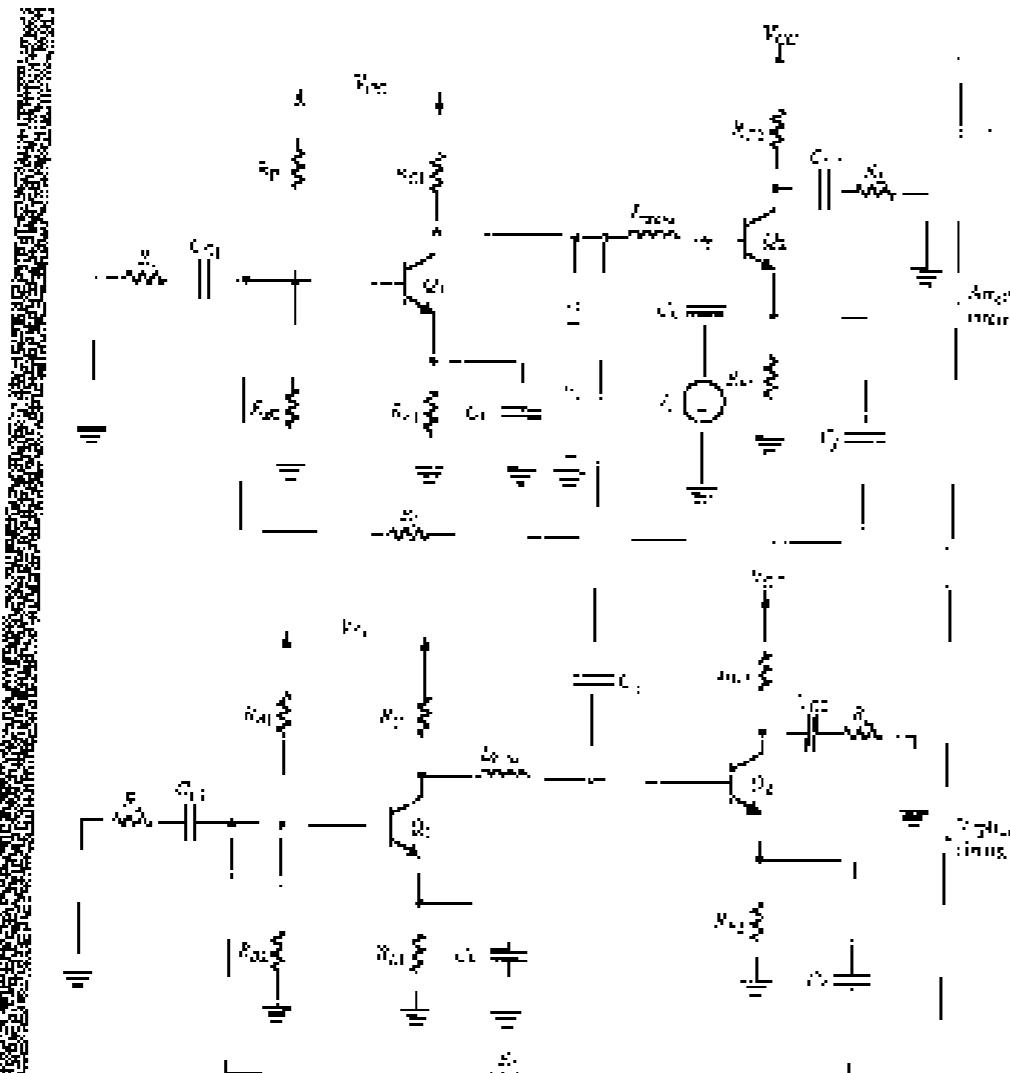


FIGURE 8.43 Circuit for calculating the loop gain $A\beta$ of the feedback amplifier in Fig. 8.41 using the replacement method.

Next we determine the loop gain $A\beta$. We apply an ac test-signal voltage V_{in} via a large coupling capacitor C_4 at the loop input at the base of Q_1 in the amplifier circuit. To do so, as described in Section 8.7,

$$A\beta = \frac{V_o}{V_{in}}$$

where V_o is the ac measured signal at the loop output, at the collector of Q_4 , in the amplifier circuit.

To compute the loop gain $A\beta$ of the feedback amplifier circuit in Fig. 8.41 using SPICE, we choose to simulate the circuit in Fig. 8.43. In the SPICE simulations, we used part 1N2221A (whose SPICE model is given in Table 3.9) for the BJT's, and we set $f_{T1} = 10$ GHz and the coupling and bypass capacitors to be 1 nF. The magnitude and phase of $A\beta$ are plotted in Fig. 8.44, from which we see that the feedback amplifier has a gain margin of 57 dB and a phase margin of 88°.

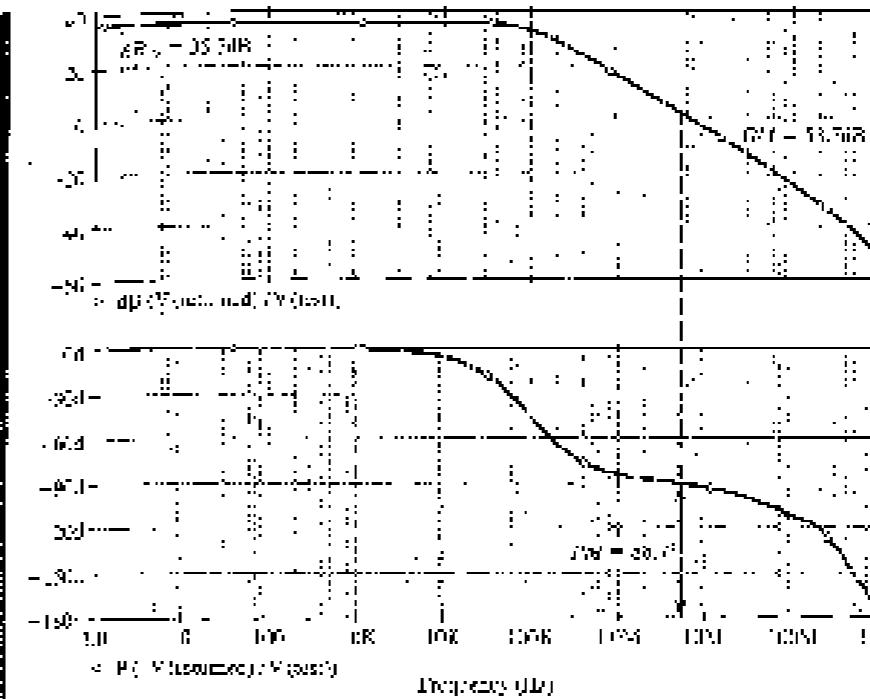


FIGURE 8.44 (a) Magnitude and (b) phase of the loop gain $A\beta$ of the feedback amplifier circuit in Fig. 8.41.

SUMMARY

- (a) Negative feedback is employed to make the overall gain less sensitive to component variations; to reduce input and output impedances; to extend bandwidth; to reduce nonlinear distortion; and to enhance signal-to-noise (and signal-to-noise-to-coupling ratio).
- (b) The advantages above are realized by the inverse of a reduction in gain, and at the risk of overcoupling (i.e., oscillating). The latter problem is solved by careful design.
- (c) For each of the four basic types of amplifiers, there is an appropriate feedback topology. The four topologies, together with their analysis procedure and their effects on input and output impedances, are summarized in Table 8.1 on page 820.
- (d) For key feedback parameters, i.e., loop gain $A\beta$, which for negative feedback must be a positive dimensionless number, and the amount of feedback $\beta = A\beta/A$. The latter quantity determines gain reduction, gain degradability, bandwidth extension, and the ages of Z_i and Z_o .
- (e) Since A and β are in general frequency dependent, the poles of the feedback amplifier are obtained by solving the characteristic equation $1 - A\beta(s) = 0$.
- (f) For the two network analyzer to obtain $A\beta$, one must plot both in the left half of the s-plane.
- (g) Stability is guaranteed if all the imaginary axes which the phase angle of $A\beta$ is 180° ($\pm 90^\circ$) or 0° . $A\beta$ is just the stability; the amount by which it is less than unity, expressed in decibels, is the gain margin. Alternatively, the amplitude is constant at the frequency at which $A\beta = 1$; the phase angle is 0° (-180° , 90°) the phase margin is the gain margin.
- (h) The stability of a feedback amplifier can be analyzed by constructing a Bode plot for A and β , or by using an s-plane plot for $1/A\beta$. Stability is guaranteed if the two poles never set with a difference in slope no greater than 6 dB/ octave.
- (i) To make a given amplifier stable for a given feedback factor β , the open-loop frequency response is split up, as required by a process known as frequency compensation.
- (j) A popular method for frequency compensation involves β -biasing: the feedback controller crosses an input level, about $\pm 10\%$ of the mean. This causes the pole formed at the input of the amplifier stage to shift to lower frequency and thus become dominant, while the pole at the output of the amplifier stage is moved to a pole f_p at a frequency not very far away from the original. This process is known as pole splitting.

PROBLEMS

SECTION 8.1: THE GENERAL FEEDBACK STRUCTURE

8.1 A negative-feedback amplifier has a class-A output gain $A = 100$ and an open-loop gain $A_f = 10^3$. What is the feedback factor β if a small-variance error results in a reduction of A_f by 1%? What closed-loop gain results? What is the percentage change in A_f corresponding to this form of 1% variation in A_f ?

8.2 Repeat Exercise 8.1, parts (b) through (e), for $A = 100$.

8.3 Repeat Exercise 8.1, parts (b) through (e), for $A_f = 10^3$. For part (d) use $V_o = 0.01$ V.

8.4 The multivibrator biasing and configuration shown in Fig. 8.4 provides a direct implementation of the feedback loop of Fig. 8.1. Assuming r_s at the output is 1 k Ω , load resistance is 100 k Ω , and output resistance $r_L = 10^3$ k Ω , what is β ? If $A = 100$, what is the closed-loop voltage gain? What is the amount of feedback in dB if $V_o = 1$ V, and v_s and v_{fb} both decrease by 10%, while the corresponding increase is A_f ?

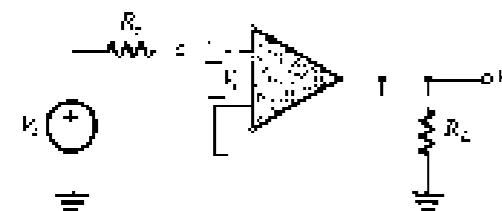


FIGURE 8.4

8.5 In a particular circuit, represented by the schematic diagram of Fig. 8.1, a signal of 1 V from the source feeds its load. If one signal of 10 mV being provided to the multiplying element A_f and 10 V applied to the load. For this arrangement, identify the values of β and β_f that apply.

8.6 Find the open-loop gain, the loop gain, and the amount of feedback in a voltage amplifier for which A_f and β_f differ by (a) 1%, (b) 5%, (c) 10%, (d) 20%.

8.7 In a particular amplifier design, the β network consists of a linear potentiometer for which $\beta = 0.01$ at one end, 1.0 at the other, and set β to the middle. As the potentiometer is adjusted, what the three values of closed-loop gain result, when the amplifier open-loop gain is (a) 1 V/V, (b) 10 V/V, (c) 100 V/V, (d) 10,000 V/V?

8.8 A newly constructed feedback amplifier undergoes a performance test with the following result: With no feedback connection removed, a sine wave signal of 3.4 V is fed into a unity-gain 10-V output stage; the load, with the feedback connection, a 1-V output requires a 90-mV source signal. For this amplifier, identify values of A_f , β , β_f , the closed-loop gain, and the amount of negative feedback (β_f).

SECTION 8.2: SOME PROPERTIES OF NEGATIVE FEEDBACK

8.9 For the negative-feedback loop of Fig. 8.1, find the gain A_f for which the sensitivity of closed-loop gain to open-loop gain (i.e., $(\partial A_f / \partial A_f)/A_f$) is 20 dB. For what value of A_f does the sensitivity become 1/2?

8.10 It is required to design an amplifier with a gain of 100, but it occurs to within $\pm 1\%$. You have available amplifiers stages with a gain of 100 that is accurate to within 10%. Provide a design that uses a number of these stages in cascade, with each stage employing negative feedback of an appropriate amount. Obviously, your design should use the lowest possible number of stages, while meeting specification.

8.11 In a feedback amplifier for which $A_f = 10^4$ and $\beta_f = 10^3$, what is the gain desensitizing factor? Find A_f exactly and approximately, using Eq. (8.5), in the two cases (a) A_f drops by 10% and the β_f drops by 10%.

8.12 Consider an amplifier having a midband gain of 100 and a low-frequency response characterized by a pole at $f = 10$ Hz and a zero at $s = 0$. If the amplifier is to be connected in a negative-feedback loop with a feedback factor β , Part (a) express an expression for the midband gain and the lower 3-dB frequency of the closed-loop amplifier. By what factor has both changed?

8.13 It is required to design an amplifier to have a nominal closed-loop gain of 10 V/V using a unity-gained amplifier whose gain reduces to half its nominal frequency value over the life of the battery. If unity-gain feedback is used, what required open-loop amplifier gain must be used in the design? (Note that since the change in A_f is a measure of time difference.) What value of β should be chosen? If a positive β -value is used in the design, how much may produce a corner at a -20% variation in β , to what value must A_f be raised to ensure the required minimum gain?

8.14 A capacitive-coupled amplifier has a midband gain of 100, a single high-frequency pole at 10 kHz, and a single low-frequency pole at 100 Hz. Negative feedback is employed in the loop; the midband gain is reduced to 10. What are the upper and lower 3-dB frequencies of the closed-loop gain?

8.15 It is required to design a dc amplifier with a low-frequency gain of 1000 and a 3-dB frequency of 0.5 MHz. You have available gain stages with a gain of 100 but with dominant high-frequency pole at 10 kHz. Provide a design that employs a number of such stages in cascade, each with negative feedback β_f an appropriate amount. Use identical stages (5%) When negative feedback of an amount $(1+\beta_f)$

is employed around the gain stage, the 3-dB frequency is increased by the factor of $(1+\beta_f)^{1/2}$.

8.16 Design a supply-ripple-reduced power amplifier, for which maximum stage having a gain of 0.9 V/V and 0.1 V output supply ripple is used. A closed-loop gain of 10 V/V is desired. What is the β_f for a low-ripple power supply needed to reduce the output ripple to 0.01 mV? To 0.001 mV? To 0.1 mV? For each case, specify the value required for the feedback factor β .

8.17 Design a feedback amplifier that has a class-A gain of $A_f = 10$ V/V and is relatively insensitive to change in basic-amplifier gain. In particular, it should provide a resolution in A_f of 0.1% for a variation in A_f of 10% about its nominal value. What is the required loop gain? At a nominal value of A_f is required? What value of β should be used? What would be the closed-loop gain because if β were increased by 10% of its own value infinite?

8.18 A feedback amplifier is to be designed using a feedback loop connected around a two-stage amplifier. The first stage is a direct-coupled small-signal amplifier with a high upper 3-dB frequency. The second stage is a power-amplifier stage with a midband gain of 10 V/V and upper- and lower 3-dB frequencies of 8 kHz and 80 Hz, respectively. The feedback amplifier should have a midband gain of 100 V/V and an upper 3-dB frequency of 40 kHz. What is the required gain of the transistors in the amplifier? What value of β should be used? What does the lower 3-dB frequency of the overall amplifier become?

8.19 The complementary-JFET follower shown in Fig. 8.19(a) has an approximate transfer characteristic as given in Fig. 8.19(b). Observe that for 0.7 V $\leq v_s \leq +0.7$ V, the output is zero. This "dead band" leads to crossover

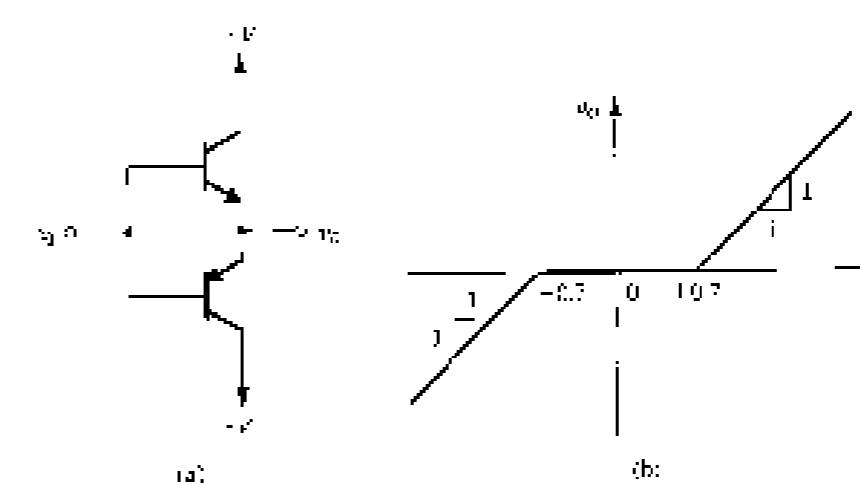


FIGURE 8.19

distortion (see Sect. 11.3). Calculate this follower justify by the output of a differential amplifier or pair. (b) When positive voltage terminal is connected to the input signal source v_s and whose negative input terminal is connected to the emitters of the follower. Sketch the transfer characteristic v_o versus v_s of the resulting feedback amplifier. What are the limits of the dead band and what are the gains outside the dead band?

8.20 A pentode amplifier has a nonlinear transfer characteristic that can be approximated as follows:

(a) For small-signal signals, $|v_s| \leq 10$ mV, $v_o/v_s = 10^3$.

(b) For intermediate-signal signals, $10 \text{ mV} \leq v_s \leq 50 \text{ mV}$, $v_o/v_s = 10^3$.

(c) For large input signals, $v_s \geq 50 \text{ mV}$, the nonlinearity

of the amplifier is suppressed by a negative feedback loop, and the feedback factor β that reduces the factor of 10 change in gain occurring in $|v_s| = 10 \text{ mV}$ to only a 10% change. What is the transfer characteristic of the amplifier with feedback?

SECTION 8.3: THE FOUR BASIC FEEDBACK TOPOLOGIES

8.21 A series-shunt feedback amplifier, representable by Fig. 8.3(a) and using single-polarity voltage amplifier stages with $V_s = 100$ mV, $V_L = 95$ mV, and $V_o = 10$ V. What are the corresponding β values? (a) and (b) include the correct units for each.

8.22 A short-series feedback amplifier is represented by Fig. 8.3(b) and using an ideal basic-coupled op-amp (generalized with $I_s = 100 \mu\text{A}$, $I_o = 10 \text{ mA}$, and $V_o = 10 \text{ mA}$). What are the corresponding values of β ? (a) and (b) include the correct units for each.

*8.23 Consider the closed-loop feedback amplifier of Fig. 8.2.

(c) For N_0, τ_0, ω_0 assumed very large, the direct analysis as opposed to feedback control, can show that the steady current gain is given by

$$A_2 = \frac{I_1}{I_2} = -\frac{K_1 + K_{21}K_{12}(K_1 + K_2)}{K_1 + \frac{1}{K_{21}} + p_{12}/R_1/R}$$

andrew@npr.org

$$K_0 = \emptyset \quad K_1 = \{x\}$$

Now, the approximate error series for A_1 and B_2 will be the same in which $\rho_{A_1} \theta_1 \approx 1$ and $(C/\rho_{B_2}) \approx k_2$.

(b) Figures A₁ and B₁, mostly and approximately, for the case in which $A_{11}, A_{21} = 100$, $R_1 = 90 \text{ cM}$, $R_2 = 90 \text{ cM}$, and $\delta_{12} = 5 \text{ cm}^2/\text{M}$.

(d) Since the negative feedback loop is dominant, let us assume that the output of the amplifier towards ground. The value of V_o can be determined as

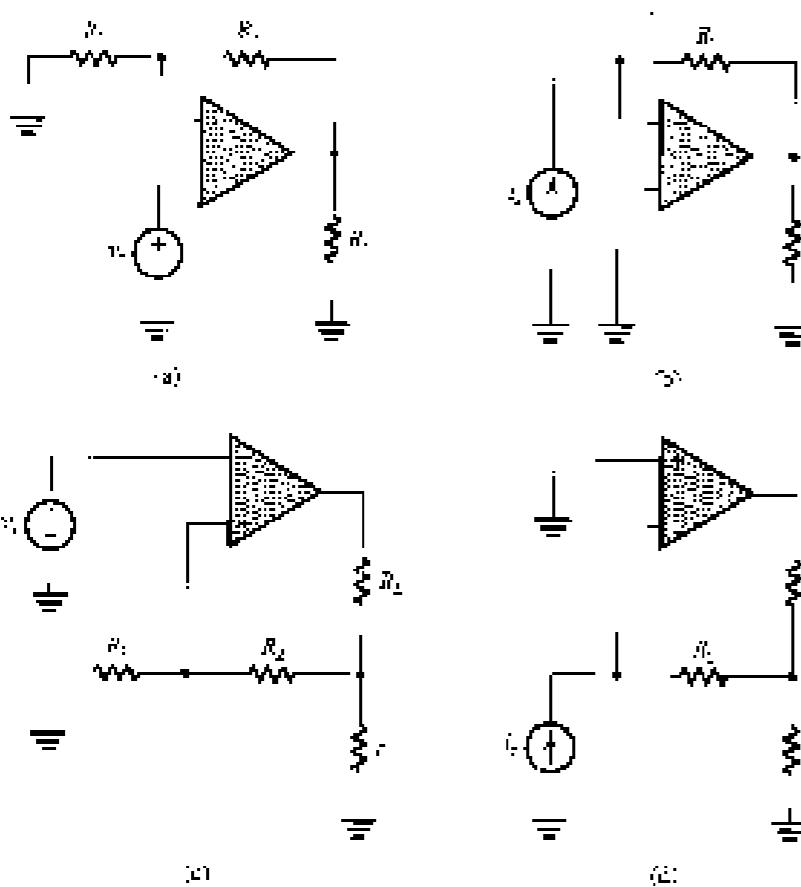


FIGURE P8.20

SECTION B.4: THE SERIES-SHUNT FEEDBACK AMPLIFIER

B.23 A series-shunt feedback amplifier employs a low-current amplifier with input and output resistances each of $1\text{ k}\Omega$ and open-loop gain $A = 20000$ V/V. The feedback factor $\delta = 0.1$ V/V. Find the gain A_f , the load resistance R_L , and the output resistance r_o of the closed-loop amplifier.

8.18 For a particular ramp filter connected in a feedback loop, at which the output voltage is controlled, measurement of the output resistance before and after the ramp is connected shows a change by a factor of 50. Is the resistance with feedback higher or lower? What is the value of the loop gain A_{FB} ? If $R_F = 100\ \Omega$, what is η , without feedback?

Ex. 19 A series-parallel feedback circuit employs a basic voltage source that has a value of 10^6 V/V and a 1 kHz frequency response with a unity-gain frequency of 1 kHz . The input resistance of the basic amplifier is $10^3 \Omega$, and its output resistance is $1 \text{ k}\Omega$. If the feedback factor $\beta = 0.1 \text{ V/V}$, find the input impedance Z_i and the output impedance Z_o of the feedback amplifier. Give equivalent circuit (i.e., Thévenin) and the common-mode rejection ratio.

B.36 A series-shunt buckboost converter takes the feed back signal shown in Fig. B8.36.

(a) Find expression(s) for the k -parameters of the feedback circuit (see Fig. 9.103);
 (b) If $G_1 = 1.333$ and $\beta = 0.01$, what are the values of all four k -parameters? Give the unique solution.

The circuit diagram shows a voltage source v_s connected in series with resistor R_1 . This combination is in parallel with a branch containing resistor R_2 and inductor L_1 in series. The current through R_2 is labeled θ . From the junction between R_2 and L_1 , a branch goes to the right containing resistor R_3 and a current source I_B pointing downwards. Another branch from this junction contains capacitor C in series with resistor R_4 . The output voltage v is measured across the node between R_4 and R_3 and the common reference rail.

FIGURE PAGE

($i = 1$ or 2 , see Fig. 1) and $R_1 = 1$ k Ω , were used, the equivalent circuit following the model in Fig. 8.15(b).

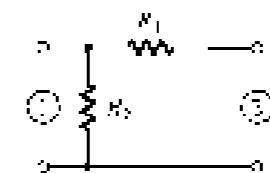


FIGURE PB.30

8.31 A feedback amplifier utilizing voltage coupling is being designed. The basic voltage amp stage has a gain of 100 V/V and an output resistance of 100Ω . If the closed-loop output resistance of 10Ω is required, what is the closed-loop gain? If the basic stage is to be implemented using a unity-gain voltage buffer, what would the closed-loop gain be?

*8.32 In the zener-diode approximation shown in Fig. 8.95, the transistors operate at $V_{BE} = 0.7$ V with $R_E = 100 \Omega$ and each voltage that is very large.

(b) Derive expressions for A , B , R_o , and R_{in} .
 (b) If $i_{in} = 1 \text{ mA}$, $A_{v2} = 100$, $R_s = 1 \text{ k}\Omega$, $R_f = 10 \text{ k}\Omega$, $R_o = 100 \text{ G}\Omega$, and $R_{in} = 1 \text{ k}\Omega$, find the dc bias voltages at the inputs and at the output, and i_{out} .

PROBLEM Figure 18.15 shows a common-emitter amplifier with the load back-biased ($\beta = 1$). The amplifier is designed at $I_{CQ} = 0$ for $V_B = 0$, with small increases in V_B from 0 V defining minimization for the negative feedback term. The technology utilized has $B = 2\pi f = 100 \text{ rad/s}$, $|V_T| = 0.1 \text{ V}$, and $|V_{BE0}| = 26 \text{ mV}$.

- (a) With the feedback loop opened and the gate bias resistors of Q_1 and Q_2 grounded find the dc current and the overdrive voltage at which each of Q_1 or Q_2 is operating. (Ignore the mismatch in I_b between Q_1 and Q_2 owing to their different drain voltages. Also find the dc voltage at the output.)
 (b) Find β , k_T , and R_s of each of the two transistors.
 (c) Find the values of A and R_o . Assume that the bias current sources are ideal.

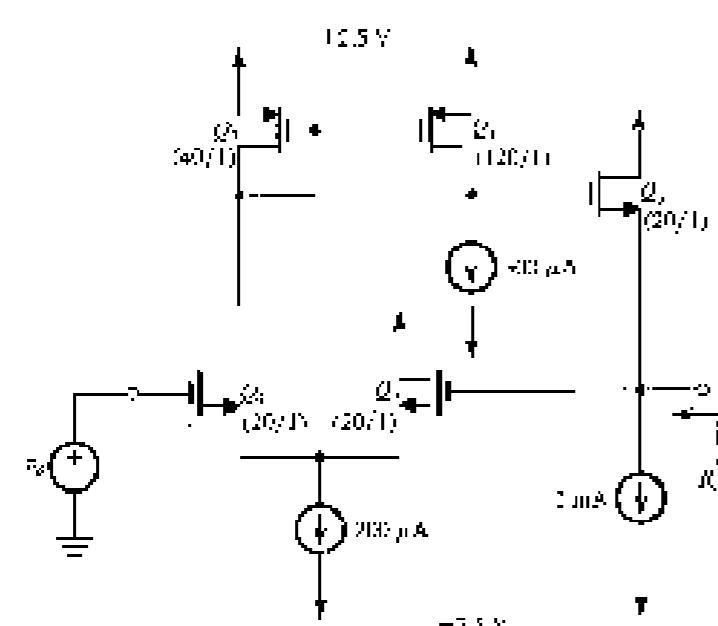


FIGURE P8.33

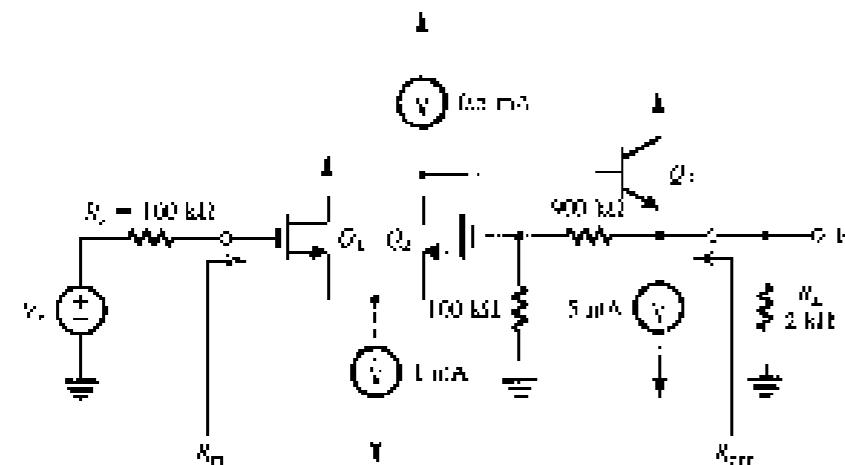


FIGURE P8.34

- (c) Find the gain with feedback, A_f , and the output resistance $R_{o,f}$.
 (d) How would you modify the circuit to reduce a crossover voltage equal to 5 V? What is the value of output resistance obtained?
***8.34** For the circuit in Fig. P8.33, $V_D = 12.5\text{ V}$, $k_T \mu_A = 100\text{ A/V}^2$, $I_b = 120\text{ }\mu\text{A}$, and the Early voltage magnitude for Q_1

device (including noise, bias current, and the current source) is 100 V. The signal source V_s has a zero dc component. Find the dc voltage at the output and at the base of Q_2 . Find the values of A_1 , A_f , k_T , and $R_{o,f}$.

***8.35** (Figure P8.35) shows a series-shunt feedback amplifier without details of the bias circuit.

- (a) Sketch the AC circuit and the circuit for determining β .
 (b) Show that if A is large then the closed-loop voltage gain is given approximately by

$$A_f = \frac{V_o}{V_s} = \frac{R_o + R_f}{R_f}$$

(c) If R_f is selected equal to 50 Ω, find R_o so that A_f results in a closed-loop gain of unity, namely 25 V/V.

(d) If Q_1 's bias is 1 mA, Q_2 at 2 mA, and Q_3 at 4 mA, and assuming that the transistors have $k_T = 100$, find approximate values for $R_{o,f}$ and $R_{e,f}$ in terms of gains from the stages of the circuit as follows: a voltage gain of Q_1 of about -10 and a voltage gain of Q_2 of about -50.

(e) For your design, what is the closed-loop voltage gain required?

(f) Calculate the input and output resistances of the closed-loop amplifier design.

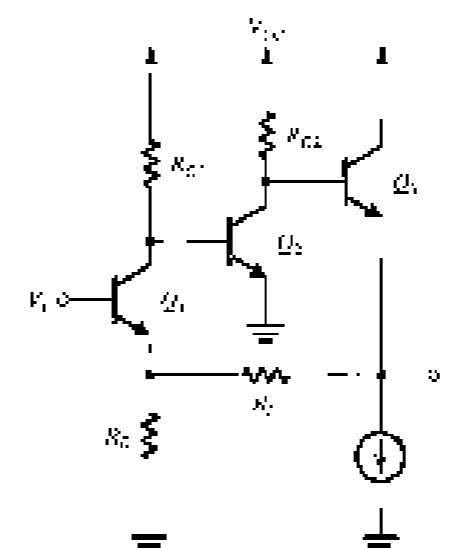


FIGURE P8.35

SECTION 8.5: THE SERIES-SERIES FEEDBACK AMPLIFIER

- 8.36** For the circuit in Fig. 8.17(a), find an approximate value for I_o/V_s assuming that the loop gain is large. Use it to determine the voltage gain V_o/V_s . Compare your results with Fig. 8.36 for and in Example 8.2.

8.37 A series-series feedback amplifier employing a transconductance amplifier having $G_v = 100\text{ mA/V}$, input resistance of 10 kΩ, and output resistance of 100 kΩ. The feedback network has $\beta = 0.1\text{ mA/A}$, an input resistance (with joint 1 open-circuited) of 100 kΩ, and an output resistance (with joint 2 open-circuited) of 10 kΩ. The amplifier operates with a signal source having a resistance of 10 kΩ and with a load resistance of 10 kΩ. Find A_f , $R_{o,f}$, and $R_{e,f}$.

***8.38** (Figure P8.38) shows a circuit for a voltage-controlled current source employing series-series feedback through the resistor R_f . (The bias circuit for the transistors is not shown.) Show that if the loop gain A_f is large,

$$\frac{I_o}{V_s} \approx \frac{R_o}{R_f}$$

Then find the value of R_f to obtain a zero- I_o transconductance of 1 mA/V. If the voltage amplifier has a differential input resistance of 100 kΩ, a voltage gain of 100, and an output resistance of 1 kΩ, and if the transistor is biased at a current of 1 mA, and its k_T of 100 and β of 100, find the actual value of loop gain A_f if V_s is real and $R_o = 10\text{ k}\Omega$. Also find the input resistance $R_{i,f}$ and the output resistance $R_{o,f}$. For calculating $R_{o,f}$, recall that the output resistance of a JFET with an emitter resistance r_{oe} is much larger than r_{oe} , approximately $4k_T/\beta$.

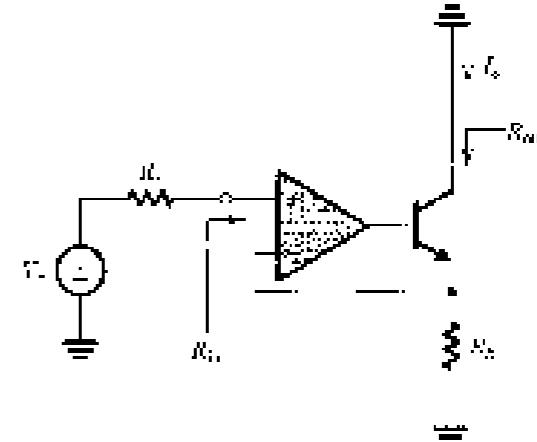


FIGURE P8.38

- 8.39** Figure P8.39 shows a circuit for a voltage-to-current converter employing series-series feedback via resistor R_f . The MJSFETs have the dimensions shown and $\mu_A C_{gs} = 20\text{ pA/V}^2$, $V_D = 12\text{ V}$, and $V_{GS1} = 12.5\text{ V}$. Let us assume that the value of I_o/V_s obtained for large loop gain A_f is feedback analysis to find a more exact value for I_o/V_s ; also, if this output voltage is taken at the source of Q_2 , what closed-loop voltage gain does it have?

- 8.40** For the series-series feedback amplifier in Fig. 8.40, the op amp is characterized by an open-loop voltage gain μ ,

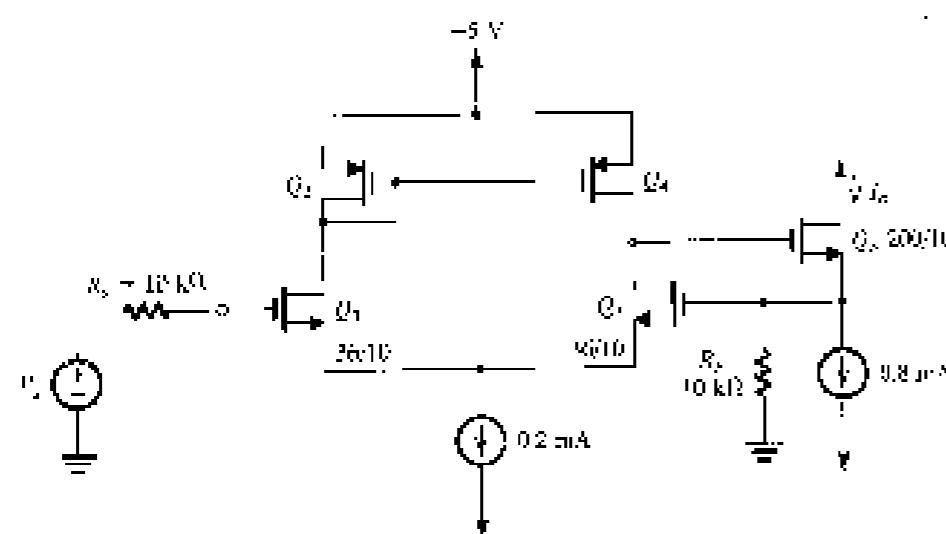


FIGURE PB.39

an input differential resistance $R_{in} = 10\text{ k}\Omega$, and an output resistance $r_o = 100\text{ }\Omega$. The amplifier supplies a current i_o to a load resistance $R_L = 1\text{ k}\Omega$. The feedback network is composed of resistors $r = 100\text{ }\Omega$, $R_s = 10\text{ k}\Omega$, and R_f . It is required to find the gain A_f with feedback $A_f = i_o / i_{in}$, the input resistance R_{in} , and the output resistance R_{out} in the following cases:

- (a) $\mu = 10^3 \text{ V/V}$ and $R_f = 10\text{ k}\Omega$
- (b) $\mu = 10^4 \text{ V/V}$ and $R_f = \infty$

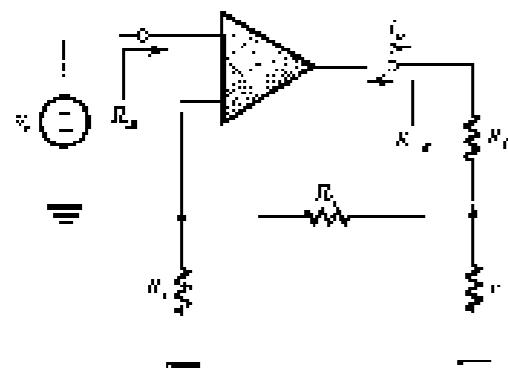


FIGURE PB.40

SECTION 8.6: THE SHUNT-SHUNT AND THE SHUNT-SERIES FEEDBACK AMPLIFIERS

PB.41 For the shunt-shunt feedback shown in Fig. 8.21(a), show that for large feedback

$$\frac{V_o}{V_i} = -\frac{R_f}{R_s}$$

Calculate this gain for the component values given in the circuit diagram, and compare the result with that found in Example 8.9. Find a new value for R_f to obtain a voltage gain of approximately -5.5 V/V .

PB.42 The shunt-shunt feedback amplifier in Fig. PB.41 has $\mu = 1 \text{ mA}$ and $V_{DD} = 10 \text{ V}$. The MOSFET has $V_t = 0.5 \text{ V}$ and $V_A = 20 \text{ V}$. For $R_s = 10\text{ k}\Omega$, $R_f = 1 \text{ M}\Omega$, and $R_o = 4.7 \text{ M}\Omega$, find the voltage gain V_o / V_i , the Lyot resistance R_{Ly} , and the output resistance R_{out} .

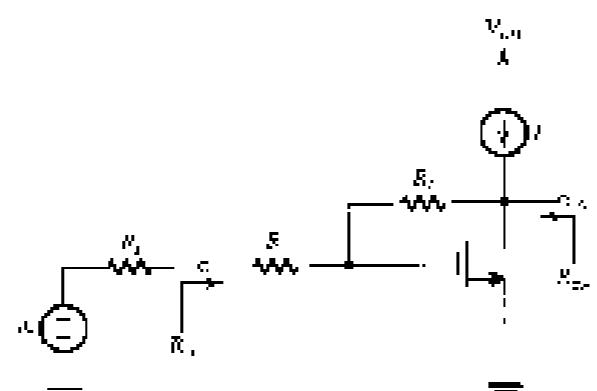


FIGURE PB.42

PB.43 A transresistance amplifier having an overall gain of 10^3 V/V , an input resistance of $1\text{ M}\Omega$, and an output resistance of $1\text{ k}\Omega$ is connected in a negative feedback loop employing a shunt-shunt topology. The feedback network has an input resistance (with port 1 short-circuited) of

$10\text{ }\Omega$ and an input resistance (with port 2 short-circuited) of $10\text{ }\Omega$ and provides a feedback factor $\beta = 0.1 \text{ mV/V}$. The amplifier is fed with a current source having $R_s = 10\text{ k}\Omega$ and a load resistance $R_L = 1\text{ M}\Omega$ is connected at the output. Find the transresistance A_{tr} of the feedback amplifier; its input resistance R_{in} ; and its output resistance R_{out} .

PB.44 For the shunt-series feedback amplifier of Fig. PB.44, derive expressions for A , β , A_{tr} , R_{in} , and R_{out} . (The latter between the terminals labeled X-X.) Neglect r_s and the body effect. Evaluate all parameters for $g_{m1} = g_{m2} = 5 \text{ mA/V}$, $R_D = 10\text{ k}\Omega$, $R_s = 10\text{ k}\Omega$, and $R_f = 30\text{ k}\Omega$. Neglect the $X-X$ load resistance. Consider a source-degeneration resistor r_s for Q_1 and R_{in} . (In case $r_s = 20\text{ }\Omega$ and neglecting the body effect, since a source-degeneration resistance R increases R_{in} by approximately $g_m R$.)

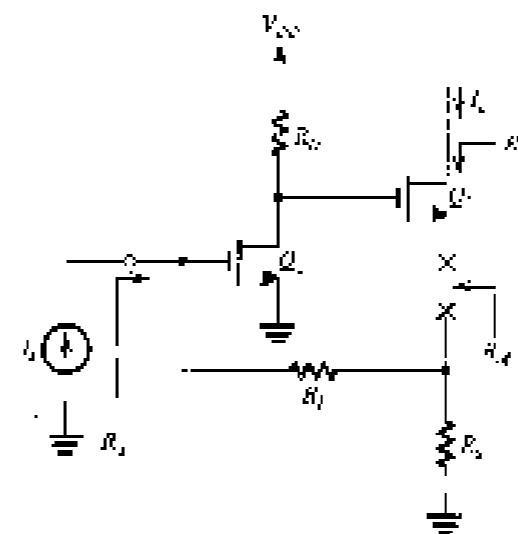


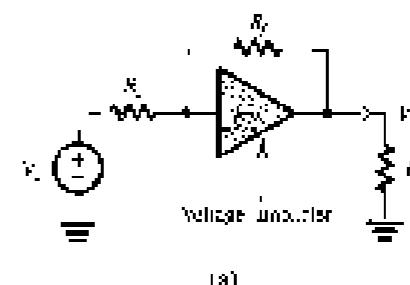
FIGURE PB.44

PB.45 Reconsider the circuit in Fig. PB.44. Now let the drain of Q_2 be connected to V_{DD} , and let the output be taken as the voltage at the source of Q_3 . Now R_f should be considered as part of the A circuit, since the voltage V_o develops across it. Convince yourself that now the amplifier can be viewed as a shunt-series topology with the feedback network comprised of R_f . Find expressions for A , β , A_{tr} , R_{in} , and R_{out} , where R_{in} is the resistance looking back into the output terminal. Neglect r_s and the body effect. Find the values of all parameters for the case in which $g_{m1} = g_{m2} = 5 \text{ mA/V}$, $R_D = 10\text{ k}\Omega$, $R_s = 10\text{ k}\Omega$, and $R_f = 30\text{ k}\Omega$.

PB.46 (a) Show that for the circuit in Fig. PB.46(a) if the loop gain is large, the voltage gain V_o / V_i is given approximately by

$$\frac{V_o}{V_i} \approx -\frac{R_f}{R_s}$$

(b) Using three cascaded stages of the type shown in Fig. PB.46(b) to implement the amplifier, design a feedback amplifier with a voltage gain of approximately -100 V/V . The amplifier is to operate between a source resistance $R_s = 10\text{ k}\Omega$ and a load resistance $R_L = 1\text{ M}\Omega$. Calculate the actual value of V_o / V_i , desired, the input resistance (excluding R_s), and the output resistance (using R_L). Assume that the BJT's have I_C of 1 mA . (Note: In practice, the three amplifier stages are not made identical, for stability reasons.)



(a)

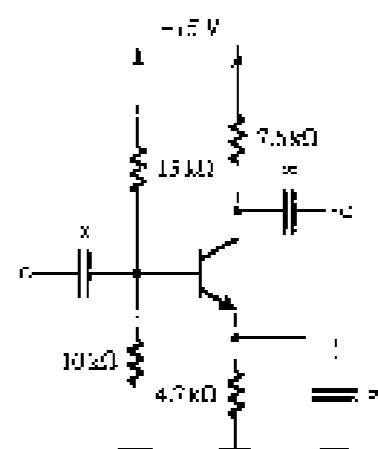


FIGURE PB.46

PB.47 Negative feedback is to be used to modify the characteristics of a particular amplifier for various purposes. Identify the feedback topologies to be used in:

- (a) Input resistance is to be lowered and output resistance raised.
- (b) Both input and output resistances are to be raised.
- (c) Both input and output resistances are to be lowered.

***PB.48** For the circuit of Fig. PB.48, use the feedback method to find the voltage gain V_o / V_i , the input resistance R_{in} , and the output resistance R_{out} . The op-amp has an open-loop gain $A = 10^6 \text{ V/V}$, $R_s = 100\text{ k}\Omega$, $r_o = 1\text{ M}\Omega$.

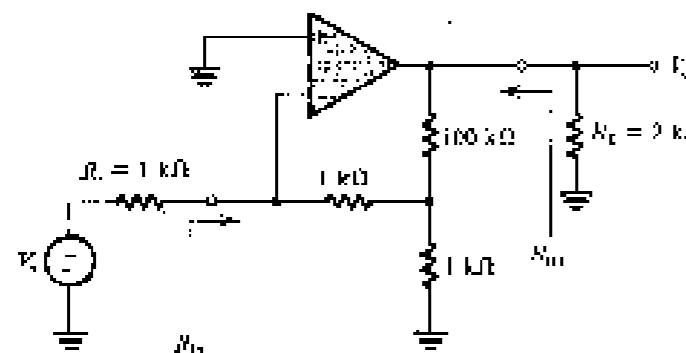


FIGURE P8.48

P8.49 Consider the amplifier of Fig. P8.25(a). It has an output at the emitter of the first current mirror Q_1 . Use the technique for a shunt-shunt feedback amplifier to calculate (V_{out}/V_{in}) and R_{in} . Using this result, calculate A_{av}/A_p . Compare it with the results obtained in Example 8.2.

P8.50 A current amplifier with a short-circuit current gain of 100 A/V, an input resistance of 1 kΩ, and an output resistance of 10 kΩ is connected in a negative-feedback loop employing the shunt-series topology. The feedback network provides a feedback factor $\beta = 0.1 \text{ A/A}$. Looking complete gain when the transistors estimate the current, input resistance, and output resistance of the feedback amplifier.

P8.51 For the amplifier circuit in Fig. P8.51, assume that V_{in} has a zero dc component; find the dc voltages at all nodes and the dc emitter currents of Q_1 and Q_2 . Let the ATIs have $\beta = 100$. Use loop analysis to find V_{out}/V_{in} and R_{in} .

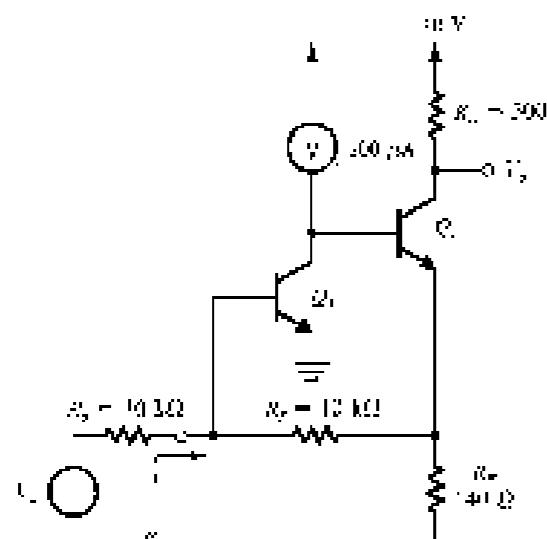


FIGURE P8.51

P8.52 The feedback amplifier of Fig. P8.52 consists of a common-emitter amplifier formed by Q_1 and R_{in} , and a feedback circuit formed by the supporting transistor Q_2 . Use the common-source transistor Q_2 . Note that the bias circuit for Q_2 is not shown. It is required to derive expressions for $A_{av} = V_{out}/V_{in}$, R_{in} , and R_{out} . Assume that C_1 and C_2 are sufficiently small that their leading effect on the open-circuit voltage can be neglected. Also neglect r_o and the body diode effect. Find the values of A_{av} , R_{in} , and R_{out} for the case in which $V_{in} = 5 \text{ mV}$, $R_{in} = 10 \text{k}\Omega$, $C_1 = 0.1 \text{ pF}$, $C_2 = 0.1 \text{ pF}$, and $g_m = 1 \text{ mA/V}$.

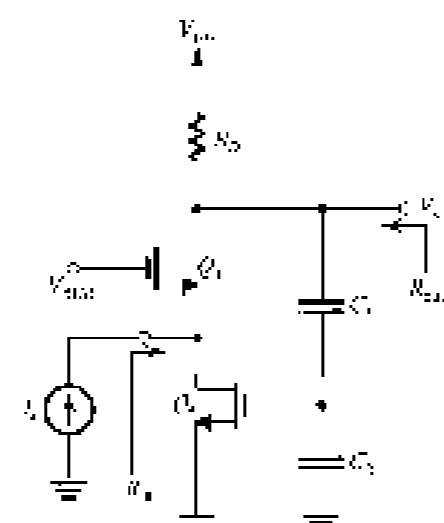


FIGURE P8.52

SECTION 8.7: DETERMINING THE LOOP GAIN

P8.53 Determine the loop gain of the amplifier in Fig. P8.21 by breaking the loop at the gate of Q_2 , i.e., finding the required voltage across the 100-kΩ resistor (which is $-2V_{out}/V_{in}$) to zero. The devices have $|V_A| = 1 \text{ V}$, $k_T V_{GS}^2 = 1 \text{ nA/V}^2$, and $R_E = 100$. The Early voltage magnitude for all devices (including those that implement the current sources) is 100 V. The

current source I_0 has no dependent component. Determine the output resistance R_{out} .

P8.54 It is required to determine the loop gain of the amplifier circuit shown in Fig. P8.35. The most convenient place to break the loop is on the base of Q_2 ; thus, connect a resistance equal to r_e between the collector of Q_1 and ground, apply a test voltage E to the base of Q_2 , and determine the test-voltaged voltage at the collector of Q_1 (with V_{in} set to zero), of course. Show that

$$\begin{aligned} A\beta &= \frac{R_{in}(R_{in} + R_{out} - 1)}{R_{in} + (k_{BS} - 1)r_{in} + R_{in} + (R_E/R_{in}))} \\ &\times \frac{r_{in}R_{in}}{R_{in} + r_{in}} \end{aligned}$$

P8.55 Show that the loop gain of the amplifier is given in Fig. P8.39 as

$$A\beta = g_{m1}(r_{in}/r_{in}) \frac{R_{in}R_{out}}{(R_{in}R_{out}) - 1/g_{m1}}$$

where g_{m1} is the g_m of each of Q_1 and Q_2 .

P8.56 Derive an expression for the loop gain of each of the $\beta = 1$ feedback circuits shown in Fig. P8.36. Assume that the open-loop is modeled by an input resistance R_{in} , an open-circuit voltage gain μ , and an output resistance r_o .

P8.57 Find the loop gain of the feedback amplifier shown in Fig. P8.33 by breaking the loop at the gate of Q_2 (and, of course, setting $\beta = 0$). Use the values given in the statement of Problem 8.11. Determine the value of R_{in} .

P8.58 For the feedback amplifier in Fig. P8.42, derive an expression for the loop gain by breaking the loop at the gate terminal of the MOSFET (and, of course, setting $\beta = 0$). Find the value of the loop gain for the exponential relation given in Problem 8.12.

P8.59 For the feedback amplifier in Fig. P8.44, set $\beta = 0$ and derive an expression for the loop gain by breaking the loop at the gate terminal of transistor Q_2 .

P8.60 For the feedback amplifier in Fig. P8.50, set $\beta = 0$ and derive an expression for the loop gain by breaking the loop at the gate terminal of transistor Q_2 .

SECTION 8.8: THE STABILITY PROBLEM

P8.61 An op-amp designed to have a low-frequency gain of 10³ and a high-frequency response dominated by a single pole at 100 rad/s, occurs, through a manufacturing error, a pair of additional poles at 10,000 rad/s. At what frequency does the total phase shift reach 180°? At this frequency, for what value of β assumed to be frequency independent, does the loop gain reach a value of unity? What is the corresponding value of closed-loop gain at zero (Explain).

P8.62 For the situation described in Problem 8.61, sketch Nyquist plots for $\beta = 10$ and 20. (Put the $\omega = 0$ rad/s, 100 rad/s, 10³ rad/s, 10⁴ rad/s, and ∞ rad/s.)

P8.63 An in-coupling having a low-frequency gain of 10³ and a single-pole roll-off at 10³ rad/s is connected in a negative-feedback loop via a feedback network having a low-pass filter and a two-pole roll-off at 10⁴ rad/s. Find the values of ω above which the closed-loop amplifier becomes unstable.

P8.64 Consider a feedback amplifier for which the open-loop gain $A(\omega)$ is given by

$$A(\omega) = \frac{1000}{(1 + \omega/10^3)(1 + \omega/10^4)}$$

If the feedback factor β is independent of frequency, find the frequency at which the phase shift is 180°, and find the critical value of β at which oscillation will commence.

SECTION 8.9: EFFECT OF FEEDBACK ON THE AMPLIFIER POLES

P8.65 A $\beta = 1$ amplifier having a single pole response with pole frequency 10² Hz and unity-gain frequency of 10 MHz is to be used in a loop whose low-frequency open-loop gain, feedback factor is 0.1. Find the low-frequency gain, the 3-dB frequency, and the unity-gain frequency of the closed-loop amplifier. By what factor does the pole shift?

P8.66 An amplifier having a low-frequency gain of 10³ and poles at 10¹ Hz and 10² Hz is operated in a closed-negative feedback loop with a frequency-independent β .

(a) For what value of β do the closed-loop poles become coincident? At what frequency?

(b) What is the low-frequency gain corresponding to the situation in (a)? What is the ω_c of the closed-loop β at the frequency of the coincident poles?

(c) What is the value of β corresponding to the situation in (a)?

(d) If β is increased by a factor of 10, what are the new pole locations? What is the corresponding pole ω_c ?

P8.67 A dc amplifier has an open-loop gain of 1000 and two poles, a dominant one at 1 kHz and a high-frequency one whose location can be controlled. It is desirable to connect this amplifier in a negative-feedback loop that provides a dc closed-loop gain of 100 and a maximally flat response. Find the required value of β and the frequency at which the second pole should be placed.

P8.68 Recompute Example 8.5 with the circuit in Fig. 8.34 modified to incorporate a so-called tapered cut-off, in which the components include only capacitors in the amplifier. Input are caused to impedance to 1000 and 100. Find expressions for the resulting pole frequency ω_p and β values. For what value of K do the poles coincide? For what value of K does the response become maximally flat? For what value of K does the circuit oscillate?

- 8.67** Three identical logic inverters, each of which can be characterized in its switching region as an inverter having $A = K - R$ and a pole at 10^7 Hz , are connected in a ring. Assuming this is a negative feedback loop with $N = 1$, find the minimum value of K for which the inverter ring may oscillate. What would the frequency of oscillation be for very small signal operation? [Note that it is possible with a ring oscillator operating with relatively large β (β logic levels) at a somewhat lower frequency.]

SECTION 8.10: STABILITY STUDY USING BODE PLOTS

- 8.70** Recompute Example 8.14 for the case of the op amp with a unity gain band of 10 Hz . At what frequency is $|A(j\omega)| = 10$? What is the corresponding phase margin?

- 8.71** Recompute Example 8.14 for the case of a noninverting op amp reducing a second pole at 0.1 Hz . What is now the frequency for which $|A(j\omega)| = 10$? What is the corresponding phase margin? For what values of β is the phase margin 45° or more?

- 8.72** For what phase margin does the gain ranking have a value of 56.7° of 10.8° if 0.1 dB of LFB is used? Use the result in Eq. 8.76.

- 8.73** An amplifier has a dc gain of 10^5 and poles at 10^3 Hz , $4.16 \times 10^3 \text{ Hz}$, and 10^5 Hz . Find the value of β and the corresponding closed-loop gain, for which a phase margin of 45° is obtained.

- 8.74** A two-pole amplifier for which $A = 10^5$ and having poles at 1 MHz and 10 MHz is to be corrected as a differentiator. On the basis of the cut-off-to-half-rate rule, what is the smallest differentiation time constant for which operation is stable? What are the corresponding gain and phase margins?

- 8.75** Use the amplifier described by Fig. 8.97 and with frequency-independent feedback. What is the minimum closed-loop voltage gain that can be obtained for phase margins of 45° and 42° ?

SECTION 8.11: FREQUENCY COMPENSATION

- 8.76** A two-pole amplifier having a first pole at 2 MHz and a dc open-loop gain of 10^5 is to be compensated for closed-loop gains as low as 10^{-2} by the introduction of a new dominant pole. At what frequency must the new pole be placed?

- 8.77** For the amplifier described in Problem 8.76, rather than introducing a new dominant pole we can use additional capacitance at the circuit node at which the pole is formed to reduce the frequency of the fast pole. If the frequency of the second pole is 10 MHz and it remains unchanged while additional capacitance is introduced as mentioned, find the

frequency to which the fast pole must be lowered so that the resulting amplifier is stable for closed-loop gains as low as unity. By what factor is the capacitance at the dominating pole increased?

- 8.78** Recompute the effects of pole splitting by considering Eqs. (8.87) and (8.88) under the conditions that $R_1 = R_2 = R$, $C_1 = C_2 = C$, $C_F = C$, and $A_{OL} = 1000K$, by calculating ω_p , ω_m , and ω_c .

- 8.79** An op amp with open-loop voltage gain of 10^5 A_v and poles at 10^3 Hz , 10^5 Hz , and 10^7 Hz is to be compensated by the addition of a fourth dominant pole to operate stably with unity feedback ($\beta = 1$). What is the frequency of the required dominant pole? The compensation network is to consist of an RC low-pass network placed in the negative feedback path of the op amp. The two resistors are such that a $1\text{ M}\Omega$ resistor can be inserted in series with each of the negative and positive input terminals. What capacitor is required between the negative input and ground to implement the required fourth pole?

- 8.80** An op amp with an open-loop voltage gain of 80 dB and poles at 10^3 Hz , 10^5 Hz , and $1 \times 10^7 \text{ Hz}$ is to be compensated to be stable for unity β . Assume that the op amp incorporates an amplifier equivalent to that in Fig. 8.43, with $C_1 = 150\text{ pF}$, $C_2 = 5\text{ pF}$, and $A_{OL} = 40\text{ mA/V}$, and that β_F is caused by the input circuit and by the output circuit of the amplifier. Find the required value of the compensating Miller capacitor and the new frequency of the control pole.

- **8.81** The op amp in the circuit of Fig. P8.81 has an open-loop gain of 10^5 and a single-pole corner frequency $\omega_{OL} = 10\text{ rad/s}$.
- Sketch a Bode plot for the loop gain.
 - Find the frequency at which $|A(j\omega)| = 1$, and find the corresponding phase margin.
 - Find the closed-loop transfer function, including its gain and poles. Sketch a pole-zero plot. Sketch the magnitude of the transfer function versus frequency, and label the important parameters on your sketch.

- 8.82** Use the amplifier described by Fig. 8.97 and with frequency-independent feedback. What is the minimum closed-loop voltage gain that can be obtained for phase margins of 45° and 42° ?

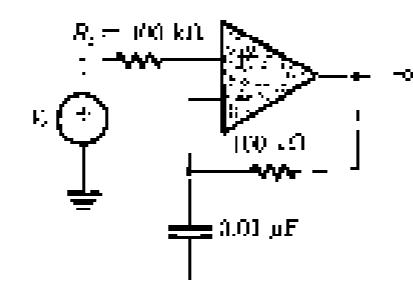


FIGURE P8.81

CHAPTER 9

Operational-Amplifier and Data-Converter Circuits

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9.1.1 Two-Stage CMOS Op-Amp	9.2	9.7.1 D/A Converters
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INTRODUCTION

Analog ICs include operational amplifiers, analog multipliers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, phase-locked loops, and a variety of other, more specialized functional blocks. All these analog subsystems are constructed internally using the basic building blocks we have studied in earlier chapters, including single-stage amplifiers, differential pairs, current mirrors, and MOS switches.

In this chapter, we shall survey the internal circuitry of the most important analog ICs: namely, operational amplifiers and data converters. The terminal characteristics and circuit applications of op amps have already been covered in Chapter 8. Here, our objective is to expose the reader to some of the ingenious techniques that have evolved over the years for combining elementary analog circuit building blocks to realize a complete op amp. We shall study both CMOS and bipolar op amps. The CMOS op-amp circuits considered here application in the

design of analog and mixed-signal VLSI circuits. Because these op amps are usually designed with a specific application in mind, they can be optimized to meet a subset of the list of desired specifications, such as high dc gain, wide bandwidth, or large output-signal swing. In contrast, the bipolar-operating circuit we shall study is of the general-purpose variety and therefore is designed to fit a wide range of specifications. As a result, its circuit represents a compromise between many performance parameters. This 741-type of op amp has been in existence for over 20 years. Nevertheless, its internal circuit remains as relevant and interesting today as it ever was.

The material on the non-inverter circuits presented in this chapter should serve as a bridge between analog circuits, on which we have been concentrating in Chapters 6 and 8, and digital circuits whose study is undertaken in Chapters 10 and 11.

To add to exposing the reader to some of the ideas that make analog IC design such an exciting topic, the example should serve to tie together many of the concepts and methods studied thus far.

9.1 THE TWO-STAGE CMOS OP AMP

The first op-amp circuit we shall study is the two-stage CMOS topology shown in Fig. 9.1. This simple but elegant circuit has become a classic and is used in a variety of forms in the design of VLSI systems. We have already studied this circuit in Section 7.7.1 as an example of a multivoltage CMOS amplifier. We urge the reader to review Section 7.7.1 before proceeding further. Here, our discussion will emphasize the performance characteristics of the circuit and the trade-offs involved in its design.

9.1.1 The Circuit

The circuit consists of two stages. The first stage is formed by the differential pair Q_1-Q_2 , together with its current mirror load Q_3-Q_4 . This differential amplifier circuit, studied in detail in Section 7.5, provides a voltage gain that is typically in the range of 20 V/V to 60 V/V.

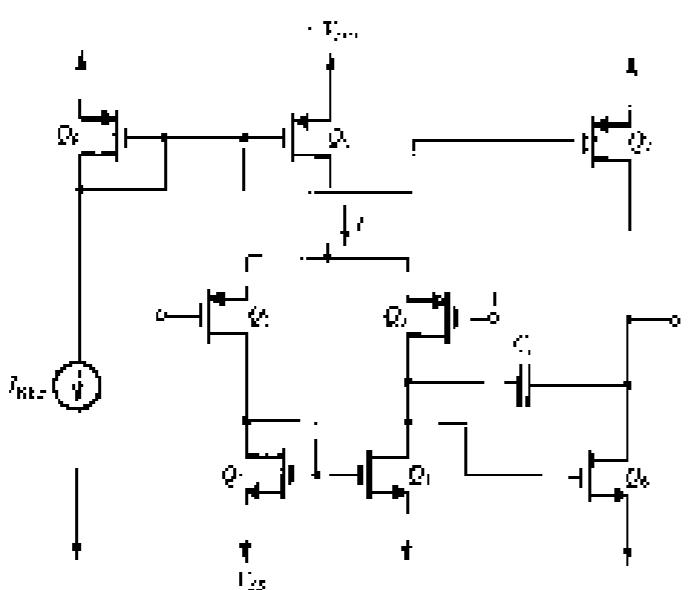


FIGURE 9.1 The basic two-stage CMOS op-amp configuration.

as well as performing conversion from differential to single-ended form while providing a reasonable common-mode rejection ratio (CMRR).

The differential pair is biased by current source Q_5 , which is one of the two output terminals of the current mirror formed by Q_3 , Q_4 , and Q_6 . The current mirror is fed by a reference current I_{REF} , which can be generated by simply connecting a precision resistor external to the chip to the negative supply voltage $-V_{DD}$ or to a more precise negative voltage reference if one is available in the same integrated circuit. Alternately, for applications with more stringent requirements, I_{REF} can be generated using a circuit such as that studied in Section 7.7.1.

The second stage consists of the common-source transistor Q_6 and its compensation load Q_5 . The second stage typically provides a gain of 50 V/V to 80 V/V. In addition, it takes part in the process of frequency compensating the op-amp. From Section 8.1, the reader will recall that to guarantee that the op-amp will operate in a stable manner (as opposed to oscillating when negative feedback of various amounts is applied), the open-loop gain is made to roll off with frequency at the uniform rate of -20 dB/decade. This is often achieved by introducing a pole at a relatively low frequency and arranging for it to dominate the frequency-response determination. In the circuit we are studying, this is implemented via a compensated capacitance C_C connected in the negative-feedback path of the second-stage amplifying transistor Q_6 . As will be seen, C_C together with the much smaller compensation capacitor C_{COMP} (accessibly Miller multiplied by the gain of the second stage), and the resulting impedance at the input of the second stage interact with the load resistance there to provide the required dominant pole (more on this later).

Unless properly designed, the CMOS op-amp circuit of Fig. 9.1 can exhibit a systematic output dc offset voltage. This point was discussed in Section 7.7.1, where it was found that the dc offset can be eliminated by arranging for V_{DD} to satisfy the following constraint:

$$\frac{(W/L)_2}{(W/L)_1} = 2 \frac{(W/L)_4}{(W/L)_3} \quad (9.1)$$

9.1.2 Input Common-Mode Range and Output Swing

Refer to Fig. 9.1 and consider what happens when the two input terminals are tied together and connected to a voltage $V_{IN,0}$. The lowest value of $V_{IN,0}$ has to be sufficiently large to keep Q_1 and Q_2 in saturation. Thus, the lowest value of $V_{IN,0}$ should not be lower than the voltage at the drain of Q_1 ($V_{DS1} = -V_{DD} + V_{IN,0} - V_{DS2}$) by more than $|V_{GS1}|$, thus

$$V_{IN,0} \geq V_{DS1} + |V_{GS1}| = V_{IN,0} - |V_{GS1}| \quad (9.2)$$

The highest value of $V_{IN,0}$ should ensure that Q_2 remains in saturation; that is, the voltage across Q_2 , V_{DS2} , should not decrease below $V_{IN,0}$. Equivalently, the voltage at the drain of Q_2 should not go higher than $V_{IN,0} - V_{DS2}$. Thus the upper limit of $V_{IN,0}$ is

$$V_{IN,0} \leq V_{DS2} = V_{IN,0} - V_{GS2}$$

or equivalently

$$V_{IN,0} \leq V_{DS2} + |V_{GS2}| = V_{IN,0} + |V_{GS2}| \quad (9.3)$$

The expressions in Eqs. (9.2) and (9.3) can be combined to express the input common-mode range as

$$-V_{GS1} + V_{DS2} + |V_{GS2}| \leq V_{IN,0} \leq V_{IN,0} + |V_{GS1}| + |V_{GS2}| \quad (9.4)$$

As expected, the overdrive voltages, which are important design parameters, subtract from the DC supply voltages, thereby reducing the input common-mode range. It follows that from a $V_{IN,0}$ range point-of-view, it is desirable to select the values of V_{GS} as low as possible.

The extent of the signal swing allowed at the output of the op-amp is limited at the lower end by the need to keep Q_1 saturated and at the upper end by the need to keep Q_2 saturated, thus

$$-V_{\text{DD}} + V_{\text{DD}} \leq v_{\text{out}} \leq V_{\text{DD}} + V_{\text{DD}}$$
 (9.5)

Once again we observe that to achieve a wide range for the output voltage swing we need to select values for V_{DD} of Q_1 and Q_2 as low as possible. This requirement, however, is compromised by the need to have a high cut-off frequency (f_c) for Q_1 . From Table 6.3 and the corresponding discussion in Section 6.2.3, we know that f_c is proportional to V_{DD} ; thus the high-frequency performance of a MOSFET improves with the increase of the operating voltage at which it is operated.

An important requirement of an op-amp circuit is that it is possible for its output terminal to be connected back to its negative input terminal so that a unity-gain amplifier is obtained. For such a connection to be possible, there must be a symmetrical overlap between the DC bias voltage of v_{out} and the allowable range of V_{DD} . This is usually the case in the CMOS amplifier circuit under study.

EXERCISE

- 9.1 For a particular design of the two-stage CMOS op-amp of Fig. 9.1, the MOSFETs used in the first stage (except for Q_1 and Q_2) are operated with supply voltages of ± 1.5 V, and the transconductances of Q_1 and Q_2 are 10 times higher than those of the other transistors. Find the input common-mode range and the range allowed for v_{out} , given that $V_{\text{DD}} = 1.5$ V, $V_{\text{DD}} = -1.5$ V, $I_{\text{DD}} = 10 \mu\text{A}$, $R_{\text{in}} = 100 \text{ k}\Omega$, $C_{\text{in}} = 100 \text{ pF}$, $C_{\text{out}} = 100 \text{ pF}$, $R_{\text{load}} = 10 \text{ k}\Omega$, and $f_c = 100 \text{ Hz}$.

9.1.3 Voltage Gain

To determine the voltage gain and the frequency response, consider a simplified equivalent circuit model for the small-signal operation of the CMOS amplifier (Fig. 9.2), where each of the two stages is modeled as a transconductance amplifier. As expected, the input resistance is practically infinite:

$$R_{\text{in}} = \infty$$

The first-stage transconductance G_{v1} is equal to the transconductance of each of Q_1 and Q_2 (see Section 7.5).

$$G_{\text{v1}} = g_{m1} r_{\text{ds1}} = g_{m2} r_{\text{ds2}} \quad (9.6)$$

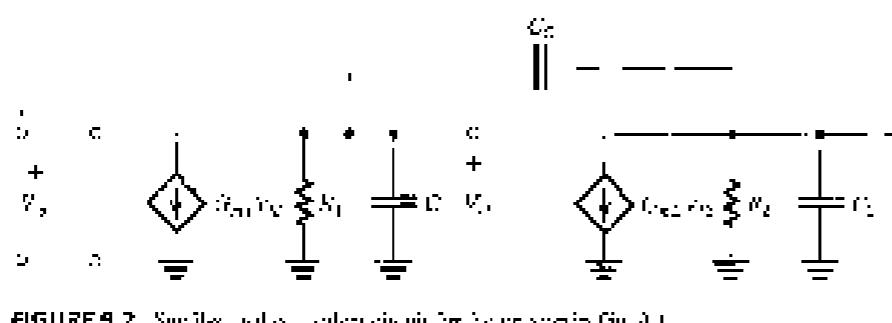


FIGURE 9.2 Simplified equivalent circuit for the op-amp in Fig. 9.1.

Since Q_1 and Q_2 are operated at equal drain currents ($I/2$) and equal overdrive voltages,

$$V_{\text{DD}} \sim V_{\text{DD}}$$

$$G_{\text{v1}} = \frac{2(I/2)}{V_{\text{DD}}} = \frac{I}{V_{\text{DD}}} \quad (9.7)$$

Resistance R_1 represents the output resistance of the first stage. Thus

$$R_1 = r_{\text{ds1}} \parallel r_{\text{ds2}} \quad (9.8)$$

where

$$r_{\text{ds}} = \frac{|V_{\text{DD}}|}{I/2} \quad (9.9)$$

and

$$r_{\text{ds}} = \frac{V_{\text{DD}}}{I/2} \quad (9.10)$$

The DC gain of the first stage is thus

$$A_1 = -G_{\text{v1}} R_1 \quad (9.11)$$

$$= -g_{m1}(r_{\text{ds1}} \parallel r_{\text{ds2}}) \quad (9.12)$$

$$= -\frac{I}{V_{\text{DD}}} \left[\frac{1}{r_{\text{ds1}}} + \frac{1}{r_{\text{ds2}}} \right] \quad (9.13)$$

Observe that the magnitude of A_1 is increased by operating the differential-pair transistors Q_1 and Q_2 at a low overdrive voltage, and by choosing a longer channel length to obtain a larger drain voltage, $|V_{\text{DD}}|$. Both actions, however, degrade the frequency response of the amplifier (see Table 6.3 and the corresponding discussion in Section 6.2.3).

Returning to the equivalent circuit in Fig. 9.2 and leaving for discussion of the various model capacitances until the next section, we note that the second-stage transconductance G_{v2} is given by

$$G_{\text{v2}} = g_{m2} r_{\text{ds2}} = \frac{2I_{\text{DD}}}{V_{\text{DD}}} \quad (9.14)$$

Resistance R_2 represents the output resistance of the second stage. Thus

$$R_2 = r_{\text{ds2}} \parallel r_{\text{ds3}} \quad (9.15)$$

where

$$r_{\text{ds}} = \frac{|V_{\text{DD}}|}{I_{\text{DD}}} \quad (9.16)$$

and

$$r_{\text{ds}} = \frac{|V_{\text{DD}}|}{I_{\text{DD}}} = \frac{|V_{\text{DD}}|}{I_{\text{DD}}} \quad (9.17)$$

The voltage gain of the second stage can now be found as

$$A_2 = -G_{\text{v2}} R_2 \quad (9.18)$$

$$= -g_{m2}(r_{\text{ds2}} \parallel r_{\text{ds3}}) \quad (9.19)$$

$$= -\frac{2}{V_{\text{DD}}} \left[\frac{1}{r_{\text{ds2}}} + \frac{1}{r_{\text{ds3}}} \right] \quad (9.20)$$

Here again we observe that to increase the magnitude of A_2 , C_6 has to be operated at a low overdrive voltage, and the channel lengths of ϕ_3 and ϕ_4 should be made longer. Both these actions, however, would reduce the amplitude bandwidth, which presents the designer with an important trade-off.

The overall dc voltage gain can be found as the product $A_1 A_2$,

$$\begin{aligned} A_3 &= A_1 A_2 \\ &= G_{v1} R_1 G_{v2} R_2 \end{aligned} \quad (9.21)$$

$$= g_{o1} (r_{sd1} \| r_{sd2} g_{os1} r_{sd1} r_{sd2}) \quad (9.22)$$

Note that A_3 is of the order of $(g_{os1})^2$. Thus the maximum value of A_3 will be in the range of 500 V/V to 5000 V/V.

Finally, we note that the output resistance of the op-amp is equal to the output resistance of the second stage,

$$R_o = r_{sd1} \| r_{sd2} \quad (9.23)$$

Hence R_o can be large (i.e., in the transconductance range). Nevertheless, since most CMOS op-amps are rarely required to drive heavy loads, the large open-loop output resistance is usually not an important issue.

Example

Design a two-stage CMOS op-amp with a total voltage gain of 1000 V/V and a unity-gain frequency of $f_u = 100$ Hz. Assume that the first stage has a voltage gain of 100 V/V and a unity-gain frequency of $f_u = 10$ Hz. The second stage has a voltage gain of 10 V/V and a unity-gain frequency of $f_u = 100$ Hz. The input voltage is $v_i = 10 \mu\text{V}$.

9.1.4 Frequency Response

Refer to the equivalent circuit in Fig. 9.2. Capacitance C_1 is the total capacitance between the output node of the first stage and ground, thus

$$C_1 = C_{1st} + C_{2st} + C_{2nd} + C_{2,0} \quad (9.24)$$

Capacitance C_2 represents the total capacitance between the output node of the op-amp and ground and includes whatever load capacitance C_L that the amplifier is required to drive, thus

$$C_2 = C_{2st} + C_{2nd} + C_{2,0} + C_L \quad (9.25)$$

Usually, C_2 is larger than the various capacitances, with the result that C_2 becomes much larger than C_1 . Finally, note that $C_{2,0}$ should be shown in parallel with C_L but has been ignored because C_L is usually much larger.

The equivalent circuit of Fig. 9.2 was analyzed in detail in Section 7.3.1, where it was found that it has two poles and a positive real-axis zero with the following approximate frequencies:

$$f_{p1} = \frac{1}{2\pi R_1 C_{1st} R_2 C_2} \quad (9.26)$$

$$f_{p2} = \frac{G_{v2}}{2\pi C_2} \quad (9.27)$$

$$f_z = \frac{G_{v1}}{2\pi C_1} \quad (9.28)$$

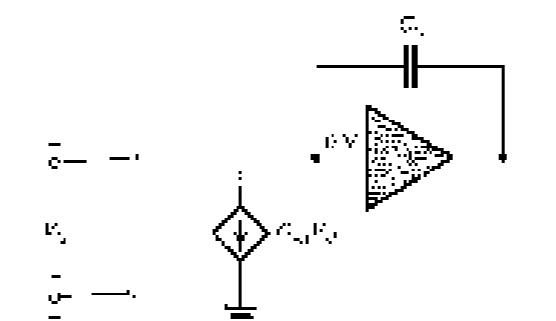


FIGURE 9.3 An equivalent high-frequency equivalent circuit of the two-stage op-amp. This circuit applies for frequencies $f > f_u$.

Next, f_u is the dominant pole caused by the interaction of Miller-influenced C_1 [i.e., $C + G_{v1} R_1 C_1 \approx G_{v1} R_1 C_1$] and R_1 . To achieve the goal of a uniform -20 dB/octave gain roll-off down to 0 dB, the unity-gain frequency f_u

$$f_u = |A_1| f_{p1} \quad (9.29)$$

$$= \frac{G_{v1}}{2\pi C_1} \quad (9.30)$$

must be lower than f_{p1} and f_z , thus the design must satisfy the following two conditions

$$\frac{G_{v1}}{C_1} < \frac{G_{v2}}{C_2} \quad (9.31)$$

and

$$G_{v1} < G_{v2} \quad (9.32)$$

Simplified Equivalent Circuit. The uniform -20 dB/octave gain roll-off obtained at frequencies $f > f_u$ suggests that at these frequencies, the op-amp can be represented by the simplified equivalent circuit shown in Fig. 9.3. Observe that this successive amplification is based on the assumption that the gain of the second stage, $|A_2|$, is large, and hence a virtual ground appears at the input terminal of the second stage. The second stage therefore effectively acts as an integrator but is fed with the output current signal of the first stage, $G_{v1} v_+$. Although derived for the CMOS amplifier, this simplified equivalent circuit is general and applies to a variety of two-stage op-amps, including the first two stages of the 741-type bipolar op-amp studied later in this chapter.

Phase Margin. The frequency compensation scheme outlined in the two-stage CMOS amplifier is of the pole-splitting type, studied in Section 8.11. It provides a dominant low-frequency pole with frequency f_{p1} and shifts the second pole beyond f_u . Figure 9.4 shows a representative Bode plot for the gain magnitude and phase. Note that at the unity-gain frequency f_u , the phase lag exceeds the 90° caused by the dominant pole at f_{p1} . This so-called excess phase shift is due to the second pole.

$$\phi_{p2} = -\tan^{-1} \left(\frac{f_u}{f_{p2}} \right) \quad (9.33)$$

and the right-half-plane zero,

$$\phi_z = -\tan^{-1} \left(\frac{f_z}{f_u} \right) \quad (9.34)$$

Thus the phase lag at $f_u = f_z$ will be

$$\phi_{\text{sum}} = 90^\circ + \tan^{-1} \left(\frac{f_u}{f_{p2}} \right) - \tan^{-1} \left(\frac{f_z}{f_u} \right) \quad (9.35)$$

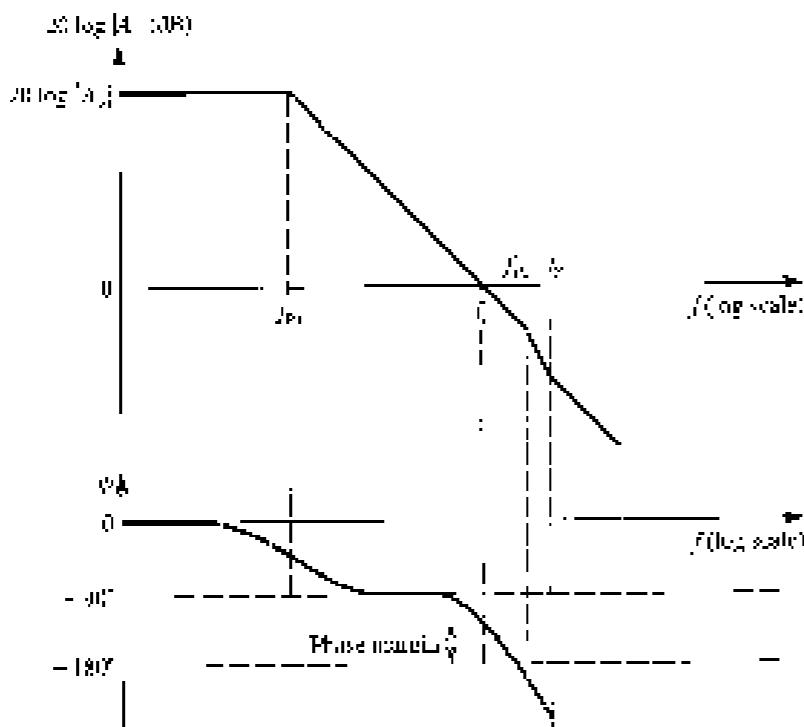


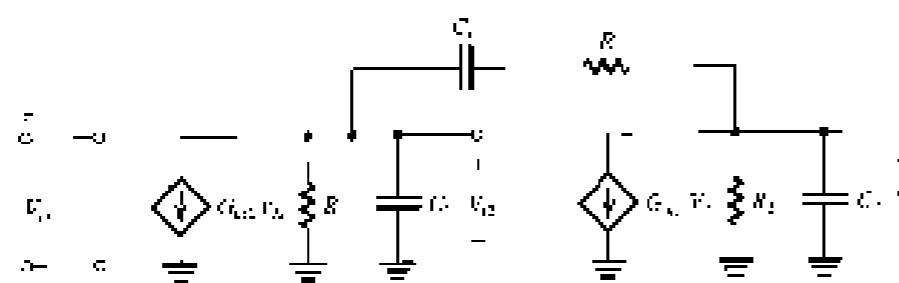
FIGURE 9.4 Typical frequency response of the two-stage op amp.

and thus the phase margin will be

$$\begin{aligned} \text{Phase margin} &= 180^\circ - \phi_{\text{margin}} \\ &= 90^\circ - \tan^{-1}(f_p/f_{\text{margin}}) - \tan^{-1}(f_p/f_p) \end{aligned} \quad (9.30)$$

From our study of the stability of feedback amplifiers in Section 8.10.2, we know that the magnitude of the phase margin significantly affects the closed-loop gain. Therefore obtaining a desired minimum value of phase margin is usually a design requirement.

The problem of the additional phase lag provided by the zero has a rather simple and elegant solution. By including a resistance R in series with C_p , as shown in Fig. 9.5, the transmission zero can be moved to other non-harmful locations. To find the new location of the

FIGURE 9.5 Small-signal equivalent circuit of the op amp in Fig. 9.1 with a resistance R included in series with C_p .

transmission zero, set $V_2 = 0$. Then, the current through C_p will be $V_2 / (R + 1/G_{v2})$, and a node equation at the output yields

$$\frac{V_2}{R + \frac{1}{G_{v2}}} = G_{o2} V_2$$

Thus the zero is now at

$$f_p = 1/G_{v2} \left(\frac{1}{R} + R \right) \quad (9.31)$$

We observe that by selecting $R = 1/G_{v2}$, we can place the zero at infinite frequency. An even better choice would be to select R greater than $1/G_{v2}$, thus placing the zero at a negative real-axis location where the phase it introduces adds to the phase margin.

EXERCISE

- (1) A typical open-loop gain of this CMOS op amp is $A_{OL} = 1.1 \times 10^5$ with a unity-gain frequency $f_p = 100$ Hz, a corner frequency $f_{p2} = 100$ kHz, and $G_{v2} = 1$ dB.
- (2) The gain margin of the two-stage op amp is -100 dB. What is the loop gain at the open-loop corner frequency?
- (3) The gain margin of the two-stage CMOS op amp is -100 dB. What is the loop gain at the unity-gain frequency?
- (4) Find the frequency of the second pole and hence find the excess phase lag at $\omega = 1$ rad/s caused by this second pole. Use the resulting phase margin, assuming that the margin in (3) persists.
- (5) At 100 Hz, 30 dB is 33.8 dB, 100 kHz is 12.4 dB. There is a 10 dB difference between the two corner frequencies. What is the phase margin at 100 Hz?

9.1.5 Slew Rate

The slew-rate limitation of op amps is discussed in Chapter 2. Here, we shall illustrate the origin of the slewing phenomenon in the context of the two-stage CMOS amplifier under study.

Consider the unity-gain follower of Fig. 9.6 with a step of say, 1 V applied at the input. Because of the amplifier dynamics, its output will not change at zero time. Thus, immediately after the input is applied, the entire value of the step will appear as a differential signal between the two output terminals. In all likelihood, such a large signal will exceed the voltage required to turn off one side of the pair (Q_2, V_{DD}) (see Fig. 7.6) and switch the entire bias

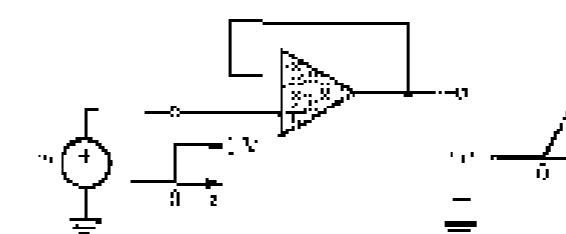


FIGURE 9.6 A unity-gain follower with a large step input. Since the output voltage cannot change instantaneously, a large differential voltage appears between the op-amp input terminals.

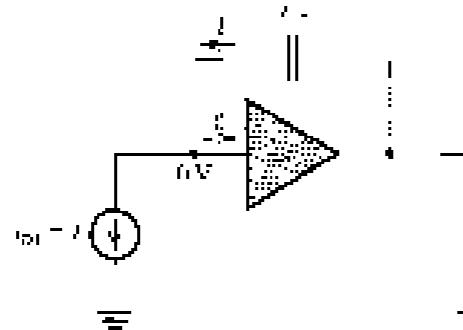


FIGURE 9.7 Model of the two-stage CMOS op amp of Fig. 9.1 where a large differential voltage is applied.

current I to the other side. Referenced to Fig. 9.1 shows that for our example, Q_2 will turn off, and Q_3 will conduct the entire current I . Thus Q_3 will sink a current I that will be pulled from C_{out} , as shown in Fig. 9.7. However, we find in Fig. 9.3, we are modeling the second stage as an ideal integrator. We see that the output voltage will be a ramp with a slope of I/C_{out} .

$$v_{\text{out}}(t) = \frac{I}{C_{\text{out}}} t \quad (9.34)$$

Thus the slew rate, SR, is given by

$$\text{SR} = \frac{I}{C_{\text{out}}} \quad (9.35)$$

It should be pointed out, however, that this is a rather simplified model of the slowing process.

Relationship Between SR and f_s . A simple relationship exists between the unity-gain bandwidth, f_s , and the slew rate SR. This relationship can be found by combining Eqs. (9.30) and (9.35) and noting that $G_{\text{out}} = g_m = I/V_{\text{DD}}$, to obtain

$$\text{SR} = 2\pi f_s V_{\text{DD}} \quad (9.40)$$

or equivalently,

$$\text{SR} = V_{\text{DD}} g_m \quad (9.41)$$

Thus, for a given v_{DD} , the slew rate is determined by the overdrive voltage at which the first-stage transistors are operated. A higher slew rate is obtained by operating Q_1 and Q_2 at a larger V_{DD} . Now, for a given bias current I , a larger V_{DD} is obtained if Q_1 and Q_2 are p-channel devices. This is an important reason for using p-channel rather than n-channel devices in the first stage of the CMOS op-amp. Another reason is that it allows the second stage to employ n-channel devices. Now, since n-channel devices have greater transconductances than corresponding p-channel devices, G_{out} will be high, resulting in a higher second-pole frequency and a correspondingly higher f_s . However, the price paid for these improvements is a lower G_{out} and hence a lower dc gain.

EXERCISE

- Find SR for the CMOS op-amp of Fig. 9.1 with $V_{\text{DD}} = 20$ V, $I = 100 \mu\text{A}$, and $C_{\text{out}} = 100 \text{ pF}$.

$$\text{Ans. } 350 \text{ V/s, } 200 \text{ pA}$$

We conclude our study of the two-stage CMOS op-amp with a design example. Let it be required to design the circuit to obtain a dc gain of 4000 V/V. Assume that the available fabrication technology is of the 0.5- μm type for which $V_s = V_{\text{DD}} = 0.5$ V, $k'_n = 200 \text{ nA/V}^2$, $k'_p = 80 \text{ nA/V}^2$, $V_{\text{DD}} = |V_{\text{DD}}| = 20$ V/ μm , and $V_{\text{DD}} - V_0 = 1.65$ V. To achieve a reasonable dc gain per stage, use $I = 100 \mu\text{A}$ for each device. Also, for simplicity, operate all devices at the same $|V_{\text{DD}}|$. In the range of 0.2 V to 0.4 V, $I = 200 \mu\text{A}$, and to obtain a higher G_{out} and hence a higher f_s , use $I_D = 0.5 \text{ mA}$. Specify the W/L ratios for all transistors. Also, give the values required for the input-voltage mode range, the maximum possible output swing, R_{L} , and R_{in} . If $C_1 = 0.1 \text{ pF}$ and $C_2 = 0.8 \text{ pF}$, find the required values of C_{out} and the static resistance R_{L} to allow the requirement $\text{SR} \geq 100 \text{ V/s}$ and to obtain the highest possible f_s consistent with a power budget of 15%. Evaluate the values required for f_s and SF .

Solution

Using the voltage-gain expression in Eq. (9.22),

$$\begin{aligned} A_v &= g_m (k'_n + k'_p) (V_{\text{DD}}/2) (1/f_s)^{1/2} \\ &= \frac{1}{2} k'_n V_{\text{DD}} \times \frac{1}{2} \times \frac{V_{\text{DD}}}{(I/2)} \times \frac{1}{2} \times \frac{V_{\text{DD}}}{I_{\text{DD}}} \\ &= \left(\frac{V_{\text{DD}}}{V_{\text{DD}}} \right)^2 \end{aligned}$$

∴ obtain $A_v = 4000$, given $V_{\text{DD}} = 20$ V,

$$\begin{aligned} 4000 &= \frac{V_{\text{DD}}}{V_{\text{DD}}} \\ V_{\text{DD}} &= 0.516 \text{ V} \end{aligned}$$

To obtain the required W/L ratios of Q_1 and Q_2 ,

$$\begin{aligned} I_{\text{DD}} &= \frac{1}{2} k'_n \left(\frac{V_{\text{DD}}}{I_{\text{DD}}} \right)^2 V_{\text{DD}} \\ 100 &= \frac{1}{2} \times 200 \left(\frac{V_{\text{DD}}}{I_{\text{DD}}} \right)^2 \times 0.5 \times 10^3 \end{aligned}$$

Thus,

$$\left(\frac{V_{\text{DD}}}{I_{\text{DD}}} \right)^2 = 25 \mu\text{m}$$

and

$$\left(\frac{V_{\text{DD}}}{I_{\text{DD}}} \right)^2 = \frac{25 \mu\text{m}}{1 \mu\text{m}}$$

For Q_1 and Q_2 , we write

$$100 = \frac{1}{2} \times 200 \left(\frac{V_{\text{DD}}}{I_{\text{DD}}} \right)^2 \times 0.21 S^2$$

To obtain

$$\left(\frac{V_o}{I_{Q_1}}\right) = \left(\frac{V_o}{I_{Q_2}}\right) = \left(\frac{10 \text{ mV}}{1 \text{ pA}}\right)$$

For Q_1 ,

$$200 = \frac{1}{2} \times 80 \left(\frac{V_o}{I_{Q_1}}\right) \times 0.316^2$$

Thus,

$$\left(\frac{V_o}{I_{Q_1}}\right) = \left(\frac{50 \text{ mV}}{1 \text{ pA}}\right)$$

Since Q_1 is required to conduct 200 nA, its β/γ ratio should be 2.5 times that of Q_2 ,

$$\left(\frac{V_o}{I_{Q_1}}\right) = 2.5 \left(\frac{V_o}{I_{Q_2}}\right) = \left(\frac{125 \text{ mV}}{1 \text{ pA}}\right)$$

For Q_2 we write

$$500 = \frac{1}{2} \times 200 \times \left(\frac{V_o}{I_{Q_2}}\right) \times 0.316^2$$

Thus,

$$\left(\frac{V_o}{I_{Q_2}}\right) = \frac{20 \text{ mV}}{1 \text{ pA}}$$

Finally, we'll solve $i_{Q_2} = 20 \mu\text{A}$, thus

$$\left(\frac{V_o}{I_{Q_2}}\right) = 0.1 \left(\frac{V_o}{I_{Q_2}}\right) = 2 \text{ pA}$$

The input common-mode range will be found using the expression in Eq. (9.4) as

$$1.53 \text{ V} \leq V_{CM} \leq 0.52 \text{ V}$$

The maximum signal swing achievable at the output is found using the expression in Eq. (9.5) as

$$1.53 \text{ V} \leq v_o \leq 1.23 \text{ V}$$

The input resistance is assumed infinite, and the output resistance is

$$R_o = r_{o2} | i_{Q_2} = \frac{1}{2} \times \frac{25}{0.5} = 25 \text{ k}\Omega$$

To determine f_T , we use Eq. (9.27) and substitute for G_{m2} ,

$$G_{m2} = g_{m2} = \frac{2i_{Q_2}}{V_{DD}} = \frac{2 \times 0.5}{0.316} = 3.2 \text{ mA/V}$$

Thus,

$$f_T2 = \frac{1.2 \times 10^3}{4\pi \times 0.8 \times 10^{-2}} = 9.27 \text{ MHz}$$

To derive the transmission zero at $s = -s_0$, we select the value of R as

$$R = \frac{1}{G_{m2}} = \frac{1}{3.2 \times 10^{-2}} = 31.25 \text{ }\Omega$$

For a phase margin of 75°, the phase shift, $\phi(0)$, between output v_o and i_{Q_2} must be 15°, and so

$$\tan^{-1} \frac{i_o}{f_{T2}} = 15^\circ$$

Thus,

$$f = 637 \times \tan 15^\circ = 171 \text{ MHz}$$

The value of C_V can be found using Eq. (9.30),

$$C_V = \frac{G_{m2}}{2\pi f}$$

where

$$G_{m2} = g_{m2} = \frac{\lambda \cdot 100 \text{ nA}}{0.1 \cdot 6 \text{ V}} = 0.65 \text{ mA/V}$$

Thus,

$$C_V = \frac{0.65 \times 10^{-3}}{2\pi \times 171 \times 10^9} = 0.6 \text{ pF}$$

The value of ΔP can now be found using Eq. (9.40) as

$$\begin{aligned} \Delta P &= 2\pi \times 1.1 \times 10^3 \times 0.316 \\ &= 340 \text{ V/Hz} \end{aligned}$$

9.2 THE FOLDED-CASCODE CMOS OP AMP

In this section we study another type of CMOS op-amp circuit: the folded cascode. The circuit is based on the folded-cascode amplifier studied in Section 6.8.6. There, it was mentioned that although it is composed of a CS transistor and a CB transistor, it appears to polarity, the folded cascode configuration is generally considered to be a single-stage amplifier. Similarly, the op-amp circuit fully based on the cascode configuration is considered to be a single-stage op amp. Nevertheless, it can be designed to provide performance parameters better than equal and in some respects exceed those of the two-stage topology studied in the preceding section. Indeed, the folded-cascode op-amp topology is currently as popular as the two-stage structure. Furthermore, the folded-cascode configuration can be used in conjunction with the two-stage structure to provide performance levels higher than those available from either circuit alone.

9.2.1 The Circuit

Figure 9.8 shows the structure of the CMOS folded-cascode op-amp. Here, Q_1 and Q_2 form the input differential pair, and Q_3 and Q_4 are the cascode transistors. Recall that for differential input signals, each of Q_1 and Q_2 acts as a common-source amplifier. Also note that the gate terminals of Q_3 and Q_4 are connected to a constant DC voltage ($V_{DD/2}$) and hence are

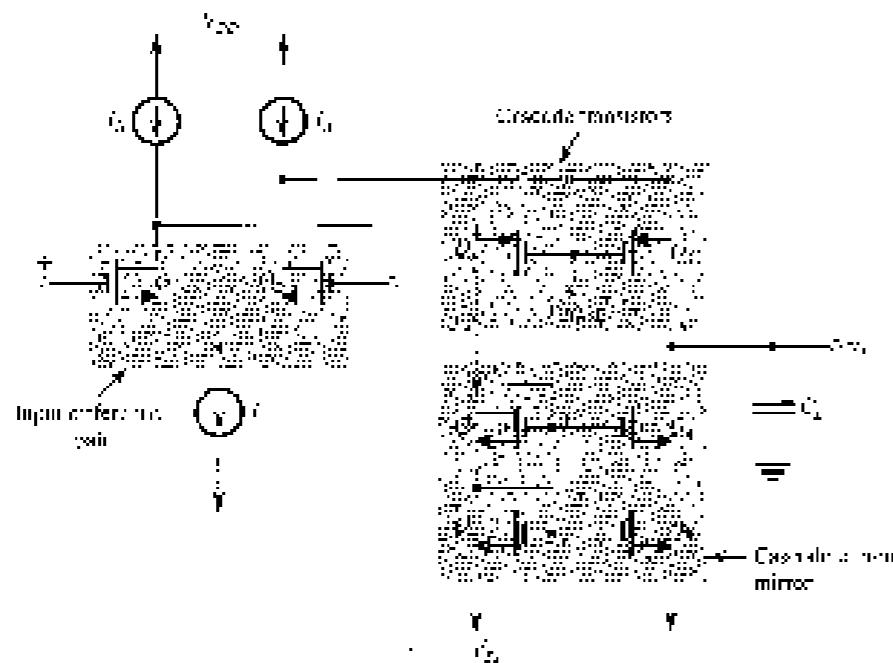


FIGURE 9.8 Symmetrically clamped 14-bit weak CMOS inverter

at signal ground. Thus, for different $\pm I$ input signals, each of the transistor pairs Q_1 - Q_2 and Q_3 - Q_4 acts as a triode-cascode amplifier, such as the one in Fig. 6.45. Note that the input differential pair is biased by a constant current source I . Thus each of Q_1 and Q_2 is operating at a bias current $I/2$. A node equation at each of their drains shows that the bias current of each of Q_3 and Q_4 is $(I_v - I/2)$. Selecting $I_v = I$ forces all transistors to operate at the same bias current of $I/2$. You realize that will be explained shortly, however, the value of I_b is usually made somewhat greater than I .

As we learned in Chapter 6, if the full advantage of the high output-resistance achieved through cascading is to be realized, the output resistance of the current source load must be equally high. This is the reason for using the constant-current mirror Q_2 to Q_4 in the circuit of Fig. 8.9. (This current-mirror circuit was studied in Section 6.12.) Initially, note that capacitance C_o denotes the total capacitance at the output node. It includes the internal transistor capacitances, an actual load capacitance (if any), and possibly an additional capacitance deliberately introduced for the purpose of frequency compensation. In many cases, however, the load capacitance will be rather large, obviating the need to provide additional capacitance to achieve the desired frequency compensation. This topic will be discussed shortly. For the time being, we note that unlike the two-stage circuit, this requires the introduction of a separate compensation capacitor C_o , here the load capacitance contributes to frequency compensation.

A more complete circuit for the CMOS folded-cascode op-amp is shown in Fig. 9.4. Here we see the two transistors Q_3 and Q_4 , which provide the constant bias currents I_B , and transistor Q_{11} , which provides the constant current I_1 utilized for biasing the differential pair. Observe that the details for generating the bias voltages $V_{B1,2,3,4}$, $V_{B11,12,13,14}$, and $V_{B15,16,17,18}$ are not shown. Nevertheless, we are interested in how the values of these voltages are to be selected. Toward that end, we evaluate the input common-mode range and the allowable output swing.

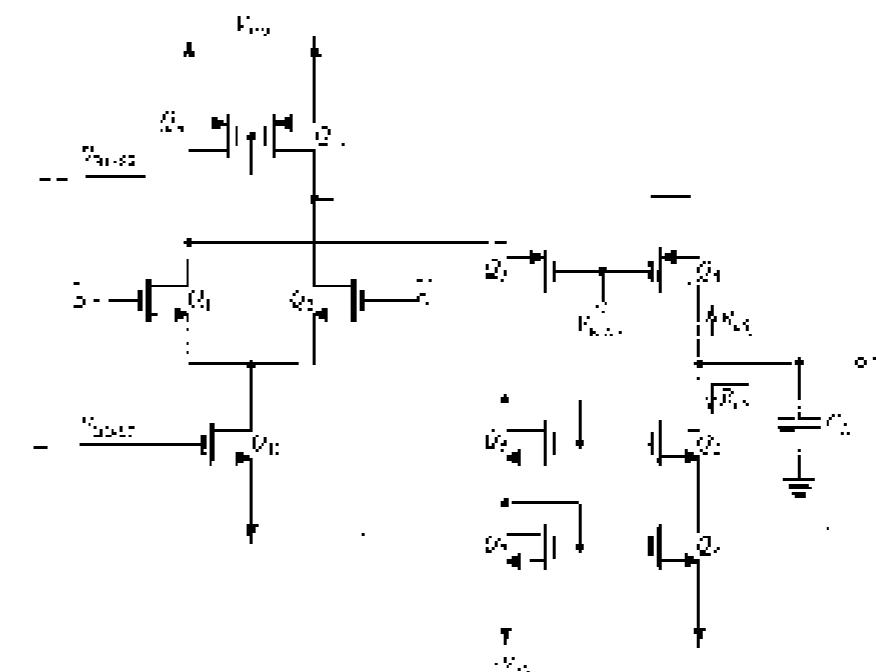


FIGURE 9.9 A more complete circuit for the calcd. cascode CMOS caspice of Fig. 9.8.

9.2.2 Input Common-Mode Range and the Output Voltage Swing

To find the input common mode range, let the two input terminals be tied together and connected to a voltage $V_{IN,2}$. The maximum value of $V_{IN,2}$ is limited by the requirement that Q_1 and Q_2 operate in saturation at 1.0 times. Thus $V_{IN,2}$ should be at most V_D volts above the voltage at the drains of Q_1 and Q_2 . The latter voltage is determined by V_{DSAT} and it is allowed for a voltage drop across Q_1 and Q_2 at least equal to their overdrive voltage, $|V_{OV1}| = |V_{OV2}|$. Assuming that Q_1 and Q_2 are indeed operated at the edge of saturation, $V_{IN,2,max}$ will be

$$V_{\text{ext}} = V_{\text{ext}} - V_{\text{ext}} = V_0 \quad (3.2)$$

which can be larger than V_{HFS} , a significant improvement over the case of the two-stage circuit. The value of V_{HFS} should be selected to yield the required value of α while operating Q_{HFS} and Q_1 at a small value of V_{HFS} (e.g., 0.2 V or so). The minimum value of V_{HFS} is the same as in the case of the two-stage circuit, namely

$$V_{\text{ext},\text{tot}} = -V_{\text{ex}} - V_{\text{ext}} = V_{\text{ext}} + V_{\text{ex}} \quad (9/2)$$

The presence of the threshold voltage V_{th} in this expression indicates that $I_{Q1,Q2}$ is not sufficiently low. Later in this section we shall describe an ingenious technique for solving this problem. For the time being, note that the value of V_{bias} should be selected to minimize the required value of I while operating $Q_{1,2}$ at a low drain-to-source voltage. Combining Eqs. (9.12) and (9.13) provides

$$V_{\text{sp}} = V_{\text{sp},\text{in}} + V_{\text{sp},\text{ex}} = k_1 \leq V_{\text{sp}} \leq V_{\text{sp}} + \beta V_{\text{sp},\text{in}} = k_2 \quad (9.44)$$

The upper end of the allowable range of v_{sp} is determined by the need to maintain Q_{in} and Q_{out} in saturation. Note that Q_{in} will operate in saturation as long as an overdrive setting [$V_{\text{ctrl}} > 0$] appears across it. It follows that to maximize the allowable positive swing of v_{sp} and v_{ctrl} , we

9.2.4 Frequency Response

From our study of the cascode configuration in Section 6.8 we know that one of its advantages is its excellent high-frequency response. It has poles at the input, at the connection between the CS and CC resistors (i.e., at the source terminals of Q_1 and Q_2), and at the output terminal. Normally, the first two poles are at very high frequencies, especially when the resistance of the signal generator that feeds the differential pair is small. Since the primary purpose of CMOS op-amps is to feed capacitive loads, C_L is usually large, and the pole at the output becomes dominant. Thus, if C_L is not large, we can increase it deliberately to give the op-amp a dominant pole. From Eq. 9.10 we can write

$$\frac{V_o}{V_{in}} = \frac{G_o R_o}{1 + sC_o R_o} \quad (9.60)$$

Thus, the dominant pole has a frequency f_p ,

$$f_p = \frac{1}{2\pi C_o R_o} \quad (9.60)$$

and the unity-gain frequency f_u will be

$$f_u = G_o R_o f_p = \frac{G_o}{2\pi C_o} \quad (9.61)$$

From a design point-of-view, the value of C_o should be such that at $f = f_u$ the excess phase resulting from the non-dominant poles is not enough to permit the required phase margin to be achieved. If C_o is not large enough to achieve this purpose, it can be augmented.

It is important to note the different effects of increasing the load resistance or the operation of the two op-amp circuits we have studied. In the two-stage circuit, if C_o is increased, the frequency of the second pole decreases, the excess phase shift at $f = f_u$ increases, and the phase margin is reduced. Here, on the other hand, when C_o is increased, f_u decreases, but the phase margin increases. In other words, a heavier load achieves and increases the bandwidth of the folded-cascode amplifier but does not impair its response (which happens when the phase margin decreases). Of course, if an increase in C_o is anticipated in the two-stage op-amp case, the designer can increase C_2 , thus decreasing f_u and restoring the phase margin to its required value.

9.2.5 Slew Rate

As discussed in Section 8.1.5, slew occurs when a large differential input signal is applied. Refer to Fig. 9.8 and consider the case when a large signal V_{in} is applied so that Q_1 cuts off and Q_2 conducts the entire bias current I . We see that Q_2 will now carry a current ($I_2 = I$) and Q_1 's wT contact a current I_1 . The current mirror will see an input current of $(I_2 - I)$ through G_2 and Q_2 , and thus its output current in the drain of Q_2 will be $I_2 - I$. It follows that at the output node the current flowing into C_L will be $I_o = I_2 - I = I_1 - (I_2 - I) = I$. Thus the output v_o will be a ramp with a slope of I/C_L , which is the slew rate.

$$SR = \frac{I}{C_L} \quad (9.62)$$

Note that the reason for selecting $I_2 > I$ is to avoid turning off the current mirror completely; if the current mirror turns off, the output distortion increases. Typically, I_2 is set 10% to 20% larger than I . Finally, Eqs. 9.6, 9.11, 9.12, and 9.13, can be combined to obtain

the following relationship between SR and i :

$$SR = 2.8i/V_{DDA} \quad (9.63)$$

which is identical to the corresponding relationship in the case of the two-stage design. Note, however, that this relationship applies only when $I_o > I$.



Consider a design of the folded-cascode op-amp of Fig. 9.9 for which $i = 200 \mu A$, $I_o = 250 \mu A$, and $|V_{DDA}|$ for JFET transistors is 2.25 V. Assume that the fabrication process provides $\beta_1 = 100 \mu A/V^2$, $\beta_2 = 40 \mu A/V^2$, $|V_1| = 2.0 \text{ V}/\mu A$, $V_{DS} = V_{GS} = 2.5 \text{ V}$, and $|V_2| = 2.75 \text{ V}$. Let JFET transistors have $L = 1 \text{ } \mu m$ (assuming $n = 4 \times 10^{-14} \text{ cm}^2/\text{V}\cdot\text{s}$ for T_h , η_{nL} , η_1 , and η_2 for all transistors), and the allowable range of $|v_{GS1}|$ and $|v_{GS2}|$ the output voltage swing. Determine the values of A_o , f_u , I_o , and SR. What is the power dissipation of the op-amp?

Solution

From the given values of i and I_o we can determine the drain current I_1 for each transistor. The transconductance of each device is found using

$$\beta_1 = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_o}{V_{DDA}} = 0.25$$

and the drain resistance r_d from

$$r_d = \frac{V_{DS}}{I_D} = \frac{2.5}{I_D}$$

The MOS ratio for each transistor is calculated from

$$\frac{W}{L} = \frac{2I_o}{eV_{DS}}$$

This requires e to be known:

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}
$I_D (\mu A)$	100	100	50	150	150	150	150	150	250	250	250	200
$\beta (\mu A/V^2)$	0.8	0.8	1.2	1.2	1.2	1.2	1.2	1.2	2.0	2.0	2.0	1.6
$ V_1 (V)$	4.0	3.9	3.8	3.9	3.9	3.9	3.9	3.9	3.7	3.7	3.7	3.6
η_1	32	32	27	1.0	48	28	48	48	2.0	2.0	2.0	1.2

Note that for all transistors,

$$z_{v_{GS}} = 250 \text{ V/V}$$

$$z_{v_{DS}} = 1.6 \text{ V}$$

Using the expression in Eq. 9.44, the input common-mode range is found to be

$$-1.25 \text{ V} \leq v_{GS} \leq 2.5 \text{ V}$$

The output voltage swing is found using Eqs. 9.46 and 9.47 to be

$$1.25 \text{ V} \leq v_o \leq 2 \text{ V}$$

To obtain the voltage gain, we last determine R_o using Eq. 9.51 as

$$R_o = 160(250/30) = 9.14 \text{ M}\Omega$$

and R_{in} using Eq. (9.52) as

$$R_{\text{in}} = 21.28 \text{ M}\Omega$$

The output resistance R_{out} can then be found as

$$R_{\text{out}} = R_{\text{L}} + R_{\text{load}} = 0.4 \text{ M}\Omega$$

and the voltage gain:

$$\begin{aligned} A_v &= G_v R_{\text{in}} = 0.8 \times 10^{-3} \cdot 21.28 \times 10^6 \\ &= 5120 \text{ V/V} \end{aligned}$$

The unity-gain bandwidth is found using Eq. (9.64),

$$f_v = \frac{0.5 \times 10^3}{2\pi \times 2 \times 10^6} = 25.5 \text{ MHz}$$

Thus, the dominant-pole frequency must be

$$f_p = \frac{f_v}{A_v} = \frac{25.5 \text{ MHz}}{5120} = 5 \text{ kHz}$$

The slew rate can be determined using Eq. (9.63),

$$SR = \frac{I}{C_f} = \frac{200 \times 10^{-12}}{5 \times 10^{-12}} = 40 \text{ V/ps}$$

Finally, to determine the power dissipation we note that the total current is $500 \mu\text{A} = 0.5 \text{ mA}$, and the rail supply voltage is 5 V, thus

$$P_D = 5 \times 0.5 = 2.5 \text{ mW}$$

9.2.6 Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation

In Section 9.2.2 we found that while the upper limit on the input common-mode range exceeds the supply voltage V_{DD} , the lower limit is significantly lower than V_{SS} . This undesirable situation occurs if the input differential amplifier is made up of NMOS transistors. It is known that an NMOS and a PMOS differential pair placed in parallel would provide an input stage with a common-mode range that exceeds the power-supply voltage in both directions. This is known as rail-to-rail input operation. Figure 9.11 shows such an arrangement. To keep the diagram simple, we have not shown the parallel connection of the two differential pairs. The two positive input terminals are to be connected together and the two negative input terminals are to be tied together. Transistors Q_1 and Q_2 are the cascode transistors for the Q_3-Q_4 pair, and transistors Q_5 and Q_6 are the cascode devices for the Q_7-Q_8 pair. The output voltage V_o is shown taken differentially between the drains of the cascode devices. To obtain a single-ended output, a differential-to-single-ended conversion circuit should be connected in cascade.

Figure 9.11 indicates by arrows the direction of the current injections that result from the application of a positive differential input signal V_{D1} . Each of the current injections indicated is equal to $G_v(V_{D1}/2)$ where $G_v = g_{m1} = g_{m2} = g_{m5} = g_{m6}$. Thus the total current feeding each of the two output nodes will be $G_v V_{D1}$. Now, if the output resistance between each of the two nodes and ground is denoted R_o , the output voltage will be

$$V_o = 2G_v R_o V_{D1} \quad (9.65)$$

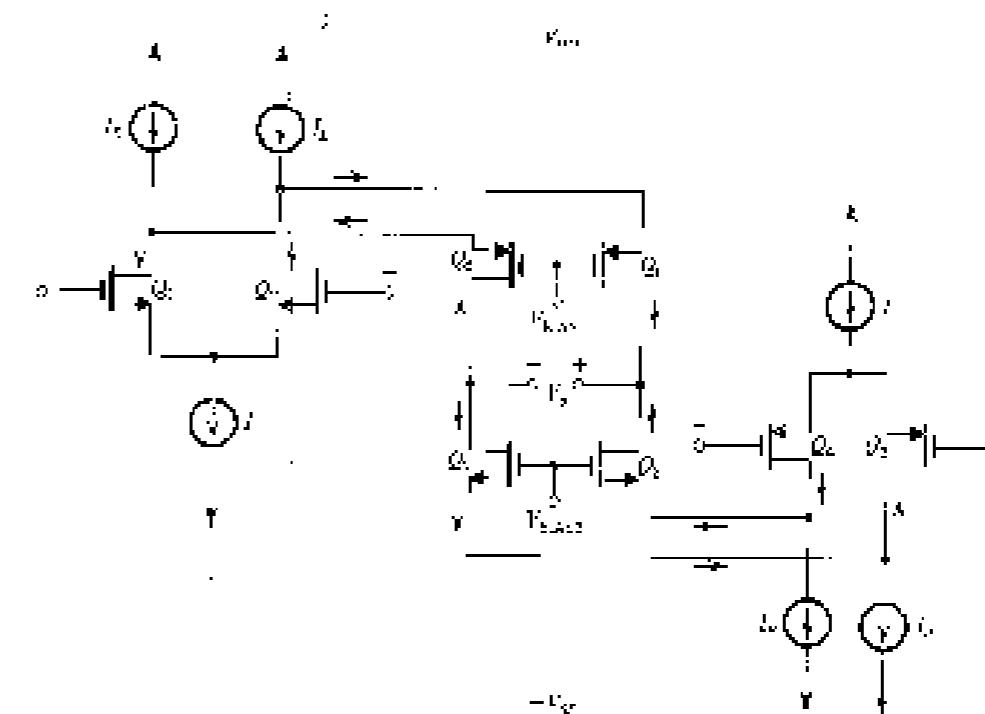


FIGURE 9.11 A folded-cascode op-amp that employs two parallel complementary input stages to achieve rail-to-rail input and output operation. Note that the two "A" terminals are connected together and the two "B" terminals are connected together.

Thus, the voltage gain will be

$$A_v = 2G_v R_o \quad (9.65)$$

This, however, assumes that both differential pairs will be operating simultaneously. This in turn occurs only over a limited range of V_{D1} . Over the remainder of the input common-mode range, only one of the two differential pairs will be operational, and the gain drops to half of the value in Eq. (9.65). This rail-to-rail folded-cascode structure is utilized in a commercially available op-amp.¹

EXERCISE

- (9.2.1) The circuit in Fig. 9.11 requires rail-to-rail operation, and operating conditions are $V_{DD} = 5 \text{ V}$, $V_{SS} = -2.9 \text{ V}$, $I_D = 500 \mu\text{A}$, and $f_v = 10 \text{ Hz}$ to 100 kHz. Find the input common-mode range, the output voltage range, and the output current range.
- (9.2.2) Find the range over which the rail-to-rail stage operates.
- (9.2.3) Find the input voltage range for high-speed CMOS overlap regions.
- (9.2.4) Find the input voltage range for low-speed CMOS overlap regions.
- (9.2.5) Calculate the output voltage range for the rail-to-rail stage.
- (9.2.6) Find the output current range for the rail-to-rail stage.
- (9.2.7) Find the output current range for the rail-to-rail stage.
- (9.2.8) Find the output current range for the rail-to-rail stage.
- (9.2.9) Find the output current range for the rail-to-rail stage.
- (9.2.10) Find the output current range for the rail-to-rail stage.
- (9.2.11) Find the output current range for the rail-to-rail stage.
- (9.2.12) Find the output current range for the rail-to-rail stage.
- (9.2.13) Find the output current range for the rail-to-rail stage.
- (9.2.14) Find the output current range for the rail-to-rail stage.
- (9.2.15) Find the output current range for the rail-to-rail stage.
- (9.2.16) Find the output current range for the rail-to-rail stage.
- (9.2.17) Find the output current range for the rail-to-rail stage.
- (9.2.18) Find the output current range for the rail-to-rail stage.
- (9.2.19) Find the output current range for the rail-to-rail stage.
- (9.2.20) Find the output current range for the rail-to-rail stage.
- (9.2.21) Find the output current range for the rail-to-rail stage.
- (9.2.22) Find the output current range for the rail-to-rail stage.
- (9.2.23) Find the output current range for the rail-to-rail stage.
- (9.2.24) Find the output current range for the rail-to-rail stage.
- (9.2.25) Find the output current range for the rail-to-rail stage.
- (9.2.26) Find the output current range for the rail-to-rail stage.
- (9.2.27) Find the output current range for the rail-to-rail stage.
- (9.2.28) Find the output current range for the rail-to-rail stage.
- (9.2.29) Find the output current range for the rail-to-rail stage.
- (9.2.30) Find the output current range for the rail-to-rail stage.
- (9.2.31) Find the output current range for the rail-to-rail stage.
- (9.2.32) Find the output current range for the rail-to-rail stage.
- (9.2.33) Find the output current range for the rail-to-rail stage.
- (9.2.34) Find the output current range for the rail-to-rail stage.
- (9.2.35) Find the output current range for the rail-to-rail stage.
- (9.2.36) Find the output current range for the rail-to-rail stage.
- (9.2.37) Find the output current range for the rail-to-rail stage.
- (9.2.38) Find the output current range for the rail-to-rail stage.
- (9.2.39) Find the output current range for the rail-to-rail stage.
- (9.2.40) Find the output current range for the rail-to-rail stage.
- (9.2.41) Find the output current range for the rail-to-rail stage.
- (9.2.42) Find the output current range for the rail-to-rail stage.
- (9.2.43) Find the output current range for the rail-to-rail stage.
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- (9.2.75) Find the output current range for the rail-to-rail stage.
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- (9.2.92) Find the output current range for the rail-to-rail stage.
- (9.2.93) Find the output current range for the rail-to-rail stage.
- (9.2.94) Find the output current range for the rail-to-rail stage.
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- (9.2.97) Find the output current range for the rail-to-rail stage.
- (9.2.98) Find the output current range for the rail-to-rail stage.
- (9.2.99) Find the output current range for the rail-to-rail stage.
- (9.2.100) Find the output current range for the rail-to-rail stage.

¹ The Texas Instruments CPA107.

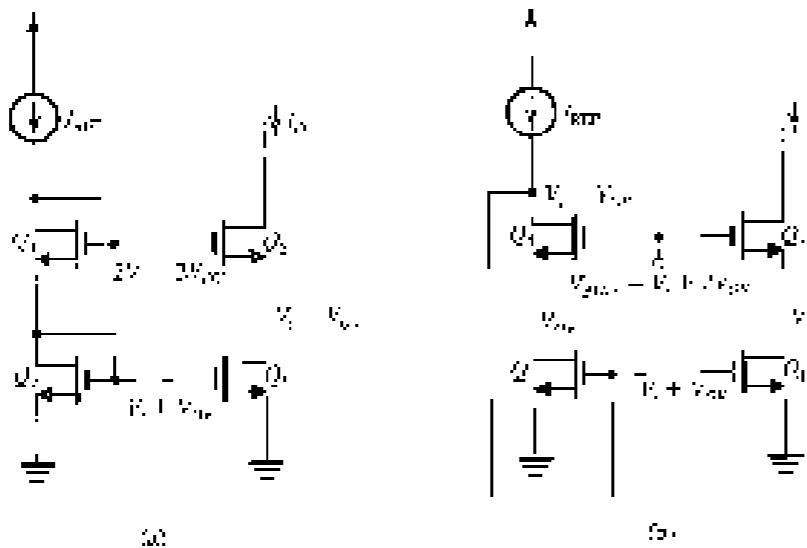


FIGURE 9.12 (a) Cascaded current mirror with its voltages and nodes labeled. Note that the minimum voltage allowed at the output is $V_{out} = V_2 - V_{DD}$. (b) A modification of the wide-swing mirror shown in (a) to increase the output voltage range to V_{DD} . This is the wide-swing current mirror.

9.2.7 Increasing the Output Voltage Range: The Wide-Swing Current Mirror

In Section 9.2.3, it was found that while the output voltage of the circuit of Fig. 9.9 can swing to within $2|V_{DD}|$ of V_{DD} , the cascode current mirror limits the negative swing to $[2|V_{DD}| - V_1]$ above $-V_{DD}$. In other words, the cascode mirror reduces the voltage swing by V_1 volts. This point is further illustrated in Fig. 9.12(a), which shows a cascode mirror (with $V_{DD} = 0$, for simplicity) and indicates the voltages that result at the various nodes. Observe that, since the voltage at the gate of Q_1 is $2V_{DD} + V_{DD}$, the minimum voltage permitted at the output (while Q_1 remains saturated) is $V_{out} = 2V_{DD}$, hence the extra V_1 . Also, observe that Q_1 is operating with a drain-to-source voltage $V_1 - V_{DD}$, which is V_1 volts greater than it needs to operate in saturation.

The observations above lead us to the conclusion that, to permit the output voltage of the drain of Q_1 to swing as low as $2V_{DD}$, we must lower the voltage at the gate of Q_1 from $V_1 = 2V_{DD} + V_{DD} = 3V_{DD}$ to $V_1 = 2V_{DD}$. This is exactly what is done in the modified mirror circuit in Fig. 9.12(b). The gate of Q_1 is now connected to a bias voltage $V_{DD} + V_1 - 2V_{DD}$. Thus the output voltage can go down to $2V_{DD}$, with Q_1 still in saturation. Also, the voltage at the drain of Q_1 is now V_1 , so that Q_1 is operating at the edge of saturation. The same is true of Q_2 , and thus the current tracking between Q_1 and Q_2 will be assured. Note, however, that we can no longer connect the gate of Q_1 to its drain. Rather, it is connected to the drain of Q_4 . This establishes a voltage of $V_1 - V_{DD}$ at the drain of Q_1 , which is sufficient to keep Q_1 in saturation (as long as V_1 is greater than V_{DD} , which is usually the case). This circuit is known as the wide-swing current mirror. Finally, note that Fig. 9.12(b) does not show the circuit for generating $V_{DD} + V_1$. There are a number of possible circuits to accomplish this task, one of which is explored in Exercise 9.8.

EXERCISE

- Show that if transistor Q_1 in the circuit of Fig. 9.12(b) is 100% saturated, the output voltage of the op-amp is given by $V_{out} = V_{DD} + V_{DD} \left(\frac{V_{DD} + V_{out}}{V_{DD} + V_{DD} - V_1} \right)^2$.

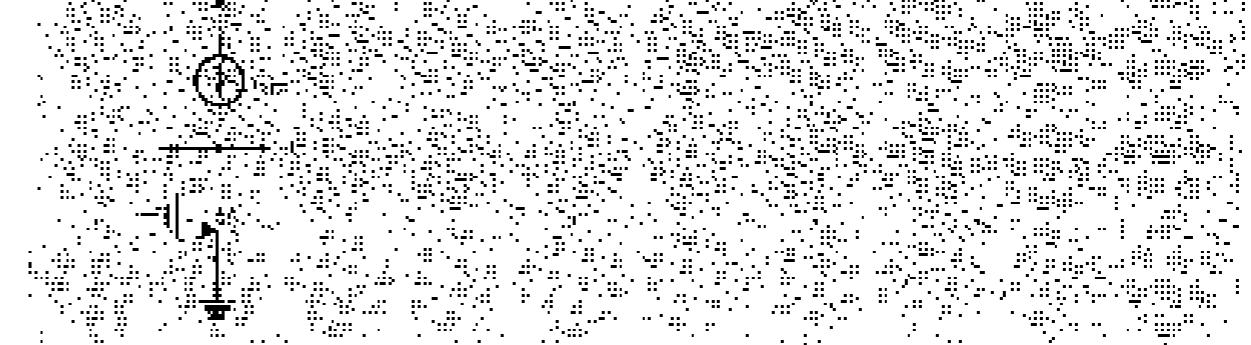


FIGURE 9.13 The 741 op-amp circuit.

9.3 THE 741 OP-AMP CIRCUIT

Our study of BJT op-amps is based on the 741 op-amp circuit, which is shown in Fig. 9.13. Note that, in keeping with the IC design philosophy, the circuit uses a large number of transistors, but relatively few resistors, and only one capacitor. This philosophy is dictated by the constraints of silicon area, ease of fabrication, quality of realizable components of the fabrication, of active and passive components in IC form (see Section 6.1 and Appendix A).

As is the case with most general-purpose IC op-amps, the 741 requires two power supplies, V_{DD} and $-V_{EE}$. Normally, $V_{DD} = V_{EE} = 15\text{ V}$, but the circuit also operates satisfactorily with the power supplies reduced to much lower values (such as $\pm 5\text{ V}$). It is important to observe that no circuit node is connected to ground, the common terminal of the two supplies.

With a relatively large circuit such as that shown in Fig. 9.13, the first step in the analysis is the identification of its recognizable parts and their functions. This can be done as follows:

9.3.1 Bias Circuit

The reference bias current of the 741 circuit (bias I_B) is generated at the bottom of the extreme left of Fig. 9.13, consisting of the two diode-connected transistors Q_{11} and Q_{12} and the resistance R_1 . Using a Wilson current source formed by Q_{11} , Q_{12} , and R_1 , bias current for the first stage is generated in the collector of Q_{11} . Another current mirror formed by Q_3 and Q_4 takes part in biasing the first stage.

The reference bias current I_{BB} is used to provide two proportional currents in the collector of Q_{11} . This double-collector, lateral² pnp transistor can be thought of as two

²See Appendix A for a description of lateral pnp transistors. Note that the transistors were discussed in Section 6.2.

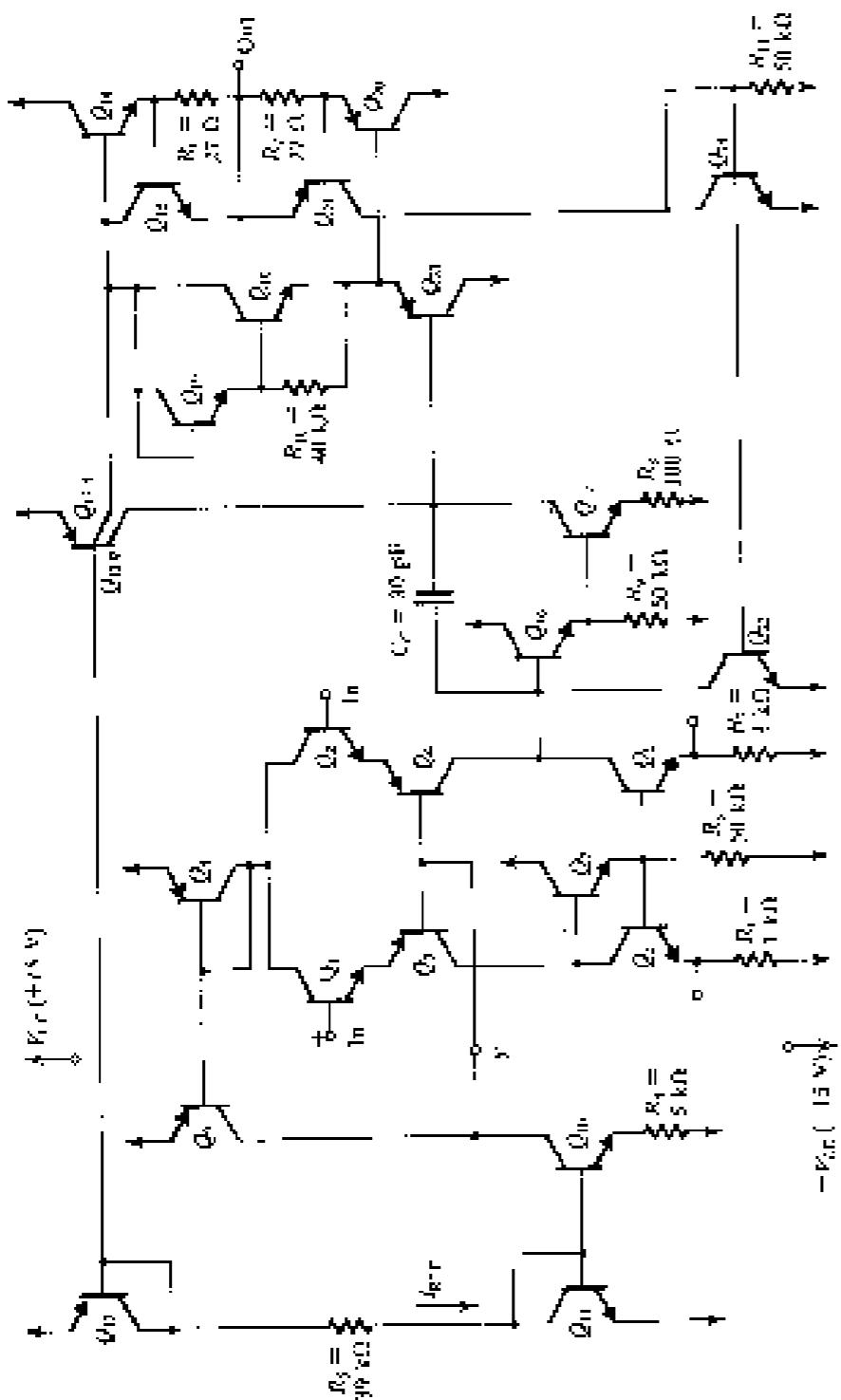


FIGURE 9.13 The 741 four-transistor op-amp circuit. The circuit has three stages: an input stage, an intermediate single-ended high-gain stage, and an output-buffering stage. The input stage consists of transistors Q_1 through Q_4 , with biasing performed by Q_{11} , Q_{12} , and Q_{13} . Transistors Q_5 and Q_6 form a differential input stage. Transistors Q_7 and Q_8 form an intermediate stage. Transistors Q_9 and Q_{10} form the output-buffering stage. Transistors Q_1 and Q_2 serve to protect the input transistors Q_1 and Q_2 .

transistors whose base-emitter junctions are connected in parallel. Thus Q_{11} and Q_{12} form a two-emitter current mirror. One output, the collector of Q_{13} , provides bias current for Q_{14} , and the other output, the collector of Q_{14} , provides bias current for the output stage of the op amp.

Two more transistors, Q_{15} and Q_{16} , take part in the dc bias process. The purpose of Q_{15} and Q_{16} is to establish two V_{BE} drops between the bases of the output transistors Q_9 and Q_{10} .

9.3.2 Short-Circuit Protection Circuitry

The 741 circuit includes a number of transistors that are normally off and conduct only in the event that one attempts to draw a large current from the op-amp output terminals. This happens, for example, if the output terminal is short-circuited to one of the two supplies. The short-circuit protection network consists of R_1 , R_2 , Q_{15} , Q_{16} , Q_{14} , R_3 , and Q_{13} . In the following we shall assume that these transistors are off. Operation of the short-circuit protection network will be explained in Section 9.5.3.

9.3.3 The Input Stage

The 741 circuit consists of three stages: an input differential stage, an intermediate single-ended high-gain stage, and an output-buffering stage. The input stage consists of transistors Q_1 through Q_4 , with biasing performed by Q_{11} , Q_{12} , and Q_{13} . Transistors Q_5 and Q_6 act as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common-base amplifier formed by Q_7 and Q_8 . Thus the input stage is the differential version of the common-collector common-base configuration discussed in Section 6.11.3.

Transistors Q_1 , Q_2 , and Q_3 and resistors R_1 , R_2 , and R_3 form the load circuit of the input stage. This is an elaborate current-mirror load circuit, which we will analyze in detail in Section 9.5.1. It will be shown that this load circuit not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection. The output of the input stage is taken single-endedly at the collector of Q_8 .

As mentioned in Section 7.7.2, every op-amp circuit includes a level shifter whose function is to shift the dc level of the signal at the op-amp output, can swing positive and negative. In the 741, level shifting is done in the first stage using the lateral-pnp transistors Q_5 and Q_6 . Although lateral-pnp transistors have poor high-frequency performance, their use in the common-base configuration (which is known to have good high-frequency response) does not seriously impair the op-amp frequency response.

The use of the lateral-pnp transistors Q_5 and Q_6 in the first stage results in an added advantage: protection of the input-stage transistors Q_1 and Q_2 against emitter-junction breakdown. Since the emitter-base junction of an n-pn transistor breaks down at about 7 V of reverse bias (see Section 5.2.5), regular op-amp differential stages suffer such a breakdown if, say, the supply voltage is accidentally connected between the input terminals. Lateral-pnp transistors, however, have high-emitter-base-breakdown voltages (about 50 V); and because they are connected in series with Q_1 and Q_2 , they provide protection of the 741 input transistors Q_1 and Q_2 .

9.3.4 The Second Stage

The second or intermediate stage is composed of Q_{15} , Q_{16} , Q_{13} , and the two resistors R_5 and R_6 . Transistor Q_{15} acts as an emitter follower, thus giving the second stage a high input

resistance. This minimizes the loading on the input stage and avoids loss of gain. Transistor Q_1 acts as a common-emitter amplifier with a Miller resistor in the emitter. Its load is composed of the high output resistance of the current source Q_{10} in parallel with the input resistance of the pump stage (seen looking into the base of Q_{11}). Using a transistor current source as a load resistance for the load) enables one to obtain high gain without resorting to the use of large load resistances, which would occupy a large chip area and require large power-supply voltages.

The output of the second stage is taken at the collector of Q_{10} . Capacitor C_2 is connected in the feedback path of the second stage to provide frequency compensation using the Miller compensation technique studied in Section 8.11. It will be shown in Section 9.5 that the relatively small capacitor C_2 gives the unity-gain dominant pole at about 1 Hz. Furthermore, noise splitting causes other poles to be shifted to much higher frequencies, giving the op-amp a unity-gain 20-dB decade gain roll-off with a unity-gain bandwidth of about 1 MHz. It should be pointed out that although C_2 is small in value, the chip area that it occupies is about 12 times that of a standard zener diode!

9.3.5 The Output Stage

The purpose of the output stage is to provide the amplifier with a low output resistance. In addition, the output stage should be able to supply relatively large load currents without dissipating an unduly large amount of power in the IC. The 741 uses an efficient output circuit known as a class AB output stage.

Output stages are studied in detail in Chapter 14, and the output stage of the 741 will be discussed in some detail in Section 9.7. For the time being we wish to point out the difference between the class AB output stage and the output stage we are familiar with, namely the emitter-follower follower. Figure 9.14(a) shows an emitter-follower bias with a constant-current source I_b . To keep the emitter-follower transistor conducting at all times, thus ensuring the low output resistance it provides, the bias current I_b must be greater than the largest magnitude of load current I_L . This is known as class A operation and the emitter-follower junction class A output stage. The drawback of class A operation is the large power dissipated in the transistor.

The power dissipated in the output stage can be reduced by arranging for the transistor to turn on only when an input signal is applied. For this to work, however, one needs two transistors, an npn to source output current and a pnp to sink output current. Such an arrangement is shown in Fig. 9.14(b). Observe that both transistors will be cut off when $v_i = 0$. In other words, the transistors are biased at zero dc current. When v_i goes positive, Q_2 conducts while Q_1 remains off. When v_i goes negative, the transistors reverse roles. This arrangement is known as class B operation and the circuit as a class B output stage.

Although efficient in terms of power dissipation, the class B circuit causes output signal distortion as illustrated in Fig. 9.14(c). This is a result of the fact that for $|v_i|$ less than about 0.5 V, neither of the transistors conducts and $v_o = 0$. This type of distortion is known as crossover distortion.

Crossover distortion can be reduced by biasing the output-stage transistors at a low current. This ensures that the output transistors Q_2 and Q_1 will remain conducting when v_i is small. As v_i increases, one of the two transistors conducts more, while the other conducts less, in a manner similar to that in the class B stage.

There are a number of ways for biasing the transistors of the class AB stage. Figure 9.14(d) shows one such approach utilizing two diode-connected transistors Q_3 and Q_4 with junction

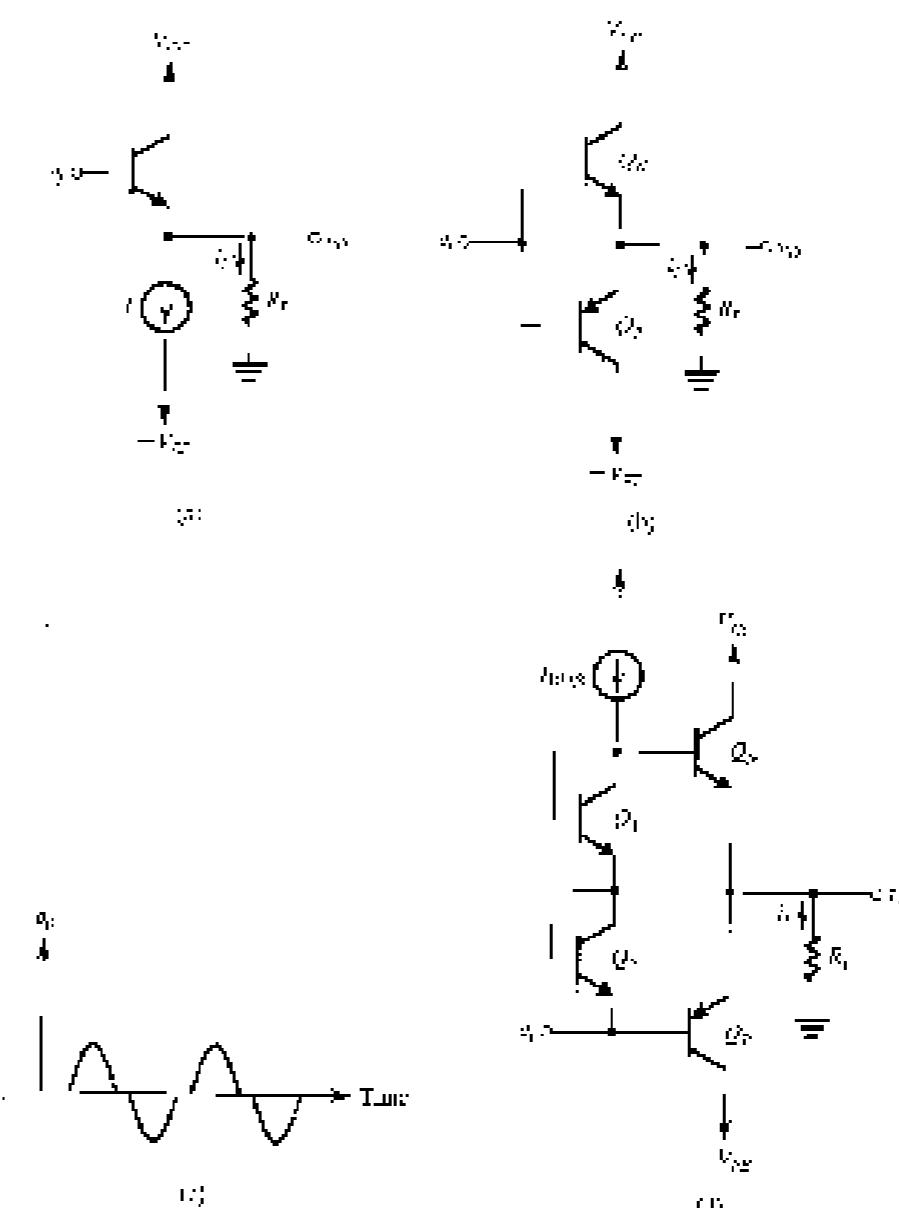


FIGURE 9.14 (a) The emitter-follower bias; (b) class B output stage; (c) Class B output stage; (d) The output stage (class AB stage fed with a 1-V input sinusoid. See v_{1D} in the previous section); (e) Class AB output stage.

currents much smaller than those of Q_1 and Q_2 . A somewhat more elaborate biasing network is utilized in the 741 output stage.

The output stage of the 741 consists of the complementary pair Q_{11} and Q_{12} , where Q_{11} is a *n*-channel pnp (see Appendix A). Transistors Q_{11} and Q_{12} are fed by current source Q_{10} and bias the output transistors Q_{13} and Q_{14} . Transistor Q_{11} (which is another substrate pnp) functions as an emitter follower, thus minimizing the leading effect of the output stage on the second stage.

9.3.6 Device Parameters

In the following sections we shall carry out a detailed analysis of the 741 circuit. For the standard npn and pnp transistors, the following parameters will be used:

$$\text{npn: } I_s = 10^{-14} \text{ A}, \beta = 200, V_T = 0.7 \text{ V}$$

$$\text{pnp: } I_s = 10^{-14} \text{ A}, \beta = 20, V_T = 50 \text{ mV}$$

In the 741 circuit the output devices are Q_{1A} , Q_{1B} and Q_{2B} . Transistor Q_3 will be assumed to be equivalent to two transistors, Q_{1A} and Q_{1B} , with parallel base-emitter junctions and having the following saturation currents:

$$I_{SD} = 0.25 \times 10^{-14} \text{ A} \quad I_{SB} = 0.75 \times 10^{-14} \text{ A}$$

Transistors Q_{1A} and Q_{2B} will be assumed to each have an area three times that of a standard device. Output transistors usually have relatively large areas, so to be able to supply large load currents and dissipate relatively large amounts of power with only a moderate increase in device temperature.

EXERCISES

- 9.9 The biasing and input operational amplifiers for the 741 are shown in Fig. 9.10. Calculate the parameters of the input stage, i.e. V_{BE1} , I_{SD1} , I_{SD2} , I_{SD3} , V_{BE3} , V_{BE4} , V_{BE5} , V_{BE6} , V_{BE7} , V_{BE8} , V_{BE9} , V_{BE10} , V_{BE11} , V_{BE12} , V_{BE13} , V_{BE14} , V_{BE15} , V_{BE16} , V_{BE17} , V_{BE18} , V_{BE19} , V_{BE20} , V_{BE21} , V_{BE22} , V_{BE23} , V_{BE24} , V_{BE25} , V_{BE26} , V_{BE27} , V_{BE28} , V_{BE29} , V_{BE30} , V_{BE31} , V_{BE32} , V_{BE33} , V_{BE34} , V_{BE35} , V_{BE36} , V_{BE37} , V_{BE38} , V_{BE39} , V_{BE40} , V_{BE41} , V_{BE42} , V_{BE43} , V_{BE44} , V_{BE45} , V_{BE46} , V_{BE47} , V_{BE48} , V_{BE49} , V_{BE50} , V_{BE51} , V_{BE52} , V_{BE53} , V_{BE54} , V_{BE55} , V_{BE56} , V_{BE57} , V_{BE58} , V_{BE59} , V_{BE60} , V_{BE61} , V_{BE62} , V_{BE63} , V_{BE64} , V_{BE65} , V_{BE66} , V_{BE67} , V_{BE68} , V_{BE69} , V_{BE70} , V_{BE71} , V_{BE72} , V_{BE73} , V_{BE74} , V_{BE75} , V_{BE76} , V_{BE77} , V_{BE78} , V_{BE79} , V_{BE80} , V_{BE81} , V_{BE82} , V_{BE83} , V_{BE84} , V_{BE85} , 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V_{BE253} , V_{BE254} , V_{BE255} , V_{BE256} , V_{BE257} , V_{BE258} , V_{BE259} , V_{BE260} , V_{BE261} , V_{BE262} , V_{BE263} , V_{BE264} , V_{BE265} , V_{BE266} , V_{BE267} , V_{BE268} , V_{BE269} , V_{BE270} , V_{BE271} , V_{BE272} , V_{BE273} , V_{BE274} , V_{BE275} , V_{BE276} , V_{BE277} , V_{BE278} , V_{BE279} , V_{BE280} , V_{BE281} , V_{BE282} , V_{BE283} , V_{BE284} , V_{BE285} , V_{BE286} , V_{BE287} , V_{BE288} , V_{BE289} , V_{BE290} , V_{BE291} , V_{BE292} , V_{BE293} , V_{BE294} , V_{BE295} , V_{BE296} , V_{BE297} , V_{BE298} , V_{BE299} , V_{BE300} , V_{BE301} , V_{BE302} , V_{BE303} , V_{BE304} , V_{BE305} , V_{BE306} , V_{BE307} , V_{BE308} , V_{BE309} , V_{BE310} , V_{BE311} , V_{BE312} , V_{BE313} , V_{BE314} , V_{BE315} , V_{BE316} , V_{BE317} , V_{BE318} , V_{BE319} , V_{BE320} , V_{BE321} , V_{BE322} , V_{BE323} , V_{BE324} , V_{BE325} , V_{BE326} , V_{BE327} , V_{BE328} , V_{BE329} , V_{BE330} , V_{BE331} , V_{BE332} , V_{BE333} , V_{BE334} , V_{BE335} , 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EXERCISE

Given the values of the transistors in Fig. 9.16, determine the value of β_{pnp} required to obtain a value of $I_{\text{in}} = 9.5 \mu\text{A}$.

Having determined I_{in} , we proceed to determine the dc current in each of the input-stage transistors. Part of the input stage is shown in Fig. 9.16. From symmetry, we see that

$$I_{\text{Q1}} = I_{\text{Q2}}$$

Denote this current by I . We see that if the sign of β is right, then

$$I_{\text{Q3}} = I_{\text{Q4}} = I$$

and the base currents of Q_1 and Q_2 are equal, with a value of $I/(\beta_p + 1) = I/\beta_{\text{pnp}}$, where β_p denotes β of the pnp devices.

The current injected from Q_1 and Q_2 is fed by an input current of $2I$. Using the result in Eq. (6.21), we can express the output current of the inverter as

$$I_{\text{Q5}} = \frac{2I}{1 + 2/\beta_p}$$

We can now write a node equation for node X in Fig. 9.16 and thus determine the value of I . If $\beta_p > 1$, then this node equation gives

$$2I = I_{\text{Q5}}$$

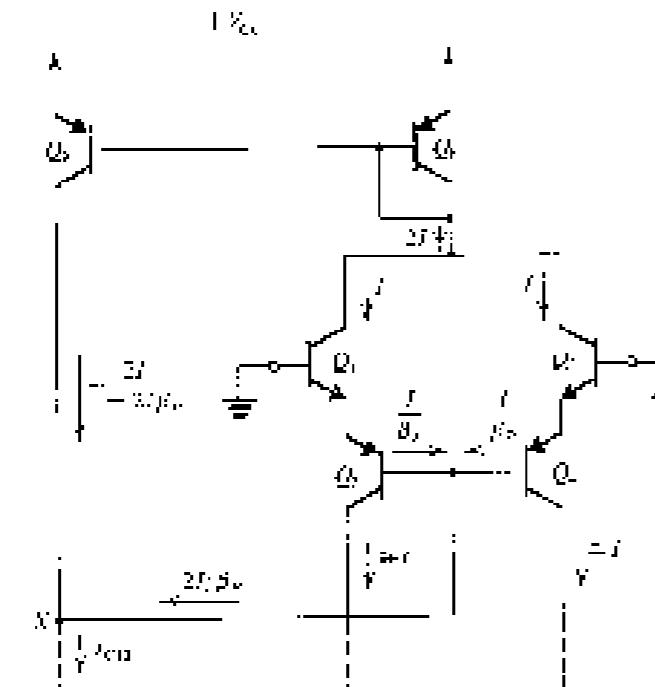


FIGURE 9.16 The dc analysis of the 741 input stage.

For $\beta_p = 75$, $I_{\text{Q5}} = 13 \mu\text{A}$; thus $I = 9.5 \mu\text{A}$. We have thus determined that

$$I_{\text{Q1}} = I_{\text{Q2}} = I_{\text{Q3}} = I_{\text{Q4}} = 9.5 \mu\text{A}$$

At this point, we should note that transistors Q_1 through Q_4 form a negative-feedback loop, which works to stabilize the value of I at approximately $I_{\text{Q5}}/2$. To appreciate this fact, assume that for some reason the current I in Q_1 and Q_2 increases. This will cause the current pulled from Q_3 to increase, and the output current of the Q_3 - Q_5 mirror will correspondingly increase. However, since I_{Q5} remains constant, node X forces the drain-to-emitter currents of Q_3 and Q_4 to decrease. This in turn will cause the emitter currents of Q_1 and Q_2 to decrease, and hence the collector currents of Q_1 and Q_2 to decrease. This is opposite in direction to the change originally assumed. Hence the feedback is negative, and it stabilizes the value of I .

Figure 9.17 shows the remainder of the 741 input stage. If we neglect the base current of Q_{10} , then

$$I_{\text{Q6}} = I$$

Similarly, neglecting the base current of Q_9 , we obtain

$$I_{\text{Q7}} = I$$

The bias current of Q_8 can be determined from

$$I_{\text{Q8}} = I_{\text{Q7}} = \frac{2I}{\beta_p} + \frac{V_{\text{BE7}} + I R_2}{R_2} \quad (9.67)$$

where β_p denotes β of the n-p-n transistor. To determine V_{BE7} , we use the translated z-parameter relationship and write

$$V_{\text{BE7}} = V_T \ln \frac{I}{I_s}$$

Substituting $I_s = 10^{-14} \text{ A}$ and $I = 9.5 \mu\text{A}$ results in $V_{\text{BE7}} = 517 \text{ mV}$. Then substituting in Eq. (9.67) yields $I_{\text{Q8}} = 10.5 \mu\text{A}$. Note that the base current of Q_8 is indeed negligible in comparison to the value of I , as has been assumed.

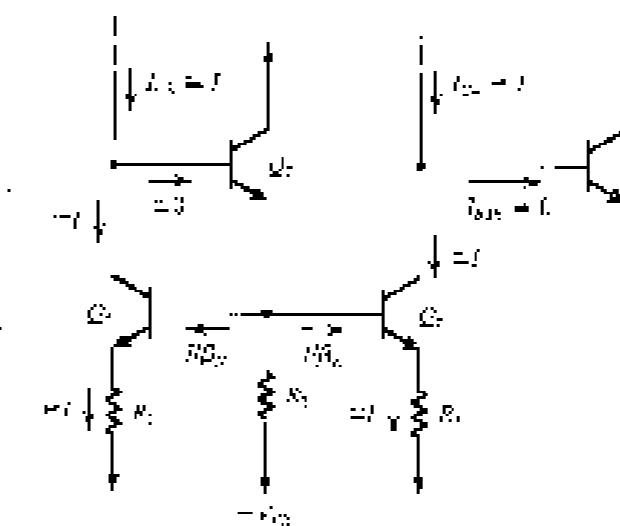


FIGURE 9.17 The dc analysis of the 741 input stage, continued.

9.4.3 Input Bias and Offset Currents

The input bias current of an op amp is defined (Chapters 2 and 7) as

$$I_b = \frac{I_{Q1} + I_{Q2}}{\beta}$$

For the 741 we obtain

$$I_b = \frac{I}{\beta_n}$$

Using $\beta_n = 200$, yields $I_b = 4.5 \mu A$. Note that this value is reasonably small and is typical for general-purpose opamps that use BJT's in the input stage. Much lower input bias currents (in the picampere or femtoamp range) can be obtained using a FET input stage. Also, there exist techniques for reducing the input bias current of bipolar-input opamps.

Because of possible mismatches in the β values of Q_1 and Q_2 , the input base currents will not be equal. Given the value of the β 's in each, one can use Eq. (7.17) to calculate the input offset current, defined as

$$I_{os} = |\beta_{Q1} - \beta_{Q2}|$$

9.4.4 Input Offset Voltage

From Chapter 7 we know that the input offset voltage is determined primarily by mismatch between the two sides of the input stage; in the 741 op amp, the input offset voltage is due to mismatch between Q_1 and Q_2 , between Q_1 and Q_3 , between Q_2 and Q_4 , and between R_1 and R_2 . Evaluation of the components of V_{os} corresponding to the various mismatches follows the method outlined in Section 7.4. Basically, we find the correct test results at the output of the first stage due to the particular mismatch being considered. Then we find the differential input voltage that must be applied to reduce the output excess to zero.

9.4.5 Input Common-Mode Range

The input common-mode range is the range of input common-mode voltages over which the input stage remains in the linear active mode. Refer to Fig. 9.13. We see that in the 741 circuit the input common-mode range is determined at the upper end by saturation of Q_1 and Q_2 , and at the lower end by saturation of Q_3 and Q_4 .

Tip

It is often necessary to determine the input common-mode range of an op amp. This can be done by applying a differential input voltage to the inputs and then increasing the common-mode voltage until one of the transistors begins to saturate. If the common-mode voltage is increased further, the output voltage will change polarity. At this point, the common-mode voltage is at its maximum value. It is also possible to determine the common-mode range by applying a common-mode voltage to the inputs and then decreasing the common-mode voltage until one of the transistors begins to saturate. At this point, the common-mode voltage is at its minimum value.

9.4.6 Second-Stage Bias

If we neglect the base current of Q_{13} then we see from Fig. 9.10 that the collector current of Q_{13} is approximately equal to the current supplied by current source Q_{10} . Because Q_{10} has a scale factor of 0.75 times that of Q_{12} , its collector current will be $I_{Q13} = 0.75 I_{Q12}$, where we have assumed that $\beta_1 = 1$. Thus $I_{Q13} = 250 \mu A$ and $I_{C13} = 550 \mu A$. At this current level the

base-emitter voltage of Q_{13} is

$$V_{BE13} = V_T \ln \frac{I_{C13}}{I_s} = 618 \text{ mV}$$

The collector current of Q_{13} can be determined from

$$I_{C13} = I_{Q13} - I_{Z13} = \frac{I_T N_3 - V_{BE13}}{R_f}$$

This calculation yields $I_{C13} = 15.2 \mu A$. Note that the base current of Q_{13} will indeed be negligible compared to the emitter-base bias I_s as we have assumed.

9.4.7 Output-Stage Bias

Figure 9.14 shows the output stage of the 741 with the short-circuit protection circuitry omitted. Current source Q_{12B} delivers a current of $0.25 I_{Q12}$. Because I_c of Q_{12B} is 0.25 times the I_c of Q_{12} , the network composed of Q_{12} , Q_{12B} , and R_{12} . If we neglect the base currents of Q_{12} and Q_{12B} , then the emitter current of Q_3 will also be equal to $0.25 I_{Q12}$. Thus

$$I_{Q12} = I_{Q12B} = 0.25 I_{Q12} = 150 \mu A$$

Thus we see that the base current of Q_3 is only $150/30 = 5.0 \mu A$, which is negligible compared to I_{Q12} as we have assumed.

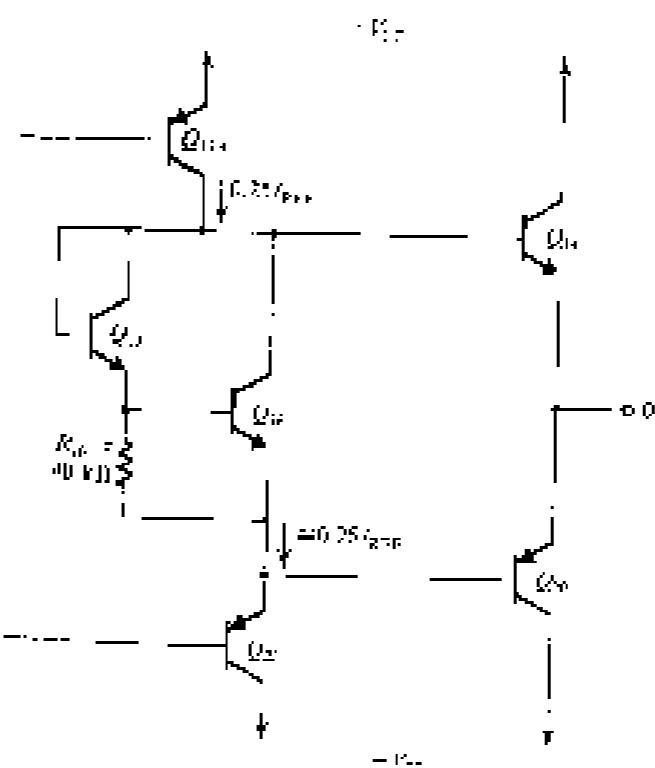


FIGURE 9.14 The 741 output stage without short-circuit protection devices.

If we assume that V_{BEQ} is approximately 0.6 V, we can determine the current in R_{10} as 15 μ A. The emitter current of Q_{10} is therefore

$$I_{E10} = 180 \cdot 15 = 165 \mu\text{A}$$

Also,

$$I_{C10} = I_{E10} - 165 \mu\text{A}$$

At this value of current we find that $V_{CEQ} = 568 \text{ mV}$, which is quite close to the value assumed. The base current of Q_4 is $165/200 = 0.8 \mu\text{A}$, which can be added to the current in R_4 to determine the Q_3 current as

$$I_{C3} = I_{B4} = 15.8 \mu\text{A}$$

The voltage drop across the base-emitter junction of Q_3 can now be determined as

$$V_{BE3} = V_T \ln \frac{I_{C3}}{I_s} = 530 \text{ mV}$$

As mentioned in Section 9.3.5, the purpose of the Q_{10} - Q_9 network is to establish bias V_{BE} as the voltage drop between the bases of the output transistors Q_2 and Q_1 . This voltage drop, V_{BE} , can be now calculated as

$$V_{BE} = V_{BE3} + V_{BEQ} = 530 + 530 = 1.06 \text{ V}$$

Since V_{BE} appears across the series combination of the base-emitter junctions of Q_1 and Q_2 we can write

$$V_{BE} = V_T \ln \frac{I_{C1}}{I_{B1}} + V_T \ln \frac{I_{C2}}{I_{B2}}$$

Using the calculated value of V_{BE} and substituting $I_{B1} = I_{B2} = 3 \times 10^{-14} \text{ A}$, we determine the collector currents as

$$I_{C1} = I_{C2} = 154 \mu\text{A}$$

This is the small current in which the class AB output stage is biased.

9.4.6 Summary

For future reference, Table 9.1 provides a listing of the values of the collector bias currents of the 741 transistors.

TABLE 9.1 DC Collector Currents of the 741 Transistors

Q	β	Q_1	Q_{10}	Q_2	Q_{11}	Q_3	Q_{12}	Q_4	Q_{13}	Q_5	Q_{14}	Q_6	Q_{15}	Q_7	Q_{16}	Q_8	Q_{17}	Q_9	Q_{18}	
Q_1	0.5	Q_2	19	Q_{10}	350	Q_3	15.8	Q_{11}	134	Q_4	0	Q_5	0	Q_6	0	Q_7	0	Q_8	0	Q_9
Q_2	0.5	Q_3	19	Q_{11}	134	Q_4	0	Q_{12}	0	Q_5	0	Q_6	0	Q_7	0	Q_8	0	Q_9	0	Q_{10}
Q_3	0.5	Q_4	19	Q_{12}	0	Q_5	0	Q_{13}	0	Q_6	0	Q_7	0	Q_8	0	Q_9	0	Q_{10}	0	Q_{11}
Q_4	0.5	Q_5	730	Q_1	16.2	Q_6	0	Q_{14}	180	Q_7	0	Q_8	0	Q_9	0	Q_{10}	0	Q_{11}	0	Q_{12}
Q_5	0.5	Q_6	730	Q_{11}	350	Q_7	0	Q_{15}	134	Q_8	0	Q_9	0	Q_{10}	0	Q_{11}	0	Q_{12}	0	Q_{13}
Q_6	0.5	Q_7	730	Q_2	16.2	Q_8	0	Q_{16}	0	Q_9	0	Q_{10}	0	Q_{11}	0	Q_{12}	0	Q_{13}	0	Q_{14}
Q_7	0.5	Q_8	730	Q_{12}	0	Q_9	0	Q_{17}	0	Q_{10}	0	Q_{11}	0	Q_{12}	0	Q_{13}	0	Q_{14}	0	Q_{15}
Q_8	0.5	Q_9	730	Q_3	15.8	Q_{10}	0	Q_{18}	0	Q_{11}	0	Q_{12}	0	Q_{13}	0	Q_{14}	0	Q_{15}	0	Q_{16}

EXERCISE

- 9.13 From the circuit in Fig. 9.18, the Q_1 - Q_2 network is replaced by a single common-emitter transistor, with $\beta = 100$. Calculate the current in Q_3 and Q_4 . Hint: Use the result of Exercise 9.10.

9.5 SMALL-SIGNAL ANALYSIS OF THE 741

9.5.1 The Input Stage

Figure 9.19 shows part of the 741 input stage for the purpose of performing small-signal analysis. Note that since the collectors of Q_1 and Q_2 are connected to a constant dc voltage, they are shown grounded. Also, the constant-current biasing of the bases of Q_1 and Q_2 is equivalent to having the common-base terminal open-circuited.

The differential signal v_x applied between the input terminals effectively appears across two equal emitter resistances connected in series—those of Q_1 , Q_2 , Q_3 , and Q_4 . As a result, emitter signal currents flow as indicated in Fig. 9.19 with

$$i_x = \frac{v_x}{4r_e} \quad (9.6a)$$

where r_e denotes the emitter resistance of each of Q_1 through Q_4 . Thus

$$r_e = \frac{V_T}{I_s} = \frac{25 \text{ mV}}{9.5 \mu\text{A}} = 2.63 \text{ k}\Omega$$

Thus the four transistors Q_1 through Q_4 supply the load circuit with a pair of complementary current signals i_x , as indicated in Fig. 9.19.

The input differential resistance of the op amp can be obtained from Fig. 9.19 as

$$R_{in} = 4(\beta_y + 1)r_e \quad (9.6b)$$

For $\beta_y = 200$, we obtain $R_{in} = 2.1 \text{ M}\Omega$.

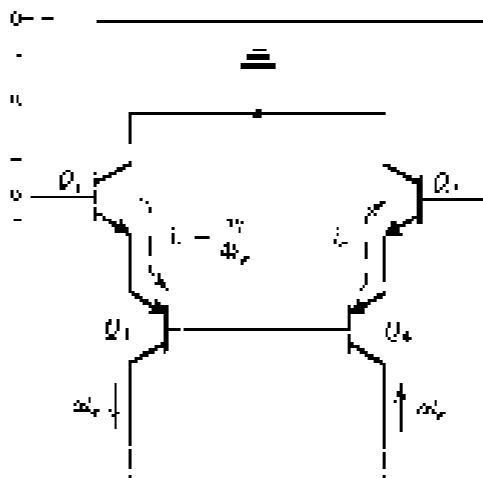


FIGURE 9.19 Small-signal analysis of the 741 input stage.

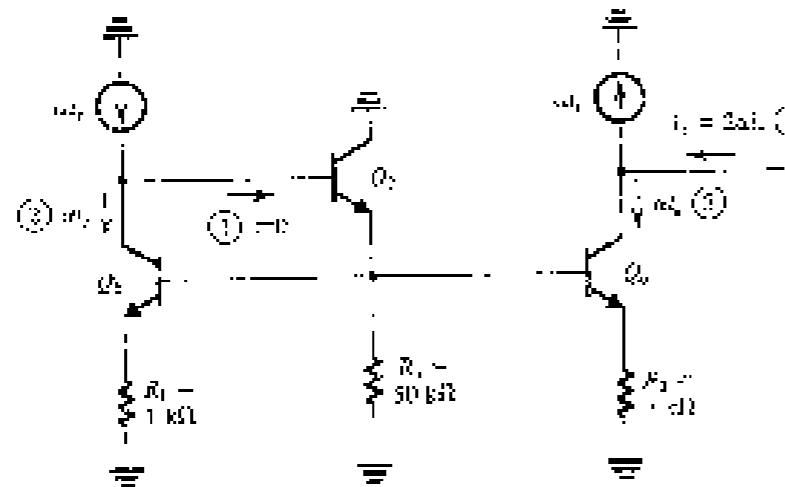


FIGURE 9.20 The load seen by the input stage fed by the two complementary current signals generated by \$Q_1\$ through \$Q_4\$ in Fig. 9.19. Circular numbers indicate the order of the analysis steps.

Proceeding with the input-stage analysis, we show in Fig. 9.20 the load circuit, fed with the complementary pair of current signals found earlier. Neglecting the signal current in the base of \$Q_1\$, we see that the collector signal current of \$Q_2\$ is approximately equal to the input current of \$Q_1\$. Now, since \$Q_1\$ and \$Q_2\$ are identical and their bases are tied together, and since equal resistances are connected to their emitters, it follows that their collector signal currents must be equal. Thus the signal current in the collector of \$Q_2\$ is forced to be equal to \$i_1^s\$. In other words, the load circuit functions as a current mirror.

Now consider the output node of the input stage. The output current \$i_o\$ is given by

$$i_o = 20i_1^s \quad (9.70)$$

The factor of 2 in this equation indicates that conversion from differential to single ended is performed without losing half the signal. The trick, of course, is the use of one current mirror to invert one of the current signals and then add the result to the other current signal (see Section 7.5).

Equations (9.68) and (9.70) can be combined to obtain the transconductance of the input stage, \$G_{in}\$:

$$G_{in} = \frac{i_o}{v_{in}} = \frac{\alpha}{2r_s} \quad (9.71)$$

Substituting \$r_s = 2.63\text{k}\Omega\$ and \$\alpha \approx 1\$ yields \$G_{in} = 15.36\text{nA/V}\$.

EXERCISE

9.5.1. Calculate the transconductance of the input stage of the 741 op amp. Assume \$V_A = 100\text{V}\$, \$I = 0.5\mu\text{A}\$, \$r_s = 2.63\text{M}\Omega\$, and \$\beta = 100\$. The answer is \$G_{in} = 15.36\text{nA/V}\$.

9.5.2. Calculate the output resistance of the input stage of the 741 op amp. Assume \$V_A = 100\text{V}\$, \$I = 0.5\mu\text{A}\$, \$r_s = 2.63\text{M}\Omega\$, and \$\beta = 100\$. The answer is \$R_{out} = 10.5\text{M}\Omega\$.

9.5.3. Calculate the input resistance of the 741 op amp. Assume \$V_A = 100\text{V}\$, \$I = 0.5\mu\text{A}\$, \$r_s = 2.63\text{M}\Omega\$, and \$\beta = 100\$. The answer is \$R_{in} = 6.7\text{M}\Omega\$.

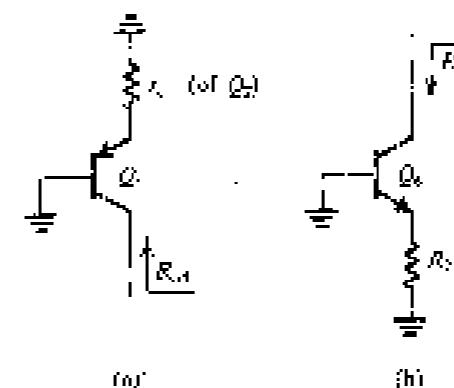


FIGURE 9.21 Simplified circuits for finding the two components of the output resistance \$R_o\$ of the input stage.

To complete our modeling of the 741 input stage we must find its output resistance \$R_o\$. This is the resistance seen "looking back" into the collector terminal of \$Q_1\$ in Fig. 9.20. Thus \$R_{o1}\$ is the parallel equivalent of the output resistance of the current source supplying the signal current \$i_1^s\$ and the output resistance of \$Q_1\$. The first component is the resistance looking into the collector of \$Q_1\$ in Fig. 9.20. Finding this resistance is considerably simplified if we assume that the common bases of \$Q_1\$ and \$Q_2\$ are at a virtual ground. This of course happens only when the input signal \$v_{in}\$ is applied in a complementary fashion. Nevertheless, this assumption does not result in a large error.

Assuming that the base of \$Q_1\$ is at virtual ground, the resistance we are after is \$R_{o1}\$, indicated in Fig. 9.21(a). This is the output resistance of a common-base transistor that has a resistance \$r_o\$ of \$Q_1\$ in its emitter. To find \$R_{o1}\$ we may use the following expression (Eq. 6.118):

$$R_{o1} = r_o(1 + \beta_r(\beta_r r_o)) \quad (9.72)$$

Substituting \$r_o = r_s = 2.63\text{M}\Omega\$ and \$\beta_r = V_A/I = 200\$ (thus \$\beta_r = 2.63\text{M}\Omega\$), and neglecting \$r_o\$ since it is \$(\beta : 1)\$ times larger than \$R_{o1}\$, results in \$R_{o1} = 10.5\text{M}\Omega\$.

The second component of the output resistance is that seen looking into the collector of \$Q_2\$ in Fig. 9.20. Although the base of \$Q_2\$ is not at virtual ground, we shall assume that the signal voltage at the base is small enough to make this approximation valid. The circuit then takes the form shown in Fig. 9.21(b), and \$R_{o2}\$ can be determined using Eq. (9.72) with \$R_F = R_2\$. Thus \$R_{o2} = 10.5\text{M}\Omega\$.

Finally, we substitute \$R_{o1}\$ and \$R_{o2}\$ in parallel to obtain the output resistance of the input stage, \$R_{out}\$, as \$R_{out} = 6.7\text{M}\Omega\$.

Figure 9.22 shows the equivalent circuit that we have derived for the input stage.

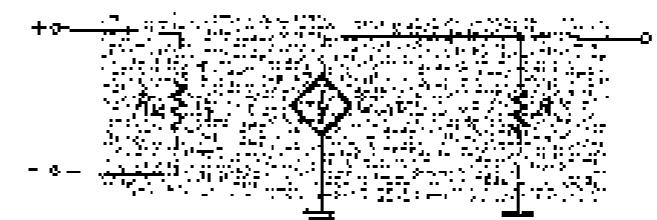


FIGURE 9.22 Small-signal equivalent circuit for the input stage of the 741 op amp.



We wish to find the input offset voltage resulting from a 2% mismatch between the resistances R_1 and R_2 in Fig. 9.15.

Solution

Consider first the situation when both input terminals are grounded, and assume that $R_1 = R + \Delta R$, $R_2 = R - \Delta R$, where $\Delta R/R = 0.02$. From Fig. 9.20 we see that, while Q_1 will conduct a current equal to I , the current in Q_2 will be smaller by ΔI . The value of ΔI can be found from

$$V_{BE2} + IR = V_{BE1} + I(R + \Delta R) \quad (9.73)$$

Thus

$$V_{BE2} - V_{BE1} = I\Delta R - \Delta I(R + \Delta R) \quad (9.74)$$

The quantity on the left-hand side is in effect the change in V_{BE} due to a change in I_B of ΔI . We may therefore write

$$V_{BE2} - V_{BE1} = \Delta I, \quad (9.75)$$

Equations (9.73) and (9.74) can be combined to obtain

$$\frac{\Delta I}{I} = \frac{\Delta R}{R + 2\Delta R + r_s} \quad (9.76)$$

Substituting $\Delta R = 1\text{ k}\Omega$ and $r_s = 2.53\text{ k}\Omega$ shows that a 2% mismatch between R_1 and R_2 gives rise to an output current $\Delta I = 5.5 \times 10^{-7}\text{ A}$. To reduce the output current to zero we have to apply an input voltage V_{IN} given by

$$V_{IN} = \frac{\Delta I}{G_{IN}} = \frac{5.5 \times 10^{-7}}{G_{IN}} \quad (9.77)$$

Substituting $I = 9.5\text{ mA}$ and $G_{IN} = 1/3.26\text{ mA/V}$ results in the offset voltage $V_{IN} = 3.2\text{ mV}$.

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

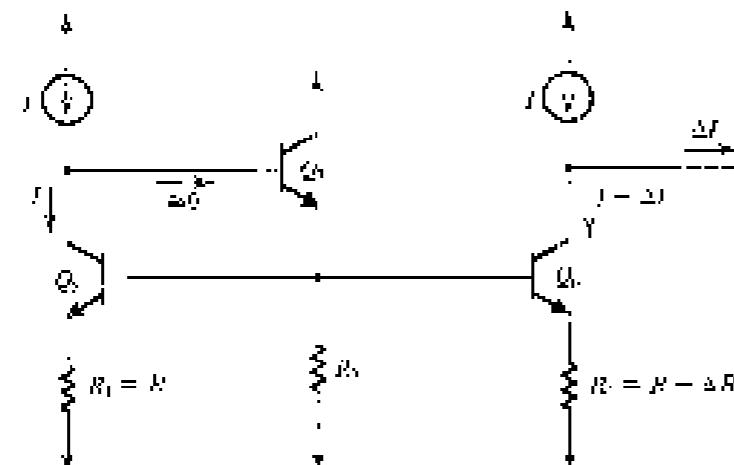


FIGURE 9.23 Input stage with both inputs grounded and a mismatch between R_1 and R_2 .

EXERCISES

The purpose of this series of exercises is to determine the small-signal voltage gain. This analysis is carried out in the half-circuit of the input stage of the 741 op-amp. Figure 9.24 shows the circuit with relevant component values and initial conditions. The input voltage is $V_{IN} = 1\text{ mV}$ and the output voltage is $V_{OUT} = 0\text{ mV}$. The input resistance is $R_{IN} = 10\text{ M}\Omega$. The output resistance is $R_{OUT} = 10\text{ M}\Omega$. The current I is 9.5 mA and the voltage V_{BB} is 1.5 V . The transistors have a current gain of $\beta = 100$ and a saturation voltage of $V_{CE(sat)} = 0.2\text{ V}$. The transistors have a threshold voltage of $V_{TH} = 0.7\text{ V}$. The transistors have a transconductance of $g_m = 1/3.26\text{ mA/V}$.

9.11 Small-signal analysis

9.12 Using the equivalent circuit of Fig. 9.25 and the values listed in Fig. 9.24, show that the output voltage V_{OUT} is given approximately by

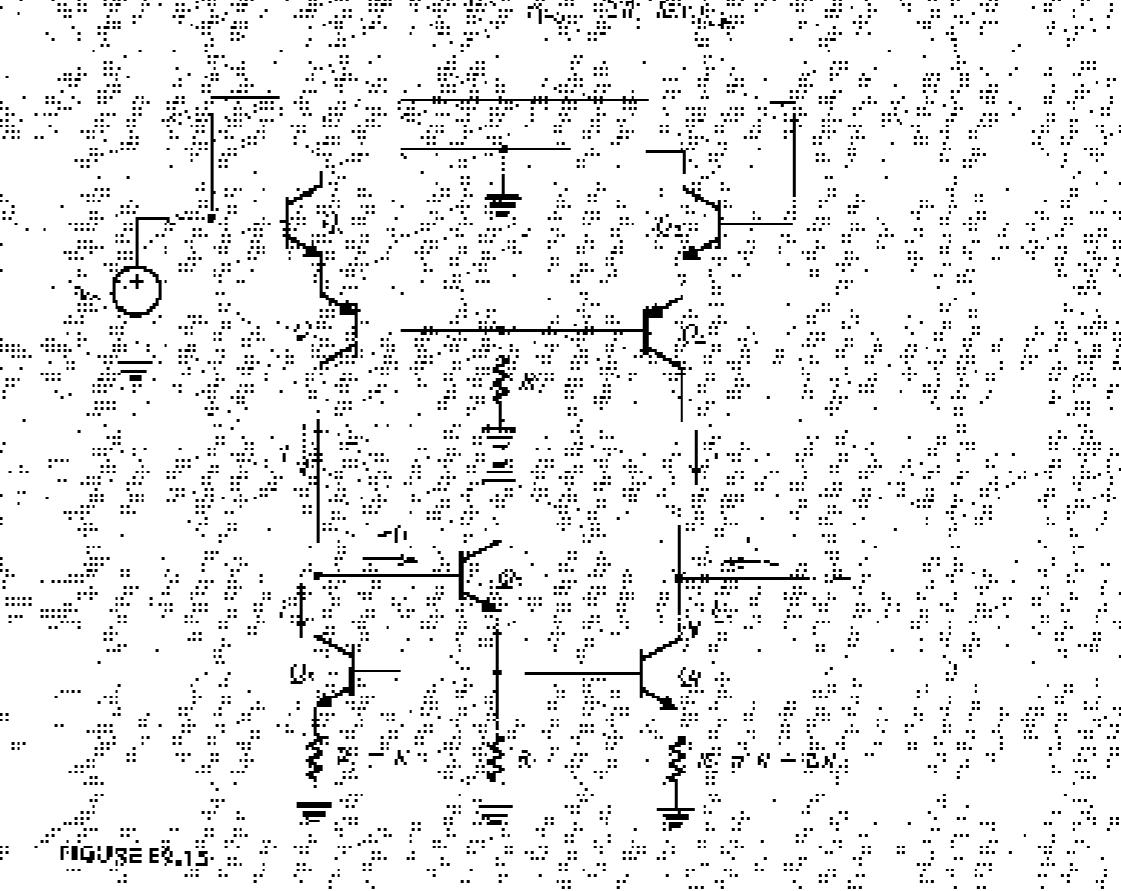


FIGURE 9.24

9.18 Refer to Fig. 9.21. Assuming that the bias voltage V_{B1} is zero, determine the small-signal output voltage V_{O1} if the input voltage is $V_{I1} = 10 \mu V$. Assume $\beta_{Q1} = 1000$, $R_1 = 10 k\Omega$, $R_2 = 10 k\Omega$, $R_{O1} = 1 M\Omega$, $R_{L1} = 1 M\Omega$.

9.19 The bias voltages V_{B1} and V_{B2} are both set to 0.7 V. Calculate the output voltage V_{O1} if the input voltage is $V_{I1} = 10 \mu V$. Assume $\beta_{Q1} = 1000$, $R_1 = 10 k\Omega$, $R_2 = 10 k\Omega$, $R_{O1} = 1 M\Omega$, $R_{L1} = 1 M\Omega$.

9.20 Let the value of C_{in} be equal to $10 pF$. Calculate the output voltage V_{O1} in Problem 9.18 if $V_{B1} = 0.7 V$ and $V_{B2} = 0$. Assume $\beta_{Q1} = 1000$, $R_1 = 10 k\Omega$, $R_2 = 10 k\Omega$, $R_{O1} = 1 M\Omega$, $R_{L1} = 1 M\Omega$.

9.21 The value of C_{in} is equal to $10 pF$. Calculate the output voltage V_{O1} in Problem 9.18 if $V_{B1} = 0.7 V$ and $V_{B2} = 0.7 V$. Assume $\beta_{Q1} = 1000$, $R_1 = 10 k\Omega$, $R_2 = 10 k\Omega$, $R_{O1} = 1 M\Omega$, $R_{L1} = 1 M\Omega$.

9.22 Recall that the common-mode rejection ratio (CMRR) of the second stage is given by $CMRR = \frac{A_{v1}}{A_{v1} + A_{v2}}$. If the second stage has a gain of $A_{v2} = 100$, calculate the CMRR if the transistors Q_{11} and Q_{12} have a transconductance of $0.5 mA/V$.

9.23 Find the CMRR of the second stage if the second stage has a gain of $A_{v2} = 100$ and the transistors Q_{11} and Q_{12} have a transconductance of $0.5 mA/V$.

9.5.2 The Second Stage

Figure 9.21 shows the 741 second stage prepared for small-signal analysis. In this section we shall analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 9.25.

Input Resistance The input resistance R_{in2} can be found by inspection to be

$$R_{in2} = (\beta_{Q1} + 1)r_{e1} + R_2/\beta_{Q1} = 10(r_{e1} + R_2) \quad (9.71)$$

Substituting the appropriate parameter values yields $R_{in2} = 4 M\Omega$.

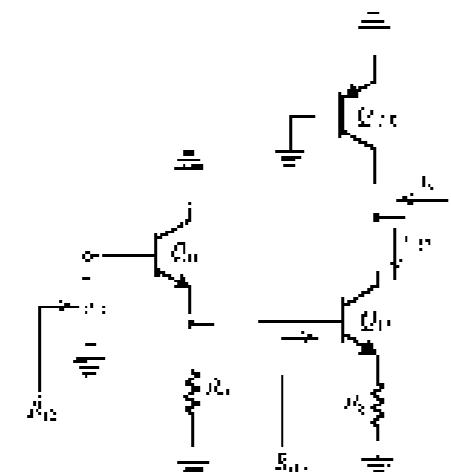


FIGURE 9.24 The 741 second stage prepared for small-signal analysis.

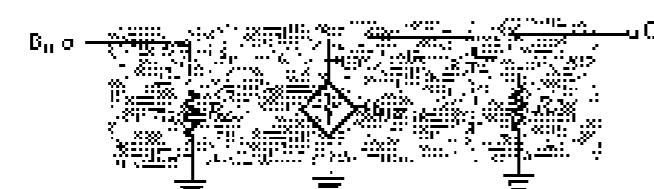


FIGURE 9.25 Small-signal equivalent circuit of the second stage.

Transconductance From the equivalent circuit of Fig. 9.25, we see that the transconductance G_{m2} is the ratio of the short-circuit current to the input voltage. Short-circuiting the output terminal of the second stage (Fig. 9.24) to ground makes the signal current through the output resistance of Q_{12} zero, and the output short-circuit current becomes equal to the collector signal current of Q_{12} , i_{c2} . This latter current can be easily related to v_{i1} as follows:

$$i_{c2} = \frac{\beta_{Q1} v_{i1}}{r_{e1} + R_2} \quad (9.72)$$

$$i_{c2} = \beta_{Q1} \frac{(R_2/r_{e1})}{(R_2/r_{e1}) + r_{e2}} \quad (9.73)$$

$$R_{in2} = (\beta_{Q1} + 1)(r_{e1} + R_2) \quad (9.74)$$

These equations can be combined to obtain

$$G_{m2} = \frac{i_{c2}}{v_{i1}} = \frac{r_{e2}}{r_{e1}} \quad (9.75)$$

which, for the 741 parameter values, is found to be $G_{m2} = 6.5 mA/V$.

Output Resistance To determine the output resistance R_{o2} of the second stage in Fig. 9.21, we ground the input terminal and find the resistance looking back into the output terminal. It follows that R_{o2} is given by

$$R_{o2} = (R_{out2}/R_{in2}) \quad (9.76)$$

where R_{out2} is the resistance looking into the collector of Q_{12} while its base and emitter are connected to ground. It can be easily seen that

$$R_{out2} = r_{e2} \quad (9.77)$$

For the 741 component values we obtain $R_{out2} = 900 k\Omega$.

The except component in Eq. (9.76), R_{in2} , is the resistance seen looking into the collector of Q_{11} , as indicated in Fig. 9.26. Since the resistance between the base of Q_{11} and ground is relatively small, one can considerably simplify matters by assuming that the base is grounded. Doing this, we can use Eq. (9.72) to determine R_{in2} . For our case the result is $R_{in2} = 18.7 k\Omega$. Combining R_{out2} and R_{in2} in parallel yields $R_{o2} = 81 k\Omega$.

Thevenin Equivalent Circuit The second-stage equivalent circuit can be converted to the Thevenin form, as shown in Fig. 9.27. Note that the stage open-circuit voltage gain is $-G_{m2}R_{L1}$.

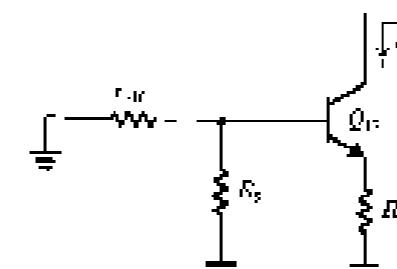


FIGURE 9.26 Definition of R_{in2} .

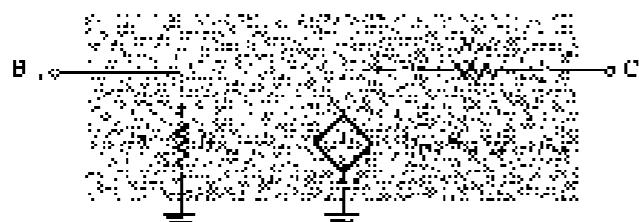


FIGURE 9.27 Thyvenin form of the small-signal model of the second stage.

- 9.17 Use Eq. 9.11 to verify that \$Q_{A2}\$ has 5 mA/V.
- 9.18 Use Eqs. 9.13 to 9.16 to verify that \$Q_{B2}\$ has 5 mA/V.
- 9.19 Verify that \$R_{B2} = 1 \text{ k}\Omega\$.
- 9.20 Verify that \$R_{C2} = 2 \text{ k}\Omega\$.
- 9.21 Verify that the voltage gain of the second stage is the 1/41.
- 9.22 Verify that the output voltage is \$26.5 \text{ V}\$.

9.5.3 The Output Stage

The 741 output stage is shown in Fig. 9.28 without the short-circuit protection circuitry. The stage is driven by the second-stage transistor \$Q_{C2}\$ and loaded with a 2-k\$\Omega\$ resistance. The circuit is of the AB class (Section 9.3.5), with the network composed of \$Q_1\$, \$Q_2\$, and \$R_{D2}\$ providing the bias of the output transistors \$Q_1\$ and \$Q_2\$. The use of this network rather than two diode-connected transistors in series enables biasing the output transistors at a low current (0.15 mA) in spite of the fact that the output devices are three times as large as the standard devices. This is obtained by arranging that the current in \$Q_1\$ is very small and thus its \$V_{BE}\$ is also small. We analyzed the driver in Section 9.4.7.

Another feature of the 741 output stage worth noting is that the stage is driven by an emitter follower (\$Q_1\$). As will be shown, this emitter follower provides voltage buffering, which makes the op-amp gain slope independent of the parameters of the output transistors.

Output Voltage Limits The maximum positive output voltage is limited by the saturation of current source transistor \$Q_{C2}\$. Thus

$$V_{Omax} = V_{CE2} + V_{DS2} = V_{CE2} \quad (9.84)$$

which is about 1 V below \$V_{CE2}\$. The minimum output voltage (i.e., maximum negative amplitude) is limited by the saturation of \$Q_1\$. Neglecting the voltage drop across \$R_{D2}\$, we obtain

$$V_{Omin} = -V_{CE2} - V_{DS1} = V_{CE2} + V_{DS1} \quad (9.85)$$

which is about 1.5 V above \$V_{CE2}\$.

Small-Signal Model We shall now carry out a small-signal analysis of the output stage for the purpose of determining the values of the parameters of the equivalent circuit model shown in Fig. 9.29. Note that this model is based on the general amplifier-equivalent circuit presented in Table 5.5 as "Equivalent Circuit A." The model is shown fed by \$v_{o2}\$, which is

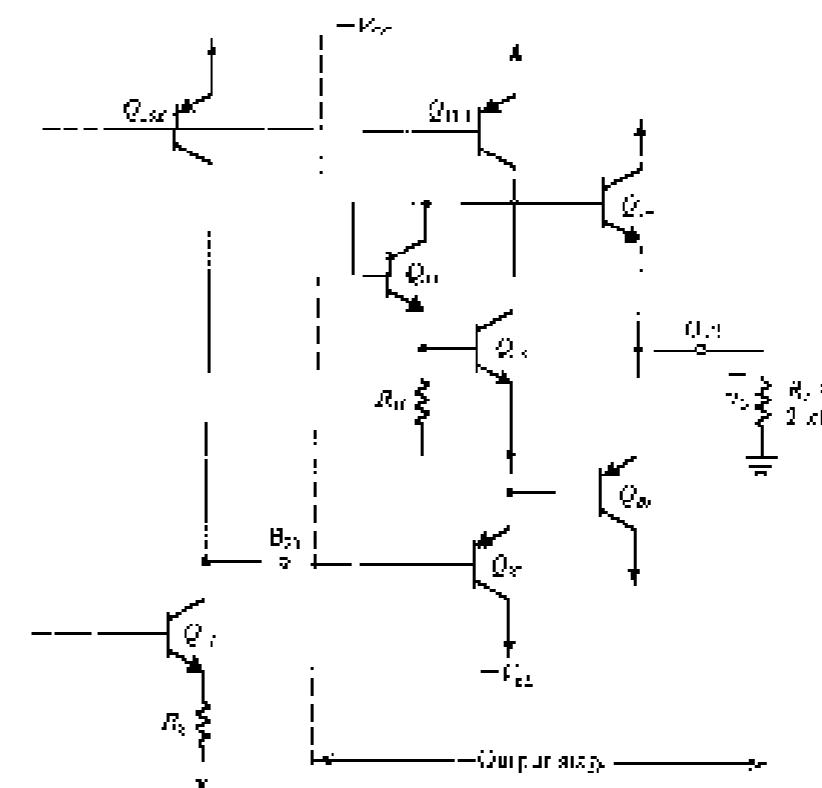


FIGURE 9.28 The 741 output stage.

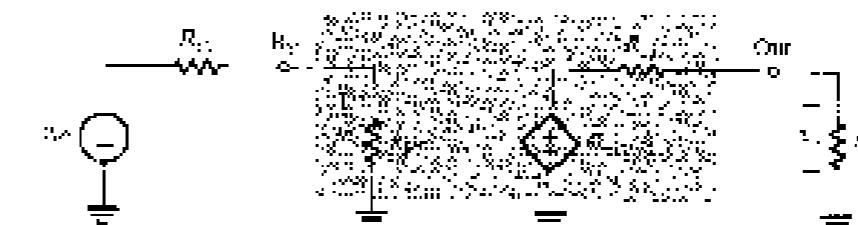


FIGURE 9.29 Model for the 741 output stage. This model is based on the amplifier-equivalent circuit presented in Table 5.5 as "Equivalent Circuit A."

The open-circuit output voltage of the second stage, from Eq. 9.21, is given by

$$v_{o2} = -G_{o2}A_{o2}v_{in} \quad (9.86)$$

where \$G_{o2}\$ and \$A_{o2}\$ were previously determined as \$G_{o2} = 6.5 \text{ mA/V}\$ and \$A_{o2} = 81 \text{ k}\Omega\$. Recall that \$R_{in}\$ is the input resistance of the output stage determined with the amplifier loaded with \$R_{D2}\$. Although the effect of loading an amplifier stage on its input resistance is negligible in the input and second stages, this is not the case in general in an output stage. Defining \$R_{pi}\$ in this manner (see Table 5.5) enables correct evaluation of the voltage gain of the second stage, \$A_{o2}\$, as

$$A_{o2} = \frac{v_{o2}}{v_{in}} = (G_{o2}R_{in}) \frac{R_{D2}}{R_{D1} + R_{D2}} \quad (9.87)$$

To determine R_{in} , assume that one of the two output transistors, say, Q_{11} , is conducting a current of, say, 5 mA . It follows that the input resistance looking into the base of Q_{11} is approximately $\beta_1 R_L$. Assuming $\beta_{10} = 50$, for $R_L = 3 \text{ k}\Omega$ the input resistance of Q_{11} is $150 \text{ k}\Omega$. This resistance appears in parallel with the series combination of the output resistance of (Q_{11}, Q_{12}) ($280 \text{ k}\Omega$) and the resistance of the $Q_{10}-Q_{11}$ network. The latter resistance is very small (about $60 \text{ k}\Omega$; see later Exercise 9.26). Thus the total resistance in the emitter of Q_{11} is approximately $(150 \text{ k}\Omega / 280 \text{ k}\Omega)$ or $72 \text{ k}\Omega$ and the input resistance R_{in} is given by

$$R_{\text{FB}} := G_0 \times 7.1 \text{ k}\Omega$$

which for $\rho_2 = 50$ is $R_{\text{eq}} = 4.4 \text{ M}\Omega$. Since $R_{\text{in}} = 37 \text{ k}\Omega$, we see that $R_{\text{out}} \gg R_{\text{in}}$, and the value of R_{out} will have little effect on the performance of the op-amp. We can use the values obtained for R_{in} to determine the gain of the second stage using Eq. (2.37) as $A_2 = -1.5 \text{ V/V}$. The value of A_2 will be needed in Section 9.6 in connection with the frequency-response analysis.

Continuing with the determination of the equivalent circuit model-parameters, we note from Fig. 3.29 that $G_{12} = 0$, i.e., the open-circuit overall voltage gain of the output stage,

$$G_{4,3} \leftarrow \frac{v_3}{c_{4,3}} \quad (9.88)$$

With $R_7 \rightarrow \infty$, the gain of the emitter-follower output transistor (Q_1 or Q_{3D}) will be nearly unity. Also, with $R_7 \rightarrow \infty$, the resistance in the emitter of Q_3 will be very large. This means that the gain of Q_3 will be nearly unity and the input resistance of Q_3 will be very large. We thus conclude that: $G_{1,2} \approx 1$.

Next, we shall find the value of the output resistance of the op amp, R_o . For this purpose refer to the circuit shown in Fig. 4-10. In accordance with the definition of R_o , the input source feeding the output stage is grounded, but its resistance (which is the output

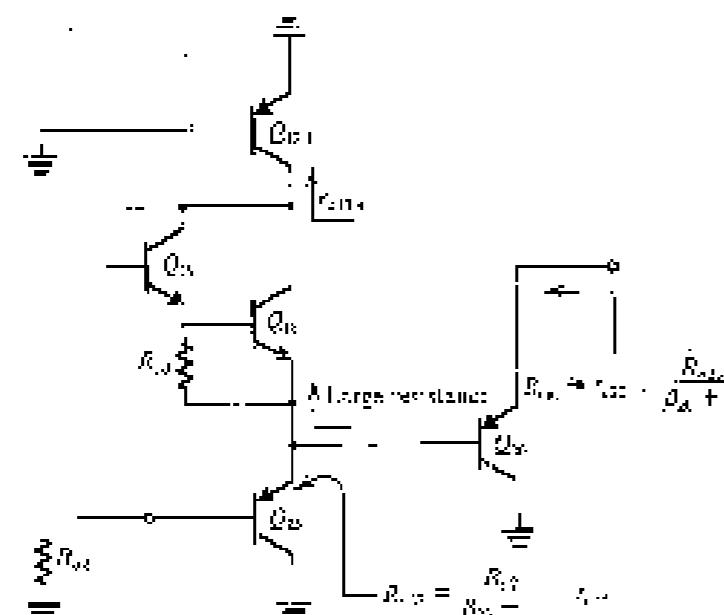


FIGURE 9.30 Circuits for finding the output resistance: (a) short-circuited load; (b) open-circuited load.

resistance of the second stage, R_{Q_2}) is included. We have assumed that the output voltage v_2 is negative, and thus Q_{21} is conducting more of the current; transistor Q_{22} has therefore been eliminated. The exact value of the output resistance will of course depend on which transistor (Q_{21} or Q_{22}) is conducting and on the value of load current. Nevertheless, we wish to find an estimate of R_{out} .

As indicated in Fig. 9.30, the resistance seen looking into the end of Q_1 is

$$R_{\text{eff}} = \frac{R_{12}}{\beta_{12} - 1} + r_{12} \quad (4.80)$$

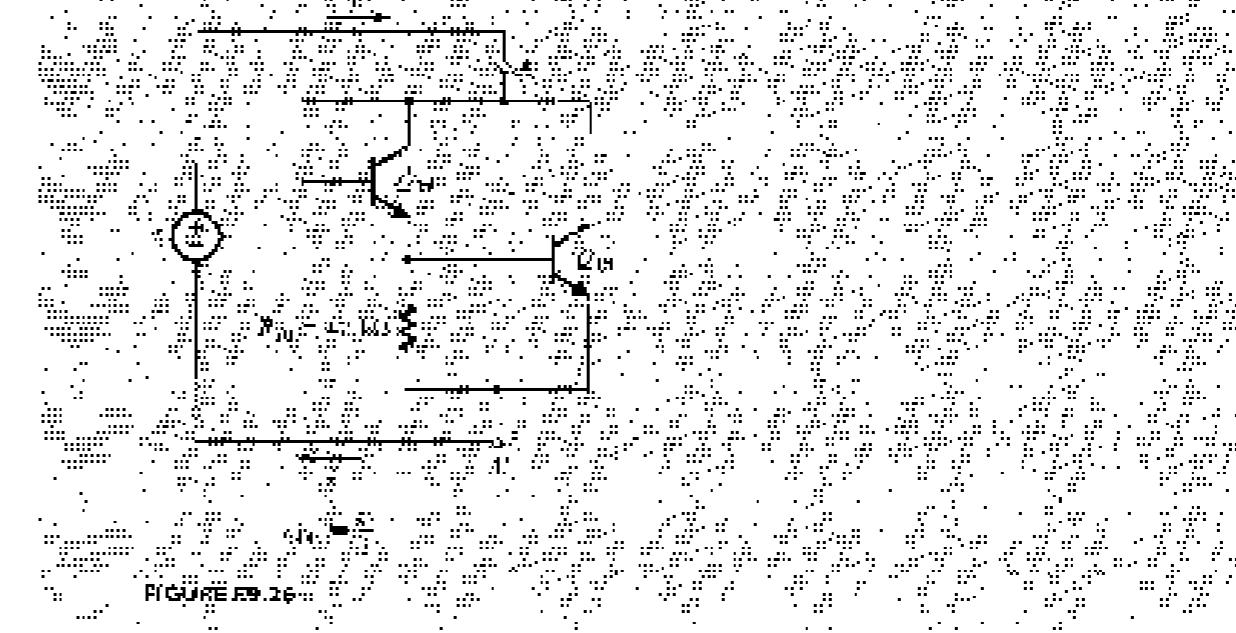
Substituting $R_{\text{in}} = 81 \text{ k}\Omega$, $\beta_I = 50$, and $r_{\text{ce}} = 2500.18 = 136 \text{ }\Omega$ yields $R_{\text{out}} = 1.72 \text{ }\mu\Omega$. This resistance appears in parallel with the series combination of r_{ce} and the resistance in the Q_1 - Q_2 network. Since r_{ce} (here $136 \text{ }\mu\Omega$) is much larger than R_{out} , the effective resistance between the base of Q_2 and ground is approximately equal to R_{out} . Now we can find the output resistance of Q_2 :

$$R_{\text{in}} = \frac{R_{\text{ext}}}{B_{\text{in}} + 1} - r_{\text{ext}} \quad (3.30)$$

For $\beta_{21} = 20$, the first component of R_{21} is 3–12. The second component depends on mainly on the value of output current. For an output current of 5 mA, $r_{21} = 3.51$ and $R_{21,2} = 39.32$. To this value we must add the resistance R_2 (27 Ω) (see Fig. 9.15), which is included for short-circuit protection. The output resistance of the 741 is specified to be typically 75 Ω.

EFERIS

- 226-1: Using a sample size of 200, results for each of the four transition matrices in Table 10.12, Table 10.13, Table 10.14, and Table 10.15, show no significant differences between $\hat{\pi}_t$ and π_t . For all four transition matrices, $\hat{\pi}_t$ and π_t are very similar.



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Figure 9.27 shows the circuit for determining the open-circuit resistance, which is primarily a load-dissolving resistor for the current. Using the resistance of the Q_{14} output stage calculated in Example 9.12, and assuming the large-signal resistance of Q_{14} is $1\text{ k}\Omega$ when it is sourcing an output current of 5 mA ,

and since

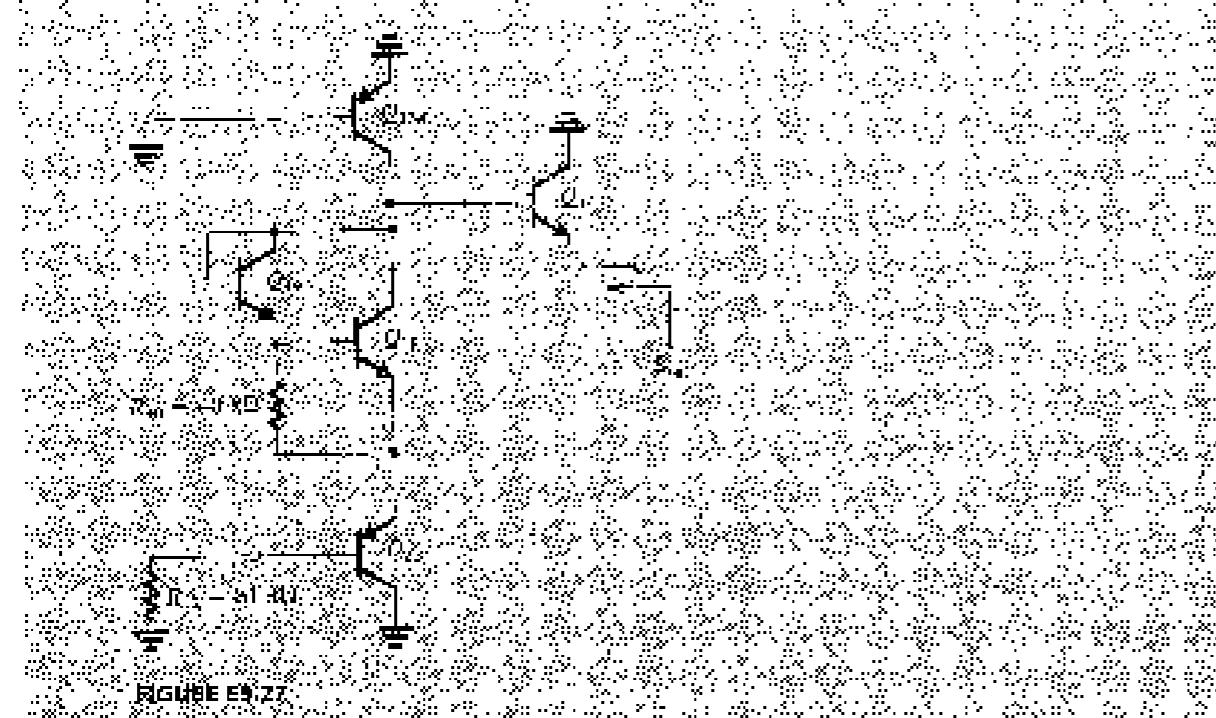


FIGURE 9.27

Output Short-Circuit Protection. If the op-amp output terminal is short-circuited to one of the power supplies, one of the two output transistors could conduct a large amount of current. Such a large current can result in sufficient heating to cause burnout of the IC (Chapter 14). To guard against this possibility, the 741 op-amp is equipped with a special circuit for short-circuit protection. The function of this circuit is to limit the current in the output transistors in the event of a short circuit.

Refer to Fig. 9.12. Resistance R_6 together with transistor Q_{14} forms the current that would flow out of Q_{14} in the event of a short circuit. Specifically, if the current in the emitter of Q_{14} exceeds about 20 mA , the voltage drop across R_6 exceeds 54 mV , which turns Q_{14} on. As Q_{14} turns on, its collector aids some of the current supplied by Q_{13} , thus reducing the base current of Q_{14} . This mechanism thus limits the maximum current that the op-amp can source (i.e., supply from the output terminal in the outward direction) to about 20 mA .

Limiting of the maximum current that the op-amp can sink, and hence the current through Q_{13} , is done by a mechanism similar to the one discussed above. The relevant circuit is composed of R_5 , Q_{13} , Q_{14} , and Q_{12} . For the components shown, the current in the inward direction is limited also to about 20 mA .

9.6 GAIN, FREQUENCY RESPONSE, AND SLEW RATE OF THE 741

In this section we shall evaluate the overall small-signal voltage gain of the 741 op-amp. We shall then consider the op-amp's frequency response and its slew-rate limitation.

9.6.1 Small-Signal Gain

The overall small-signal gain can be easily found from the cascade of the equivalent circuits derived in the preceding sections for the three op-amp stages. This cascade is shown in Fig. 9.31, loaded with $R_L = 2\text{ k}\Omega$, which is the typical value used in measuring and specifying the 741 data. The overall gain can be expressed as

$$\frac{v_o}{v_i} = \frac{R_L v_{o2} v_{o3}}{R_1 v_{i1} v_{i2}} \quad (9.91)$$

$$= -C_{o3}(R_{o3}/\beta R_{13})(-C_{o2}K_{12})G_{12} \cdot \frac{R_L}{R_1 + R_{o2}}. \quad (9.92)$$

Using the values found earlier yields for the overall open-circuit voltage gain,

$$A_o = \frac{v_o}{v_i} = -76.1 \times (-526.5) \times 0.97 = 393,147 \text{ V/V} \quad (9.93)$$

$$= 107.7 \text{ dB}$$

9.6.2 Frequency Response

The 741 is an internally compensated op-amp. It employs the Miller compensation technique, studied in Section 8.11.3, to introduce a dominant low-frequency pole. Specifically, a 30-pF capacitor (C_5) is connected in the negative-feedback path of the second stage. An approximate estimate of the frequency of the dominant pole can be obtained as follows.

Using Miller's theorem (Section 6.4.4) the effective capacitance due to C_5 between the base of Q_{12} and ground is (see Fig. 9.3)

$$C_{\text{eff}} = C_5(1 + A_{12}) \quad (9.94)$$

where A_{12} is the second-stage gain. Use of the value calculated for A_{12} in Section 9.5.3, $A_{12} = -515$, results in $C_{\text{eff}} = 15.480\text{ pF}$. Since this capacitance is quite large, we shall neglect all other capacitances between the base of Q_{12} and signal ground. The total resistance between this node and ground is

$$R_b = (R_{12}\beta R_{13})$$

$$= (6.7 \text{ M}\Omega)(4 \text{ MHz}) = 2.5 \text{ M}\Omega \quad (9.95)$$

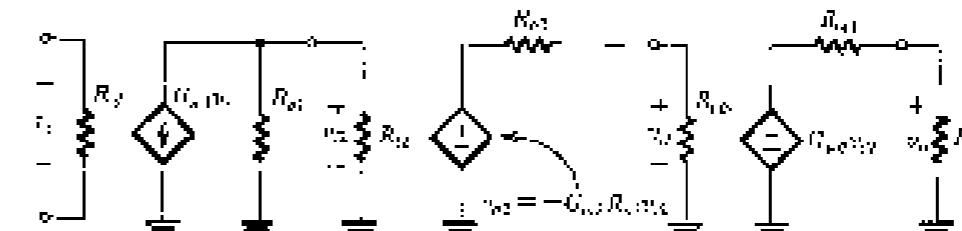


FIGURE 9.31 Calculating the small-signal equivalent circuit of the individual stages for the evaluation of the overall voltage gain.

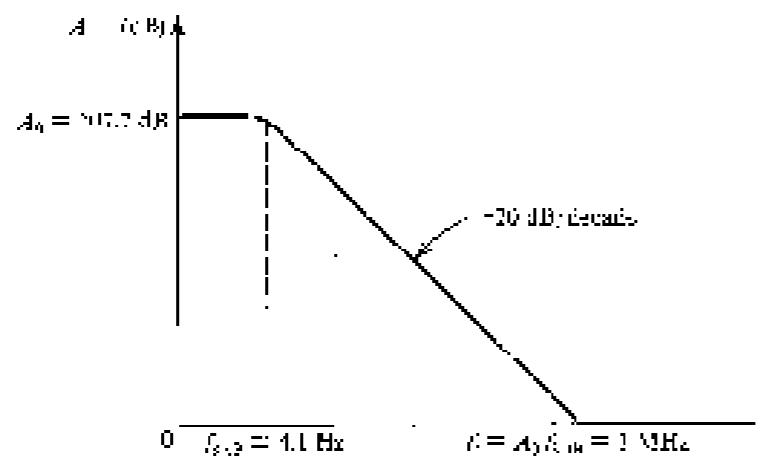


FIGURE 9.32 Bode plot of the 741 gain, neglecting nondominant poles.

Thus the dominant pole has a frequency f_p given by

$$f_p = \frac{1}{2\pi C_m R_2} = 1.1 \text{ Hz} \quad (9.98)$$

It should be noted that this approach is equivalent to using the approximate formula in Eq. (8.87).

As discussed in Section 8.1.3, Miller compensation provides an additional advantage: effect, namely pole splitting. As a result, the other poles of the circuit are moved to very high frequencies. This has been confirmed by computer-aided analysis [see Gray et al. (2001)].

Assuming that all nondominant poles are at very high frequencies, the calculated values give rise to the Bode plot shown in Fig. 9.32 where $f_{p,2} = f_p$. The unity-gain bandwidth f_t can be calculated from

$$f_t = A_0 f_{p,2} \quad (9.99)$$

Thus,

$$f_t = 246,147 \times 1.1 = 1 \text{ MHz} \quad (9.100)$$

Although this Bode plot implies that the phase shift $\omega_c f_t \approx -40^\circ$ and thus that the phase margin is 90° , in practice a phase margin of, say, 80° is obtained. The excess phase shift ($\approx 10^\circ$) is due to the nondominant poles. This phase margin is sufficient to provide stable operation of a two-loop amplifier with any value of feedback factor β . This convenience of use of the internally compensated 741 is achieved at the expense of a great reduction in open-loop gain and hence in the amount of negative feedback. In other words, it requires a closed-loop amplifier with a gain of 1000. Just the 741 is overcompensated for such an application, and one could be much better off designing one's own compensation (assuming, of course, the availability of an op amp that is not internally compensated).

9.6.3 A Simplified Model

Figure 9.33 shows a simplified model of the 741 op amp in which the high-gain second stage, with its feedback capacitance C_{fb} , is modeled by an ideal integrator. In this model, the

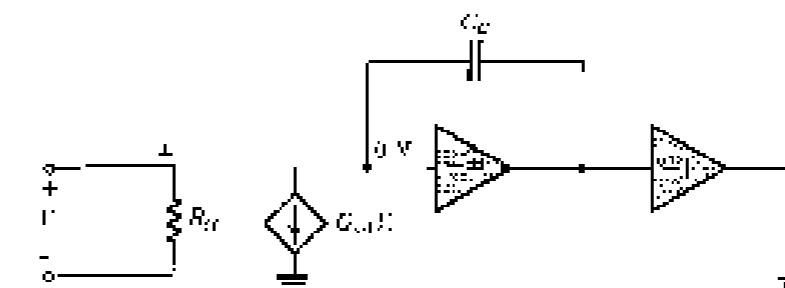


FIGURE 9.33 A simple model for the 741, based on modeling the second stage as an integrator.

gain of the second stage is assumed sufficiently large that a virtual ground appears at its input. For this reason the output resistance of the input stage and the input resistance of the second stage have been omitted. Furthermore, the output stage is assumed to be an ideal unity-gain follower. Except for the presence of the output stage, this model is identical to that which we used for the two-stage CMOS amplifier in Section 9.1.4 (Fig. 9.5).

Analysis of the model in Fig. 9.33 gives

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_m2}{sC_2} \quad (9.101)$$

Thus,

$$A(j\omega) = \frac{G_m2}{j\omega C_2} \quad (9.102)$$

and the magnitude of gain becomes unity at $\omega = \omega_t$, where

$$\omega_t = \frac{G_m2}{C_2} \quad (9.103)$$

Substituting $G_m2 = 15.26 \text{ mA/V}$ and $C_2 = 30 \text{ pF}$ yields

$$\omega_t = \frac{G_m2}{3\pi} = 1 \text{ MHz} \quad (9.104)$$

which is equal to the value calculated before. It should be pointed out, however, that this model is valid only at frequencies $f < f_{t,2}$. At such frequencies the gain falls off with a slope of -20 dB/decade , just like that of an integrator.

9.6.4 Slew Rate

The slew-rate limitation of op amps is discussed in Chapter 2. Here we shall illustrate the origin of the slewing phenomena in the context of the 741 circuit.

Consider the unity-gain follower of Fig. 9.34 with a step of, say, 10 V applied at the input. Because of amplifier dynamics, its output will not change in zero time. This naturally affects the input as the input is amplified, almost linearly, the value of the step will appear as a differential signal between the two input terminals. This large input voltage causes the input stage to be overdriven, and its small-signal model no longer applies. Rather, both the stage cut-offs and the other half conduct all the current. Specifically, reference to Fig. 9.13 shows that a large positive differential input voltage causes Q_1 and Q_2 to conduct all the available bias current (I_b) while Q_3 and Q_4 will be cut off. The current mirror Q_5 , Q_6 , and Q_7 will still function, and Q_8 will produce a collector current of $2I_b$.

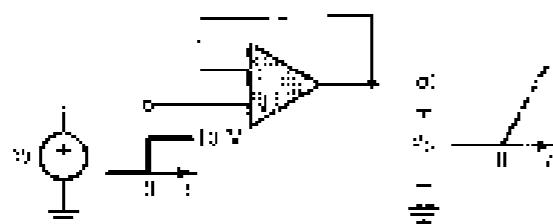


FIGURE 9.34 A unity-gain follower with a large step input. Since the output voltage cannot keep increasing, until the large differential voltage is fed between the op-amp input terminals.

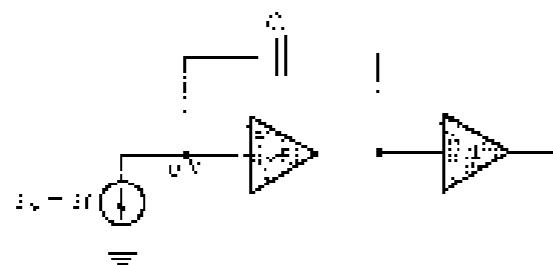


FIGURE 9.35 Miller circuit 741 operating with a large positive differential voltage applied.

Using the calculations above, and modeling the second stage as an (ideal) integrator, results in the model of Fig. 9.36. From this circuit we see that the output voltage will be a ramp with a slope of $2V_1/C_V$.

$$\omega_c(t) = \frac{2I}{C_V} \quad (9.103)$$

Thus the slew rate SR is given by

$$SR = \frac{\omega_c}{C_V} \quad (9.104)$$

For the 741, $I = 9.5 \mu\text{A}$ and $C_V = 70 \text{ pF}$, resulting in $SR = 0.63 \text{ V/}\mu\text{s}$.

It should be pointed out that this is a rather simple model of the slewing process. More detail can be found in Gray et al. (2002).

EXERCISE

- 9.28 (10 points) If the Miller circuit of Fig. 9.35 is used in the fall of the V_{DD} voltage, calculate the slew rate. Assume that the load current is $\pm 10 \mu\text{A}$ and $C_V = 70 \text{ pF}$. Hint: The Miller circuit is equivalent to a single-stage op-amp with a negative feedback loop.

9.6.5 Relationship Between f_T and SR

A simple relationship exists between the unity-gain bandwidth, f_T , and the slew rate SR. This relationship is obtained from Eqs. (9.101) and (9.104) together with

$$G_{AV} = \frac{2I}{f_T}$$

where r_i is the common-emitter resistance of each of Q_1 through Q_4 . Thus

$$I = \frac{V_T}{r_i}$$

and

$$G_{AV} = \frac{I}{2r_i} \quad (9.105)$$

Substituting in Eq. (9.101) results in

$$\omega_c = \frac{I}{2C_V V_T} \quad (9.106)$$

Substituting for I/C_V from Eq. (9.104) gives

$$\omega_c = \frac{SR}{4V_T} \quad (9.107)$$

which can be expressed in the alternative form

$$SR = 4V_T \omega_c \quad (9.108)$$

As a check, for the 741 we have

$$SR = 4 \times 75 \times 10^{-3} \times 2\pi \times 10^7 = 0.63 \text{ V/}\mu\text{s}$$

which is the result obtained previously. Observe that Eq. (9.108) is of the same form as Eq. (9.41), which applies to the two-stage CMOS op-amp. Here, $4V_T$ replaces V_{DD} . Since, typically, V_{DD} will be two to three times the value of $4V_T$, a two-stage CMOS op-amp with an f_T equal to that of the 741 exhibits a slew rate that is two to three times as large as that of the 741.

A general form for the relationship between SR and ω_c for an op-amp with a structure similar to that of the 741 (including the two-stage CMOS circuit) is

$$SR = \alpha/\omega_c$$

where α is the constant of proportionality relating the transconductance of the first stage G_{AV} to the total bias current to the input differential stage. That is, for the 741, $G_{AV} = \alpha/I$, while for the CMOS circuit of Fig. 9.1, $G_{AV} = \alpha I^2$. Thus, given α , a higher value of SR is obtained by making α smaller; that is, the total bias current is kept constant and G_{AV} is reduced. This is a viable technique for increasing slew rate. It is referred to as the G_{AV} -reduction method (see Exercise 9.30).

EXERCISES

- 9.29 (10 points) The 741 has a f_T of 10 Hz . If the input voltage is varied at a rate of $10 \text{ V/}\mu\text{s}$, calculate the slew rate. Hint: The Miller circuit is equivalent to a single-stage op-amp with a negative feedback loop.
- Ans. $0.27 \text{ V/}\mu\text{s}$
- 9.30 (10 points) A two-stage CMOS op-amp has a f_T of 10 Hz . If the input voltage is varied at a rate of $10 \text{ V/}\mu\text{s}$, calculate the slew rate. Hint: The output of R_{out} is fed back to the N node, the node before the load resistor. Hint: The new values of C_V , the f_T , and the 5-dB frequency?
- Ans. $0.083 \text{ V/}\mu\text{s}$
- 9.31 (10 points) If $f_T = 10 \text{ Hz}$ for a 741, calculate the slew rate if the f_T is increased to 100 Hz . Hint: The f_T is increased by a factor of 10, so the G_{AV} is reduced by a factor of 10. Hint: The G_{AV} is reduced by a factor of 10, so the f_T is increased by a factor of 10.

⁵ The difference is just a factor of 10, since the 741 contains one more stage than the input differential stage of the CMOS circuit, and we used 24 for the 741 instead.

9.7 DATA CONVERTERS—AN INTRODUCTION

In this section we begin the study of another group of analog IC circuits of great importance; namely, data converters.

9.7.1 Digital Processing of Signals

Most physical signals, such as those obtained at transducer outputs, exist in thealog form. Some of the processing required on these signals is most conveniently performed in an analog fashion. For instance, in instrumentation systems it's quite common to use a high-gain impedance, high-GMRR differential amplifier right at the output of the transducer. This is usually followed by a filter whose purpose is to eliminate interference. However, further signal processing is usually required, which can range from simply obtaining a measurement of signal strength to performing some algebraic manipulations on this and related signals to obtain the value of a particular system parameter of interest, as is usually the case in systems intended to provide a complex control function. Another example of signal processing can be found in the common need for transmission of signals to a remote receiver.

Many such forms of signal processing can be performed by using micros. In earlier chapters we encountered circuits for implementing a number of such tasks. However, an alternative alternative exists. It is to convert, following some initial analog processing, the signal from analog to digital form and then use economical, accurate, and cost-reducing digital ICs to perform digital signal processing. Such processing can in its simplest form provide us with a measure of the signal strength as an easy-to-read number (or word, e.g., 16-bit digital word). In more involved cases the digital signal processor can perform a variety of arithmetic and logic operations that implement a filtering algorithm. The resulting digital filter does many of the same tasks that an analog filter performs—namely, eliminate noise, reference, and so on. Yet another example of digital signal processing is found in digital communications systems, where signals are transmitted in a sequence of binary pulses, with the obvious advantage that corruption of the amplitudes of these pulses by noise is, to a large extent, of no consequence.

Once digital signal processing has been performed, we might be content to display the result in digital form, such as a printed list of numbers. Alternatively, we might require an analog output. Such is the case in a telecommunications system, where the final output may be audible speech. If such an analog output is desired, then obviously we need to convert the digital signal back to an analog form.

This is not our purpose here to study the techniques of digital signal processing. Rather, we shall examine the interface circuits between the analog and digital domains. Specifically, we shall study the basic techniques and circuits employed to convert an analog signal to digital form (analog-to-digital or simply A/D conversion) and those used to convert a digital signal to analog form (digital-to-analog or simply D/A conversion). Digital circuits are studied in Chapters 10 and 11.

9.7.2 Sampling of Analog Signals

The principle underlying digital signal processing is that of sampling the analog signal. Figure 9.36 illustrates in a conceptual form the process of obtaining samples of an analog signal. The switch shown closes periodically under the control of a periodic pulse signal ($\bar{S}(t)$). The closure time of the switch, t_s , is relatively short, and the samples obtained are

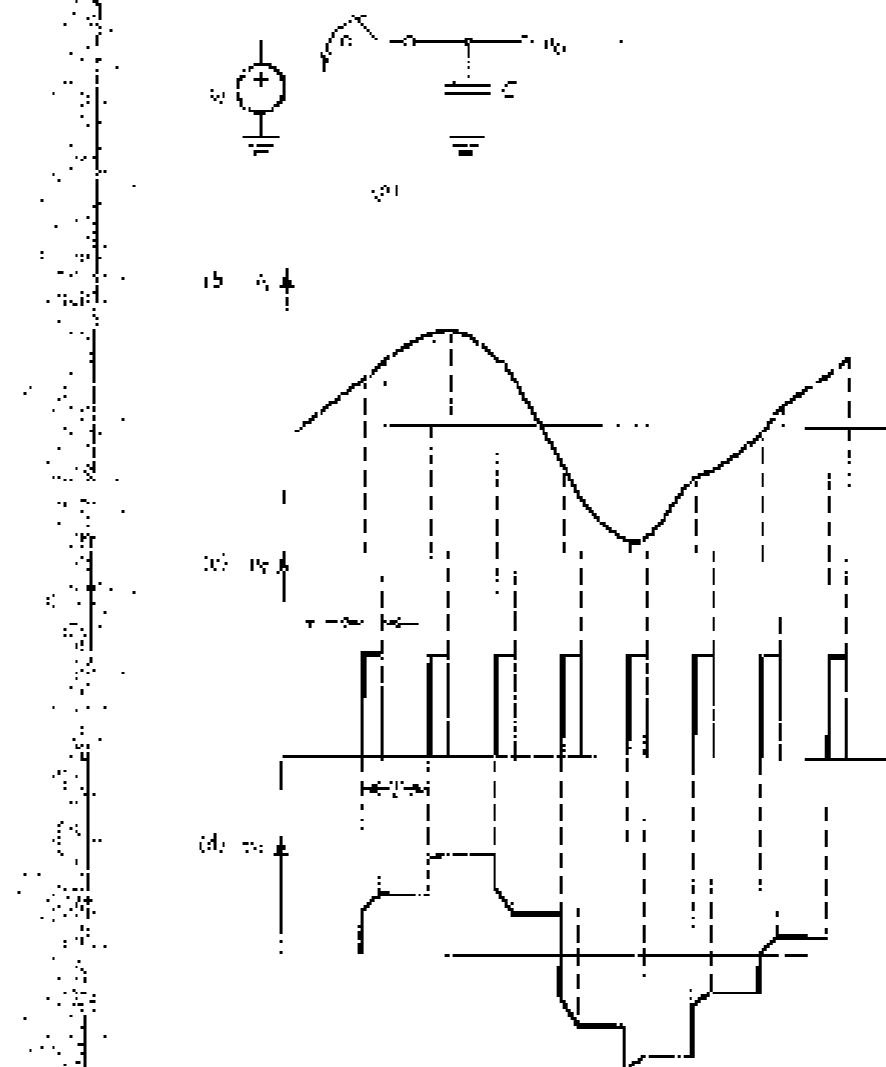


FIGURE 9.36 The process of periodically sampling an analog signal. (a) Sample-and-hold (S/H) circuit. The switch closes for a small portion of every clock period (T_s). (b) Input signal $V_a(t)$ and output signal $V_o(t)$. (c) Sampling clock $S(t)$ and digital output $D(t)$.

stored (held) on the capacitor. The circuit of Fig. 9.36 is known as a sample-and-hold (S/H) circuit. As indicated, the S/H circuit consists of an analog switch that can be implemented by a MOSFET transmission gate (Section 10.5), a storage capacitor, and (not shown) a buffer after it.

Between the sampling intervals—that is, during the hold intervals—the voltage level on the capacitor represents the signal samples we have taken. Each of these voltage levels is then fed to the input of an A/D converter, which provides an N-bit binary number proportional to the value of signal sample.

The fact that we can do our processing on a limited number of samples of an analog signal while ignoring the analog signal details between samples is based on the Shannon's sampling theorem [see Lathi (1985)].

9.7.3 Signal Quantization

Consider an analog signal whose voltage range from 0 to 10 V. Let us assume that we wish to convert this signal to digital form and that the required output is a 4-bit digital signal.⁴ We know that a 4-bit binary number can represent 16 different values, 0 to 15; it follows that the resolution of our conversion will be $10\text{ V}/15 = \frac{2}{3}\text{ V}$. Thus an analog signal of 0 V will be represented by 0000, $\frac{2}{3}\text{ V}$ will be represented by 0001, $\frac{4}{3}\text{ V}$ will be represented by 0010, and 10 V will be represented by 1111.

All these sample numbers are multiples of the basic increment $\frac{2}{3}\text{ V}$. A question now arises regarding the conversion of currency that fall between these successive intermediate levels. For instance, consider the case of a 0.2-V analog level. This falls between $\frac{2}{3}\text{ V}$ and $\frac{4}{3}\text{ V}$. However, since it is closer to $\frac{2}{3}\text{ V}$ we treat it as if it were $\frac{2}{3}\text{ V}$ and code it as 1001. This process is called quantization. Obviously errors are inherent in this process; such errors are called quantization errors. Using more bits to represent tolerance or, simply, resolution, analog signal reduces quantization errors but requires more complex circuitry.

9.7.4 The A/D and D/A Converters as Functional Blocks

Figure 9.37 depicts the functional block representations of A/D and D/A converters. As indicated, the A/D converter (also called an ADC) accepts an analog sample v_a and produces an N -bit digital word. Conversely, the D/A converter (also called a DAC) accepts an N -bit digital word and produces an analog sample. The output samples of the D/A converter are often fed to a sample-and-hold circuit. At the output of the S/H circuit a waveform such as that in Fig. 9.38 is obtained. The staircase waveform can then be smoothed by a

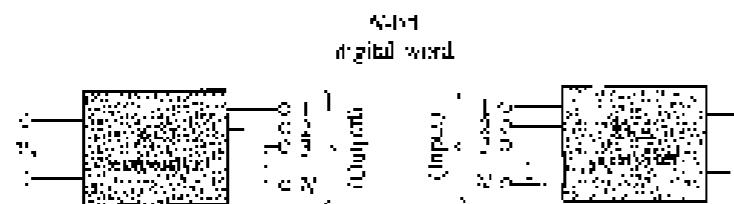


FIGURE 9.37 The A/D and D/A converters as functional blocks.

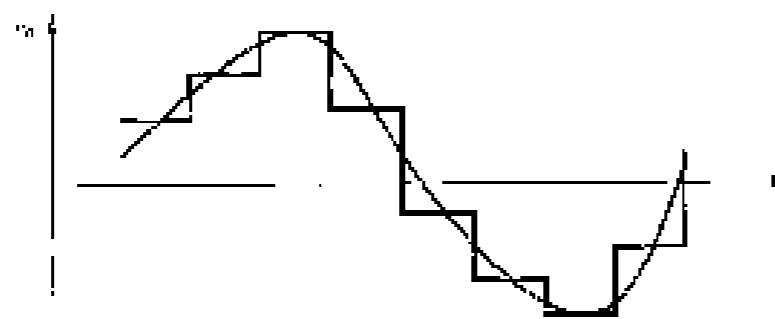


FIGURE 9.38 The staircase output of the output of a D/A converter is usually fed to a sample-and-hold circuit to obtain the steady-state value shown. This waveform can then be filtered to obtain the smooth waveform shown in order that it may be measured by the metering circuit.

⁴ Bit stands for binary digit.

low-pass filter, giving rise to the smooth curve shown in color in Fig. 9.38. In this way an analog output signal is reconstructed. Finally, note that the quantization error of an A/D converter is equivalent to ± 1 least significant bit (b_N).

EXERCISE

- 9.8.1 A sampling signal with a frequency of 10 Hz is converted to a 3.8 kHz digital output. If the original signal has a bandwidth of 10 Hz , what is the digital representation of the signal? What is the maximum quantization error in the digital output? Assume that the quantization error is uniform. What is the percentage of the quantization error in dB? Recall that the largest possible quantization error is $\pm 1/2$ of the quantization interval. Hint: $10\text{ Hz} = 10/(2\pi f) = 1.591\text{ rad/s}$; $10\text{ Hz} = 10/(10^3/2\pi) = 0.0004\text{ s}^{-1} = 0.00423\text{ rad/s}$.

9.8 D/A CONVERTER CIRCUITS

9.8.1 Basic Circuit Using Binary-Weighted Resistors

Figure 9.39 shows a simple circuit for an N -bit D/A converter. The circuit consists of a reference voltage V_{ref} , N binary-weighted resistors $R_1, 2R_1, 4R_1, \dots, 2^{N-1}R_1$, a single-pole switch S_1 , binary switches S_2, S_3, \dots, S_N , and an op-amp together with its feedback resistance $R_f = R/2$.

The switches are controlled by an N -bit digital input word D ,

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \dots + \frac{b_N}{2^N} \quad (9.109)$$

where b_1, b_2 , and b_N are bit coefficients that are either 1 or 0. Note that the bit b_N is the least significant bit (LSB) and b_1 is the most significant bit (MSB). In the circuit in Fig. 9.39, b_1 controls switch S_1 , b_2 controls S_2 , and so on. When $b_i = 0$, switch S_i is in position 1, and when $b_i = 1$, switch S_i is in position 2.

Since position 1 of all switches is ground and position 2 is virtual ground, the current through each resistor remains constant. Each switch simply connects where its corresponding current goes to ground (when the corresponding bit is 0) or to virtual ground (when the corresponding bit is 1). The currents flowing into the virtual ground add up, and the sum flows

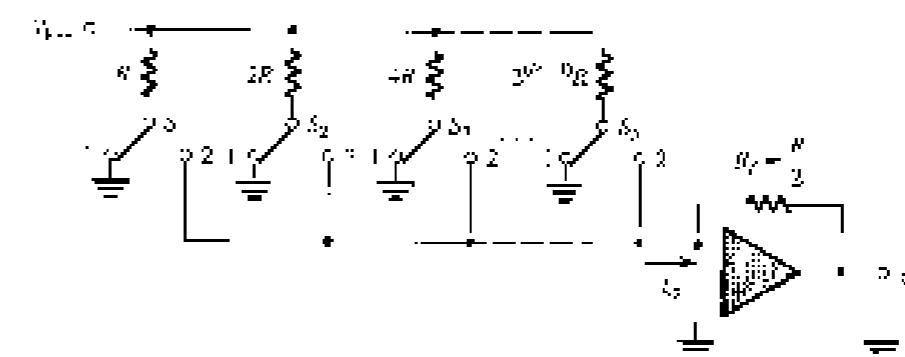


FIGURE 9.39 An N -bit D/A converter using binary-weighted resistor-based method.

through the feedback resistor R_f . The total current i_o is therefore given by

$$\begin{aligned} i_o &= \frac{V_{ref} b_1}{R} + \frac{V_{ref} b_2}{2R} + \dots + \frac{V_{ref} b_N}{2^{N-1} R} \\ &= \frac{2V_{ref}(b_1 - b_2 + \dots + b_N)}{R(2^N - 2)} \end{aligned}$$

Thus,

$$i_o = \frac{2V_{ref} D}{R} \quad (9.10)$$

and the output voltage v_o is given by

$$v_o = i_o R_o = -i_o R_f \quad (9.11)$$

which is directly proportional to the digital word D , as desired.

It should be noted that the accuracy of the DAC depends critically on (1) the accuracy of V_{ref} , (2) the precision of the binary-weighted resistors, and (3) the precision of the switches. Regarding the third point, we should emphasize that these switches handle analog signals, and their performance is of considerable interest. While the offset voltage and the ratio of resistance are not of critical significance at a digital switch, these parameters are of extreme importance in analog switches. The use of MOSFETs to implement analog switches will be discussed in Chapter 10. Also, we shall shortly see that practical circuit implementations of the DAC, the binary-weighted currents are generated by current sources. In this case, the analog switch can be realized using the differential pair circuit, as will be shown shortly.

A disadvantage of the binary-weighted resistor network is that, for a large number of bits ($N > 4$), the spread between the smallest and largest resistances becomes quite large. This implies difficulties in maintaining accuracy in resistor values. A more conventional scheme exists utilizing a resistive network called the $R-2R$ ladder.

9.8.2 R-2R Ladders

Figure 9.40 shows the basic arrangement of a DAC using an $R-2R$ ladder. Because of the small spread in resistor values, this network is usually preferred to the binary-weighted scheme discussed earlier, especially for $N > 4$. Operation of the $R-2R$ ladder is straightforward. First, it can be shown, by starting from the right and working toward the left, that the

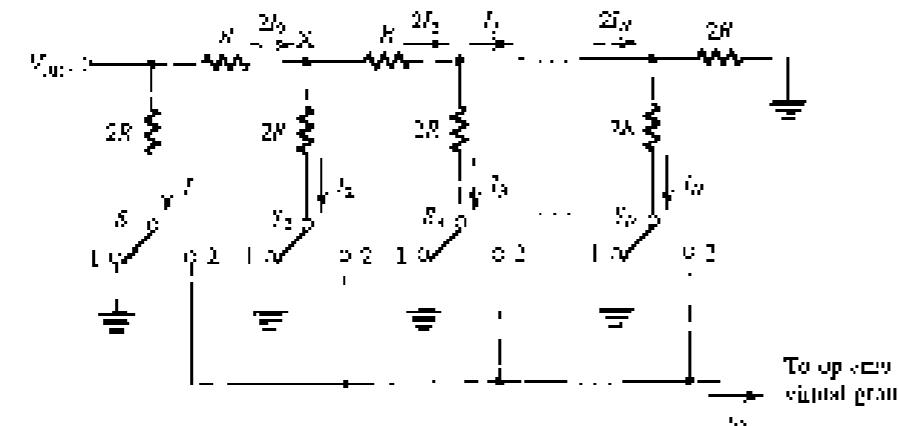


FIGURE 9.40 The basic b_1 – b_N circuit of a DAC utilizing an $R-2R$ ladder network.

resistance to the right of each ladder node, such as that labeled X , is equal to $2R$. Thus the current flowing to the right, away from each node, is equal to the current flowing downward to ground, and twice the current flows in to the node from the left side. It follows that

$$I = I_1 = I_2 = \dots = 2^{N-1} i_o \quad (9.12)$$

Thus, as in the binary-weighted resistive network, the currents controlled by the switches are binary weighted. The output current i_o will therefore be given by

$$i_o = \frac{V_{ref} D}{R} \quad (9.13)$$

9.8.3 A Practical Circuit Implementation

A practical circuit implementation of the DAC utilizing an $R-2R$ ladder is shown in Fig. 9.41. The circuit utilizes BJT's to generate binary-weighted constant currents I_1, I_2, \dots, I_N , which are switched between ground and virtual ground of an output buffer amplifying section (inverter). We shall first show that the currents I_1 to I_N are indeed binary-weighted, with I_1 corresponding to the MSB and I_N corresponding to the LSB of the DAC.

Starting in the two rightmost transistors Q_2 and Q_3 , we see that if they are matched, their emitter currents will be equal and are denoted i_{o1} (Fig.). Transistor Q_1 is included to provide proper termination of the $R-2R$ network. The voltage between the base line of the BJTs and node V will be

$$V_b = V_{be1} + \frac{2i_o}{2R} \quad (9.14)$$

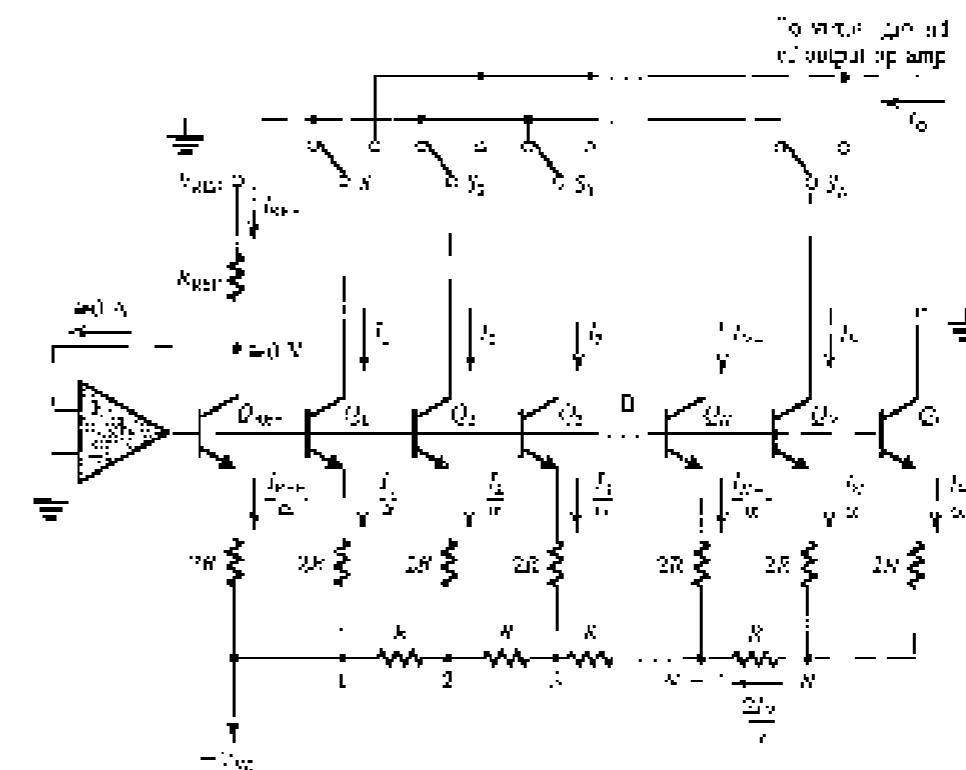


FIGURE 9.41 A practical circuit implementation of a DAC utilizing an $R-2R$ ladder network.

where V_{Q_1} is the base-emitter voltage of Q_1 . Since the current flowing through the resistor R connected to node A is 21 mA, the voltage between Node B and Node (N - 1) will be

$$V_{n+1} = V_n + \frac{f(x_n)}{\mu} [R - V_{\text{avg}}] + \frac{A f_n}{\mu} R$$

Assuming, for the moment, that $V_{B_{Q_1}} = V_{B_{Q_2}}$, we see that a voltage of $14V_{BEQ}$ appears across the resistance $2R$ in the emitter of Q_{N1} . Thus Q_{N1} will have an emitter current of $(2I_{Q1})/2$ and a collector current of $(2I_{Q1})$, twice the current in Q_1 . The two transistors will have equal V_{BE} drops if their junction areas are scaled in the same proportion as their currents, which is usually done in practice.

Proceeding in the manner above we can show that

$$f_1 = 2f_2 = 4f_3 = \cdots = 2^{N-1}f_N \quad (9.1.7)$$

under the assumption that the TBF areas of \mathcal{Q}_1 to \mathcal{Q}_n are scaled in a binary-weighted fast way.

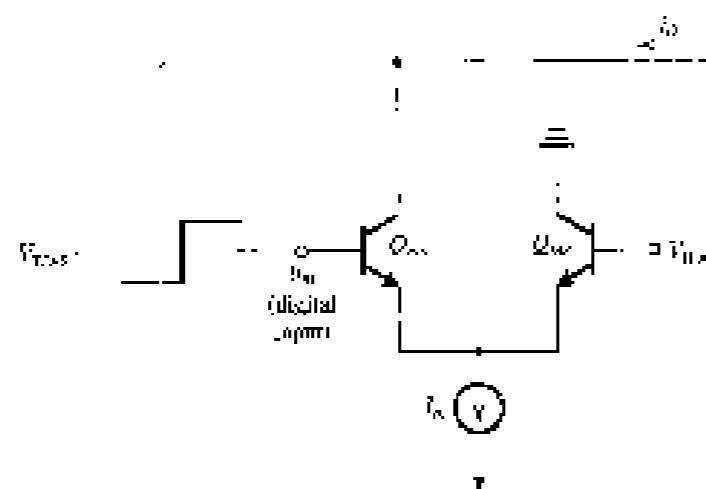
Next, consider op-amp A_1 , which, together with the reference inverter G_{ref} , forms a negative feedback loop. (Convince yourself that the feedback is indeed negative.) A virtual ground appears at the collector of Q_{ref} , forcing it to conduct a collector current $I_{\text{Cref}} = V_{\text{DD}}/\text{R}_\text{ref}$ independent of whatever imperfections Q_{ref} might have. Now, if Q_{ref} and Q_1 are matched, their collector currents will be equal,

$$t = \int_{\mu_0}^{\mu}$$

Thus, the binary-weighted currents are directly added to the reference current, independent of the exact values of V_m and α . Also observe that op amp A_1 supplies the base currents of all the BJTs.

5.8.4 Current Switches

Each of the single-pole double-throw switches in the DAC circuit of Fig. 9.41 can be implemented by a circuit such as that shown in Fig. 9.42 for switch S_{ab} . Here I_o denotes the current flowing in the collector of the nMOS bit transistor. The circuit is a differential pair with the



base of the reference transistor Q_{ref} connected to a suitable dc voltage V_{bias} , and the signal voltage representing the cell bit b_0 applied to the base of the other transistor Q_{ext} . If the voltage representing b_0 is higher than V_{bias} by a few hundred millivolts, Q_{ext} will turn on and Q_{ref} will turn off. The bit current I_b will then flow through Q_{ext} and/or to the output summing line. On the other hand, when b_0 is low, Q_{ext} will be off and I_b will flow through Q_{ref} instead.

The current switch of Fig. 9-42 is symmetrical and features high-speed operation. It suffers, however, from the fact that part of the current I_s flows through the base of Q_{10} , and thus does not appear in the output common-emitter line. More elaborate circuits for current switches can be found in Gehrke (1981). Also, in a BiCMOS technology, the differential-pair transistors Q_1 and Q_2 can be replaced with MOSFETs, thus eliminating the base-current problem.

EXERCISES

922. Which is the maximum positive current passed by the diode in the circuit? (Neglect the diode's own voltage drop.)
 Ans: 0.4A

923. The load current in the bridge rectifier circuit shown is 10 A. The peak-to-peak output voltage across the load is 100 V. If the peak input voltage is 100 V, what is the peak current through the diodes? (Assume the diodes are ideal.)
 Ans: 2.018 A

5.9 A/D CONVERTER CIRCUITS

There exist a number of A/D conversion techniques varying in complexity and speed. We shall discuss four different approaches: (i) a simple, bin-slow, scheme; (ii) a complex (in terms of the amount of circuitry required) but extremely fast method; and, finally, a method specifically suited for MOS implementation.

9.9.1 The Feedback-Type Converter

Figure 9.41 shows a simple A/D converter that employs a comparator, an up/down counter, and a D/A converter. The source amplitude provides no output that assures one of two

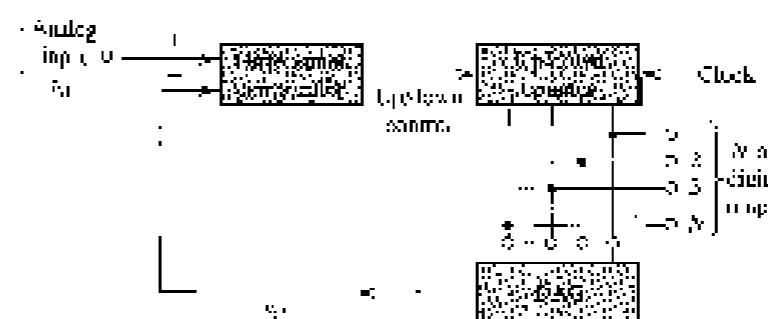


FIGURE 9.42 A series of red wavelengths add together.

discrete voltage, positive when the difference input signal is negative, and negative when the difference input signal is positive. We shall study comparator circuits in Chapter 13. An up-down counter is simply a counter that can count either up or down depending on the binary level applied to its up/down control terminal. Because the A/D converter of Fig. 9.45 employs a DAC in its feedback loop it is usually called a feedback-type A/D converter. It operates as follows: With a 0 count in the counter, the D/A converter output, v_A , will be zero and the output of the comparator will be high, instructing the counter to count the electrons in the up direction. As the count increases, the output of the DAC rises. The process continues until the DAC output reaches the value of the analog input signal, at which point the comparator switches and stops the counter. The counter output will then be the digital equivalent of the input analog voltage.

Operation of the converter of Fig. 9.45 is slow if it starts from zero. This converter, however, makes incremental changes in the input signal quite rapidly.

9.9.2 The Dual-Slope A/D Converter

A very popular high-resolution 12- to 14-bit (but slow) A/D conversion scheme is illustrated in Fig. 9.44. To see how it operates, refer to Fig. 9.44 and assume that the analog input signal, v_A , is negative. Prior to the start of the conversion cycle, switch S_1 is closed, thus discharging capacitor C and setting $v_I = 0$. The conversion cycle begins with opening S_1 and connecting the integrator input through switch S_2 to the analog input signal, since v_A is negative, current $I = v_A/R$ will flow through R in the direction away from the integrator. Thus v_I rises linearly with a slope of $I/C = v_A/RC$, as indicated in Fig. 9.44(b). Simultaneously, the counter is enabled and it counts the pulses from a fixed-frequency clock. This phase of the conversion process continues for a fixed duration T_1 . It ends when the counter has accumulated a fixed count denoted n_{MAX} . Usually, for an N -bit converter, $n_{MAX} = 2^N$. Denoting the peak voltage at the output of the integrator as V_{MAX} , we can write with reference to Fig. 9.44(b)

$$\frac{V_{MAX}}{T_1} = \frac{v_A}{RC} \quad (9.15)$$

At the end of this phase, the counter is reset to zero.

Phase II of the conversion begins at $t = T_1$ by connecting the integrator input through switch S_2 to the positive reference voltage V_{REF} . The current into the integrator reverses direction and is equal to V_{REF}/R . Thus v_I decreases linearly with a slope of (V_{REF}/RC) . Simultaneously, the counter is enabled and it counts the pulses from the fixed-frequency clock. When v_I reaches zero volts, the comparator signal's control logic turns off the counter. Denoting the duration of phase II by T_2 , we can write, by reference to Fig. 9.44(b),

$$\frac{V_{MAX}}{T_2} = \frac{V_{REF}}{RC} \quad (9.16)$$

Dividing (9.15) and (9.16) can be combined to yield

$$T_2 = T_1 \left(\frac{V_{REF}}{V_{MAX}} \right) \quad (9.17)$$

Since the counter reading, n_{MAX} , at the end of T_1 is proportional to T_1 and the reading, n , at the end of T_2 is proportional to T_2 , we have

$$n = n_{MAX} \left(\frac{T_2}{T_1} \right) \quad (9.18)$$

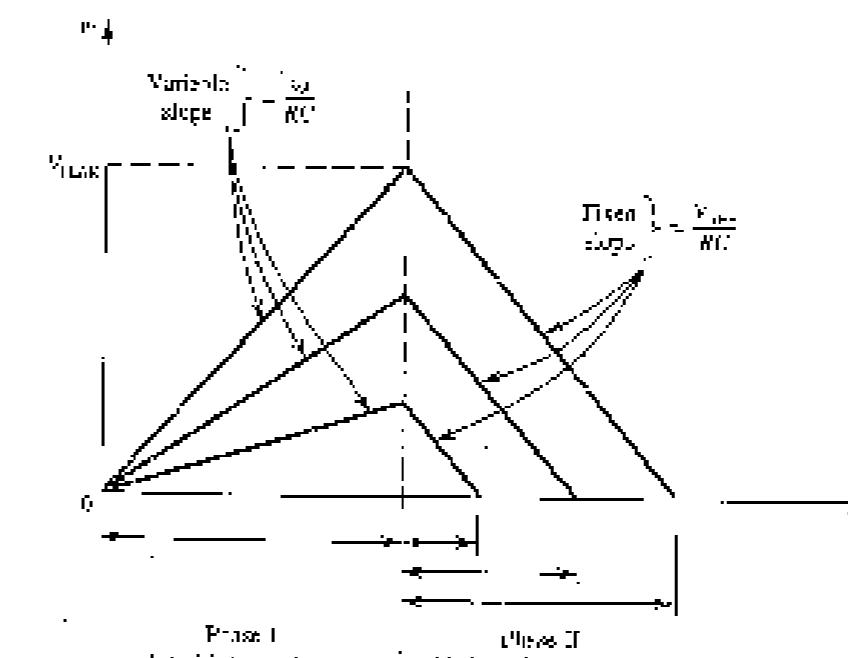
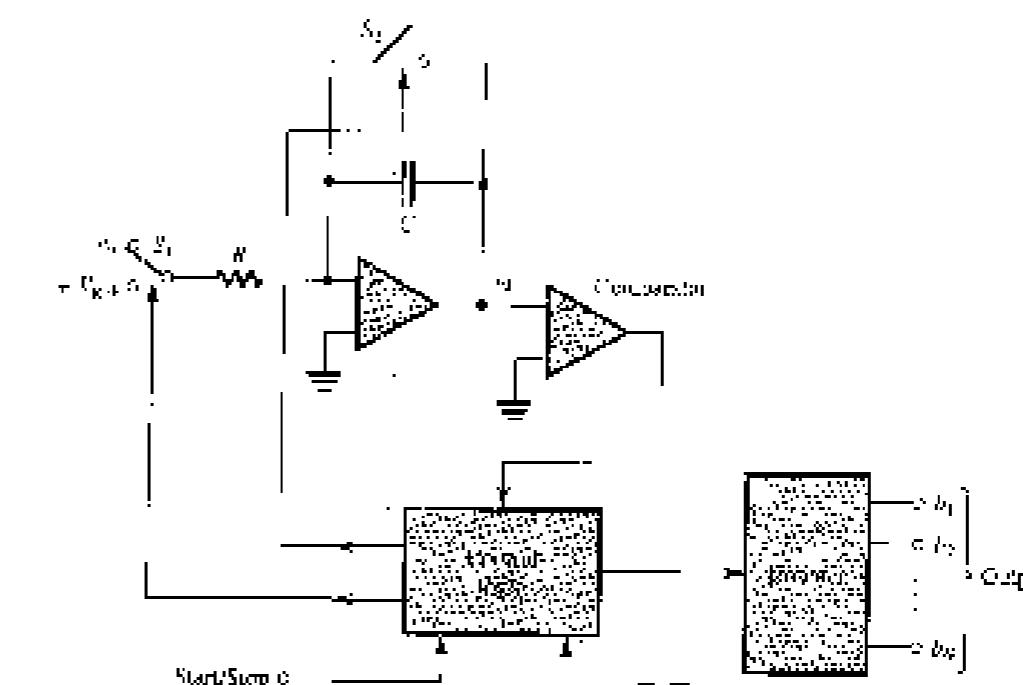


FIGURE 9.44 The dual-slope A/D conversion method. Note that v_A is assumed to be negative.

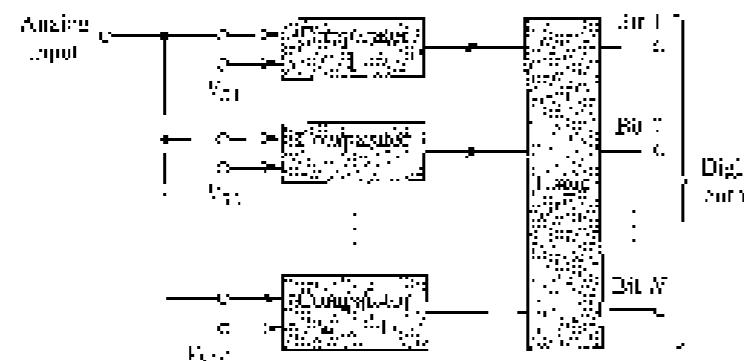


FIGURE 9.45 Parallel dual-slope flash A/D conversion.

This is the extent of the circuit.⁵ At the end of the conversion process is the digitized representation of v_A .

The dual-slope converter features high accuracy, since its performance is independent of the exact values of R and C . There exist many commercial implementations of the dual-slope method, some of which utilize CMOS technology.

9.9.3 The Parallel or Flash Converter

The fastest A/D conversion scheme is the simultaneous, parallel, or flash conversion process illustrated in Fig. 9.15. Conceptually, flash conversion is very simple. It utilizes $2^N - 1$ comparators to compare the input signal level with each of the $2^N - 1$ possible quantization levels. The outputs of the comparators are processed by an encoding logic block to provide the N bits of the output digital word. Note that a complete conversion can be obtained within one clock cycle.

Although flash conversion is very fast, the price paid is a rather complex circuit implementation. Variations on the basic technique have been successfully employed in the design of IC converters.

9.9.4 The Charge-Redistribution Converter

The last A/D conversion technique that we shall discuss is particularly suited for CMOS implementation. As shown in Fig. 9.16, the circuit utilizes a binary weighted capacitor array, a voltage distributor, and analog switches, control logic (not shown in Fig. 9.16), as also required. The circuit shown is for a 5-bit converter; capacitor C_7 serves the purpose of terminating the capacitor array, making the total capacitance equal to the desired value of $2C$.

Operation of the converter can be divided into three distinct phases, as illustrated in Fig. 9.16. In the sample phase (Fig. 9.46a) switch S_2 is closed, thus connecting the top plate of all capacitors to ground and setting v_o to zero. Meanwhile, switch S_3 is connected to the analog input voltage v_A . Thus the voltage v_A appears across the total C parallel of $2C$, resulting in a stored charge of $2Cv_A$. Thus, during this phase, a sample of v_A is taken, and a proportional amount of charge is stored on the capacitor array.

⁵ Note that v_A is not a continuous function of time, as implied incorrectly from Fig. 9.11B. Rather, v_A is a discrete event corresponding to one of the 2^N quantized levels of v_A .

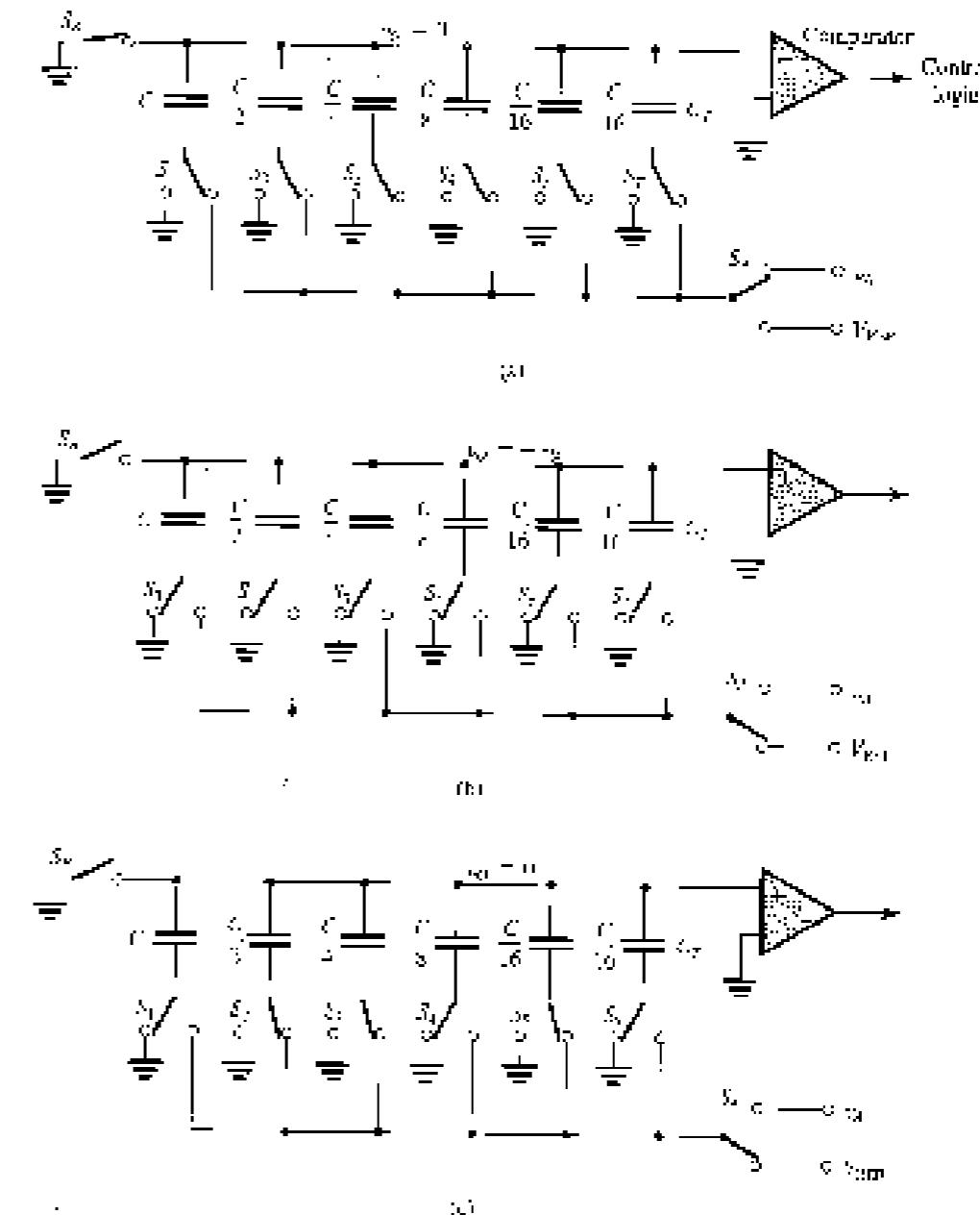


FIGURE 9.46 Charge redistribution A/D converter suitable for CMOS. (a) Sample phase; (b) hold phase; and (c) charge redistribution phase.

During the hold phase (Fig. 9.46b), switch S_2 is opened, and switches S_1 to S_4 , and S_5 , are connected to the ground side. Thus the top plate of the capacitor array is open-circuited while both bottom plates are connected to ground. Since no discharge path has been provided, the capacitor charges must remain constant, with the total equal to $2Cv_A$. It follows that the voltage at the top plate must remain $-v_o$. Finally, note that during the hold phase, S_3 is connected to V_{ref+} in preparation for the charge-redistribution phase.

Next, we consider the operation during the charge-redistribution phase illustrated in Fig. 9.46(c). First, switch S_1 is connected to V_{DD} (through S_2). The circuit then consists of V_{DD} as a series capacitor C_1 , and a total capacitance to ground of value C . This capacitive divider causes a voltage increment of $V_{DD}/2$ to appear on the top plate. Now, if v_1 is greater than $V_{DD}/2$, the net voltage at the top plate will remain negative, which means that S_1 will be left in its new position as we move on to switch S_2 . If, on the other hand, v_1 was smaller than $V_{DD}/2$, then the net voltage at the top plate would become positive. The comparator will detect this situation and signal the control logic to return S_1 to its ground position and then to move on to S_2 .

Next, switch S_2 is connected to V_{REF} , which causes a voltage increment of $V_{DD}/4$ to appear on the top plate. If the resulting voltage is still negative, S_2 is left in its new position; otherwise, S_2 is returned to its ground position. We then move on to switch S_3 , and so on until all the bit switches S_1 to S_8 have been tried.

It can be seen that during the charge-redistribution phase the voltage on the top plate will be reduced incrementally to zero. The connection of the bit switches at the conclusion of this phase gives the output digital word; a switch connected to ground indicates a 0 value for the corresponding bit, whereas connecting to V_{REF} indicates a 1. The particular switch configuration depicted in Fig. 9.46(c) is for $B = 01101$. Observe that at the end of the conversion process, all the charge is stored in the capacitors corresponding to 1 bits; the capacitors of the 0 bits have been discharged.

The accuracy of this A/D conversion method is independent of the value of stray capacitances from the bottom plate of the capacitors to ground. This is because the bottom plates are connected either to ground or to V_{REF} ; thus the charge on the stray capacitances will not flow into the capacitor array. Also, because both the initial and the final voltages on the top plate are zero, the circuit is also insensitive to the stray capacitances between the top plates and ground.⁶ The insensitivity to stray capacitances makes the charge-redistribution technique a reasonably accurate method capable of implementing A/D converters with as many as 10 bits.

EXERCISES

- 9.35 Consider the 5-bit charge-redistribution converter in Fig. 9.47 with $V_{DD} = 5$ V. What is the voltage at the output of the first stage of the converter? Assume that the input voltage is 2.5 V, which will be converted into a 5-bit digital output of 01101.
- 9.36 Express the error in ppm due to the mismatch of the two capacitors in the charge-redistribution converter of Fig. 9.47.
- 9.37 Express the error in ppm due to the mismatch of the two capacitors in the charge-redistribution converter of Fig. 9.47.
- 9.38 Express the error in ppm due to the mismatch of the two capacitors in the charge-redistribution converter of Fig. 9.47.

9.10 SPICE SIMULATION EXAMPLE

We conclude this chapter with an example to illustrate the use of SPICE in the simulation of the two-stage CMOS op amp.

⁶ More precisely, the total voltage can change from $-V_{DD}$ by as much as the analog equivalent of one LSB. Thus, the insensitivity to top plate capacitance is not complete.

A TWO-STAGE CMOS OP AMP

In this example, we will use PSpice to aid in designing the frequency compensation of the two-stage CMOS circuit whose layout schematic is shown in Fig. 9.47. PSpice will then be employed to determine the frequency response and the slew rate of the op amp. We will assume a 0.5- μ m n-well CMOS technology for the NMOS/PMOS and use the ATPCB level 1 model parameters listed in Table 4.8. Observe that to eliminate the body effect and minimize the matching between M_1 and M_2 , the source terminals of the input NMOS transistors M_1 and M_2 are connected to their n well.

The op-amp circuit in Fig. 9.47 is designed using a reference current $I_{ref} = 60\ \mu$ A, a supply voltage $V_{DD} = 2.5$ V, and a load capacitor $C_L = 1\ pF$. Unit-size transistors with $W/L = 1.25\ \mu$ m / 0.6 μ m are used for both the NMOS and PMOS devices. The transistors are sized for an overdrive voltage $V_{GS} = 0.5$ V. The corresponding multiplication factors are given in Fig. 9.47.

In PSpice, the common-mode input voltage V_{CM} of the op-amp circuit is set to $V_{DD}/2 = 1.25$ V. A bias-point simulator is performed to determine the dc operating point. Using the values found in the simulator script file for the small-signal parameters of the MOSFETs, we obtain⁷

$$\begin{aligned}G_{v1} &= 0.313\text{ mA/V} \\G_{v2} &= 0.030\text{ mA/V} \\C_1 &= 26.5\text{ fF} \\C_2 &= 1.04\text{ pF}\end{aligned}$$

using Eqs. (9.7), (9.14), (9.24), and (9.25), respectively. Then, using Eq. (9.27), the frequency of the second noninverting pole can be found as

$$f_{p2} = \frac{G_{v2}}{2\pi C_2} = 57.2\text{ MHz}$$

In order to place the transmission zero, given by Eq. (9.37), at infinite frequency, we select

$$R = \frac{1}{G_{v2}} = 1.52\text{ k}\Omega$$

Now, using Eq. (9.56), the phase margin of the op-amp can be expressed as

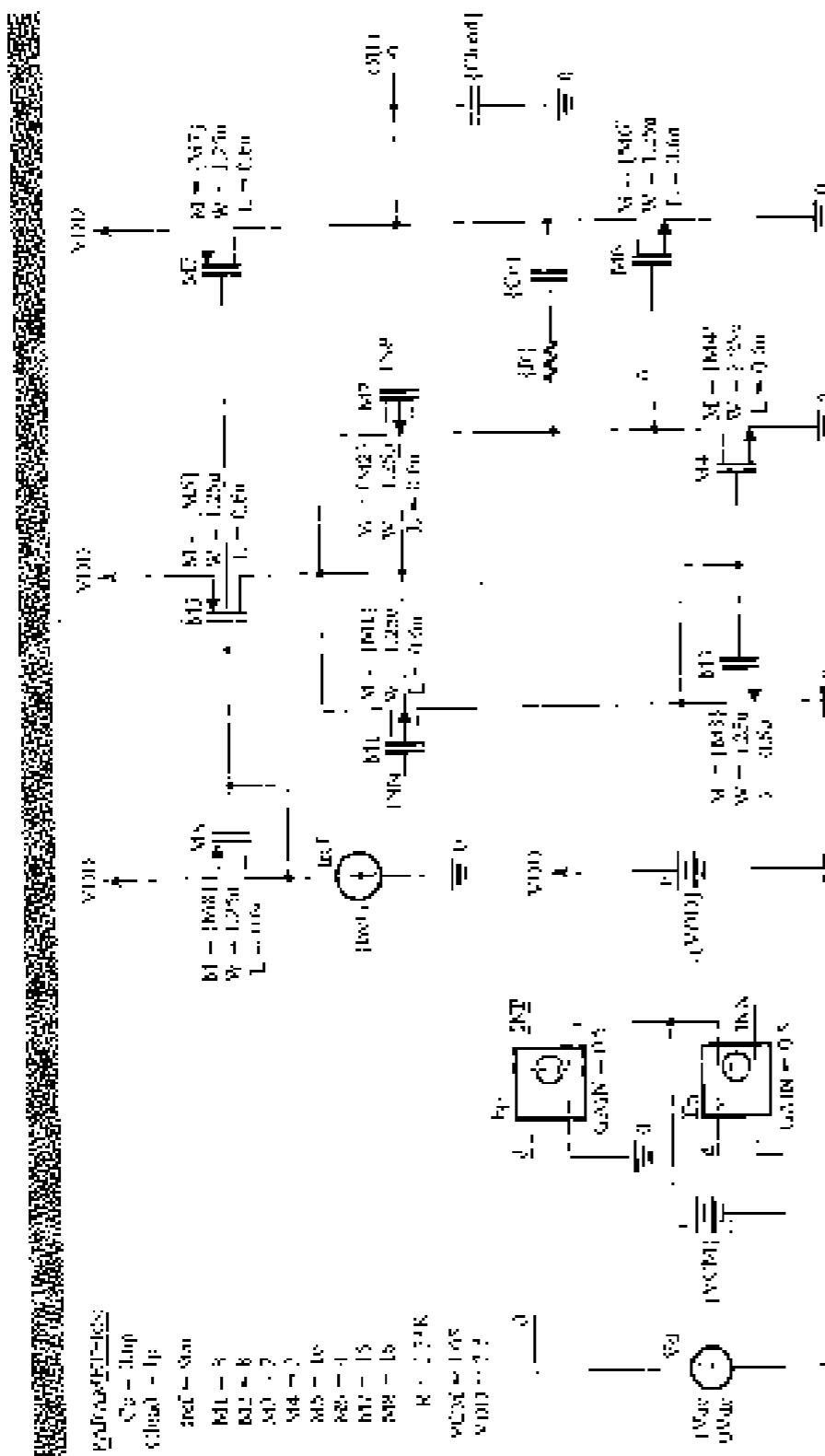
$$\text{PM} = 90^\circ - \tan^{-1}\left(\frac{f_p}{f_{p2}}\right) \quad (9.119)$$

where f_p is the unity-gain frequency, given in Eq. (9.30).

$$f_p = \frac{C_1}{2\pi G_{v1}} \quad (9.120)$$

Using Eqs. (9.119) and (9.120) we determine that compensation capacitors of $C_1 = 0.08\text{ pF}$ and $C_2 = 2\text{ pF}$ are required to achieve phase margins of $\text{PM} = 55^\circ$ and $\text{PM} = 75^\circ$, respectively.

⁷ Recall that G_{v1} and G_{v2} are the analog characters of, respectively, the first and second stages of the op-amp. Capacitors C_1 and C_2 represent the load capacitance introduced at the output node, respectively, the first and second stage of the op-amp.



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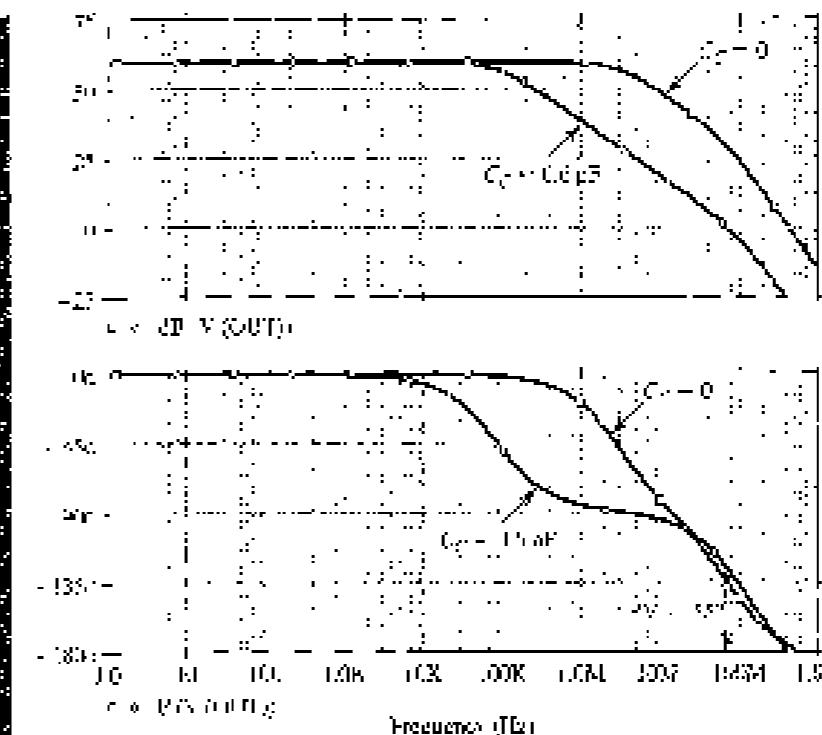


FIGURE 9.46 Magnitude and phase response of the epicyclic system in Fig. 9.45, $\omega = 1.5 \times \omega_0$, $C_0 = 0$.

Near-analysesis simulation is performed in PSpice to compute the frequency response of the op-amp and to verify the foregoing design values. It was found that with $V = 1.53$ V, we need $C_{\text{in}} = 0.6 \text{ pF}$ and $C_{\text{out}} = 1.6 \text{ pF}$ to set $\text{PM} = 55^\circ$ and $\text{PM} = 75^\circ$, respectively. We note that these are the values recommended by hand analysis. The corresponding frequency responses are shown in Figs. 9.48 and 9.49. For comparison, we also show the frequency response of the uncompensated op-amp ($C_{\text{in}} = 0$). Observe that the unity-gain frequency falls from 20.2 MHz to 26.1 MHz as C_{in} increases to improve PM (as anticipated from Fig. 9.12(b)).

Rather than increasing the compensation capacitor C_2 , the value of the active resistor R can be increased to improve the phase margin PM. For a given C_2 , increasing R gives $1/G_{d1}$ places the transient zero from a negative real-axis location (Eq. 8.37), where the phase it introduces only to the phase margin. Thus, PM can be improved without affecting f_T . To verify this point, we set C_2 to 10 pF and simulate the frequency response Bode for the cases of $R = 5.1 \text{ k}\Omega$ and $R = 5.2 \text{ k}\Omega$. The corresponding frequency response is plotted in Fig. 9.50. Observe how f_T is approximately independent of R . However, by increasing R , PM is improved from 55° to 75°.

However, the PVF is desirable because it reduces the overshoot in the step response of the system. To verify this claim, we simulate in Pôpice the step response of the system for $P_M = 5.5$ and $P_M = 25$. To do that, we consider the system in a unity gain configuration, apply a small (1-mV) sinusoidal signal at the input, with very short ($\sim 0.1\text{ ms}$) and 100 times to simulate a step input, perform a transient-analysis simulation, and plot the output voltage as shown in Fig. 9.5. Observe that the overshoot in the step response drops from 15% to 1.4% when the phase margin is increased from 55° to 90°.

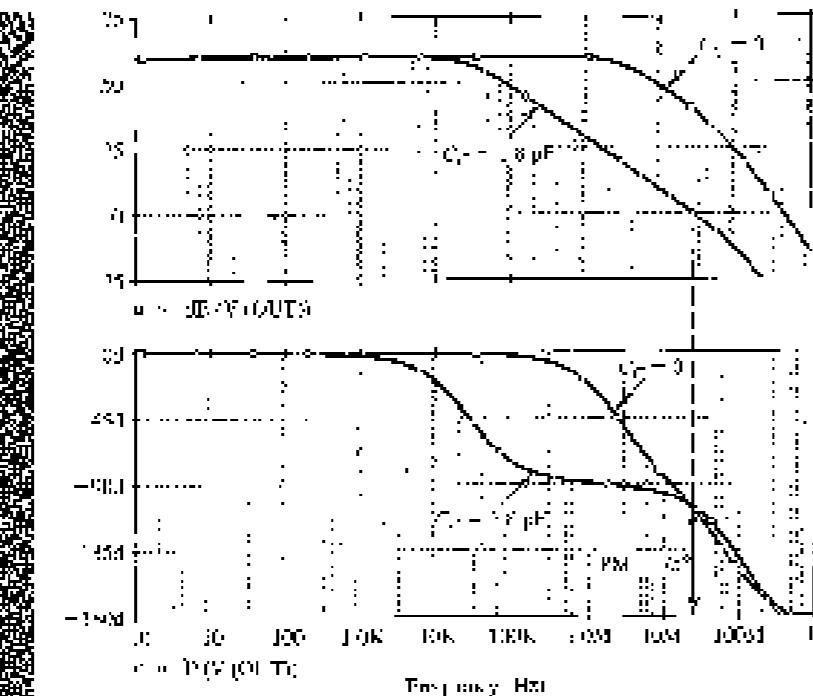


FIGURE 9.49 Magnitude and phase response of the op-amp circuit in Fig. 9.13; $R = 1.53\text{ k}\Omega$, $C_f = 0\text{ pF}$ (open-loop configuration), and $C_f = 1.8\text{ pF}$ ($\text{PM} = 75^\circ$).

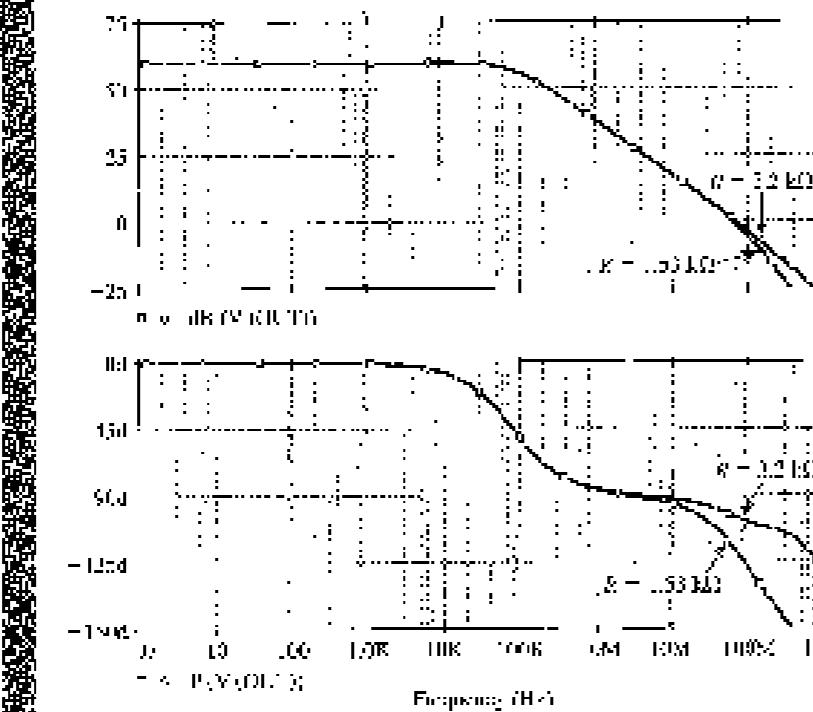


FIGURE 9.50 Magnitude and phase response of the op-amp circuit in Fig. 9.13; $C_f = 0.6\text{ pF}$, $R = 1.5\text{ k}\Omega$ ($\text{PM} = 75^\circ$), and $K = 1.2\text{ k}\Omega$ ($\text{PM} = 75^\circ$).

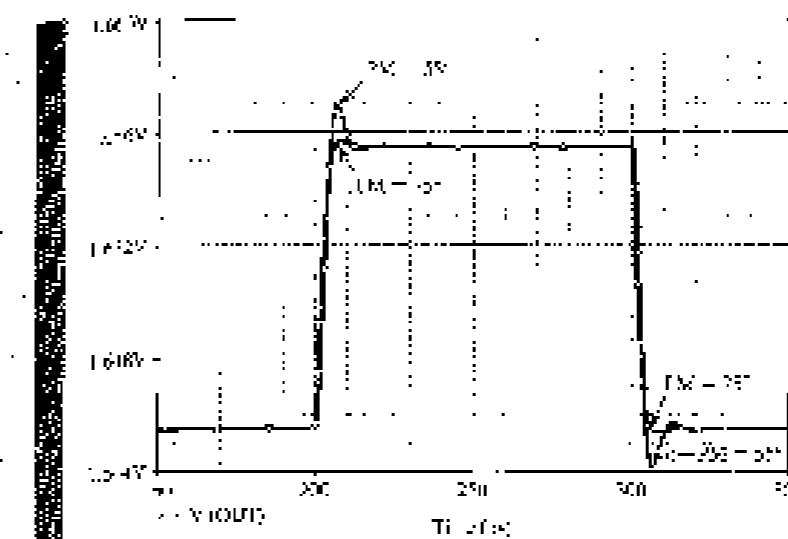


FIGURE 9.51 Small-signal step response ($V_{IN} = 0.4\text{ mV}$ step input) of the op-amp circuit in Fig. 9.13 (open-loop in unity-gain configuration); $C_f = 0.6\text{ pF}$, $R = 1.53\text{ k}\Omega$, and $\text{PM} = 75^\circ$; $C_f = 1.8\text{ pF}$, $R = 3.7\text{ k}\Omega$.

We conclude this example by computing ΔR , the slew rate of the op-amp. From Eq. (9.40),

$$\Delta R = \Delta V / \Delta t = \frac{C_f}{R} V_{DD} = \frac{C_f}{R} V_{DD} = 166.7\text{ V/}\mu\text{s}$$

where $C_f = 0.6\text{ pF}$. Next, to determine ΔR using PSpice (see Example 9.9), we again connect the op-amp in a unity-gain configuration, and perform a transient-analysis simulation. However, we now apply a large pulse signal (3.3 V) to the input to cause slew-rate limiting at the output. The corresponding output voltage waveform is plotted in Fig. 9.52. The slope of the slew-rate-limited output waveform corresponds to the slew rate of the op-amp, and is found to be $\Delta R = 50\text{ V/}\mu\text{s}$ and $60\text{ V/}\mu\text{s}$ for the negative- and positive-going output, respectively. These results, with the principal

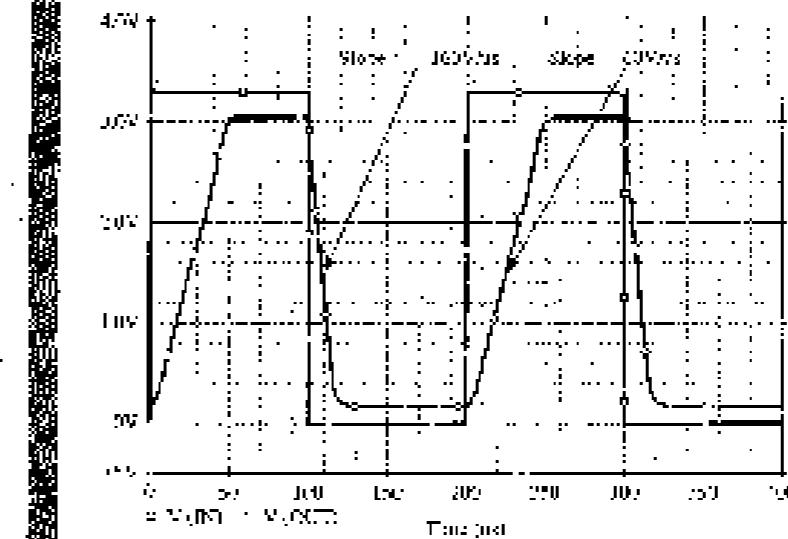


FIGURE 9.52 Large-signal step response ($V_{IN} = 0.4\text{ mV}$ step input) of the op-amp circuit in Fig. 9.13 (open-loop in unity-gain configuration). The slope of the rising and falling edges of the output waveform corresponds to the slew rate of the op-amp.



values of β_2 of the two diodes, differ from those predicted by the small-signal model for the slew-rate limiting of the two-stage op-amp circuit (Section 9.1.5). The difference can perhaps be ascribed to a result of transistor M_3 entering the triode region and its output current (which is summed through C_3) being correspondingly reduced. Of course, the availability of PSpice should enable the reader to explore this point further.

SUMMARY

- Most CMOS op-amps are designed to operate in a V_{DD} circuit, thus they are required to drive only small currents (I_{DS}). Therefore, most CMOS op-amps have low output transconductance stages.
- There are basically two approaches in the design of CMOS op-amps: a two-stage configuration, and a single-stage topology utilizing the folded-cascode circuit.
- In the two-stage CMOS op-amp, complementary equal gains are realized at the two stages.
- The intrinsic mismatch ΔV , together with the low transconductance of the input stage, result in a larger output voltage for CMOS op-amps than for bipolar units.
- Miller compensation is employed in the two-stage CMOS op-amp, but a series resistor is required to place the compensation node either r_{in} or on the negative feedback.
- CMOS op-amps have higher slew rates than their bipolar counterparts with comparable β values.
- Use of the cascode configuration increases the gain of a CMOS op-amp by about one orders of magnitude, but it also provides a single-stage op-amp.
- The dominant pole of the folded-cascode op-amp is determined by C_1 , i.e., capacitance at the output node. C_1 increasing C_1 improves the phase margin at the expense of reducing the bandwidth.
- By using two complementary input differential pairs in parallel, the input common-mode voltage can be extended to equal the entire power-supply voltage, providing a wider common-mode operation at the input.
- The common-mode range of the folded-cascode op-amp can be extended by using a wide-swing current mirror at place of the second cascode.
- The internal operation of the CMOS op-amps follows many of the digital techniques employed in logic or analog integrated circuits.
- The 1/41 common-mode of a bipolar differential stage, a high-gain single-ended second stage, and a unity-gain third stage. This three-stage topology is modern BJT op-amps and is known as the two-stage topology (not covering 20).
- Output stage, it is the same structure used in the two-stage CMOS op-amp (Section 9.1).
- To obtain low input offset voltage and current, and high CMRR, the 24-V CMOS op-amp is designed to be perfectly balanced. The CMRR is generated by common-mode feedback, which also stabilizes the oscillating point.
- Load-balancing consists of two input cancellation, the input stage of the 24-V is operated for very low drain load.
- In the 741, compensation for nonlinearity is accomplished by turning on a cascode that takes away part of the bias current drive of the output inverter.
- The use of Miller frequency compensation in the 741 circuit enables locating the dominant pole at a very low frequency, while employing extremely small compensating capacitance.
- Two-stage op-amps can be realized as a transconductance amplifier feeding an ideal integrator with C_1 as the integrating capacitor.
- The slew rate of a two-stage op-amp is determined by the two-stage bias current and the frequency compensation capacitors.
- AD81 and AD82 are voltage-controlled-current-injection op-amps (CCOs).
- A DAC consists of (i) generating the reference current, (ii) a circuit that designs unity weight $w_{j,k}$ as the ratio of the reference current, (iii) switches that make the sum of the weights of the output, (iv) a feed-back loop to provide constant binary-weighted current to an output summing node, and (v) an op-amp that converts the current to an output voltage. The circuit of Fig. 9.1 can be implemented by either a binary-weighted resistor network or an $\text{R}-\text{2R}$ ladder.
- Two simple but slow implementations of the ADC are the feed-back-type converter (Fig. 9.42) and the dual-slope converter (Fig. 9.44).
- The fastest available ADC implementation is the parallel flash converter (Fig. 9.45).
- The charge-redistribution method (Fig. 9.46) utilizes switched-capacitor techniques and is particularly suited for the implementation of ADCs in CMOS technology.



PROBLEMS

SECTION 9.1: THE TWO-STAGE CMOS OP AMP

- P9.1** A particular design of the two-stage CMOS operational amplifier of Fig. 9.1 utilizes 25-NM process technology. All transistors are operated at excessive voltages of 0.5-V magnitude. The process technology provides devices with $|V_{GS}| = |V_{DS}| = 0.7$ V. Find the input common-mode range, and the range of β for α_1 .

- P9.2** The CMOS op-amp of Fig. 9.1 is fabricated in a process for which $|V_{GS}| = 2.5$ V/cm and $|V_{DS}| = 2.0$ V/cm. Find β_1 , β_2 , and β_3 if all devices are 0.5- μm long and are operated at equal overdrive voltages of 1.0-V magnitude. Also, determine the dominant output resistance obtained when the second stage is biased at 0.4 mA. What do you expect the output resistance of a unity-gain voltage amplifier to be, using this op-amp?

- P9.3** The CMOS op-amp of Fig. 9.1 is fabricated in a process for which $|V_{GS}|$ for all devices is 1.0 V/cm. If all transistors have $L = 1$ μm and are operated at equal overdrive voltages, find the magnitude of the dominant voltage gain for a stable open-loop gain of 2500 V/V.

- P9.4** This problem is identical to Problem 9.9.

- Consider the circuit in Fig. 9.1 with the device geometries shown in the bottom of this page.

- Let $\beta_{1,2} = 275$ μA , $|V_{GS}|$ for all devices = 0.75 V, $\beta_3 C_{12} = 130$ $\mu\text{A}/\text{V}^2$, $\beta_3 C_1 = 80$ $\mu\text{A}/\text{V}^2$, $|V_{GS}|$ for all devices = 0.7 V, $V_{DD} = V_S = 1.5$ V. Determine the width of O_3 , W_3 , that will ensure that the op-amp will not have a systematic offset voltage. Then, for 10 devices, use $\beta_{1,2} = |V_{GS}| / |V_{DS}| \beta_1$, $\beta_3 = \beta_3$. Provide your results in a table. Also, find α_1 , α_2 , α_3 , the open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_D on the bias currents.

- P9.5** A particular implementation of the CMOS amplifier of Figs. 9.1 and 9.2 provides $\beta_1 = 0.3$ mA/V, $\beta_{1,2} = 0.6$ mA/V, $\beta_3 = \beta_4 = 2.22$ mA, $R_{12} = R_2 = 111$ $\text{k}\Omega$, and $C_1 = 1$ pF.

- (a) Find the frequency of the second pole, f_2 .
(b) Find the value of the resistance R which when placed in series with C_1 causes the dominant pole to be located at $f = 10$ Hz.

Transistor:	$\beta_1 = 0.3$	$\beta_{1,2} = 0.6$	$\beta_3 = \beta_4 = 2.22$	$\beta_{1,2} = 0.6$	$\beta_3 = \beta_4 = 2.22$
Process:	400-S	500-S	100-S	100-S	500-S

- (c) With R in place, again, find the value of C_1 that results in the highest possible value of β , while maintaining a phase margin of 60°. What value of β is real, and what is the corresponding frequency of the dominant pole?

- (d) For a β value should C_1 be changed to double the value of C_1 ? At the new value of β , what is the phase margin provided by the second pole? To reduce the excess phase and to increase the β value resulting, what value should R be changed to?

- P9.6** A two-stage CMOS op-amp similar to that in Fig. 9.1 is found to have a capacitance between the output node and ground of 1 pF. If it is desired to have a unity-gain bandwidth of 100 MHz with a phase margin of 72° what value C_1 be set to? Assume that a resistance R is connected in series with the first-stage bias resistor, capacitor C_1 is adjusted to place the transmission zero at infinity. What value should R have? If the first stage is operated at $|V_{GS}| = 0.2$ V, what is the value of slew rate obtained? If the first stage bias current is $I = 200$ μA , what is the required value of C_1 ?

- P9.7** A CMOS op-amp with the topology shown in Fig. 9.1 but with a resistor R connected in series with C_1 , is designed to produce $\beta_1 = 1$ mA/V and $C_1 = 2$ nA/V.

- (a) Find the value of C_1 that results in $f_2 = 100$ Hz.
(b) For $R = 10$ k Ω , what is the maximum allowed value of C_1 before a phase margin of at least 60° is obtained?

- P9.8** A two-stage UV/VS op-amp consisting of that in Fig. 9.1 is found to have a slew rate of 0.6 V/ μs and a unity-gain bandwidth of 150 MHz.

- (a) For what value of the feedback voltage at which the two-stage common mode occurs?
(b) If the reference bias current, $I = 100$ μA , what value of C_1 must be used?
(c) For a process for which $\beta_{1,2} = 50$ $\mu\text{A}/\text{V}^2$, what will the open-loop gain for C_1 and C_2 ?

- P9.9** Sketch the circuit of a two-stage CMOS amplifier having the same bias as $V_{DD} = 1$ V, but using NMOS transistors. Let $\beta = 1$ for the input stage, $\beta_1 = 1$ μA .

SECTION 9.2: THE FOLDED-CASCODE OP AMP

- P9.10** The circuit of Fig. 9.3 utilizes ±1.5-V power supplies and the power dissipation is to be limited to 1 mW.

the values i_{Q_1} and i_1 . To avoid turning off the current mirror during slewing, select i_2 to be 20% larger than i_1 .

9.11 For the folded-cascode op-amp utilizing power-supply rails of ± 1.65 V, find the values of V_{DDC} , V_{PSS} , and V_{NSS} to maximize the allowable range of V_{IN} , and i_1 . Assume that all transistors are operated at equal overdrive voltages of 0.2 V. Assume $|V_t|$ for all devices is 0.5 V. Specify the maximum transconductance and i_1 .

9.12 For the folded-cascode op-amp circuit of Figs. 9.6 and 9.9 with bias currents $i_1 = 25 \mu\text{A}$ and $i_2 = 150 \mu\text{A}$, and with all transistors operated at overdrive voltage of 0.2 V, find the i_1 - i_2 ratios for all devices. Assume that the transconductance is characterized by $k'_t = 250 \mu\text{A/V}^2$ and $k''_t = 60 \mu\text{A/V}^2$.

9.13 Consider the folded-cascode op-amp when loaded with a 10-pF capacitive load. What should the bias current i_1 be to obtain a slew rate of at least $1 \text{ V/}\mu\text{s}$? If the input-stage transistors are operated at overdrive voltage of 0.2 V, what is the unity-gain bandwidth, and for $f_T = 10.2$ V, what is the phase margin obtained? If it is required to have a phase margin of 75°, what must i_1 be reduced to? By how much should i_2 be increased? What is the new value of Δf_T ?

9.14 Consider a design of the cascode op-amp of Fig. 9.9 in which $i_1 = 25 \mu\text{A}$ and $i_2 = 150 \mu\text{A}$. Assume that all transistors are operated at $|V_{DD}| = 12$ V and that the tail-currents, $i_3 = 10 \mu\text{A}$. Find k'_t , k''_t , and A_{vD} . Assume that the op-amp is connected in the feedback configuration shown in Fig. 9.1, and the voltage gain and output resistance of the closed-loop amplifier.

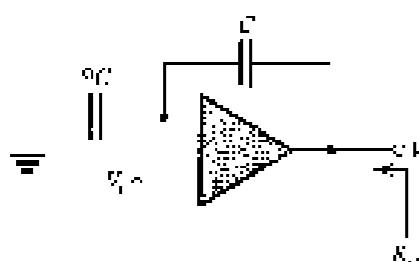


FIGURE P9.14

9.15 For the circuit in Fig. 9.11, assume that all transistors are operating at equal overdrive voltages of 0.2-V magnitude and have $|V_t| = 0.5$ V and that $V_{DD} = V_{SS} = 1.65$ V. Find (a) the range over which the NMOS input stage operates, (b) the range over which the PMOS input stage operates, (c) the range over which both operate (the overdrive voltage and (d) the input common-mode range.

9.16 A particular design of the wide-swing current mirror of Fig. 9.12(b) uses devices having $W/L = 25$ and $|V_t| = 0.5$ V, and $i_{Q_1} = 100 \mu\text{A}$ give the voltages that prevent saturation or breakdown of Q_1 and Q_2 . What differential input voltage would result in the breakdown of the input-stage transistors?

9.17 It is required to design the folded-cascode circuit of Fig. 9.9 to provide voltage gain of 80 dB and a unity-gain frequency of 10 MHz when $C_o = 10 \text{ pF}$. Design for $i_1 = i_2$ and assume all devices are operated at the same $|V_{DD}|$. Utilize transistors with 1- μm channel length for which $|V_t|$ is specified to be 0.2 V. Find the required overdrive voltages and bias currents. What slew rate is achieved? Also, if $k'_t = 2.5 \text{ mA/V}^2$ and $k''_t = 200 \mu\text{A/V}^2$, specify the input i_1 width of each of the two transistors.

9.18 Sketch the circuit that is complementary to that in Fig. 9.6, that is, one that uses an input-referred differential pair.

9.19 For the folded-cascode circuit of Fig. 9.8, let the i_1 - i_2 capacitance to ground, at each of the source nodes of Q_1 and Q_2 , be denoted C_0 . Show that the pole due to C_0 at the interface between the first and second stages has a frequency of $f_p = g_{PD}/2\pi C_0$. Note, if this is the only nondominant pole, what is the largest value that C_0 can be expected as a fraction of C_D while maintaining a phase margin of 75° is achieved? Assume that all transistors are operated at the same bias current and overdrive voltage.

SECTION 9.3: THE 741 OP-AMP CIRCUIT

9.20 In the 741 op-amp circuit of Fig. 9.13, Q_1 , Q_2 , Q_3 , and Q_4 are biased at collector currents of $6.5 \mu\text{A}$; Q_5 is biased at a collector current of $16.2 \mu\text{A}$ and Q_6 is biased at a collector current of $550 \mu\text{A}$. All these devices are of the "standard-gate" type, having $k'_t = 10^{-4} \text{ A}$, $0 = 200$, and $|V_t| = 125$ V. For each of these transistors, find V_{DS} , k''_t , i_{SD} , and i_{DS} . Develop your results in table form. (Note that these parameter values are utilized in the text in the analysis of the 741 circuit.)

9.21 For the circuit in Fig. 9.10 and the result verified in the associated Exercise, find i_1 for the case in which $i_{Q_1} = 3 \times 10^{14} \text{ A}$, $i_{Q_2} = 5 \times 10^{14} \text{ A}$, and $i_{Q_3} = i_{Q_4} = 10^{14} \text{ A}$ and for which a bias current $i_2 = 54 \mu\text{A}$ is required.

9.22 Transistor Q_1 in the circuit of Fig. 9.13 consists, in effect, of two transistors whose emitter-base junctions are connected in parallel and for which $i_{Q_1} = 0.25 \times 10^{14} \text{ A}$, $i_{SD} = 0.75 \times 10^{14} \text{ A}$, $\beta = 50$, and $|V_t| = 50$ V. For operational & total collector current of 0.79 mA, find values for the parameters V_{DD} , R_f , r_s , r_o , and i_1 for the A and B modes.

9.23 In the circuit of Fig. 9.11, Q_1 and Q_2 exhibit emitter-base breakdown at V_V , while for Q_3 and Q_4 , such a breakdown occurs at about $2(V_V - 0.5)$ V. What differential input voltage would result in the breakdown of the input-stage transistors?

9.24 Figure P9.24 shows the CMOS version of the circuit in Fig. 9.13. Find i_1 , i_2 , and i_3 in terms of i_{Q_1} , i_{Q_2} , i_{Q_3} , and i_{Q_4} of the four transistors, assuming the threshold voltages of all devices to be zero in magnitude. Note that $V_{DD} = 5 \text{ V}$, $V_{SS} = 0$, and $|V_t| = 125$ V. Assume that $i_{Q_1} = i_{Q_2} = 10 \mu\text{A}$, the bias required value of i_1 to yield a bias current of i_{Q_3} in Q_3 and i_2 of 1.6 mA .

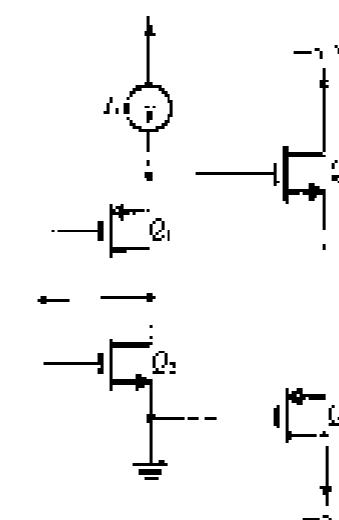


FIGURE P9.24

SECTION 9.4: DC ANALYSIS OF THE 741

9.25 For the 741 circuit, compute the input-referred current $i_{R_{in}}$ in the event that ± 5 -V supplies are used. Find a value for R_f assuming that, for the 70% fT 's involved, $i_1 = 10^{-4} \text{ A}$. What value of R_b would be necessary to make the source bias a collector -5 V supplies as exists for ± 15 V in the original circuit?

9.26 In the 741 circuit, consider the common-mode feedback loop comprising transistors Q_1 , Q_2 , Q_3 , Q_4 , Q_5 , and Q_6 . We wish to find the loop gain $|A_{cm}|$. This can be conveniently done by breaking the loop between the common-emitter connection of Q_1 and Q_2 , and the single-connected transistor Q_5 . Apply a test current signal I_{cm} to Q_1 , and find the related current signal I_{cm} in the common-emitter connection of Q_1 and Q_2 . Thus determine the loop gain. Assume that Q_1 and Q_2 act as ideal current sources; i.e., Q_1 and Q_2 have $\beta = \infty$; find the amount of common-mode feedback in the loop.

9.27 Design the Widlar current source of Fig. 9.13 so as to generate a current $i_{Q_1} = 25 \mu\text{A}$ given that $i_{Q_2} = 0.5 \text{ mA}$. If the characteristics $i_1 = 10^{14} \text{ A}$, and $|V_t| = 125$ V, assume i_2 is high.

9.28 Consider the dc analysis of the 741 input stage shown in Fig. 9.16. For what value of i_1 do the currents in Q_1 & Q_2 differ from their value of $i_{Q_1,2}$ by 10%?

9.29 Consider the dc analysis of the 741 input stage shown in Fig. 9.16 for the situation in which $i_3 = 0.5 \mu\text{A}$. Recall that $i_1 = 10 \mu\text{A}$, $i_2 = 100 \mu\text{A}$, and $i_{Q_1,2} = 10 \mu\text{A}$. Redesign the Widlar source to establish $i_1 = i_2 = 2.5 \mu\text{A}$.

9.30 In the op-amp circuit shown in Fig. 9.17 with the bias and component values given in the text for the 741 circuit, what does the current in Q_1 become if i_1 is altered?

9.31 It is required to redesign the circuit of Fig. 9.13 by selecting a new value for R_f so that when the bias currents are not negligible, the collector currents of Q_1 , Q_2 , and Q_3 all become ∞ , assuming that the input current, $i_1 = 9.4 \mu\text{A}$. Find the new value of R_f & the three currents. Recall that $|V_t| = 20$ V.

9.32 Consider the $i_{R_{in}}$ circuit of the 741 op-amp of Fig. 9.16 when the collector current of Q_3 is about $15 \mu\text{A}$. If β of Q_1 is 150 and that of Q_2 is 200, find the input bias current, i_1 , and the input offset current, $i_{R_{in}}$, of the op-amp.

9.33 For a particular application, consideration is being given to selecting ± 10 -V dc bias and offset currents limited to $40 \mu\text{A}$ and $4 \mu\text{A}$, respectively. Assume all other aspects of the 741 circuit. If the $i_{R_{in}}$ is to be minimum, β of Q_1 what $|V_t|$ variation are justified?

9.34 A manufacturing problem in a 741 op-amp is to find the current transfer ratio of the output current that loads the input stage to become 0.9 A/mA. For input devices (Q_1 – Q_4) approximately matched and with high β , and normally biased at $9.5 \mu\text{A}$, what is our offset voltage result?

9.35 Consider the $i_{R_{in}}$ of the second stage of the 741. What value of R_f would be needed to reduce $i_{R_{in}}$ to $9.5 \mu\text{A}$?

9.36 Consider the 741 output stage shown in Fig. 9.18, in which R_{11} is adjustable to make $i_{Q_1} = i_{Q_2}$. What is the new value of R_{11} ? With values of $i_{Q_1,2}$, the $i_{R_{in}}$ is?

9.37 An alternative approach to providing the voltage drop needed to bias the output transistors is the μ -V_D-multiplier circuit shown in Fig. 9.37. Design the circuit to provide a terminal voltage of 1.15 V (the same as in the 741 circuit). Base your design on $i_{Q_1,2}$, the current flowing through R_f , and assume that $i_1 = 10^{-4} \text{ A}$ and $\beta = 200$. What is the incremental

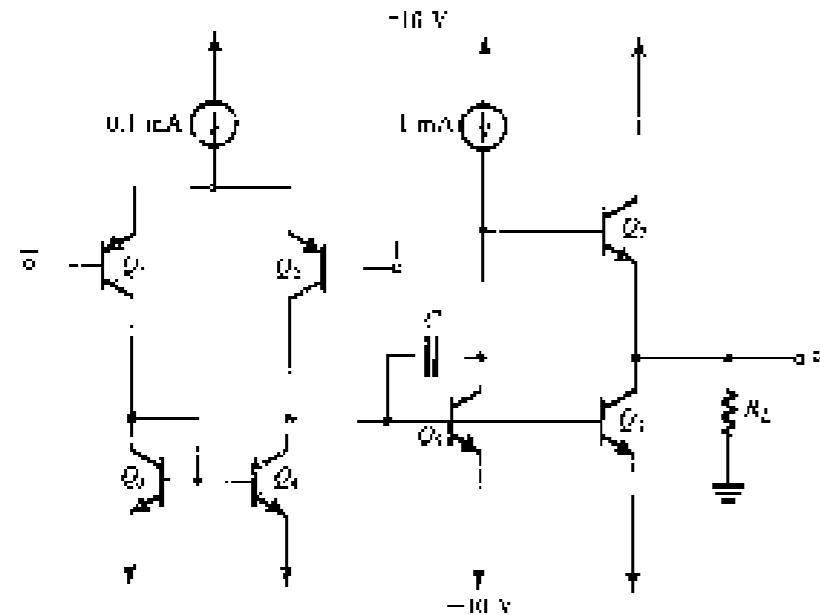


FIGURE 9.61

(c) With load as in (b), calculate the value of the capacitor C required for a 0.01% error over a 1-MHz bandwidth.

SECTION 9.7: DATA CONVERTERS—AN INTRODUCTION

9.62 A 12-bit ADC digitizes an analog signal in the range 0 to +10 V to be digitized with a quantization error of less than 1% of full scale. What is the number of bits required? What is the resolution of the converter? If the range is to be extended to ± 10 V with the same resolution, what is the number of bits required? For an analog-to-digital range of 0 to +10 V, how many bits are required to provide the same resolution? What is the corresponding resolution and quantization error?

***9.63** Consider Fig. 9.38. On the staircase output of the DAC circuit sketch the output of a simple low-pass RC circuit with a time constant that is 10 times that of the sampling interval and the equal to the sampling interval.

SECTION 9.8: D/A CONVERTER CIRCUITS

9.64 Consider the DAC circuit of Fig. 9.39 for the cases $N = 2, 4$, and 8 . What is the tolerance, expressed as parts to which the resistors should be selected to limit the resulting output error to the equivalent of ± 1 LSB?

9.65 The BJT's in the circuit of Fig. 9.46 are two-base emitter junctions scaled in the ratios indicated. Find I_1 in terms of I .

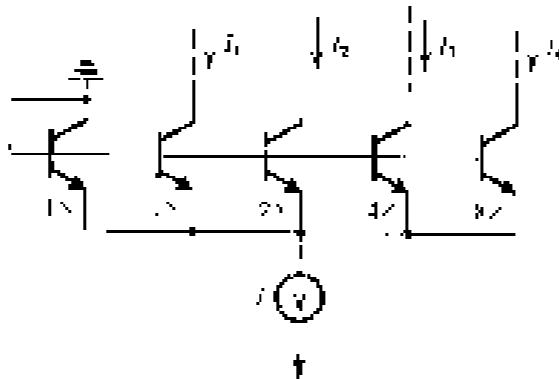


FIGURE 9.65

D*9.67 The circuit in Fig. 9.41 can be used to multiply an analog signal by a digital code by feeding the analog signal to the V_{in} terminal. In this case, the D/A converter is used as a multiplying DAC or MDAC. Given an input, a staircase signal of 10 mV bin width, use the circuit of Fig. 9.41 together with an operational amp to compute $v_o = D v_{in}$, where D is the digital word given by Eq. (9.125) for $N = 4$. How many discrete staircase amplitudes are available at the output? What is the analog error if N is the largest? To what digital input does a 10-V peak-to-peak output correspond?

9.68 What is the input resistance seen by V_{in} in the circuit of Fig. 9.41?

SECTION 9.9: A/D CONVERTER CIRCUITS

9.69 A 12-bit, multistep ADC of the type outlined in Fig. 9.44 utilizes a 1-MHz clock and has $V_{ref} = +10$ V. The analog input voltage is in the range from -10 V. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N . What is the time required to convert an input voltage equal to the full-scale value? If the peak voltage reached at the output of the integrator is 10 V, what is the integration time constant? If the noise is 8 times μV and C increases by 1%, what does V_{out} become? Does the conversion accuracy change?

9.70 The design of a 4-bit flash ADC such as the shown in Fig. 9.45 is being considered. How many comparators are required? For an input signal in the range of 0 to +10 V, what are the reference voltages needed? Show how they are generated using a 10-V reference and several 1-k Ω resistors (know margin). If a comparison is possible in 50 ns and the associated logic requires 30 ns, what is the maximum possible conversion rate? For one of the digital code you expect at the output of the comparators and the output of the logic in no input at (a) 0 V, (b) +5.1 V, and (c) +10 V.

CHAPTER 10

Digital CMOS Logic Circuits

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INTRODUCTION

This chapter is concerned with the study of CMOS digital logic circuits. CMOS is by far the most popular technology for the implementation of digital systems. The small size, ease of fabrication, and low power dissipation of MOSFET's make extremely high levels of integration of both logic and memory circuits. The latter will be studied in Chapter 11.

The chapter begins with an overview section whose objective is to place its proper perspective the material we shall study in this chapter and the next. Then, building on the study of the CMOS inverter in Section 4.10, we take a comprehensive look at its design and analysis. This material is then applied to the design of CMOS logic circuits and two other types of logic circuits (namely, pseudo-NMOS and pass-transistor logic) that are frequently employed in special applications, as supplements to CMOS.

To reduce the power dissipation even further, and simultaneously to increase performance (speed of operation), dynamic logic techniques are employed. This challenging topic is the subject of Sec. 10.6 and completes our study of logic circuits. The chapter concludes with a SPICE simulation example.

In summary, this chapter provides a reasonably comprehensive and in-depth treatment of CMOS digital integrated-circuit design, perhaps the most significant area (at least in

terms of production volume and societal impact) of electronic circuits is. To gain the most out of studying this chapter, the reader must be thoroughly familiar with the MOS transistor. Thus, a review of Chapter 4 is recommended, and a careful study of Section 4.10 is a must.

10.1 DIGITAL CIRCUIT DESIGN: AN OVERVIEW

In this section, we build on the introduction to digital circuits presented in Section 1.7 and provide an overview of the subject. We discuss the various technologies and logic-circuit families currently in use, consider the parameters employed to characterize the operation and performance of logic circuits, and finally mention the various styles for digital-system design.

10.1.1 Digital IC Technologies and Logic-Circuit Families

The chart in Figure 10.1 shows the major IC technologies and logic-circuit families that are currently in use. The concept of a logic-circuit family perhaps needs a few words of explanation. Members of each family are made with the same technology, have a similar circuit structure, and exhibit the same basic features. Each logic-circuit family offers a unique set of advantages and disadvantages. In the conventional style of designing systems, one selects an appropriate logic family (e.g., TTL, CMOS, or ECL) and attempts to implement as much of the system as possible using circuit modules (chips) that belong to this family. In this way, interconnection of the various packages is relatively straightforward. On the other hand, packages from more than one family are used, one has to design suitable interface circuits. The selection of a logic family is based on such considerations as logic flexibility, speed of operation, availability of complex functions, noise immunity, operating-voltage range, power dissipation, and cost. We will discuss some of these considerations in this chapter and the next. To begin with, we make some remarks on each of the four technologies listed in the chart of Fig. 10.1.

CMOS Although shown as one of four possible technologies, this is not an indication of digital IC market share. CMOS technology is, by a large margin, the most dominant of all the IC technologies available for digital-circuit design. As mentioned earlier, CMOS has replaced NMOS, which was employed in the early days of VLSI (in the 1970s). There are a number of reasons for this development, the most important of which is the much lower power dissipation of CMOS circuits. CMOS has also replaced bipolar as the technology-of-choice in digital-system design, and has made possible levels of integration (or circuit-packing

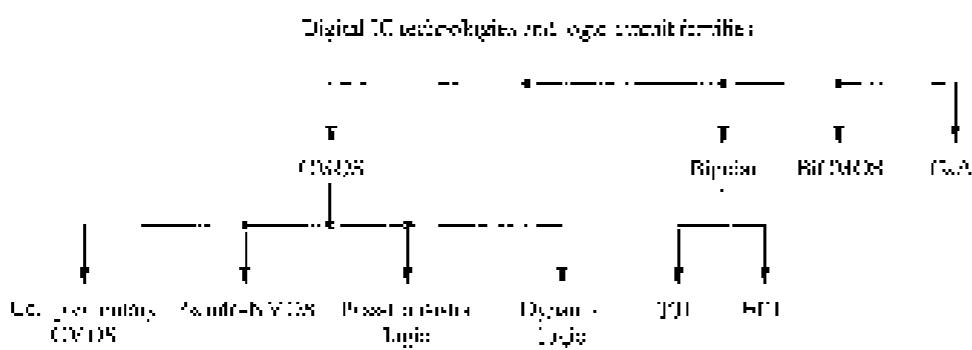


FIGURE 10.1 Digital IC technologies and logic-circuit families.

densities), and a range of applications, none of which would have been possible with bipolar technology. Furthermore, CMOS continues to advance, whereas there appear to be few improvements at the present time in bipolar digital circuits. Some of the reasons for CMOS surpassing bipolar technology in digital applications are as follows:

1. CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuitry on a chip than is possible with bipolar circuits. We will have a lot more to say about power dissipation in the following sections.
2. The high input impedance of the MOS transistor allows the designer to use charge storage as a means for the temporary storage of information in both logic and memory circuits. This technique cannot be used in bipolar circuits.
3. The feature size (i.e., minimum channel length) of the MOS transistor has decreased dramatically over the years, with some recently reported designs utilizing channel lengths as short as 0.06 μm . This permits very tight circuit packing and, correspondingly, very high levels of integration.

Of the various forms of CMOS, complementary CMOS circuits based on the inverter studied in Section 4.10 are the most widely used. They are available both as small-scale integrated (SSI) circuit packages containing ~10 logic gates and medium-scale integrated (MSI) circuit packages (~1–100 gates per chip) for assembling digital systems on printed-circuit boards. More significantly, complementary CMOS is used in VLSI logic (with millions of gates per chip) and memory circuit design. In some applications, complementary CMOS is supplemented by one or both of two other MOS logic-circuit forms. These are pseudo-NMOS, so-named because of its similarity in structure to NMOS logic, and pass-transistor logic, both of which will be studied in this chapter.

A fourth type of CMOS logic circuit utilizes dynamic techniques to obtain fast circuit operation, while keeping the power dissipation very low. Dynamic CMOS logic represents an area of growing importance. Lastly, CMOS technology is used in the design of memory chips, as will be detailed in Chapter 21.

Bipolar Two logic-circuit families based on the bipolar junction transistor are in widespread use at present: TTL and ECL. Transistor-transistor logic (TTL, or T^2L) was for many years the most widely used logic-circuit family. Its decline was precipitated by the advent of the VLSI era. TTL manufacturers, however, fought back with the introduction of low-power and high-speed versions. In these newer versions, the higher speeds of operation are made possible by preventing the BJT from saturating and thus avoiding the slow turnoff process of a saturated transistor. These nonsaturating versions of TTL utilize the Schottky diode discussed in Section 3.8 and are called Schottky TTL or variations on this name. Despite all these efforts, TTL is no longer a significant logic-circuit family and will not be studied in this book.

The other bipolar logic-circuit family in present use is emitter-coupled logic (ECL). It is based on the current-switch implementation of the inverter, discussed in Section 1.7. The basic element in ECL is the differential EPI pair studied in Chapter 7. Because ECL is basically a current-steering logic, and, correspondingly, also called current-mode logic (CML), in which saturation is avoided, very high speeds of operation are possible. Indeed, of all the commercially available logic-circuit families, ECL is the fastest. ECL is also used in VLSI circuit design when very high operating speeds are required and the designer is willing to accept higher power dissipation and increased silicon area. As such, ECL is considered an important specialty technology and will be briefly discussed in Chapter 11.

BiCMOS BiCMOS combines the high switching speeds possible with BJT's because of their inherently higher conductances, with the low power dissipation and other excellent characteristics of CMOS. Like CMOS, BiCMOS allows for the implementation of both analog and digital circuits on the same chip. (See the discussion of using BiCMOS diversity in Chapter 6.) At present, BiCMOS is used to great advantage in special applications, including memory chips, where its high performance as a high-speed capacitive-current driver justifies the more complex technology it requires. A brief discussion of BiCMOS is provided in Chapter 11.

Gallium Arsenide (GaAs) The high carrier mobility in GaAs results in very high speeds of operation. This has been demonstrated in a number of digital IC's using GaAs technology. It should be pointed out, however, that GaAs remains an "emerging technology," one that appears to have great potential but has not yet achieved such potential commercially. As such, it will not be studied in this book. Nevertheless, considerable material on GaAs devices and circuits, including digital circuits, can be found in the CD accompanying this book and on the book's website.

10.1.2 Logic-Circuit Characterization

The following parameters are usually used to characterize the operation and performance of a logic-circuit family.

Noise Margins The static operation of a logic-circuit family is characterized by the voltage transfer characteristic (VTC) of its basic inverter. Figure 10.2 shows such a VTC and defines its four parameters, V_{DD} , V_{DD} , V_{SS} , and V_{SS} . Note that V_{DD} and V_{SS} are defined as the points at which the slope of the VTC is -1 . Also indicated is the definition of the threshold voltage, V_{TH} , or V_T , as we shall frequently call it, as the point at which $V_O = V_I$. Recall that we discussed the VTC in its generic form in Section 1.7, and have also seen specific VTCs in Section 4.10 for the CMOS inverter, and in Section 5.10 for the BJT inverter.

The robustness of a logic-circuit family is determined by its ability to reject noise, and thus by the noise margins NM_H and NM_L :

$$NM_H \equiv V_{DD} - V_{DD} \quad (10.1)$$

$$NM_L \equiv V_{SS} - V_{SS} \quad (10.2)$$

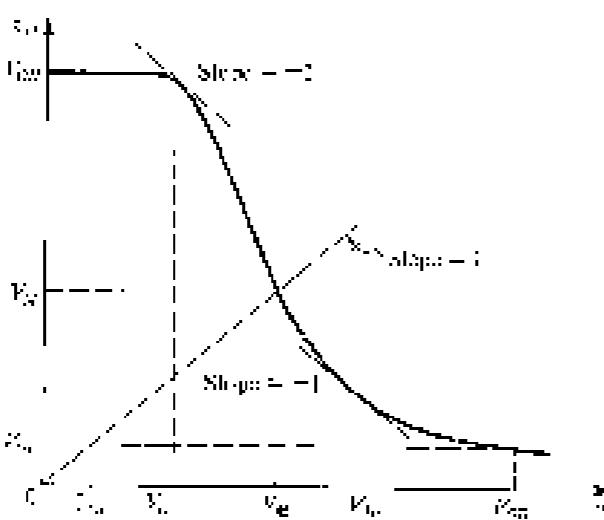


FIGURE 10.2 Typical voltage transfer characteristic (VTC) of a logic inverter. (Inverters are often built with the output inverter.)

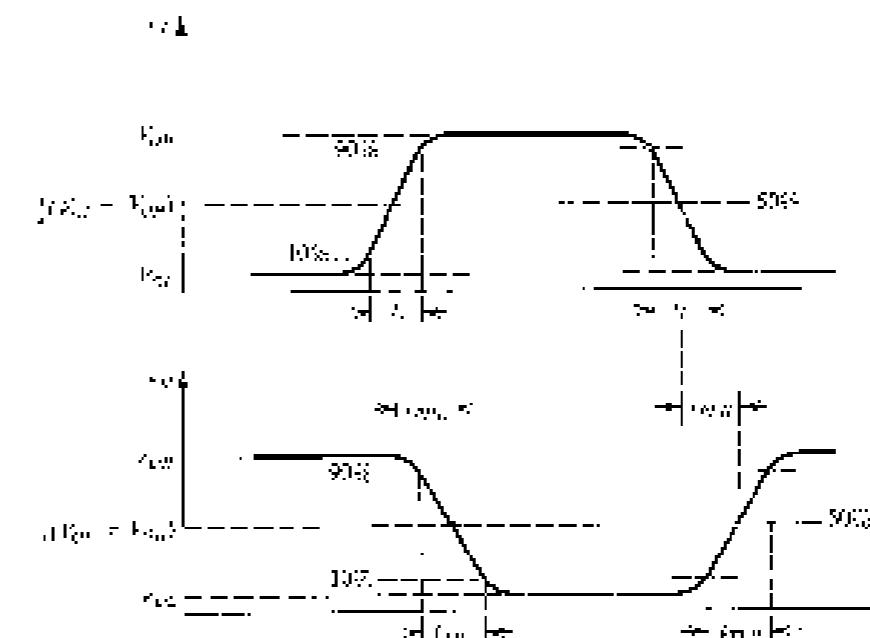


FIGURE 10.3 Definition of propagation delays and switching times for the logic inverter.

An ideal inverter is one for which $NM_H = NM_L = V_{DD}/2$, where V_{DD} is the power-supply voltage. Further, in an ideal inverter, the threshold voltage $V_T = V_{DD}/2$.

Propagation Delay The dynamic performance of a logic-circuit family is characterized by the propagation delay of its basic inverter. Figure 10.3 illustrates the definition of the low-to-high propagation delay (t_{DH}) and the high-to-low propagation delay (t_{DL}). The inverter propagation delay (t_P) is defined as the average of these two quantities:

$$t_P = \frac{1}{2}(t_{DH} + t_{DL}) \quad (10.3)$$

Obviously, the shorter the propagation delay, the higher the speed at which the logic-circuit family can operate.

Power Dissipation Power dissipation is an important issue in digital-circuit design. This needs to minimize the gate power dissipation is motivated by the desire to pack an ever-increasing number of gates on a chip, which in turn is motivator by space and cost considerations. In general, however, in today's digital systems of VLSI, the numbers of gates and memory cells, and thus the total power required within reasonable bounds, the power dissipation per gate and per memory cell should be kept as low as possible. This is most clearly the case for portable, battery-powered equipment such as cellular phones and personal digital assistants (PDAs).

There are two types of power dissipation in a logic gate: static and dynamic. Static power refers to the power that the gate dissipates in the absence of switching action. It results from the presence of a path in the gate circuit, between the power-supply and ground, in one or both of its two states (i.e., with the output either low or high). Dynamic power, on the other hand, occurs only when the gate is switching. An inverter operated from a power supply V_{DD} and driving a load capacitance C , dissipates dynamic power P_D ,

$$P_D = \frac{1}{2}CV_{DD}^2 \quad (10.4)$$

where f is the frequency at which the inverter is being switched. The derivation of this equation (Section 4.10) is based on the assumption that the low and high output voltage levels are 0 and V_{DD} , respectively.

Delay-Power Product One is usually interested in high-speed performance (low t_{PD}) combined with low power dissipation. Unfortunately, these two requirements are often in conflict; generally, when designing a gate, if one attempts to reduce power dissipation by decreasing the supply voltage, or the supply current, or both, the current-driving capability of the gate decreases. This in turn results in longer times to charge and discharge the load and parasitic capacitance, and thus the propagation delay increases. It follows that a figure-of-merit for comparing logic-circuit technologies (or families) is the delay-power product, defined as

$$DP = P_D t_{PD} \quad (10.5)$$

where P_D is the power dissipation of the gate. Note that DP has the units of joules. The lower the DP figure for a logic family, the more effective it is.

Silicon Area An obvious objective in the design of digital VLSI circuits is the minimization of silicon area per logic gate. Smaller area requirement enables the fabrication of a larger number of gates per chip, which has economic and space advantages from a system-design standpoint. Area reduction occurs in three different ways: through advances in processing technology that enable the reduction of the minimum device size, through layout techniques, and through careful chip layout. In this book, our interest lies in circuit design, and we shall make frequent comments on the relationship between the circuit design and its silicon area. As a general rule, the simpler the circuit, the smaller the area required. As will be seen shortly, the circuit designer has to decide on device sizes. Choosing smaller devices has the obvious advantage of requiring smaller silicon areas and at the same time reducing parasitic capacitance and thus increasing speed. Smaller devices, however, have lower current-driving capability, which tends to increase delay. Thus, as in all engineering design problems, there is a trade off to be quantified and exercised in a manner that optimizes whatever aspect of the design is thought to be critical for the application at hand.

Fan-in and Fan-out The fan-in of a gate is the number of its inputs. Thus, a four-input NOR gate has a fan-in of 4. Fan-out is the maximum number of similar gates that a gate can drive while operating within guaranteed specifications. As an example, we saw in Section 4.10 that increasing the fan-out of the RFT inverter reduces t_{PD} and hence NM_{eff} . In this case, to keep NM_{eff} above a certain minimum, the fan-out has to be limited to a calculable π , minimum value.

10.1.3 Styles for Digital System Design

The conventional approach to designing digital systems consists of assembling the system using standard IC packages of various levels of complexity (and hence integration). Many systems have been built this way using, for example, TTL, ECL, and MSI packages. The recent VLSI, in addition to providing the system designer with more powerful off-the-shelf components such as microprocessors and memory chips, has made possible alternative design styles. One such alternative is to opt for implementing part or all of the system using one or more custom ICs. However, custom IC design is usually economically justified only when the production volume is large (greater than about 100,000 parts).

An intermediate approach, known as semi-custom design, utilizes standard chips. These are integrated circuits containing 100,000 or more interconnected logic gates. Their interconnection can be achieved by a final metallization step (performed at the IC fabrication facility).

asments are pre-set specified by the user to implement the user's particular functional need. A more recently available type of gate array, known as a field-programmable gate array (FPGA), as its name indicates, be programmed directly by the user. FPGAs provide a very malleable means for the digital system designer to implement complex logic functions in VLSI form without having to incur either the cost or the "turn-around time" inherent in custom and, to a lesser extent, in semi-custom IC design (see Finne and Rose (1995)).

10.1.4 Design Abstraction and Computer Aids

The design of very complex digital systems, whether on a single IC chip or using off-the-shelf components, is made possible by the use of different levels of design abstraction, and the use of a variety of computer aids. To appreciate the concept of design abstraction, consider the process of designing a digital system using off-the-shelf packages of logic gates. The designer consults data sheets (and books) to determine the input and output characteristics of the gates, their fan-in and fan-out limitations, and so on. In connecting the gates, the designer needs to adhere to a set of rules specified by the manufacturer in the data sheets. The designer does not need to consider, in a direct way, the circuit inside the gate package to effect the circuit, has been abstracted in the form of a functional block that can be used as a component. This greatly simplifies system design. The digital IC designer follows a similar process. Circuit blocks are designed, characterized, and stored in a library as standard cells. These cells can then be used by the IC designer to assemble a larger subsystem (e.g., an adder or a multiplier), which in turn is characterized and stored as a functional block to be used in the design of an even larger system (e.g., an entire processor).

At every level of design abstraction, the need arises for simulation and other computer programs that help make the design process as automated as possible. While SPICE is employed in circuit simulation, other software tools are utilized at other levels and in other phases of the design process. Although digital system design and design automation are outside the scope of this book, it is important that the reader appreciate the role of design abstraction and computer aids in digital design. They are what make it basically possible to design a 100 million-transistor digital IC. Unfortunately, analog IC design does not lend itself to the same level of abstraction and automation. Each analog IC to a large extent has to be "hand-crafted." As a result, the complexity and density of analog ICs remain much below what is possible in a digital IC.

Whatever approach or style is adopted in digital design, being familiar with the various digital circuit technologies and design techniques is essential. This chapter and the next aim to provide such a background.

10.2 DESIGN AND PERFORMANCE ANALYSIS OF THE CMOS INVERTER

The CMOS logic inverter was introduced and studied in Section 4.10, which we urge the reader to review before proceeding any further. In this section, we take a more comprehensive look at the inverter, investigating its performance and exploring the trade-offs available in its design. This material will serve as the foundation for the study of CMOS logic circuits in the following section.

10.2.1 Circuit Structure

The inverter circuit, shown in Fig. 10.4(a), consists of a pair of complementary MOSFETs switched by the input voltage v_i . Although not shown, the source of each device is connected

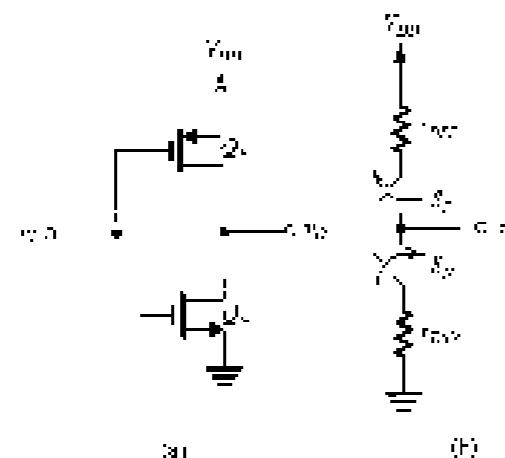


FIGURE 10.4 (a) the CMOS inverter and (b) its representation as a pair of switches operating in complementary fashion.

width L , thus eliminating the body effect. Usually, the threshold voltages V_{th} and V_V are equal in magnitude; that is, $V_{th} = V_D - V_S$, which is in the range of 0.2 V to 0.5 V, with values near the lower end of this range for modern process technologies having small feature size (e.g., with channel length of 0.5 to 0.1 μm or less).

The inverter circuit can be represented by a pair of switches operating in a complementary fashion, as shown in Fig. 10.4(b). As indicated, each switch is modeled by a finite on resistance, which is the steady-state resistance of the respective transistor, evaluated near $v_{ds} \approx 0$,

$$r_{on1} = k_1 \left(\frac{W}{L} \right) \left(V_{DD} - V_{th} \right) \quad (10.6)$$

$$r_{on2} = k_2 \left(\frac{W}{L} \right) \left(V_{DD} - V_{th} \right) \quad (10.7)$$

10.2.2 Static Operation

With $v_1 = v_2 = v_{DD} = V_{DD}$, and the output node is connected to V_{DD} through the resistance r_{on1} of the pull-up network of Q_1 . Similarly, with $v_1 = V_{DD}$, $v_2 = V_{DD} = 0$, and the output node is connected to ground through the resistance r_{on2} of the pull-down transistor Q_2 . Thus, in the steady state, no direct-current path exists between V_{DD} and ground, and the static-current and the static-power dissipation are both zero (leakage effects are usually negligibly small, particularly for large-value L devices).

The voltage transfer characteristic of the inverter is shown in Fig. 10.5, from which it is confirmed that the input voltage levels are 0 and V_{DD} , and that the output voltage swing is the maximum possible. The fact that V_{DD} and $V_{DD}/2$ are independent of device dimensions makes CMOS very different from other forms of MOS logic.

The CMOS inverter can be made a switch at the midpoint of the logic swing, 0 to V_{DD} , that is, at $V_{DD}/2$, by appropriately sizing the transistors. Specifically, it can be shown that the switching threshold $1/V_D$ (or $V_{DD}/2$) is given by

$$V_D = \frac{V_{DD} - V_{th}}{1 + \sqrt{k_1/k_2}} \quad (10.8)$$

where $k_1 = k_2(W/L)_1$ and $k_2 = k_1(W/L)_2$, from which we see that for the typical case where $V_{DD} = V_{DD_0}$, $V_D = V_{DD}/2$ for $k_1 = k_2$, that is,

$$V_D(W/L)_1 = L_2^2/(W/L)_2 \quad (10.9)$$

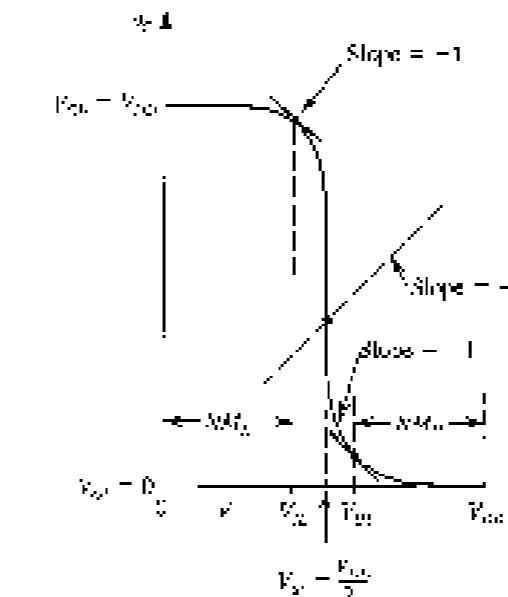


FIGURE 10.5 Inverse transfer characteristic (ITC) of the CMOS inverter when Q_1 and Q_2 are equal.

This a symmetric transfer characteristic is obtained when the devices are designed to have equal transconductance parameters, a condition we refer to as matching. Since μ_n is two to four times larger than μ_p , matching is achieved by making $(W/L)_2$ two to four times $(W/L)_1$, $k_2/k_1 \approx 2$ to 4.

$$\left(\frac{W}{L} \right)_2 = \frac{\mu_n}{\mu_p} \left(\frac{W}{L} \right)_1 \quad (10.10)$$

Normally, the two devices have the same channel length, L , which is set at the minimum allowable for the given process technology. The minimum width of the NMOS transistor is usually one and a half to two times L , and the width of the PMOS transistor is up to three times that. For example, for a 0.25- μm process for which $\mu_n/\mu_p = 3$, $L = 0.25 \mu\text{m}$, $(W/L)_1 = 0.35 \mu\text{m}/0.25 \mu\text{m}$, and $(W/L)_2 = 1.25 \mu\text{m}/0.25 \mu\text{m}$. As we shall discuss shortly, if the inverter is required to drive a relatively large capacitive load, the transistors are made wider. However, in dense chip areas, most of the inverters would have this "minimum size." For future purposes, we shall denote the (W/L) ratio of the NMOS transistor of this minimum-size inverter by α and the (W/L) ratio of the PMOS transistor by β . Since the inverter area can be represented by $W_1L_1 + W_2L_2 = (W_1 + W_2)L$, the area of the minimum-size inverter is $(\alpha + \beta)L^2$, and we can use the factor $(\alpha + \beta)$ as a proxy for area. For the example cited earlier, $\alpha = 1.5$, $\beta = 1.5$, and the area factor $\alpha + \beta = 6$.

Besides setting the gate threshold at the center of the logic swing, matching the transconductance parameters of Q_1 and Q_2 provides the inverter with equal current-driving capability in both directions (pull-up and pull-down). Furthermore, and obviously related, it makes $t_{PD1} = t_{PD2}$. Thus an inverter with matched transistors will have equal propagation delays, $t_{PD} = 0.5(t_{PD1} + t_{PD2})$.

When the inverter threshold is at $V_{DD}/2$, the noise margins NMr and NMd are equalized, and their values are maximized, such that (Section 4.10):

$$NMr = NMd = \frac{1}{2}(V_{DD} - \frac{V_D}{2}) \quad (10.11)$$

Since typically $V = 0.1$ to $0.2 V_{DD}$, the noise margins are approximately $0.4 V_{DD}$. This value being close to half the power supply voltage, makes the CMOS inverter nearly ideal from a noise-margins standpoint. Further, since the inverter dc input current is practically zero, the noise margins are not dependent on the gate fan-out.

Although we have emphasized the advantages of matching Q_u and Q_p , there are occasions in which this scaling is not advised. One might, for instance, forgo the advantages of matching in return for reducing chip area and simply make $(W/L)_u = (W/L)_p$. There are also instances in which a deliberate mismatch is used to place V_{th} at a specified value other than $V_{th0}/2$. Note that by making $\beta_r > \beta_p$, V_{th} moves closer to zero, whereas $k_1 > k_0$ moves V_{th} closer to V_{th0} .

As a final comment on the inverted VTC, we note that the slope in the transition region through α_{app} , as given by $-1/\alpha_{\text{app}} = g_0 \partial \alpha_{\text{app}} / \partial \mu$, is

19.2.3 Dynamic Operation

The propagation delay of the inverter is set by the required width of the transition that it is to drive an identical inverter. This situation is depicted in Fig. 10.6. We wish to analyze this circuit to determine the propagation delay of the inverter comprising Q_1 and Q_2 , which is driven by a low-frequency source v_{in} and is loaded by the inverter consisting of Q_3 and Q_4 . Indicated in the figure are the various transient internal capacitances that are connected to the output node of the (Q_1, Q_2) inverter. Obviously, an exact pencil-and-paper analysis of this circuit will be too complicated to yield useful design insight, and a simplification of the circuit is in order. Specifically, we wish to replace all the capacitances attached to the inverter output node with a single capacitance C connected between the output node and ground. If we are able to do that, we can utilize the results of the transient analysis performed in Section 10.3. Toward that end, we note that during time $t = t_{out}$, the output of the first inverter changes from 0 to $V_{DD}/2$ or from $V_{SS}/2$ to $V_{DD}/2$, respectively. It follows that the second inverter remains in the same state during each of our analysis intervals. This observation will have an important bearing on our estimation of the equivalent input capacitance of the second inverter. Let's now consider the contribution of each of the capacitances to

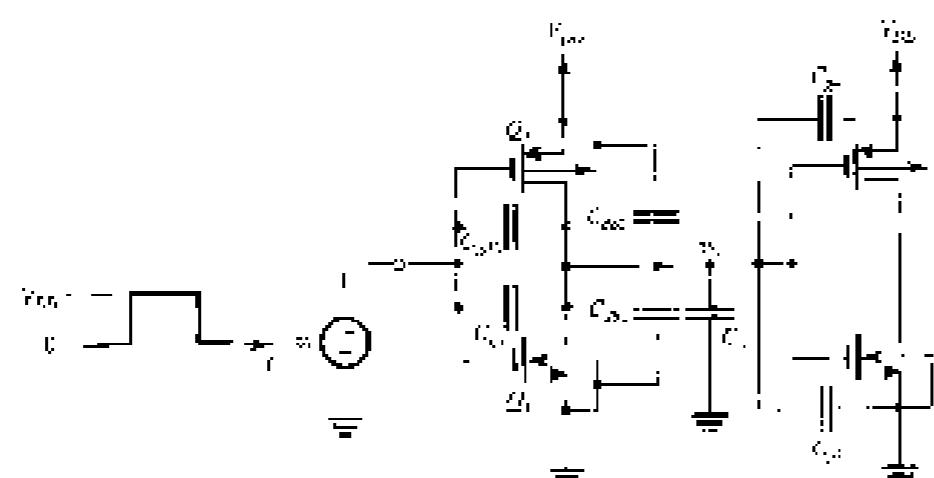


FIGURE 10-6 Circuit for analyzing the propagation delay of the inverter formed by Q_1 and Q_2 , which draws an idle current, inverse formed by Q_3 and Q_4 .

Fig. 10.6 In the value of the equivalent load expansion

- The gate-drain overlap capacitance of Q_2 , C_{gso} , can be replaced by an equivalent capacitance between the output node and ground of $2C_{gso}$. The factor 2 arises because of the Miller effect (Section 8.1.4). Specifically, note that as v_t goes high and v_o goes low by the same amount, the change in voltage across C_{gso} is twice that amount. Thus the output node sees in effect twice the value of C_{gso} . The same applies for the gate-drain overlap capacitance of Q_3 , C_{gso} , which can be replaced by a capacitance $2C_{gso}$ between the output node and ground.
 - Each of the drain-body capacitances C_{bs1} and C_{bs2} can be represented as a constant with sign. Thus for the purpose of our analysis here, C_{bs1} and C_{bs2} can be replaced with equal capacitances between the output node and ground. Note, however, that the form as given in Section 4.8 for calculating C_{bs1} and C_{bs2} are small-signal relationships, whereas the analysis here is obviously a large-signal one. A technique has been developed for finding equivalent large-signal values for C_{bs1} and C_{bs2} (see Hodges and Jackson (1988) and Rabacy (2002)).
 - Since the second inverter does not switch steady, we will assume that the input capacitances of Q_3 and Q_4 remain approximately constant and equal to the total gate capacitance ($2(C_{gso} + C_{bs2}) = C_{gso} = C_{input}$). That is, the input capacitance of the load inverter will be

$$C_{\text{rel}} + C_{\text{A}} = (\text{WL})_1 C_{\text{rel}} + (\text{WL})_2 C_{\text{rel}} + C_{\text{new}} + C_{\text{wels}} + C_{\text{weld}} + C_{\text{old}}$$

- The last component of C is the wiring capacitance C_w , which simply adds to the value of C .

Thus, the real value of C is given by

$$C = 2C_{\text{eff}} + 2C_{\text{eff}} - C_{\text{eff}} + C_{\text{eff}} + C_{\text{eff}} + C_{\text{eff}} = C_b \quad (10.2)$$

Having determined an approximate value for the equivalent capacitance between the inverter output node and ground, we can utilize the circuit in Fig. 10.7 to determine t_{on} and t_{off} , respectively. Since the two circuits are similar, we need only consider one and apply the result directly to the other. Consider the circuit in Fig. 10.7(a), which applies when $V_{\text{in}} > V_{\text{th}}$ and C_{L} discharges C from its initial voltage of V_{off} to the final value of 0. The analysis is somewhat complicated by the fact that initially Q_C will be in the saturation mode and then, when v_C falls below $V_{\text{th}} - V_t$, it will go into the triode region of operation. We have in fact performed this analysis in Section 4.10 and obtained the following approximate expression for t_{on} :

$$t_{\text{min}} = \frac{1.6C}{k_e^2 \frac{\epsilon_0}{T} V_{\text{DD}}} \quad (16.12)$$

where we have assumed that $\lambda = 0.2 \text{ fm}$, which is around the value

There is an alternative, an approximate but simpler, method for analyzing the circuit in Fig. 10.25(a). It is based on computing an average value for the discharge current i_{Q_1} during the interval $t = 0$ to $t = t_{Q_1}$. Specifically, at $t = 0$, Q_1 will be saturated, and $i_{Q_1}(0)$ is given by

$$t_{2,\mu}(0) = \frac{1}{2} k_0^2 \left(\frac{M_\pi}{r_0} \right)^2 (V_{2\mu} - V_0)^2 \quad (10.14)$$

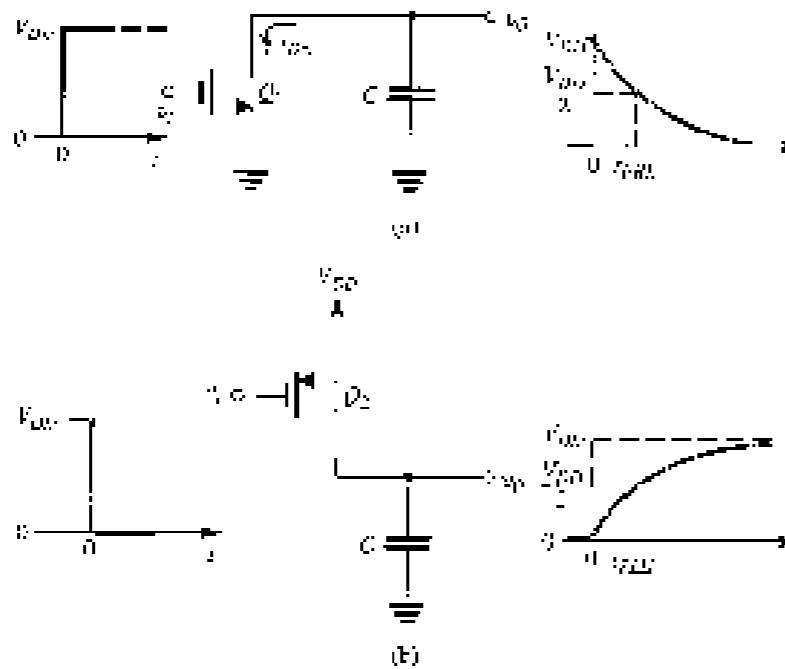


FIGURE 10.7 Equivalent circuit diagrams for determining the propagation delay: (a) V_{DD} is 0; (b) V_{DD} is the inverter.

At $t = t_{\text{prop}}$, Q_1 will be in the triode region, and $i_{\text{dis}}(t_{\text{prop}})$ will be

$$i_{\text{dis}}(t_{\text{prop}}) = \frac{V_{DD}^2}{L_s I_s} \left[(V_{DD} - V_{T_{SD}}) \frac{V_{DD}}{2} - \frac{1}{2} \left(\frac{V_{DD}}{2} \right)^2 \right] \quad (10.15)$$

The average discharge current can then be found as

$$i_{\text{avg}} = \frac{1}{2} i_{\text{dis}}(0) + i_{\text{dis}}(t_{\text{prop}}) \quad (10.16)$$

and the discharge interval t_{prop} computed from

$$t_{\text{prop}} = \frac{CAY}{i_{\text{avg},\text{av}}} = \frac{CV_{DD}/2}{i_{\text{avg},\text{av}}} \quad (10.17)$$

Dividing Eqs. (10.14) through (10.17) and substituting $k_s \approx 0.2 V_{DD}$ gives

$$\text{FAC} \triangleq \frac{1.7C}{C \left(\frac{V^2}{L_s} \right) V_{DD}} \quad (10.18)$$

which yields a value very close to that obtained by the more precise formula of Eq. (10.13). Which formula to use is not very relevant, since we have already made many approximations. Indeed, our interest in these formulas is not in obtaining a precise value of t_{prop} but in what they tell us about the effect of the various elements on determining the inverter delay. It is such insight that the circuit designer hopes to obtain from manual analysis. Precise values for delay can be determined using computer simulation (Section 10.7).

An expression for the low-to-high inverter delay, t_{prop} , can be written by analogy to the t_{prop} expression in Eq. (10.17),

$$t_{\text{prop}} \triangleq \frac{1.7C}{A_s \left(\frac{V^2}{L_s} \right) V_{DD}} \quad (10.19)$$

Finally, the propagation delay t_p can be found as the average of t_{prop} and t_{rise} ,

$$t_p = \frac{1}{2} (t_{\text{prop}} + t_{\text{rise}})$$

Evaluation of the formulas in Eqs. (10.18) and (10.19) enables us to make a number of useful observations:

1. As expected, the two components of t_p can be equated by selecting the (W/L) ratios to equalize L_s and L_d , that is, by matching Q_s and Q_d .
2. Since t_p is proportional to C , the designer should strive to reduce C . This is achieved by using the minimum possible channel length and by minimizing wiring and other parasitic capacitances. Careful layout of the chip can result in significant reduction in such capacitances and in the value of C_{int} .
3. Using a process technology with large transconductance parameter A_s can result in smaller propagation delays. Keep in mind, however, that for such processes C_{int} is increased, and thus the value of C increases at the same time.
4. Using larger (W/L) ratios can result in a reduction in t_p . Care, however, should be exercised here also, since increasing the size of the devices increases the value of C , and thus the expected reduction in t_p might not materialize. Reducing t_p by increasing (W/L) is an effective strategy when C is dominated by components directly related to the size of the device device (such as wiring or layout devices).
5. A larger supply voltage V_{DD} results in a lower t_p . However, V_{DD} is determined by the process technology and thus is often not under the control of the designer. Furthermore, modern process technologies in which device sizes are reduced require lower V_{DD} (see Table 6.1). A interesting factor that influences V_{DD} is the need to keep the dynamic power dissipation at acceptable levels, especially in very high density chips. We will have more to say on this point shortly.

These observations clearly illustrate the conflicting requirements and the trade-offs available in the design of a CMOS digital integrated circuit (and indeed in any engineering design problem).

10.2.4 Dynamic Power Dissipation

The negligible static power dissipation of CMOS has been a significant factor in its dominance as the technology of choice in manufacturing high-density VLSI circuits. However, as the number of gates per chip steadily increases, the dynamic power dissipation has become a serious issue. The dynamic power dissipated in the CMOS inverter is given by Eq. (10.20), which we repeat here as

$$P_D = f C V_{DD}^2 \quad (10.20)$$

where f is the frequency at which the gate is switched. It follows that minimizing C is an effective means for reducing dynamic power dissipation. An even more effective strategy is the use of a lower power-supply voltage. As we have mentioned, new CMOS process technologies utilize V_{DD} values as low as 1 V. These lower chips, however, pack much more circuitry

on the chip (as many as 100 million transistors) and operate at higher frequencies (where process clock frequencies above 1 GHz are now available). The dynamic power dissipation of such high-density chips can be over 100 W.

Example 10.1 Consider a CMOS inverter fabricated in a 0.25- μm process for which $C_{\text{ox}} = 6 \text{ fF}/\mu\text{m}^2$, $\theta_{\text{A}}C_{\text{ox}} = 1.15 \text{ pA/V}^2$, $\mu_{\text{A}}/\mu_{\text{D}} = 20$ (mA/V^2), $V_{\text{DD}} = -V_{\text{SS}} = 0.4 \text{ V}$, and $V_{\text{DDO}} = 2.5 \text{ V}$. The W/L ratio of Q_1 is $0.25 \text{ }\mu\text{m}/0.25 \text{ }\mu\text{m}$ and that for Q_2 is $1.125 \text{ }\mu\text{m}/0.25 \text{ }\mu\text{m}$. The gate source and gate-drain overlap capacitances are specified to be $0.3 \text{ fF}/\mu\text{m}$ of gate width. Further, the effective value of drain-to-body capacitance is $C_{\text{DB}} = 1 \text{ fF}$ (so $C_{\text{DB}} = 1 \text{ fF}$). The wiring capacitance $C_{\text{w}} = 0.3 \text{ fF}$. For t_{PDH} , t_{LH} , and t_{HL} .

Solution

First we determine the value of the equivalent capacitance C using Eq. (10.12):

$$C = 2C_{\text{DB}} + 2C_{\text{gate}} + C_{\text{w}} = C_{\text{DB}} + C_{\text{g1}} + C_{\text{g2}} + C_{\text{w}}$$

where

$$C_{\text{g1}} = 0.3 \times W_{\text{g1}} = 0.3 \times 0.375 = 0.1125 \text{ fF}$$

$$C_{\text{g2}} = 0.3 \times W_{\text{g2}} = 0.3 \times 1.125 = 0.3375 \text{ fF}$$

$$C_{\text{DB}} = 1 \text{ fF}$$

$$C_{\text{w}} = 1 \text{ fF}$$

$$C_{\text{g1}} = 0.375 \times 0.25 \times 6 = 2 \times 0.3 \times 0.375 = 0.75 \text{ fF}$$

$$C_{\text{g2}} = 1.125 \times 0.25 \times 6 + 2 \times 0.3 \times 1.125 = 2.3625 \text{ fF}$$

$$C_{\text{w}} = 0.3 \text{ fF}$$

Thus,

$$C = 2 \times 0.1125 + 2 \times 0.3375 + 1.125 + 2.3625 + 0.3 = 6.25 \text{ fF}$$

Next, although we can use the formula in Eq. (10.18) to determine t_{PDH} , we shall take an alternative route. Specifically, we shall consider the discharge of C through Q_2 and determine the average discharge current using Eqs. (10.14) through (10.16):

$$\begin{aligned} i_{\text{dis}}(0) &= \frac{1}{2} k_{\text{D}}' \left(\frac{V_{\text{DD}}}{L_{\text{in}}} \right) (V_{\text{DD}} - V_{\text{I}})^2 \\ &= \frac{1}{2} \times 115 \left(\frac{0.375}{0.25} \right) [(2.5 - 0.4)^2] = 280 \text{ }\mu\text{A} \end{aligned}$$

$$\begin{aligned} i_{\text{dis}}(t_{\text{PDH}}) &= k_{\text{D}}' \left(\frac{V_{\text{DD}}}{L_{\text{in}}} \right) (V_{\text{DD}} - \frac{V_{\text{DD}} - V_{\text{I}}}{2} - \frac{V_{\text{DD}}}{2})^2 \\ &= 115 \times \frac{0.375}{0.25} (2.5 - 0.4) \frac{2.5 - 1.25}{2} = 280 \text{ }\mu\text{A} \\ &= 318 \text{ }\mu\text{A} \end{aligned}$$

Thus

$$i_{\text{dis}}|_{\text{PDH}} = \frac{318 - 280}{2} = 19 \text{ }\mu\text{A}$$

and

$$t_{\text{PDH}} = \frac{C(V_{\text{DD}}/2)}{i_{\text{dis}}|_{\text{PDH}}} = \frac{6.25 \times 10^{-19} \times 1.25}{19 \times 10^{-12}} = 23.3 \text{ ps}$$

Since $V_{\text{DD}}/V_{\text{I}} = 2$ and $\mu_{\text{A}}/\mu_{\text{D}} = 20$, the inverter is not perfectly matched. Therefore, we expect t_{LH} to be greater than t_{PDH} by a factor of $3.83/3 = 1.3$, thus

$$t_{\text{LH}} = 1.3 \times 23.3 = 30 \text{ ps}$$

and thus t_{H} will be

$$\begin{aligned} t_{\text{H}} &= \frac{1}{2}(t_{\text{PDH}} + t_{\text{LH}}) \\ &= \frac{1}{2}(23.3 + 30) = 26.5 \text{ ps} \end{aligned}$$

EXERCISES

- (10.1) For the inverter in Example 10.1, determine the total power dissipation.
- (10.2) For the inverter in Example 10.1, determine the percentage realization inefficiency due to the mismatch between the two NMOS and PMOS transistors.
- (10.3) For the inverter of Example 10.1, find the average power dissipation when clocked at a 50% VDD rate.

10.3 CMOS LOGIC-GATE CIRCUITS

In this section, we build on our knowledge of inverter design and consider the design of CMOS circuits that realize combinational logic functions. In combinational circuits, the output at any time is a function only of the values of input signals at that time. Thus, these circuits do not have memory and do not employ feedback. Combinational-logic circuits are used in large quantities in a multitude of applications; indeed, every digital system contains large numbers of combinational-logic circuits.

10.3.1 Basic Structure

A CMOS logic circuit is in effect an extension, or a generalization, of the CMOS inverter. The inverter consists of an NMOS pull-down transistor and a PMOS pull-up transistor, operated by the input voltage in a complementary fashion. The CMOS logic gate consists of four networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors (see Fig. 10.8). The two networks are operated by the input variables, in a complementary fashion. Thus, for the three input gate configurations shown in Fig. 10.8, the PDN will conduct for all input combinations that require a low output ($Y = 0$) and will then pull the output node down to ground, causing a zero voltage to

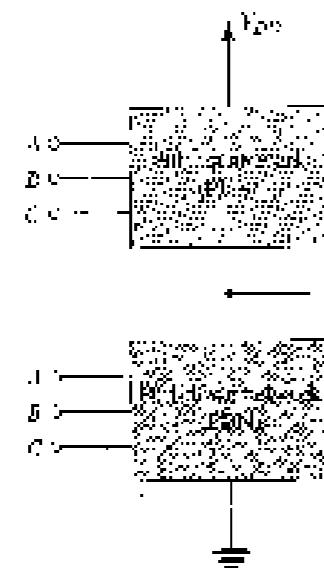


FIGURE 10.8 Representation of a three-input CMOS logic gate. The PUN consists of PMOS transistors, and the PDN consists of NMOS transistors.

appear at the output, $y_F = 0$. Simultaneously, the PDN will be off, and no direct dc path will exist between V_{DD} and ground. On the other hand, all input combinations that call for a high output ($Y = 1$) will cause the PUN to conduct, and the PUN will then pull the output node up to V_{DD} , establishing an output voltage $y_F = V_{DD}$. In other words, the PDN will be at off, and again no dc current path between V_{DD} and ground will exist in this circuit.

Now, given the PUN consists of NMOS transistors, and since an NMOS transistor conducts when the signal at its gate is high, the PUN is activated (i.e., conducting) when the inputs are high. In a dual manner, the PDN consists of PMOS transistors, and a PMOS transistor conducts when the input signal at its gate is low, thus the PUN is activated when the inputs are low.

The PUN and the PDN each allows devices in parallel to form an OR function, and devices in series to form an AND function. Here, the OR and AND notation refer to current flow or conduction. Figure 10.9 shows examples of PUNs. For the circuit in Fig. 10.9(a), we observe that Q_1 will conduct when A is high ($a_F = V_{DD}$), and will then pull y_F from node down to ground ($y_F = 0$, $F = 0$). Similarly, Q_2 conducts and pull y_F down when B is high. Thus F

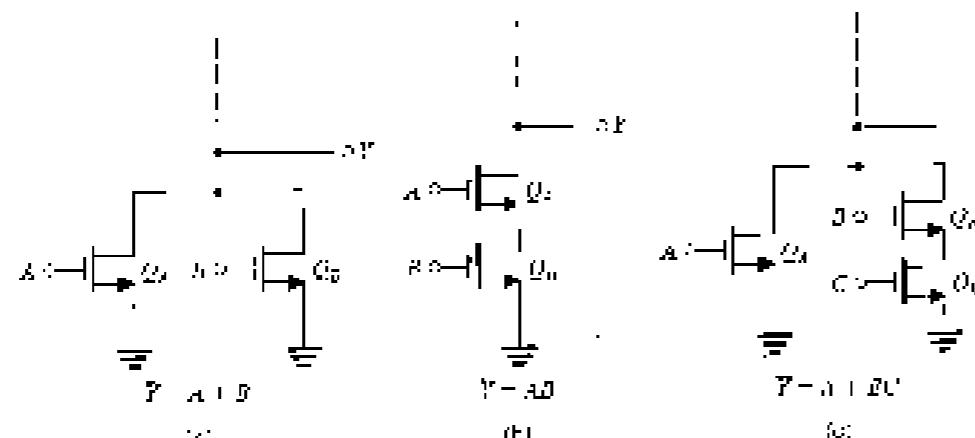


FIGURE 10.9 Examples of PUN down networks.

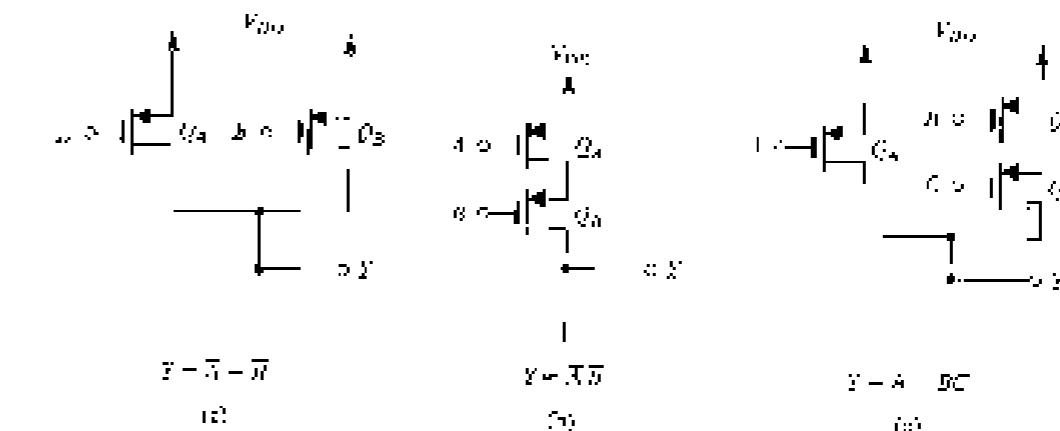


FIGURE 10.10 Examples of PUN up networks.

will be low when A is high or B is high, which can be expressed as

$$F = A \oplus B$$

or equivalently

$$F = \overline{A} \oplus B$$

The PUN in Fig. 10.10(a) will conduct only when A and B are both high simultaneously. Thus F will be low when A is high and B is high.

$$F = A B$$

or equivalently

$$F = \overline{A} \overline{B}$$

As a final example, the PUN in Fig. 10.10(c) will conduct and cause F to be 0 when A is high or when B and C are both high; thus

$$F = A + B C$$

or equivalently

$$F = \overline{A} + \overline{B} \overline{C}$$

Next consider the PUN examples shown in Fig. 10.10. The PUN in Fig. 10.10(b) will conduct and pull y_F to V_{DD} ($F = 1$) when A is low or B is low, thus

$$F = A \oplus \overline{B}$$

The PUN in Fig. 10.10(b) will conduct and produce a high output ($y_F = V_{DD}$, $F = 1$) only when A and B are both low, thus

$$F = \overline{A} B$$

Finally, the PUN in Fig. 10.10(c) will conduct and cause F to be high (logic 1) if A is low or if B and C are both low, thus

$$F = \overline{A} + A C$$

Having developed an understanding and an appreciation of the structure and operation of PUNs and PDNs, we now consider complete CMOS gates. Before doing so, however, we wish to introduce alternative circuit symbols that are almost universally used for MOS transistors by

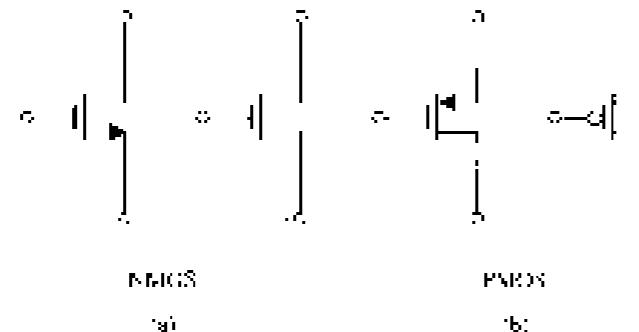


FIGURE 10.17 New and derivative country symbols for ISO-3166

Digital-circuit designers. Figure 10.1 shows our usual symbols (left) and the corresponding “digital” symbols (right). Observe that the symbol for the PMOS transistor with a circle at the gate terminal, is intended to indicate that the signal at the gate has to be low for the device to be activated, i.e., to conduct. Thus, in terms of logic circuit terminology, the gate terminal of the PMOS transistor is an active-low input. Besides indicating this property of PMOS devices, the digital symbol’s arbitrary indication of which of the device terminals is the source and which is the drain. This should cause no difficulty at this stage of our study; simply remember that for an NMOS transistor, the drain is the terminal that is at the higher voltage (current flows from drain to source) and for a PMOS transistor the source is the terminal that is at the higher voltage (current flows from source to drain). To be consistent with the literature, we shall henceforth use these modified symbols for MOS transistors in logic applications, except in situations where our usual symbols help in understanding a circuit operation.

10.3.2 The Two-Input NOR Gate

We first consider the TMC3- α - β that realizes the two input NMR lines.

$$z = \overline{A - B} = \overline{A} + \overline{B} \quad (10.2)$$

We see that T is to be low (PTIN conducting) when A is high or B is high. Thus the PTIN consists of two parallel NMOS devices with A and B as inputs (i.e., the circuit in Fig. 10.9e). For the PUN, we note from the second expression in Eq. (10.21) that Y is to be high when A and B are both low. Thus the PUN consists of two series PMOS devices with A and B as the inputs (i.e., the circuit in Fig. 10.10e). Putting the PUN and the PTIN together gives the CMOS NOR gate shown in Fig. 10.12. Note that, as expected for a higher number of inputs, it is straightforward: for each additional input, an NMOS transistor is added in parallel with Q_1 and Q_{21} , and a PMOS transistor is added in series with Q_N and Q_{2N} .

19.3.3 The Two-input NAND Gate

The `new` from `NANO` function is described by the `Reactor` expression.

$$Y = \overline{J\beta} = \bar{A} - \bar{B} \quad (2.2)$$

To synthesize the PBN, we consider the input combinations that require P to be low. There is only one such combination, namely, A and B both high. Thus, the PBN simply comprise two NMOS transistors in series (such as the circuit in Fig. 10.9b). To synthesize the IVN, we consider the input combinations that result in V being high. These are found from the

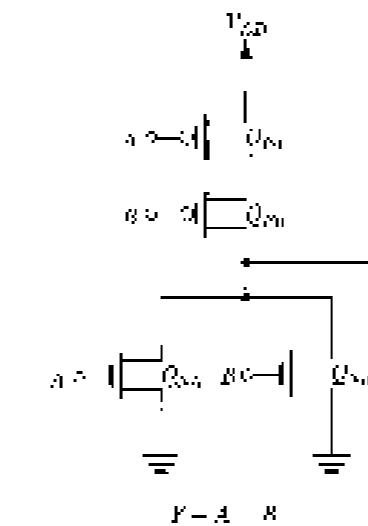


FIGURE 10.12 A typical nonCMOS NOR gate.

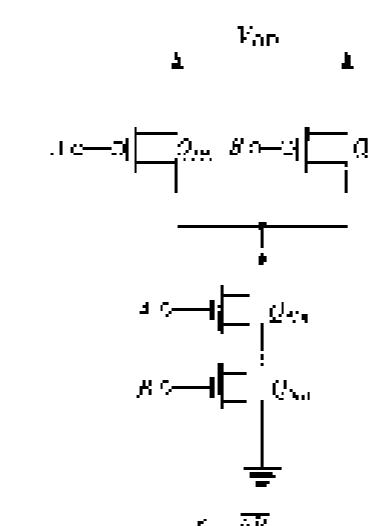


FIGURE 10.11 A portion of the CHOCOMAPDB.

second expression in Eq. 10.10. This is how the PUN consists of two parallel PMOS transistors with A and B applied to their gates (such as the circuit in Fig. 10.10a). Putting the PUN and PDN together results in the CMOS NAND gate implementation shown in Fig. 10.14. Note that extension to a higher number of inputs is straightforward. For each additional input, we add an NMOS transistor in series with Q_1 , and Q_2 , and a PMOS transistor in parallel with Q_1 and Q_2 .

10.34 A Complex Get

Complexity: the more complex logic function

$$Y \equiv \overline{A(\beta + C(t))} \quad (C.23)$$

Since $\bar{Y} = A(H - CD)$, we see that \bar{Y} should be low for a 'right' and simultaneously either B high or C low. This is the type of PON which the PON is directly obtained. To obtain the PON, we

need to express Y in terms of the unplemented variables. We do this through repeated application of DeMorgan's law, as follows:

$$\begin{aligned} Y &= \overline{A(B - CD)} \\ &= \overline{A} + \overline{B} - \overline{CD} \\ &= \overline{A} + \overline{B} \overline{C} \overline{D} \\ &= \overline{A} + \overline{B} \overline{C} \overline{D} \end{aligned} \quad (10.24)$$

Thus, Y is high for A low or B low and either C or D low. The corresponding complete CMOS circuit will be as shown in Fig. 10.14.

10.3.5 Obtaining the PUN from the PDN and Vice Versa

From the CMOS gate circuits considered thus far (e.g., that in Fig. 10.17), we observe that the PDN and the PUN are dual networks. Where a series branch exists in one, a parallel branch exists in the other. Thus, we can obtain one from the other, a process that can be simpler than having to synthesize each separately from the Boolean expression of the function. For instance, in the circuit of Fig. 10.14, we found it relatively easy to obtain the PDN, simply because we already had Y in terms of the unplemented inputs. On the other hand, to obtain the PUN, we had to manipulate the given Boolean expression to express Y as a function of the complemented variables, the form convenient for synthesizing PUNs. Alternatively, we could have used this duality property to obtain the PUN from the PDN. The reader is urged to refer to Fig. 10.14 to convince herself that this is indeed possible.

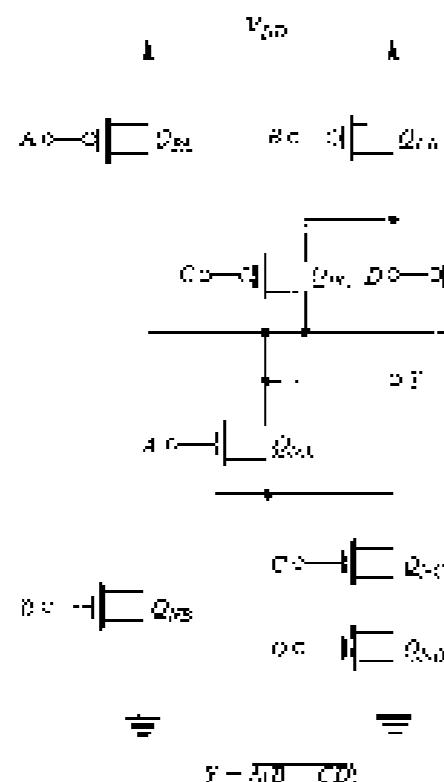


FIGURE 10.14 CMOS realization of a complex gate.

$$Y = \overline{A}(\overline{B} - \overline{CD})$$

It should, however, be mentioned that this is not easy to obtain one of the two networks from the other using the duality property. For such cases, one has to resort to a more rigorous process, which is beyond the scope of this book [see Kang and Leblebici (1997)].

10.3.6 The Exclusive-OR Function

An important function that often arises in logic design is the exclusive-OR (XOR) function:

$$Y = A \oplus B \quad (10.25)$$

We observe that since Y is either high or \overline{Y} is given, it is easier to synthesize the PUN. We note, however, that unfortunately Y is not a function of the complemented variables only (as we would like it to be). Thus, we will need additional inverters. The PUN realization directly from Eq. (10.25) is shown in Fig. 10.15(a). Note that the (Q_1, Q_2) branch realizes the \overline{AB} term ($\overline{A}\overline{B}$), whereas the (Q_3, Q_4) branch realizes the second term ($\overline{A}B$). Note also the need for two additional inverters to generate \overline{A} and \overline{B} .

As for synthesizing the PDN, we can obtain it as the dual network of the PUN in Fig. 10.15(a). Alternatively, we can develop an expression for \overline{Y} and use it to synthesize the PDN. Leaving the first approach for the reader to do as an exercise, we shall give the direct synthesis approach. DeMorgan's law can be applied to the expression in Eq. (10.25) to obtain \overline{Y} as

$$\overline{Y} = \overline{AB} + \overline{A}\overline{B} \quad (10.26)$$

The corresponding PDN will be as in Fig. 10.15(b), which shows the CMOS realization of the exclusive-OR function except for the two additional inverters. Note that the exclusive-OR requires 12 transistors for its realization, a rather complex network. Later, in Section 10.5, we shall view a simpler realization of the XOR employing a different form of CMOS logic.

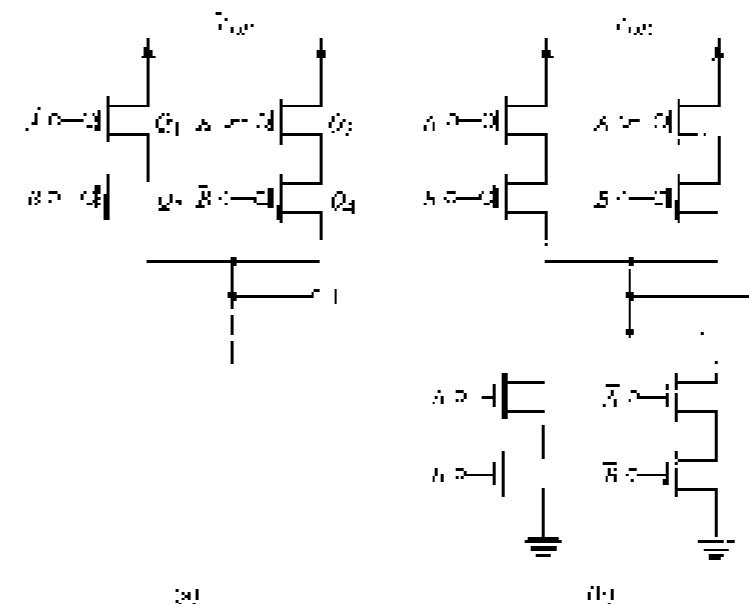


FIGURE 10.15 Realization of the exclusive-OR (XOR) function: (a) The PUN synthesized directly from the expression in Eq. (10.25); (b) The complete XOR realization utilizing the PUN in (a), and a PDN that is synthesized directly from the expression in Eq. (10.26). Note the two inverter blocks shown that are needed to implement the unplemented variables. As we see, the total XOR realization of the PUN and the PDN and their networks; however, a realization with only one network is possible (see Problem 10.27).

Another interesting observation follows from the circuit in Fig. 10.15(b). The PDN and the PUN here are not dual networks. Indeed, duality of the PDN and the PUN is not a necessary condition. Thus, although a dual of PDN (or PUN) can always be used for PUN (or PDN), the two networks are not necessarily dual.

10.3.7 Summary of the Synthesis Method

1. The PDN can be most directly synthesized by expressing \bar{Y} as a function of the *uncomplemented* variables. If complemented variables appear in this expression, additional inverters will be required to generate them.
2. The PUN can be most directly synthesized by expressing \bar{Y} as a function of the *complemented* variables and then applying the uncomplemented variables to the gates of the PMOS transistors. If uncomplemented variables appear in the expression, additional inverters will be needed.
3. The PDN can be obtained from the PUN (and vice versa) using the duality property.

10.3.8 Transistor Sizing

Once a CMOS gate circuit has been generated, the only significant step remaining in the design is to decide on W/L ratios for all devices. These ratios generally are selected to provide the gate with current driving capability at both directions equal to that of the basic inverter. The reader will recall from Section 10.2 that for the basic inverter design, we denoted $(W/L)_0 = n$ and $(W/L)_0 = p$, where n is usually 1.5 to 2 and, for a matched design, $p = (\mu_0/\mu_s)n$. Thus, we wish to select individual W/L ratios for all transistors in a logic gate so that the PDN should be able to provide a capacitor discharge current ten times equal to that of an NMOS transistor with $W/L = n$, and the PUN should be able to provide a charging current of four times equal to that of a PMOS transistor with $W/L = p$. This will guarantee a *worst-case* gate delay equal to that of the basic inverter.

In the preceding narration, the idea of "worst case" should be emphasized. It means that in deciding on device sizing, we should find the input combinations that result in the lowest output current and then choose sizes that will make this current equal to that of the basic inverter. Before we consider examples, we need to address the issue of determining the correct driving capability of a circuit consisting of a number of MOS transistors. In other words, we need to find the equivalent W/L ratio of a network of MOS transistors. Toward that end, we consider the parallel and series connection of MOSFETs and find the equivalent W/L ratios.

The derivation of the equivalent W/L ratio is based on the fact that the on-resistance of a MOSFET is inversely proportional to W/L . Thus, if a network of MOSFETs having ratios of $(W/L)_1, (W/L)_2, \dots$ are connected in series, the equivalent series resistance obtained by adding the on-resistances will be

$$\begin{aligned} R_{\text{series}} &= r_{\text{on},1} + r_{\text{on},2} + \dots \\ &= \frac{\text{constant}}{(W/L)_1} + \frac{\text{constant}}{(W/L)_2} + \dots \\ &= \text{constant} \left[\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \dots \right] \\ &= \frac{\text{constant}}{W/L_{\text{eq}}} \end{aligned}$$

¹ For static conditions, the total effective capacitance C of the logic gate is the same as that of the inverter. In actual practice, the value of C will be larger, especially at the fan-in extremes.⁴

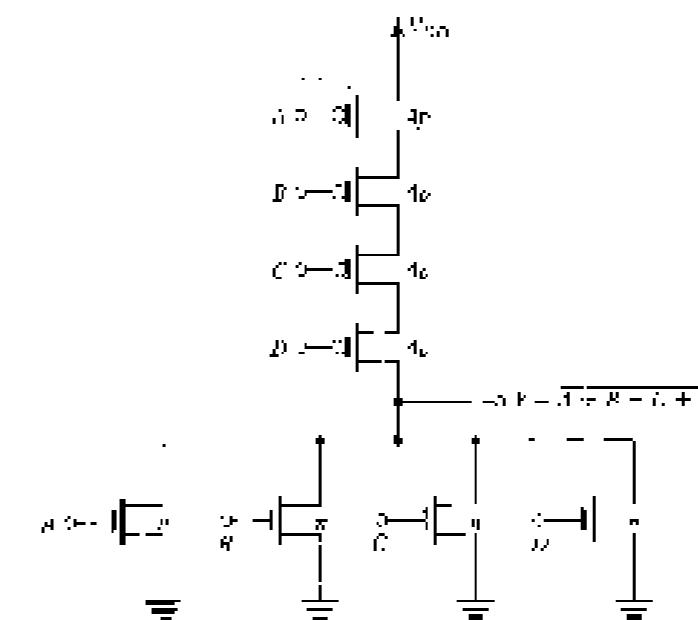


FIGURE 10.16 Proper transistor sizing for a four-input NOR gate. Note that n and p denote the (W/L) ratios of Q_0 and Q_1 , respectively, of the basic inverter.

resulting in the following expression for $(W/L)_{\text{eq}}$ for transistors connected in series:

$$(W/L)_{\text{eq}} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \dots} \quad (10.27)$$

Similarly, we can show that the parallel connection of transistors with W/L ratios of $(W/L)_1, (W/L)_2, \dots$ results in an equivalent W/L of

$$(W/L)_{\text{eq}} = (W/L)_1 + (W/L)_2 + \dots \quad (10.28)$$

As an example, two identical MOS transistors with individual W/L ratios of 4 result in an equivalent W/L of 2 when connected in series and of 8 when connected in parallel.

As an example of proper sizing, consider the four-input NOR in Fig. 10.16. Here, the worst case (the lowest current for the PDN) is observed when only one of the NMOS transistors is conducting. We therefore select the W/L of each NMOS transistor to be exactly that of the NMOS transistor of the basic inverter, namely, n . For the PUN, however, the worst-case situation (and indeed the only one) is when all inputs are low and the four series PMOS transistors are conducting. Since the equivalent W/L will be one-quarter of that of each PMOS device, we should select the W/L ratio of each PMOS transistor to be four times that of Q_0 of the basic inverter, that is, $4n$.

As another example, we show in Fig. 10.17 the proper sizing for a four-input NAND gate. Comparison of the NAND and NOR gates in Figs. 10.16 and 10.17 indicates that because p is usually two to three times n , the NOR gate will require much greater area than the NAND gate. For this reason, NAND gates are generally preferred for implementing combinational logic functions in CMOS.

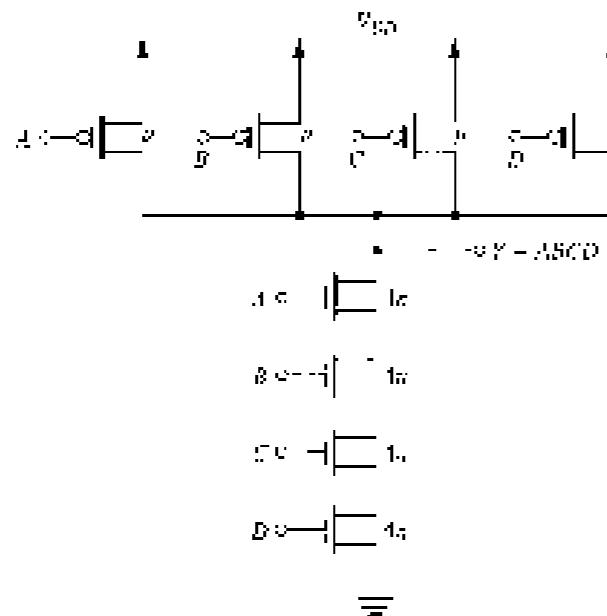


FIGURE 10.17 Power transistor sizing for a two-input NOR gate. Here m_a and n denote the W/L ratios of Q_1 and Q_2 , respectively, of the logic inverter.

- Provide appropriate W/L ratios for the logic circuit shown in Fig. 10.18. Assume that for the basic inverter $w = 1 \mu\text{m}$ and $n = 5$ and that the channel length is $0.25 \mu\text{m}$.

Solution

Refer to Fig. 10.18, and consider the PDN first. We note that the worst case occurs when Q_{10} is on and either Q_{11} or Q_{12} is on. That is, in the worst case, we have two transistors in series. Therefore, we select each of Q_{10} , Q_{11} , and Q_{12} to have twice the width of the w channel devices in the basic inverter, thus

$$Q_{10}: W/L = 2w = 2 = 0.35/0.25$$

$$Q_{11}: W/L = 2w = 2 = 0.75/0.25$$

$$Q_{12}: W/L = 2w = 2 = 0.75/0.25$$

For transistor Q_{13} , select W/L to be equal to that of the w -channel device in the basic inverter:

$$Q_{13}: W/L = n = 5 = 0.375/0.25$$

Next, consider the PDN. Here, we see that in the worst case, we have three transistors in series (Q_{21} , Q_{22} , and Q_{23}). Therefore, we set the W/L ratio of each of these to be three times that of Q_{13} in the basic inverter, that is, $3n$, thus

$$Q_{21}: W/L = 3n = 15 = 0.375/0.25$$

$$Q_{22}: W/L = 3n = 15 = 0.375/0.25$$

$$Q_{23}: W/L = 3n = 15 = 0.375/0.25$$

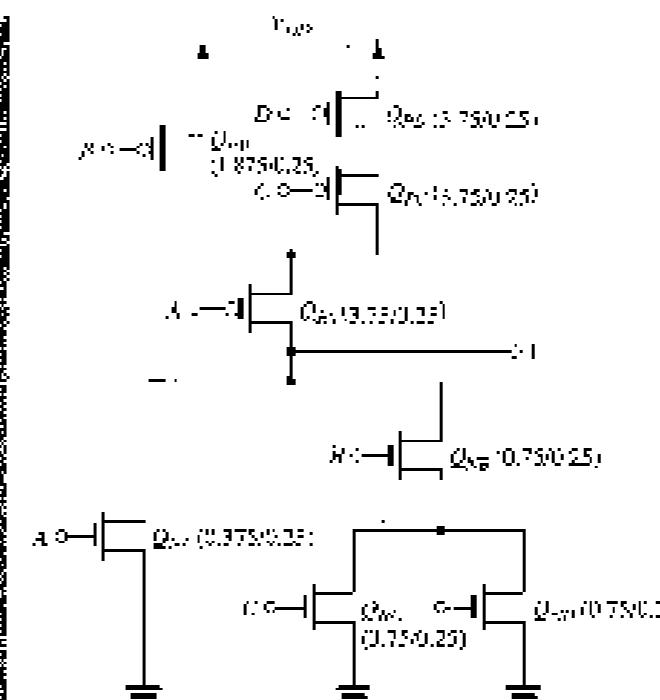


FIGURE 10.18 Logic circuit for Example 10.2.

Finally, the W/L ratio for Q_{14} should be selected so that the equivalent W/L of the series combination of Q_{10} and Q_{11} should be equal to n . It follows that for Q_{14} the ratio should be $1.5p$,

$$Q_{14}: W/L = 1.5p = 7.5 = 0.875/0.25$$

Figure 10.19 shows the circuit with the transistor sizes indicated.

10.3.9 Effects of Fan-In and Fan-Out on Propagation Delay

Each additional input to a CMOS gate requires two additional transistors (one NMOS and one PMOS). This is in contrast to other forms of MOS logic, where each additional input requires only one additional transistor. The additional transistor in CMOS not only increases the chip area but also increases the total effective capacitance per gate and, in turn, increases the propagation delay. The size-scaling method described earlier can compensate for some of the increase in t_{pd} . Specifically, by increasing device size, we are able to preserve the current-driving capability. However, the capacitance C increases because of both the increased number of transistors and the increase in device size. Thus, t_{pd} will still increase with fan-in... but has imposed a practical limit on the fan-in of any CMOS gate to about 4. If a higher number of inputs is required, then "clever" logic design should be adopted to realize the given Boolean function with gates of no more than four inputs. This would usually mean an increase in the number of cascaded stages and thus an increase in delay. However, such an increase in delay can be less than the increase due to the large fan-in (see Problem 10.36).

An increase in a gate's fan-out adds directly to its load capacitance and, thus, increases its propagation delay.

Thus although CMOS has many advantages, it does suffer from increased circuit complexity when the fan-in and fan-out are increased, and from the corresponding effects of this complexity on both chip area and propagation delay. In the following two sections we shall study some simplified forms of CMOS logic that attempt to reduce this complexity, although at the expense of some loss of the advantages of basic CMOS.

EXERCISE

- 10.4 A metal-junction diode, with $L = 0.5 \text{ nm}$, $\kappa = 1.5 \times 10^{-3} \text{ eV nm}^{-1}$, gives about 1000 times more current at 100 mV than at 0 mV. Calculate the relative area and the two Miller-Mössbauer factors between 100 mV and 0 mV.

Note: $N_A N_D / \text{Area} = 2.5 \times 10^{15} \text{ cm}^{-2}$.

10.5 For the same NMOS device as in Exercise 10.1 find the ratio of the maximum drain current and the average drain current for an input voltage of 0.1 V. Assume that the carrier mobility is constant.

10.4 PSEUDO-NMOS LOGIC CIRCUITS

As explained in Section 10.3, despite its many great advantages, CMOS suffers from increased area, and correspondingly increased capacitance and delay, as the logic gates become more complex. For this reason, designers of digital integrated circuits have been searching for forms of CMOS logic circuits that can be used to supplement the complementary-type circuits studied in Sections 10.2 and 10.3. These forms are not intended to replace complementary CMOS but rather to be used in special applications for special purposes. We shall examine two such CMOS logic styles in this and the following section.

10.4.1 The Pseudo-NMOS Inverter

Figure 20.14(c) shows a modified form of the CMOS inverter. Here, only Q_1 is driven by the input voltage while the gate of Q_2 is grounded; node Q_1 acts as an active load for Q_2 . Even before we examine the operation of this circuit in detail, an advantage over complementary CMOS is obvious. Each input must be connected to the gate of only one transistor or, alternatively, only one additional transistor (an NMOS) will be needed for each additional gate input. Thus the area and delay penalties arising from increased fan-in in a complementary CMOS gate will be reduced. This is indeed the motivation for exploring this modified inverter circuit.

The inverter circuit of Fig. 10.19(a) resembles other forms of NMOS logic that consist of a driver transistor (Q_1) and a load resistor (in this case, Q_2); hence the name pseudo-NMOS. For comparison purposes, we shall briefly mention two older forms of NMOS logic. The earliest form, popular in the mid-1970s, utilized an enhancement-mode (or the load element) in a topology whose basic inverter is shown in Fig. 10.19(b). Enhancement-load NMOS logic circuitry suffered from a relatively small logic swing, small noise margins, and high static power dissipation. For these reasons, this logic-circuit technology is now virtually obsolete. It was replaced in the late 1970s and early 1980s with depletion-load NMOS circuits, in which a depletion NMOS transistor with its gate connected to its source is used as the load element. The topology of the basic depletion-load inverter is shown in Fig. 10.19(c).

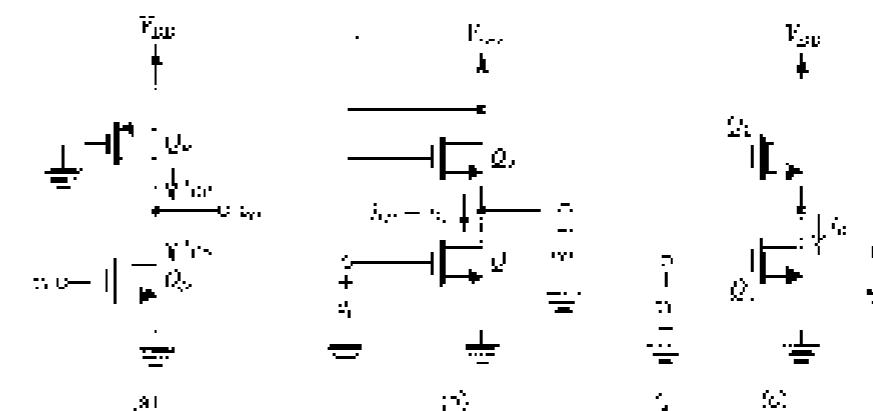


FIGURE 10.19 (a) The present NMOS logic inverters. (b) The older compensated NMOS inverter. (c) The uncompensated NMOS inverter.

It was initially expected that the depletion NMOS with $V_{GS} = 0$ would operate as a constant current source and would thus provide an excellent load element.¹ However, it was quickly realized that the body effect in the depletion transistor causes its I_D characteristic to deviate considerably from that of a constant-current source. Nevertheless, depletion-load NMOS circuits feature significant improvements over their enhancement-load counterparts, enough to justify the extra processing step required to fabricate the depletion devices. Namely, ion-implanting the channel. Although depletion-load NMOS has been virtually replaced by CMOS, one can still see some depletion-load circuits in specialized applications. We will not study depletion-load NMOS logic here (the interested reader can refer to the third edition of this book).

The present NMOS Inverter that we are about to study is similar to depletion-load NMOS but with rather improved characteristics. It also has the advantage of being directly compatible with complementary CMOS circuitry.

12.4.1 Static Characteristics

The static characteristics of the pseudo-NMOS inverter can be derived in a manner similar to that used in complementary CMOS. In bold font code, we note that the drain currents of G_1 and G_2 are given by

$$(\mu_s - V) \eta = V \eta^2, \quad \text{for } \mu_s > V, \quad (\text{saturation}) \quad (10.29)$$

$$i_{\alpha} = k_{\alpha}/(\eta_0 - V_0 \rho_{\alpha} - \frac{1}{2} \dot{\rho}_{\alpha}^2), \quad (\text{at } \eta_0 \leq \eta \leq \eta_0 + \delta), \quad (11.32)$$

$$\langle \rho_{\text{eff}} \rangle = \delta V_0 / (V_{\text{eff}} - V_{\text{ext}})^2 \quad (\text{for } V_{\text{ext}} < V_{\text{eff}} \text{ (saturation)}) \quad (10.3)$$

$$I_{\text{eff}} = k_B \left[(V_{\text{eff}} - V_{\text{c}}) (V_{\text{eff}} - v_{\text{c}}^2) - \frac{1}{2} (V_{\text{eff}} - v_{\text{c}})^2 \right], \quad \text{for } v_{\text{c}} > V_{\text{c}} \quad (\text{inside}) \quad (10.32)$$

where we have assumed that $V_{ij} = -V_{ji} = V_i$, and have used $k_x = k_x^0(\phi/2)_0$ and $k_y = k_y^0(\phi'/2)_0$ to simplify notation.

A constant-current load provides a capacitor charging current that does not diminish as the voltage V_{DC} increases. This is the case with a resistive load. Thus the value of t_{cap} obtained with a constant-current load is significantly less than that obtained with a resistive load (see Problem 10.38). On the other hand, a resistor is simply out of the question because of the way it gets all current; it would always trip before any of the capacitors of the parallel bank.

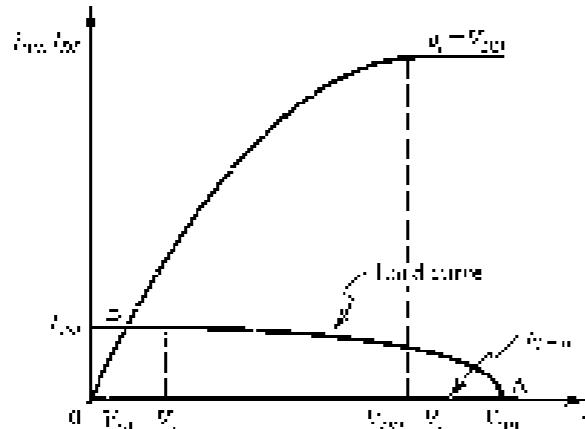


FIGURE 10.20 Graphical construction to determine the VTC of the inverter (Fig. 10.19).

To obtain the VTC of the inverter, we superimpose the load curve represented by Eqs. (10.31) and (10.32) on the $i_{DS}-v_D$ characteristics of Q_2 , which can be relabeled as $i_{DS}-v_D$ and drawn for various values of $v_{GS} - v_T$. Such a graphical construction is shown in Fig. 10.20 where, to keep the diagram simple, we show the Q_2 curves for only the two extreme values of v_G , namely, 0 and V_{DD} . Two observations follow.

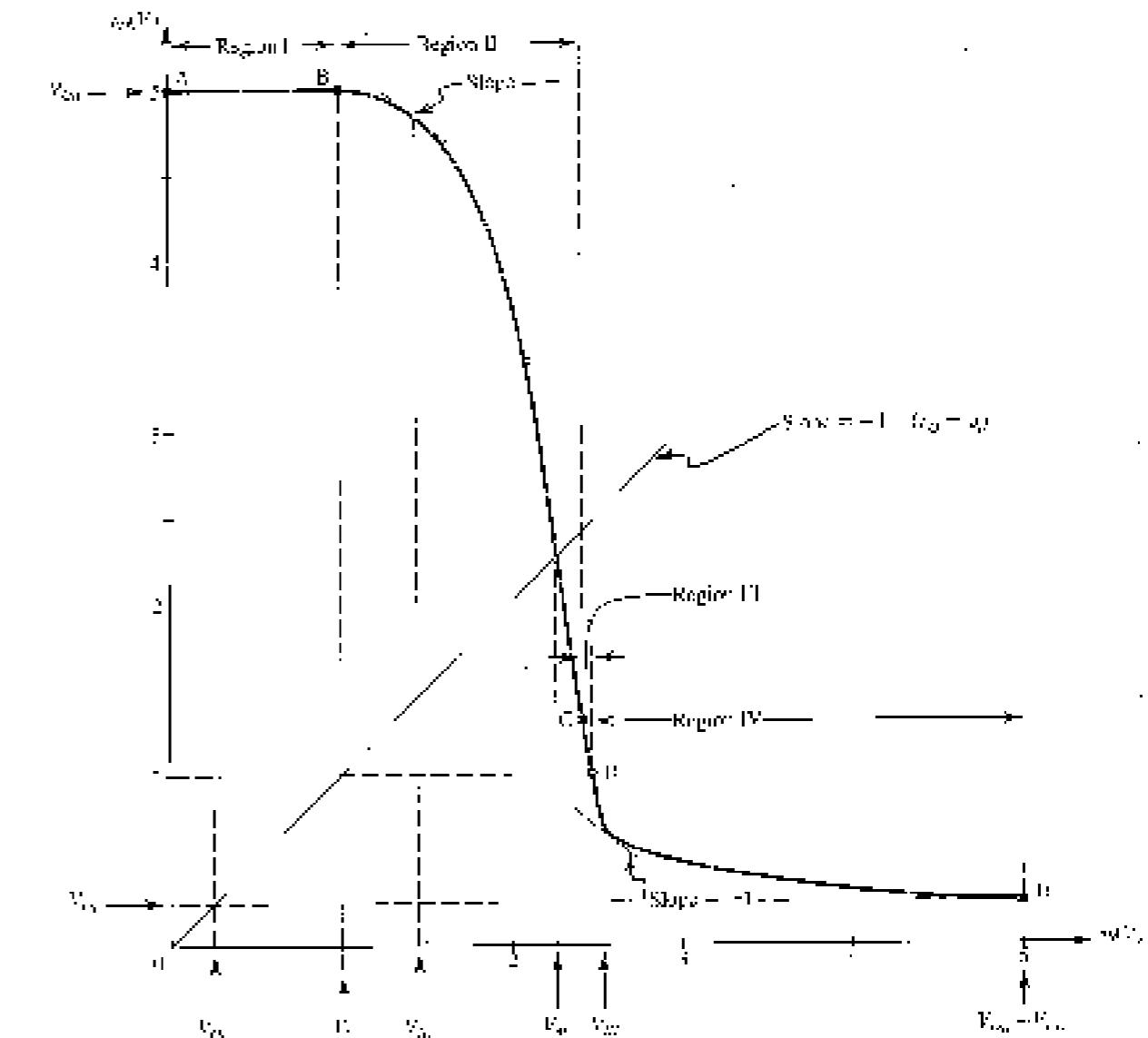
1. The load curve represents a much lower saturation current (Eq. 10.31) than is represented by the corresponding curve for Q_1 , namely, that for $v_G = V_{DD}$. This is a result of the fact that the pseudo-NMOS inverter is usually designed so that k is greater than k_p by a factor of 4 to 10. As we will show shortly, this inverter is of the so-called rat-tail type,³ and the ratio $\kappa = L_s/L_d$ determines all the breakdowns of the VTC, that is, V_{DS}, V_{GS}, V_{ds} , and so on, and thus determines the noise margins. Selection of a relatively high value for κ reduces V_{DS} and widens the noise margins.
2. Although one tends to think of Q_2 as acting as a constant-current source, it actually operates in saturation for only a small range of v_D , namely, $v_D \leq V_T$. For the remainder of the v_D range, Q_2 operates in the triode region.

Consider first the two extreme cases of v_G . When $v_G = 0$, Q_1 is cut off and Q_2 is operating all the triode region, though with zero current and zero drain-source voltage. Thus the operating point is that labeled A in Fig. 10.20, where $v_D = 0$, $i_{DS} = I_{DS,0}$, the static current is zero, and the static power dissipation is zero. When $v_G = V_{DD}$, the inverter will operate at the point labeled B in Fig. 10.20. Observe that unlike coupled-unity CMOS, here $I_{DS,0}$ is not zero, an obvious disadvantage. At other drain voltages v_D that the gate controls current (I_{DS}) in the low-output state, and thus there will be static power dissipation ($P_D = I_{DS} \times V_{DD}$).

10.4.5 Derivation of the VTC

Figure 10.21 shows the VTC of the pseudo-NMOS inverter. As indicated, it has four distinct regions, labeled I through IV, corresponding to the different combinations of possible modes

³For the NMOS inverter, I_{DS} depends on the ratio of the transconductance parameters of the devices, that is, on the ratio $(\mu N^2 L_s)/(\mu P^2 L_d)$, (μ_N/μ_P) . Since $\mu_N > \mu_P$, therefore known as reduced logic circuits, unique to the CMOS logic family, the net form κ is dependent and can therefore be controlled.

FIGURE 10.21 VTC for the pseudo-NMOS inverter. This curve is plotted for $V_{DD} = 5$ V, $V_g = V_s = 1$ V, and $\kappa = 9$.

of operation of Q_2 and Q_1 . The four regions, the corresponding current modes of operation, and the conditions that define the regions are listed in Table 10.1. We can utilize the information in this table together with the device equations given in Eqs. (10.29) through (10.32) to derive expressions for the various segments of the VTC and, in particular, for the important parameters that characterize the static operation of the inverter.

■ Region I (segment AB):

$$v_D = V_{DS} - V_{DD} \quad (10.33)$$

Table 10.1 Regions of Operation of the Pseudo-NMOS Inverter

Region	Segment of VTC	Q_h	Q_l	Condition
I	AB	On/off	Triode	$v_o < V_t$
II	BC	Saturation	Triode	$v_o \geq v_d + V_t$
III	CD	Triode	Triode	$V_t \leq v_o \leq v_d + V_t$
IV	DE	Triode	Saturation	$v_o \geq V_d$

■ Region II (segment BC)

Equating i_{dA} from Eq. (10.29) and i_{ds} from Eq. (10.32) together with substituting $k_s = k_{pL}$ and with some rearrangements, we obtain

$$v_o - V_t = \frac{1}{2}(V_{DD} - V_t)^2 \cdot r(v_t - V_t)^2 \quad (10.43)$$

The value of V_{DD} can be obtained by differentiating this equation and substituting $dv_{DD}/dv_t = -1$ and $v_t = V_{DD}$:

$$V_{DD} = V_t + \frac{V_{DD} - V_t}{\sqrt{r^2 + 1}} \quad (10.44)$$

The threshold voltage V_t for V_{DD} is by definition the value of v_t for which $v_o = v_d$:

$$V_t = v_d - \frac{V_{DD} - V_d}{\sqrt{r + 1}} \quad (10.45)$$

Finally, the end of the region II segment (point C) can be found by substituting $v_o = v_d + V_t$ in Eq. (10.24), the condition for Q_h leaving saturation and entering the triode region.

■ Region III (segment CD)

This is a short segment that is not of great interest. Point D is characterized by $v_o = V_d$.

■ Region IV (segment DE)

Equating i_{dA} from Eq. (10.30) to i_{ds} from Eq. (10.31) and substituting $k_s = k_{pL}$, results in

$$v_o = (v_t + V_t) - \frac{1}{2}v_t - V_t^2 - \frac{1}{2}(V_{DD} - V_t)^2 \quad (10.46)$$

The value of V_{DD} can be determined by differentiating this equation and setting $dv_{DD}/dv_t = -1$ and $v_t = V_{DD}$:

$$V_{DD} = V_t + \frac{2}{\sqrt{r^2 + 1}}(V_{DD} - V_t) \quad (10.47)$$

The value of V_{DD} can be found by substituting $v_t = V_{DD}$ into Eq. (10.47).

$$V_{DD} = (V_{DD} - V_t) \left[1 + \frac{1}{r^2 + 1} \right] \quad (10.48)$$

The static current conducted by the inverter in the low-output state is found from Eq. (10.7) as

$$I_{dA} = \frac{1}{2}k_s(V_{DD} - V_t)^2 \quad (10.49)$$

Finally, we can use Eqs. (10.35) and (10.39) to determine M_M and Eqs. (10.33) and (10.35) to determine M_M' :

$$\Delta M_s = V_t - (V_{DD} - V_t) \left[1 + \frac{1}{r^2 + 1} + \frac{1}{\sqrt{r^2 + 1}} \right] \quad (10.41)$$

$$\Delta M_s' = (V_{DD} - V_t) \left(1 - \frac{2}{\sqrt{r^2 + 1}} \right) \quad (10.42)$$

As a final reservation, we note that since V_{DD} and V_t are determined by the process technology, the only design parameter for controlling the values of V_{DD} and the noise margins is the ratio r .

10.4.4 Dynamic Operation

Analyzing the inverter's rise time response to determine t_{Rise} with the resistor loaded by a capacitance C is identical to that of the complementary CMOS inverter. The capacitance will be charged by the current i_{dA} ; we can determine an estimate for t_{Rise} by using the average value of i_{dA} over the range of v_t from 0 to $v_t + V_{DD}/2$. The result is the following approximate expression (where we have assumed $V_t \approx 0.2V_{DD}$):

$$t_{Rise} = \frac{1.7C}{k_s V_{DD}} \quad (10.43)$$

The case for the capacitor discharge is somewhat different because the current i_{dA} has to be subtracted from i_{ds} to determine the discharge current. The result is the approximate expression:

$$t_{Fall} = \frac{1.7C}{k_s} - \frac{0.46}{r^2 + 1} V_{DD} \quad (10.44)$$

which, for a large value of r , reduces to

$$t_{Fall} = \frac{1.7C}{k_s V_{DD}} \quad (10.45)$$

Although these are identical formulas to those for the complementary CMOS inverter, the pseudo-NMOS inverter has a special problem: Since k_s is r times smaller than k_{pL} , t_{Rise} will be r times larger than t_{Fall} . Thus the circuit exhibits an asymmetric delay performance. Recall, however, that fast gates with large fan-in, pseudo-NMOS require power transistors and thus C can be smaller than in the corresponding complementary CMOS gate.

10.4.5 Design

The design involves selecting the ratio r and the $t_{Rise/L}$ for one of the transistors. The value of $t_{Rise/L}$ for the other device can then be obtained using r . The design parameters of interest are V_{DD} , M_M , M_M' , I_{dA} , P_{on} , t_{Rise} , and t_{Fall} . Important design considerations are as follows:

1. The ratio r determines all the breakpoints of the VTC. The larger the value of r , the lower V_{DD} is (Eq. 10.39) and the wider the noise margins are (Eqs. 10.41 and 10.42). However, a larger r increases the asymmetry in the dynamic response and, for a given $t_{Rise/L}$, it makes the gate larger. Thus selecting a value for r represents a compromise.

between noise margins on the one hand and circuit area and power on the other. Usually, r is selected in the range 4 to 10.

2. Once r has been determined, a value for $(W/L)_S$, or $(W/L)_D$, can be selected and the other determined. Here, one would select a small $(W/L)_S$ to keep the gate area small and thus obtain a small value for C . Similarly, a small $(W/L)_D$ keeps I_{DS} and P_D low. On the other hand, one would want to select larger (W/L) ratios to obtain low t_{PD} and thus fast response. For usual (high-speed) applications, $(W/L)_S$ is selected so that I_{DS} is in the range of 50 to 100 μA , which for $V_{DD} = 5 \text{ V}$ results in P_D in the range of 0.25 mW to 0.5 mW.

10.4.6 Gate Circuits

Except for the load devices, the pseudo-NMOS gate circuit is identical to the PTN of the complementary CMOS gate. Two-input pseudo-NMOS NOR and NAND gates are shown in Fig. 10.22. Note that each requires two transistors, compared to the eight used in complementary CMOS. In pseudo-NMOS, NOR gates are preferred over NAND gates since the former do not utilize transistors in series, and thus can be designed with minimum-size NMOS devices.

10.4.7 Concluding Remarks

Pseudo-NMOS is particularly suited for applications in which the output remains high most of the time. In such applications, the static power dissipation can be reasonably low (since the gate dissipates static power only in the low-output state). Further, the output transitions that materialize will presumably be high-to-low ones (where the propagation delay can be made as short as necessary). A particular application of this type can be found in the design of address decoders for memory chips (Section 11.2) and in read-only memories (Section 11.6).

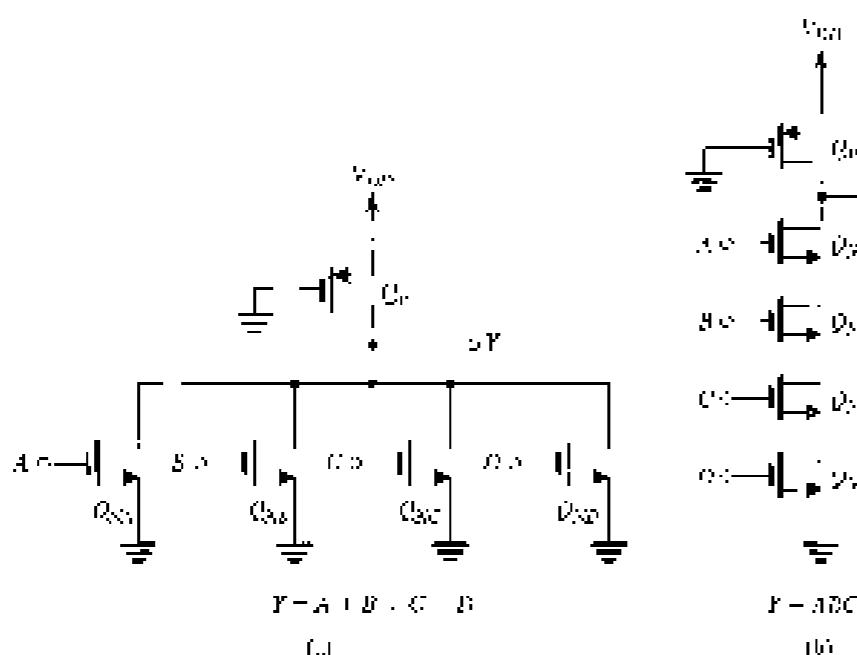


FIGURE 10.22 NOR and NAND gates of the pseudo-NMOS type.

Example 10.10

Consider a pseudo-NMOS inverter fabricated in the CMOS technology specified in Example 10.1 for which $\mu_sC_{ox} = 11.5 \mu\text{A/V}^2$, $\mu_pC_{ox} = 30 \mu\text{A/V}^2$, $V_A = -V_Y = 1.4 \text{ V}$, and $V_{DD} = 2.5 \text{ V}$. Let the W/L ratio of Q_1 be $0.275 \mu\text{m}/0.25 \mu\text{m}$ and $r = 9$. Find:

- V_{IN} , V_{OL} , V_{OH} , NM_N , and NM_P .
- $(W/L)_S$.
- I_{DS} and P_D .
- t_{PD} , t_{Rise} , and t_{Fall} , assuming a total capacitance at the inverter output of 7 fF .

Solution

$$(a) V_{IN} = V_{DD} = 2.5 \text{ V}$$

V_{IN} is determined from Eq. (10.41) as

$$V_{IN} = (2.5 - 0.4)(1 - \frac{1}{r}) = 0.12 \text{ V}$$

V_{OH} is determined from Eq. (10.25) as

$$V_{OH} = 0.4 + \frac{2.5 - 0.4}{\sqrt{9(9+1)}} = 0.23 \text{ V}$$

V_{OL} is determined from Eq. (10.58) as

$$V_{OL} = 0.4 + \frac{2}{\sqrt{2 \times 9}} \times (2.5 - 0.4) = 1.21 \text{ V}$$

V_{IN} is determined from Eq. (10.16) as

$$V_{IN} = 0.4 + \frac{2.5 - 0.4}{\sqrt{9+1}} = 1.06 \text{ V}$$

The noise margins can now be determined as

$$NM_N = V_{OH} - V_{IN} = 0.23 - 0.12 = 0.11 \text{ V}$$

$$NM_P = V_{IN} - V_{OL} = 0.12 - 0.04 = 0.08 \text{ V}$$

Observe that the noise margins are not equal and that NM_P is rather low.

- (b) The (W/L) ratio of Q_1 can be found from

$$\begin{aligned} \frac{\mu_s C_{ox} (W/L)}{\mu_p C_{ox} (W/L)} &= r \\ 11.5 \times \frac{0.275}{30} &= 9 \end{aligned}$$

Thus

$$(W/L)_S = 0.64$$

- (c) The dc current in the low-output state can be determined from Eq. (10.40), as

$$I_{DS} = \frac{1}{2} \times 30 \times 0.04 (2.5 - 0.11)^2 = 12.3 \mu\text{A}$$

The traffic pattern distribution can never be found from

$$P_{\text{eff}} = I_{\text{out}} V_{\text{DD}}$$

(d) The wavefunction expectation value can be found from Eq. (3.43), as

$$t_{\text{FWH}} = \frac{1.3 \times 7 \times 10^{-10}}{3.0 \times 10^{-4} \times 0.6 \times 2.5} = 0.22 \text{ ns}$$

The high to low proportionality factor can be found from Eq.(10) as

$$t_{\text{dyn}} = \frac{7 \times 7 \times 10^{-3}}{115 \times 10^6 \times \frac{0.375}{c_{\infty}} \times 2.5} = 0.03 \text{ s}$$

$\lambda_{\text{eff}} = 1.03$ nm means that class can be determined as

$$t_2 = \frac{1}{2}(0.25 - 0.01) = 0.14 \text{ m}$$

Although the propagation delay is considerably greater than that of the complementary CMOS inverter of Example 10.1, this is not an entirely fair comparison. Recall that the advantage of standard NMOS occurs in gates with three fan-in, not in a single inverter.

卷之三

الآن، في ظل التحديات التي تحيط بالبلدان، يتعين على الجميع العمل معاً لضمان مستقبل أفضل للأجيال القادمة.

10.5 PASS-TRANSISTOR LOGIC CIRCUITS

A conceptually simple approach for implementing logic functions is to use series and parallel combinations of switches that are controlled by input logic variables to connect the input and output nodes (see Fig. 10.23). Each of the switches can be implemented either by a single NMOS transistor (Fig. 10.24a) or by a pair of complementary MOS transistors connected in what is known as the CMOS transmission-gate configuration (Fig. 10.24b). The result is a simple form of logic circuit that is particularly suited for some special logic functions and is frequently used in conjunction with complementary CMOS logic to implement such functions efficiently.

Because this form of logic utilizes MOS transistors in the series path from input to output, it is less susceptible to block signal transmission; it is known as pass-transistor logic (PTL). As mentioned earlier, CMOS transmission gates are frequently employed to implement the switches, giving this logic-circuit form the alternative name, transmission-gate logic. The terms are used interchangeably independent of the actual implementation of the switches.

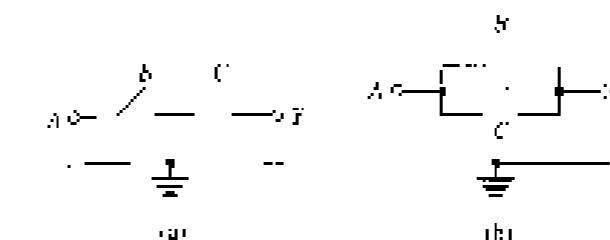


FIGURE 10.23 Conceptual pass transistor logic gates can have switches controlled by the inputs of either (a) or (b), when connected in series. The value between their potentials, which is the voltage applied to variable A , is applied and the output voltage from input B (or $y = g_A(B)$) realize the function $y = A \oplus B$. (b) When the two switches are connected in parallel, the output realized is $y = A(B + C)$.

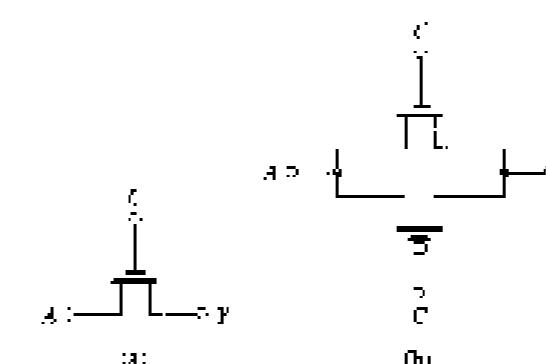


FIGURE 10.24 Two possible implementations of a write-around cache using two memory banks. A two-bus pipelining KVMOS architecture is shown.

Through exceptionally simple, pass-transistor logic elements have to be designed with care. In the following, we shall study the basic principles of the L circuit, design and present examples of its use (see [2]).

12.5.1 An Essential Design Requirement

An essential requirement in the design of PTL circuits is保障 that every circuit node has at all times a low-resistance path to V_{DD} or ground. To appreciate this point, consider the situation depicted in Fig. 10.25(a): A switch S_1 , usually part of a larger PTL network, not shown, is used to form the AND function of its comprising variable B and the variable A available at the output of a CMOS inverter. The output Y of the PTL circuit is shown connected to the input of another inverter. Obviously, if B is high, S_1 closes and $Y = A$. Node Y will then be connected either to V_{DD} (if A is high through S_1) or to ground (if A is low) through Q_1 . But, what happens when B goes low and S_1 opens? Node Y will now become a high-impedance node. If initially, v_Y was zero, it will remain so. However, if initially, v_Y was a high at V_{DD} , this voltage will be maintained by the charge on the parasitic capacitance C_Y , but for only a time: The inevitable leakage currents will slowly discharge C_Y ; v_Y will diminish correspondingly. In any case, the circuit can no longer be considered a static complementary logic circuit.

The problem can be easily solved by establishing for mode 1 a low-resistance path that is activated when B goes low, as shown in Fig. 10.25(a). Here, another switch, S_2 , controlled by A is connected between X and ground. When B goes low, S_2 closes and establishes a low-resistance path between X and ground.

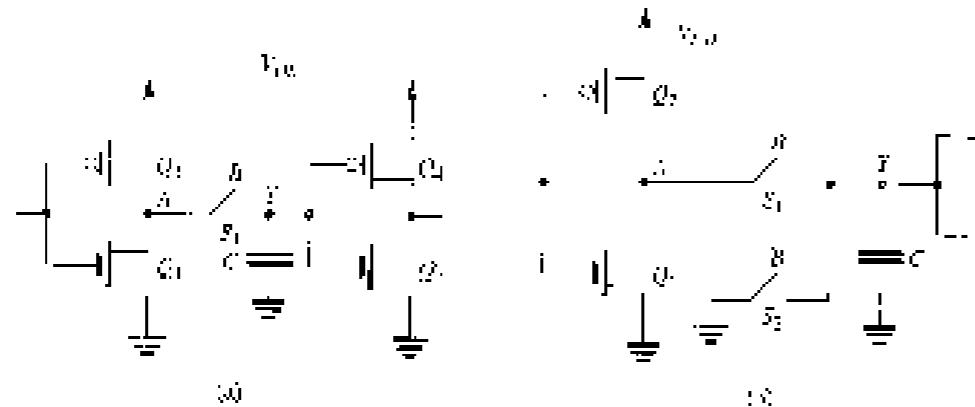


FIGURE 10.25 A simplified logic element of ECL circuit. In fact every node has, in addition, a low-resistance pull-to-either ground or V_{DD} . Such a path does not exist in (a) when it is not on. V_D 's open, it is provided in (b) through switch S_2 .

10.5.2 Operation with NMOS Transistors as Switches

Replacing the switches in a PT₂ circuit with single NMOS transistors results in a simple circuit with small area and small node capacitances. These advantages, however, are obtained at the expense of serious shortcomings in both the static characteristics and the dynamic performance of the resulting circuits. To illustrate, consider the circuit shown in Fig. 10.26, where an NMOS transistor Q is used to implement a switch connecting an input node with voltage v_i and an output node. The total capacitance between the g input node and ground is represented by capacitor C . The switch is shown in the closed state with the control signal applied to its gate being high at V_{DD} . We wish to analyze the operation of the circuit as the input voltage v_i goes high (i.e., $v_i > V_{DD}$) at time $t = 0$. We assume that initially the output voltage v_o is zero and capacitor C is fully discharged.

When v_i goes high, the transistor operates in the saturation mode and delivers a current i_Q to charge the capacitor:

$$i_Q = \frac{1}{2} k_n (V_{DD} - v_i - V_b)^2 \quad (10.46)$$

where $k_n = \mu_n C_s V_t / 2$, and V_b is determined by the body effect since the source is at a voltage v_o relative to the body, thus (see Eq. 4.63)

$$V_b = V_{DD} + \sqrt{v_o + 2\phi_b - 2V_t} \quad (10.47)$$

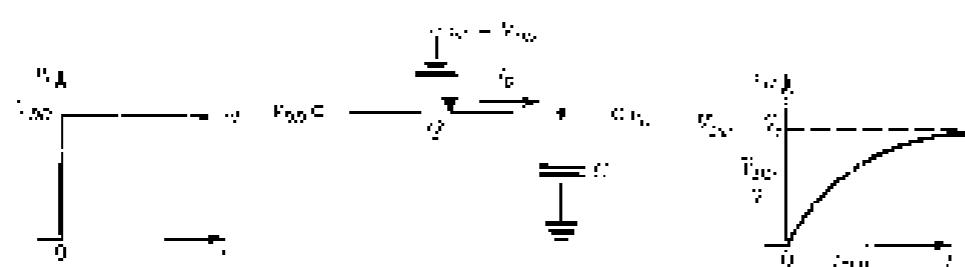


FIGURE 10.26 Operation of the NMOS transistor as switch in the implementation of ECL circuits. This suggests for the case $v_i < V_{DD}$ the switch closed (v_o high) and the input going high ($v_i = V_{DD}$).

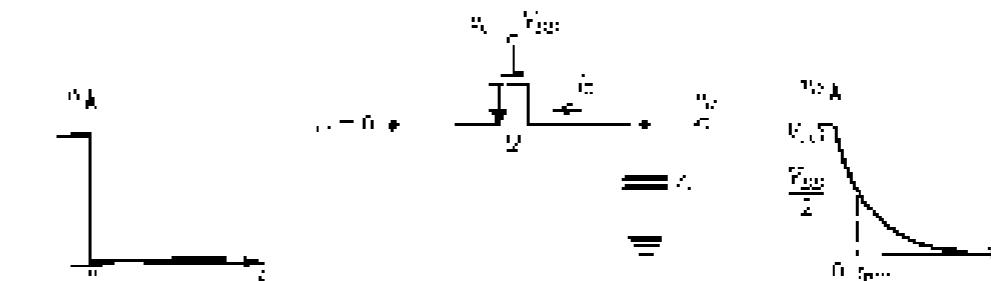


FIGURE 10.27 Operation of the NMOS switch in the fan-out law ($n = 2$). Note that the drain of an NMOS transistor is always higher in voltage than the source (current analogy), the drain and source were interchanged in comparison to (a) and (c) in Fig. 10.26.

Thus, initially (at $t = 0$), $V_b = V_D$ and the current i_Q is relatively large. However, as C charges up and v_o rises, V_b increases (Eq. 10.47) and i_Q decreases. The latter effect is due to both the increase of v_o and in V_b . It follows that the process of charging the capacitor will be relatively slow. More seriously, observe from Eq. (10.46) that i_Q goes to zero when v_o reaches $(V_{DD} - V_b)$. Thus the high output voltage (V_{DD}) will not be equal to V_{DD} taken, it will be lower by V_b , and to make matters worse, the value of V_b can be as high as 1.5 to 2 times V_t !

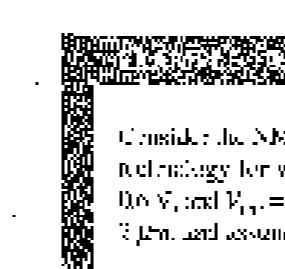
In addition to reducing the gate noise immunity, the low value of V_{DD} (commonly referred to as "speed β ") has another detrimental effect. Consider what happens when the output node is connected to the input of, say, a unity CMOS inverter (as the circuit in Fig. 10.25). The low value of V_{DD} causes Q_1 of the load inverter to conduct. Thus the inverter will have a finite static current and static power dissipation.

The propagation delay (t_{pd}) of the PT₂ core of Fig. 10.25 can be determined as the time for v_o to reach $V_{DD}/2$. This can be calculated using techniques similar to those employed in the preceding sections, as will be illustrated shortly in an example.

Figure 10.27 shows the NMOS switch circuit when v_i is brought down to 0 V. We assume that initially $v_o = V_{DD}$. Thus at $t = 0$, the transistor conducts and operates in the saturation region.

$$i_Q = \frac{1}{2} k_n (V_{DD} - V_b)^2 \quad (10.48)$$

where we note that now the source is now at 0 V (note that the drain and source have interchanged roles); there will be no body effect, and V_b remains constant (Fig. 4.6). As C discharges, v_o increases and the transistor enters the triode region at $v_o = V_{DD} - V_b$. Nevertheless, the capacitor discharges asymptotically until C is fully discharged and $v_o = 0$. Thus, the NMOS transistor provides $v_o > 0$, or a "good 0." Again, the propagation delay t_{pd} can be determined using usual techniques, as illustrated by the following example.



Consider the NMOS transistor switch in the circuit of Figs. 10.26 and 10.27 to be fabricated in a technology for which $k_n C_s = 50 \text{ nA/V}^2$, $\mu_p C_s = 20 \text{ }\mu\text{A/V}^2$, $V_{DD} = 1 \text{ V}$, $\gamma = 0.5 \text{ V}^{-1}$, $\lambda_n = 0.6 \text{ V}$, and $V_{t,n} = 5 \text{ V}$. Let the transistor be of the minimum size for this technology, namely, $4 \text{ }\mu\text{m} \times 2 \text{ }\mu\text{m}$, and assume that the total capacitive load between the output node and ground is $C = 30 \text{ fF}$.

For the case with v_i high (Fig. 10.26), find V_{DD} .

- (c) If the circuit feeds a CMOS inverter whose $(W/L)_p = 2.5$, $(W/L)_n = 0.5 \mu\text{m}/2 \mu\text{m}$, find the static current of the inverter and its power dissipation when its input is at the value found in (b). Also find the inverter output voltage.
- (d) Find i_{off} .
- (e) For the case with i_{off} given here (Fig. 10.27), find $i_{\text{off},\text{avg}}$.
- (f) Find t_{off} .

Solution

(a) Referring Fig. 10.25, V_{off} is the value of v_2 at which Q stops conducting.

$$V_{\text{off}} = V_{\text{DD}} - V_t = 0$$

Thus,

$$V_{\text{DD}} = V_{\text{DD}} - V_t$$

where V_t is the value of the threshold voltage of a source-body-drain diode equal to $V_{\text{DD}}/17$ in Eq. (10.47).

$$\begin{aligned} V_t &= V_{\text{DD}} + \sqrt{V_{\text{DD}} + 2\phi_f} - \sqrt{2\phi_f} \\ &= V_{\text{DD}} + \sqrt{V_{\text{DD}} + V_t - 2\phi_f} - \sqrt{2\phi_f} \end{aligned}$$

Substituting $V_{\text{DD}} = 5$, $\gamma = 0.5$, $V_{\text{DD}} = 5$, and $2\phi_f = 0.6$, we obtain a quadratic equation in V_t , whose solution yields

$$V_t = 1.6 \text{ V}$$

Thus,

$$V_{\text{DD}} = 3.4 \text{ V}$$

Note that this represents a significant loss in signal amplitude.

(b) The n -channel inverter will see an input signal of 3.4 V. Thus, as Q_2 will conduct a current of

$$i_{\text{on}} = \frac{1}{2} \times 20 \times \frac{1}{2}(5 - 3.4 - 1)^2 = 15.4 \mu\text{A}$$

Thus, the static power dissipation of the inverter will be

$$P_S = V_{\text{DD}} i_{\text{on}} = 5 \times 15.4 = 90 \mu\text{W}$$

The output voltage of the inverter can be found by noting that Q_1 will be operating in the triode region, equating its current to that of Q_2 (i.e., 15.4 μA) enables us to determine the output voltage to be 0.38 V.

(c) To determine $i_{\text{off},\text{avg}}$, we need to find the current i_2 at $v_2 = 0$ (where $v_2 = 0$, $V_t = V_{\text{DD}} - 1$ V) and at $i = i_{\text{off},\text{avg}}$ (where $v_2 = 2.5$ V, V_t to be determined), as follows:

$$i_2(0) = \frac{1}{2} \times 20 \times \frac{1}{2}(5 - 1)^2 = 800 \mu\text{A}$$

$$V_t \text{ (at } v_2 = 2.5 \text{ V)} = -(0.5t_c\sqrt{2.5 - 0.5} - \sqrt{0.6}) = 1.49 \text{ V}$$

$$i_2(i_{\text{off},\text{avg}}) = \frac{1}{2} \times 20 \times \frac{1}{2}(5 - 2.5 - 1.49)^2 = 53 \mu\text{A}$$

We can now compute the average discharge current as

$$i_{\text{off},\text{avg}} = \frac{800 + 53}{2} = 425 \mu\text{A}$$

and the time to discharge

$$\begin{aligned} t_{\text{off},\text{avg}} &= \frac{C(V_{\text{DD}}/2)}{i_{\text{off},\text{avg}}} \\ &= \frac{50 \times 10^{-12} \times 2.5}{425 \times 10^{-6}} = 0.29 \text{ ns} \end{aligned}$$

(d) Refer to the circuit in Fig. 10.27. Observe that here, V_t remains constant at $V_t = 1$ V. The drain current $i_d = 0$ is

$$i_d(0) = \frac{1}{2} \times 20 \times \frac{1}{2}(5 - 1)^2 = 800 \mu\text{A}$$

At $t = t_{\text{off}}$, Q will be operating in the triode region, and thus

$$\begin{aligned} i_d(t_{\text{off}}) &= 20 \times \frac{1}{2}(5 - 1) \times 2.5 - \frac{1}{2} \times 2.5^2 \\ &\approx 690 \mu\text{A} \end{aligned}$$

Thus, the average discharge current is given by

$$i_{\text{off},\text{avg}} = \frac{1}{2}(800 + 690) = 745 \mu\text{A}$$

and $t_{\text{off},\text{avg}}$ can be determined as

$$t_{\text{off},\text{avg}} = \frac{50 \times 10^{-12} \times 2.5}{745 \times 10^{-6}} = 0.17 \text{ ns}$$

$$(e) t_{\text{off}} = \frac{1}{2}(t_{\text{off},\text{avg}} + t_{\text{off},\text{avg}}) = \frac{1}{2}(0.29 + 0.17) = 0.23 \text{ ns}$$

Example 10.4 Illustrates clearly the problem of signal-level loss and its deleterious effect on the operation of the succeeding CMOS inverter. Some rather ingenious techniques have been developed to reduce the output load to V_{DD} . We shall briefly discuss two such techniques. One is circuit-based and the other is based on process technology.

The circuit-based approach is illustrated in Fig. 10.28. Here, Q_1 is a pass-transistor controlled by signal A_0 . The output node of the PTL network is connected to the drain of a complementary inverter formed by Q_2 and Q_3 . A PMOS transistor Q_4 , whose gate is controlled by the output voltage of the inverter, $v_{2\text{out}}$, has been added to the circuit. Observe that at the time that the output of the PTL gate, $v_{2\text{out}}$, is low (at ground), $v_{2\text{out}}$ will be high (at V_{DD}), and Q_4 will be off. On the other hand, if $v_{2\text{out}}$ is high but not quite equal to V_{DD} , the output of the

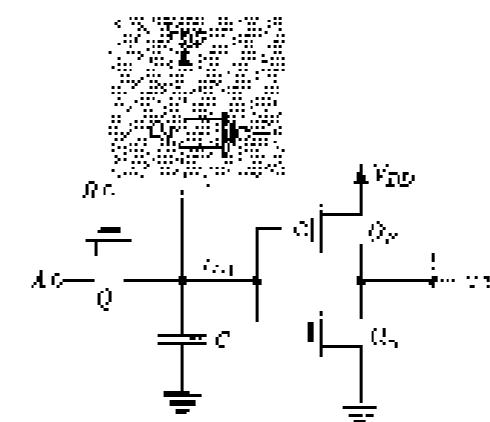


FIGURE 10.28 The use of transistor Q_4 can reduce signal-level loss around the CMOS inverter by biasing the $v_{2\text{out}}$ level produced by Q_2 to V_{DD} .

inverter will be low (or off) and Q_2 will turn on, supplying a current to charge C_{in} to V_{DD} . This process will stop when $v_o = V_{\text{DD}}$, that is, when the output voltage has been restored to its proper level. The "level-restoring" function performed by Q_2 is frequently employed in MOS digital circuit design. It should be noted that although the description of operation is relatively straightforward, the addition of Q_2 creates a "positive-feedback" loop toward the CMOS inverter, and this situation is more involved than it appears, especially during transients. Selection of a R/D ratio for Q_2 is also a somewhat involved process, although normally k_s is selected to be much larger than k_n (say, a third or a fifth as large). Intuitively, this is appealing, for it implies that Q_2 will not play a major role in circuit operation, apart from restoring the level of V_{DD} to V_{DD} , as explained [see Raynor (1967)]. Therefore Q_2 is said to be a "weak PMOS transistor."

The other technique for correcting for the loss of the high-output signal level (V_{DD}) in a technology-based solution is specific, but the loss in the value of V_{DD} is equal to V_{DD} . It follows that we can reduce the loss by using a lower value of V_{DD} for the NMOS switches, and we can eliminate the loss altogether by using devices for which $V_t = 0$. These were discussed above; they can be fabricated by using ion implantation to control the value of V_t and are known as **natural devices**.

10.5.3 The Use of CMOS Transmission Gates as Switches

Great improvements in static and dynamic performance are obtained when the switches are implemented with CMOS transmission gates. The transmission gate utilizes a pair of complementary transistors connected in parallel. It acts as an excellent switch, providing full differential current flow, and it exhibits an on-resistance that remains almost constant for wide ranges of input voltage. These characteristics make the transmission gate not only an excellent switch in digital applications but also an excellent analog switch in such applications as data converters (Chapter 9) and switched capacitor filters (Chapter 12).

Figure 10.29(a) shows the transmission-gate switch in the "on" position with the input, v_i , using $|V_{\text{DD}}| < v_i < 0$. Assuming, as before, that initially the output voltage is zero, we see that Q_2 will be operating in saturation and providing a charging current of

$$I_{\text{DD}} = \frac{2k_s}{L} (V_{\text{DD}} - v_i - V_{\text{DD}})^2 \quad (10.49)$$

where, as in the case of the single NMOS switch, V_{DD} is determined by the body effect:

$$V_{\text{DD}} = V_{\text{DD}} + \sqrt{2q_s(1 + 2q_s)} \quad (10.50)$$

Transistor Q_1 will conduct a diminishing current that reaches zero at $v_i = V_{\text{DD}} - V_{\text{DD}}$. Observe, however, that Q_1 operates with $V_{\text{DD}} = V_{\text{DD}}$ and is initially in saturation,

$$I_{\text{DD}} = \frac{2k_s}{L} (V_{\text{DD}} - |V_{\text{DD}}|)^2 \quad (10.51)$$

where, since the body of Q_1 is connected to V_{DD} , V_{DD} remains constant at the value V_{DD} assumed to be the same value as for the n-channel device. The total capacitor-charging current is, however, I_{DD} , and again, Q_1 will enter the triode region at $v_i = |V_{\text{DD}}|$, but will continue to conduct until C is fully charged and $v_i = V_{\text{DD}} = V_{\text{DD}}$. Thus, the p-channel device will provide the gate with a "spike." The value of v_{DD} can be calculated using usual techniques, where we expect that the result will be additional current available from the PMOS device, for the static value of C , I_{DD} , will be lesser than in the case of the single NMOS switch. Note, however, that adding the PMOS transistor increases the value of C .

When v_i goes low, as shown in Fig. 10.29(b), Q_1 and Q_2 interchange roles. Analysis of the circuit in Fig. 10.29(b) will indicate that Q_1 will cease conduction when v_i falls to $|V_{\text{DD}}|$.

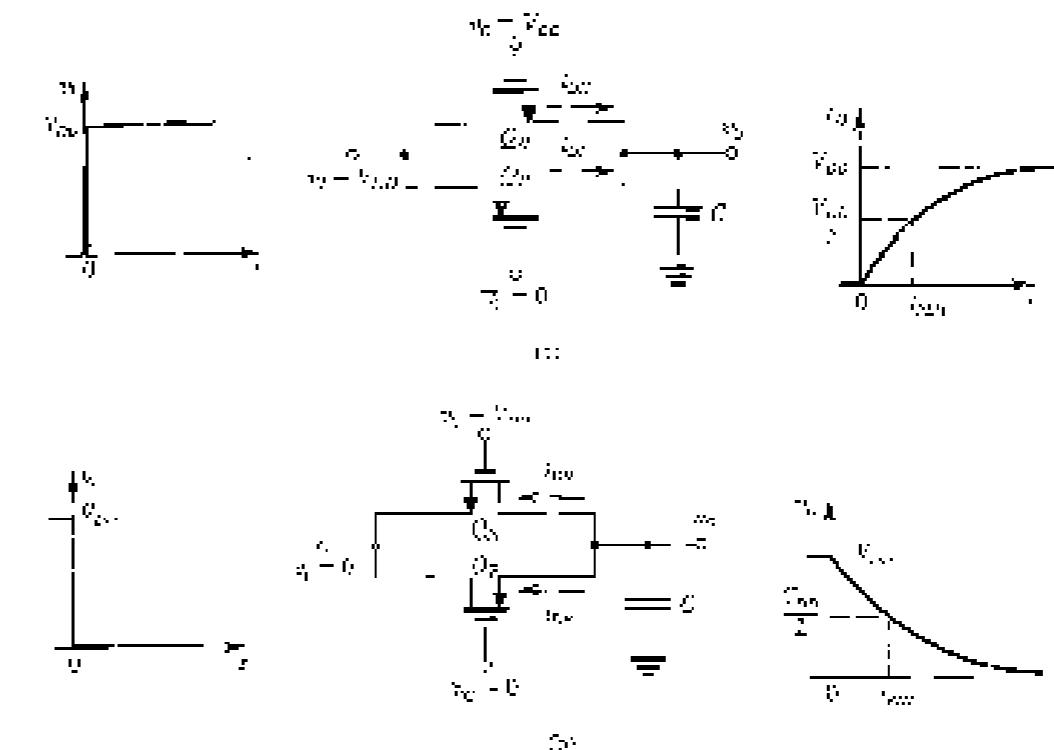


FIGURE 10.29 Operation of the transmission gate as a switch in TTL circuits: (a) v_i high and (b) v_i low.

where $|V_{\text{DD}}|$ is given by

$$V_{\text{DD}} = V_{\text{DD}} + \sqrt{2q_s(L/k_s) - 1} = \sqrt{2q_s} \quad (10.52)$$

Transistor Q_2 , however, continues to conduct until C is fully discharged and $v_i = V_{\text{DD}} = 0$ V, a "good 0."

We conclude that transmission gates provide far superior performance, both static and dynamic, than is possible with simple NMOS switches. The price paid is increased circuit complexity, area, and capacitance.

EXERCISE

- 10.8 If the transmission-gate switch of Fig. 10.29(a) is to have a total on-resistance of 10Ω , what must k_s be? Assume $V_{\text{DD}} = 10$ V and $L = 1 \mu\text{m}$.
 10.9 Design a CMOS inverter using transmission-gate switches. Assume $V_{\text{DD}} = 10$ V and $L = 1 \mu\text{m}$. The design requires the minimum number of transistors. The output voltage should be V_{DD} when $v_i = 0$ and 0 V when $v_i = V_{\text{DD}}$.
 10.10 In the design of the inverter in Exercise 10.9, assume that the inverter is to be used in a logic family with a maximum fanout of 4. The output voltage should be V_{DD} when $v_i = 0$ and 0 V when $v_i = V_{\text{DD}}$.
 10.11 For the inverter designed in Exercise 10.9, find the value of C required to obtain a rise time of 10 ns and a fall time of 10 ns .
 10.12 Find the value of C required to obtain a rise time of 10 ns and a fall time of 10 ns for the inverter in Exercise 10.9, assuming that $k_s = 100 \text{ mA/V}^2$, $k_n = 50 \text{ mA/V}^2$, $V_{\text{DD}} = 10$ V, and $L = 1 \mu\text{m}$.
 10.13 Find the value of C required to obtain a rise time of 10 ns and a fall time of 10 ns for the inverter in Exercise 10.9, assuming that $k_s = 100 \text{ mA/V}^2$, $k_n = 50 \text{ mA/V}^2$, $V_{\text{DD}} = 10$ V, and $L = 1 \mu\text{m}$.
 10.14 Find the value of C required to obtain a rise time of 10 ns and a fall time of 10 ns for the inverter in Exercise 10.9, assuming that $k_s = 100 \text{ mA/V}^2$, $k_n = 50 \text{ mA/V}^2$, $V_{\text{DD}} = 10$ V, and $L = 1 \mu\text{m}$.

10.5.4 Pass-Transistor Logic Circuit Examples

We conclude this section by showing examples of PTL logic circuits. Figure 10.30 shows a PTL realization of a two-to-one multiplexer. Depending on the logic value of C , either A or B is connected to the output Y . The circuit realizes the Boolean function

$$Y = CA + \bar{C}B$$

Our second example is an efficient realization of the exclusive-OR (XOR) function. The circuit, shown in Fig. 10.31, requires four transistors in the transmission gates and another four for the two inverters needed to generate the complements \bar{A} and \bar{B} , for a total of eight transistors. Note that 12 transistors are needed in the realization with complementary CMOS.

Our final PTL example is the circuit shown in Fig. 10.32. It uses NMOS switches with low or zero threshold. Observe that both the input variables and their complements are

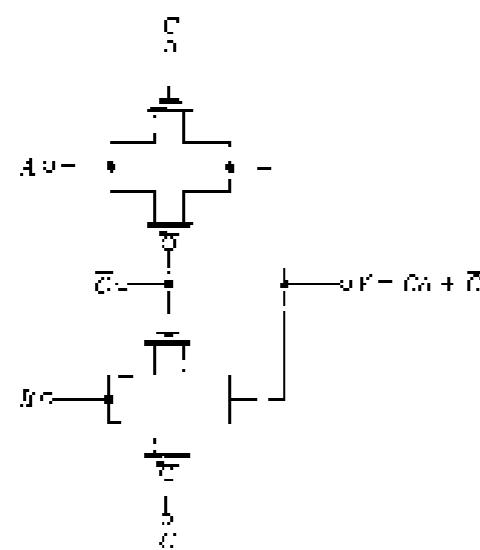


FIGURE 10.30 Realization of a two-to-one multiplexer using pass-transistor logic.

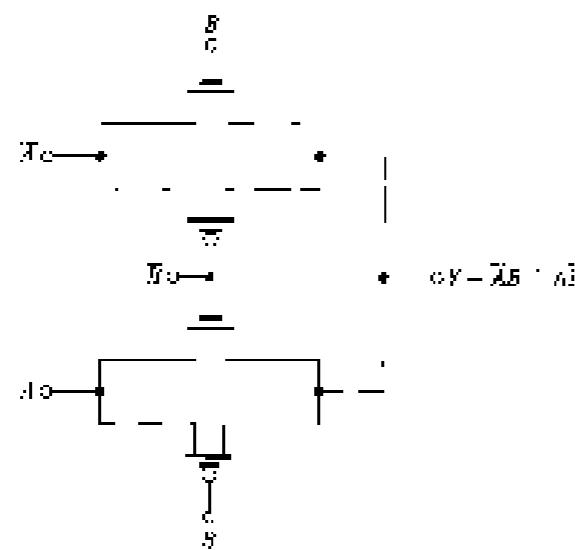


FIGURE 10.31 Realization of the XOR function using pass-transistor logic.

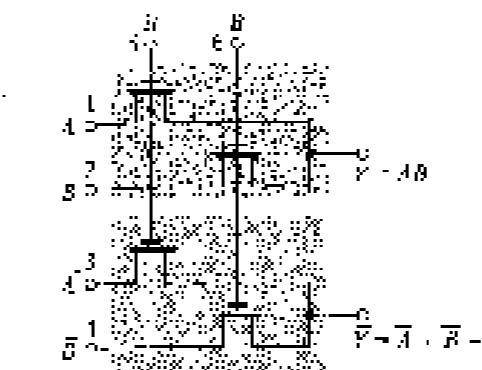


FIGURE 10.32 An example of a pass-transistor logic gate utilizing both the input variables and their complements. This type of circuit is therefore known as complementary pass-transistor logic (CPL). Note that both the output functions are the complement of what is generated.

employed and that the circuit generates both the Boolean function and its complement. This type of circuit is known as complementary pass-transistor logic (CPL). The circuit consists of two identical networks of pass transistors with the corresponding transmission gates controlled by the same signal (B and \bar{B}). The inputs to the PTL, however, are complements \bar{A} and B for the first network, and A and \bar{B} for the second. The circuit shown realizes both the AND and NOR functions.

EXERCISE

- 10.9 Consider the circuit in Fig. 10.31 with the input signals shown in the network for exercise. Find Y and \bar{Y} for each time interval. The signals of terminals A and B are applied at time $t = 0$ and are applied until $t = 1$ (at which time they are removed). At time $t = 1$, the signal at terminal C is changed to \bar{A} , and the signal at terminal D is changed to \bar{B} . At time $t = 2$, the signal at terminal C is changed back to A , and the signal at terminal D is changed back to B .
- (a) If $A = 1$, $B = 0$, $C = 1$, $D = 0$ at the OR output $Y = \bar{A}B + A\bar{B}$, verify $\bar{Y} = 1$.
 (b) Verify $Y = 0$ at the OR output $Y = \bar{A}B + A\bar{B}$ when $A = 0$, $B = 1$, $C = 0$, $D = 1$.
 (c) Verify $Y = 1$ at the OR output $Y = \bar{A}B + A\bar{B}$ when $A = 1$, $B = 1$, $C = 0$, $D = 1$.

10.5.5 A Final Remark

Although the use of zero-threshold devices solves the problem of the loss of signal levels when NMOS switches are used, the switching circuitry can be much more sensitive to noise and other effects, such as leakage currents resulting from subthreshold conduction.

10.6 DYNAMIC LOGIC CIRCUITS

The logic circuits that we have studied thus far are of the static type. In a static logic circuit, every node has, at all times, a low-resistance path to V_{DD} or ground. By the same token, the voltage of each node is well defined at all times, and no node is left floating. Static circuits do not need clocks (i.e., periodic timing signals) for their operation, although clocks may be present for other purposes. In contrast, the dynamic logic circuits we are about to discuss rely on the storage of signal voltages on parasitic capacitances at certain circuit nodes. Since charge will leak away with time, the circuit needs to be periodically refreshed; thus the presence of a clock with a certain specified minimum frequency is essential.

To place dynamic logic circuits into perspective, let's take stock of the various logic circuit styles we have studied. Complementary CMOS excels in nearly every performance category: It is easy to design, has the maximum possible logic swing, is robust from noise immunity standpoint, dissipates no static power, and can be designed to provide equal low-to-high and high-to-low propagation delays. Its main disadvantage is the requirement of two transistors for each additional logic level, which for high fan-in gates can make the chip area large and increase the total capacitance and, correspondingly, the propagation delays and the dynamic power dissipation. Pseudo-NMOS requires the number of required transistors at the expense of static power dissipation. Pass-transistor logic can result in simple small-area circuits but is limited to special applications and requires the use of complementary inverters to restore a given level, especially when the switches are simple NMOS transistors. The dynamic logic techniques studied in this section maintain the low device count of pseudo-NMOS while reducing the static power dissipation to zero. As will be seen, this is achieved at the expense of more complex and less robust design.

10.6.1 Basic Principle

Figure 10.33(a) shows the basic dynamic logic gate. It consists of a pull-down network (PDN) that realizes the logic function in exactly the same way as the PDN in a complementary CMOS gate or a pseudo-NMOS gate. Here, however, we have two switches in series that are periodically activated by the clock signal ϕ whose waveform is shown in Fig. 10.33(b). When ϕ is low, Q_1 is turned on, and the circuit is said to be in the setup or precharge phase. When ϕ is high, Q_1 is off, and Q_2 turns on, and the circuit is in the evaluation phase. Finally, note that C_1 denotes the total capacitive load between the output node and ground.

During precharge, Q_1 conducts the charge current I_1 , so that at the end of the precharge interval, the voltage at Y is equal to V_{DD} . Also during precharge, the inputs A , B , and C are allowed to change and settle to their primary values. Observe that because Q_1 is off, no path to ground exists.

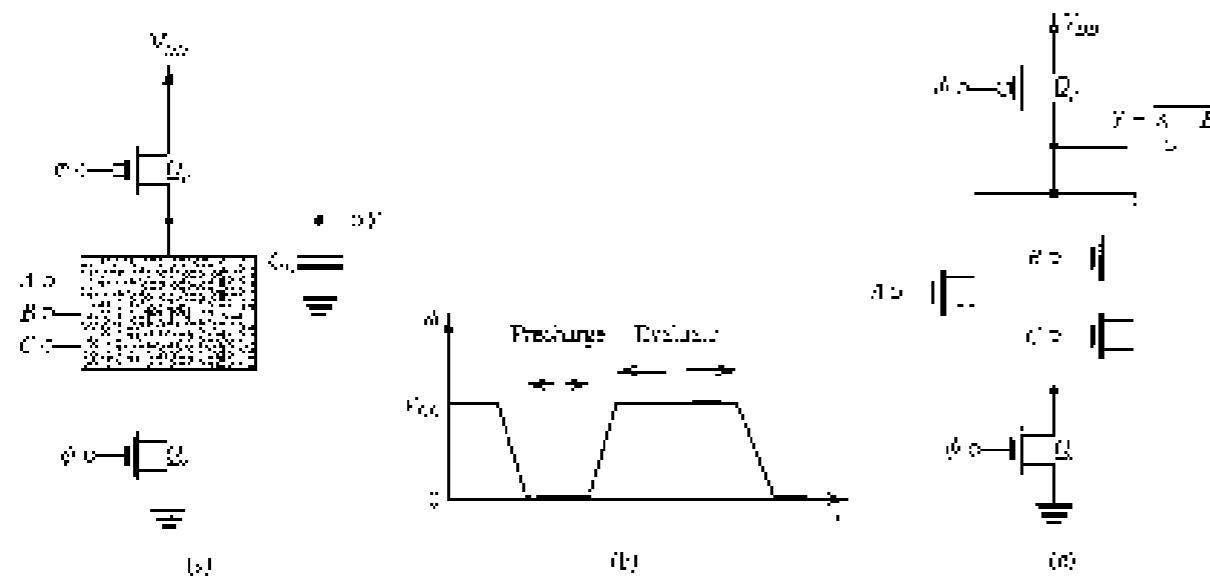


FIGURE 10.33 (a) Block diagram of dynamic NMOS logic; (b) waveform of the clock needed to operate the dynamic logic circuit; (c) logic symbol.

During the evaluation phase, Q_1 is off and Q_2 is turned on. Now, if the input combination is such that it corresponds to a logic output, the PDN does not conduct just as in a complementary CMOS gate and the output remains high at V_{DD} , thus $V_{DD} = V_{out}$. Observe that no low-to-high propagation delay is required, thus $t_{PHL} = 0$. On the other hand, if the combination of inputs is one that corresponds to a low output, the n-type NMOS transistors in the PDN will conduct and establish a path between the output node and ground through the on transistor Q_2 . Thus C_1 will be discharged through the PDN, and the voltage at the output node will reduce to $V_{DD} - V_s$. The high-to-low propagation delay t_{PLH} can be calculated in exactly the same way as for a complementary CMOS circuit except that here we have an additional transistor, Q_2 , in the series path to ground. Although this will increase the delay slightly, the increase will be more than offset by the reduced capacitance at the output node as a result of the absence of the PDN.

As an example, we show in Fig. 10.33(c) the circuit that realizes the function $F = \overline{A} + \overline{BC}$. Sizing of the PMOS transistors often follows the same procedure employed in the design of static CMOS. For Q_1 , we select a W/L ratio large enough to ensure that C_1 will be fully charged during the precharge interval. The size of Q_2 , however, should be small so that the capacitance C_1 will not be increased significantly. This is a raceless form of MOS logic, where the output levels do not depend on the transistors' W/L ratios.

EXERCISES

- 10.16 Consider the dynamic NMOS inverter shown in Fig. 10.33. The PMOS transistors have a W/L ratio of 100 and $V_{DD} = 5\text{ V}$. The NMOS transistors have a W/L ratio of 10. The clock frequency is 100 MHz. The output voltage is measured to be 2.5 V. Find the value of C_1 assuming the current in Q_1 is 4.5 mA and the output voltage is approximately 2.5 V ($C_1 = C_s/0.33 + 0.17$), where C_s is the average value of the parasitic capacitors.
- Ans. $\$30.24$; 112 aF ; 2.5 V
- 10.17 Next consider the inverter of the high-to-low propagation delay. If the switching time is 10 ns, find the W/L ratio of the five-NMOS transmission gate. Then, find the driving capability of Q_1 at $V_{DD} = 2.5\text{ V}$. Finally, use the inverter of Exercise 10.16 to compute the total delay of the inverter.
- Ans. 17.7 aF ; 14.8 aF ; 2.5 V

10.6.2 Nonideal Effects

We now briefly consider various sources of nonideal operation of dynamic logic circuits.

Noise Margins Since, during the evaluation phase, the NMOS transistors begin to conduct for $A = V_{DD}$,

$$V_{DD} \equiv V_{in} \equiv V_p$$

and thus the noise margins will be

$$NM_L = V_{DD}$$

$$NM_H = V_{DD} - V_s$$

Thus the noise margins are far from equal, and M_{H1} is rather low. Although M_{H1} is high, other nonlinear effects reduce its value, as we shall shortly see. At this time, however, observe that the output node is a high-impedance node and thus will be susceptible to noise pickup and other disturbances.

Output Voltage Decay Due to Leakage Effects. In the absence of a path to ground through the PDN, the output voltage will ideally remain high at V_{DD} . This, however, is based on the assumption that the charge on C_1 will remain intact. In practice, there will be leakage current that will cause C_1 to slowly discharge and v_1 to decay. The principal source of leakage is the reverse current of the reverse-biased junction between the drain of all transistors connected to the output node and the substrate. Such currents can be in the range of 10^{-12} A to 10^{-3} A, and they increase rapidly with temperature (approximately doubling for every 5°C rise in temperature). Thus the circuit can malfunction if the clock is operating at a very low frequency and the output node is not "refreshed" periodically. This latter point will be encountered when we study dynamic memory cells in Chapter 11.

Charge Shaving. There is an unusual often overlooked way for C_1 to lose some of its charge and thus cause v_1 to fall slightly below V_{DD} . To see how this can happen, refer to Fig. 10.34(b), which shows only Q_1 and Q_2 , the two up-transistors of the PDN, together with the precharge transistor Q_3 . Here, C_1 is the capacitor between the common node of Q_1 and Q_2 and ground. At the beginning of the evaluation phase, after Q_1 has turned off and w.r.t. C_1 charged to V_{DD} (Fig. 10.34a), we assume that C_1 is initially discharged and that the nodes are such that at the gate of Q_2 we have a high signal, whereas at the gate of Q_3 the signal is low. We can easily see that Q_2 will turn on and its drain current, i_{D2} , will flow as indicated

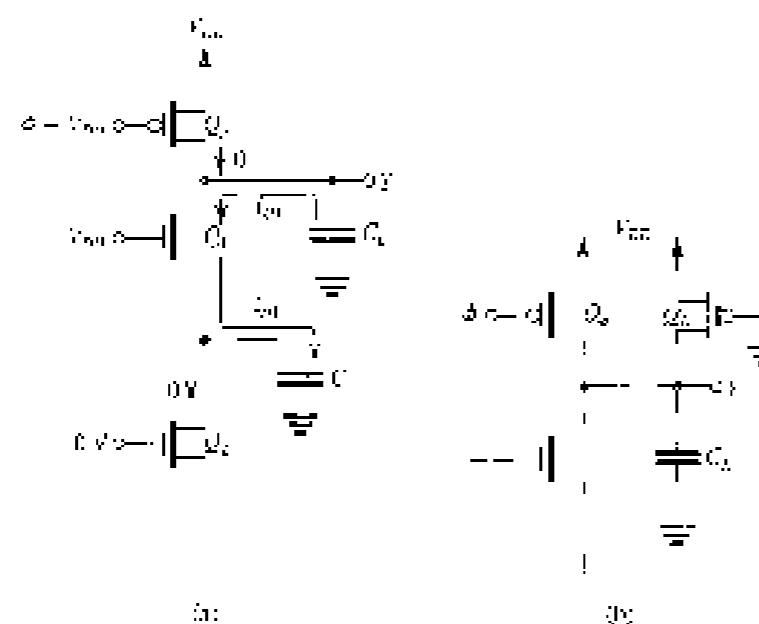


FIGURE 10.34 (a) Charge shaving; (b) adding a p-channel metal-oxide-transistor Q_2 solves the charge-shaving problem at the expense of more power dissipation.

in Fig. 10.34(b). This will discharge C_1 and charge C_2 . Although eventually i_{D2} will reduce to zero, C_1 will have lost some of its charge, which will have been transferred to C_2 . This phenomenon is known as charge sharing.

We shall not pursue the problem of charge sharing any further here, except to point out a series of techniques already employed to minimize it. One approach involves adding a p-channel device that continuously conducts a small current to replenish the charge lost by C_1 , as shown in Fig. 10.34(b). This arrangement should remind us of pseudo-NMOS. Indeed, adding this transistor will cause the gate to dissipate static power. On the positive side, however, the added transistor will lower the impedance level of the output node and make it less susceptible to noise as well as solving the leakage and charge-sharing problems. Another approach to solving the charge-shaving problem is to precharge the internal nodes, that is, to precharge capacitor C_1 . The price paid in this case is increased circuit complexity and more capacitance.

Cascading Dynamic Logic Gates. A serious problem arises if one stage feeds to cascaded dynamic logic gates. Consider the situation depicted in Fig. 10.35, where two single input dynamic gates are cascaded. During the precharge phase, C_{11} and C_{21} will be charged through Q_{11} and Q_{21} , respectively. Thus, at the end of the precharge interval, $v_{11} = V_{DD}$ and $v_{21} = V_{DD}$. Now consider what happens in the evaluation phase for the case of high input A . Obviously, the correct result will be v_1 low ($v_{11} = 0\text{ V}$) and v_2 high ($v_{21} = V_{DD}$). What happens, however, is somewhat different. As the evaluation phase begins, v_{11} turns on and C_{11} begins to discharge. However, simultaneously, Q_{21} turns on and C_{21} also begins to discharge. Only when v_{11} drops below V_{DD} will Q_{21} turn off. Unfortunately, however, by that time, C_{21} will have lost a significant amount of its charge, and v_{21} will be less than the expected value of V_{DD} . (Here, it is important to note that in dynamic logic, once charge has been lost, it cannot be recovered.) This problem is sufficiently serious to make simple cascading an impractical proposition. As usual, however, the ingenuity of circuit designers has come to the rescue, and a number of schemes have been proposed to make cascading possible in dynamic logic circuits. We shall discuss one such scheme after considering Example 10.12.

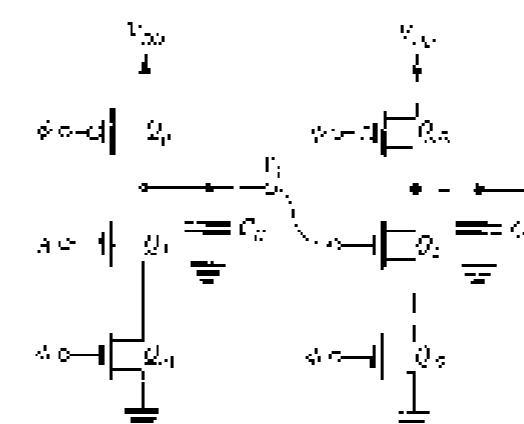


FIGURE 10.35 Two single input dynamic logic gates connected in cascade. With the input A high during the evaluation phase, C_{11} will partially discharge and the outputs v_{11} and v_{21} will fall lower than V_{DD} , which causes logic malfunction.

EXERCISE

10.22 The following logic function is to be implemented using a single dynamic CMOS inverter. The output voltage V_{out} is to be given by

$$V_{out} = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + A \cdot \overline{B} \cdot \overline{C} + A \cdot B \cdot \overline{C}$$

Assume that the inputs A, B, C are connected to the inputs of the inverter. The output of the inverter is connected to the output V_{out} . The output of the inverter is also connected to one input of a second inverter, which has its other input connected to ground. The output of the second inverter is connected to the input C of the first inverter. The output of the second inverter is also connected to one input of a third inverter, which has its other input connected to ground. The output of the third inverter is connected to the input B of the first inverter. The output of the third inverter is also connected to one input of a fourth inverter, which has its other input connected to ground. The output of the fourth inverter is connected to the input A of the first inverter. The output of the fourth inverter is also connected to one input of a fifth inverter, which has its other input connected to ground. The output of the fifth inverter is connected to the output V_{out} .

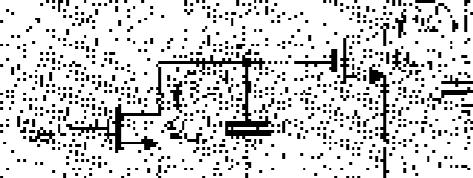


FIGURE 10.35

- (a) Find the transient response of the output V_{out} versus time for the following input values. Record each of the four input conditions (marked A, B, C, D) in the order indicated. Also, the outputs of the logic elements are to be measured when the output voltage is steady through its excursion (i.e., if $V_{out} < V_{th}$, then Q_1 will remain saturated).
- (b) Assume $V_{DD} = 1.75$ V, $V_{th} = 0.75$ V, $C_{in} = 100$ fF, $C_{out} = 1.4$ pF, and $\lambda_1 = 3.6$ V.

10.6.3 Domino CMOS Logic

Domino CMOS logic is a form of symmetric logic that results in cascadable gates. Figure 10.36 shows the structure of the Domino CMOS logic gate. We observe that it is simply the basic dynamic logic gate of Fig. 10.32(a) with a static CMOS inverter connected to its output. Operation of the gate is slightly different. During precharge, A will be raised to V_{DD} , and the gate output Y will be at 0 V. During evaluation, depending on the combination of input variables, either Y will remain high and X will remain low ($y_{out} = 0$) or X will be brought down to 0 V and the output Y will rise to V_{DD} ($y_{out} = 1$). Thus, during evaluation, the output either remains low or makes only one low-to-high transition.

To see why Domino CMOS gates can be cascaded, consider the situation in Fig. 10.37(a), where we show two Domino gates connected in cascade. For simplicity, we show single-input gates. At the end of precharge, X_1 will be at V_{DD} , Y_1 will be at 0 V, X_2 will be at V_{DD} , and Y_2 will be at 0 V. As in the preceding case, assume A is high at the beginning of evaluation.

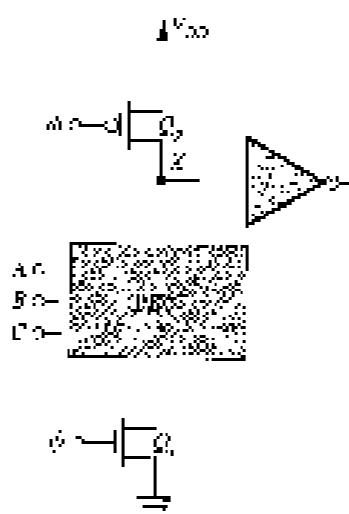


FIGURE 10.36 The Domino CMOS logic gate. The circuit consists of a dynamic CMOS logic gate with a static CMOS inverter connected to the output. During evaluation, either with some low ($y_{out} = 0$) makes one low-to-high transition for V_{out} .

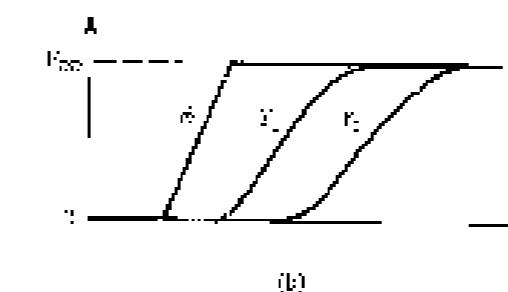
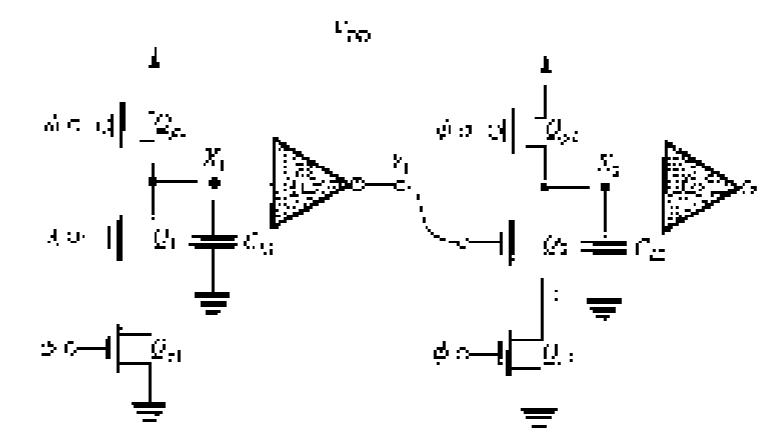


FIGURE 10.37 (a) Two single-input Domino CMOS logic gates cascaded in parallel. (b) Waveforms during the evaluation state.

Thus, as ϕ goes up, capacitor C_{in} will begin charging, pulling X_1 down. Meanwhile, the low input at the gate of i_2 keeps Q_2 off, and C_{in} remains fully charged. When X_1 falls below the threshold voltage of inverter i_1 , Y_1 will go operating Q_1 on, which in turn begins to discharge C_{in} and pull X_1 low. Eventually, X_1 rises to V_{DD} .

From this description, we see that because the output of the Domino gate is low at the beginning of evaluation, no legitimate capacitor discharge will occur in the subsequent gate in the cascade. As indicated in Fig. 10.27(b), output Y_1 will make a 0-to-1 transition after t_{pd} seconds after the rising edge of the clock. Subsequently, output Y_2 makes a 0-to-1 transition after another t_{pd} interval. The propagation of the rising edge through a cascade of gates resembles configuration links passing over each inpling the next, which is the origin of the name Domino CMOS logic. Domino CMOS logic finds application in the design of address decoders in memory chips, for example.

10.8.4 Concluding Remarks

Dynamic logic presents many challenges to the circuit designer. Although it can provide considerable reduction in the chip-area requirement, as well as high-speed operation, and zero total-state-power dissipation, the circuits are prone to many nonlinear effects, some of which have been discussed here. It should also be remembered that dynamic-power dissipation is an important issue in dynamic logic. Another factor that should be considered is the "dead time" during precharge when the output of the circuit is not yet available.

10.7 SPICE SIMULATION EXAMPLE

We conclude this chapter with an example illustrating the use of SPICE in the analysis of CMOS digital circuits. To appreciate the need for SPICE, recall that throughout this chapter we have had to make many simplifying assumptions so that transient analysis can be made possible and also so that the results can be sufficiently simple to yield design insights. This is especially the case in the analysis of the dynamic operation of logic circuits. Computer-aided analysis using SPICE not only obviates the need to make approximations, thus providing accurate results, but it also allows the use of more precise MOSFET models. Such models, of course, are too complex to use in manual analysis.

OPERATION OF THE CMOS INVERTER

In this example, we will use PSpice to simulate the CMOS inverter whose capture schematic is shown in Fig. 10.38. We will assume a 0.3- μm CMOS technology for the NMOSFETs and use p-type NMOSFETs and PMOSFETs whose level-1 model parameters are listed in Table 4.8. In addition to the channel length L and the channel width W , we have used the multiplicative factors m to specify the dimensions of the MOSFETs. The MOSTLIT parameter m , whose default value is 1, is used in SPICE to specify the number of unit-size MOSFETs connected in parallel (see Fig. 4.6). In our simulation, we will use unit-size transistors with $L = 0.5 \mu\text{m}$ and $W = 1.25 \mu\text{m}$. We will simulate the inverter for two cases: (a) assume $m_N/m_P = 1$ so that the NMOS and PMOS transistors have equal widths, and (b) setting $m_N/m_P = 0.25/4 = 4$ so that the PMOS transistor is four times wider than the NMOS transistor to compensate for the lower mobility of p-channel devices as compared with n-channel ones. Here, m_N and m_P are the multiplicative factors of, respectively, the NMOS and PMOS transistors of the inverter.

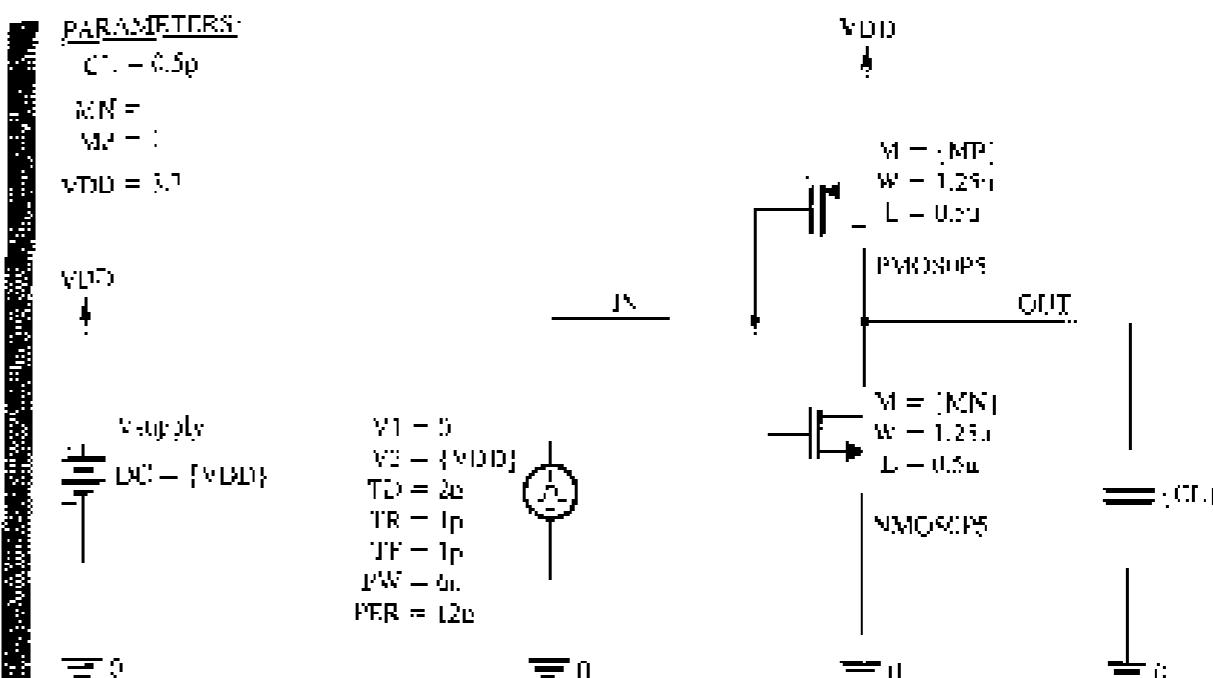


FIGURE 10.38 Capture schematic of the CMOS inverter in Example 10.5.

To compute both the voltage transfer characteristic (VTC) of the inverter and its supply current at various values of the input voltage V_I , we apply a dc voltage source at the inductor port and a noise source with V_n swept over the range 0 to V_{DD} . The resulting VTC is plotted in Fig. 10.29. Note that the slope of the VTC in the switching region (where the NMOS and PMOS devices are both in saturation) is not infinite as predicted from the simple theory presented earlier (Section 4.10, e.g., Fig. 4.53). Rather, the nonzero value of k causes the inverter gain to be finite. Using the derivative feature of PSpice, we can find the two points on the VTC at which the inverter gain is unity (i.e., the VTC slope is 1 V/V) and hence determine V_0 and V_{10} . Using the results given in Fig. 10.36, the corresponding noise margins are $AM_0 = 3.3V_0 - 1.74\text{ V}$ for the inverter with $m_N/m_P = 4$, while $AM_0 = 0.975\text{ V}$ and $AM_0 = 1.74\text{ V}$ for the inverter with $m_N/m_P = 1$. Observe that these results correlate reasonably well with the values obtained using the approximate formulation Eq. (10.81). Furthermore, note that, with $m_N/m_P = K_0/K_1 = 4$, the NMOS and PMOS devices are closely matched and, hence, the two noise margins are equal.

The threshold voltage V_T of the CMOS inverter is defined as the input voltage that results in an identical output voltage V_{DD} , that is,

$$V_T = V_D |_{V_{DD} = V_O} \quad (10.53)$$

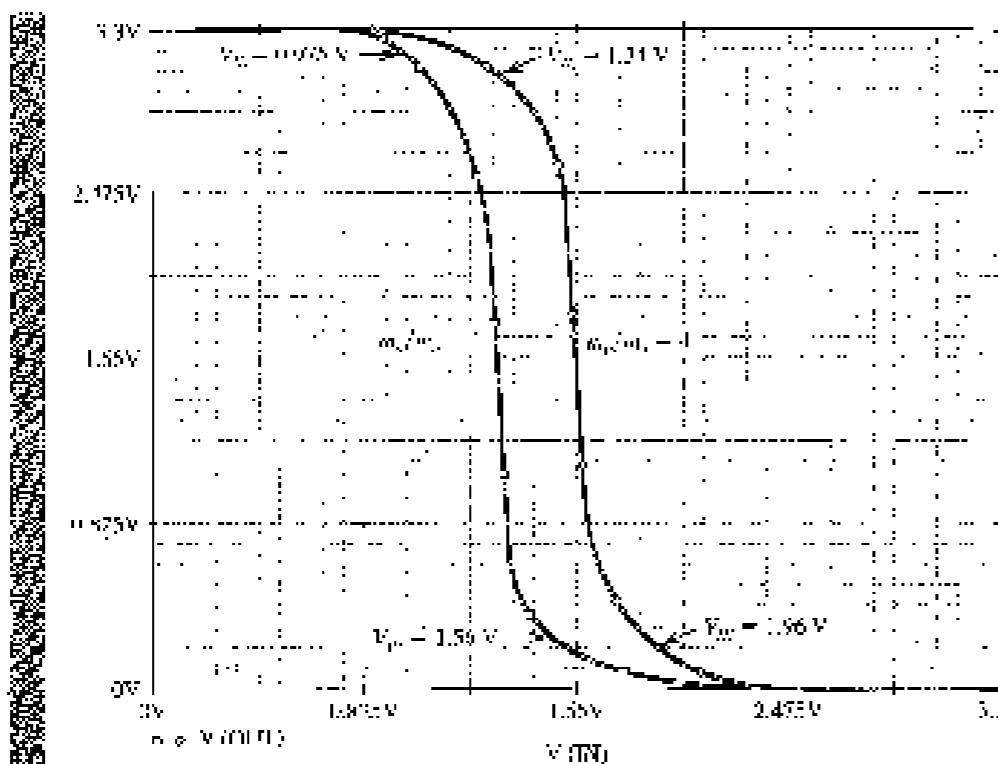


FIGURE 10.39 Input-output voltage transfer characteristic (VTC) of the CMOS inverter in Example 10.5 with $m_p/m_n = 1$ and $m_p/m_n = 4$.

Thus, as shown in Fig. 10.40, V_{th} is the intersection of the V_{DD} with the straight line corresponding to $m_p/m_n = m_n$ (this line can be simply generated in Probe by plotting m_n versus m_p/m_n , as shown in Fig. 10.40). Note that $V_{th} < V_{DD}/2$ for the inverter with $m_p/m_n = 1$. Furthermore, decreasing m_p/m_n decreases V_{th} (see earlier Exercise 1.11). Figure 10.40 also shows the inverter supply current versus V_{DD} . Observe that the location of the supply-current peak shifts with the threshold voltage.

To investigate the dynamic operation of the inverter with PSpice, we apply a pulse signal to the input (Fig. 10.41), perform a transient analysis, and plot the input and output waveforms as shown in Fig. 10.41. The rise and fall times of the pulse source are chosen to be very short. Note that increasing m_p/m_n from 1 to 4 decreases t_{RTP} (from 1.13 ns to 0.25 ns) because of the increased current available to charge C_L , with only a minor increase in t_{FPT} (from 0.23 ns to 0.34 ns). The two propagation delays, t_{RTP} and t_{FPT} , are not exactly equal when $m_p/m_n = 4$ because the NMOS and PMOS transistors are still not perfectly matched (e.g., $V_{th} \neq V_{DP}$).

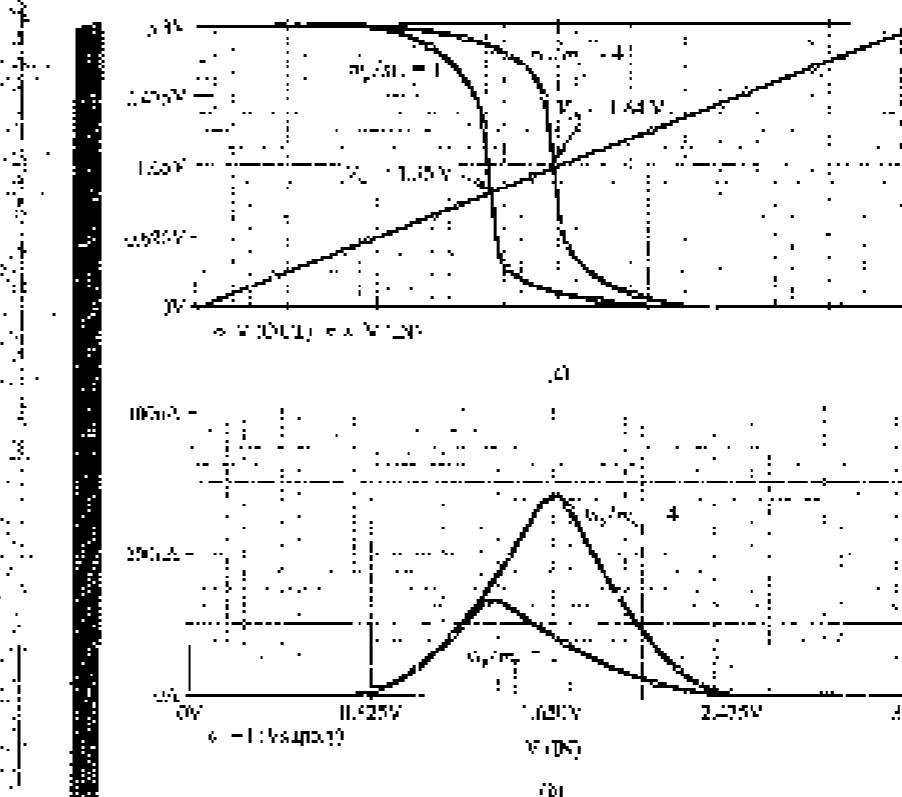


FIGURE 10.40 (a) Output voltage V_{DD} and (b) supply current versus input voltage for the CMOS inverter in Example 10.5 with $m_p/m_n = 1$ and $m_p/m_n = 4$.

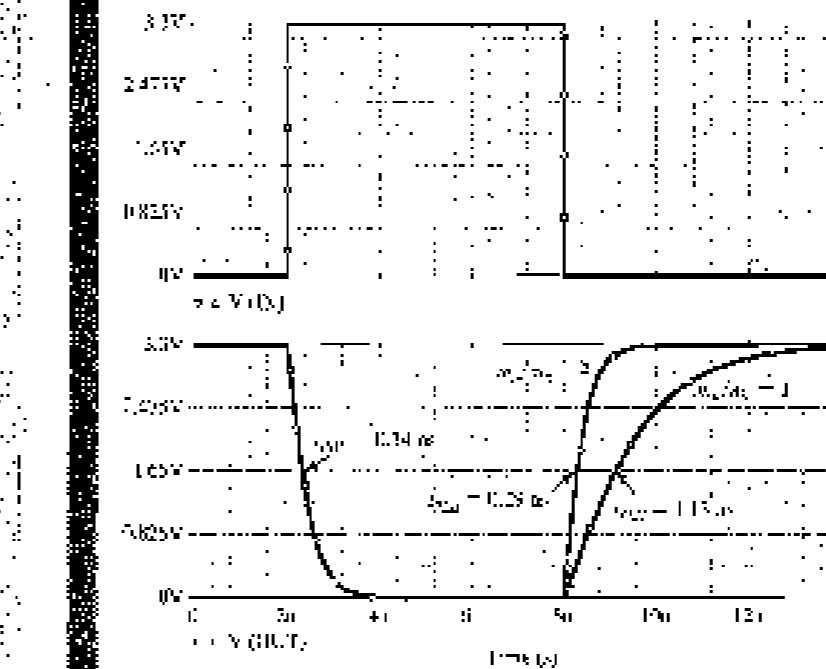


FIGURE 10.41 Transient response of the CMOS inverter in Example 10.5 with $m_p/m_n = 1$ and $m_p/m_n = 4$.

SUMMARY

- 1** Although CMOS is one of the digital technologies currently in use (the others are bipolar, BiCMOS, and GaAs), it is the most popular. This is due to its low static power dissipation and excellent static and dynamic noise margins. Further, advances in CMOS process technology have made possible the fabrication of MOS transistors with channel lengths as small as 0.13 μm. The high input impedance of MOS transistors allows the use of charge storage to implement a number of realization techniques, a technique successfully exploited in both dynamic logic and dynamic memory.
- 2** The CMOS inverter is usually designed using the minimum-channel-length NMOS and PMOS transistors. The width of the NMOS transistor is usually 1.5 to 2 times L_s , and the width of the PMOS device is (L_s/k_1) . Note that the latter matching condition ensures that the inverter will switch at $V_{DD}/2$ and gives equal current-driving capabilities in both directions and hence symmetrical propagation delays.
- 3** A simple technique for determining the propagation delay of a logic gate is to determine the average current I_{av} available to charge the discharge load capacitor (C). Then, for the fan-out n , it is given by $t_p = C(V_{DD} - V_{DD}/n)$.
- 4** A complementary CMOS logic gate consists of an NMOS pull-down network (PDN) and a PMOS pull-up network (PPN). The PPN conductance goes to zero in all combination but one when a low current flows in the NMOS transistors when its output is high; the PDN is most directly synthesized from the expression for the low (\bar{y}) part (\bar{f}) as a function of the input complement. In a complementary fashion, the PPN conductance for every input combination but one when a low current flows in the NMOS transistors when its output is high, the PPN is most directly synthesized from the expression for a high output (y) as a function of the inputs and inputs.
- 5** CMOS logic circuits are easily designed to provide equal current driving capability in both directions, and therefore the average value of the pull-up and pull-down currents

is made equal to those of the basic inverter, inverting, and inverter-based on the principle of symmetry of the equivalent $1/2$ -ratio of series and parallel devices (Eqs. 10.27 and 10.28).

- 6** Complementary CMOS logic utilizes two transistors, one NMOS and a PMOS, for each input variable. Thus the circuit complexity, silicon area, and parasitic capacitance all increase with扇出.

- 7** To reduce the Jaynes effect, two other forms of static CMOS, namely, pseudo-NMOS and pass-transistor logic (PTL), are employed in special applications as supplements to complementary CMOS.

- 8** Pseudo-NMOS utilizes the same PDN as in complementary CMOS logic but replaces the PPN with a single PMOS transistor whose gate is grounded. Unlike dynamic memory CMOS, pseudo-NMOS is a related form of logic in which V_{DD} is determined by the ratio of k_1 to k_2 . Specifically, k_1 is selected in the range 4 to 10 and k_2 is used to determine the noise margin.

- 9** Pseudo-NMOS has the disadvantage of dissipating gate power when the output of the logic gate is low. Source power can be eliminated by adding the PPN's load to the only a brief interval, known as the pre-charge interval, to charge the output node to V_{DD} . Then the inputs are applied, and depending on the input combination, the output node either remains high or discharges through the PPN. This is the essence of dynamic logic.

- 10** Pass-resistor logic utilizes either single NMOS transistors or CMOS resistors as on-gates to implement a network of switches that are controlled by the input logic variables. Switches implemented by single NMOS transistors, though simple, result in the reduction of V_{DD} from V_{DD} to $V_{DD} - V_s$.

- 11** A particular form of dynamic logic circuits, known as device logic, allows the possibility of dynamic logic gates.

PROBLEMS

SECTION 10.7: DIGITAL CIRCUIT DESIGN: AN OVERVIEW

- 10.1** For a logic-circuit family employing a p-V technology, suggest an ideal set of values for V_{DD} , V_{TH} , V_{DD}/k_1 , V_{DD}/k_2 , R_{ON} . Also, sketch the VTC. What value of voltage g_m is in the transition region does your ideal specification imply?

- 10.2** For a particular logic-circuit family, the logic threshold voltage V_{TH} is constant (but to the small-signal low-frequency voltage gain of 30 V/V), L_s , with a 3.3-V supply, the values of V_{DD} and $V_{DD}/2$ are ideal, but $V_{DD} = 0.4 V_{DD}$, what are the best possible values of V_{DD} and $V_{DD}/2$ that can be expected? What are the best possible gate-voltages you can choose? If the signal noise margins are only 7.10% of these values, what P_{DD} and V_{DD} result? What is the large-signal voltage gain defined as $V_{DD} \cdot V_{DD}/(V_{DD} - V_{DD})$? Offer the straightforward approximations for the VTC.

- 10.3** A logic circuit family intended for use in a digital signal processing application is currently developed to operate at 1.5 V. If the 1.5-V noise margin, the output signals swing between 1 and V_{DD} , the "gain of one" points are separated by less than 1/3 V_{DD}, and the noise margins are within 30% of one another, what ranges of values of V_{DD} , $V_{DD}/2$, $V_{DD}/3$, $3V_{DD}/4$, and $5V_{DD}/6$ can you choose for the lowest possible battery supply?

- 10.4** In a particular logic family, the standard inverter, when loaded by a unit load, has a propagation delay specified to be 1.2 ns.

- (a) If the inverter is able to supply a load of unity or 3 as fast as logic as that available to discharge the capacitor, what do you expect t_{PD} and t_{PDL} to be?

- (b) If an external capacitive load of 1 pF is added to the inverter output, its propagation delay increases by 10%, what do you estimate the required load to achieve a 1.2-ns propagation delay to be?

- (c) If, without the additional 1-pF load connected, the load capacitors removed and no propagation delays were observed to decrease by 40%, compare the two components of the capacitance term, i.e., the capacitor due to the inverter output and other associated parasitics, and the component due to the input of the load inverter?

- 10.5** For a particular logic family, operating with a 3.3-V supply, the basic inverter draws (from the supply) a current of 400 pA in one state and 600 pA in the other. When the inverter is switched at the rate of 100 MHz, the average supply current

- becomes 150 μA. Estimate the equivalent capacitance of the output node of the inverter.

- 10.6** A collection of logic gates for which the static power dissipation is zero, and the dynamic-power dissipation, as specified by Eq. (10.4), is 10 mW per inverter at 50 MHz with a 5-V supply. By what factor could the power dissipation be reduced if operation at 3.3 V were possible? If the frequency of operation is reduced by the same factor as the supply voltage (i.e., 33 MHz), what supply voltage can be used?

- 10.7** A logic-circuit family with zero static-power dissipation originally operates at $V_{DD} = 5$ V. The set of its dynamic-power dissipation, which is specified by Eq. (10.4), operation at 3.3 V is considered. It is found, however, that the current available to charge and discharge load capacitors also decreases. If current is (a) proportional to V_{DD} , or (b) proportional to V_{DD}^2 , what reductions in maximum operating frequency do you expect in each case? What fractional change in delay-power product do you expect in each case?

- 10.8** Recompute the situation described in Problem 10.7, for the situation in which a threshold relation exists such that the current depends on $V_{DD} = V_s$ rather than V_{DD} directly. For note the change of current, propagation delay, operating frequency, dynamic power, etc., delay-power product as a result of decreasing V_{DD} from 5 V to 3.3 V. Assume that the currents are proportional to $\ln(V_{DD} - V_s)$, or the $V_{DD} - V_s$, for V_{DD} from 10 to 1 V and 100 pA.

- 10.9** Consideration is being given to reducing by 10% the chip area, including oxide thickness, of a silicon digital CMOS process. Note that for a MOS device the available current is related to

$$I = \frac{1}{2} q C_{ox} \frac{W}{L} (V_{DD} - V)^2$$

- where $C_{ox} = \epsilon_0 / t_{ox}$. Also assume that the total effort to scale down the dimensions that determines the propagation delay is divided about equally between MOS capacitances that are proportional to t_{ox} and inversely proportional to t_{ox} , and reverse-bias junction capacitances that are proportional to t_{ox} . Find the factors by which the 3.3-V low-power parameter chip-area, current, effective capacitance, propagation delay, operating frequency, dynamic-power dissipation, delay-power product, and performance (in operations per unit area per second). If the supply voltage is also reduced by 10% (but V_s is left), what other changes result?

less area and lower propagation delay because it uses NOR gates with fewer transistors. Assuming narrow transistors in both circuits are properly sized to provide each gate with a current-driving capability equal to that of the basic inverter, find the number of transistors and the total area of each circuit. Assume the basic inverter to have a W/L ratio of 1.2 nm/0.8 μm and a mobility ratio of 3.0 nm/0.8 μm .

*10.37 Consider the two-input CMOS NOR gate of Fig. 10.17 whose transistors are properly sized so that the current-driving capability in each direction is equal to that of a standard inverter. For $V_s = 0$ and $V_{DD} = 5$ V, find the gate threshold in the cases for which (a) input node A is connected to ground and (b) the two input terminals are tied together. Neglect the body effect in C_{SS} .

SECTION 10.4: PSEUDO-NMOS LOGIC CIRCUITS

10.38 The purpose of this problem is to compare the value of t_{PD} obtained with a resistive load (see Fig. P10.3-a) to that obtained with a current source load (see Fig. P10.3-b). For a fair comparison, let the current source $I = V_{DD}/R_D$, which is the input current available to charge the capacitor in the case of a resistive load. Find t_{PD} for each case, and hence the percentage reduction realized when a current-source load is used.

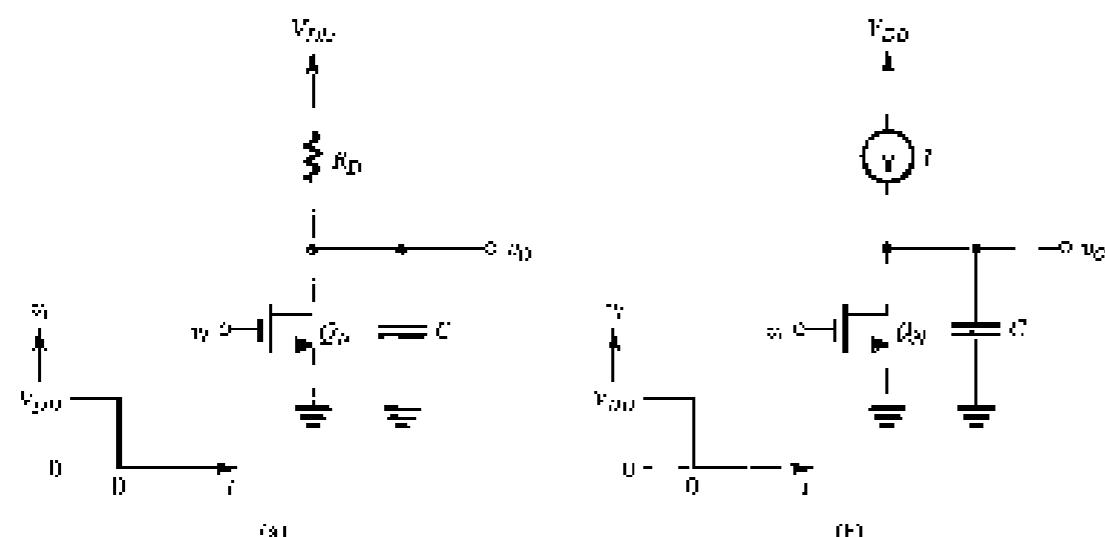


FIGURE P10.3

10.41 Design a pseudo-NMOS inverter that has equal positive and negative capacitive-driving output currents, $i_+ = i_- = V_{DD}/4$ for use in a system with $V_{DD} = 5$ V, $|V_t| = 0.5$ V, $k_f = 3k_b = 75 \mu\text{A/V}^2$, and $(W/L)_n = 1.2 \text{ nm}/0.8 \mu\text{m}$. What are the values of $(W/L)_p$, V_{DD} , V_{SS} , V_{DD} , V_{SS} , and R_D ?

10.42 Consider a pseudo-NMOS inverter with $r = 1$, $(W/L)_p = 1.2 \text{ nm}/0.8 \mu\text{m}$, $V_{DD} = 5$ V, $|V_t| = 0.5$ V, and $k_f = 3k_b = 75 \mu\text{A/V}^2$. Let the output capacitance per micrometer of device width be $C_o = 1.5 \text{ fF}$, $C_{SS} = 0.5 \text{ fF}$, and $C_{DD} = 2 \text{ fF}$. Estimate the input and output capacitances and the values of t_{PD} , t_{PDH} , and t_{PDL} obtained when the inverter is driven (a) with a resistor load, (b) with a current source load, and (c) with a complementary CMOS inverter with a matched design.

10.43 Use Eq. (10.41) to find the value of r for which AM_p is maximized. What is the corresponding value of AM_p ?

10.44 Design a pseudo-NMOS inverter at $V_{DD} = 0.1$ V, $V_{SS} = -0.5$ V, $|V_t| = 0.4$ V, $k_f = 100 \mu\text{A/V}^2$, and $(W/L)_p = 0.175 \text{ nm}/0.25 \mu\text{m}$. What is the value of $(W/L)_n$? Is it possible to obtain AM_p and the static power dissipation?

10.45 For what value of r does AM_p of a pseudo-NMOS inverter become zero? Prepare a table of AM_p versus r for $r = 1$ to 16.

10.46 For a pseudo-NMOS inverter, what value of r results in $AM_p = AM_n$? Let $V_{DD} = 5$ V and $V_t = 0.5$ V. What is the resulting margin?

10.47 It is required to design a minimum-area pseudo-NMOS inverter with equal high and low noise margins using a 3-V supply and devices for which $|V_t| = 0.5$ V, $k_f = 3k_b = 75 \mu\text{A/V}^2$, and the drain-to-body diode has $(W/L)_d = 1.2 \text{ nm}/0.8 \mu\text{m}$. Use $r = 2.72$ and show that $AM_p = AM_n$. Specify the values of $(W/L)_p$ and $(W/L)_n$. What is the power dissipated in this gate? What is the ratio of propagation delays for high- and low-transistor-on or an external capacitive load of 1 pF, and neglecting the drain-to-body diode capacitance, find t_{PDH} , t_{PDL} , and t_{PD} . At what operating voltage would the static and dynamic power levels be equal? Is this state of operation possible in view of the t_{PD} values you found? What is the ratio of dynamic power to static power and you may assume is the amount of time it takes using frequency (say, $1/42t_{PD} + 2t_{PD} \times 10^9$)

10.48 Sketch a pseudo-NMOS realization of the function $Y = A + B(C + D)$.

10.49 Sketch a pseudo-NMOS realization of the exclusive OR function $Y = \bar{A}B + \bar{A}B$.

10.50 Consider a four-input pseudo-NMOS NOR gate in which the NMOS devices have $(W/L)_n = (1.2 \text{ nm}/1.2 \mu\text{m})$. It is required to find $(W/L)_p$ so that the static-voltage value of V_{DD} is 0.2 V. Let $V_{DD} = 5$ V, $|V_t| = 0.5$ V, and $k_f = 3k_b = 75 \mu\text{A/V}^2$.

SECTION 10.5: PASS-TRANSISTOR LOGIC CIRCUITS

10.51 Is the circuit in Fig. P10.51 a satisfactory pass-transistor logic circuit? What are its deficiencies? What is F as a function of A , B , C , D ? What does the output become if the two V_{DD} connections are driven by a CMOS inverter with invert F ?

(a) After a string of minimum-area single MOS transistors can do complex logic functions, (b)

(c) that there must always be a path between output and a supply terminal.

Outspeakingly, to find consist 6 two-gates, shown in Fig. 10.45. For each, express Y as a function of A and B . In each case, what can be said about general operation? About the logic levels of Y ? Above node S ? On either of these circuits true condition? C in one case the terminal is connected to V_{DD} is isolated connected to the output of a CMOS inverter whose input is connected to a signal C . What does the function F become?

10.52 An NMOS pass-transistor switch with $W/L = 1.2 \text{ nm}/0.8 \mu\text{m}$, used in a 3.3-V system for which $V_t = 0.5$ V, $k_f = 0.5 \mu\text{A/V}^2$, $C_{DD} = 3 \mu\text{F}$, $C_{SS} = 75 \mu\text{A/V}^2$, drives a 100-fF load capacitance at the input of a cascaded three-inverter using $(W/L)_n = 1.2 \text{ nm}/0.8 \mu\text{m}$. For the switch gate terminal at V_{DD} , calculate the switch V_{DD} and V_{SS} for inputs at V_{DD} and 0 V, respectively. For the value of V_{DD} , what inverter static current results? Estimate t_{PDH} and t_{PDL} in this arrangement as measured from the input to the output of the switch itself.

10.53 The purpose of this problem is to design the level-restoring circuit in Fig. 10.28 and gain insight into its

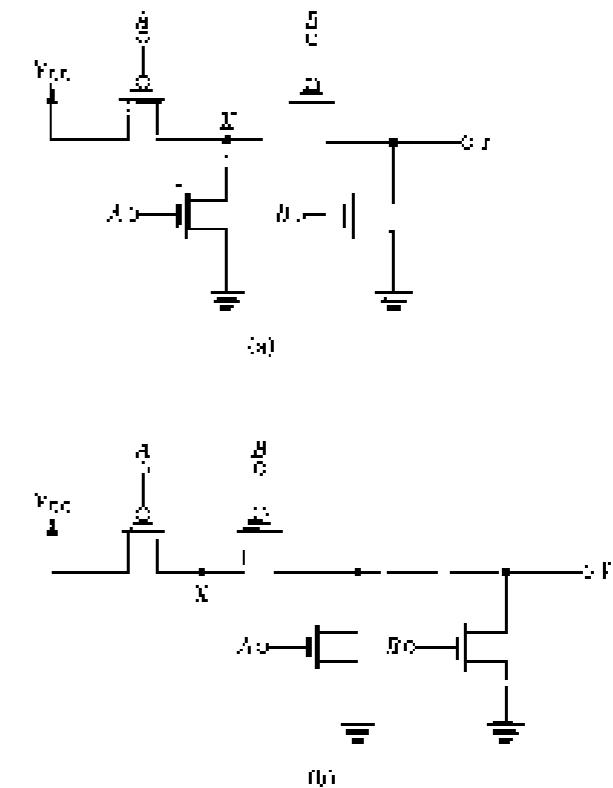


FIGURE P10.49

and with V_{DD} and V_{SS} connections interchanged. What do the output functions F become?

10.54 Is the circuit in Fig. P10.51 a satisfactory pass-transistor circuit? What are its deficiencies? What is F as a function of A , B , C , D ? What does the output become if the two V_{DD} connections are driven by a CMOS inverter with invert F ?

An NMOS pass-transistor switch with $W/L = 1.2 \text{ nm}/0.8 \mu\text{m}$, used in a 3.3-V system for which $V_t = 0.5$ V, $k_f = 0.5 \mu\text{A/V}^2$, $C_{DD} = 3 \mu\text{F}$, $C_{SS} = 75 \mu\text{A/V}^2$, drives a 100-fF load capacitance at the input of a cascaded three-inverter using $(W/L)_n = 1.2 \text{ nm}/0.8 \mu\text{m}$. For the switch gate terminal at V_{DD} , calculate the switch V_{DD} and V_{SS} for inputs at V_{DD} and 0 V, respectively. For the value of V_{DD} , what inverter static current results? Estimate t_{PDH} and t_{PDL} in this arrangement as measured from the input to the output of the switch itself.

10.55 The purpose of this problem is to design the level-restoring circuit in Fig. 10.28 and gain insight into its

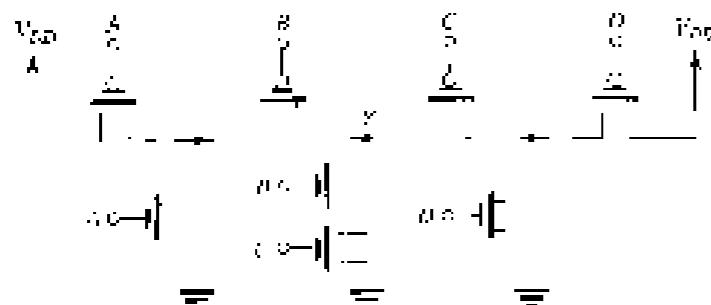


FIGURE P10.51

operation. Assume that $k_A = k_B = 75 \mu\text{A/V}^2$, $V_{DD} = 5.0 \text{ V}$, $V_{thN} = 0.8 \text{ V}$, $V_{thP} = -0.5 \text{ V}$, $2\phi_f = 0.6 \text{ V}$, $10VDD_1 = 19.6 \text{ V}$, $1.2 \text{ nm} \times 0.8 \mu\text{m} \times 400L_D = 3.6 \text{ nm} \times 0.8 \mu\text{m}$, and $C = 20 \text{ fF}$. Let $v_o = V_{DD}$.

- (a) Consider first the situation with $v_o = V_{DD}$, find the value of the voltage v_{Q1} that causes v_o to drop to its hold voltage (v_{HOLD}) that is, to 2.5 V so that Q_1 turns on. At this value of v_{Q1} , find i_{Q1} at Q_1 . What is the current charging current available at this time? What is $v_{Q2} = 0$? What is the average current available for charging C ? Find now v_{Q2} from the equation $v_{Q2} = 0$.
- (b) Now, to determine a suitable RCL load for Q_2 , consider the situation when v_o is brought down to 0 V and Q_2 starts to turn on to precharge C . The voltage v_{Q2} will begin to drop. Meanwhile, i_{Q2} is still low and Q_1 is conducting. The current through Q_1 remains until $v_{Q1} = 0$. Find the value of v_{Q1} at which the inverter begins to switch. This is $V_{DD} - \frac{1}{2}(V_{DD} - 2V_{th})$. Then, find the current that Q_1 conducts at this value of v_{Q1} . Choose R_{Q2} to set the current to, say, $10 \mu\text{A}$ and find the value of the resistor in Q_2 . What is the RCL you have chosen? Calculate t_{PD} as the time for v_{Q2} to drop from V_{DD} to V_{thP} .

P10.54 (a) Use the given model of the exclusive-OR realization in Fig. 10.51 to realize $Y = AP + AB + BC$. (b) Find a realization for Y using two transmission gates.

(c) Now, combine the circuit obtained in (a) with the circuit in Fig. 10.51 to show a realization of the function $Z = PC + PC'$, where C is a J-K flip-flop. Sketch the complete transmission-gate realization of Z . Note that Z is a three-input exclusive-OR.

P10.55 Using the CMOS presented in Fig. 10.42, sketch a CPL device whose output is $Y = AB + 4B + 4C + 4D + 4E + 4F$.

P10.56 Extend the 1-bit adder in Fig. 10.44 to three variables to form $Z = ABC + \bar{A}BC' + \bar{A}B'C + \bar{A}B'C' + \bar{A}B'C'' + \bar{A}B'C''' + \bar{A}B'C'''' + \bar{A}B'C'''''$.

charge redistribution. For $V_{DD} = 1 \text{ V}$, $V_{DD} = 3 \text{ V}$, $C_L = 30 \text{ fF}$ and neglecting the body effect in Q_1 , find the drop in voltage v_{Q1} developed in the two nodes ($v_{Q1} = 5.0 \text{ V}$ and $v_{Q1}' = 11.0 \text{ V}$) as Q_1 turns on and in saturation during its turn-on switching time interval.

10.61 The leakage current in a typical logic gate causes the capacitor C_L to leakage during the evaluation phase even if the PMOS is not conducting. For $V_{DD} = 10 \text{ V}$, see

$I_{leak,1} = 10^{-15} \text{ A}$. Find the longest allowable evaluation time if the decrease in output voltage is to be limited to 0.5 V. If the precharge interval is much shorter than the maximum allowable evaluation time, find the minimum clocking frequency required.

10.62 For the four-input Dynamic-Logic NAND gate analyzed in Examples 10.10 and 10.11, assume the minimum clocking frequency allowed.

SECTION 10.6: DYNAMIC LOGIC CIRCUITS

D10.57 Based on the basic dynamic-logic circuit of Fig. 10.39, sketch complete circuits for NOT, NAND, and NOR gates, the latter two with two inputs, and a three- or four-input OR.

10.58 In this and the following problem, we investigate the dynamic operation of a four-input NAND gate realized in the dynamic-logic form and fabricated in a CMOS process technology in which $k_A = k_B = 75 \mu\text{A/V}^2$, $V_{th} = V_{DD} = 0.8 \text{ V}$, and $V_{DD} = 5 \text{ V}$, $1.2 \text{ nm} \times 0.8 \mu\text{m} \times 400L_D = 3.6 \text{ nm} \times 0.8 \mu\text{m}$. The NMOS devices are used for $n = \text{high}$, $3\phi_2 = 1.2 \text{ nm} \times 0.8 \mu\text{m}$; the PMOS precharge resistor R_{Q2} has $2.4 \mu\text{m}/0.8 \mu\text{m}$. The capacitance C_L is found to be 15 fF . Consider the precharge operation with the gate of Q_1 at 0 V; and assume that $v_{Q1} = 0$, Q_1 is fully discharged. We wish to calculate the rise time of the output voltage, defined as the time for v_{Q1} to rise from 10% to 90% of the final value of 1 V. Find the current $i_{Q1} = 1.5 \text{ V}$ at the current $v_{Q1} = 2.7 \text{ V}$, then compute an appropriate value for R_{Q2} , i.e., $R_{Q2} = 1.5/(2.7 - v_{Q1})$, where v_{Q1} is the desired value of the relevant node.

D10.59 For the gate specified in Problem 10.23, evaluate the eight-to-low propagation delay, t_{PLD} . To obtain t_{PLD} close to t_{PD} , replace the three-series NMOS transistors with one n -channel device and find the average discharge current.

***10.60** In this problem, we wish to evaluate the reduction in the output voltage of a dynamic logic gate as a result of charge redistribution. Refer to the circuit in Fig. 10.34(a), and assume that $w = b = v_{DD}$ and $v_{th} = 0$. As v_{Q1} goes high and Q_1 turns off, simultaneously the voltage of the gate of Q_2 goes high via v_{DD} turning Q_2 on. Transistor Q_3 will turn on by turning on either the voltage of its source node or because $v_{Q1} < v_{DD}$ or $v_{Q1} = v_{DD}$, whichever comes first. In both cases, the final value of v_{Q1} can be derived using

PART III

SELECTED TOPICS

CHAPTER 11

Memory and Advanced Digital Circuits 1013

CHAPTER 12

Filters and Tuned Amplifiers 1083

CHAPTER 13

Signal Generators and Waveform-Shaping Circuits 1165

CHAPTER 14

Output Stages and Power Amplifiers 1229

INTRODUCTION

To round out our study of electronic circuits we have selected, from among the many possible somewhat-specialized topics, four to include in the third and final part of this book.

Chapter 11 deals with the important subject of digital memory. In addition, two advanced digital circuit technologies—ECL and BiCMOS—are studied. The material in Chapter 11 follows naturally the study of logic circuits presented in Chapter 10. Together, these two chapters should provide a preparation sufficient for advanced courses in digital electronics and VLSI design.

The subsequent two chapters, 12 and 13, focus on applications or systems orientation. Chapter 12 deals with the design of filters, which are important building blocks of communications and instrumentation systems. Filter design is one of the few areas of engineering for which a complete design theory exists, starting from specification and culminating in an actual working circuit. The material presented should allow the reader to perform such a complete design process.

In the design of electronic systems, the need usually arises for signals of various waveforms—sinusoidal, pulse, square-wave, etc. The generation of such signals is the subject of Chapter 13. It will be seen that some of the circuits utilized in waveform generation possess memory and are in fact the analog counterparts of the digital memory circuits studied in Chapter 11.

The material in Chapters 12 and 13 assumes knowledge of op amps (Chapter 2) and makes use of frequency response and s-plane concepts (Chapter 6) and of feedback (Chapter 8).

The last of the four selected-topics chapters (Chapter 14) deals with the design of amplifiers that are required to deliver large amounts of load power; for example, the amplifier that drives the loudspeaker in a stereo system. As will be seen, the design of these high-power circuits is based on different considerations than those for small-signal amplifiers. Most of the material in Chapter 14 should be accessible to the reader who has studied Part I of this book.

CHAPTER 11

Memory and Advanced Digital Circuits

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INTRODUCTION

The logic circuits studied in Chapter 10 are called **combinational** (*or combinational*). Their output depends only on the present value of the input. Thus these circuits do not have memory. Memory is a very important part of digital systems. Its availability in digital computers allows for storing programs and data. Furthermore, it is important for temporary storage of the output produced by a combinational circuit for use at a later time in the operation of a digital system.

Logic circuits that incorporate memory are called **sequential circuits**; that is, their output depends not only on the present value of the input but also on the input's previous values. Such circuits require a timing generator (a *clock*) for their operation.

There are basically two approaches for providing memory to a digital circuit. The first relies on the application of positive feedback; that is, will be seen shortly, can be arranged to provide a circuit with two stable states. Such a *bistable* circuit can then be used to store one bit of information. One stable state would correspond to a stored 0, and the other to a stored 1. A bistable circuit can remain in either state indefinitely, and thus belongs to the category of *static sequential circuits*. The other approach to realizing memory utilizes the storage of

charge on a capacitor. When the capacitor is charged, it would be regarded as having a 1; when it is uncharged, it would be viewing a 0. Since the inevitable leakage effects will cause the capacitor to discharge, such a form of memory requires the periodic recharging of the capacitor, a process known as regenesis. Thus, the dynamic logic memory based on charge storage is known as *dynamically* memory, and the corresponding sequential circuits as *dynamical* sequential circuits.

In addition to the study of a variety of memory types and circuits in this chapter, we will also learn about two important digital-circuit technologies: *Primer* (primal logic) and *BICMOS*, which utilizes Bipolar transistors and achieves very high speeds of operation; and *BICMOS*, which combines Bipolar transistors and CMOS to great advantage.

11.1 LATCHES AND FLIP-FLOPS

In this section, we shall study the basic memory element—the latch, and consider a sampling of its applications. Both static and dynamic circuits will be considered.

11.1.1 The Latch

The basic memory element, the latch, is shown in Fig. 11.1(a). It consists of two cross-coupled logic inverters, G_1 and G_2 . The inverters form a positive feedback loop. To investigate the operation of the latch we break the feedback loop at the input of one of the inverters, say G_1 , and apply an input signal v_x , as shown in Fig. 11.1(b). Assuming that the input impedance of G_1 is large, breaking the feedback loop will not change the loop voltage transfer characteristic, which can be determined from the circuit of Fig. 11.1(b) by plotting v_z versus v_x . This is the voltage transfer characteristic of two cascaded inverters and thus takes the shape shown in Fig. 11.1(c). Observe that the transfer characteristic consists of three segments, with the middle segment corresponding to the transition region of the inverters.

Also shown in Fig. 11.1(c) is a straight line with unity slope. This straight line represents the relationship $v_x = v_z$, that is realized by connecting Z to W to close the feedback loop.

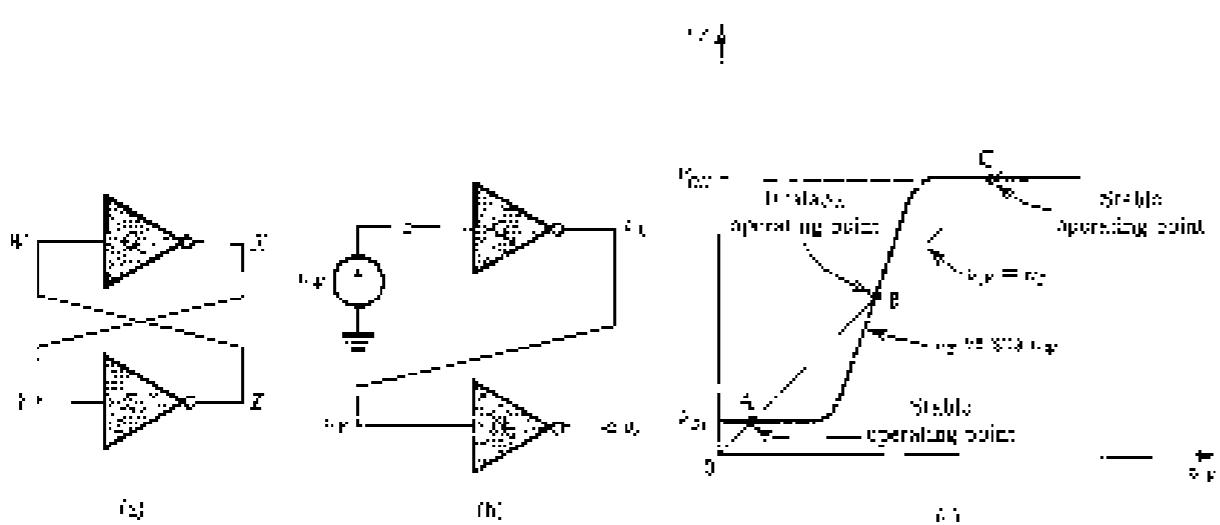


FIGURE 11.1 (a) Basic latch; (b) The latch with the feedback loop opened; (c) Determining the operating points of the latch.

As indicated, the straight line intersects the loop transfer curve at three points A, B, and C. Thus any of these three points can serve as the operating point for the latch. We shall now show that while points A and C are stable operating points in the sense that the circuit can remain at either indefinitely, point B is an unstable operating point; the latch cannot operate at B for any significant period of time.

The reason why B is unstable can be seen by considering the latch circuit in Fig. 11.1(a) to be oscillating at point B, and taking account of the electrical interference (or noise) that is inevitably present in any circuit. Let the voltage v_x increase by a small increment Δv_x . The voltage v_z will increase (in magnitude) by a larger increment, equal to the product of Δv_x and the incremental gain of G_1 at point B. The resulting signal v_z is applied to G_2 and gives rise to an even larger signal at node Z. The voltage v_z is reduced to the original increment Δv_x by the loop gain at point B, which is the slope of the curve of v_z versus v_x at point B. This gain is usually much greater than unity. Since v_z is coupled to the input of G_1 , it will be further amplified by the loop gain. This regenerative process continues, shifting the operating point from B upward to point C. Since at C the loop gain is zero (or almost zero), no regeneration can take place.

In the description above, we assumed an initial positive voltage increment at X. Had we instead assumed a negative voltage increment, we would have seen that the operating point moves downward from B to A. Again, since at point A the slope of the transfer curve is zero (or almost zero), no regeneration can take place. In fact for regeneration to occur the loop gain must be greater than unity, which is the case at both B and C.

The discussion above leads us to conclude that the latch has two stable operating points, A and C. At point C, v_x is high, v_y is low, v_z is low, and v_w is high. The reverse is true at point A. If we consider X and Z as the latch outputs, we see that in one of the stable states (say that corresponding to operating point A) v_x is high (at V_{DD}) and v_z is low (at V_{DD}). In the other state (corresponding to operating point C) v_x is low (at V_{DD}) and v_z is high (at V_{DD}). Thus the latch is a bistable circuit having two complementary outputs. The stable state in which the latch operates depends on the external excitation that forces it to the particular state. The latch then remembers this external action by staying indefinitely in the acquired state. As a memory element, the latch is capable of storing one bit of information. Furthermore, we can arbitrarily designate the state in which v_x is high and v_z is low as corresponding to a stored logic 1. The other complementary state, here designated by a stored logic 0. Finally, it should be obvious that the latch circuit described is of the static variety.

It now remains to devise a mechanism by which the latch can be triggered to change state. The latch, together with the triggering circuitry forms a flip-flop. This will be discussed next. Analog bistable circuits utilizing op amps will be presented in Chapter 13.

11.1.2 The SR Flip-Flop

The simplest type of flip flop is the set/reset (SR) flip-flop shown in Fig. 11.2(a). It is formed by cross-coupling two NMOS gates, and thus it incorporates a latch. The second input

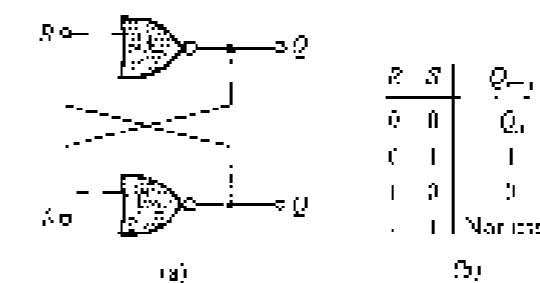


FIGURE 11.2 (a) The simplest SR flip-flop; (b) its truth table.

of each NOR gate inverter serve as the trigger inputs of the flip-flop. These two inputs are labeled S (for set) and R (for reset). The outputs are labeled Q and \bar{Q} , emphasizing their complementarity. The flip-flop is considered to be set, i.e., storing a logic 1 when Q is high and \bar{Q} is low. When the flip-flop is in the other state (Q low, \bar{Q} high), it is considered to be reset, storing a logic 0.

In the first of memory state (i.e., when we do not wish to change the state of the flip-flop), both the S and R inputs should be low. Consider the case when the flip-flop is storing a log. 0. Since \bar{Q} will be low, both inputs to the NOR gate G_1 will be low, its output will therefore be high. This high is applied to the input of G_2 , causing its output Q to be low, satisfying the original assumption. To set the flip-flop we raise S to the logical level while leaving R at 0. The 1 at the S terminal will force the output of G_2 , \bar{Q} , to 0. Thus the two inputs to G_1 will both be high and its output Q will go to 1. Now even if R returns to 0, the flip-flop remains in the newly acquired set state. Obviously, if we raise R to 1 again (with S remaining at 0) no change will occur. To reset the flip-flop we need to raise R to 1 while leaving $S = 0$. We can readily show that this forces the flip-flop into the reset state and that the flip-flop remains in this state even after R has returned to 0. It should be observed that the trigger signal merely starts the regeneration action of the positive-feedback loop of the latch.

Finally, we inquire into what happens if both S and R are simultaneously raised to 1. If the two NOR gates will cause both Q and \bar{Q} to become 0 (note that in this case the complementary labeling of these two variables is incorrect). However, if R and S return to the rest state ($R = S = 0$) simultaneously, the state of the flip-flop will be undefined. In other words, it will be impossible to predict the final state of the flip-flop. For this reason, this initial combination is usually disallowed (i.e., not used). Note, however, that this situation arises only in the idealized case, when both R and S return to 0 precisely simultaneously. In actual practice one of the two will return to 0 first, and the final state will be determined by the input that remains high longer.

The operation of the flip-flop is summarized by the truth table in Fig. 11.20, where Q_0 denotes the value of Q at time t_0 , just before the application of the R and S signals, and Q_{t_0} denotes the value of Q at time t_0 , after the application of the input signals.

Rather than using two NOR gates, one can also implement an SR flip-flop by cross-coupling two NAND gates in which case the set and reset functions are active when low and the inputs are correspondingly called S and R .

11.1.3 CMOS Implementation of SR Flip-Flops

The SR flip-flop of Fig. 11.2 can be directly implemented in CMOS by simply replacing each of the NOR gates by its CMOS circuit realization. We encourage the reader to sketch the resulting circuit. Although the CMOS circuit thus obtained works well, it is somewhat complex. As an alternative, we consider a simplified circuit that furthermore implements additional logic. Specifically, Fig. 11.3 shows a clocked version of an SR flip-flop. Since the clock input from AND functions with the set and reset inputs, the flip-flop can be set or reset only when the clock ϕ is high. Observe that although the two cross-coupled inverters is the heart of the flip-flop core of the complementary CMOS type, only NMOS transistors are used for the set-reset circuitry. Nevertheless, since there is no conducting path between V_{DD} and ground (except during switching), the circuit does not dissipate any static power.

Except for the addition of clocking, the SR flip-flop of Fig. 11.3 operates in exactly the same way as its logic antecedent in Fig. 11.2. To illustrate, consider what happens when the flip-flop is in the reset state ($Q = 0$, $\bar{Q} = 1$, $v_Q = 0$, $v_{\bar{Q}} = V_{DD}$), and assume that we wish to set it. To do so, we arrange for a high (V_{DD}) signal to appear on the S input while R is held low at 0 V. Then, when the clock ϕ goes high, both Q_1 and Q_2 will conduct, pulling the

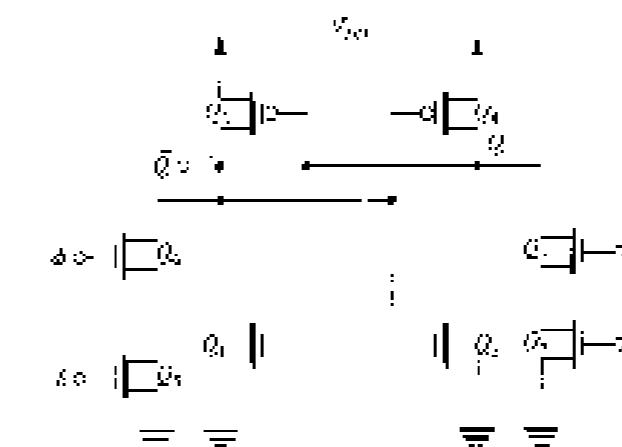


FIGURE 11.3 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ .

node v_{Q_1} down. If v_{Q_1} goes below the threshold of the (Q_1, Q_2) inverter, the inverter will switch states for at least long enough to switch states, and its output v_Q will rise. This increase in v_Q is fed back to the input of the (Q_1, Q_2) inverter, causing its output $v_{\bar{Q}}$ to go down even further. The regeneration process, characteristic of the positive-feedback latch, is now in progress.

The preceding description of the switching is predicated on two assumptions:

1. Transistors Q_1 and Q_2 supply sufficient current to pull the node \bar{Q}_1 down to a voltage at least slightly below the threshold of the (Q_1, Q_2) inverter. This is essential for the regeneration process to begin. Without this initial trigger, the flip-flop will fail to switch. In Example 11.1, we shall investigate the minimum W/L ratios that Q_1 and Q_2 must have to meet this requirement.
2. The set signal remains high for an interval long enough to cause regeneration to take over the switching process. An estimate of the minimum width required for the set pulse can be obtained as the sum of the interval during which $v_{\bar{Q}}$ is reduced from V_{DD} to $V_{DD}/2$, and the interval for the voltage v_Q to respond and rise to $V_{DD}/2$.

Finally, note that the symmetry of the circuit indicates that all the preceding comments apply equally well to the reset process.

PROBLEMS

The CMOS SR flip-flop in Fig. 11.3 is fabricated on a process technology for which $\alpha_C = 2.5 \mu\text{A/V}^2$, $C_{ox} = 50 \text{ fF}/\mu\text{m}^2$, $V_{DD} = 1V$, and $V_{TH} = 0.5 \text{ V}$. The inverters have $W/L_1 = 4 \mu\text{m}/2 \mu\text{m}$ and $W/L_2 = 10 \mu\text{m}/2 \mu\text{m}$. The four NMOS transistors in the set-reset circuit have equal W/L ratios. Determine the intrinsic value required for this W/L to ensure that the flip-flop will switch.

Solution

Figure 11.4 shows the relevant portion of the circuit for our present purposes. Observe that since regeneration has yet begun, we assume that $v_Q = 0$ and thus Q_2 will be conducting. The circuit is an ideal p-channel-NMOS gate, and our task is to select the W/L ratios for Q_1 and Q_2 so that v_{Q_1} at this time too is lower than $V_{DD}/2$ (the threshold of the Q_1, Q_2 inverter whose Q_1 and Q_2 are

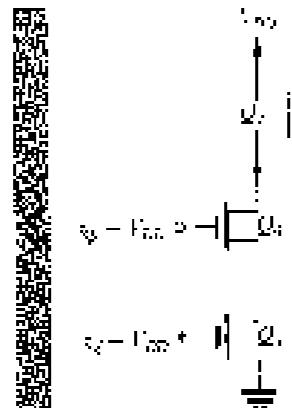


FIGURE 11.4 The relevant portion of the D flip-flop circuit of Fig. 11.3 for determining the minimum W/L ratios of Q_1 and Q_2 . Note that the top diagram uses the open-drain switch.

matched). The resistance required for Q_1 and Q_2 can be found by equating the current supplied by Q_1 at $v_Q = V_{DD}/2$ to the current supplied by Q_2 at $v_Q = V_{DD}/2$. To simplify matters, we assume that the series connection of $n^2 Q_1$ and Q_2 is approximately equivalent to a single transistor whose W/L is half the W/L of each of Q_1 and Q_2 . Now, since at $v_Q = V_{DD}/2$ both this equivalent transistor and Q_2 will be operating in the triode region, we can write

$$50 \times \frac{1}{2} \times \left(\frac{W}{L} \right) \left(\frac{V_{DD}}{2} - 1 \right) \times \frac{5}{2} = \frac{1}{2} \times \left(\frac{W}{L} \right)^2 \left(\frac{V_{DD}}{2} - 1 \right)$$

which leads to

$$\frac{W}{L} = 4 \quad \text{and} \quad \frac{W}{L} = 4$$

Resulting that this is an absolute minimum value, we would in practice select a ratio of 5 to 6.

EXERCISES

11.1 Design a D flip-flop using the following components: $(W/L)_1 = (W/L)_2 = 4$, and switching transistors with $W/L = 10$.

11.2 Design a D flip-flop using the following components: $(W/L)_1 = (W/L)_2 = 4$, and switching transistors with $W/L = 10$. Assume $(W/L)_3 = 1000$ and $(W/L)_4 = 10$. Assume that the load capacitors for the Q_1 and Q_2 nodes are 10 pF . Determine the high-to-low propagation delay due to the discharge current available to discharge the capacitance after the voltage falls to $0.1 V_{DD}/2$. Remember that C will be conducting a current until it adequately recharges the output node to its original value. Assume $(W/L)_5 = 1000$; 10 nA and use the methodology presented given in Example 11.1.

11.3 Design a D flip-flop using the following components: $(W/L)_1 = (W/L)_2 = 4$, and switching transistors with $W/L = 10$. Assume $(W/L)_3 = 1000$ and $(W/L)_4 = 10$. Assume that the load capacitors for the Q_1 and Q_2 nodes are 10 pF . Determine the high-to-low propagation delay due to the discharge current available to discharge the capacitance after the voltage falls to $0.1 V_{DD}/2$. Remember that C will be conducting a current until it adequately recharges the output node to its original value. Assume $(W/L)_5 = 1000$; 10 nA and use the methodology presented given in Example 11.1.

11.4 Design a broad pulse delay circuit of 50 D flip-flops as implemented in each chapter of the text. (a) 0.11 ns; (b) 0.27 ns; (c) 0.28 ns

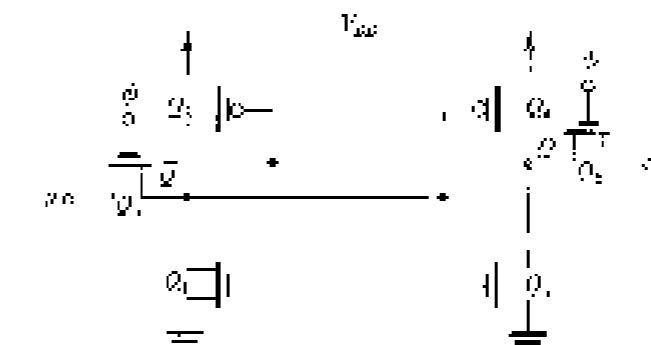


FIGURE 11.5 A simple CMOS implementation of a clocked SR flip-flop. This circuit is popular as the basic cell in the design of static random-access memory (SRAM) chips.

11.1.4 A Simpler CMOS Implementation of the Clocked SR Flip-Flop

A simpler implementation of a clocked SR flip-flop is shown in Fig. 11.5. Here, pass-transistor logic is employed to implement the clocked set-reset functions. This circuit is very popular in the design of static random-access memory (SRAM) chips, where it is used as the basic memory cell (Section 11.4.1).

11.1.5 D Flip-Flop Circuits

A variety of flip-flop types exist and can be synthesized using logic gates. CMOS circuit implementations can be obtained by simply replacing the gates with their CMOS circuit realizations. This approach, however, usually results in rather complex circuits. In many cases, simpler circuits can be found by taking a circuit design viewpoint, rather than a logic-design one. To illustrate this point, we shall consider the CMOS implementation of a very important type of flip-flop, the edge-triggered D flip-flop.

The D flip-flop is shown in block-diagram form in Fig. 11.6. It has two inputs, the data input D and the clock input ϕ . The complementary outputs are labeled Q and \bar{Q} . When the clock is low, the flip-flop is in the memory, or set, state, since changes on the D input line have no effect on the state of the flip-flop. As the clock goes high, the flip-flop acquires the logic level, that existed on the D line just before the rising edge of the clock. Such a flip-flop is said to be edge-triggered. Some implementations of the D flip-flop include direct set and reset inputs, that override the clocked operation just described.

A simple implementation of the D flip-flop is shown in Fig. 11.7. The circuit consists of two inverters connected in a positive-feedback loop, just as in the state latch of Fig. 11.1(m).

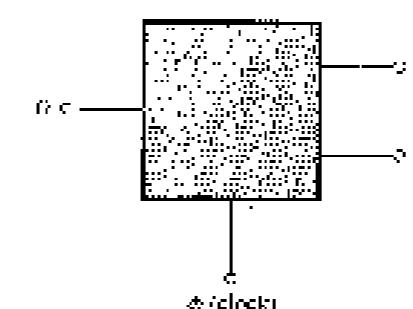


FIGURE 11.6 A block diagram representation of the D flip-flop.

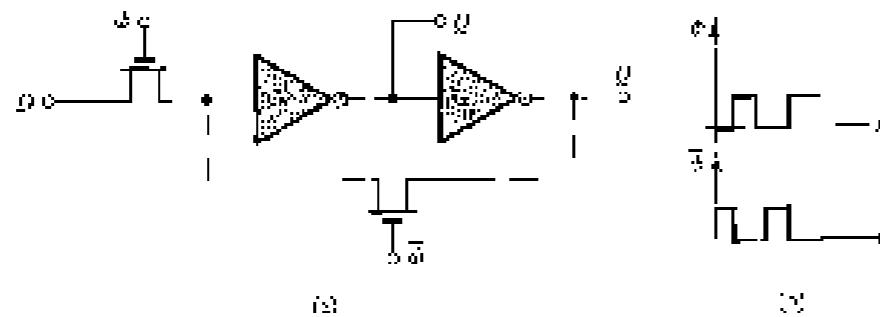


FIGURE 11.7 A simple implementation of the D flip-flop. The circuit in (a) utilizes the two-phase non-overlapping clock whose waveforms are shown in (b).

except that here the loop is closed for only part of the time. Specifically, the loop is closed when the clock is low ($\phi = \phi_2, \bar{\phi} = 1$). The input D is connected to the flip-flop through a switch that closes when the clock is high. Operation is straightforward: When ϕ is high, the loop is opened, and the input D is connected to the input of inverter G_1 . The capacitance at the input node of G_1 is charged to the value of D , and the capacitance in the front node of G_2 is charged to the value of \bar{D} . Then, when the clock goes low, the input line is isolated from the flip-flop, the feedback loop is closed, and the latch acquires the state corresponding to the value of D just before ϕ went down, providing an output $Q = D$.

From the preceding, we observe that the circuit in Fig. 11.7 combines the positive-feedback technique of static bistable circuits and the charge-storage technique of dynamic circuits. It is important to note that the proper operation of this circuit, and of many circuits that use clocks, is predicated on the assumption that ϕ and $\bar{\phi}$ cannot be simultaneously high at any time. This condition is defined by referring to the two clock phases as being non-overlapping.

An inherent drawback of the D flip-flop implementation of Fig. 11.7 is that during ϕ the output of the flip-flop simply follows the signal on the D input. (i.e., This can cause problems in certain logic design situations.) The problem is solved very effectively by using the master-slave configuration shown in Fig. 11.8(a). Before discussing its circuit operation, we note that although the switches are shown implemented with single NMOS transistors, CMOS transmission gates are employed in many applications. We are simply using the single-MOS transistor as a "switched capacitor" for a series switch.

The master-slave circuit consists of a pair of circuits of the type shown in Fig. 11.7, operated with strict, i.e., clock phases. Here, to emphasize that the two clock phases must be nonoverlapping, we denote them ϕ_1 and ϕ_2 , and clearly show the nonoverlap interval in the waveforms of Fig. 11.8(b). Operation of the circuit is as follows:

1. When ϕ_1 is high and ϕ_2 is low, the input is connected to the master latch whose feedback loop is opened, while the slave latch is isolated. Thus, the output Q remains at the value stored previously in the slave latch whose loop is now closed. The node capacitances of the master latch are charged to the appropriate voltages corresponding to the present value of D .
2. When ϕ_1 goes low, the master latch is isolated from the input data line. Then, when ϕ_2 goes high, the feedback loop of the master latch is closed, locking in the value of D . Further, its output is connected to the slave latch whose feedback loop is now open. The node capacitances in the slave are appropriately charged so that when ϕ_1 goes high again, the slave latch locks in the new value of D and provides it. (The output $Q = D$.)

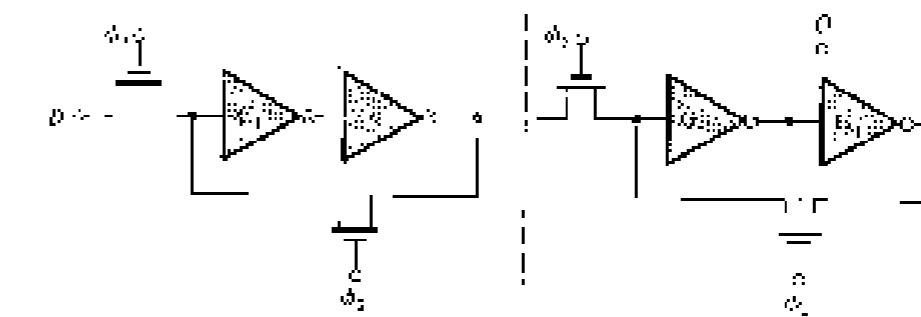


FIGURE 11.8 (a) Master-slave D flip-flop. The switches can be, and usually are, simple nodes with CMOS transmission gates. (b) Waveforms for the two-phase non-overlapping clock (a), (b).

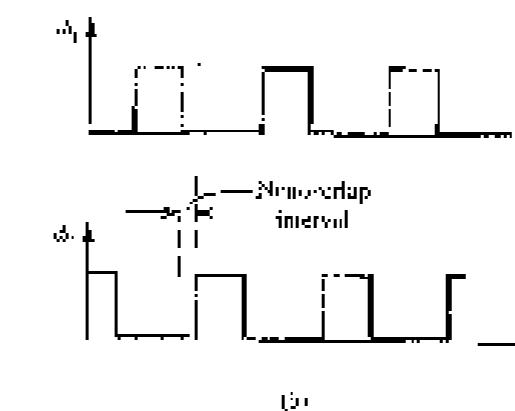


FIGURE 11.8 (a) Master-slave D flip-flop. The switches can be, and usually are, simple nodes with CMOS transmission gates. (b) Waveforms for the two-phase non-overlapping clock (a), (b).

From this description, we note that at the positive transition of clock ϕ_2 the output Q retains the value of D that existed on the D line at the end of the preceding clock phase, ϕ_1 . This output value remains constant for one clock period. Finally, note that during the nonoverlap interval both latches have their feedback loops open and we are relying on the node capacitances to maintain most of their charge. It follows that the nonoverlap interval should be kept reasonably short (perhaps one tenth or less of the clock period, and of the order of 1 ns or so in current practice).

11.2 MULTIVIBRATOR CIRCUITS

As mentioned before, the flip-flop has two stable states and is called a bistable multivibrator. There are two other types of multivibrator: monostable and astable. The monostable multivibrator has one stable state in which it can remain indefinitely. It has another quasi-stable state to which it can be triggered. The monostable multivibrator can remain in the quasi-stable state for a predetermined interval T , after which it automatically reverts to the stable state. In this way the monostable multivibrator generates an output pulse of duration T . This pulse duration is not necessarily related to the details of the triggering pulse, as is indicated schematically

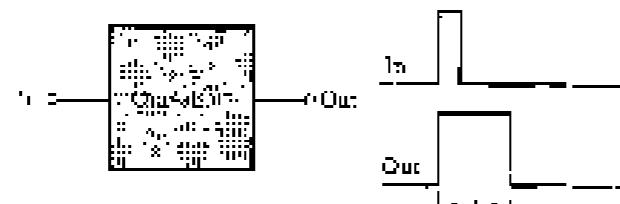


FIGURE 11.9 The inveritable multivibrator (one shot) as a functional block, shown to be triggered by a positive pulse. In addition, there are one shots that are triggered by a negative pulse.

in Fig. 11.9. The inveritable multivibrator can therefore be used as a pulse generator, where appropriately, a pulse generator. A metastable multivibrator is also referred to as a ring-shaker.

The metastable multivibrator has no stable states. Rather, it has two quasi-stable states, and it remains in each for random time intervals T_1 and T_2 . Thus after T_1 seconds in one of the quasi-stable states the bistable switches to the other quasi-stable state and remains here for T_2 seconds, after which it reverts back to the original state, and so on. The metastable multivibrator thus oscillates with a period $T = T_1 + T_2$ at a frequency $f = 1/T$, and it can be used to generate periodic pulses such as those required for clacking.

In Chapter 13 we will study astable and monostable multivibrator circuits that use op amps. In the following, we shall discuss monostable and astable circuits using logic gates. We also present an alternative, and very popular, oscillator circuit, the ring oscillator.

11.2.1 A CMOS Monostable Circuit

Figure 11.10 shows a simple and popular circuit for a monostable multivibrator. It is composed of two two-input CMOS NOR gates, G_1 and G_2 , a capacitor of capacitance C , and a resistor of resistance R . The input source V_T supplies the triggering pulses for the monostable multivibrator.

Commercially available CMOS gates have a special arrangement of diodes connected at their input terminals, as indicated in Fig. 11.11(a). The purpose of these diodes is to prevent the input voltage signal from rising above the supply voltage V_{DD} (by more than one diode drop) and from falling below ground voltage (by more than one diode drop). These clamping diodes have an important effect on the operation of the monostable circuit. Specifically, we shall be interested in the effect of these diodes on the operation of the inverter-connected gate G_2 . In this case, each pair of corresponding diodes appears in parallel, giving rise to the equivalent circuit in Fig. 11.11(b). While the diodes provide a low-resistance path to the power supply for voltages exceeding the power-supply limits, the input current for intermediate-state voltages is essentially zero.

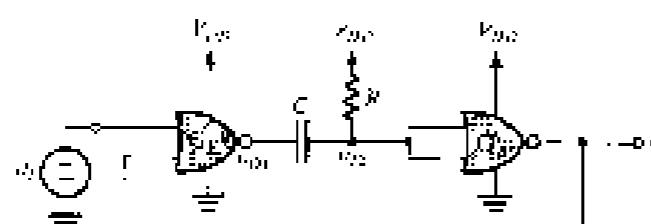


FIGURE 11.10 A monostable circuit using CMOS NOR gates. Signal source V_T supplies positive trigger pulses.

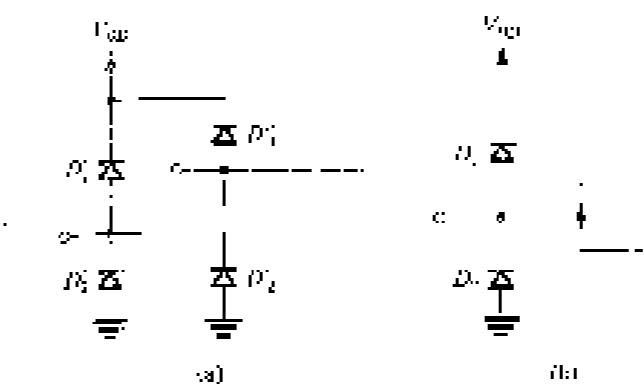


FIGURE 11.11 (a) Diode-clamped CMOS gate symbol. (b) Equivalent circuit when the two inputs of the gate are joined together. Note that the diodes are intended to prevent the device from being destroyed by destructive overvoltage due to static charge accumulation.

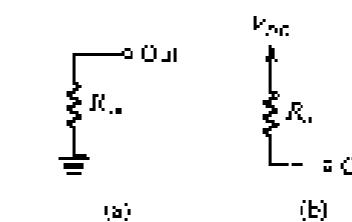


FIGURE 11.12 Output equivalent circuit of CMOS gate when the output is (a) low and (b) high.

To simplify matters we shall use the approach of output equivalent circuits of the gate, illustrated in Fig. 11.12. Figure 11.12(a) indicates that when the gate output is low, its output characteristic can be represented by a resistance R_{on} to ground, which is normally a few hundred ohms. In this state, current can flow from the external circuit to the output terminal of the gate; the gate is said to be sinking current. Similarly, the equivalent output circuit in Fig. 11.12(b) applies when the gate output is high. In this state, current can flow from V_{DD} through the output terminal of the gate into the external circuit; the gate is said to be sourcing current.

To see how the monostable circuit of Fig. 11.10 operates, consider the timing diagram given in Fig. 11.13. Here a short triggering pulse of duration t is shown in Fig. 11.13(a). In the following we shall neglect the propagation delays through G_1 and G_2 . These delays, however, set a lower limit on the pulse width $t > t_0$ (Fig. 11.12).

Consider first the stable state of the monostable circuit—that is, the state of the circuit before the trigger pulse is applied. The output of G_1 is high at V_{DD} , the capacitor is discharged, and the input voltage to G_2 is high at V_{DD} . Thus the output of G_2 is low, at ground voltage. This low voltage is fed back to G_1 ; since G_1 's input is low, the output of G_1 is high, as initially assumed.

Next consider what happens as the trigger pulse is applied. The output voltage of G_1 will go low. However, because G_1 will be sinking some current and because of its finite output resistance R_{on} , its output will not go all the way to 0 V. Rather, the output of G_1 drops by a value ΔV_1 , which we shall shortly evaluate.

The drop ΔV_1 is coupled through C (which acts as a short circuit during the transient) to the input of G_2 . Thus the input voltage of G_2 drops (from V_{DD}) by an identical amount ΔV_1 . Here, we note that during the transient there will be an instantaneous current flow from

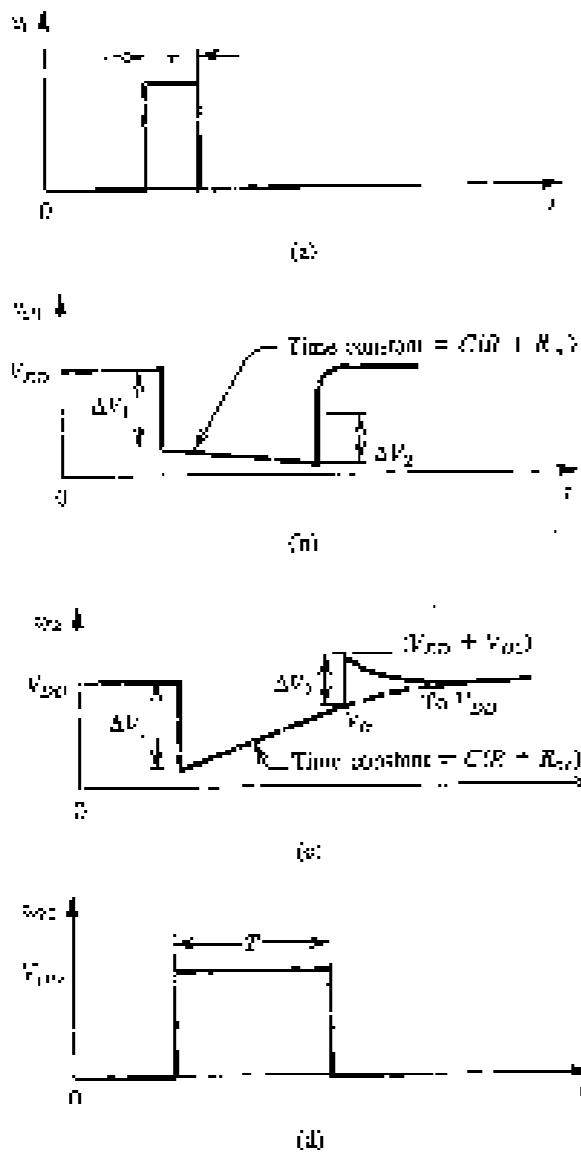


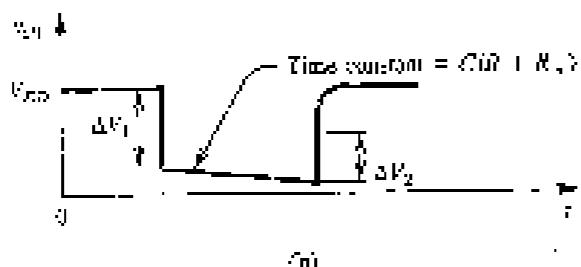
FIGURE 11.13 Timing diagrams for the metastable circuit (see Fig. 11.10).

V_{in} through R and C and into the output terminal of G_1 to ground. We thus have a voltage divider formed by R and R_{in} (note that the instantaneous voltage across C is zero) from which we can determine ΔV_1 as

$$\Delta V_1 = V_{in} \frac{R}{R + R_{in}} \quad (11.1)$$

Returning to G_2 , we see that the drop of voltage at its input causes its output to go high (to V_{DD}). This signal keeps the output of G_1 low even after the triggering pulse has disappeared. The circuit is now in the quasi-stable state.

We next consider operation in the quasi-stable state. The current through R , C , and R_{in} causes C to charge, and the voltage v_{o2} rises exponentially toward V_{DD} with a time constant

FIGURE 11.14 Circuit diagram during the charging of G_2 's output in the metastable pulse interval T .

$C(R + R_{in})$, as indicated in Fig. 11.17(a). The voltage v_{o2} will continue to rise until it reaches the value of the threshold voltage V_1 of inverter G_2 . At this time G_2 will switch and its output v_{o2} will go to 0 V, which will in turn cause G_1 to switch. The output of G_1 will attempt to rise to V_{DD} , but, as will become obvious shortly, its instantaneous rise will be limited to an amount ΔV_2 . This rise in v_{o1} is coupled back through C to the input of G_2 . Thus the input of G_2 will rise by an equal amount ΔV_2 . Note here that because of diode D_1 , between the input of G_2 and V_{DD} , the voltage v_{o1} can rise only to $V_{DD} - V_{D1}$, where V_{D1} (approximately 0.7 V) is the drop across D_1 . Thus from Fig. 11.14(c) we see that

$$\Delta V_2 = V_{DD} - V_{D1} - V_{o1} \quad (11.2)$$

Thus it is diode D_1 that limits the size of the increment ΔV_2 .

Because now v_{o2} is higher than V_{DD} (by V_{D1}), current will flow from the output of G_1 through C and then through the parallel combination of R and D_1 . This current discharges C until v_{o2} drops to V_{DD} and v_{o1} rises to V_{DD} . The discharging circuit is depicted in Fig. 11.14(d), from which we note that the existence of the diode causes the discharge to be a nonlinear process. Although the details of the waveform at the end of the pulse are not of immediate interest, it is important to note that the monostable circuit should not be triggered until the capacitor has been discharged, since otherwise the output obtained will not be the intended pulse, which the one shot is intended to provide. The capacitor discharge interval is known as the recovery time.

An expression can be derived for the pulse interval T by referring to Fig. 11.15(c) and expressing $v_{o2}(t)$ as

$$v_{o2}(t) = V_{DD} - \Delta V_1 e^{-\frac{t}{T_1}}$$

where $T_1 = C(R + R_{in})$. Substituting for $t = T$ and $v_{o2}(T) = V_{DD}$ and for ΔV_1 from Eq. (11.1) gives, after a little manipulation:

$$T = C(R + R_{in}) \ln \left(\frac{R}{R + R_{in}} \frac{V_{DD}}{V_{DD} - V_{D1}} \right)$$

EXERCISES

11.1. A 100-pF capacitor is connected to a 10-kΩ resistor in series with a 10-V DC source. If the current in the circuit is 1 mA, what is the voltage across the capacitor?

11.2. A 100-pF capacitor is connected to a 10-kΩ resistor in series with a 10-V DC source. If the current in the circuit is 1 mA, what is the voltage across the capacitor?

11.3. A 100-pF capacitor is connected to a 10-kΩ resistor in series with a 10-V DC source. If the current in the circuit is 1 mA, what is the voltage across the capacitor?

11.4. A 100-pF capacitor is connected to a 10-kΩ resistor in series with a 10-V DC source. If the current in the circuit is 1 mA, what is the voltage across the capacitor?

11.5. A 100-pF capacitor is connected to a 10-kΩ resistor in series with a 10-V DC source. If the current in the circuit is 1 mA, what is the voltage across the capacitor?

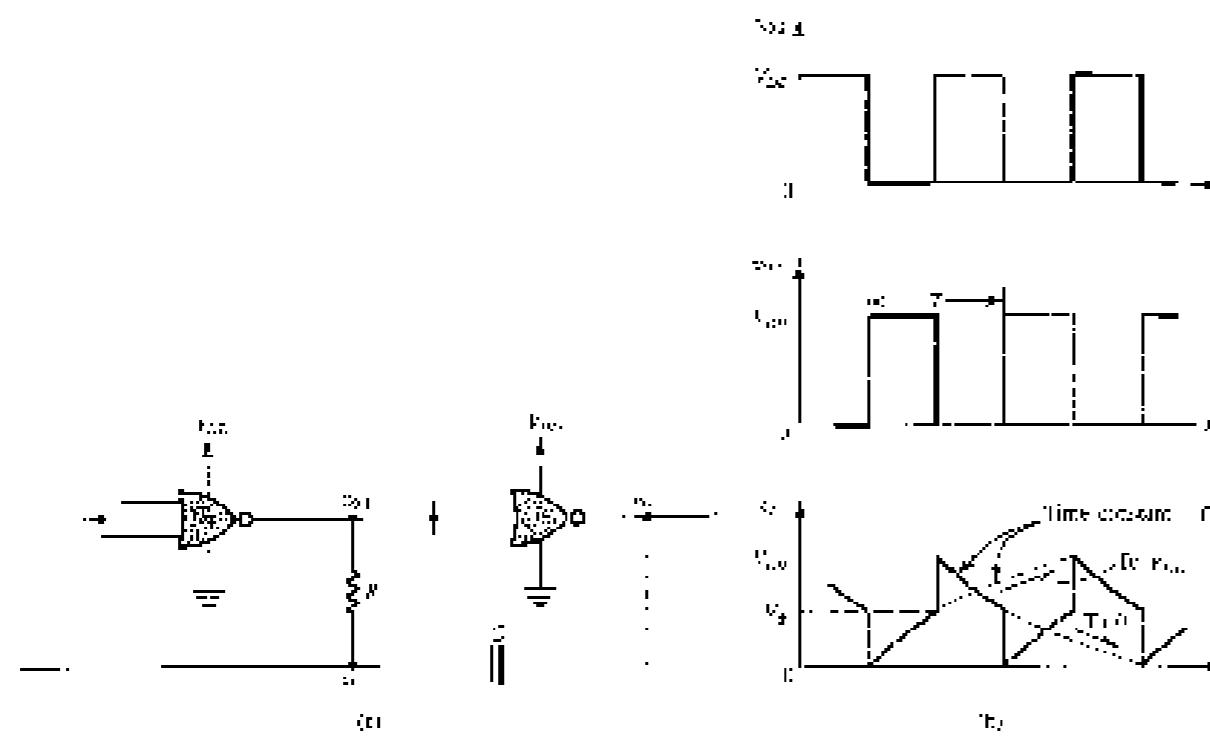


FIGURE 11.15 (a) A simple astable multivibrator circuit using CMOS logic. (b) Waveforms for the stable circuit. (c) The diodes in the gate inputs are assumed to be ideal and thus to limit the voltage to 0.7V.

11.2.2 An Astable Circuit

Figure 11.15(a) shows a popular astable circuit composed of two inverters connected NOR gates, a resistor, and a capacitor. We shall consider its operation by assuming that the NOR gates are of the CMOS family. However, to simplify matters we shall make some further approximations, neglecting the finite output resistance of the CMOS gate and assuming that the clamping diodes are ideal (thus have zero voltage drop when conducting).

With these simplifying assumptions, the waveforms of Fig. 11.15(b) are obtained. The reader is urged to examine the operation of this circuit in a step-by-step manner and verify that the waveforms shown indeed apply.¹

EXERCISE

- (11.3-4) The DC operating point of the circuit of Fig. 11.15(a) is $V_{DD} = 5\text{V}$, $R = 10\text{k}\Omega$, $C = 1\text{nF}$, and D_1 is an ideal diode. Find the steady-state values of the output voltage V_{out} and the capacitor voltage V_C .

¹ Practical circuits often use a large resistance in series with the input to G_1 . This minimizes the effect of diode conduction and allows v_0 to rise to a voltage greater than V_{DD} and, as well, to fall below zero.

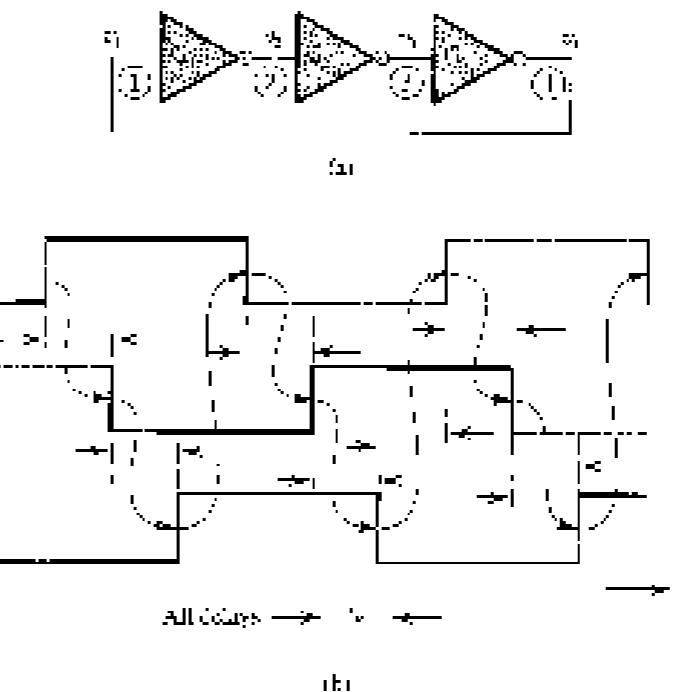
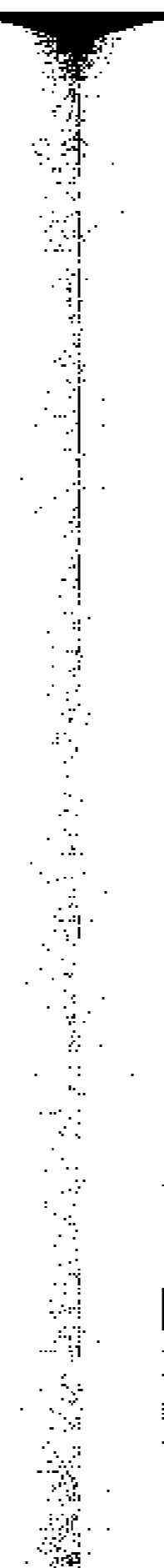


FIGURE 11.16 (a) A ring oscillator formed by connecting three inverters in series. Normally at least two inverters are used. (b) The resulting waveform. Observe that the circuit oscillates with frequency $1/T_{osc}$.

11.2.3 The Ring Oscillator

Another type of oscillator commonly used in digital circuits is the ring oscillator. It is formed by connecting an odd number of inverters in a loop. Although usually at least five inverters are used, we illustrate the principle of operation using a ring of three inverters, as shown in Fig. 11.16(a). Figure 11.16(b) shows the waveforms obtained at the outputs of the three inverters. These waveforms are identical in the sense that their edges have zero rise and fall times. Nevertheless, they will serve to explain the circuit operation.

Observe that a rising edge at node 1 propagates through gates 1, 2, and 3 to return inverted after a delay of $3t_p$. This falling edge then propagates, and returns with the original (rising) polarity after another $3t_p$ interval. It follows that the circuit oscillates with a period of $6t_p$ or equivalently with frequency $1/6t_p$. In general, a ring of $2N+1$ inverters (where N must be odd) will oscillate with period of $2Nt_p$ and frequency $1/2Nt_p$.

As a final remark, we note that the ring oscillator provides a relatively simple means for measuring the inverter propagation delay.

EXERCISE

- (11.3-5) The total propagation delay of a ring of three inverters of the same type (comparator delay) is determined to be $t_p = 1\text{ ns}$. Assume $V_{DD} = 5\text{V}$, $R = 10\text{k}\Omega$, and $C = 1\text{nF}$. Find the frequency of oscillation.

11.3 SEMICONDUCTOR MEMORIES: TYPES AND ARCHITECTURES

A computer system, whether a large mainframe or a microcomputer, requires memory for storing data and program instructions. Furthermore, within a given computer system there usually are various types of memory utilizing a variety of technologies and having different access times. Usually speaking, computer memory can be divided into two types: main memory and mass storage memory. The main memory is usually the most rapidly accessible memory and the one from which most, often all, instructions in programs are executed. The main memory is usually of the random-access type. A random-access memory (RAM) is one in which the time required for storing (writing) information and for retrieving (reading) it in operation is independent of the physical location within the memory in which the information is stored.

Random-access memories should be contrasted with serial or sequential memories, such as disks and tapes, from which data are available only in the sequence in which the data were originally stored. Thus, in a serial memory the time to access particular information depends on the memory location in which the required information is stored, and the average access time is longer than the access time of random-access memory. In a computer system, serial memory is used for mass storage items not frequently accessed, such as large parts of the computer operating system, are usually stored in a memory called a memory shell, or magnetic disk.

Another important classification of memory relates to whether it is a read/write or a read-only memory. Read/write (R/W) memory permits data to be stored and retrieved at comparable speeds. Computer systems require random-access read/write memory for data and program storage.

Read-only memories (ROM) permit reading at the same high speeds as R/W memories (or perhaps higher) but neither the writing operation. ROMs can be used to store a microprocessor executing system program. They are also employed in operations that require table lookup, such as finding the values of mathematical functions. A popular application of ROMs is their use in video game cartridges. It should be noted that read-only memory is usually of the random-access type. Nevertheless, in the digital circuit jargon, the acronym RAM usually refers to read/write, random-access memory, while ROM is used for read-only memory.

The regular nature of memory circuits has made them an ideal application for design of the circuits of the very large-scale integrated (VLSI) type. Indeed, at any moment, memory chips represent the state of the art in packing density and hence integration level. Beginning with the introduction of the 1K-1T chip in 1970, memory chip density has quadrupled about every 3 years. At the present time, chips containing 256M bits¹ are commercially available, while multigigabit memory chips are being tested in research and development laboratories. In this and the next two sections, we shall study some of the basic circuits employed in VLSI RAM chips. Read-only memory circuits are studied in Section 11.6.

11.3.1 Memory-Chip Organization

The bits on a memory chip are addressable either individually or in groups of 4 to 4⁴. As an example, a 64M-bit chip in which all bits are individually addressable is said to be organized as 32M words \times 1 bit (or simply 32M \times 1). Such a chip needs a 26-bit address ($2^6 = 65,536$) (64M). On the other hand, the 64M-bit chip can be organized as 16M words \times 4 bits

¹The capacity of a memory chip is defined by information in binary digits (bit) is measured in K-bit and M-bit units, where 1K = 2^{10} bits; and 1M = $2^{20} = 1024 \times 1024 = 1.048 \times 10^6$ bits. Thus a 32M-bit chip contains 65,536,000 bits of memory.

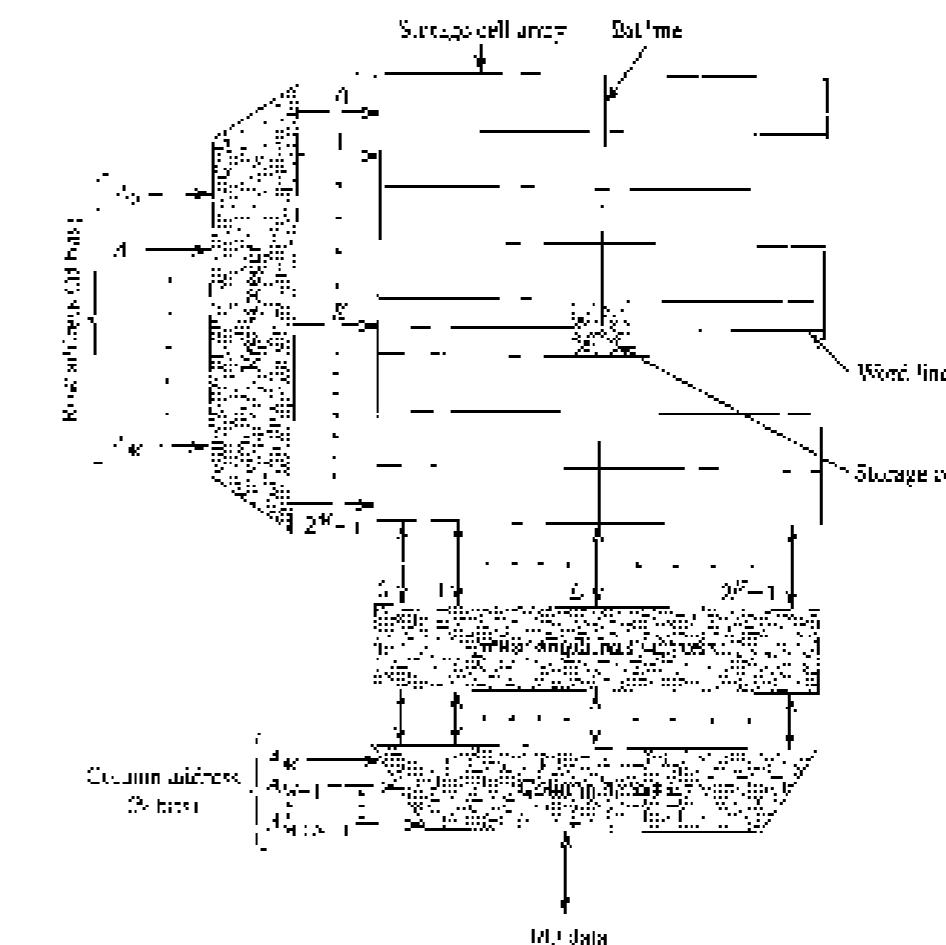


FIGURE 11.17 A $2^{10} \times 2^{10}$ memory chip organized as a matrix of 2^{10} rows $\times 2^{10}$ columns.

(256M \times 1), in which case a 24-bit address is required. For simplicity we shall assume in our subsequent discussion that all the bits on a memory chip are individually addressable.

The bulk of the memory chip consists of the cells in which the bits are stored. Each memory cell is an electronic circuit capable of storing one bit. We shall study memory cell circuits in Section 11.4. For reasons that will become clear shortly, it is desirable to physically organize the storage cells on a chip in a square or a nearly square matrix. Figure 11.17 illustrates such an organization. The cell matrix has 2^M rows and 2^N columns, for a total storage capacity of 2^{M+N} . For example, a 1M-bit square matrix would have 1024 rows and 1024 columns ($M = N = 10$). Each cell in the array is connected to one of the 2^M row lines, known rather loosely, but universally, as word lines, and to one of the 2^N column lines, known as digit lines or, more commonly, bit lines. A particular cell is selected for reading or writing by activating its word line and its bit line.

Activating one of the 2^M word lines is performed by the row decoder, a combinational logic circuit that selects (raises the voltage of) the particular word line whose bit address is applied to the decoder input. The address bus is denoted A_0, A_1, \dots, A_{M-1} . When the k th word line is activated for, say, a read operation, all 2^N cells in row k will provide their contents in their respective bit lines. Thus, if the cell in column L (Fig. 11.17) is storing a 1, the voltage

of bit-line number k , will be sensed, usually by a small voltage, say 0.1 V to 0.2 V. The readout voltage is small because the cell is small. It is an iterate design decision, since the number of cells is very large. The small readout signal is applied to a sense amplifier connected to the bit line. As Fig. 11.17 indicates, there is a sense amplifier for every cell line. The sense amplifier provides a full-swing digital signal (from 0 to 1.5 V) as output. The signal, together with the output signals from all the other cells in the selected row, is then delivered to the column decoder. The column decoder selects the signal at the particular column whose k th address is applied to the decoder input (the address bits are denoted A_0, A_1, \dots, A_{m-1}) and connects this signal to appear on the chip input/output (I/O) data line.

A write operation proceeds in a similar manner. The data bit to be stored (1 or 0) is applied to the I/O line. The cell in which the data bit is to be stored is selected through the combination of its row address and its column address. The sense amplifier of the selected cell is actuated to write the applied signal into the selected cell. Circuits for sense amplifiers and address decoders will be studied in Section 11.5.

Before leaving the topic of memory organization (or memory chip architecture), we wish to mention a relatively recent innovation in organization dictated by the exponential increase in chip density. To appreciate the need for a change, note first that the number of cells in the array increases, the physical lengths of the word lines and the bit lines increase. This has occurred even though for each new generation of memory chips, the transistor size has decreased (presently, CMOS process technologies with 0.1–0.3 μm feature size are utilized). The net increase in word-line and bit-line lengths increases their total resistance and capacitance, and thus slows down the transition response. That is, as the lines lengthen, the exponential rise of the voltage of the word line becomes slower, and it takes longer for the cells to be activated. This problem has been solved by partitioning the memory chip into a number of blocks. Each of the blocks has its own row, column address, and bit lines, but the data selected come from only one of the blocks. Block selection is achieved by using an appropriate number of the address bits as a block address. Such an architecture can be thought of as three-dimensional rows, columns, and blocks.

11.3.2 Memory-Chip Timing

The memory access time is the time between the initiation of a read operation and the appearance of the output data. The memory cycle time is the minimum time allowed between two consecutive memory operations. To be on the conservative side, a memory operation is usually taken to include both read and write (in the same location). MOS memory have access and cycle times in the range of a few to a few hundred nanoseconds.

EXERCISES

- 11.7 A typical SRAM cell is shown in Fig. 11.18. Consider the cell to be initially in the state $Q = 1$. If the word line (W) is raised to 1.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.8 Consider the SRAM cell of Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.9 Consider the SRAM cell of Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.10 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.11 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.12 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.13 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.14 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.15 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.16 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.17 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.18 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.19 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.20 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.21 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.22 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.23 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.24 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.25 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.26 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.27 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.28 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.29 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.30 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.31 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.32 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.33 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.34 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.35 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.36 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.37 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.38 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.39 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.40 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.41 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.42 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.43 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.44 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.45 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.46 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.47 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.48 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.49 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.50 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.51 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.52 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.53 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.54 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.55 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.56 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.57 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.58 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.59 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.60 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.61 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.62 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.63 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.64 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
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- 11.67 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.68 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.69 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and Q_2 are fully turned on.
- 11.70 A SRAM cell is shown in Fig. 11.18. If the word line (W) is held at 1.5 V, and the bit line (B) is held at 0.5 V, what is the value of Q ? Assume that the access transistors Q_1 and $Q_2</math$

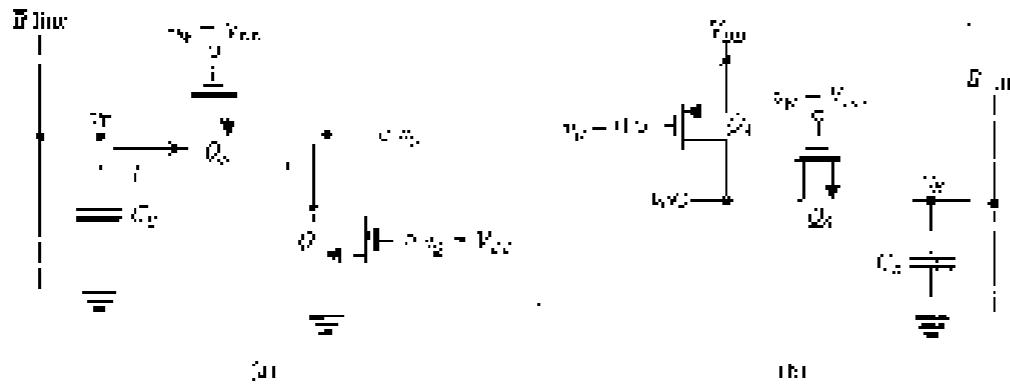


FIGURE 11.19 Relevant parts of the SRAM cell during read operation to determine the cell voltage at logic 1. Note that initially $v_p = V_{DD}$ and $v_n = 0$. Also note that the A and B lines are initially precharged to a voltage of about $V_{DD}/2$. However, in Example 11.2, it is assumed for simplicity that the precharge voltage is V_{DD} .

usually $V_{DD}/2$. (The circuit for precharging will be shown in Section 11.5 in conjunction with the sense amplifiers.) When the word line is selected and Q_1 and Q_2 are turned on, we see that current will flow from V_{DD} through Q_1 and Q_2 onto bit line B , charging the capacitance of line B . On the other side of the circuit, current will flow from the precharged bit line through Q_3 and Q_4 to ground, thus discharging C_A . It follows that the relevant parts of the circuit during a read operation are those shown in Fig. 11.19.

From this description, we note that during a read "1" operation, the voltage across C_A will rise and that across C_B will fall. Thus, a differential voltage v_{AB} develops between bit line B and bit line A . Usually, only 0.2 V or so is required for the sense amplifier to detect the presence of a 1 at the cell. Observe that the cell must be designed so that the charges in v_p and v_n are small enough to prevent the flip-flop from changing state during readout. The read operation in an SRAM is nondestructive. Typically, each of the inverters is designed so that Q_1 and Q_2 are matched, thus placing the inverter threshold at $V_{DD}/2$. The access transistors are usually made two to three times wider than Q_1 of the inverters.

Example 11.2

The purpose of this example is to analyze the dynamic operation of the CMOS SRAM cell of Fig. 11.18. Assume that the cell is fabricated in a process technology for which $\mu_p C_{ox} = 50 \text{ fA/V}^2$, $\mu_n C_{ox} = 20 \text{ fA/V}^2$, $V_{DD} = -V_{SS} = 1 \text{ V}$, $V_T = 0.6 \text{ V}$, $\gamma = 0.5 \text{ V}^{-1}$, and $T_{ox} = 5 \text{ nm}$. Let the cell be read at time $t = 0$, $V_{DD} = 10 \text{ mV}$, and let the access resistance have $R_{AA} = 10 \Omega$. Assuming that the cell is reading a 1 and that the capacitance of each bit line is 1 pF, determine the time required to develop an output voltage of 0.2 V. To simplify the analysis, assume that the B and A lines are precharged to V_{DD} .

Solution

We note at the outset that the dynamic analysis of this circuit is complex, and we must therefore make a number of simplifying assumptions. Of course, a precise analysis can always be obtained using simulation. However, much insight can be gained from even an approximate paper-and-pencil analysis.

Refer to Fig. 11.19 and recall that initially $v_p = V_{DD}$, $v_n = 0$, and $v_p = v_n = V_{DD}$. We see immediately that the circuit in Fig. 11.19(b) will not be conducting, and thus v_p will remain constant at V_{DD} . Turning our attention then to the circuit in Fig. 11.19(a), we observe that since v_p will change by only 0.2 V (i.e., from 1 V to 1.2 V) during the readout process, transistor Q_3 will be operating in saturation, and thus C_A will be discharged with a constant current, I_3 . But if Q_3 were to conduct in saturation, v_p would rise. We note, however, that this rise will not exceed the threshold of inverter Q_1 (V_T), which is $V_{DD}/2$, since the peak-to-transition voltage of inverters are matched. There will be a brief interval during which v_p will change by small positive capacitance between node Q_1 and ground as v_p above V_T sufficient to operate Q_1 in the triode mode at a current I_1 equal to I_3 . The current I_1 can then be expressed as

$$I_1 = \mu_p C_{ox} \left(\frac{V}{L_{Q1}} \right) \left(V_{DD} - V_T \right)^2 \left(1 + \frac{1}{2} \frac{\gamma}{V} \right)$$

where we have assumed that v_p will remain constant at V_{DD} . Since the source of Q_1 is at ground, $V_s = -V_D$ and,

$$I_1 = 50 \times \frac{4\pi}{2} (1.5 - 1.05 + \frac{1}{2} \cdot \frac{0.6}{1})$$

For Q_2 , we can write

$$I_2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{V}{L_{Q2}} \right) \left(V_{DD} - V_p - V_{DD} \right)^2$$

where the threshold voltage V_T can be determined from

$$V_T = 1 + 0.5 \sqrt{V_D + 0.6} \quad (11.2)$$

Since we do not yet know v_p , we need to solve by iteration. For a first iteration, we set $V_D = V_T = 1 \text{ V}$, thus I_2 will be

$$I_2 = 1 \times 50 \times \frac{4\pi}{2} (1 - 1.0 - 1)^2$$

Now equating I_1 from Eq. (11.2) to I_2 from Eq. (11.3) and solving for v_p results in $v_p = 1.05 \text{ V}$. As a second iteration, we use the value of v_p in Eq. (11.2) to determine V_T . The result is $V_T = 1.4 \text{ V}$. This value is then used in the expression for I_2 and the process repeated, with the result that $v_p = 1.6 \text{ V}$. This is close enough to the original value, and no further iteration seems warranted. The current I_1 can now be determined: $I_1 = 0.2 \text{ nA}$. Observe that v_p is indeed less than $V_{DD}/2$, and thus the flip-flop cell is not switched from a "1" to a "0". In fact, V_p for this iteration is 2.125 V; thus the assumption that v_p stays at V_{DD} is justified, although v_p will change somewhat at point we shall now pursue any further in this approximate analysis.

We can now determine the maximum 0.2 V decrement to appear on the B line from

$$\Delta t = \frac{C_B V}{I_2}$$

Thus,

$$\Delta t = \frac{1 \times 10^{-12} \times 0.2}{0.2 \times 10^{-9}} = 0.4 \text{ ns}$$

We should point out that Δt is only one component of the delay encountered in the read operation. Another significant component is due to the finite rise time of the voltage on the word line. Indeed, even the calculation of Δt is optimistic, since the word line will have only reached a voltage lower than V_{DD} when the process of discharging C_A takes place.

Another, even more approximate, final solution can be obtained by observing that in the circuit of Fig. 11.20(a), Q_1 and Q_2 have equal gate voltages (V_{G1}) and are connected in series. We may assume that they are approximately equivalent to a single transistor with $n = 1$, $r_{DS} = \infty$.

$$(AV)^2 I_{D1} = \frac{V_{DD} - V_{G1}}{\left(\frac{V_{DD} - V_{G1}}{r_{DS} I_{D1}} + \frac{1}{2}\right)} = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}$$

The equivalent transistor will operate in saturation, so its current I will be

$$I = \frac{1}{2} \times R_s \times \frac{V_{DD} - V_{G1}}{2} = 5.57 \text{ mA}$$

I is only 14% greater than the value found earlier. The voltage v_2 can be found by multiplying I by the approximate value of r_{DS} of 10, in the triode region:

$$v_2 = 1.75 \times 10^{-9} \times \frac{1}{2} \times 5.57 = 2.5 \text{ mV}$$

Hence,

$$v_2 = 0.57 \times 2.5 = 1.4 \text{ V}$$

Again, this is reasonably close to the value found earlier.

The Write Operation. Next we consider the write operation. Assume that the cell is initially storing a 1, $v_{G1} = V_{DD}$, and $v_{G2} = 0$ and that we wish to write a 0. To do this, the B line is lowered to 0 V and the B line is raised to V_{DD} , thus reverse biasing the cell, as selected by raising the word line to V_{DD} . Figure 11.20 shows the relevant parts of the circuit during the interval in which node \bar{Q} is being pulled up towards the threshold voltage $V_{DD}/2$ (Fig. 11.20(a)) and node Q is being pulled down toward $V_{DD}/2$ (Fig. 11.20(b)). Capacitors C_2 and C_3 are the parasitic capacitances to nodes Q_1 and Q_2 , respectively. An approximate analysis can be performed on either circuit to determine the time required for latching to take place. Note that the negative feedback that causes the flip flop to switch will begin when either v_2 or v_3 reaches $V_{DD}/2$. When this happens, the positive feedback takes over, and the circuits in Fig. 11.20 no longer apply.

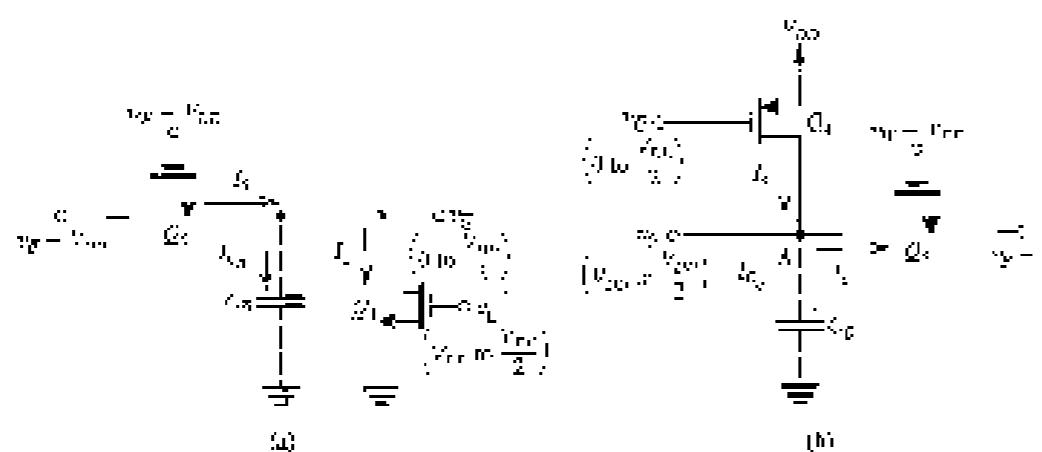


FIGURE 11.20 Equivalent parts of the SRAM circuit during a write operation. In part (a), the SRAM has a “write 1” and a “writing writer.” These equivalent circuits apply before writing takes place. (a) The circuit is pulling node \bar{Q} down toward $V_{DD}/2$. (b) The circuit is pulling node Q down toward $V_{DD}/2$.

We shall briefly explain the operation of the circuit in Fig. 11.20, leaving the analysis for the reader to perform in Exercise 11.9 and Problems 11.21 and 11.24. Consider first the circuit in Fig. 11.20(a), and note that Q_1 will be operating in saturation. Initially, its source voltage will be 0, and thus its V_g will be equal to V_{DD} . At 0 initially, Q_2 will be off because its drain voltage is zero. The current I_2 will initially flow into C_2 , charging it up, and thus v_2 will rise and Q_1 will conduct. Q_1 will be in the triode region and its current I_1 will subtract from I_2 , reducing the current available for charging C_2 . Eventually, as v_2 rises, V_g will increase owing to the body effect, and I_2 will reduce. Another effect caused by the circuit in Fig. 11.20(b) is that v_3 will be falling from V_{DD} toward $V_{DD}/2$. This will cause a corresponding decrease in the current I_3 . Despite all these complications, one can easily calculate an approximate average value for the capacitor charging current I_{avg} over the interval beginning with $(v_2 = V_{DD}, v_3 = 0)$ and ending with $v_2 = V_{DD}/2, v_3 = V_{DD}/2$. We can then use this current value to determine the time for the voltage across C_2 to increase by $V_{DD}/2$.

The circuit in Fig. 11.20(b) operates in much the same fashion except that neither of the two transistors is susceptible to the body effect. Thus, this circuit will provide C_3 with a larger discharge current than the current provided by the circuit in Fig. 11.20(a) to charge C_2 . The result will be that C_2 will discharge faster than C_3 will charge. In other words, v_2 will reach $V_{DD}/2$ before v_3 does. It follows that an estimate of this component of the write delay time can be obtained by considering only the circuit in Fig. 11.20(b).

Another component of write delay is that taken up by the switching action of the flip flop. This can be approximated by the delay time of one inverter.

EXERCISE

11.9. Consider the SRAM circuit shown in Fig. 11.20(b). Assuming that the SRAM has the parameters as specified in Exercise 11.8, we wish to determine the interval t_c required for C_3 to discharge, during which v_3 falls from V_{DD} to $V_{DD}/2$. (a) At the beginning of time t_c , the flip flop is set such that $v_2 = V_{DD}$ and $v_3 = 0$. Calculate the voltage across C_3 at time t_c . (b) Calculate the interval t_c during which v_3 falls from V_{DD} to $V_{DD}/2$. (c) Calculate the total time of the memory cell during the write operation.

From the results of Exercise 11.9, we note that this component of write delay is much smaller than the corresponding component in the read operation. This is because in the write operation, only the small cap. C_3 needs to be charged (or discharged), whereas in the read operation, we have to charge (or discharge) the much larger capacitance of the B or \bar{B} lines. In the write operation, the B and \bar{B} line capacitances are charged (and discharged) relatively quickly by the driver circuitry. The end result is that the delay time in the write operation is dominated by the word-line delay.

¹ Implicit in this statement is the assumption that both v_2 and v_3 will reach $V_{DD}/2$ simultaneously. As will be seen shortly, this is not the case. Nevertheless, it is a reasonable assumption to make for the purpose of obtaining an approximate estimate of the write delay time.

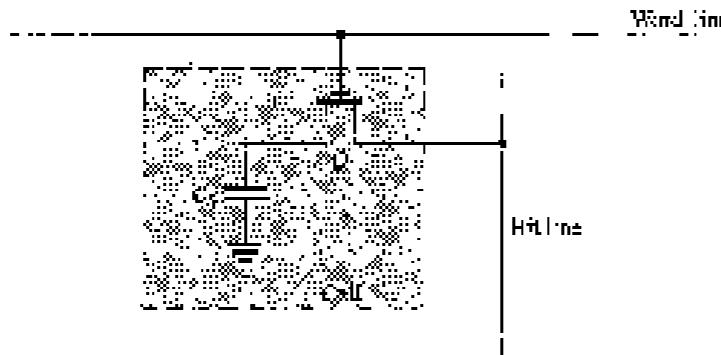
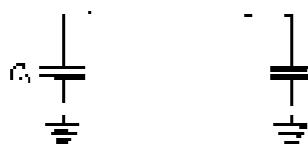


FIGURE 11.21 Top-view transistor dynamic RAM cell.

FIGURE 11.22 When the voltage of the selected word line is raised, the transistors conduct, thus connecting the storage capacitor C_s to the bit-line capacitance C_b .

11.4.2 Dynamic Memory Cell

Although a variety of DRAM storage cells have been proposed over the years, a particular cell, shown in Fig. 11.21, has become the industry standard. The cell consists of a single n-channel MOSFET, known as the access transistor, and a storage capacitor C_s . The cell is appropriately known as the one-transistor cell.¹ The gate of the transistor is connected to the word line, and its source (drain) is connected to the bit line. Observe that only one bit line is used in DRAMs, whereas in SRAMs both the bit and bid lines are utilized.

The DRAM cell stores its bit of information as charge on the cell capacitor C_s . When the cell is storing a 1, the capacitor is charged to $(V_{DD} - V_t)$; when a 0 is stored, the capacitor is discharged to a zero voltage.² Because of leakage effects, the capacitor charge will leak off, and hence the cell must be refreshed periodically. During refresh, the cell content is read and the data bit is rewritten, thus restoring the capacitor voltage to its proper value. The refresh operation must be performed every 5 ms to 10 ms.

Let us now consider the DRAM operation in more detail. As in the static RAM, the row decoder selects a particular row by raising the voltage of its word line. This causes all the access transistors in the selected row to become conductive, thereby connecting the storage capacitors of all the cells in the selected row to their respective bit lines. Thus the cell capacitor C_s is connected in parallel with the bit-line capacitance C_b , as indicated in Fig. 11.22. Here, it should be noted that C_s is typically 30 fF to 50 fF, whereas C_b is 10 to 50 times larger. Now, if the operation is a read, the bit line is precharged to $V_{DD}/2$. To find the charge

¹ The name was originally used to distinguish this cell from earlier ones utilizing three transistors.

² The reason that the 0 level is less than V_{DD} by the magnitude of the threshold V_t is as follows: Consider a write-1 operation. The word line is at V_{DD} and the bit line is at V_{DD} and the transistor is conductive, charging C_s . The transistor will cease conduction when the voltage on C_s reaches $(V_{DD} - V_t)$ where V_t is higher than V_s because of the body effect. We have analyzed this situation at length in Section 10.5 in connection with precharge logic.

in the voltage on the bit line resulting from connecting a cell capacitor C_s to it, let the initial voltage on the cell capacitor be V_{C2} ($V_{C2} > V_{DD} - V_t$ when a 1 is stored, but $V_{C2} = 0$ V when a 0 is stored). Using charge conservation, we can write

$$C_s V_{C2} + C_b \frac{V_{DD}}{2} = (C_s + C_b) \left(\frac{V_{DD}}{2} + \Delta V \right),$$

from which we can obtain for ΔV

$$\Delta V = \frac{C_s}{C_s + C_b} \left(V_{DD} - \frac{V_{C2}}{2} \right) \quad (11.6)$$

and since $C_b \gg C_s$,

$$\Delta V = \frac{C_s}{C_b} \left(V_{DD} - \frac{V_{C2}}{2} \right) \quad (11.7)$$

Now, if the cell is storing a 1, $V_{C2} = V_{DD} - V_t$, and

$$\Delta V(1) = \frac{C_s}{C_b} \left(\frac{V_{DD}}{2} - V_t \right) \quad (11.8)$$

whereas if the cell is storing a 0, $V_{C2} = 0$, and

$$\Delta V(0) = -\frac{C_s}{C_b} \left(\frac{V_{DD}}{2} \right) \quad (11.9)$$

Since usually C_b is much greater than C_s , these readout voltages are very small. For example, for $C_b = 40 C_s$, $V_{DD} = 5$ V, and $V_t = 1.5$ V, $\Delta V(0)$ will be about -80 mV, and $\Delta V(1)$ will be 35 mV. This is a best-case scenario, for the 1 level in the cell might very well be below $(V_{DD} - V_t)$. Furthermore, in modern memory chips, V_{DD} is 3.3 V or even lower. In any case, we see that a stored 1 in the cell results in a small positive increment in the bit-line voltage, whereas a stored zero results in a small negative increment. Observe also that the readout process is destructive, since the resulting voltage across C_s will no longer be $(V_{DD} - V_t)$ or 0.

The change of voltage on the bit line is detected and amplified by the column sense amplifier. The amplified signal is then impressed on the storage capacitor, thus restoring its signal to the proper level (V_{DD} , 0, or 0). In this way, all the cells in the selected row are refreshed. Simultaneously, the signal at the output of the sense amplifier of the selected column is fed to the data-output line of the chip through the action of the column decoder.

The write operation proceeds similarly to the read operation, except that the data bit to be written, which is impressed on the data input line, is applied by the column decoder to the selected bit line. Thus, if the data bit to be written is a 1, the bit-line voltage is raised to V_{DD} (i.e., C_s is charged to V_{DD}). When the access transistor of the particular cell is turned on, its capacitor C_s will be charged to $V_{DD} - V_t$ thus a 1 is written in the cell. Simultaneously, all the other cells in the selected row are simply refreshed.

Although the read and write operations result in systematic refreshing of all the cells in the selected row, provision must be made for the periodic refreshing of the entire memory every 5 to 10 ms, as specified for the particular chip. The refresh operation is carried out in a *burst mode*: one row at a time. During refresh, the chip will not be available for read or write operations. This is not a serious matter, however, since the interval required to refresh the entire chip is negligibly less than 2% of the time between refresh cycles. In other words, the memory chip is available for normal operation more than 98% of the time.

EXERCISES

- 11.10 In a given column, the bit line voltage is $V_{BL} = 0.1V$, $V_{BL\bar{}} = 5.0V$. Ignoring the body effect, calculate the output voltage if the word line is applied. What is the output voltage if the bit line is applied? Assume $V_{DD} = 5.0V$.
- 11.11 A 4x4 SRAM chip has a total of 16 memory cells. If each cell requires 1.0 pF of load, and each cell has a 1.0 pF load, determine the dimensions of the peripheral circuitry (e.g., sense amplifiers, decoders, address buffers) in the chip area, assuming the area of the peripheral circuitry is 10% of the total chip area.
- 11.12 A 4x4 SRAM chip has a total of 16 memory cells. If each cell requires 1.0 pF of load, and each cell has a 1.0 pF load, determine the dimensions of the peripheral circuitry (e.g., sense amplifiers, decoders, address buffers) in the chip area, assuming the area of the peripheral circuitry is 10% of the total chip area.

11.5 SENSE AMPLIFIERS AND ADDRESS DECODERS

Having studied the circuits commonly used to implement the storage cells in SRAMs and DRAMs, we now consider some of the other important circuit blocks in a memory chip. The design of these circuits, commonly referred to as the *memory peripheral circuitry*, presents exciting challenges and opportunities to integrated circuit designers. Improving the performance of peripheral circuits can result in denser and faster memory chips that dissipate less power.

11.5.1 The Sense Amplifier

Next to the storage cells, the sense amplifier is the most critical component in a memory chip. Sense amplifiers are essential to the proper operation of DRAMs, and their use in SRAMs results in speed and area improvements.

A variety of sense amplifier designs are in use, some of which closely resemble the active load CMOS differential amplifier studied in Chapter 7. Here, we describe a differential sense amplifier that employs positive feedback. Because the circuit is differential, it can be employed directly in SRAMs where the SRAM cell utilizes both the B and \bar{B} lines. On the other hand, the one-bit-per-cell DRAM circuit we studied in Section 11.4.2 is a single-ended circuit, utilizing one bit line only. The DRAM circuit, however, can be made to resemble a differential signal source through the use of the "dummy cell" technique, which we shall discuss shortly. Therefore, we shall assume that the memory cell whose output is to be amplified develops a difference output voltage between the B and \bar{B} lines. This signal, which can range between 30 μ V and 500 μ V depending on the memory type and cell design, will be applied to the input terminals of the sense amplifier. The sense amplifier in turn responds by providing a full-swing $\pm 1.0V$ signal at its output terminals. The particular amplifier circuit we shall discuss here has a rather unusual property: *its output and input terminals are the same!*

A Sense Amplifier with Positive Feedback Figure 11.23 shows the sense amplifier together with some of the other column circuitry of a RAM chip. Note that the sense amplifier is nothing but the familiar ladder formed by cross-coupling two CMOS inverters. One inverter is implemented by transistors Q_1 and Q_2 , and the other by transistors Q_3 and Q_4 . Transistors Q_5 and Q_6 act as switches that connect the sense amplifier to ground and V_{DD} only when data-sampling occurs. Otherwise, Q_5 is low and the sense amplifier is turned off. This conserves power, an important consideration because usually there is one sense amplifier per column, resulting in thousands of sense amplifiers per chip. Note again,

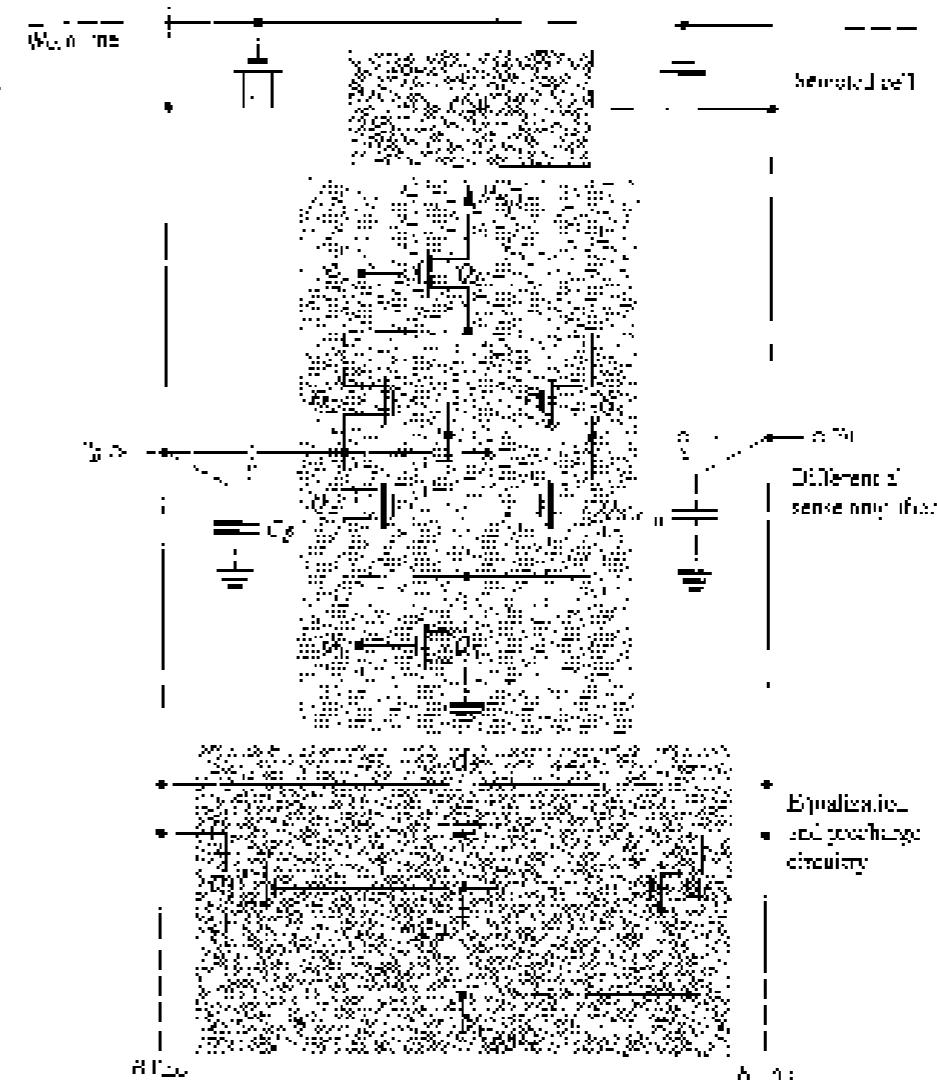


FIGURE 11.23 A differential sense amplifier connected to the bit lines of a particular column. This arrangement can be used directly for SRAMs, while to utilize both the B and \bar{B} lines, DRAMs can be built into a "dummy cell" arrangement shown in Fig. 11.25.

that terminals x and y are both the input and the output terminals of the amplifier. As indicated, these I/O terminals are connected to the B and \bar{B} lines. The amplifier is required to detect a small signal appearing between B and \bar{B} , and to amplify it to provide a full-swing signal at B and \bar{B} . For instance, if during a read operation, the cell has a stored 1, then a small positive voltage will develop between B and \bar{B} , with v_B higher than $v_{\bar{B}}$. The amplifier will then cause v_B to rise to V_{DD} and $v_{\bar{B}}$ to fall to 0 V. The I/O output is then directed to the chip I/O pin by the column decoder (not shown) and at the same time is used to rewrite 1 in the DRAM cell, thus performing the restore operation that is required because the DRAM cell must operate in contention.

Figure 11.25 also shows the precharge and equalization circuit. Operation of this circuit is somewhat straightforward: When Q_5 goes high (or in a read operation, all three transistors conduct),

While Q_3 and Q_4 precharge the \bar{A} and B lines to $V_{DD}/2$, transistor Q_1 helps speed up this process by equalizing the initial voltages on the two lines. This equalization is critical to the proper operation of the sense amplifier. Any voltage difference present between \bar{B} and B prior to commencement of the read operation can result in erroneous interpretation by the sense amplifier of its input signal. In Fig. 11.23, we show only one of the cells in this particular column, namely, the cell whose word line is activated. The cell can be either an SRAM or a DRAM cell. All other cells in that column will not be connected to the \bar{B} and B lines because their word lines will remain low.

Let us now consider the sequence of events during a read operation:

1. The precharge and equalization circuit is activated by raising the control signal q_1 . This will cause the \bar{B} and B lines to be at equal voltages, equal to $V_{DD}/2$. The clock q_3 then goes low, and the \bar{B} and B lines are left to float for a brief interval.
2. The word line q_{10} goes up, connecting the cell to the \bar{B} and B lines. A voltage then develops between \bar{B} and B , with v_B higher than $v_{\bar{B}}$ if the accessed cell is storing a 1, or $v_{\bar{B}}$ lower than v_B if the cell is storing a 0. To keep the cell design simple, and to facilitate operation at higher speeds, the readout signal, which the cell is required to provide between B and \bar{B} , is kept small (typically, 30–300 mV).
3. Once an adequate difference voltage signal has been developed between B and \bar{B} by the storage cell, the sense amplifier is turned on by connecting \bar{B} to ground and V_{DD} through Q_3 and Q_4 , activated by raising the sense-control signal q_4 . Because initially the input terminals of the inverters are at $V_{DD}/2$, the inverters will be operating in their linear region where the gain is high (Section 10.2). It follows that initially the latch will be operating at its unstable equilibrium point. Thus, depending on the signal between the input terminals, the latch will quickly move to one of its two stable equilibrium points (refer to the description of the latch operation in Section 11.1). This is achieved by the regenerative action, inherent in positive feedback. Figure 11.24 clearly illustrates this point by showing the waveforms of the signal on the bit line for both a read-1 and a read-0 operation. Observe that once activated, the sense amplifier causes the small initial difference, $\Delta V(1)$ or $\Delta V(0)$, provided by the cell, to grow exponentially to either V_{DD} (for a read-1 operation) or 0 (for a read-0 operation).

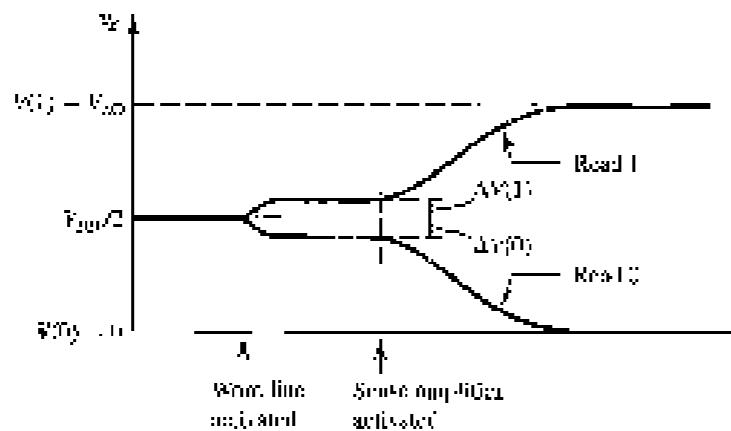


FIGURE 11.24 Waveforms of $v_B(t)$ shown for the selection of the sense amplifier. In a read-1 operation, the sense amplifier causes $v_B - V_{DD}/2$ (small initial $\Delta V(1)$) to grow exponentially to V_{DD} . In a read-0 operation, the negative $\Delta V(0)$ grows to 0. Complementary signal waveforms existing on the \bar{B} line.

The waveforms of the signal on the \bar{B} line will be complementary to those shown in Fig. 11.24 for the B line. In the following, we quantify the process of exponential growth of v_B and $v_{\bar{B}}$.

A Closer Look at the Operation of the Sense Amplifier. Developing a precise expression for the output signal of the sense amplifier shown in Fig. 11.23 is a rather complex task, requiring the use of large-signal (and thus nonlinear) models of the inverter voltage transfer characteristic, as well as taking the positive feedback into account. We will not do this here; rather, we shall consider the operation in a quantitative way.

Recall that at the time the sense amplifier is activated, each of its two inverters is operating in the transition region at $V_{DD}/2$. Thus, for small-signal operation, each inverter can be modeled using g_{in} and g_{out} , the transconductances of Q_3 and Q_4 , respectively, evaluated at an input bias of $V_{DD}/2$. Specifically, a small-signal v_B superimposed on $V_{DD}/2$ at the input of one of the inverters gives rise to an inverted output current signal of $(g_{out} + g_{in})v_B = G_{in}v_B$. This output current is delivered in one of the capacitors, C_2 or C_3 . The voltage thus developed across the capacitor is then fed back to the other inverter and is multiplied by its g_{out} , which gives rise to an output current feeding the other capacitor, and so on, in a regenerative process. The positive feedback in this loop will mean that the signal around the loop, and thus v_B and $v_{\bar{B}}$, will rise or decay exponentially (see Fig. 11.24) with a time constant of (C_2/C_3) (or (C_3/C_2)), since we have been assuming $C_2 = C_3$. Thus, for example, in a read-1 operation we obtain

$$v_B = \frac{V_{DD}}{2} + A V(1)e^{C_2/t_{RC}} \quad v_B \leq V_{DD} \quad (11.10)$$

whereas in a read-0 operation,

$$v_B = \frac{V_{DD}}{2} - A V(0)e^{-C_2/t_{RC}} \quad (11.11)$$

Because these expressions have been derived assuming small-signal operation, they describe the exponential growth (decay) of v_B reasonably accurately only for values close to $V_{DD}/2$. Nevertheless, they can be used to obtain a reasonable estimate of the time required to develop a particular signal level on the bit line.

Example 11.2

Consider the sense-amplifier circuit of Fig. 11.23 during the reading of a 1. Assume that the storage cell provides a voltage difference on the B line of $\Delta V(1) = 0.1\text{ V}$ if the NMOS devices in the inverters have $(W/L)_1 = 12\text{ }\mu\text{m}/4\text{ }\mu\text{m}$ and the PMOS devices have $(W/L)_2 = 20\text{ }\mu\text{m}/4\text{ }\mu\text{m}$, and assuming that the other parameters of the process technology are as specified in Example 11.2. Find the time required for v_B to reach 1.5 V. Assume $C_2 = 1\text{ pF}$.

Solution

First, we determine the transconductances g_{in} and g_{out} :

$$\begin{aligned} g_{in} &= n_p C_{in} \left(\frac{W}{L} \right) (V_{DD} - V_0) \\ &= 50 \times \frac{12}{4} (2.5 - 1) \\ &= 0.225 \text{ mA/V} \end{aligned}$$



$$v_{\text{in}} = k_1 C_s \left(\frac{V_{\text{DD}}}{L_{\text{in}}} (V_{\text{DD}} - V_{\text{t}}) \right)$$

$$\sim 20 \times \frac{2}{3}(2.5 - 1) = 0.225 \text{ mV}$$

Thus, the inverter G_1 is

$$G_1 = g_{\text{in}} + v_{\text{in}} = 0.15 \text{ mA/V}$$

and the time constant for the exponential growth of v_{S} will be

$$t = \frac{C}{G_1} = \frac{1.8 \cdot 10^{-12}}{0.15 \cdot 10^{-12}} = 2.22 \text{ ns}$$

Now, the time, t , for v_{S} to reach $\pm 5 \text{ V}$ can be determined from

$$t = 2.5 + 0.1e^{0.1777}$$

resulting in

$$t = 6.65 \text{ ns}$$

Obtaining Differential Operation in Dynamic RAMs. The sense amplifier described earlier responds to difference signals appearing between the bit lines. Thus, it is capable of rejecting interference signals that are common to both lines, such as those caused by capacitive coupling from the word lines. For this common-mode rejection to be effective, great care has to be taken to match both sides of the circuit tree, taking into account the circuit that feeds each side. This is an important consideration in any attempt to make the inherently single-ended nature of the DRAM cell appear differential. We shall now discuss an ingenious scheme for accomplishing this task. Although the technique has been around for many years (see the first edition of this book, published in 1982), it is still in use today. The method is illustrated in Fig. 11.25.

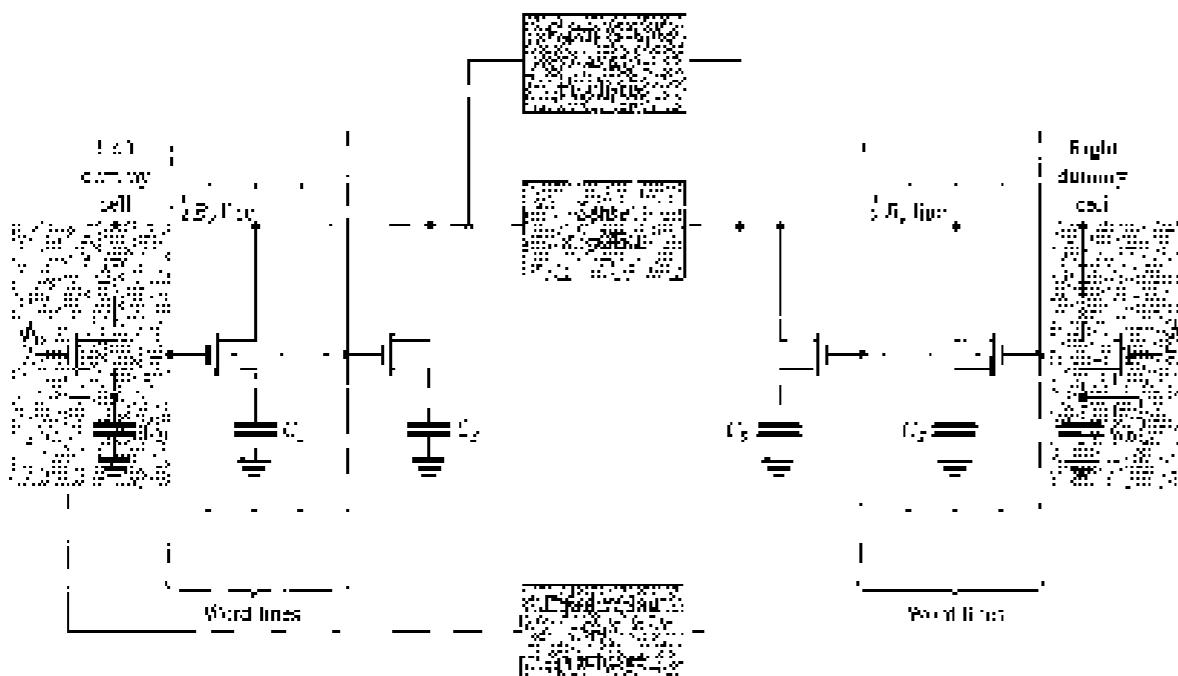


FIGURE 11.25 A cell segment of a dynamic DRAM chip, illustrating the single-ended DRAM cell. Note the dummy cells. (Xilinx, Inc.)

Basically, each bit line is split into two identical halves. Each half-line is connected to half the cells in the column and to an additional cell, known as a dummy cell, having a storage capacitor $C_d = C_s$. When a word line on the left side is selected for reading, the dummy cell on the right side (controlled by ϕ_2) is also selected, and vice versa; that is, when a word line on the right side is selected, the dummy cell on the left (controlled by ϕ_1) is also selected. In effect, then, the dummy cell serves as the other half of a differential DRAM cell. When the left-half bit line is in operation, the right-half bit line acts as its complement for \bar{d} line, and vice versa.

Operation of the circuit in Fig. 11.25 is as follows: The two halves of the line are precharged to $V_{\text{DD}}/2$ and their voltages are equalized. At the same time, the capacities of the two dummy cells are precharged to $V_{\text{DD}}/2$. Then a word line is selected, and the dummy cell on the other side is enabled (via ϕ_1 or ϕ_2) raised to V_{DD} . Thus the half-line connected to the selected cell will develop a voltage increment (around $V_{\text{DD}}/21$ or ΔV_1) or ΔV_0 depending on whether a 1 or a 0 is stored in the cell). Meanwhile, the other half of the line will have its voltage held equal to that of C_d (i.e., $V_{\text{DD}}/2$). The result is a differential signal of ΔV_1 or ΔV_0 that the sense amplifier detects and amplifies when it is enabled. As usual, by the end of the regenerative process, the amplifier will cause the voltage on one half of the line to become V_{DD} and that on the other half to become 0.

EXERCISES

11.12 If the required τ requires the times in Fig. 11.24, calculate the total time required for the memory to respond to an address, assuming the settling time of each inverter, τ_{sett} , is 10% of the τ of the inverter.

11.13 In the same memory as Example 11.3, the signal available from the cell outputs is W_1 and W_0 (bit lines), W_1 and \bar{W}_0 (bit lines), \bar{W}_1 and W_0 (bit lines), and \bar{W}_1 and \bar{W}_0 (bit lines). If A_1 is 1, A_2 is 0, and A_3 is 0, which of these four signals is the output?

11.14 If the address decoder of Fig. 11.13 is to be replaced by a 3-to-8 decoder, how many inputs does the decoder require? If the address decoder of Fig. 11.13 is to be replaced by a 4-to-16 decoder, how many inputs does the decoder require?

11.15 If the address decoder of Fig. 11.13 is to be replaced by a 3-to-8 decoder, how many inputs does the decoder require? If the address decoder of Fig. 11.13 is to be replaced by a 4-to-16 decoder, how many inputs does the decoder require?

11.5.2 The Row-Address Decoder

As described in Section 11.3, the row-address decoder is required to select one of the 2^M word lines in response to an M -bit address input. As an example, consider the case of $M = 3$ and denote the three address bits A_0 , A_1 , and A_2 , and the eight word lines W_0 , W_1 , ..., W_7 . Conventionally, word line W_0 will be high when $A_2 = 0$, $A_1 = 0$, and $A_0 = 0$; thus we can express W_0 as a logic function of A_0 , A_1 , and A_2 :

$$W_0 = \overline{A_2} \cdot \overline{A_1} \cdot \overline{A_0} = \overline{A_2} \cdot \overline{A_1} \cdot \overline{A_0}$$

Thus the selection of W_0 can be accomplished by a three-input NOR gate whose three inputs are connected to $\overline{A_2}$, $\overline{A_1}$, and $\overline{A_0}$, and whose output is connected to word line 0. Word line W_1 will be high when $A_2 = 1$, $A_1 = 0$, and $A_0 = 0$, thus

$$W_1 = A_2 \cdot \overline{A_1} \cdot \overline{A_0} = \overline{A_2} + \overline{A_1} + A_0$$

Thus the selection of W_1 can be realized by a three-input NOR gate whose three inputs are connected to $\overline{A_2}$, $\overline{A_1}$, and A_0 , and whose output is connected to word line 1. We can thus see that the address decoder can be realized by eight three-input NOR gates. Each NOR gate is

Indicate the appropriate combination of address bits and their complements, corresponding to the word line to which the patient is connected.

A simple approach to realising these NOR functions is provided by the static x-wire logic shown in Fig. 11.26. The circuit shown is a dynamic one (Section 10.6). Attached to each row line is a n-channel device that is activated, prior to the decoding process, by the pre-charge control signal ϕ_1 . During precharge (ϕ_1 low), all the word lines are pulled high to V_{DD} . It is assumed that at this time the address input b is low but yet been applied and all the inputs are low; notice there is no need for the circuit to include the evaluation transistor utilised in dynamic logic gates. Then, the decoding operation begins when the address bits

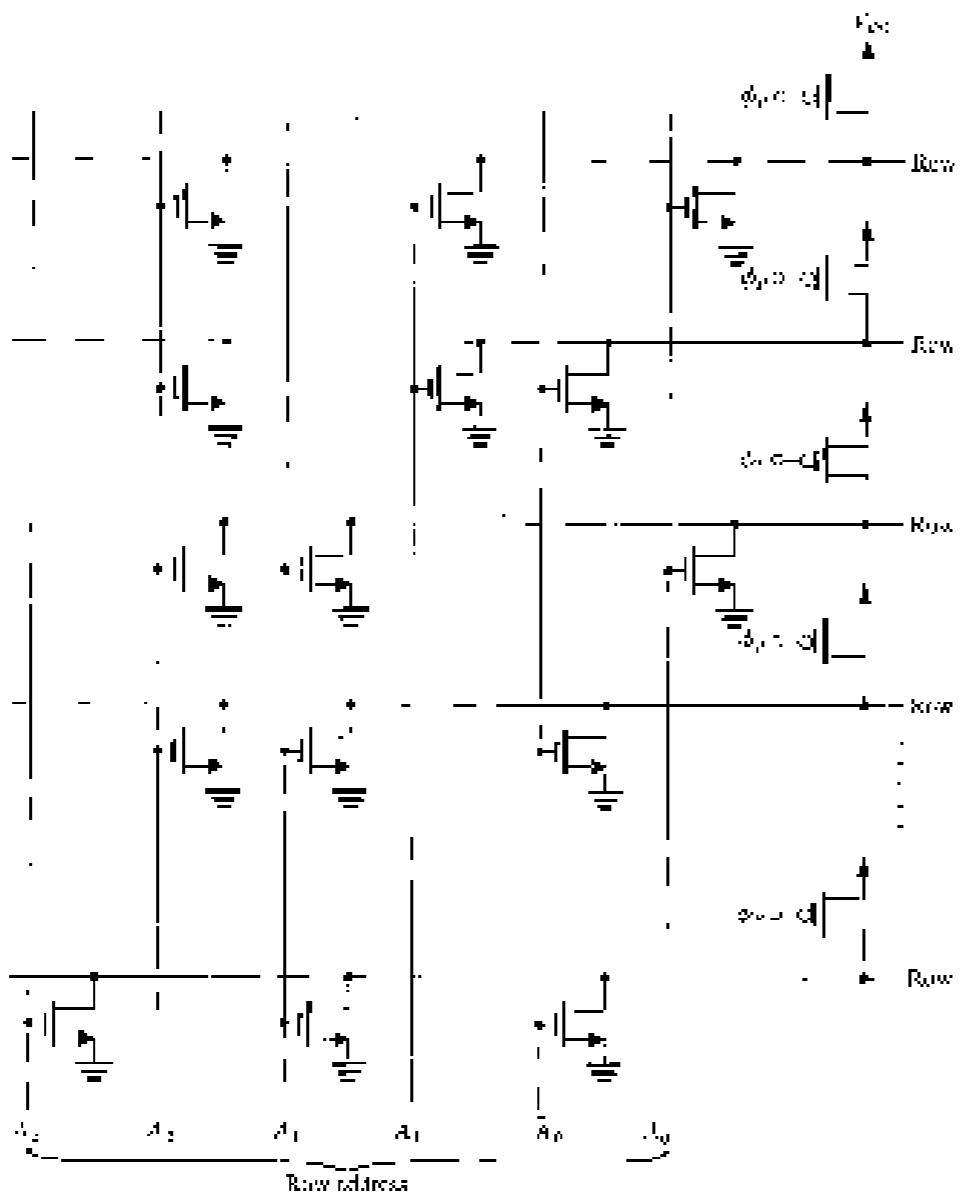


FIGURE 11.20 A MAC address learned by the switch. Channel 1's light blue box (*new Mac*) is a learned MAC address.

and their complements are applied. Observe that the NMOS transistors are placed so that the word lines not selected will be discharged. For any input combination, only one word line will not be discharged, and thus its voltage remains high at V_{DD} . For instance, row 0 will be high only when $A_2 = 0$, $A_1 = 0$, or $A_0 = 1$; this is the only combination that will result in all three transistors connected to row 0 being cut off. Similarly, row 3 has transistors connected to \bar{A}_2 , \bar{A}_1 , and A_0 , and thus it will be high when $A_0 = 1$, $A_1 = 1$, $A_2 = 0$, and so on. After the decoder output s_i has been latched, the output line s_i is connected to the word lines of the array, thereby via clock-controlled transmission gates. This decoder is known as a NOR decoder. Observe that, since the precharge is open, i.e., the decoder output does not dissipate static power,

REVIEW

- 11.14 Wie many new students are forecasted for NYS in October will attend schools?
Ans. 302,790 students

11.5.3 The Column-Address Decoder

From the description in Section 11.3, the function of the column address decoder is to connect one of the 2^8 bit lines to the data I/O line of the chip. As such, it is a multiplexer and can be implemented using transmission logic (Section 10.5) as shown in Fig. 11.27. Here, each bit line is connected to the data I/O line through an NMOS transistor. The gates of the pass transistors are controlled by 2^3 lines, one of which is selected by a NOR decoder similar to that used for decoding the row address.

An other major implementation of the column decoder that uses a smaller number of transistors (but at the expense of slower speed of operation) is shown in Fig. 11.2b. This circuit, known as a tree decoder, has a static structure of pass transistors. Unfortunately, since a relatively large number of transistors can exist in the signal path, the resistance of the bit line increases and the speed decreases correspondingly.

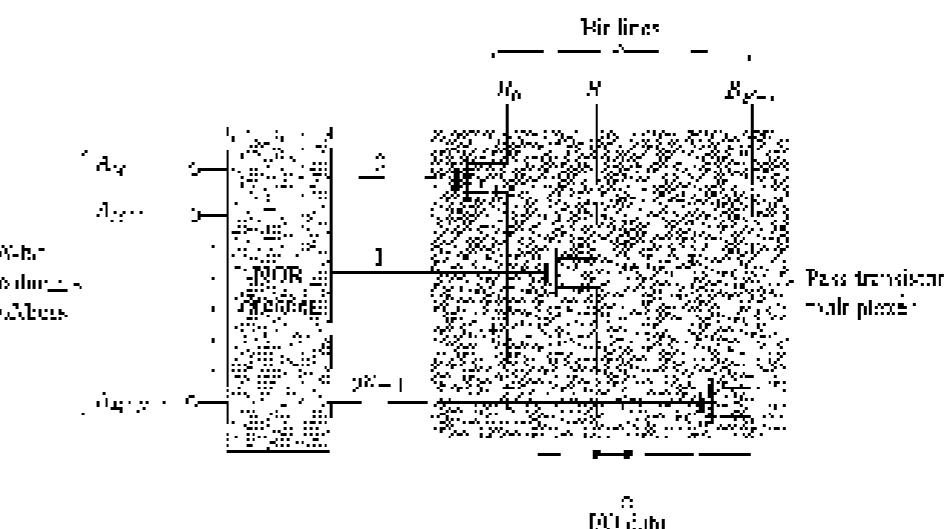


FIGURE 11.27 A column decoder realized by a combination of a NOR Decoder and a three-to-sixteen multiplexer.

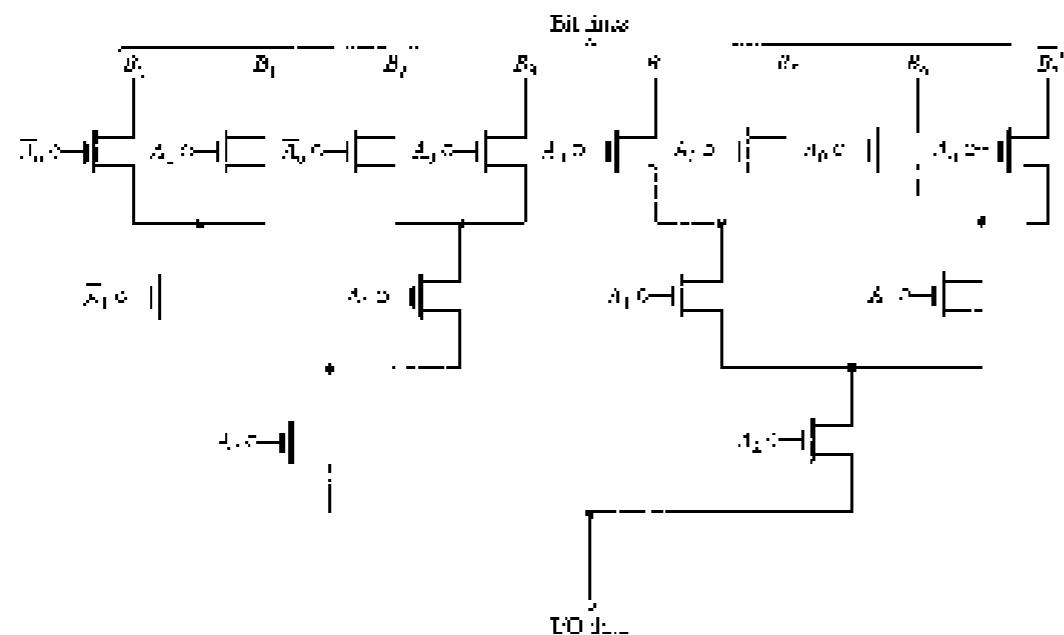


FIGURE 11.28 A tree search for dec�ar . Note that the colored pushdown boundary indicates that we are evaluating why $\delta = 1$, $A_1 = Q$ and $\lambda_1 = 1$, then it is clear that node 24 is immediately legal to the state δ .

EXERCISE

11.6 READ-ONLY MEMORY (ROM)

As mentioned in Section 1.1.3, read-only memory (ROM) is memory that contains fixed data patterns. It is used in a variety of digital-system applications. One of the most popular applications is the use of ROM in microcontroller systems to store the instructions of the system's basic operating program. ROM is particularly suited for such an application because it is nonvolatile; that is, it retains its contents when the power supply is switched off.

A ROM can be viewed as a combinational logic circuit for which the input is the collection of address bits of the ROM and the output is the set of data bits retrieved from the addressed location. This viewpoint leads to the application of ROMs in code conversion—that is, in changing the code of the signal from one system (say, binary) to another. Code conversion is employed, for instance, in secure communication systems, where the process is known as scrambling. It consists of feeding the code of the data to be transmitted to a ROM that provides corresponding bits in a (supposedly) secret code. The reverse process, which also uses a ROM, is applied at the receiving end.

In this section we will study various types of read-only memory. These include fixed ROM, which we refer to simply as ROM, programmable ROM (PROM), and erasable programmable ROM (EPROM).

11.6.1 A MOS ROM

Figure 11.29 shows a simplified 32-bit (or 8-word \times 4-bit) MOS ROM. As indicated, the memory consists of an array of n -channel MOSFETs whose gates are connected to the word lines, whose sources are grounded, and whose drains are connected to the bit lines. Each bit line is connected to the power-supply via a PMOS load transistor, in the manner of pseudo-NMOS logic (Section 10.4). An NMOS transistor exists in a particular cell if the cell is storing a 0; a cell storing a 1 has no MOSFET. This ROM can be thought of as 8 words of 4 bits each. The row decoder selects one of the 8 words by raising the voltage of the corresponding word line. The cell transistors connected to this word line will then conduct. By pulling the voltage of the bit lines on which transistors in the selected row are connected down from V_{DD} to a voltage close to ground voltage (the logic-0 level), the bit lines that are connected to cells (of the selected word) without transistors (i.e., the cells that are storing 1) will remain at the power-supply voltage (logic 1) because of the action of the pull-up PMOS load devices. In this way, the bits of the addressed word can be read.

A disadvantage of the 2OM circuit in Fig. 1.129 is that it dissipates static power. Specifically, when a word is selected, the transistors in this particular row will conduct static current that is supplied by the PMOS load transistors. Static power dissipation can be eliminated by a simple change. Rather than connecting the gate terminals of the PMOS transistors, we can connect these transistors to a precharge line ϕ_{PR} that is normally high. Just before a reading operation, ϕ is lowered and the bit lines are precharged to V_{DD} through the PMOS transistors. The precharge signal ϕ_{PR} then goes high and the word line is selected. The bit lines that have transistors in the selected word are then discharged, thus indicating stored zeros; whereas those lines for which no transistor is present remain at V_{DD} , indicating stored ones.

BYEBEIS

10. The purpose of the following questions is to help you evaluate the importance of the MMT framework for the U.S. fiscal system. In particular, focus on how MMT distinguishes the U.S. fiscal system from other countries' fiscal systems. In addition, focus on how MMT distinguishes the U.S. fiscal system from the fiscal systems of countries that do not have a central bank that is independent of the government.

11. During the period 1985-1995, the U.S. inflation rate averaged 3.0%. The U.S. inflation rate was at its lowest point during the 1980s. It was at its highest point during the 1990s. The U.S. inflation rate is 3.0%. Does this indicate a positive or negative inflation?

12. At the end of the previous lecture, find the value of π_{t+1} . For the first consideration, the inflation rate is 3.0% and the real interest rate is 6.0%. Calculate the real interest rate if the nominal interest rate is 9.0%. What is the percentage of each of the parameters in π_{t+1} ? Is there a difference between the contribution of each parameter? If there is a difference, which one of the parameters is more sensitive to changes in the value of π_{t+1} ?

13. When you look at the experimental results, what do you think the main finding is? Is it that inflation is a response to the output gap, or is it that inflation is a response to the interest rate? In other words, does the model support the Fisher hypothesis or the quantity theory of money?

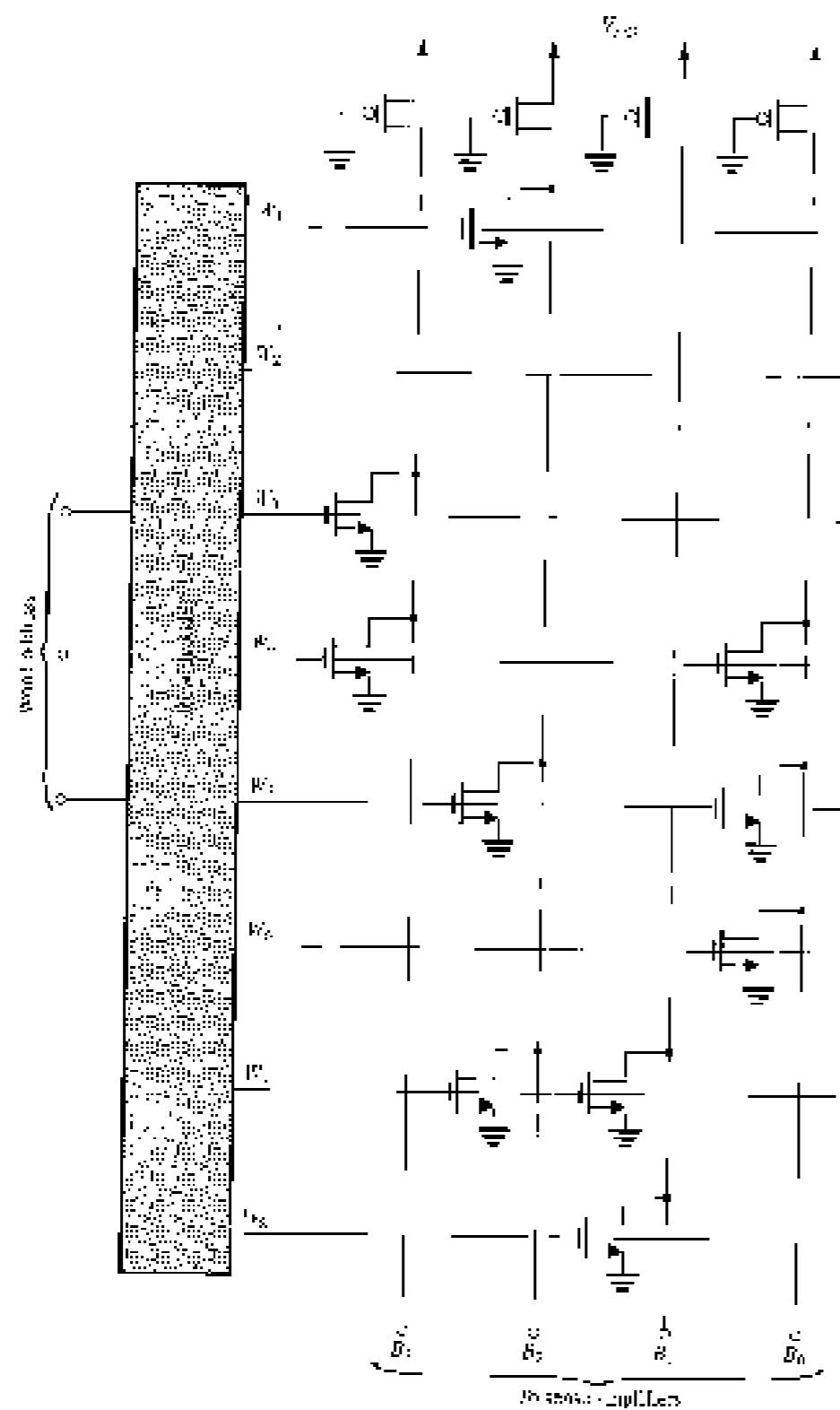


FIGURE 11.29 A CIRCUIT DIAGRAM OF THE INTERNAL ORGANIZATION OF A ROM CHIP.

11.6.2 Mask-Programmable ROMs

The data stored in the ROMs discussed thus far is determined at the time of fabrication, according to the user's specifications. However, to avoid having to custom design each ROM from scratch (which would be extremely costly), ROMs are manufactured using a process known as mask programming. As explained in Appendix A, integrated circuits are fabricated on a wafer of silicon using a sequence of processing steps that include photomasking, etching, and diffusion. In this way, a pattern of junctions and interconnections is created on the surface of the wafer. One of the final steps in the fabrication process consists of coating the surface of the wafer with a layer of aluminum, then selectively fusing a mask; etching away portions of the aluminum, leaving aluminum only where interconnections are desired. This last step can be used to program (i.e., to store a desired pattern) in a ROM. For instance, if the ROM is made of MOS transistors as in Fig. 11.28, MOSFETs can be included at all bit locations, but only the gates of those transistors where 1s are to be stored are connected. In the word lines, the gates of transistors where 0s are to be stored are not connected. This pattern is determined by the mask, which is produced according to the user's specifications.

The economic advantages of the mask programming process should be obvious: All ROMs are fabricated similarly; customization occurs only during one of the final steps in fabrication.

11.6.3 Programmable ROMs (PROMs and EEPROMs)

PROMs are ROMs that can be programmed by the user, but only once. A typical arrangement employed in 1-BIT PROMs involves using polysilicon lines to connect the emitter of each BJT to the corresponding digit line. Depending on the desired content of a ROM cell, the fuse can be either blown or blown out using a larger current. The programming process is obviously irreversible.

An erasable programmable ROM, or EEPROM, is a ROM that can be erased and reprogrammed as many times as the user wishes. It is therefore the most versatile type of read-only memory. It should be noted, however, that the process of erasure and reprogramming is time consuming and is intended to be performed only infrequently.

State-of-the-art EEPROMs use variations of the memory cell whose cross section is shown in Fig. 11.30(a). The cell is basically an enhancement-type n-channel MOSFET with two

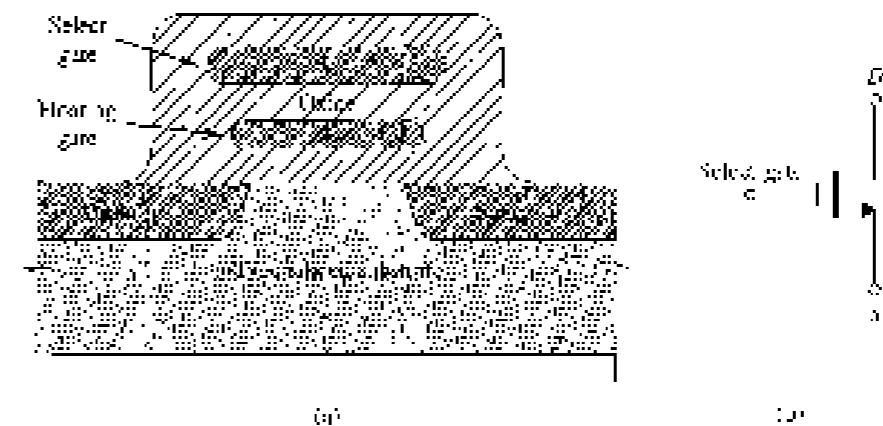


FIGURE 11.30 (a) CROSS SECTION AND (b) CIRCUIT SYMBOL OF THE FLOATING-GATE TRANSISTOR USED AS AN EEPROM CELL.

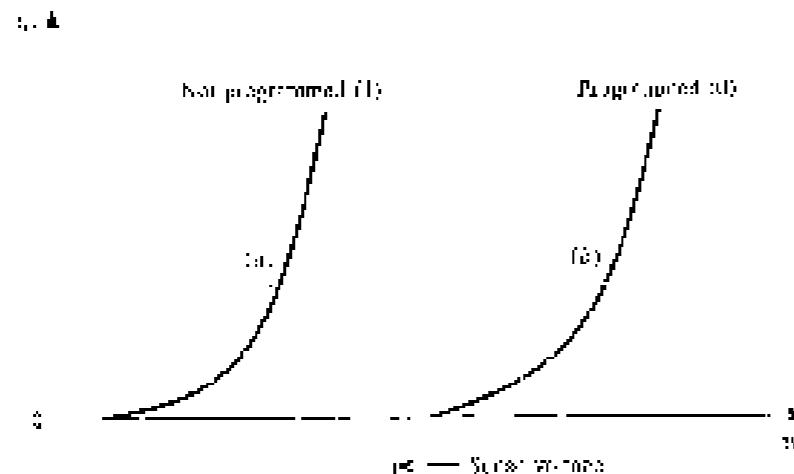


FIGURE 11.31 Illustrating the shift in the I_{DS} - V_{DS} characteristic of a floating-gate transistor as a result of programming.

gates made of polysilicon material.⁵ One of the gates is not electrically connected to any other part of the circuit; rather, it is left floating and is appropriately called a floating gate. The other gate, called a select gate, functions in the same manner as the gate of a regular enhancement MOSFET.

The MOS transistor of Fig. 11.30(a) is known as a floating-gate transistor and is given the circuit symbol shown in Fig. 11.30(b). In this symbol the broken line denotes the floating gate. The memory cell is known as the stacked-gate cell.

Let us now examine the operation of the floating-gate transistor. Before the cell is programmed (we will shortly explain what this means), no charge exists on the floating gate and the device operates as a regular n -channel enhancement MOSFET. It has exhibits the I_{DS} - V_{DS} characteristic shown as curve (a) in Fig. 11.31. Note that in this case the threshold voltage (V_{th}) is rather low. This state of the transistor is known as the not-programmed state. It is one of two states in which the floating-gate transistor can exist. Let us artificially take the not-programmed state to represent a stored 0. That is, a floating-gate transistor whose I_{DS} - V_{DS} characteristic is that shown as curve (a) in Fig. 11.31 will be said to be storing a 0.

To program the floating-gate transistor, a large voltage (16–20 V) is applied between its drain and source. Simultaneously, a large voltage (about 25 V) is applied to its select gate. Figure 11.32 shows the floating-gate MOSFET during programming. In the absence of any charge on the floating gate the device behaves as a regular n -channel enhancement MOSFET. An n -type inversion layer (channel) is created at the surface as a result of the large positive voltage applied to the select gate. Because of the large positive voltage at the drain, the channel has a tapered shape.

The drain-to-source voltage accelerates electrons through the channel. As these electrons reach the drain end of the channel, they acquire large kinetic energy and are referred to as hot electrons. The large positive voltage on the select gate (greater than the drain voltage) establishes an electric field in the insulating oxide. This electric field attracts the hot electrons

⁵ See Appendix A for a discussion of salicidation technology.

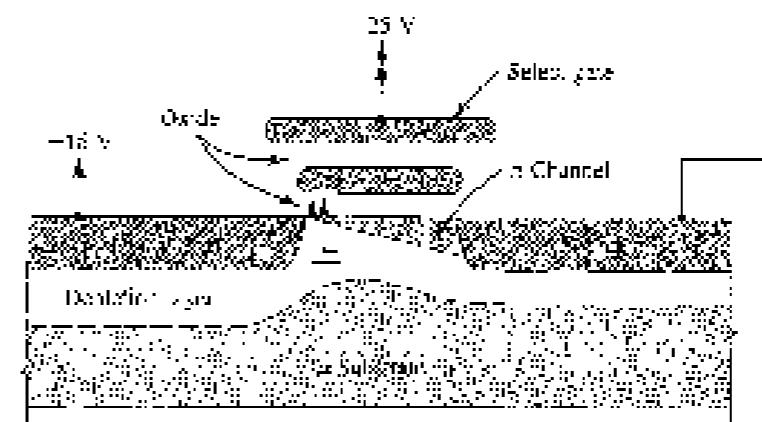


FIGURE 11.32 The floating gate inversion during programming.

and accelerates them through the oxide toward the floating gate. In this way, the floating gate is charged, and the charge that accumulates on it becomes trapped.

Properly, the process of charging the floating gate is called floating. The negative charge that accumulates on the floating gate reduces the strength of the electric field in the oxide to the point that it eventually becomes incapable of accelerating any more of the hot electrons.

Let us now inquire about the effect of the floating gate's negative charge on the operation of the transistor. The negative charge trapped on the floating gate will cause electrons to be repelled from the surface of the substrate. This implies that to form a channel, the positive voltage that has to be applied to the source side will have to be greater than that required when the floating gate is not charged. In other words, the threshold voltage (V_{th}) of the programmed transistor will be higher than that of the not-programmed device. In fact, programming causes the I_{DS} - V_{DS} characteristic to shift to the curve labeled (b) in Fig. 11.31. In this state, known as the programmed state, the cell is said to be storing a 1.

Once programmed, the floating-gate device remains in a charged state (curve b) even when the power supply is turned off. In fact, experimental results indicate that the level can remain in the programmed state for as long as 100 years!

Reading the current of the stacked-gate cell is easy. A voltage V_{DS} somewhere between the low and high threshold values (see Fig. 11.31) is applied to the selected gate. While a programmed device (one that is storing a 1) will conduct, a not-programmed device (one that is storing a 0) will conduct hardly.

To return the floating-gate MOSFET to its not-programmed state, the charge stored on the floating gate has to be returned to the substrate. This erasure process can be accomplished by illuminating the cell with ultraviolet light of the correct wavelength (255 nm) for a specified duration. The ultraviolet light imparts sufficient photon energy to the trapped electrons to allow them to overcome the inherent energy barrier, and thus be transported through the oxide back to the substrate. To allow this erasure process, the EPROM package contains a quartz window. Finally, it should be noted that the device is extremely durable and can be erased and programmed many times.

A more versatile programmable ROM is the electrically erasable PROM (or EEPROM). As the name implies, an EEPROM can be erased and reprogrammed electrically without the need for ultraviolet illumination. EEPROMs utilize a variant of the floating-gate MOSFET. An important class of EEPROMs using a floating-gate variant and long-emitting ESRAM are referred to as Flash memories.

11.7 Emitter-Coupled Logic (ECL)

Boltzmann-coupled logic (BCI) is the fastest logic circuit family.⁷ High speed is achieved by operating all transistors out of saturation, thus avoiding storage time delays, and by keeping the logic signal swings relatively small (about 0.5 V or less), thus reducing the time required to charge and discharge the various load and material capacitances. Synchronization in BCI is avoided by using the BIT differential pair as a current switch.⁸ The BIT differential pair was studied in Chapter 7, and we urge the reader to review the introduction given in Section 7.3 before proceeding with the study of BCI.

11.7.1 The Basic Principle

Exhibit-coupled logic is based on the use of the current-steering switch introduced in Section 1.1. Such a switch can be most conveniently realized using the differential pair shown in Fig. 1.1.34. The pair is biased with a constant current source I_0 , and one side is connected to a reference voltage V_{RR} . As shown in Section 7.3, the current I can be steered to either Ω_1 or Ω_2 under the control of the input signal v_i . Specifically, when v_i is greater than V_A by about $4V_T$ ($\approx 16.7\text{ mV}$), nearly all the current I is conducted by Ω_1 , and this for $v_i \geq V_A + V_{RR} - M_V$. Strikingly, the current through Ω_2 will be nearly zero, and thus $v_{o2} = V_{RR}$. Conversely, when v_i is lower than V_A by about $4V_T$, most of the current I will flow through Ω_2 , and the current through Ω_1 will be nearly zero. Thus $v_{o1} = V_{RR}$ and $v_{o2} = V_{RR} - M_V$.

The preceding assertion suggests that as a logic element , the differential pair requires an inversion function at v_1 , and simultaneously provides the complementary output signal at v_2 . The output logic levels are $V_{out} = V_{ex}$ and $V_{out} = V_{ex} - |V_{ex}|$, $|V_{ex}|$, and thus the output logic

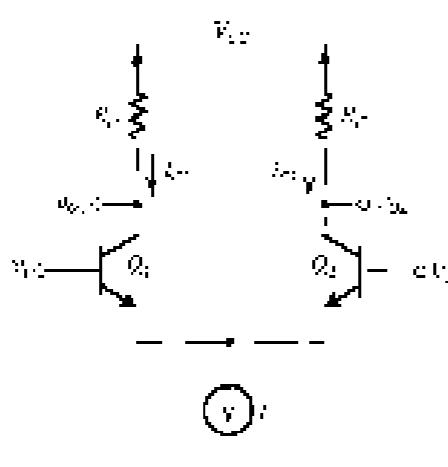


FIGURE 11.88 The basic element of DCC is the differential pair, where V_{DD} is a reference voltage.

⁷ Although higher speeds of operation can be obtained with gallium arsenide (GaAs) circuits, the latter are not available as off-the-shelf components for conventional digital systems (ex. pn. GaAs digital circuits are not covered in this book). However, a substantial amount of literature on this subject can be found on the CD accompanying the book, at www.electronics-world.com.

*This is a sharp contrast to the technique of, and its accompanying variety of transient resistance, used by TTS to characterize Schottky TJs. There, a Schottky diode is placed across the CBJ junction to short circuit the reverse current and, owing to the low voltage drop of the Schottky diode, the CBJ from the bias voltage. (See Fig. 1)

existing is IR_2 . A number of additional contacts can be made connecting this circuitry.

- The differential nature of the circuit makes it less susceptible to picked-up noise. In particular, an interfering signal will tend to affect both sides of the differential pair similarly and this will not result in current switching. This is the common mode rejection property of the differential pair (see Section 7.3).
 - The current drawn from the power supply remains constant during switching. Thus, unlike CMOS logic, no supply current spikes occur in ECL, eliminating an important source of noise in digital circuits. This is due to the design, especially since ECL is usually designed to operate with small signal swing and has acceptably low noise margins.
 - The output signal levels are both referenced to V_{DD} and thus can be made particularly stable by operating the circuit with $V_{DD} = 0$; in other words, by utilising a negative power supply and connecting the V_{DD} line to ground. In this case, $V_{O1} = 0$ and $V_{O2} = -V_{DD}$.
 - Some means has to be provided to make the output signal levels compatible with those at the input so that one pair can drive another. As we shall see shortly, practical ECL gate circuits incorporate a level-shifting arrangement that serves to centre the output signal levels on the value of V_{DD} .
 - The inability of complementary outputs to provide sharp interface design will limit ECL's usefulness in interfacing with other logic families.

ANSWER

الآن، يُمكننا إثبات أن $\Delta \mu_{\text{ex}} = -0.38 \pm 0.05$ دلارات، حيث تم الحصول على النتيجة من خلال التكامل بين النتائج المنشورة في المنشورات السابقة.

11.72 ECL Families

Currently there are two popular forms of commercially available GaN - namely, P-GaN and n-GaN. The n-GaN series features gate delays of the order of 0.75 ns and dissipation about 40 mW/gate, for a delay-power product of 30 pJ. Although its power dissipation is relatively high, the n-GaN series provides the shortest available gate delay.

The ECL-10K series is slightly slower; it features a gate propagation delay of 2 ns and a power dissipation of 25 mW for a delay-power product of 50 pJ. Although the value of DP is higher than that obtained in the 100K series, the 10K series is easier to use. This is because the rise and fall times of the pulse signals are deliberately made longer, thus reducing signal coupling or crosstalk between adjacent signal lines. ECL-10K has an "edge speed" of about 6.5 ns, compared with the approximately 1 ns of ECL-100K. To give consistency to our study of ECL, in the following we shall consider the regular ECL-10K in some detail. The same techniques, however, can be applied to other types of ECL.

In addition to its usage in small- and medium-scale integrated-circuit packages, PCL is also employed in large-scale and VLSI applications. A variant of PCL known as current-mode logic (CML) is well-known in VLSI applications (see Tondlak et al., 1981) and Wilson et al., 1990).

11.7.3 The Basic Gate Circuits

The basic gate circuit of the ECL 10K family is shown in Fig. 11-7a. The circuit consists of three parts. The network Δ consists of C_1 , D_1 , D_2 , X_1 , R_1 , and R_2 , centered at a reference voltage

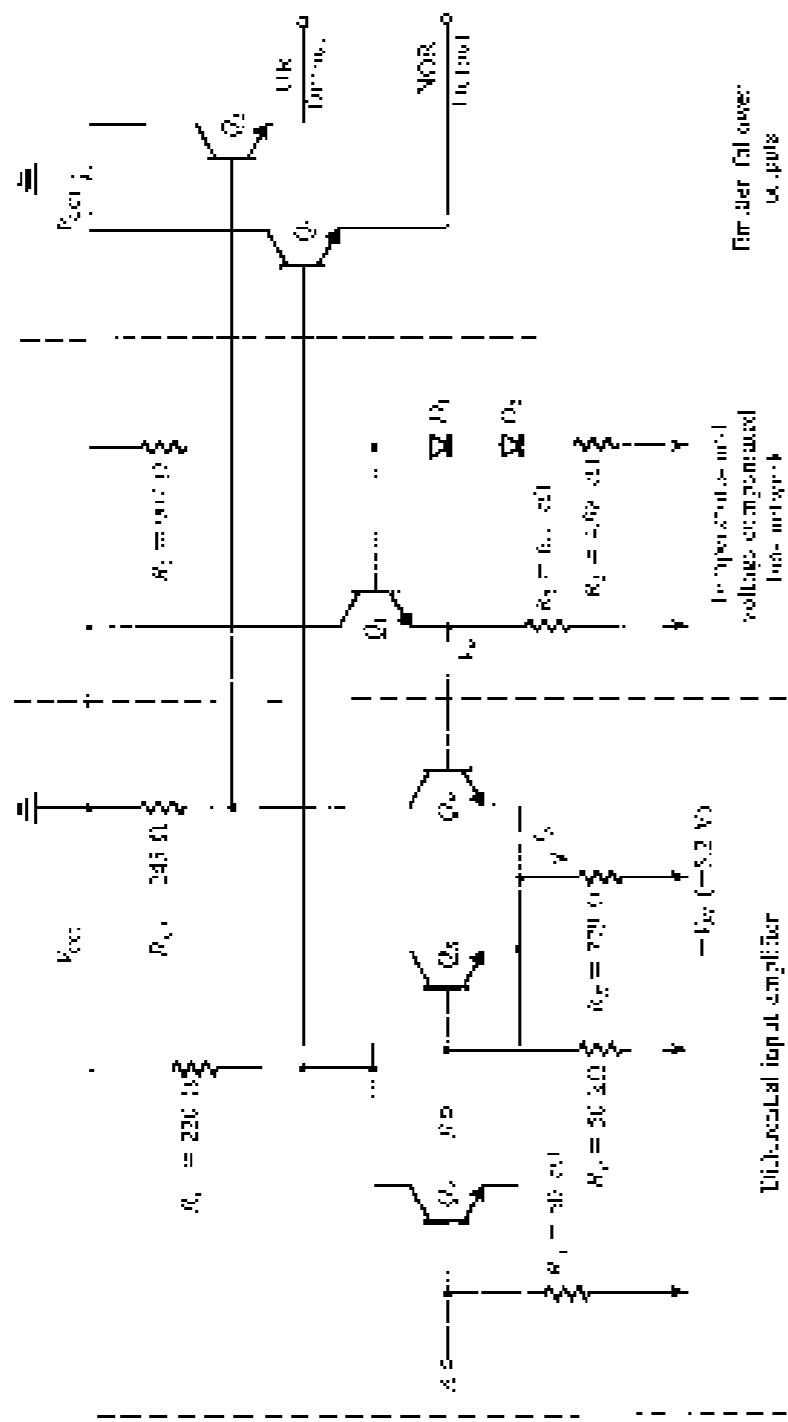


FIGURE 11.34 Basic circuit of the ECL NOR gate family.

V_r , whose value at room temperature is -1.32 V. As will be shown, the value of this reference voltage is made to change with temperature at a predetermined manner to keep the noise margin almost constant. Also, the reference voltage V_r is made relatively insensitive to variations in the power-supply voltage V_{cc} .

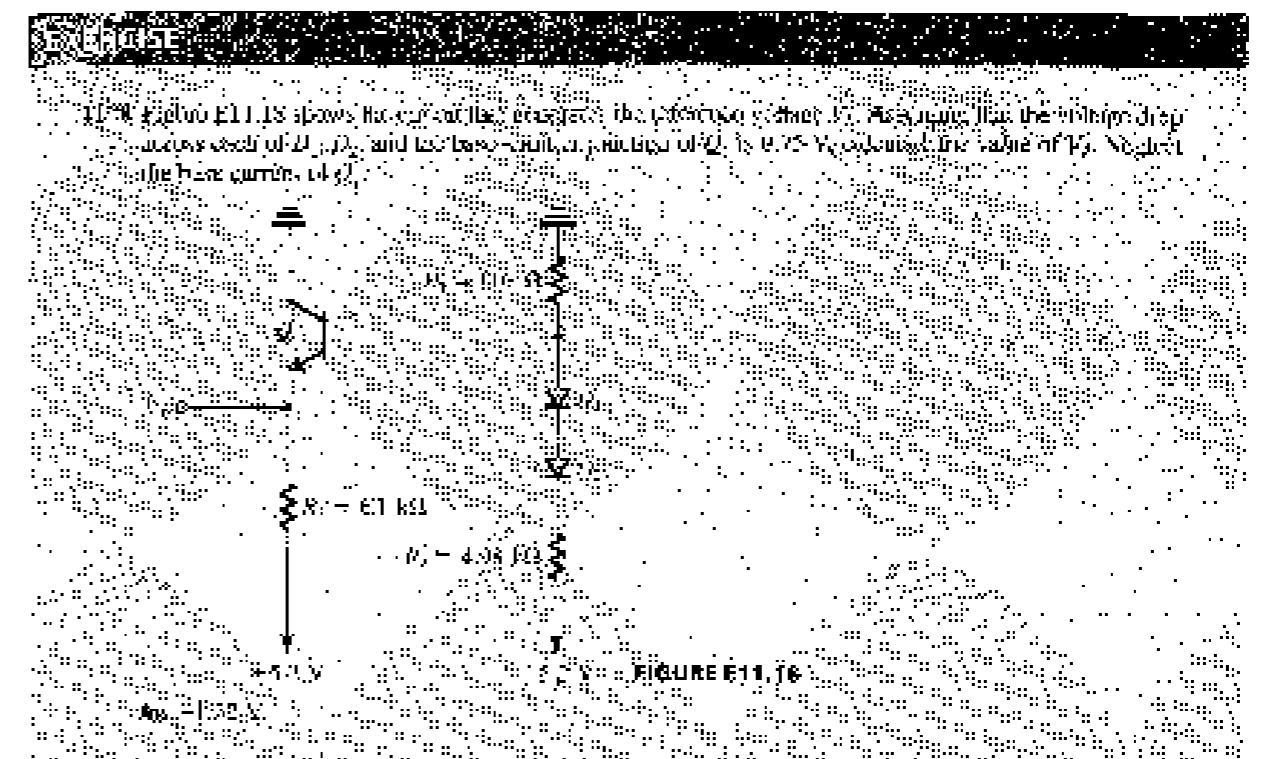


FIGURE 11.18

The second part, and the heart of the gate, is the differential amplifier formed by Q_3 and either Q_4 or Q_6 . This differential amplifier is biased out by a constant-current source, as was done in the circuit of Fig. 11.33, but with a resistor R_3 connected to the negative supply $-V_{ee}$. Nevertheless, we will shortly show that the current in R_3 remains approximately constant over the normal range of operation of the gate. One side of the differential amplifier consists of the reference transistor Q_r , whose base is connected to the reference voltage V_r . The other side consists of a number of transistors (two in the case shown), connected in parallel, with separated bases, each connected to a gate input. If the voltages applied to A and B are at the logic-0 level, which, as we will soon find out, is about 0.4 V below V_r , both Q_3 and Q_6 will be off and the current in R_3 will flow through the reference transistor Q_r . The resulting voltage drop across R_3 will cause the collector voltage of Q_3 to go low.

On the other hand, when the voltage applied to A or B is at the logic-1 level, which, as we will show shortly, is about 0.1 V above V_r , transistor Q_3 or Q_6 or both, will be on and Q_2 will be off. Thus the current I_3 will flow through Q_3 or Q_6 or both, and an almost equal current flows through R_3 . The resulting voltage drop across R_3 will cause the collector voltage to drop. Meanwhile, since Q_3 is off, its collector voltage rises. We thus see that the voltage at the collector of Q_3 will be high if A or B, or both, is high, and thus at the collector of Q_5 the NOR logic function $A \cdot B$ is realized. On the other hand, the common collector of Q_3 and Q_6 will be high only when A and B are simultaneously low. Thus, at the outputs

collector nodes Q_1 and Q_2 , the logic function $\overline{AB} = \overline{A} + \overline{B}$ is realized. We therefore conclude that the two-input gate of Fig. 11.34 realizes the OR function and its complement, the NOR function. The availability of complementary outputs is an important advantage of BCL; it simplifies logic design and avoids the use of additional inverters with associated time delay.

It should be noted that the resistance connecting each of the gate input terminals to the negative supply enables the user to leave an unused input terminal open. An open input terminal will be pulled down to the negative supply voltage, and its associated transistor will be off.

Exercise



The third part of the BCL gate circuit is composed of the two emitter followers, Q_1 and Q_2 . The source followers do not have on-chip loads; since in many applications of high-speed logic circuits the gate output drives a transmission line terminated at the other end, as indicated in Fig. 11.35, (More on this later in Section 11.7.6.)

The emitter followers have two purposes: first, they shift the level of the output signals by one V_{BE} drop. Thus, using the results of Exercise 11.13, we see that the output levels become approximately -1.75 V and -0.75 V. These shifted levels are centered approximately around the reference voltage ($V_T = 1.22$ V), which means that one pole can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

The second function of the output emitter followers is to provide the gate with low output resistances and with the large output currents required for charging load capacitances. Since these large transition currents can cause spikes on the power-supply line, the collectors of the emitter followers are connected to a power-supply terminal V_{CC} separate from that of the differential amplifier and the reference voltage circuit, V_{REF} . Here we note that the supply current of the differential amplifier and the reference circuit remains almost constant. The use of separate power-supply terminals prevents the coupling of power-supply spikes from the output circuit to the gate circuit and thus reduces the likelihood of false gate switching. Both V_{CC} and V_{REF} are of course connected to the same system ground, external to the chip.

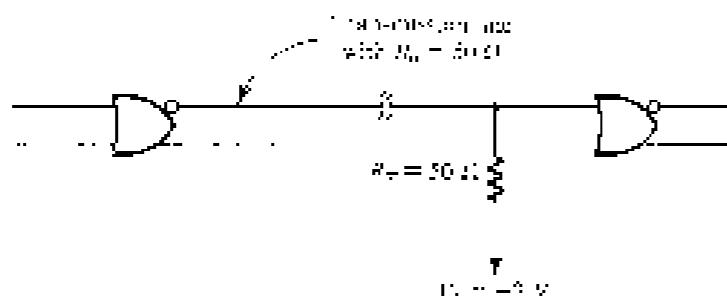


FIGURE 11.36 Simplified schematic of the BCL gate for the purpose of finding transfer characteristics.

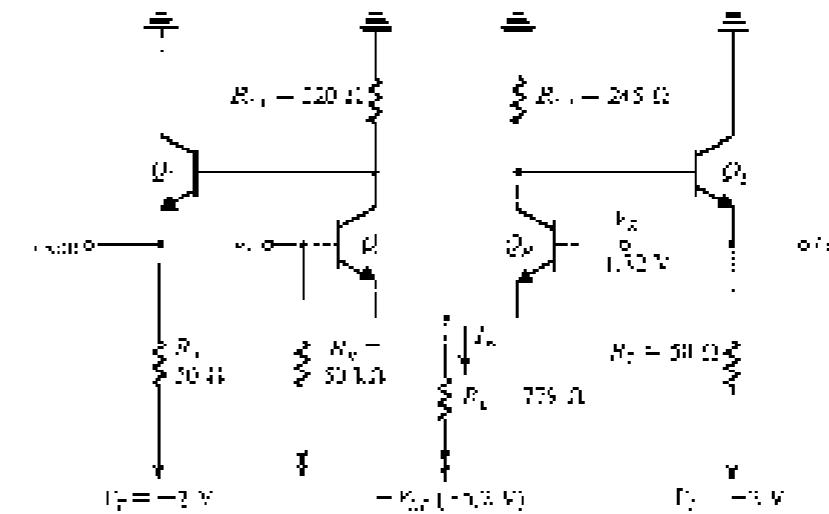


FIGURE 11.37 Simplified analysis of the BCL gate for the purpose of finding transfer characteristics.

11.7.4 Voltage Transfer Characteristics

Having provided a qualitative description of the operation of the BCL gate, we shall now derive its voltage transfer characteristics. This will be done under the conditions that the outputs are terminated in the manner indicated in Fig. 11.35. Assuming that the B input is low and that Q_2 is off, the circuit simplifies to that shown in Fig. 11.36. We wish to analyze this circuit to determine V_{BE} versus v_B and V_{BE} versus v_T (where $v_T = v_B$).

In the analysis to follow we will make use of the exponential $i_v - v_v$ characteristic of the BJT. Since the BJTs used in BCL circuits have on all areas in order to have small capacitances and hence high f_T , their scale factors k_v are small. We will therefore assume that at an operating current of 1 mA an ECL transistor has a V_{BE} drop of 0.75 V.

The OR Transfer Curve. Figure 11.37 is a sketch of the OR transfer characteristic, V_{BE} versus v_B , with the parameters V_{CC} , V_{REF} , V_T , and R_C indicated. However, to simplify the correlation of V_{BE} and $V_{BE}|Q_1$ we shall use an alternative to the unity-gain definition. Specifically, we shall assume that at point x , transistor Q_1 is conducting 1% of I_C while Q_2 is conducting 99% of I_C . The reverse will be assumed for unity. Thus at point x we have

$$\frac{i_{C|Q_2}}{i_{C|Q_1}} = 99$$

Using the exponential $i_v - v_v$ relationship, we obtain

$$V_{BE}|Q_2 - V_{BE}|Q_1 = V_T \ln 99 = 1.15 \text{ mV}$$

which gives

$$V_{BE} = V_T + V_{BE}|Q_1 - 1.15 \text{ mV}$$

Assuming Q_1 and Q_2 to be matched, we can write

$$V_{BE} = V_T + V_{BE}|Q_1 - V_T$$

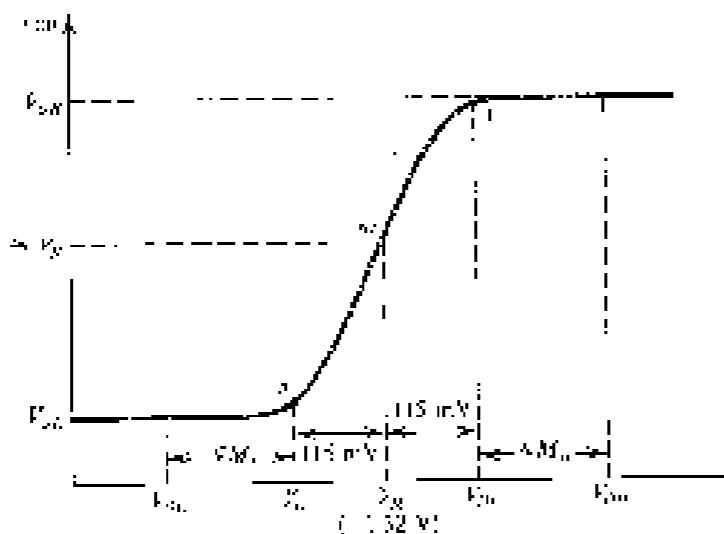


FIGURE 11.37 The OR transfer characteristic for the circuit in Fig. 11.36.

which can be used to find V_{in} , as

$$V_{in} = -1.205 \text{ V}$$

To obtain V_{in} , we note that Q_1 is off and Q_2 carries the entire current I_E , given by

$$\begin{aligned} I_E &= \frac{V_E - V_{BE}|_{Q_2} - V_{CE}}{R_L} \\ &= \frac{1.32 - 0.73 - 5.2}{0.774} \\ &\approx 4 \text{ mA} \end{aligned}$$

If we wish, we can iterate to determine a better estimate of $V_{BE|Q_2}$ and hence of I_E , assuming that Q_2 has a large β so that its $\alpha \approx 1$, its collector current will be approximately 4 mA. If we neglect the base current of Q_2 , we obtain for the collector voltage of Q_2

$$V_C|_{Q_2} \approx 4 \times 0.245 = 0.98 \text{ V}$$

Thus a first approximation for the value of the output voltage V_{out} is

$$\begin{aligned} V_{out} &= V_C|_{Q_2} + V_{BE|Q_2} \\ &\approx 0.98 + 0.73 = 1.71 \text{ V} \end{aligned}$$

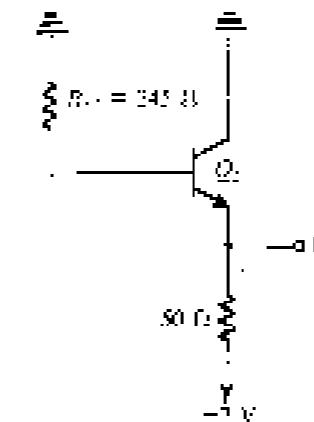
We can use this value to find the emitter current of Q_2 and then iterate to determine a better estimate of its base-emitter voltage. The result is $V_{BE|Q_2} \approx 0.79 \text{ V}$ and, correspondingly,

$$V_{out} \approx 1.77 \text{ V}$$

At this value of output voltage, Q_2 supplies a load current of about 4.6 mA.

To find the value of V_{out} we assume that Q_2 is completely cut off (because $v_i > V_{in}$). Thus the circuit for determining V_{out} simplifies to that in Fig. 11.38. Analysis of this circuit assuming $\beta_2 = 100$ results in $V_{out} \approx 0.83 \text{ V}$, $I_{C2} = 22.1 \mu\text{A}$, and

$$V_{out} \approx -0.86 \text{ V}$$

FIGURE 11.38 Circuit for determining V_{out} .

EXERCISE

- 11.20. In the circuit in Fig. 11.36, determine the values of the parameters required to obtain a noise margin $N.M. = 0.75$, 3.97 mV , 4.00 mA , 182 nA , -1.205 V .
 Hint: $V_{in1} = -1.32 \text{ V}$, $V_{in2} = -0.73 \text{ V}$, $V_{DD} = 5.2 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $R_{L1} = 343.2 \text{ k}\Omega$, $R_{L2} = 50 \Omega$, $\beta_1 = 100$, $\beta_2 = 100$, $I_{C1} = 22.1 \mu\text{A}$, $I_{C2} = 22.1 \mu\text{A}$, $V_{BE1} = 0.73 \text{ V}$, $V_{BE2} = 0.245 \text{ V}$, $V_{CE1} = 5.2 \text{ V}$, $V_{CE2} = 0.98 \text{ V}$, $V_{out1} = 1.71 \text{ V}$, $V_{out2} = -0.86 \text{ V}$.

Noise Margins The results of Exercise 11.20 indicate that the noise current I_E remains approximately constant. Also, the output voltage corresponding to $v_i = V_p$ is approximately equal to V_p . Notice further that this is also approximately the midpoint of the logic swing; specifically,

$$\frac{V_{in1} + V_{in2}}{2} = -1.325 \approx V_p$$

Thus the output logic levels are centered around the midpoint of the input transition range. This is an ideal situation from the point of view of noise margins, and it is one of the reasons for selecting the rather arbitrary-looking numbers ($V_{in1} = -1.32 \text{ V}$ and $V_{in2} = 5.2 \text{ V}$) for reference and supply voltages.

The noise margins can now be evaluated as follows:

$$\begin{aligned} NM_H &= V_{in1} - V_{in} \\ &= -0.38 - (-1.205) = 0.825 \text{ V} \end{aligned} \quad \begin{aligned} NM_L &= V_{in} - V_{in2} \\ &= -1.435 - 1.77 = -0.295 \text{ V} \end{aligned}$$

Note that these values are approximately equal.

The NOR Transfer Curve The NOR transfer characteristic, which is v_i versus v_o for the circuit in Fig. 11.36, is sketched in Fig. 11.39. The values of V_{in1} and V_{in2} are identical to those found earlier for the OR characteristic. To emphasize this we have labeled the threshold points x and y , the same letters used in Fig. 11.37.

For $v_i < V_{in1}$, Q_1 is off and the output voltage v_{out} can be found by analyzing the circuit composed of R_{L1} , Q_2 , and its 50-Ω transmission line, except that R_{L1} is slightly smaller than R_{L2} . This circuit is identical to that in Fig. 11.38. Thus the output voltage will be only slightly

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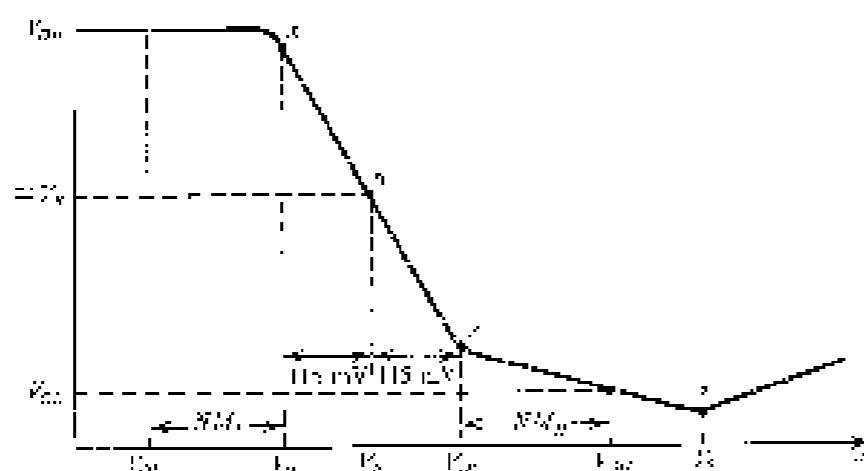


FIGURE 11.39 The NOR transfer characteristic, y_{NOR} , versus x_1 for a unit in Fig. 11.38.

greater than the value V_{off} (unpublished). In the sketch of Fig. 11-39 we have assumed that the output voltage is approximately equal to V_{off} .

For $v_2 > V_{DD}$, v_3 is on and is conducting the entire bias current. The circuit, then, simplifies to that in Fig. 11.16. This circuit can be easily analyzed to obtain v_{out} versus v_2 for the range $v_2 > V_{DD}$. A number of observations are in order. First, note that $v_2 = V_{DD}$ results in no output voltage slightly higher than V_{DD} . This is because $R_{21} \gg R_{31}$ than R_{31} . In fact, R_{21} is chosen lower in value than R_{31} so that with v_3 equal to the normal logic-1 value (i.e., V_{DD}), which is approximately +0.6 V, the output will be equal to the V_{DD} value found earlier for the OR output.

Second, note that as α exceeds β_{ad} , transistor Q_1 operates in the active mode and the circuit of Fig. 1.1.10 can be analyzed to find the gain of the amplifier, which is the slope of the segment xy of the transistor characteristic. At point x , transistor Q_1 enters lather operation; in x (beyond the point $x = V_{\text{ad}}$) the voltage v_{out} and hence A_{out} increase.

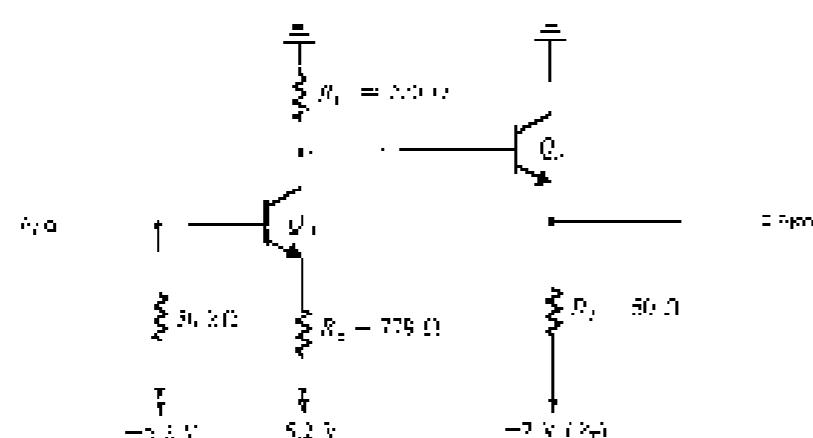


FIGURE 11.40 Circuit for finding μ_{fric} without a balance scale.

The slope of the segment of the transient characteristic beyond point c, however, is not unity but is about 0.5 because as Q_2 is driven deeper into saturation, a portion of the current in c_2 appears as no increase in the base-collector forward-bias voltage. The reader is urged to solve Exercise 11.21, which is concerned with the details of the NPN transistor characteristics.

EXERCISE

- (b) Find the value of θ when $V_{AB} = -0.2$ V. Assume that $V_{AB} = 0$ V at $\theta = 0^\circ$.

Answer: 127° (Ans) ($-0.2 \times 100 = -0.2$ V)

Manufacturers' Specifications (10) manufacturers supply gas transmission characteristics of the form shown in Figs. 11-37 and 11-38. A manufacturer usually provides such curves measured at a number of ten pressures. In addition, at each relevant pressure, specific values for the parameters V_{g} , V_{m} , V_{sc} , and V_{sh} are given. These corner-case values are associated with the invariable component tolerances taken into account. As an example, Manufacturers specify that for NPGCL 10,000 at 25°C the following corner-case values apply¹⁴:

$$V_{R,\text{max}} = -1.475 \text{ V} \quad V_{R,\text{min}} = -1.105 \text{ V}$$

These values can be used to detect the well-known noise patterns.

$$\delta E_{\text{H}} = 0.155 \text{ eV} \quad \delta M_{\text{H}} = 0.128 \text{ eV}$$

which are about half the size of the previous ones.

For additional information on MECL see Ritter's *The integrated reader* as referred to in the Mouloua, (1988, 1989) publications listed in the bibliography at the end of the book.

1175 Fan-Qi

When the input signal to an ECL gate is low, the input current is equal to the current that flows in the 50 kΩ pull-down resistor. Thus,

$$I_{\text{ch}} = \frac{1.77 + 5.2}{80} = 0.75 \mu A$$

When the object is large, the input current is greater because of the base current of the input transistor. Thus, assuming a resistance of 10 k Ω , we obtain

$$f_{cr} = \frac{-0.88 + 0.2}{\varepsilon_0} + \frac{4}{|V|} = 126 \text{ } \mu\text{s}$$

Both these current values are quite small, which, coupled with the very small output resistance of the FET gate, indicates that little degradation of logic-signal levels results from the input currents of fan-out gates. It follows that the fan-out of FET gates is not limited by

"MEL is the trade name used by Vicks for its 12

logic level considerations, but rather by the degradation of the circuit speed (rise and fall times). This latter effect is due to the circumstance that each fan-out gate presents to the driving gate capacitively 3 pF . Thus while the $\Delta V_{\text{fan-out}}$ can be as high as 50 mV , this does not represent a design problem, the $\Delta t_{\text{fan-out}}$ is limited by considerations of circuit speed to 10 ns or so.

11.7.6 Speed of Operation and Signal Transmission

The speed of operation of a logic family is measured by the delay of its basic gate and by the rise and fall times of the output wave forms. Typical values of these parameters for ECL have already been given. Here we should note that because the output circuit is not an emitter follower, the rise time of the output signal is shorter than its fall time, since on the rising edge of the output pulse the emitter follower functions and provides the output current required to charge up the load and parasitic capacitance. On the other hand, at the signal at the base of the driver is lower, i.e., the emitter follower is off, and the load capacitance discharges through the combination of load and pull-down resistances.

To take full advantage of the very high speed of operation possible with ECL, special attention should be paid to the method of interconnecting the various logic gates in a system. To appreciate this point, we shall briefly discuss the problem of signal transmission.

ECL deals with signals whose rise times may be 1 ns or even less, the time it takes the light to travel only 30 cm or so. For such signals a wire and its environment become a relatively compact circuit element along which signals propagate with finite speed (perhaps half the speed of light—i.e., 15 cm/ns). Unless special care is taken, energy that reaches the end of such a wire is not absorbed but rather reflects as a reflection to the transmitting end, where (without special care) it may be re-reflected. The result of this process of reflection is what can be observed as ringing, a damped oscillatory excursion of the signal about its final value.

Unfortunately, ECL is particularly sensitive to ringing because the signal levels are so small. Thus it is important that transmission of signals be well controlled, and supply energy dissipated, to prevent reflections. The accepted technique is to limit the nature of connecting wires in some way. One way is to make them be very short, where "short" is taken to mean with respect to the signal rise time. The reason for this is that if the wire connection is so short that reflections return while the input is still rising, the result becomes only a slow-browned "boring" rising edge.

If, however, the reflected voltage after the rising edge, it produces not simply a modification of the initiating edge but an independent second event. This is clearly bad! Thus the time taken for a signal to go from one end of a line and back is restricted to less than the rise time of the driving signal by some factor—say, 5 . This for a signal with a 1-ns rise time and propagation at the speed of light (30 cm/ns), a double path of only 0.2-cm equivalent length, $\approx 6 \text{ cm}$, would be allowed, representing in the limit a wire only 3 cm from end to end.

This is the restriction on ECL 100R; however, ECL 10K has an intentionally slower rise time of about 3.5 ns . Using the same rules, wires can accordingly be as long as about 16 cm for ECL 10K.

If greater lengths are needed, then transmission lines must be used. These are simply wires in a controlled environment in which the distance to a ground reference plane or second wire is tightly controlled. Thus they might simply be twisted pairs of wires, one of which is grounded, or parallel ribbon wires, every second of which is grounded, so-called microstrip lines on a printed-circuit board. The latter are simply copper strips of controlled geometry on one side of a thin printed-circuit board, the other side of which consists of a grounded plane.

Such transmission lines have a characteristic impedance, R_0 , that ranges from a few tens of ohms to hundreds of ohms. Signals propagate on such lines somewhat more slowly than the speed of light, perhaps half as fast. When a transmission line is terminated at its receiving end in a resistance equal to its characteristic impedance, R_0 , all the energy sent on the line is absorbed at the receiving end, and no reflections occur since the termination acts as a limitless length of transmission line. Thus, signal integrity is guaranteed. Such transmission lines are said to be *properly terminated*. A properly terminated line appears at its sending end as a resistance of value R_0 . The followers of ECL 10K with their numbers and low output resistances (specified to be 7.11 ohm) are ideally suited for driving transmission lines. ECL is also good as a line receiver. The sink gate with its high ($50\text{-k}\Omega$) pull-down input resistor represents a very high resistance to the line. Thus a few such gates can be connected to a terminated line with little difficulty. Both of these ideas are represented in Fig. 11-15.

11.7.7 Power Dissipation

Because of the differential-ampifier nature of ECL, the gate current remains approximately constant and is simply steered from one side of the gate to the other depending on the input logic signals. Thus, the supply current and hence the gate power dissipation of unterminated ECL can remain relatively constant, independent of the logic state of the gate. It follows that no voltage spikes are introduced on the supply line. Such spikes can be a dangerous source of noise in a digital system. It follows that in ECL, the need for supply line bypassing is not as great as in, say, TTL. This is another advantage of ECL.

At this juncture we should reiterate a point we made earlier, namely, that although an ECL gate would operate with $V_{\text{DD}} = 0$ and $V_{\text{CC}} = +5.2 \text{ V}$, the selection of $V_{\text{DD}} = -5.2 \text{ V}$ and $V_{\text{CC}} = 0 \text{ V}$ is recommended because in the circuit all signal levels are referenced to V_{DD} and ground is certainly an excellent reference.

EXERCISE

11.27 For the ECL gate of Fig. 11-14, calculate the minimum value of the $\Delta V_{\text{fan-out}}$ required to make the transition time fall within the maximum permissible time of 10 ns . Assume that the gate has a unity-gain corner frequency of 10 MHz and hence a 3-dB corner frequency of 3.2 ns .

11.7.8 Thermal Effects

In our analysis of the ECL gate of Fig. 11-14, we found that at zero temperature the reference voltage V_r is -1.52 V . We have also shown that the midpoint of the output logic swing is approximately equal to this voltage, which is an ideal situation in that it results in equal high and low noise margins. In Example 11-4, we shall derive expressions for the temperature coefficients of the reference voltage and of the output low and high voltages. In this way, it will be shown that the midpoint of the output logic swing varies with temperature at the same rate as the reference voltage. As a result, although the magnitudes of the high and low noise margins change with temperature, their values remain equal. This is an added advantage of ECL and provides a compensation of the high degree of design optimization of this gate circuit.



We wish to determine the temperature coefficient of the reference voltage V_R and of the voltage V_{BE} between V_{BE} and V_{DD} .

Solution

To determine the temperature coefficient of V_R , consider the circuit in Fig. 11.41. It may assume that the temperature changes by $+1^\circ\text{C}$. Denoting the temperature coefficient of the diode and transistor voltage drops by δ where $\delta = 2 \text{ mV/C}$, we obtain the equivalent circuit shown in Fig. 11.41. In the latter circuit the changes in device voltage drops are considered as unequal, and hence the power supply is shown as a zener diode.

In the circuit of Fig. 11.41 we have two signal generators, and we wish to analyze the circuit to determine ΔV_R , the change in V_R . We shall do so using the principle of superposition. Consider first the input R_1 , D_1 , D_2 , R_3 , and R_4 , and neglect the signal base current of Q_1 . The voltage swing at the base of Q_2 can be easily obtained from

$$\Delta v = \frac{2\delta \times R_1}{R_1 + r_{D_1} + r_{D_2} + R_3}$$

where r_{D_1} and r_{D_2} denote the incremental resistances of diodes D_1 and D_2 , respectively. The dc bias current through D_1 and D_2 is approximately 0.48 mA, and thus $r_{D_1} = r_{D_2} = 20.2 \text{ k}\Omega$. Hence $r_{D_1} = 0.18 \text{ k}\Omega$. Since the gain of the emitter follower Q_1 is approximately unity, it follows that the component of ΔV_R due to the generator Δv is approximately equal to Δv , that is, $\Delta V_{R1} = 0.3 \text{ mV}$.

Consider next the component of ΔV_R due to the generator δ . Recalculating into the emitter circuit of the result resistance of the base circuit, $R_1 [r_{D_1} + r_{D_2} + R_3]$, by dividing it by $\beta + 1$ (with $\beta = 100$) results in the following component of ΔV_R :

$$\Delta V_{R2} = -\frac{\delta \times R_1}{R_1 [r_{D_1} + r_{D_2} + R_3] (\beta + 1) + r_{D_1} + R_3}$$

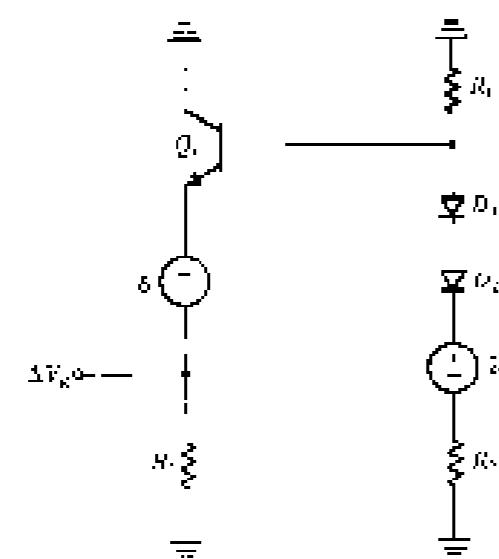


FIGURE 11.41 Equivalent circuit for determining the temperature coefficient of the reference voltage V_R .

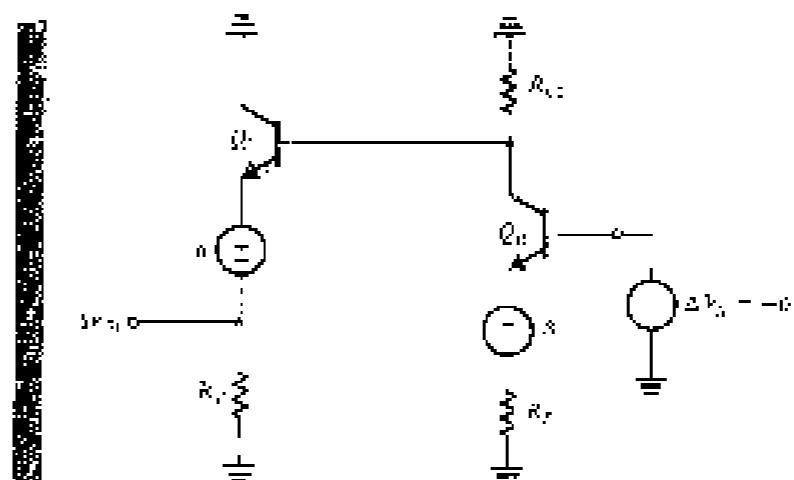


FIGURE 11.42 Emitter-coupled circuit for determining the temperature coefficient of V_{BE} .

where R_x denotes the load resistance in the base circuit, and r_{T_x} denotes the collector resistance of Q_x ($x = 1, 2$). This calculation yields $\Delta V_{R2} = -\delta$. Adding this value to the value in the generator δ gives $\Delta V_R = -0.74$. Thus for $\delta = 2 \text{ mV/C}$ the temperature coefficient of V_R is $-1.4 \text{ mV/}^\circ\text{C}$.

We next consider the determination of the temperature coefficient of V_{BE} . The circuit with which to perform this analysis is shown in Fig. 11.42. Here we have three parameters whose contributions can be calculated separately and the resulting components (ΔV_{B1}) summed. The result is

$$\begin{aligned} \Delta V_{B1} &= \Delta V_B \frac{R_{T1}}{r_{T1} + R_x} \frac{R_x}{R_x + r_{T2}} \\ &= \delta \frac{R_{T1}}{r_{T1} + R_x} \frac{R_x}{R_x + r_{T2}} \\ &= -\delta \frac{R_T}{R_x + r_{T1} + R_{T2}/(\beta + 1)} \end{aligned}$$

Substituting the values given and those obtained throughout the analysis of this section, we find

$$\Delta V_{B1} = -0.738$$

The circuit for determining the temperature coefficient of V_{BE} is shown in Fig. 11.7, from which we obtain

$$\Delta V_{BE} = \delta \frac{R_x}{R_x + r_{T1} + R_{T2}/(\beta + 1)} = -0.535$$

We now can obtain the variation of the midpoint of the logic swing as

$$\frac{\Delta V_{L1} - \Delta V_{H1}}{2} = -0.685$$

which is approximately equal to that of the reference voltage V_R (0.738).

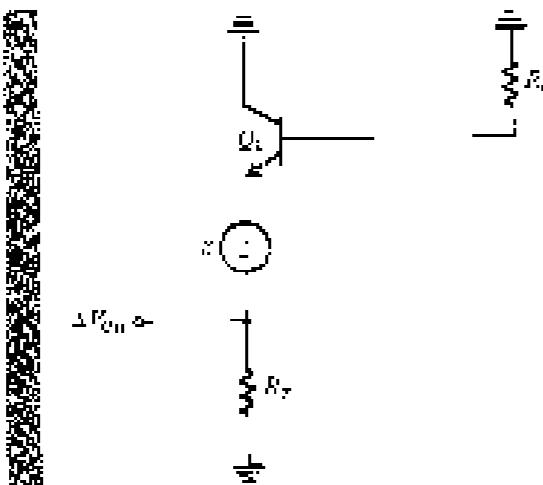


FIGURE 11.43 Equivalent circuit for determining the temperature coefficient of V_{DD} .

11.7.9 The Wired-OR Capability

The emitter-follower output stage of the ECL module allows an additional level of logic to be performed ... very low cost by simply wiring the outputs of several gates in parallel. This is illustrated in Fig. 11.44, where the outputs of two gates are wired together. Note that the base-emitter diodes of the output followers perform an OR function. This wired-OR connection can be used to provide gates with high fan-in as well as to increase the flexibility of ECL in logic design.

11.7.10 Final Remarks

We have chosen to study ECL by focusing on a commercially available circuit family. As has been demonstrated, a great deal of design optimization has been applied to create a very-high-performance family of ECL and MESI logic circuits. As already mentioned, ECL and variants of its variants are also used in VLSI circuit design. Applications include very-high-speed processors such as those used in supercomputers, as well as high-speed and high-frequency communication systems. When employed in VLSI design, current-squared biasing is almost always utilized. Further, a variety of circuit configurations are employed (see Roberts (1990)).

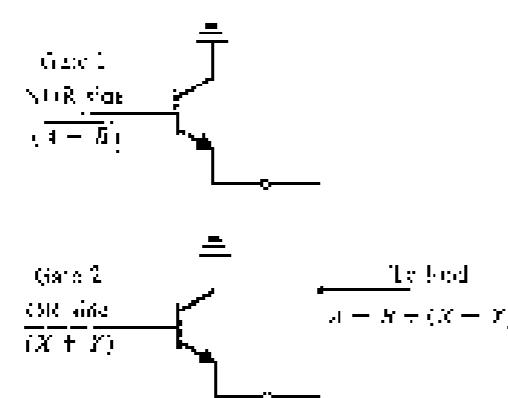


FIGURE 11.44 The wired-OR capability of ECL.

11.8 BiCMOS DIGITAL CIRCUITS

In this section, we provide an introduction to a VLSI circuit technology that is becoming increasingly popular, BiCMOS. As its name implies, BiCMOS technology combines bipolar and CMOS circuits on one IC chip. The aim is to combine the low power, high input impedance, and wide noise margins of CMOS with the high current-driving capability of bipolar transistors. Specifically, CMOS, although a nearly ideal logic circuit technology in many respects, has a limited current-driving capability. This is not a serious problem when the CMOS gate has to drive a few other CMOS gates. It becomes a serious issue, however, when relatively large capacitive loads (e.g., greater than 0.5 pF or so) are present. In such cases, one has to either resort to the use of elaborate CMOS buffer circuits or face the usually unacceptable consequence of long propagation delays. On the other hand, we know that by virtue of its much larger static conductance, the BJT is capable of large output currents. We have seen a practical illustration of that in the emitter-follower output stage of TLL. Indeed, the high current-driving capability contributes to making TLL two to five times faster than CMOS (under equivalent conditions), of course, at the expense of high power dissipation. In summary, then, BiCMOS series attempts to combine the best of the CMOS and bipolar technologies to obtain a class of circuits that is particularly useful when output currents that are higher than those with CMOS are needed. Furthermore, since BiCMOS technology is well suited for the implementation of high-performance analog circuitry, it makes possible the realization of both analog and digital functions on the same IC chip, making the "systems-on-a-chip" an achievable goal. The price paid is a more complex, and hence more expensive (than CMOS) processing technology.

11.8.1 The BiCMOS Inverter

A variety of BiCMOS inverter circuits have been proposed and are in use. All of them are based on the use of open transistors to increase the output current available from a CMOS inverter. This can be most simply achieved by connecting each of the Q_1 and Q_2 devices of the CMOS inverter with an open transistor, as shown in Fig. 11.45(a). Observe that this circuit can be thought of as utilizing the pair of complementary composite MOS-BJT devices shown in Fig. 11.45(b). These composite devices¹⁷ retain the high output impedance of the MOS transistor while in effect multiplying its drain current by the factor β . It is important to observe that the output stage formed by Q_1 and Q_2 has what is known as the full-complement configuration utilized by TTL.

The circuit of Fig. 11.45(a) operates as follows: When v_i is low, both Q_2 and Q_1 are off while Q_3 conducts and supplies Q_1 with a current, thus turning it on. Transistor Q_1 , then, provides a large output current to charge the load capacitance. The result is a very fast charging of the load capacitance and correspondingly a short low-to-high propagation delay, t_{PD} . Transistor Q_1 turns off when v_i reaches a value about $V_{DD} - V_{THN}$, and then the output high level is lower than V_{DD} , a disadvantage. When v_i goes high, Q_2 and Q_1 turn off, and Q_3 turns on, providing its drain current into the base of Q_1 . Transistor Q_1 , then turns on and provides a large output current that quickly discharges the load capacitance. Here again the result is a short high-to-low propagation delay, t_{PD} . On the negative side, Q_1 turns off when v_i reaches a value about V_{DD} , and this the output low level is greater than zero, a disadvantage.

¹⁷ It is often stated to note that these composite devices were proposed as early as 1970 [see Lai et al. (1996)].

¹⁸ Note that the CD4004 operating rail levels form a negative voltage rail in the 17-V-supply circuit since it is a four-pole output stage.

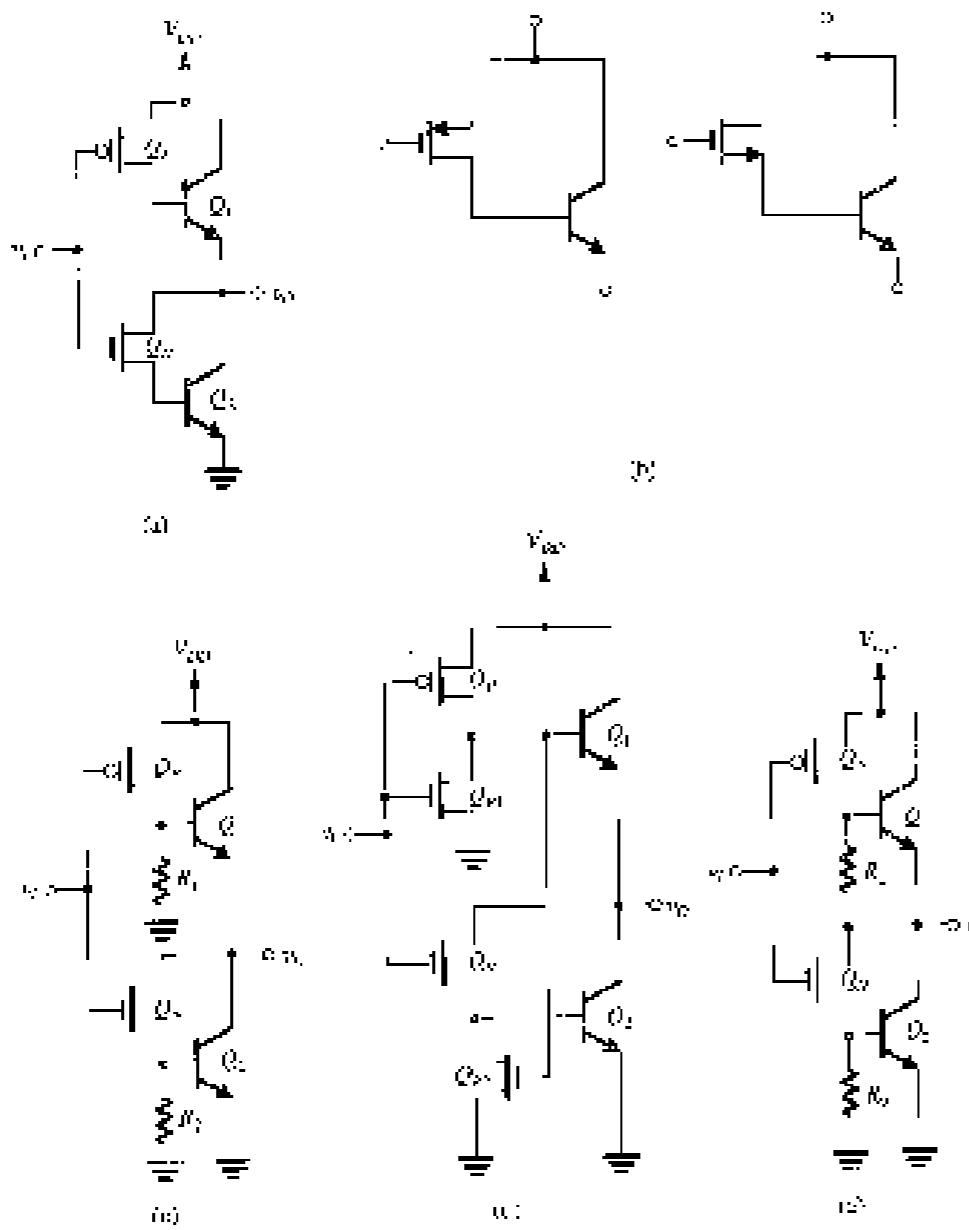


FIGURE 11.45 Development of the BiCMOS inverter circuit. (a) The base concept, as to use an additional bipolar transistor to reduce the output current draw of each of Q_1 and Q_2 of the CMOS inverter. (b) The circuit can be thought of as consisting these composite devices. (c) To reduce the number of Q_1 and Q_2 , "bleeder" resistors R_1 and R_2 are used. (d) Implementation of the circuit in (c) using NMOS transistors to realize the resistors. (e) An improved version of the circuit in (c) obtained by connecting a lower value of R_1 to the output node.

Thus, while the circuit of Fig. 11.45(a) features large output current and short propagation delays, it has the disadvantage of reduced logic swing, and, correspondingly, reduced noise margins. There is also another and perhaps more serious disadvantage, namely, the relatively long turn-off delays of Q_1 and Q_2 arising from the absence of circuit paths along

which the base charge can be removed. This problem can be solved by adding a resistor between the base of each of Q_1 and Q_2 and ground, as shown in Fig. 11.45(c). Now when either Q_1 or Q_2 is turned off, its stored base charge is removed to ground through R_1 or R_2 , respectively. Resistor R_2 provides an additional benefit: With v_i high, and after Q_1 cuts off, v_o continues to fall below V_{DD} , and the output node is pulled to ground through the series path of Q_2 and R_2 . Thus, R_2 functions as a pull-down resistor. The Q_2 - R_2 path, however, is a high-impedance one with the result that putting v_o in ground is a rather slow process. Incorporating the resistor R_1 , however, is disadvantageous from a static power-dissipation stand point: When v_i is low, a dc path exists between V_{DD} and ground through the conducting Q_1 and R_1 . Finally, it should be noted that R_1 and R_2 take some of the drain currents of Q_1 and Q_2 away from the bases of Q_1 and Q_2 , and thus slightly reduce the gate output current available to charge and discharge the load capacitance.

Figure 11.45(d) shows the way in which R_1 and R_2 are usually implemented. As indicated, NMOS devices Q_{1P} and Q_{2P} are used to realize R_1 and R_2 . As an added innovation these two transistors are made to conduct only when needed. Thus, Q_{2P} will conduct only when v_i rises, at which time its drain current constitutes a reverse base current for Q_1 , speeding up its turn-off. Similarly Q_{1P} will conduct only when v_i falls and Q_2 conducts, pulling the gate of Q_{2P} high. The drain current of Q_{2P} then constitutes a reverse base current for Q_2 , speeding up its turn-off.

As a final circuit for the BiCMOS inverter, we show the so-called R -circuit in Fig. 11.45(e). This circuit differs from that in Fig. 11.45(c) in only one respect: Rather than returning R_2 to ground, we have connected R_2 to the output node of the inverter. This simple change has two benefits. First, the problem of static power dissipation is now solved. Second, R_2 now functions as a pull-up resistor, pulling the output node voltage up to V_{DD} (through the conducting Q_{1P}) after Q_1 has turned off. Thus, the R circuit in Fig. 11.45(e) does in fact have output levels very close to V_{DD} and ground.

As a final remark on the BiCMOS inverter, we note that the circuit is designed so that transistors Q_1 and Q_2 are never simultaneously conducting and neither is allowed to saturate. Unfortunately, sometimes the resistance of the collector region of the BJT in conjunction with large capacitive charging currents causes saturation to occur. Specifically, at large output currents, the voltage developed across r_C (which can be of the order of $100\ \Omega$) can lower the voltage at the intrinsic collector terminal and cause the CBT to become forward biased. As the collector will饱和, saturation is a harmful effect for two reasons: It limits the collector current to a value less than βI_S , and it slows down the transistor turn-off.

11.8.2 Dynamic Operation

A detailed analysis of the dynamic operation of the BiCMOS inverter circuit is a rather complex undertaking. Nevertheless, an estimate of its propagation delay can be obtained by considering only the time required to charge and discharge a load capacitance C . Such an approximation is justified when C is relatively large and thus its effect on inverter dynamics is dominant. In other words, when we are able to neglect the time required to charge the parasitic capacitances present at internal circuit nodes. Fortunately, this is usually the case in practice, for if the load capacitance is not large, one would use the simpler CMOS inverter. In fact, it has been shown [Ershabi, Bellalouar, and Elouayy (1993)] that the speed advantage of BiCMOS (over CMOS) becomes evident only when the gate is required to drive a large fan-out or a large load capacitance. For instance, at a load capacitance of $50\ fF$ to $100\ fF$, BiCMOS and CMOS typically feature equal delays. However, at a load capacitance of $1\ pF$, that of a BiCMOS inverter is $0.3\ ns$, whereas that of an otherwise comparable CMOS inverter is about $1\ ns$.

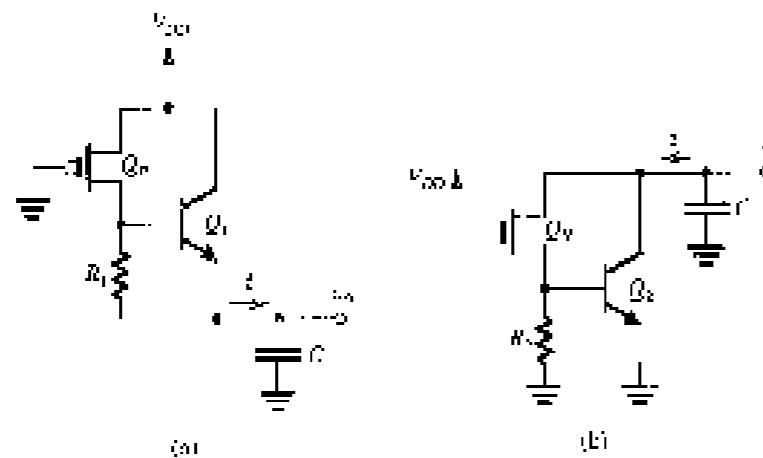


FIGURE 11-46 Equivalent circuit for charging and discharging a bare capacitance C . Note that the internal resistance is zero at the optimum node.

Finally, in Fig. 11.46, we show simplified equivalent circuits that can be employed for obtaining rough estimates of types and levels of the N -type BiCMOS inverter (see Problem 11.55).

11.8.3 BiCMOS Logic Gates

In BiCMOS, the logic is performed by the CMOS part of the gate, with the bipolar part simply functioning as an output stage. It follows that BiCMOS logic-gate circuits can be generated following the same approach used in CMOS. As an example, we show in Fig. 11.4 a BiCMOS logic-inverter.

As a final remark, we note that BiCMOS technology is applied in a variety of products including microprocessors, static RAMs, and gate arrays (see Appendix 1, §93).

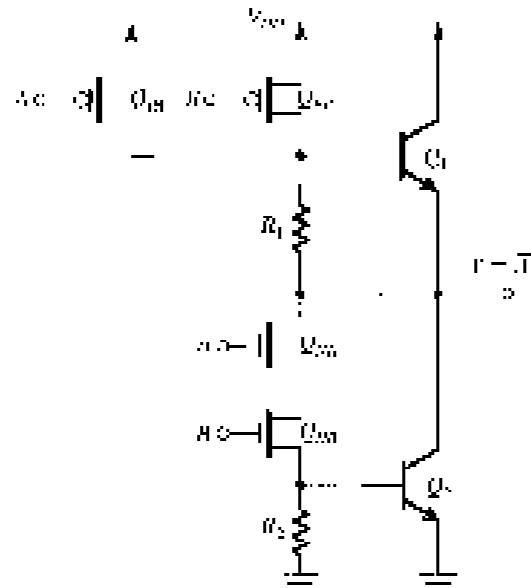


FIGURE 11.47 A BiCMOS two-input NAND gate.

11.9 SPICE SIMULATION EXAMPLE

We conclude this chapter by presenting an example that illustrates the use of SPICE in the analysis of bipolar digital circuits.

STATIC AND DYNAMIC OPERATION OF AN ECL GATE

In this example, we use PSpice to investigate the static and dynamic operation of the ECT gear (studied in Section 11.7) whose Capture schematic is shown in Fig. 11.48.

Having no access to the actual values for the SPOT model parameters of the TBTs utilized in commercially available ECIs, we have selected parameter values representative of the technology used that, from our experience, would lead to reasonable agreement between simulation

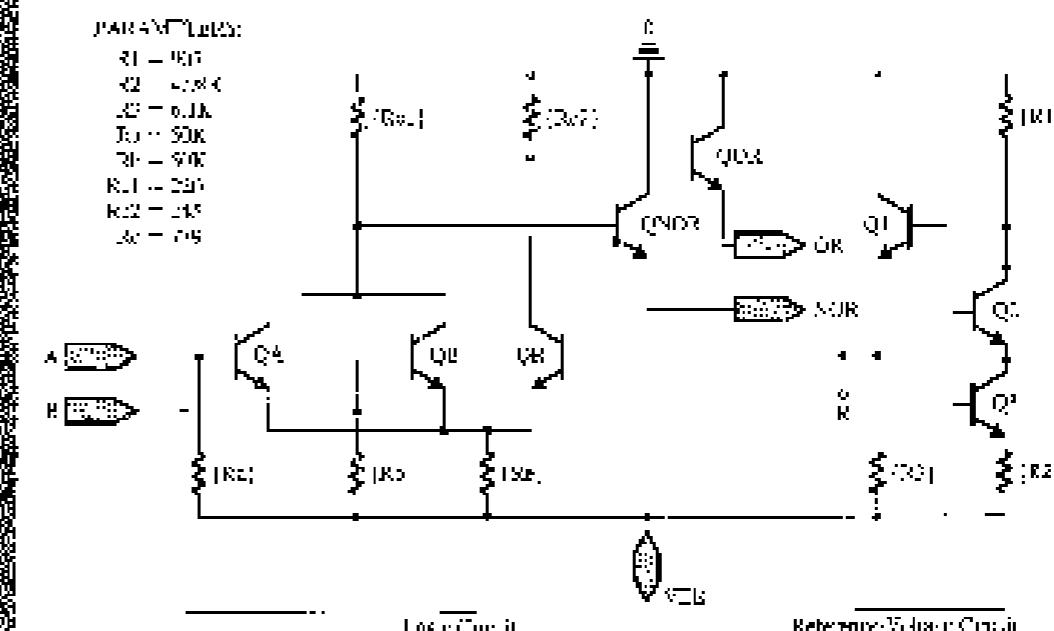


FIGURE 11.42 Capture schematic of the two-step ECI cycle for Fcc-type 11.5.

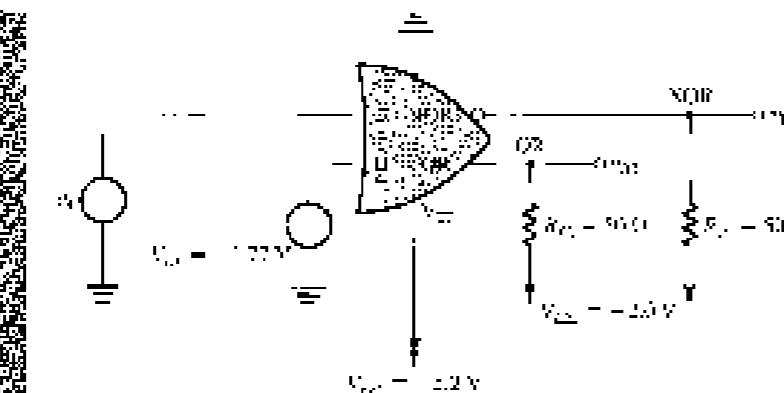


FIGURE 11.49 Current measurement from input A to voltage transfer characteristic of the DCL gate in Fig. 11.4a.

results and the measured performance data supplied by the manufacturer. It should be noted that this problem would not be encountered by an IC designer using SPICE as an aid; again, naturally, the designer would have full access to the proprietary process parameters and the corresponding device model parameters. In any case, for the simulation we conducted, we have utilized the following RTT model parameter values:¹⁷ $\beta_1 = 0.9644$, $\beta_2 = 0.04$, $\beta_3 = 1$, $\gamma_1 = 0.1$, $\gamma_2 = 1$, $C_L = 1\text{ pF}$, $C_{OSS} = 1.5\text{ pF}$, and $|V_A| = 0.0\text{ V}$.

We next employ the circuit arrangement of Fig. 11.40 to compute the voltage transfer characteristics of the ECL gate, that is, V_{DD} and V_{DD} versus v_1 , where v_1 is the input voltage at terminal A. For this investigation, the other input is deactivated by applying a voltage $v_2 = V_{DD} = 1.77\text{ V}$. In TSpice, we performed a dc analysis simulation with v_1 swept over the range -2 V to 2 V in 10 mV increments and plotted V_{DD} and V_{DD} versus v_1 . The simulation results are shown in Fig. 11.50. We immediately recognize the VTCs as those we have seen and (partially) verified by manual analysis in Section 11.4. The two transfer curves are symmetrical about an input voltage of -1.32 V . TSpice also determined V_D , the voltage V_D at the base of the reference transistor (Q_2) has exactly the value of -1.32 V , which is also identical to the value we computed by hand analysis of the reference voltage circuit.

Using Probe (or equivalent features of PSpice), one can determine the values of the important parameters of the VTC, as follows:

$$\text{OR output: } V_{DD} = 1.77\text{ V}, V_{DD} = 0.38\text{ V}, V_D = -1.11\text{ V}, \text{ and } V_H = -1.22\text{ V}; \text{ thus, } \\ M_{D1} = 0.34\text{ V} \text{ and } M_{D2} = 0.36\text{ V}$$

$$\text{NOR output: } V_{DD} = 1.78\text{ V}, V_{DD} = 0.39\text{ V}, V_D = -1.14\text{ V}, \text{ and } V_H = -1.22\text{ V}; \text{ thus, } \\ M_{D1} = 0.34\text{ V} \text{ and } M_{D2} = 0.37\text{ V}$$

These values are remarkably close to those found by pencil-and-paper analysis in Section 11.4.

We next use TSpice to investigate the temperature dependence of the transfer characteristics. The reader will recall that in Section 11.7 we discussed this point of some length and carried out a thermal analysis in Example 11.4. Here, we use TSpice to find the voltage transfer characteristics at two temperatures, $(27^\circ\text{C}$ and 0°C) (the VTCs shown in Fig. 11.50 were computed at 27°C) for two diode cases: the first case with V_D generated as in Fig. 11.4b, and the second with the reference-voltage circuit eliminated and a constant, temperature-independent, reference voltage of -1.32 V applied to the base of Q_2 . The simulation results are displayed in Fig. 11.51. Figure 11.51(a) shows plots

¹⁷ In TSpice, we have created a portion of QECI based on Exact 3.1 model parameter values. Readers can find this netlist in the SHIBA library, which is available on the CD accompanying this book or we.liau@louisville.edu.

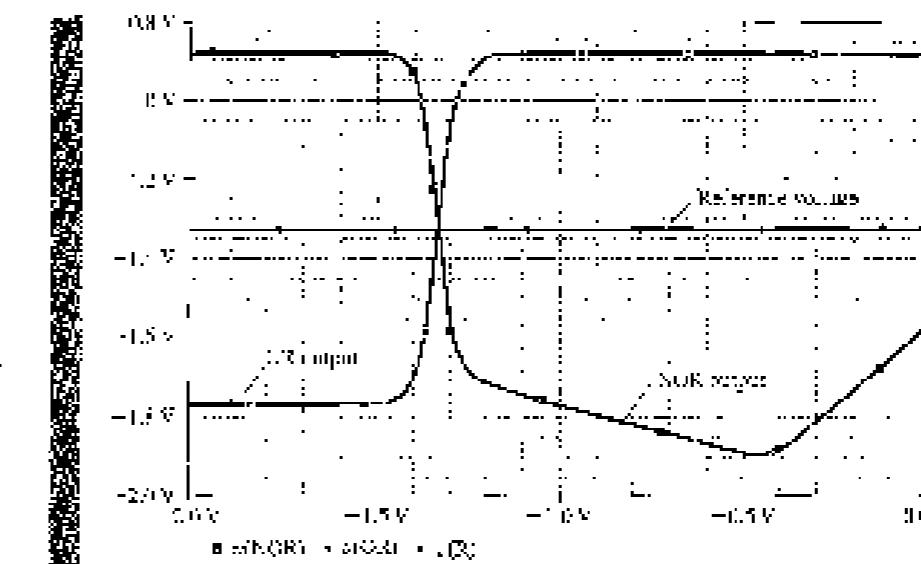
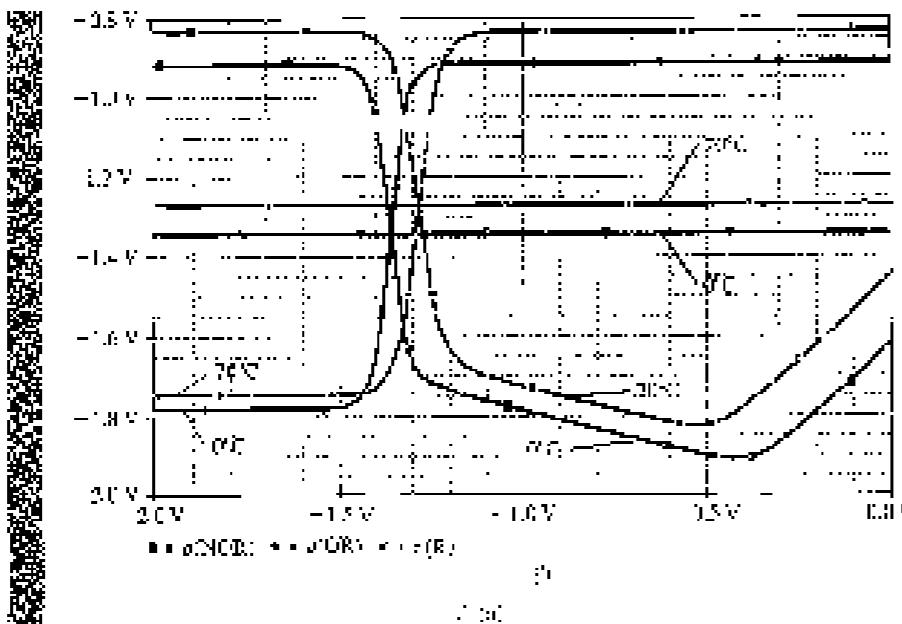


FIGURE 11.50 Voltage transfer characteristic of the OR and NOR outputs for the ECL gate shown in Fig. 11.4a. Also indicated is the reference voltage, $V_D = -1.32\text{ V}$.

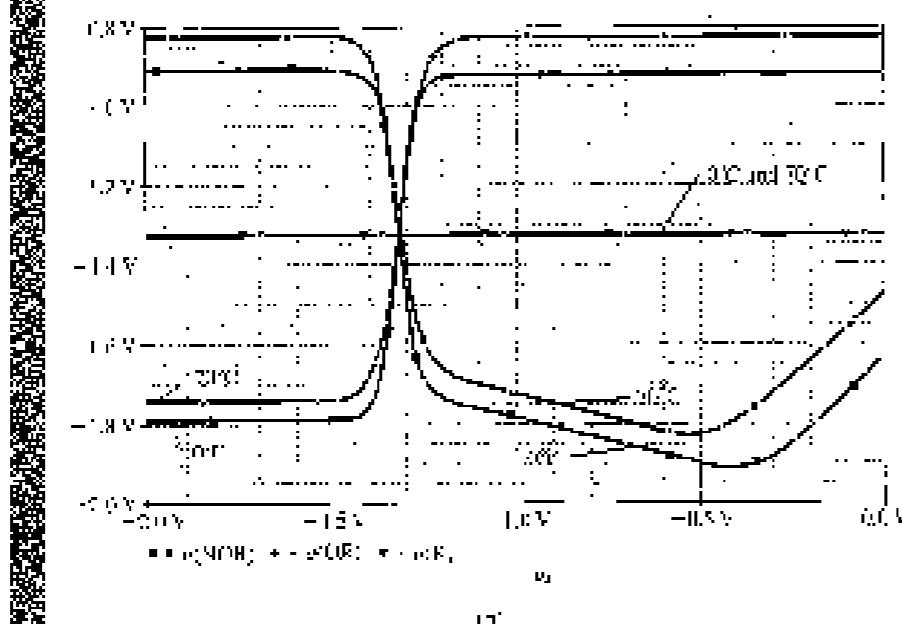
of the transfer characteristics for the case in which the reference circuit is nullified and Fig. 11.51(b) shows plots for the case in which a constant reference voltage is employed. Figure 11.51(a) indicates that as the temperature is varied and V_D changes, the values of V_{DD} and V_{DD} also change but remain nearly equal. As we learned in Section 11.7 (as demonstrated in the analysis of Example 11.4), this is the basic idea behind making V_D temperature dependent. When V_D is not temperature dependent, the symmetry of V_{DD} and V_{DD} around V_D is no longer maintained, as demonstrated in Fig. 11.51(b); similarly, we show in Table 11.1 some of the values obtained. Observe that for the larger temperature case, the

temperature compensation is still present, as shown in Table 11.1. TABLE 11.1 SPICE-Computed Parameter Values of the ECL Gate With and Without Temperature Compensation at Two Different Temperatures

Temperature	Parameter	Temperature Compensated		Not Temperature Compensated	
		OR	NOR	OR	NOR
27°C	V_{DD}	-1.779 V	-1.786 V	-1.786 V	-1.790 V
	V_{DD}	0.9147 V	0.9139 V	0.9147 V	0.9160 V
	$V_{DD} + \frac{V_{DD}}{2}$	-1.3169 V	-1.3541 V	-1.5501 V	-1.3311 V
	V_D	-1.342 V	-1.355 V	-1.32 V	-1.32 V
0°C	$ V_D $	1.6169 V	1.6169 V	1.6169 V	1.6169 V
	V_{DD}	1.742 V	1.80 V	-1.729 V	-1.735 V
	V_{DD}	-0.8138 V	-0.8235 V	-0.8338 V	-0.8395 V
	$V_{DD} + \frac{V_{DD}}{2}$	-1.233 V	-1.29 V	-1.1913 V	-1.264 V
0°C	V_D	-1.271 V	-1.271 V	-1.32 V	-1.32 V
	$ V_D - V_H$	1.7 mV	1.6 mV	1.6 mV	26.2 mV



(a)



(b)

FIGURE 11.51 Comparing the voltage transfer characteristics of the ECL and NOR outputs (see Fig. 11.49 of the ECL gate shown in Fig. 11.48, and the reference voltage V_1 generated using (a) the temperature compensated bias network of Fig. 11.48; (b) a universal temperature voltage source).

average value of V_{T1} and V_{T2} remains very close to V_0 . The reader is encouraged to compare these results to those obtained in Example 11.1.

The dynamic operation of the ECL gate is investigated using the arrangement of Fig. 11.52. Here, two gates are connected by a 1.5-m coaxial cable having a characteristic impedance (Z_0) of

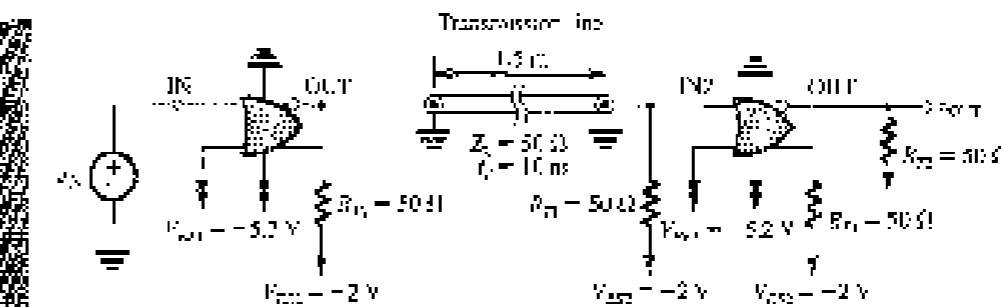


FIGURE 11.52 Circuit arrangement for investigating the dynamic operation of ECL. Two ECL gates (Fig. 11.48) are connected in cascade via a 1.5-m coaxial cable which has a characteristic impedance $Z_0 = 50\Omega$ and a propagation delay $t_p = 10\text{ ns}$. Resistor R_1 and R_2 are placed at the inputs and outputs of the transmission line.

50Ω . The manufacturer specifies that signals propagate along this cable (which is approximately ten times faster than light) half the speed of light, or 15 ns. Thus we would expect the 1.5-m cable we are using to introduce a delay t_p of 10 ns. Observe that in this circuit (Fig. 11.52), resistor R_1 provides the proper cable termination. The cable is assumed to be lossless and is modeled in PSpice using the transmission line element (the T part in the Analog library) with $Z_0 = 50\Omega$ and $t_p = 10\text{ ns}$. A voltage step, rising from -1.77 V to -0.394 V in 1 ns, is applied to the input of the first gate, and a transient analysis over a 10-ns interval is requested. Figure 11.53 shows parts of the waveforms of the input, the voltage at the output of the first gate, the voltage at the input of the second gate, and the output. Observe that despite the very high edge speeds involved, the waveforms are remarkably clean and free of excessive ringing and reflections. This is particularly remarkable

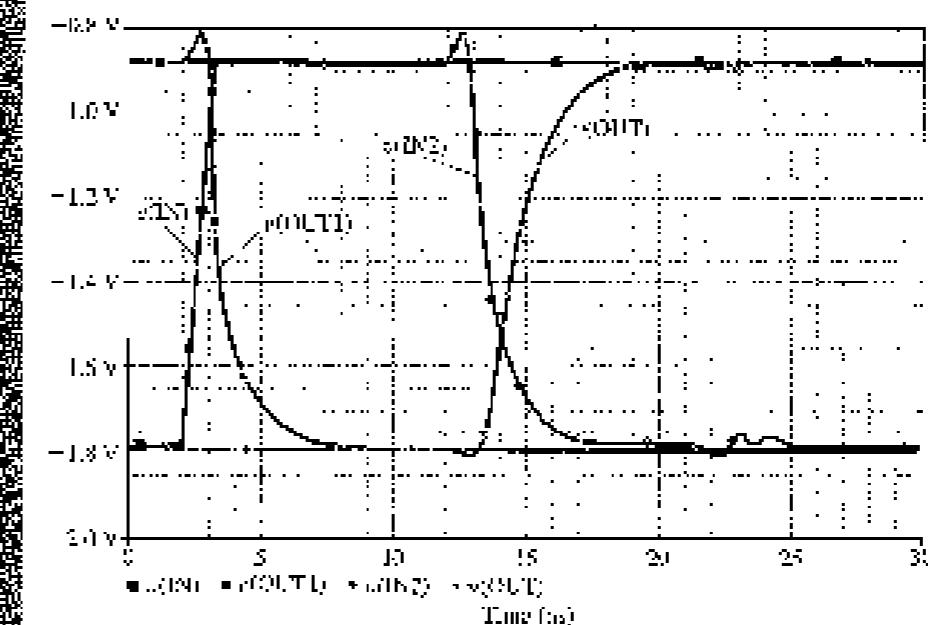


FIGURE 11.53 Transient response of a cascaded ECL gate pair interconnected by a 1.5-m coaxial cable having a characteristic impedance $Z_0 = 50\Omega$ and a delay of 10 ns (see Fig. 11.52).

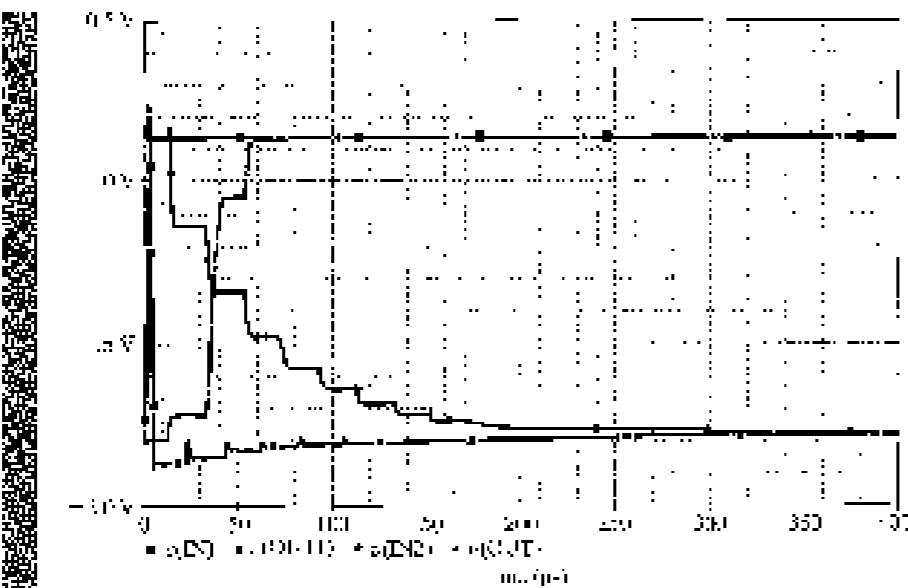


FIGURE 11.54 Transient response of a logic signal from two ECL gates connected by a 150-m cable, using a characteristic impedance of 100Ω . The termination resistance R_t is $\sqrt{Z_0}$ (see Fig. 11.37) or 100Ω , assuming $Z_0 = 100 \Omega$. Note that $a(DT)$ is the state of the $a(DT)$.

because the gate is being transmitted over a relatively long distance. A detailed examination of the waveforms reveals that the delay along the cable is indeed 10 ns , and the delay of the second gate is about 1.20 ns .

Finally, to see if we need to properly terminating the transmission line, the dynamic analysis is repeated this time with the 50Ω coaxial cables shown in Fig. 11.44 instead of cables while keeping the termination resistance unchanged. The results are the same, except one telling and long delayed wave form is shown in Fig. 11.54. (Note the change of plotting scales.)

SUMMARY

- Flip-flops employ two exclusive latches. The basic and the most common circuit implementation uses two inverters connected in a positive feedback loop. The latch can remain in either state indefinitely.
- As an alternative to the positive feedback approach, memory can be provided through the use of charge-storage flip-flops. Bipolar junction transistors are the way, instead of static metal-silicon D flip-flops.
- A monolithic static SR flip-flop has a state in which it cannot maintain itself, known as a metastable state, which is characterized by a random state, which it exists up to a certain time and then it returns to its previous state. It is used for a particular class of logic, "SR flip-flops," which can be used to generate a pulse signal of predetermined height and width.
- A bistable multivibrator has no stable states. Rather, it has two quasi-stable states, between which it oscillates. The oscillator circuit is sustained, i.e., it is not a square-wave generator.
- A ring oscillator is implemented by connecting an odd number of inverters in a loop: $f_{osc} = 1/2.67\mu$.
- A random-access memory (RAM) is one in which the data required to storage (written) or retrieve (or refresh) the stored information is independent of the physical location within the memory, in which the information is stored.
- The major part of a memory chip consists of the cells in which the bits are stored and they are typically organized

in a row matrix. A cell is selected for reading or writing by activating its row, via the row address decoder, and its column, via the column address decoder. The sense amplifier detects the voltage in the selected cell and provides it to the data output terminal of the cell.

- There are two kinds of RAM: SRAMs are static and cache and SRAMs (SRAMs) are dynamic. Up to now, the storage cells in a dynamic RAM (DRAM), data is stored in a capacitor and thus must be periodically refreshed. DRAM chips provide the highest possible storage capacity for a given chip area.
- Although sense amplifiers are utilized in SRAMs in speed-up operation, they are essential in DRAMs. A sense-amplifier-based SRAM cell contains a differential gate that compares feedback or column output signal. This process exponentially toward either V_{DD} or 0 .
- Read-only memory (ROM) contains fixed data patterns that are stored at the time of fabrication and cannot be changed by the user. On the other hand, the contents of a programmable ROM (PROM) can be changed by the user. The erasure and reprogramming of the ROMs is done during the manufacturing process and is performed only subsequently.
- Since EEPROMs utilize floating-gate MOSFETs as the memory cell, the cell is programmed by applying a high voltage to the select gate. Erasing is achieved by illuminating the chip by ultraviolet light. Even more versatile, EEPROMs can be erased and reprogrammed electrically.
- Bipolar-coupled logic (ECL) is the fastest logic-circuit family. It achieves its high speed of operation by avoiding
- transistor saturation and by utilizing small logic signal swings.
- In ECL, the input signals are used to steer a bias current between a reference transistor and an input transistors. The basic gate configuration is that of a differential pair driver.
- There are two popular monolithic available ECL types: ECL 10K, having $t_{pd} = 2 \text{ ns}$, $I_{DD} = 22 \text{ mA}$, and ECL 50K, having $t_{pd} = 0.75 \text{ ns}$, $I_{DD} = 4.7 \text{ mA}$, and $I_{DD} = 0.5 \text{ mA}$. ECL 10K is chosen to use because the rise and fall times of its signals are deliberately made long ($t_{pd} = 2 \text{ ns}$)
- Because of the very high operating speeds of ECL, care should be taken in connecting the output of one gate to the input of another. Transmission-line techniques are usually employed.
- The design of the ECL gate is optimized so that the noise margins are equal and remain equal as temperature changes.
- The ECL gate provides two complementary outputs, realizing the OR and NOR functions.
- The outputs of ECL gates can be wired together to realize the OR function of the individual output variables.
- BiCMOS combines the low power and wide noise margin of CMOS with the high current driving capability (and thus the short gate delay) of LTL technology. Thus, it is capable of implementing very dense, complex, high-speed VLSI circuits that can also include analog modules.

PROBLEMS

SECTION 11.1: LATCHES AND FLIP-FLOPS

- 11.1** Consider the clocked SR flip-flop of Fig. 11.3 for which a minimum-area design is required. Thus Q_1 , Q_2 , Q_3 , and Q_4 are minimum-area devices for which $W/L = 2 \mu\text{m}/1 \mu\text{m}$. All the other components have $W/L = 4 \mu\text{m}/1 \mu\text{m}$, $V_{DD} = 5 \text{ V}$, $V_{SS} = -5 \text{ V}$, $V_T = 2.125 \mu\text{A}/\text{V}^2$, and the total capacitance at each of nodes Q and \bar{Q} is 0.1 pF . Follow the method outlined in Exercise 11.1.
- 11.2** Design the flop of the type shown in Fig. 11.3, determined as minimum-area width required at the set and reset pulses, i.e., Q_1 , Q_2 , Q_3 , and Q_4 are minimum-area devices for which $W/L = 2 \mu\text{m}/1 \mu\text{m}$, $L = 1 \mu\text{m}$, and $C = 0.1 \text{ pF}$. Other components have $V_{DD} = 4 \text{ V}$, $V_{SS} = 0 \text{ V}$, $V_T = 1.5 \mu\text{A}/\text{V}^2$, and the total capacitance at each of nodes Q and \bar{Q} is 0.1 pF . Follow the method outlined in Exercise 11.1.
- 11.3** Consider an n-p-n transistor for the circuit in Fig. 11.5. Related the R signal, set Y and the S inputs to R, set S and R normally rest at relatively high voltage under the control of a relatively high impedance source in series with the n-p-n. What is the minimum W/L required for Q_1 and Q_2 ? Also, find $V_T = 10 \mu\text{V}$, $L = 1 \mu\text{m}$. To guarantee operation and lower switching times, n-p-n devices would normally be used.

which joint logic voltage increases rapidly. For $\bar{Q}_1, \bar{Q}_2, Q_3$, and Q_4 all maintained at 0, $V_{DD} = 2.1$ V ($V_{DD} = 0$), if \bar{Q}_1 can be lowered to 2.3 V by a 2-V system, then \bar{Q}_2 is brought down to 0 V. Assume $V_T = 1$ V, $A_V = 50$, $75 \mu\text{A/V}$.

11.1.4 The clocked SR flip-flop in Fig. 11.3 is not a full complementary CMOS circuit. Sketch the full complete memory version by augmenting the circuit with the PNP corresponding to the PNP complement $\bar{Q}_1, \bar{Q}_2, Q_3$, and Q_4 . Note that the fully complementary version requires 12 transistors. Although the circuit is more complex, it is switchable.

11.1.5 Sketch the complementary CMOS circuit implementation of the SR flip-flop in Fig. 11.3.

11.1.6 Sketch the logic gate symbolic representation of an SR flip-flop using NAND gates. Give the truth table and describe the operation. Also sketch a CMOS circuit implementation.

11.1.7 Consider the latch of Fig. 11.1 as implemented in CMOS technology. Let $nC_s = 20 \mu\text{F}$, $V_T = 20$ mV, $L_s = 25$ nm, $L_d = L_i = 6 \mu\text{m}$, $V_s = 1$ V, and $V_{DD} = 5$ V.

(a) Plot the transfer characteristic of each inverter—that is, v_o versus v_s starting from $v_s = 0$. Draw the hysteresis loop with voltages of 1.15, 2.25, 3.3, 2.75, 3, 3.5, 4, and 5 volts.

(b) Use the characteristics in (a) to determine the loop voltage transfer curve of the latch—that is, v_o versus v_s . Plot the coordinates of points A, B, and C as defined in Fig. 11.1(a).

11.1.8 Two CMOS inverters operating from a 5-V supply have V_s and V_o of 2.12 and 2.69 V and corresponding output pulse of 4.4 V and 4.5 V, respectively, and are connected as a latch. Approximating the unit-gate current per square centimeter of area I_s by a constant I_s between the threshold voltage and the back-to-back drain-to-source characteristic, sketch the back-to-back drain-to-source characteristic. What are the coordinates of point D? What is the loop gain at D?

SECTION 11.2: MULTIVIBRATOR CIRCUITS

11.1.9 For the monostable circuit of Fig. 11.1, use the approximate expression derived in Exercise 11.2 to find the appropriate values for R and C so that $T = 1$ ms and the maximum value of the voltage v_s is 1.4 V. As a result of neglecting R_s in the design, is 2%? Assume that R_{DD} is limited to a maximum value of 1 k Ω .

11.1.10 Consider the monostable circuit of Fig. 11.10 under the condition that $R_{DD} \ll R$. What does the expression for T

reduce to? $V_{DD} = 2$ and 4.2 V, but may vary due to process variations in the range $0.7V_{DD}$ to $0.8V_{DD}$ (including a corresponding variation in T expressed as a percentage of the nominal value).

11.1.11 The waveforms for the monostable circuit of Fig. 11.10 are given in Fig. 11.12. Let $V_{DD} = 10$ V, $V_s = V_{DD}/2$, $R = 10$ k Ω , $C = 0.001 \mu\text{F}$, and $R_{DD} = 100$ M Ω . Find the values of T , A_{V1} , and A_{V2} . By how much does v_s change during the quasi-stable period? What is the peak current through C_1 assuming no load? Sketch.

11.1.12 Using the circuit of Fig. 11.10 design a monostable circuit with CMOS logic for which $R_s = 100$ M Ω , $R_{DD} = 5$ V, and $V_s = 14$ V, and $C = 100 \text{ pF}$ to generate an output pulse of duration $T = 1$ s. What value of R should be used?

11.1.13 By use of the expression given in Exercise 11.5 to find an expression for the frequency of oscillation f_0 for the stable multivibrator of Fig. 11.13 under the condition that $V_s = V_{DD}/2$,

(a) Find suitable values for R and C so that $f_0 = 10$ kHz.

11.1.14 Variations in manufacturing result in the CMOS gates used in implementing the stable circuit of Fig. 11.13 to have threshold voltages in the range 0.44 to 0.57 V with 0.5% using the nominal value. Express the expected corresponding variation in the value of f_0 (from initially) as a percentage of the nominal value. You may use the expression given in Exercise 11.5.

11.1.15 Over-estimation of the circuit of Fig. 11.15 in which a resistor $\propto 10^6$ to 10 Ω is inserted between the main node of C and R and the input node of Cr. This resistor allows the voltage above v_s to rise above V_{DD} and, in general, sketch the resulting modified transfer of v_o , to know that the period T is now given by

$$T = CR + \frac{2V_{DD} - V_D}{2(V_{DD} - V_s)}.$$

11.1.16 Consider a ring oscillator consisting of five inverters, each having $t_{PD} = 10$ ns and $t_{PD} = 40$ ns. Sketch one of the output waveforms and specify its frequency and the percentage of the cycle during which the output is high.

11.1.17 A ring of six odd and four n-pn junction diodes at 20 MHz. Find the propagation delay of the circuit.

SECTION 11.3: SEMICONDUCTOR MEMORIES: TYPES AND ARCHITECTURES

11.1.18 A particular 1-Mbit square memory array has its peripheral circuitry organized to allow for the reading of a 16-bit word. How many address bits will be now required?

11.1.19 For the memory chip described in Problem 11.19, how many words can now be enabled by the row decoder? How many sense amplifiers will be used? What word implementation requires? If the chip power consumption is 50 mW with a 5-V supply for continuous operation with a 200-ns cycle time, and that all the power loss is dynamic, estimate the total capacitance of all logic affected in any one cycle. If we require that 60% of this power loss occurs in array access, calculate the weight capacitor contribution will be the size (load), calculate the capacitance per bit line and per bit for this design. If closer manufacturing control allows the memory array to operate at 2 V, you must larger / memory 60% of the design in technology at about the same power level?

11.1.20 At the beginning of interval Δt , find the values of i_s, I_s , and I_{DD} .

(a) At the beginning of interval Δt , find the values of i_s, I_s , and I_{DD} .

(b) Find an estimate of the average value of I_{DD} during interval Δt .

(c) If $C_g = 50 \text{ fF}$, estimate the capacitance value of C_s to make $V_{DD}/2$. Recalling that regeneration begins when voltage v_s at v_g reaches $V_{DD}/2$, what do you estimate the delay to be?

11.1.21 In order to facilitate analysis of the read operation of the SRAM cell in Example 11.2. This time, assume that V_s and V_{DD} are precharged to $V_{DD}/2$. Also assume the discharge of C_g (see Fig. 11.19(a)) to begin at the instant the voltage on v_s reaches $V_{DD}/2$. Recall that the resistance and capacitance of the word line cause its voltage to rise relatively slowly toward $V_{DD}/2$. Using a approach similar to that in Example 11.2, determine the read delay defined as the time required to reduce the voltage of the bit line by 10%. Assume all other logic and device parameters are those specified in Example 11.2.

11.1.22 A 256-Mbit XRAM chip contains 16-bit read/write memory in a 4-bit design with 8-bit cell size. For a single address bus, bits are allocated for the clock generator, data-in, data-out, and column decoder?

SECTION 11.4: RANDOM-ACCESS MEMORY (RAM) CELLS

11.1.23 Consider the write operation of the SRAM cell of Fig. 11.18. Specifically, refer to relevant parts of the circuit as depicted in Fig. 11.20 (with the power-supply voltage characterized by $V_s/V_D = 0.5$, $\gamma = 0.5 \text{ V}^{1/2}$, $|V_{DD}| = 0.8$ V, $2W = 0.9$ V, and $V_{DD} = 5$ V). Also let each of the two inverters be matched and $2RZ_1 = 2RZ_2 = 2$, where n denotes the 2^n ratio of a minimum-size device.

(a) Using the circuit in Fig. 11.20(a), find the minimum required 90% of Q_2 (in terms of n) so that node \bar{Q} can be pulled to $V_{DD}/2$, that is, $v_s = 2.5$ V, $\bar{v}_D = 0$.

(b) Using the circuit of Fig. 11.20(b), find the minimum required 90% of Q_2 (in terms of n) so that node \bar{Q} can be pulled down to $V_{DD}/2$, that is, $v_s = V_{DD}/2, \bar{v}_D = 0$.

(c) Since Q_2 and Q_1 are designed to have equal 2^n ratios, which of the two values found in (a) and (b) would you choose for n in the final design?

(d) For the value found in (a) or (b), $n = 2$, and $\mu_C = 10 \mu\text{A/V}^2$, determine the time for v_s to reach $V_{DD}/2$. Let $C_s = 50 \text{ fF}$.

11.1.24 Consider the circuit in Fig. 11.20(d), and assume that the device dimensions and process technology parameters are also specified in Example 11.2. We wish to determine the information required for C_g to charge, and its voltage to rise from 0 to $V_{DD}/2$.

(a) At the beginning of interval Δt , find the values of i_s, I_s , and I_{DD} .

(b) At the beginning of interval Δt , find the values of i_s, I_s , and I_{DD} .

(c) Find an estimate of the average value of I_{DD} during interval Δt .

(d) If $C_g = 50 \text{ fF}$, estimate the capacitance value of C_s to make $V_{DD}/2$. Recalling that regeneration begins when voltage v_s at v_g reaches $V_{DD}/2$, what do you estimate the delay to be?

11.1.25 Refer to the analysis of the read operation of the SRAM cell in Example 11.2. This time, assume that V_s and V_{DD} are precharged to $V_{DD}/2$. Also consider the discharge of C_g (see Fig. 11.19(d)) to begin at the instant the voltage on v_s reaches $V_{DD}/2$. Recall that the resistance and capacitance of the word line cause its voltage to rise relatively slowly toward $V_{DD}/2$. Using a approach similar to that in Example 11.2, determine the read delay defined as the time required to reduce the voltage of the bit line by 10%. Assume all other logic and device parameters are those specified in Example 11.2.

11.1.26 For a particular DRAM design, the cell capacitor is $C_s = 50 \text{ fF}$, $V_{DD} = 5$ V, and $V_s = 1.5$ V. (Note that the word line voltage is 1.5 V.) Each cell requires a specific load on the bit line of 2 pF. The sense amplifier and other circuitry attached to the bit line has a 20 fF capacitance. What is the maximum number of cells that can be achieved to a bit line while ensuring a minimum access time of 100 ns? How many bits of raw memory can be used? The sense-amplifier gain is increased by a factor of 3, how many word lines addressed can be accommodated?

11.1.27 For a DRAM available for regular use (90S:1), which having a row-to-column ratio of 2:1, a cycle time of 20 ns, and a refresh cycle of 8 ms, estimate the total memory capacity.

11.1.28 In a particular dynamic memory chip, $C_s = 25 \text{ fF}$, the bit-line capacitance per cell is 1.1 fF and the cell count of memory devices is 1.1 fF. For a 1-Mbit square array, what bit-line length is required when one cell is read? When a stored 0 is read? Assume that $V_{DD} = 5$ V and V_s (including the body effect) = 1.5 V. Recall that the bit line are precharged to $V_{DD}/2$.

11.1.29 For a DRAM cell utilizing a capacitance of 25 fF, which is required within 0.6 ns. The bit-line has the capacitance of 1 fF. What is the largest read/write voltage swing that can be tolerated?

SECTION 11.5: SENSE AMPLIFIERS AND ADDRESS DECODERS

D11.39 Consider the operation of the differential sense amplifier of Fig. 11.22 following the issue of the sense control signal S_0 . Assume that a balanced differential signal of 0.2 V is established between the bit lines, each of which goes to a capacitor, C_{bit} . If $V_{\text{DD}} = 3 \text{ V}$, what is the value of S_0 at each of the inverters X_1 in the switches required to cause the outputs to reach $0.1V_{\text{DD}}$ and $0.5V_{\text{DD}}$? (Initial values of $0.1V_{\text{DD}} = (0.1/2)$ and $0.5V_{\text{DD}} = (0.1/2) + 1 \text{ V}$, respectively.) (Ans: 1.78) If the matched inverters, $V_L = 0.8 \text{ V}$ and $I_L = 3 \text{ A} = 75 \mu\text{A/mm}^2$, what are the device widths required? (If the input signal is 0.2 V , what does the output driver response time become?)

11.31 A particular version of the regenerative varactor amplifier of Fig. 11.29 in a GaAs technology uses transistors for which $V_T = 0.8$ V, $I_{DS}^S = 10\text{A}/\mu\text{m}^2$, $V_{DS} = 5.3$ V, with $(V_{GS})_0 = 6$ $\mu\text{m}^2/\text{C}$ and $(V_{DS})_0 = 1$ $\mu\text{m}^2/\text{C}$. The width of the gate for the source-drain pair is $10 \mu\text{m}$.

will be the amplifier response time when ω_0 is real? When ω_0 is real?

11.3.4 Consider a 512 row NOR memory. To how many address bits does this correspond? How many output lines does it have? How many input lines does the NOR memory require? How many NMOS and PMOS transistors does such a memory have?

11.35 For the column decoder shown in Fig. 1.37, how many column-address bits are needed to 256 K bit square array? How many NMOS pass transistors are needed in the multiplexer? How many NMOS transistors are needed in the NOR decoder? How many PMOS transistors are used? Why is the total number of NMOS and PMOS transistors needed?

11.3.6 Consider the use of the tree code in [Problem 11.2](#) shown in Fig. 11.23 for application with a square 256-Kbit array. How many address bits are involved? How many levels of prefetching are used? How many page translations are there in total?

SECTION 11.6: READ-ONLY MEMORY (ROM)

11.37 List the eight nodes stored in the ROM of Fig. 11.20.

D11.38 Design the bit pattern to be stored in a 16 × 4-RAM that provides the 4-bit product of two 2-bit variables. Give a circuit diagram of the RAM array using a 74HC similar to that of Fig. 11-29.

11.39 Consider a dynamic version of the ROM in Fig. 11.29 in which the gates of the PMOS devices are connected to a precharge control signal, V_{ctrl} . Let all the NMOS devices have $W/L = 2 \mu\text{m} \times 1.2 \mu\text{m}$ and all the PMOS devices have $W/L = 12 \mu\text{m} \times 1.2 \mu\text{m}$. Assume $V_t = M_t = 90 \mu\text{A}/\text{V}^2$, $V_{\text{ctrl}} = -V_{\text{DD}} = 1.8 \text{ V}$, and $V_{\text{DD}} = 5 \text{ V}$.

(c) During the overcharge interval, ω is lowered to 0.5 V. Estimate the time required to charge a bat line from 0 to 5.5 V. Use an average charging current. The battery is supplied by a PMOS transistor at a bat line voltage V_{bat} less than the 0 to 5 V extension, i.e., 2.5 V. The bat line capacitance is 1 pF. Note that all NMOS BSs are turned off at this time.

(b) After the precharge interval is completed and a memory cell at V_{CC} , the row decoder takes the average of the selected word lines. Because of the fin's resistance and capacitance of the word lines, the voltage class exponentially toward V_{DD} . If the resistance of each of the poly-silicon word lines is $5\text{ k}\Omega$ and the capacitance between the word line and ground is 1 pF , what is the (0% to 90%) rise time of the word-line voltage? What is the voltage reached at the end of time $t = 0.1\text{ ns}$?

(c) If we approximate the exponential rise of the wave line voltage by a straight line to the voltage needed to turn the transistor ON, find the interval Δt required for an NMOS gate to discharge the bias line and lower its voltage by $1V$.

SECTION 11.7: Emitter-Coupled Logic (ECL)

P11.40 For the ECL circuit in Fig. P11.30, the transistors have a threshold voltage V_{T0} of 0.75 V at an emitter current I_E and have very high β .

- (a) Find V_{DD} and V_{SS} .

 - For the input at 0 sufficiently negative for Q_2 to be cut off what voltage at 4 causes a change of 10% in flow in Q_3 ?
 - Repeat the bias current in Q_3 at 0.98A.
 - Request (c) for a current in Q_3 of 0.01A.
 - Use the results of (c) and (d) to specify R_A and V_{AB} .
 - Find ΔV_D and ΔV_S .
 - Find the voltage V_D that makes the noise minimum equal to the width of the transition region, $V_{DD} - V_{DS}$.
 - Using the M -value calculated in (g), give numerical values for V_{DD} , V_{SS} , V_{AB} , V_{DS} , and V_D for this FET.

11.4.1 Three logic inverters are connected in a ring. Specifications for this family of gates indicates a typical propagation delay of 2 ns for high-to-low current transitions and 1 ns for low-to-high transitions. Assume that it takes 1 ns to re-invert the input to one of the gates under goes a low-to-high transition. By sketching the waveforms at the outputs of the three gates and keeping track of their relative positions, show that the circuit functions in an oscillator while the frequency of oscillation of this uncontrolled ring is roughly 10 ns long. (The output of the first gate is the input to the second, etc.)

*11.42 To leverage the idea of turning as little as introduced in Problem 11.21, consider an implementation using *string*'s *if* version.

Fig. 11. TRNG inverters. Assume that the inverters have no delay along the falling edges (and thus the waveforms are trapezoidal in shape). Let the first 50% rise and fall times be equal to 1 ns. Also, let the propagation delay (t_p) in both transistors be 1 ns. Let $T = 1$ ns. Propagate a trapezoidal signal of the five output nodes, taking care that relevant phase information is preserved. What is the response of node N_1 ?

11.43 Using the logic and circuit flexibility of TCL indicated by Figs. 11.34 and 11.44, sketch a TCL logic circuit that realizes the exclusive-OR function $Y = A \oplus B$.

***11.44** For the circuit in Fig. 11.65, if the load current i_L is 1 A, the load voltage v_{L1} is 10 V, and the load power is 10 W, find the load power factor. The input voltage v_{in} is 120 V, and the source resistance is 1Ω . Assume $\mu = 100$. Use the results of Exercise 11.20, and let the circuit in Fig. 11.65 be the same as that in Fig. 11.44.

11.45 For the circuit in Fig. 11.36, whose transfer characteristic is shown in Fig. 1–42, find V_{in} and V_{out} if v_+ and v_- are defined as the outputs of op^+ .

(b) 99% of the time, t is switched
at $y = 2\pi$ of the current t , i.e., see (d).

11.46 For the symmetrical balanced circuit of Fig. 11-46, for balanced input signal levels $V_{in1} = -1.88 \text{ V}$ and $V_{in2} = +1.77 \text{ V}$, calculate the power in each load resistor R_L and determine the crosstalk. What does this tell you?

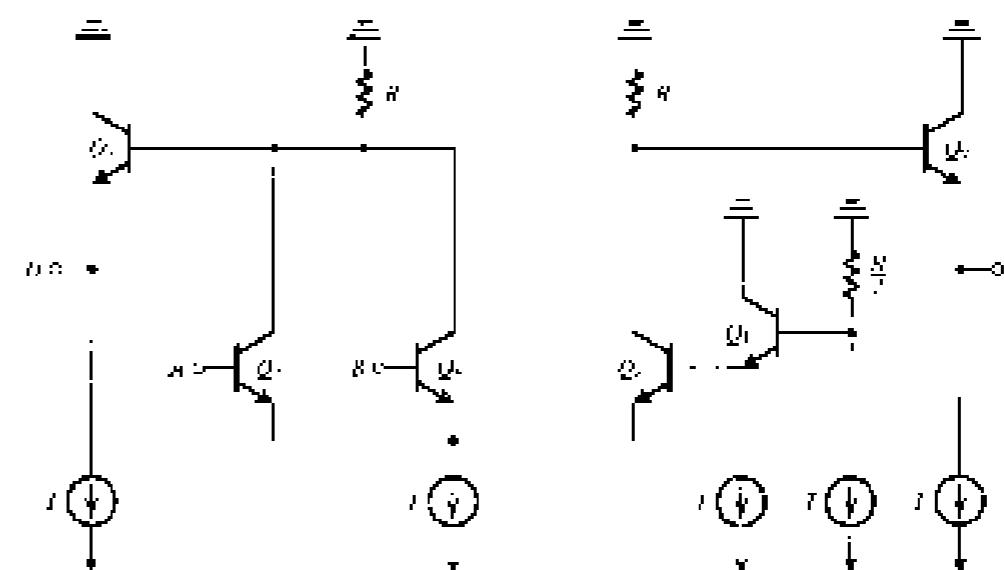


FIGURE P17.90

disconnected at a single \bar{Q}_1 gate including its symmetrical output terminals? Why?

11.47 Considering the circuit of Fig. 11.48, what is the value of β of \bar{Q}_1 for which the high noise margin (N_MH) is increasing 50%?

11.48 Consider an ECL gate whose inverting output is terminated in a 50Ω resistance connected to a -5 V supply. Let the total load capacitance be denoted C_L . As the input of the gate rises, the output emitter follower turns off and the load capacitance C_L discharges through the 50Ω load until the emitter follower conducts again. Find the value of β that will result in a discharge time of 1 ns. Assume that the two output levels are -0.85 V and -1.77 V .

11.49 For signals whose rise and fall times are 2.5 ns , what length of unshielded gate-to-gate wire interconnect can be used if a rise or fall time to return time of 5% is required? Assume the capacitance of the wire to be such that the signal propagates at two-thirds the speed of light ($c = 300\text{ nm}$).

11.50 For the circuit in Fig. 11.50 let the level of the inputs A , B , C , and D be 0 and $+5\text{ V}$. To what minimum ratio V_A

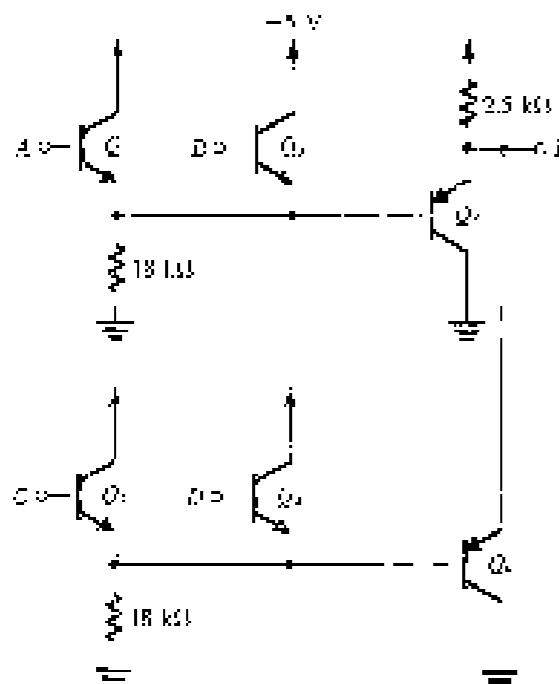


FIGURE P11.50

will the voltage at $E1E2A$ and C are raised to -5 V , while the voltage at $E1$ assume $|V_{BE}| = 0.7\text{ V}$ and $\beta = 50$. Express B as a logic function of A , B , C , and D .

SECTION 11.8: BJCMOS DIGITAL CIRCUITS

11.51 Consider the conventional BiCMOS circuit of Fig. 11.45(a); for the conditions of $V_{DD} = 5\text{ V}$, $V_T = 1\text{ V}$, $V_{BE} = 0.7\text{ V}$, $\beta = 100$, $N_A = 2.5\mu\text{m}^2$, $L_D = 100\mu\text{m}^2$, and $(W/L)_D = 2\mu\text{m}/1\mu\text{m}$. For $i_D = i_A = V_{DD}/2(1/\beta + (W/L)_D)$, at $t = 0$, $i_{Q_1} = I_{Q_2} = 0$. What is this initial-pulse current, and

11.52 Consider the complementary BiCMOS circuit of Fig. 11.45(b) for the conditions stated in Problem 11.51. What is the threshold voltage of the inverter? Both Q_1 and Q_2 have $N_A = 2\mu\text{m}^2/\mu\text{m}^2$? What is the peak current, i_{Q_1} , at t_2 , equal to the threshold voltage?

11.53 Consider the choice of values for R_1 and R_2 in the circuit of Fig. 11.45(c). An important consideration in making the choice is that the loss of base-drive current be limited. This loss becomes particularly acute when the current through Q_1 and Q_2 becomes small. This in turn happens near the end of the amp-to-signal swing when the associated MOS devices are operating in triode operation (say at $|V_{DS}| = |V_{GS}|$). Desirable values for R_1 and R_2 so that the loss in base current is limited to 50% when i_{Q_1} and i_{Q_2} is 100 pA. Report for a 20% loss in base drive.

11.54 For the circuit of Fig. 11.45(d) with parameters as in Problem 11.51 and with $(W/L)_D \sim (W/L)_I$, estimate the propagation delays t_{PD} , t_{PR} and t_{PF} obtained for a load capacitance of 2 pF . Note, however, that calculated node capacitances do not sum to zero in this result. Use average values for the switch-on charging and discharging currents.

11.55 Review Problem 11.54 for the circuit in Fig. 11.45(e), assuming that $R = R_2 = 5\text{k}\Omega$.

11.56 Considering the dynamic response of the NAND gate of Fig. 11.46 with a large external capacitive load. If the worst-case response is to be identical to that of the inverter of Fig. 11.43(e), how must the (W/L) ratios of Q_{11} , Q_{12} , Q_{21} , Q_{22} be related?

11.57 Sketch the circuit of a BiCMOS four-input NOR gate. If when loaded with a large capacitance the gate is to have worst-case delays equal to the corresponding values of the levels of F_{DD} , 11.45(e), and W/L of each transistor in terms of $(W/L)_D$ and $(W/L)_I$.

CHAPTER 12

Filters and Tuned Amplifiers

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INTRODUCTION

In this chapter, we study the design of an important building block of communications and instrumentation systems: the electronic filter. Filter design is one of the very few areas of engineering for which a complete design theory exists, starting from specification and working with a circuit realization. A detailed study of filter design requires an entire book, and indeed such textbooks exist. In the limited space available here, we shall concentrate on a selection of topics that provide an introduction to the subject as well as a useful subset of filter circuits and design methods.

The oldest technique for realizing filters makes use of inductors and capacitors, and the resulting circuits are called passive LC filters. Such filters work well at high frequencies,

however, in low-frequency applications (ω to 100 kHz) the required inductors are large and physically bulky, and their characteristics are quite nonlinear. Furthermore, such inductors are impossible to fabricate in monolithic form and are incompatible with any of the modern techniques for assembling electronic systems. Therefore, there has been considerable interest in finding filter realizations that do not require inductors. Of the various possible types of inductorless filters, we shall study active-RC filters and switched-capacitor filters.

Active-RC filters utilize op-amps together with resistors and capacitors and are fabricated using discrete, hybrid, thin-film, or hybrid thin-film technology. However, for large-volume production, such technologies do not yield the economies achieved by monolithic (IC) fabrication. At the present time, the most viable approach for realizing fully integrated monolithic filters is the switched-capacitor technique.

The last topic studied in this chapter is the tuned amplifier commonly employed in the design of radio and TV receivers. Although tuned amplifiers are in effect bandpass filters, they are studied separately because their design is based on somewhat different techniques.

12.1 FILTER TRANSMISSION, TYPES, AND SPECIFICATION

12.1.1 Filter Transmission

The filters we are about to study are linear circuits that can be represented by the general two-port network shown in Fig. 12.1. The filter transfer function $T(j\omega)$ is the ratio of the output voltage $V_o(j\omega)$ to the input voltage $V_i(j\omega)$:

$$T(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} \quad (12.1)$$

The filter transmission is found by evaluating $T(j\omega)$ for physical frequency ω , $\omega = j\omega$, and can be expressed in terms of its magnitude and phase as

$$T(j\omega) = |T(j\omega)|e^{j\phi(\omega)} \quad (12.2)$$

The magnitude of transmission is often expressed in decibels in terms of the gain function

$$G(\omega) = 20 \log|T(j\omega)|, \text{ dB} \quad (12.3)$$

or, alternatively, in terms of the attenuation function

$$A(\omega) = -20 \log|T(j\omega)|, \text{ dB} \quad (12.4)$$

A filter shapes the frequency spectrum of the input signal, $V_i(j\omega)$, according to the magnitude of the transfer function $|T(j\omega)|$ thus providing an output $V_o(j\omega)$ with a spectrum

$$V_o(j\omega) = T(j\omega)V_i(j\omega) \quad (12.5)$$

Also, the phase characteristics of the signal are modified as it passes through the filter according to the filter phase function $\phi(\omega)$.



FIGURE 12.1 The filters studied in this chapter are linear two-port networks of the general two-port network shown. The filter transfer function $T(j\omega) = V_o(j\omega)/V_i(j\omega)$.

12.1.2 Filter Types

We are specifically interested here in filters that perform a frequency-selection function, passing signals whose frequency spectrum lies within a specified range, and stopping signals whose frequency spectrum falls outside this range. Such a filter has ideally a frequency band (or band) over which the magnitude of transmission is unity (the filter passband) and a frequency band (or bands) over which the transmission is zero (the filter stopbands). Figure 12.2 defines the ideal transmission characteristics of the four major filter types. Low-pass (LP) in Fig. 12.2(a), high-pass (HP) in Fig. 12.2(b), bandpass (BP) in Fig. 12.2(c), and bandstop (BS) or band-reject in Fig. 12.2(d). These idealized characteristics, by virtue of their vertical edges, are known as brick-wall responses.

12.1.3 Filter Specification

The filter design process begins with the filter user specifying the transmission characteristics required of the filter. Such a specification cannot be of the form shown in Fig. 12.3 because physical circuits cannot realize these idealized characteristics. Figure 12.3 shows realistic specifications for the transmission characteristics of a low-pass filter. Observe that since a physical circuit cannot provide constant transmission over all bandwidth requirements, the specifications allow for deviation of the bandwidth transmission from the ideal. One places no upper bound, ω_{∞} , on this deviation. Depending on the specification, ω_{∞} typically ranges from 0.05 dB to 2 dB. Also, since a physical circuit cannot provide zero transmission at all acceptable frequencies, the specifications in Fig. 12.3 allow for some transmission

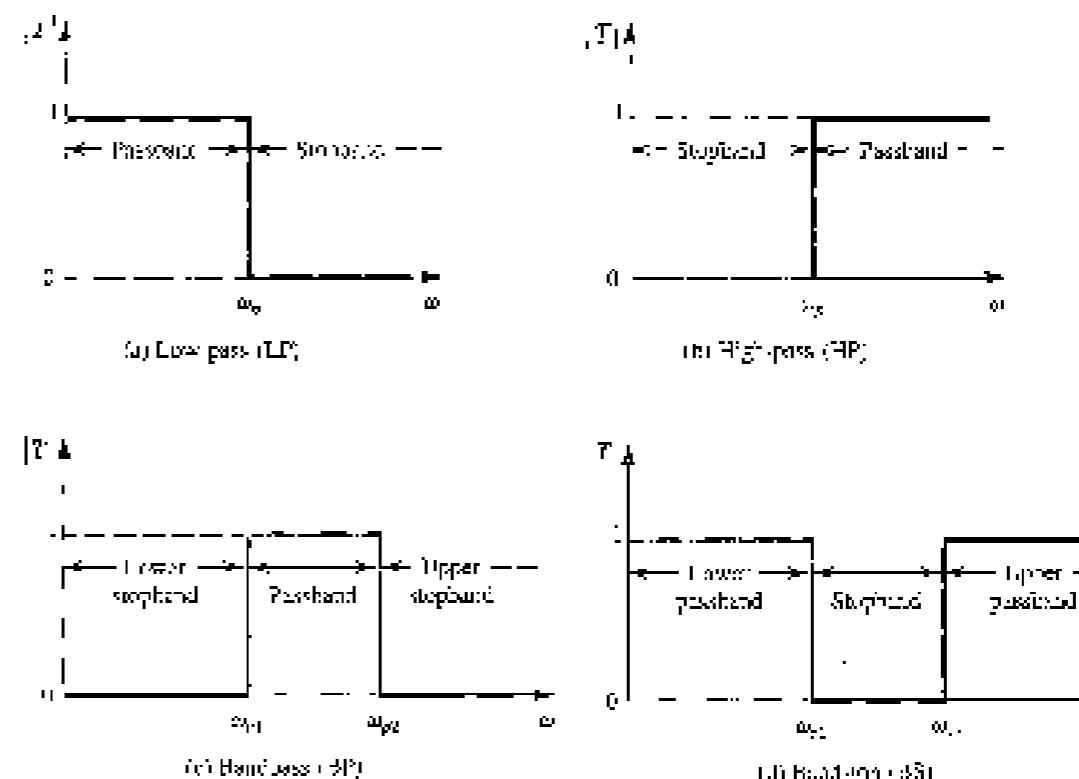


FIGURE 12.2 Ideal transmission characteristics of four major filter types: (a) low-pass (LP), (b) high-pass (HP), (c) bandpass (BP), and (d) bandstop (BS).

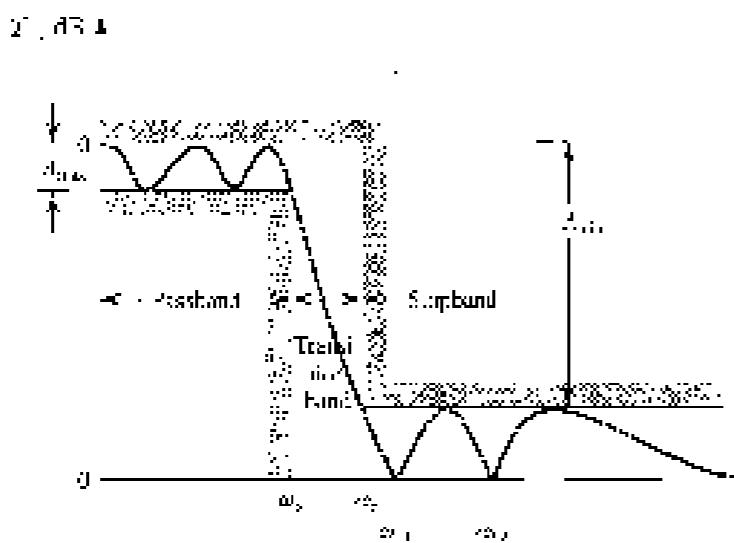


FIGURE 12.3 Specification of the transmission characteristics of a low-pass filter. The magnitude response curve other than just meets specifications is also shown.

over the stopband. However, the specifications require the stopband signals to be attenuated by at least A_{stop} (dB) relative to the passband signals. Depending on the filter applicator, A_{stop} can range from 20 dB to 100 dB.

Since the transmission of a physical circuit cannot change abruptly at the edge of the passband, the specifications of Fig. 12.3 provide for a band of frequencies over which the attenuation increases from near 0 dB to A_{stop} . This transition band extends from the passband edge ω_p to the stopband edge ω_s . The ratio ω_s/ω_p is usually used as a measure of the sharpness of the low-pass filter response and is called the selectivity factor. Finally, observe that for convenience the passband transmission is specified to be 0 dB. The final filter, however, can be given a passband gain, if desired, without changing its selectivity characteristics.

To summarize, the transmission of a low-pass filter is specified by four parameters:

1. The passband edge ω_p
2. The maximum allowed variation in passband transmission, A_{max}
3. The stopband edge ω_s
4. The minimum required stopband attenuation A_{stop}

The more tightly one specifies a filter—that is, lower A_{max} , higher A_{stop} , and/or a selectivity ratio ω_s/ω_p closer to unity—the closer the response of the resulting filter will be to the ideal. However, the resulting filter circuit must be of higher order and thus more complex and expensive.

In addition to specifying the magnitude of transmission, there are applications in which the phase response of the filter is also of interest. The filter design problem, however, is considerably complicated when both magnitude and phase are specified.

Once the filter specifications have been decided upon, the next step in the design is to find a transfer function whose magnitude meets the specification. To meet specification, the magnitude-response curve must lie in the shaded area in Fig. 12.3. The curve shown in the figure is an filter that just meets specifications. Observe that for this particular filter the magnitude response ripples throughout the passband with the ripples peaks being all

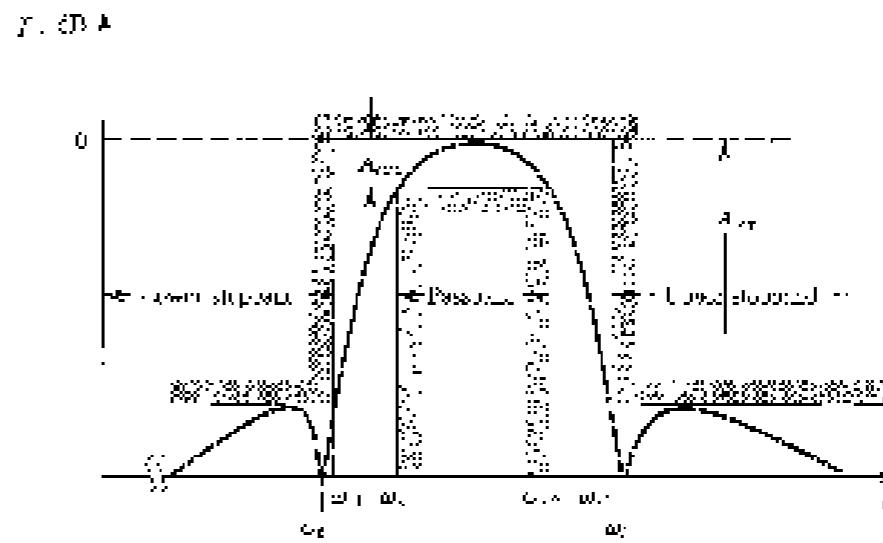


FIGURE 12.4 Transmission specifications for a bandpass filter. The magnitude response of a filter that just meets specifications is also shown. Note that (top) $\omega_c = \omega_1$; (bottom) $\omega_c = \omega_1 + \omega_2$ (minimum decreasing transmission in the passband on both sides of the peak frequency).

equal. Since the peak ripple is equal to A_{max} , it is usual to refer to A_{max} as the passband ripple and to ω_p as the ripple bandwidth. The particular filter response shown ripples also in the stopband, again with the ripple peaks at equal and of such a value that the minimum stopband attenuation achieved is equal to the specified value, A_{stop} . Thus this particular response is said to be equiripple in both the passband and the stopband.

The process of obtaining a transfer function that meets given specifications is known as filter approximation. Filter approximation is usually performed using computer programs (Snedgrove, 1982; Oishi and Sodha, 1995) or filter design tables (Zverev, 1967). In simpler cases, filter approximation can be performed using closed-form expressions, as will be seen in Section 12.3.

Finally, Fig. 12.4 shows transmission specifications for a bandpass filter and the response of a filter that meets these specifications. For this example we have chosen an approximating function that does not ripple in the passband; rather, the transmission decreases monotonically on both sides of the center frequency, obtaining the maximum allowable deviation at the two edges of the passband.

EXERCISES

12.1. A low-pass filter has the following magnitude response: $A(\omega) = 10 \log \left(1 + \frac{\omega^2}{\omega_p^2} \right)$, where $\omega_p = 0.7, 0.5, 0.1, 0.05$.

Determine $(0, 0.1, 1, 2, 5, 20, 40, 100)$.

12.2. If the minimum stopband requirement is to permit a signal to be within $\pm 5\%$ of the applied voltage, the minimum stopband attenuation is 40 dB of the maximum transmission.

12.3. The minimum stopband requirement is to permit a signal to be within $\pm 5\%$ of the applied voltage, the minimum stopband attenuation is 40 dB of the maximum transmission.

12.2 THE FILTER TRANSFER FUNCTION

The filter transfer function $T(s)$ can be written as the ratio of two polynomials as

$$T(s) = \frac{a_0 s^M + a_1 s^{M-1} + \dots + a_M}{b_0 s^N + b_1 s^{N-1} + \dots + b_N} \quad (12.6)$$

The degree of the denominator, N , is the **filter order**. For the filter circuit to be stable, the degree of the numerator must be less than or equal to that of the denominator: $M \leq N$. The numerator and denominator coefficients, a_0, a_1, \dots, a_M and b_0, b_1, \dots, b_N , are real numbers. The polynomials in the numerator and denominator can be factored, and $T(s)$ can be expressed in the form

$$T(s) = \frac{s_{p_1}(s - z_1)(s - z_2) \cdots (s - z_{p_1})}{(s - p_1)(s - p_2) \cdots (s - p_{p_2})} \quad (12.7)$$

The numerator roots, z_1, z_2, \dots, z_{p_1} , are the **transfer-function zeros**, or transmission zeros; and the denominator roots, p_1, p_2, \dots, p_{p_2} , are the **transfer-function poles**, or the natural modes.¹ Each transmission zero or pole can be either a real or a complex number. Complex zeros and poles, however, must occur in conjugate pairs. Thus, if $-1 - j/2$ happens to be a zero, then $-1 + j/2$ also must be a zero.

Since in the filter stopband the transmission is required to be zero or small, the filter transmission zeros are usually placed on the *j*axis at stopband frequencies. This indeed is the case for the filter whose transmission function is sketched in Fig. 12.1. This particular filter can be seen to have infinite attenuation (zero transmission) at two stopband frequencies: ω_0 and ω_2 . The filter then must have transmission zeros at $s = +j\omega_0$ and $s = -j\omega_0$. However, since complex zeros occur in conjugate pairs, there must also be transmission zeros at $s = -j\omega_2$ and $s = +j\omega_2$. Thus the numerator polynomial of this filter will have the factors $(s + j\omega_0)(s - j\omega_0)(s - j\omega_2)(s + j\omega_2)$, which can be written as $(s^2 - \omega_0^2)(s^2 + \omega_2^2)$. For $s = j\omega$ (physical frequencies) the numerator becomes $(\omega^2 - \omega_0^2)(\omega^2 + \omega_2^2)$, which is zero at $\omega = \omega_0$ and $\omega = \omega_2$.

Continuing with the example in Fig. 12.1, we observe that the transmission decreases toward ∞ as s approaches ∞ . Thus the filter must have one or more transmission zeros at $s = \infty$. In general, the number of transmission zeros at $s = \infty$ is the difference between the degree of the numerator polynomial, M , and the degree of the denominator polynomial, N , of the transfer function in Eq. (12.6). This is because as s approaches ∞ , $T(s)$ approaches a_0/s^{N-M} and thus is said to have $N - M$ zeros at $s = \infty$.

For a filter circuit to be stable, all its poles must lie in the left half of the *s* plane, and thus p_1, p_2, \dots, p_{p_2} must all have negative real parts. Figure 12.5 shows typical pole and zero locations for the low-pass filter whose transmission function is depicted in Fig. 12.3. We have assumed that this filter is of fifth order ($N = 5$). It has two pairs of complex conjugate poles and one real-axis pole, for a total of five poles. All the poles lie in the vicinity of the passband, which is what gives the filter its high transmission at passband frequencies. The five transmission zeros are at $s = -j\omega_0$, $s = +j\omega_0$, and $s = \infty$. Thus, the transfer function for this filter is of the form

$$T(s) = \frac{\alpha (s^2 - j\omega_1)(s^2 + \omega_1^2)}{s^5 + b_1 s^4 + b_2 s^3 + b_3 s^2 + b_4 s + b_5} \quad (12.8)$$

¹ Throughout this chapter, we use the names poles and natural modes interchangeably.

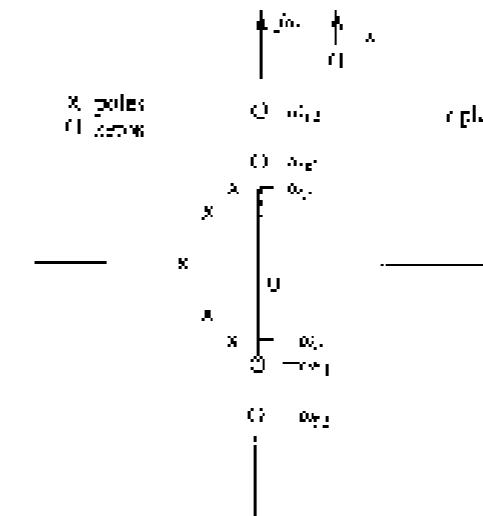


FIGURE 12.5 Pole-zero pattern for the low-pass filter where transmission is shaded. (Fig. 12.3) This is a fifth-order filter ($N = 5$).

As another example, consider the bandpass filter whose magnitude response is shown in Fig. 12.4. This filter has transmission zeros at $s = \pm j\omega_0$ and $s = -j\omega_2$. It also has one or more zeros at $s = 0$ and one or more zeros at $s = \infty$ (because the transmission decreases toward 0 as s approaches 0 and ∞). Assuming that only one zero exists at each of $s = 0$ and $s = \infty$, the filter must be of sixth order, and its transfer function takes the form

$$T(s) = \frac{a_0 s(s^2 - \omega_0^2)(s^2 + \omega_2^2)}{s^6 + b_1 s^5 + b_2 s^4 + b_3 s^3 + b_4 s^2 + b_5 s + b_6} \quad (12.9)$$

A typical pole-zero plot for such a filter is shown in Fig. 12.6.

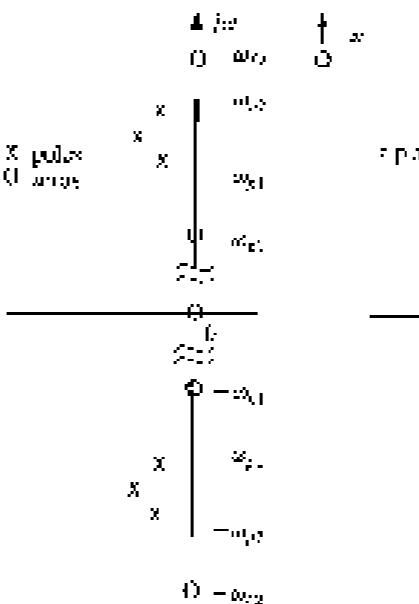


FIGURE 12.6 Pole-zero pattern for the bandpass filter where transmission function is shown in Fig. 12.4. This is a sixth-order filter ($N = 6$).

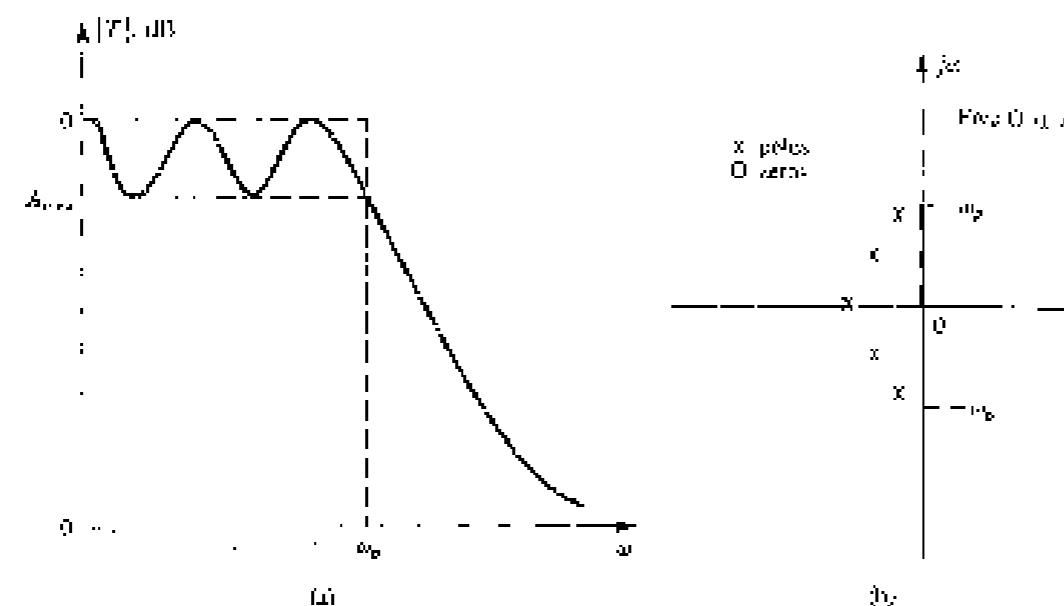


FIGURE 12.7 (a) Transient absorption patterns of three different wavelengths filtered through all transmission zeros of the TV. (b) The zero pattern for the filter in (a).

As a third and final example, consider the low-pass filter whose transmission function is depicted in Fig. 12.71(a). We observe that in this case there are no finite values of ω at which the attenuation is not into infinity (denomination). It is possible that all the transmission zeros of this filter are at $\gamma = \infty$. If this is the case, the filtered transfer function takes the form

$$T(x) = \frac{A_0}{x^k + b_{k+1}x^{k+1} + \dots + b_1}, \quad (12.11)$$

Such a filter is known as an all-pole filter. Typical pole-zero locations for a filter-order 4 all-pole low-pass filter are shown in Fig. 12.7(b).

Nearly all the filters studied in this chapter have all their transmission zeros on the $j\omega$ -axis, in the filter stopband(s), including $\omega = 0$ and $\omega = \infty$. Also, to obtain high selectivity, all the natural poles will be complex conjugate (except for the case of odd-order filters, where one natural pole must lie on the real axis). Finally we note that the more selective the required filter becomes is, the higher its order must be, and the closer its natural angles are to the $j\omega$ -axis.

EXERCISE

- وهو ينبع من مبدأ عدم التسامي بين الأجيال، فالآباء يرثون العادات والتقاليد التي يعيشونها، بينما يولد الأطفال بغيرها، مما ينذر بالخلاف والصراع.

⁴ One might argue that a filter should not have a transmission zero at $\omega = 0$, and, similarly, a high-pass filter should not have a transmission zero at $\omega = \pi$.

124. A cylindrical balloon with zero transverse heat $\phi = 0$, has a radius of 1 m and a height of 2 m. The density of air is 1.225 kg/m^3 . The atmospheric pressure is 101325 Pa . The temperature of the air inside the balloon is 20°C . The density of air at 20°C is 1.166 kg/m^3 . The density of air at 0°C is 1.225 kg/m^3 .

125. Consider the following third-order linear differential equation whose coefficients and initial conditions are given below. It is to be solved by the method of successive approximations. Let the initial conditions be $y(0) = 0$, $y'(0) = 1$, and $y''(0) = 0$.

12.3 BUTTERWORTH AND CHEBYSHEV FILTERS

In this section, we present two functions that are frequently used in approximating the transmission characteristics of low-pass filters. Closed-form expressions are available for the parameters of these functions, and thus one can design a filter without the need for computer or filter-design tables. Their utility, however, is limited to relatively simple applications.

Although in this section we discuss the design of low-pass filters only, the approach and functions presented can be applied to the design of other filter types through the use of frequency transformations (see Saito and Bruckstein (1978)).

12.3.1 The Butterworth Filter

Figure 12.8 shows a sketch of the magnitude response of a Butterworth³ filter. This filter exhibits a monotonically decreasing transmission with all the transmission zeros at $\omega = \infty$, making it an all pole filter. The magnitude function for an N th order Butterworth filter with a passband edge at ω_0 is given by

$$|T(\omega)| = \frac{1}{\sqrt{1 + \epsilon_1^2(\omega)^2}} \quad (12.11)$$

$$(\mathcal{D}(j\alpha_j)) = \frac{1}{\sqrt{1-\zeta^2}} \quad (1.2.12)$$

Thus, the parameter ϵ determines the exactitude criterion in pairwise transmission. A low enough ϵ guarantees

$$A_{\text{rec}} = 20 \log_{10} \sqrt{1 + \epsilon} \quad (12.1.3)$$

Conversely, given A_{opt} , the value of ϵ can be determined from

$$t = \sqrt{10^{A_0} e^{-B_0}} - 1 \quad (12.14)$$

Observe that in the Butterworth response the maximum deviation is guaranteed transmission (from the ideal value of unity) occurs at the passband edge only. It can be shown that the first

²The Butterworth-Gauß approximation is named after S. Butterworth, a British engineer who in 1930 was among the first to employ it.

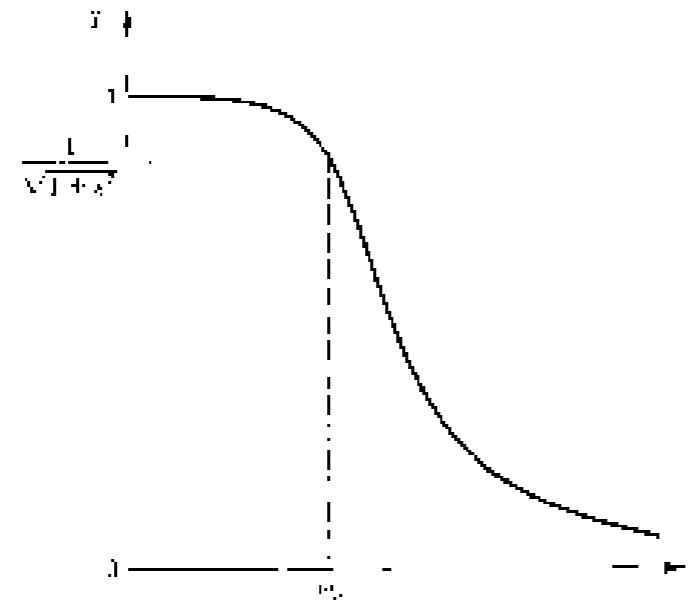
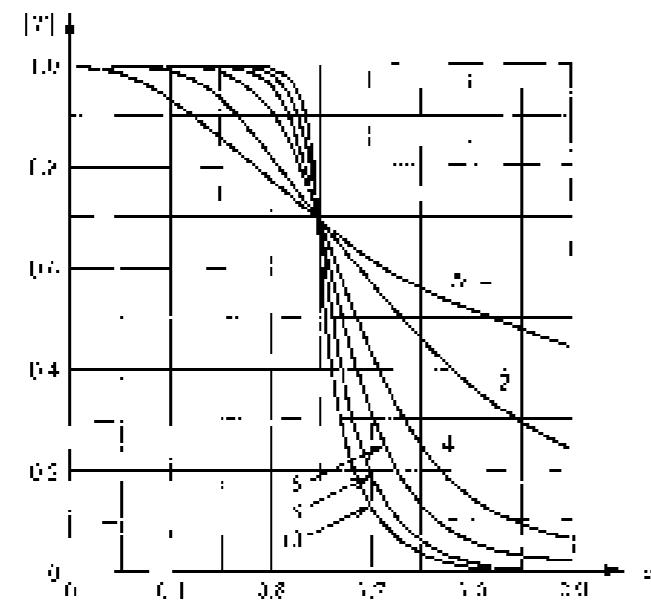


FIGURE 12.8 The magnitude response of a Butterworth filter.

$2N-1$ successive zeros of $|H|$ relative to $\omega = \omega_0$ are zero at $\omega = 0$ [see Van Valkenburg (1980)]. This property makes the Butterworth response very flat near $\omega = 0$ and gives the response the steepest maximally flat response. The degree of passband flatness increases \propto the order $N^{1/2}$ (increasing, as can be seen from Fig. 12.9). This figure indicates also that, as should be expected, as the order N is increased the filter response approaches the ideal brick-wall type of response.

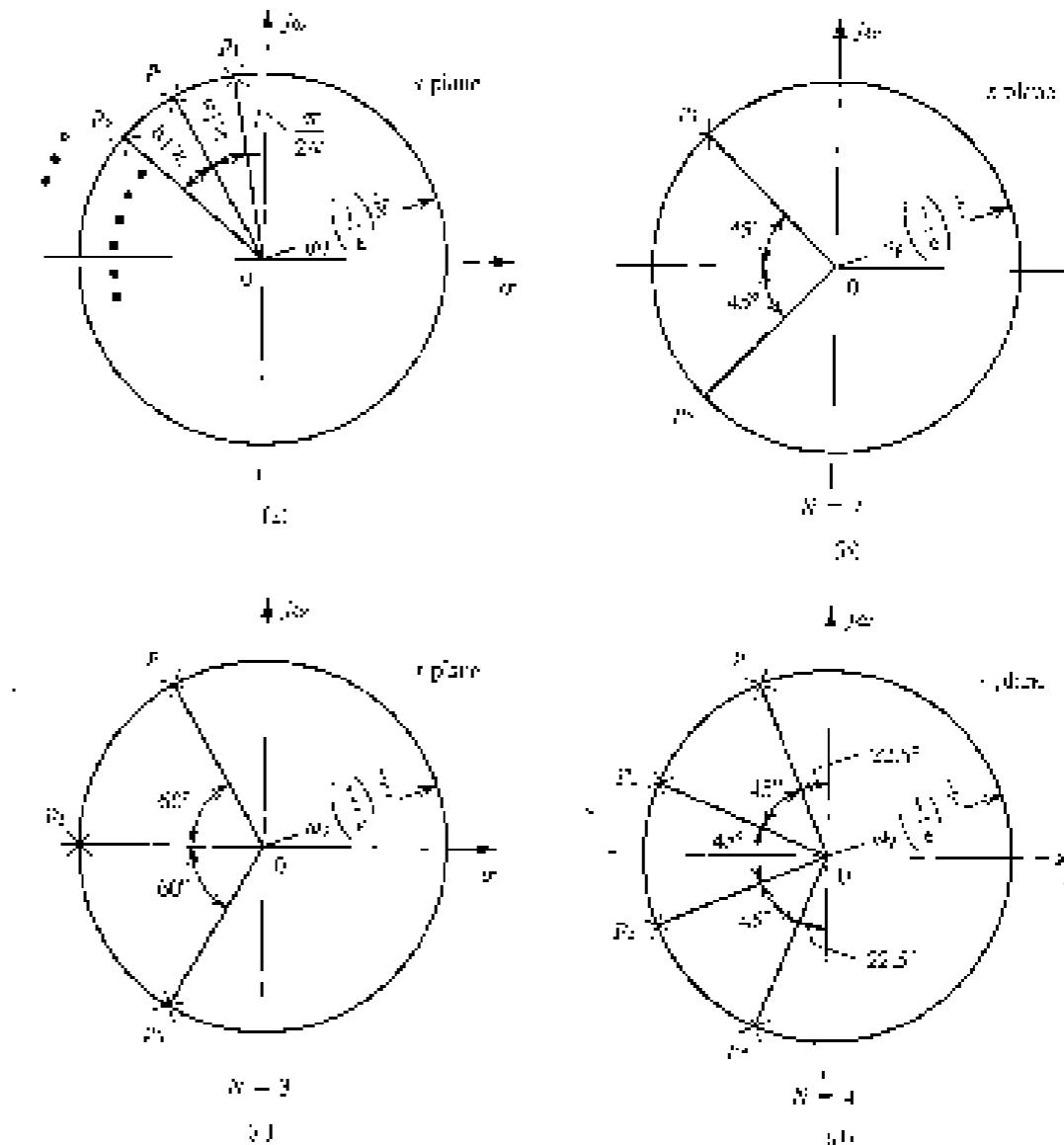
FIGURE 12.9 Magnitude response for Butterworth filters of various orders with $\epsilon = 1.0$ (as the order increases, the response approaches the ideal brick-wall type of transmission).

At the edge of the stopband, $\omega \approx \omega_0$, the attenuation of the Butterworth filter is given by

$$\begin{aligned} A(\omega_0) &= -20 \log \left[\left(\sqrt{\epsilon} + \sqrt{\epsilon^2 + (\omega_0/\omega_0)^{2N}} \right)^{2N} \right] \\ &= -N \log \left[1 + \epsilon^2 (\omega_0/\omega_0)^{2N} \right]. \end{aligned} \quad (12.15)$$

This equation can be used to determine the filter order required, which is the lowest integer value of N that yields $A(\omega_0) \geq A_{\text{att}}$.

The natural poles of an N th-order Butterworth filter can be determined from the graphical construction shown in Fig. 12.10(a). Observe that the natural poles lie on a circle of

FIGURE 12.10 Graphical construction for determining the poles of a Butterworth filter of order N . All the poles lie in the left half of the complex s -plane (unless $\omega_0 = \omega_0^* \text{e}^{j\pi/4}$, where ω_0^* is the weak-pole location parameter, i.e., $\omega_0^* (1 + \epsilon^{1/(2N)})^{1/2}$). (a) General case; (b) $N = 3$; (c) $N = 2$; and (d) $N = 1$.

radius $\omega_0/(\epsilon e^{jN\pi})$ and are spaced by equal angles of π/N , with the last node at an angle $\pi/2N$ from the σ -axis. Since the natural modes all have equal radial distance from the origin they all have the same frequency $\omega_0 = \omega_p \sqrt{1-\epsilon^2}$. Figure 12.10(b), (c), and (d) shows the natural modes of Butterworth filters of order $N = 2, 3$, and 4 , respectively. Once the N natural modes p_1, p_2, \dots, p_N have been found, the transfer function can be written as

$$T(s) = \frac{K \omega_0^N}{(s-p_1)(s-p_2) \cdots (s-p_N)} \quad (12.16)$$

where K is a constant equal to the required dc gain of the filter.

To summarize, for a Butterworth transfer function that meets transmission specification (b) of the form in Fig. 12.3 we perform the following procedure:

1. Determine ϵ from Eq. (12.15)
2. Use Eq. (12.15) to determine the required filter order as the lowest integer value of N that results in $A(\omega_p) \geq A_{\text{des}}$.
3. Use Fig. 12.9(a) to determine the N natural modes.
4. Use Eq. (12.16) to determine $T(s)$.

PROBLEMS

Find the Butterworth transfer function that meets the following low-pass filter specifications: $f_p = 10 \text{ kHz}$, $A_{\text{des}} = 13 \text{ dB}$, $f_s = 15 \text{ kHz}$, $A_{\text{stop}} = 20 \text{ dB}$, dc gain = 1.

Solution

Substituting $A_{\text{des}} = -13 \text{ dB}$ into Eq. (12.11) yields $\epsilon = 0.9063$. Equation (12.15) is then used to determine the filter order by trying various values for N . We find that $N = 8$ yields $A(\omega_p) = 22.5 \text{ dB}$ and $N = 9$ gives 25.6 dB. We thus select $N = 9$.

Figure 12.11 shows the graphical construction for determining the poles. The poles all have the same frequency $\omega_0 = \omega_p \sqrt{1-\epsilon^2} = 2\pi \times 10 \times 10^3 \sqrt{1-0.9063^2} = 6.774 \times 10^3 \text{ rad/s}$. The first pole p_1 is given by

$$p_1 = \omega_0(-\cos 80^\circ + j \sin 80^\circ) = \omega_0(-0.1736 + j 0.9848)$$

Combining p_1 with its complex conjugate p_9 yields the factor $(s^2 + s0.3472\omega_0 + \omega_0^2)$ in the denominator of the transfer function. The same can be done for the other complex poles, and the complete transfer function is obtained using Eq. (12.16).

$$\begin{aligned} T(s) &= \frac{\omega_0^9}{(s+\omega_0)(s^2+s0.3472\omega_0+\omega_0^2)(s^2+s0.6948\omega_0+\omega_0^2)} \\ &\times \frac{1}{(s^2+s0.1736\omega_0+\omega_0^2)(s^2+s0.3472\omega_0+\omega_0^2)} \end{aligned} \quad (12.17)$$

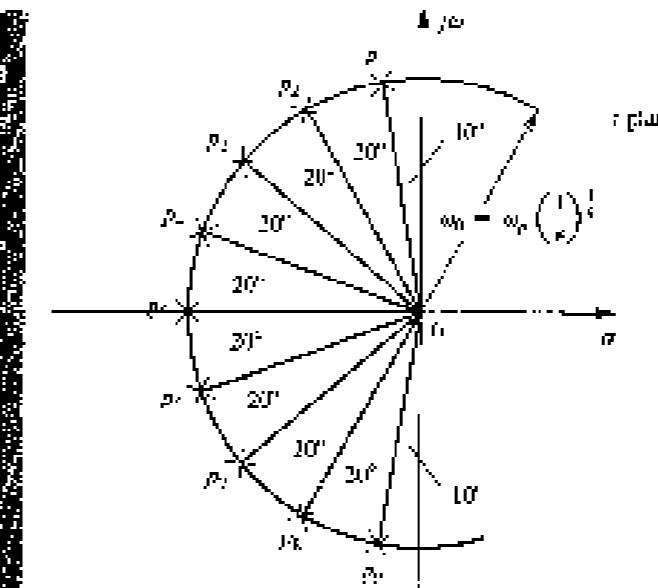


FIGURE 12.11 Poles of the ninth-order Butterworth filter of Example 12.2.

12.3.2 The Chebyshev Filter

Figure 12.12 shows representative transmission functions for Chebyshev⁴ filters of even and odd order. The Chebyshev filter exhibits no equiripple response in the passband and a monotonically decreasing transmission in the stopband. While the odd-order filter has $|T(s)| = 1$, the even-order filter exhibits its maximum magnitude deviation at $\omega = 0$. In both cases the total number of passband ripples and cut-offs equals the order of the filter, N . All the transmission zeros of the Chebyshev filter are at $\omega = \infty$, making it an all-pole filter.

The magnitude of the transfer function of an N th-order Chebyshev filter with a passband edge (triple bandwidth) ω_c is given by

$$|T(j\omega)| = \frac{1}{\sqrt{1 + \epsilon^2 \cos^2(N \cot^{-1}(\omega/\omega_c))}} \quad \text{for } \omega \leq \omega_c \quad (12.18)$$

and

$$|T(j\omega)| = \frac{1}{\sqrt{1 + \epsilon^2 \cos^2(N \cot^{-1}(\omega/\omega_c))}} \quad \text{for } \omega \geq \omega_c \quad (12.19)$$

At the passband edge, $\omega = \omega_c$, the magnitude function is given by

$$|T(j\omega_c)| = \frac{1}{\sqrt{1 + \epsilon^2}}$$

⁴ Named after the Russian mathematician P. L. Chebyshev, who in 1859 used these functions in studying the construction of steam engines.

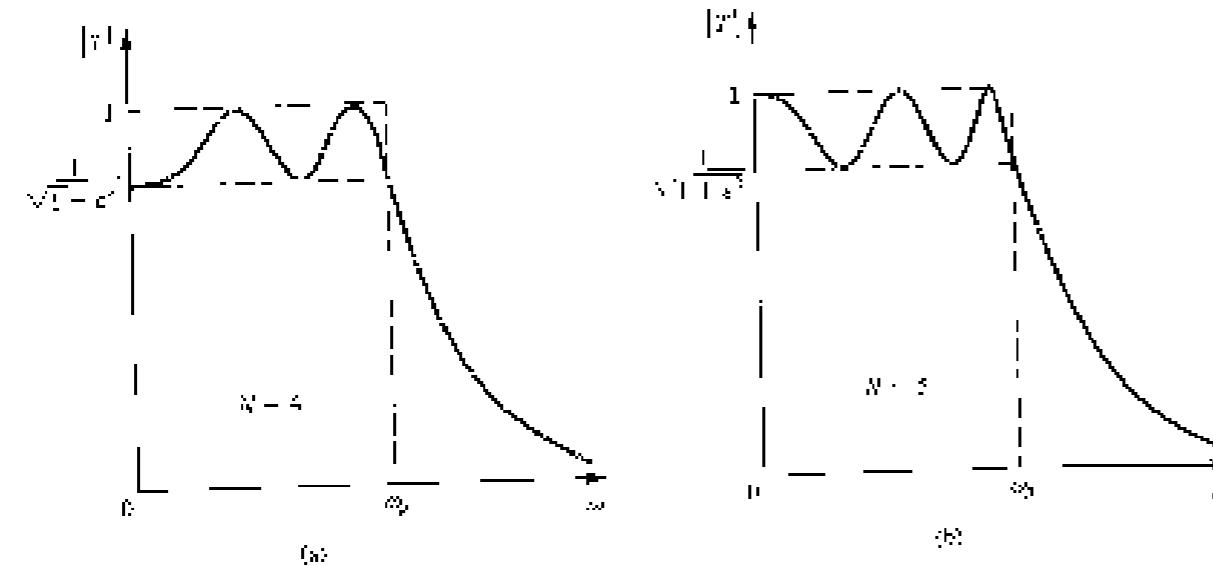


FIGURE 12.12 Sketches of the transmission characteristics of nonminimum phase (a) Butterworth; (b) odd-order Chebyshev filters.

thus, the parameter ϵ determines the passbandripple according to

$$A_{\text{err}} = 10 \log (1 + \epsilon^2) \quad (12.20)$$

Conversely, given A_{err} , the value of ϵ is determined from

$$\epsilon = \sqrt{10^{A_{\text{err}}/10} - 1} \quad (12.21)$$

The attenuation achieved by the Chebyshev filter at the stopband edge ($\omega = \omega_s$) is found using Eq. (12.19) as

$$A(\omega_s) = 10 \log [1 + \epsilon^2 \cosh^2(N \operatorname{asinh}^{-1}(\omega_s/\omega_c))] \quad (12.22)$$

With the aid of a calculator this equation can be used to determine the order N required to obtain a specified A_{err} by finding the lowest integer value of N that yields $A(\omega_s) \geq A_{\text{err}}$. As in the case of the Butterworth filter, increasing the order N of the Chebyshev filter causes it to magnify the function to approach the ideal brick-wall low-pass response.

The poles of the Chebyshev filter are given by

$$\begin{aligned} p_k &= \omega_c \exp \left[j \frac{2k-1}{N} \pi \sinh^{-1} \left(\frac{1}{\epsilon} \sinh^{-1} \frac{1}{\epsilon} \right) \right] \\ &\quad + j \omega_c \cos \left[\frac{2k-1}{N} \pi \cosh^{-1} \left(\frac{1}{\epsilon} \sinh^{-1} \frac{1}{\epsilon} \right) \right] \quad k = 1, 2, \dots, N \end{aligned} \quad (12.23)$$

Finally, the transfer function of the Chebyshev filter can be written as

$$T(\omega) = \frac{K \omega_c^N}{\omega_c^N (\omega - p_1)(\omega - p_2) \cdots (\omega - p_N)} \quad (12.24)$$

where K is the dc gain that the filter is required to have.

To summarize, given low-pass transmission specifications of the type shown in Fig. 12.3, the transfer function of a Chebyshev filter that meets these specifications can be found as follows:

1. Determine ϵ from Eq. (12.21).
2. Use Eq. (12.22) to determine the order required.
3. Determine the poles using Eq. (12.23).
4. Determine the transfer function using Eq. (12.24).

The Chebyshev filter provides a more efficient approximation than the Butterworth filter. Thus, for the same order and the same A_{err} , the Chebyshev filter provides greater stopband attenuation than the Butterworth filter. Alternatively, to meet identical specifications, one requires a lower order for the Chebyshev than for the Butterworth filter. This point will be illustrated by the following example.

Example 12.1

Find the Chebyshev transfer function that meets the same low-pass filter specifications given in Example 12.1; namely, $\omega_c = 10 \text{ kHz}$, $A_{\text{err}} = 1 \text{ dB}$, $\omega_s = 5 \text{ kHz}$, $A_{\text{stop}} = 20 \text{ dB}$, $\omega_c/\omega_s = 1$.

Solution

Substituting $A_{\text{err}} = 1 \text{ dB}$ into Eq. (12.21) yields $\epsilon = 0.0985$. By trying various values for N in Eq. (12.22) we find that $N = 4$ yields $A(\omega_s) = 21.0 \text{ dB}$ and $N = 5$ provides 29.9 dB . We thus select $N = 5$ since that we require a smaller-order Butterworth filter to meet the same specifications as Example 12.1.

The poles are obtained by substituting ϵ in Eq. (12.23) as

$$\begin{aligned} p_1, p_2 &= \omega_c i (-0.2895 \pm j 0.9851) \\ p_3, p_4 &= \omega_c i (-0.2342 \pm j 0.6119) \\ p_5 &= \omega_c i (-0.2895) \end{aligned}$$

The transfer function is obtained by substituting these values in Eq. (12.24) as

$$\begin{aligned} T(\omega) &= \frac{\omega_c^5}{8.2348(\omega - 0.2895 \omega_c)(\omega^2 - 0.2342 \omega_c + 0.4297 \omega_c^2)} \\ &\quad \times \frac{1}{\omega^2 + 20.1789 \omega_c - 0.9851 \omega_c^2} \end{aligned} \quad (12.25)$$

where $\omega_c = 2\pi \times 10^4 \text{ rad/s}$.

EXERCISES

- 12.6.1 Recalling that the Butterworth filter has a flat passband ($A(\omega) = 0$), determine the order required to obtain a 10-dB stopband attenuation for a Butterworth filter with a corner frequency of $\omega_c = 10 \text{ rad/s}$.
- 12.6.2 What is the corner value of the minimum phase Butterworth filter?
- 12.6.3 At what corner frequency is the magnitude of the Butterworth filter given by Eq. (12.18) unity?
- 12.6.4 If the $\omega_c = 47.3 \text{ rad/s}$ and $A_{\text{err}} = 0.1 \text{ dB}$, determine the order required for a Butterworth filter.

- (12.5) Find the desired poles and the ω_n for the realization of a Butterworth filter with $\omega_n = 1$, $\omega_c = 1$, and $\phi = 0^\circ$.
 Ans. $\omega_1 = \pm j\sqrt{2}/2$ and $\omega_2 = j(1/\sqrt{2} + 1)/(j + 1)$.
- (12.6) Observe that Eq. (12.19) is obtained by finding the ω -regions in the passband or the stopband regions and using voltage dividers parallel to the resistors in the $\cos^2(\frac{\pi}{2}\omega)$ term to calculate the frequency response of the filter. Implement this technique for the frequency response of a Butterworth filter.
 Ans. $\omega_1 = \pm j\sqrt{2}/2$ and $\omega_2 = j(1/\sqrt{2} + 1)/(j + 1)$.
- (12.7) Find the all-pass function $A(s) = 1/s$ for a Chebyshev filter with $N = 1$ and $\omega_c = 1$.
 Ans. $A(s) = (s - j)/s + j$.
- (12.8) Find the all-pass function $A(s) = 1/s$ for a Chebyshev filter with $N = 2$ and $\omega_c = 1$.
 Ans. $A(s) = (s - j)/s + j$.
- (12.9) Find the all-pass function $A(s) = 1/s$ for a Chebyshev filter with $N = 3$ and $\omega_c = 1$.
 Ans. $A(s) = (s - j)/s + j$.
- (12.10) Find the all-pass function $A(s) = 1/s$ for a Chebyshev filter with $N = 4$ and $\omega_c = 1$.
 Ans. $A(s) = (s - j)/s + j$.

12.4 FIRST-ORDER AND SECOND-ORDER FILTER FUNCTIONS

In this section, we shall study the simplest filter transfer functions, those of first and second order. These functions are useful in their own right in the design of simple filters. First- and second-order filters can also be cascaded to realize a high-order filter. Cascade design is in fact one of the most popular methods for the design of active filters (those utilizing op amps and RC circuits). Because the filter poles occur in complex-conjugate pairs, a high-order transfer function $T(s)$ is factored into the product of second-order functions. If $T(s)$ is real, there will also be a first-order function in the factorization. Each of the second-order functions yield the first-order function when $T(s)$ is real, is then realized using one of the op-amp-RC circuits that will be studied in this chapter, and the resulting blocks are placed in cascade. If the output of each block is taken at the output terminal of an op-amp where the impedance level is low (ideally zero), cascading does not change the transfer functions of the individual blocks. Thus the overall transfer function of the cascade is simply the product of the transfer functions of the individual blocks, which is the original $T(s)$.

12.4.1 First-Order Filters

The general first-order transfer function is given by

$$T(s) = \frac{a_1 s + a_0}{s + a_1} \quad (12.26)$$

This bilinear transfer function characterizes a first-order filter with a natural mode at $s = -a_1$, a transmission zero at $s = -a_0/a_1$, and a high-frequency gain that approaches a_1 . The numerator coefficients, a_0 and a_1 , determine the type of filter (e.g., low pass, high pass, etc.). Some special cases together with passive (RC) and active (op-amp-RC) realizations are shown in Fig. 12.13. Note that the active realizations provide considerably more versatility than their passive counterparts; in many cases the gain can be set to a desired value, and some transfer function parameters can be adjusted without affecting others. The input impedance of the active circuit is also very low, making cascading easily possible. The op-amp, however, limits the high-frequency operation of the active circuits.

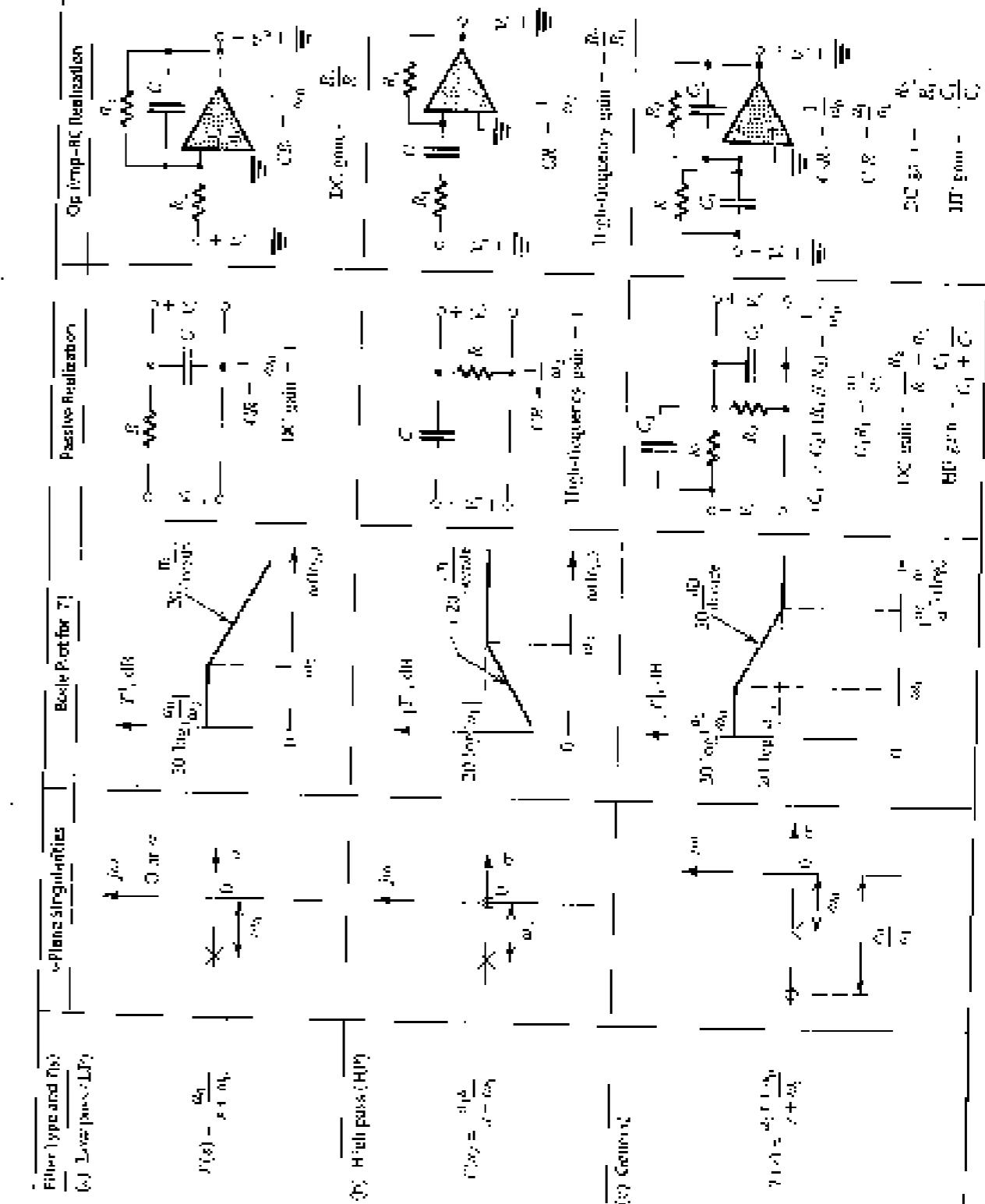


FIGURE 12.13 Five-order filters.

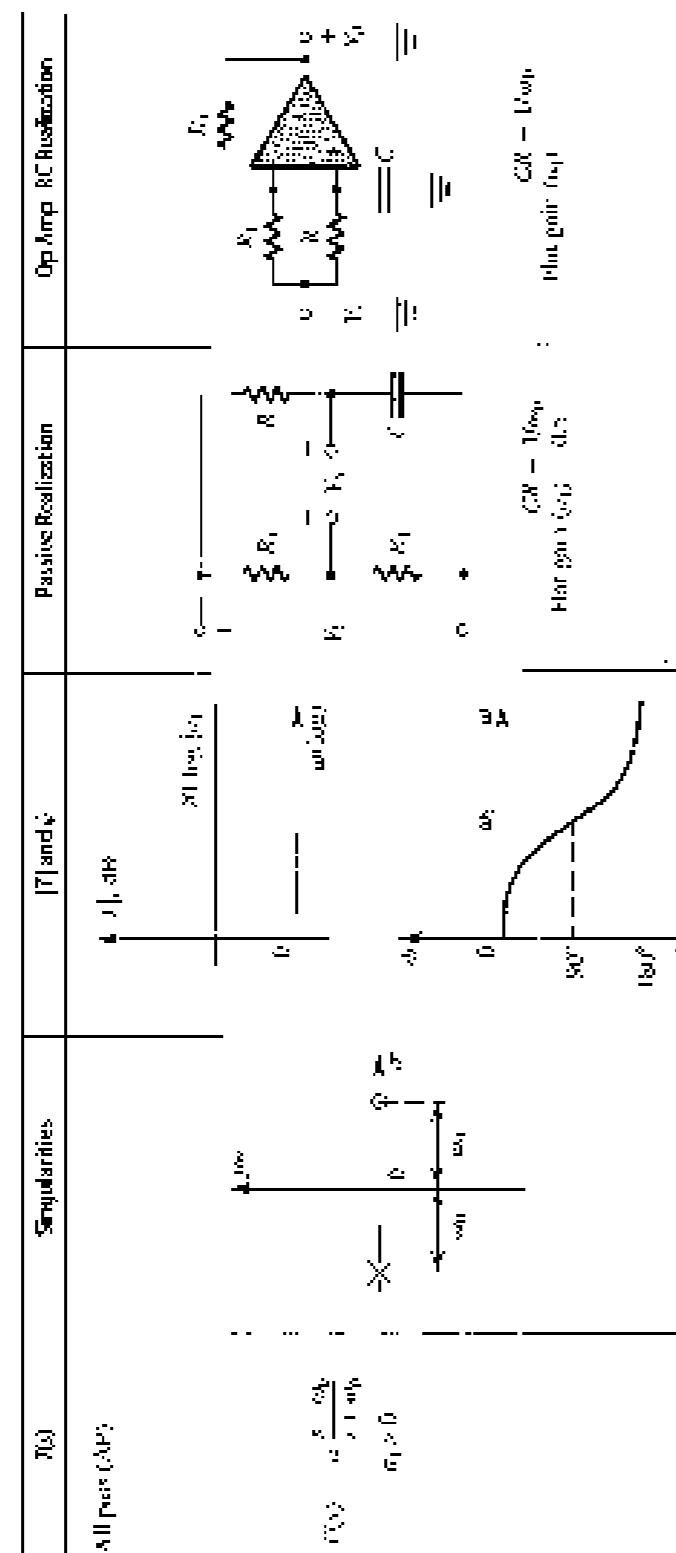


FIGURE 12.14: First-order all-pass filter.

An important special case of the first-order filter function is the all-pass filter shown in Fig. 12.14. Here, the transmission zero and the natural mode are symmetrically located relative to the $j\omega$ axis. (They are said to display mirror-image symmetry with respect to the $j\omega$ axis.) Observe that although the transmission of the all-pass filter is (ideally) constant at all frequencies, its phase shows frequency sensitivity. All-pass filters are used as phase shifters and in systems that require phase shaping (e.g., in the design of circuits called delay equalizers, which cause the overall time delay of a transmission system to be constant with frequency).

EXERCISES

- 12.11 Using the s -plane realization of the RC filter in Fig. 12.10, determine the transmission function $T(s)$ for the following frequencies:
 a) $\omega = 100 \text{ rad/s}$
 b) $\omega = 1000 \text{ rad/s}$
- 12.12 Design the circuit in Fig. 12.14 to realize a first-order filter with a 90° phase shift at 10 rad/s. Select suitable component values.
- Ans. Possible choices: $R_1 = 50 \Omega$; $R_2 = 10 \text{ k}\Omega$; $C = 0.1 \mu\text{F}$.

12.4.2 Second-Order Filter Functions

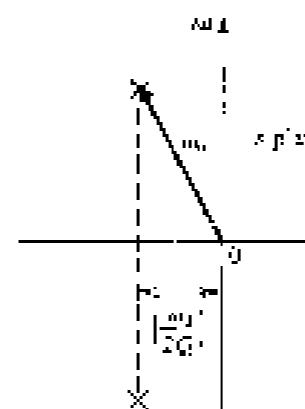
The general second-order (or biquadratic) filter transfer function is usually expressed in the standard form

$$T(s) = \frac{\omega_0 s^2 - 2\zeta s + \omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}, \quad (12.27)$$

where ω_0 and ζ determine the natural modes (poles) according to

$$\omega_1, \omega_2 = \pm \frac{\omega_0}{2\zeta} \pm j\sqrt{\omega_0^2 - (1/4\zeta^2)\omega_0^2}. \quad (12.28)$$

We are usually interested in the case of non-alias-conjugate natural modes, obtained for $\zeta > 0.5$. Figure 12.15 shows the location of the pair of complex-conjugate poles in the s -plane. Observe that the radial distance of the natural modes (from the origin) is equal to ω_0 , which is known

FIGURE 12.15: Definition of the parameters ω_0 , ζ , and α_0 in the complex-s plane.

as the pole frequency. The parameter Q determines the distance of the poles from the $j\omega$ axis; the higher the value of Q , the closer the poles are to the $j\omega$ axis, and the more selective the filter response becomes. An infinite value for Q locates the poles on the $j\omega$ axis and can yield sustained oscillations in the circuit realization. A negative value of Q implies that the poles are in the right half of the s plane, which certainly produces oscillations. The parameter Q is called the pole quality factor, or simply, pole Q .

The transmission zeros of the second-order filters are determined by the numerator coefficients a_0 , a_1 , and a_2 . It follows that the numerator coefficients determine the type of second-order filter function (e.g., LP, HP, BP). Seven special cases of interest are illustrated in Fig. 12.16. For each case we give the transfer function, the s -plane locations of the transfer-function singularities, and the magnitude response. Circuit realizations for the various second-order filter functions will be given in subsequent sections.

All seven special second-order filters have a pair of complex-conjugate natural modes characterized by a frequency ω_0 and a quality factor, Q .

In the low-pass (LP) case, shown in Fig. 12.16(a), the two transmission zeros are at $s = \infty$. The magnitude response can exhibit a peak with the details indicated. It can be shown that the peak occurs only for $Q > 1/\sqrt{2}$. The response obtained for $Q = 1/\sqrt{2}$ is the Butterworth, or maximally flat, response.

The high-pass (HP) function shown in Fig. 12.16(b) has one transmission zero at $s = 0$ (dc). The magnitude response shows a peak for $Q \geq 1/\sqrt{2}$, with the details of the response as indicated. Observe the duality between the LP and HP responses.

Next consider the bandpass (BP) filter function shown in Fig. 12.16(c). Here, one transmission zero is at $s = 0$ (dc), and the other is at $s = \infty$. The magnitude response peaks at $\omega = \omega_0$. Thus the center frequency of the bandpass filter is equal to the pole frequency ω_0 . The selectivity of the second-order bandpass filter is usually measured by its 3-dB bandwidth, that is, the difference between the two frequencies ω_1 and ω_2 at which the magnitude response is $3\sqrt{2}$ below its maximum value (at ω_0). It can be shown that

$$\omega_2/\omega_1 = \omega_0\sqrt{1 + (1/4Q^2)} \pm \frac{\omega_0}{2Q} \quad (12.29)$$

Thus,

$$BW = \omega_2 - \omega_1 = \omega_0/Q \quad (12.30)$$

Observe that as Q increases, the bandwidth decreases and the bandpass filter becomes more selective.

If the transmission zeros are located on the $j\omega$ axis, at the complex-conjugate locations $\pm j\omega_0$, then the magnitude response exhibits zero transmission at $\omega = \omega_0$. Thus a notch in the magnitude response occurs at $\omega = \omega_0$, and ω_0 is known as the notch frequency. These cases of the second-order notch filter are passible: the regular notch, obtained when $a_1 < a_0$ (Fig. 12.16(d); the low-pass notch, obtained when $a_0 > a_1$ (Fig. 12.16(e)); and the high-pass notch, obtained when $a_1 < a_0$ (Fig. 12.16(f)). The reader is urged to verify the response details given in these figures (a rather tedious task, though!). Observe that in all notch cases, the transmission at dc and at $s = \infty$ is finite. This is so because there are no transmission zeros at either $s = 0$ or $s = \infty$.

The last special case of interest is the all-pass (AP) filter whose characteristics are illustrated in Fig. 12.16(g). Here the two transmission zeros are in the right half of the s plane, as the right-half-plane locations of the poles. (This is the case for all pass functions of any order.) The magnitude response of the all-pass function is constant over all frequencies; the flat gain, as it is called, is in our case equal to $|a_1|$. The frequency selectivity of the all-pass function is in its phase response.

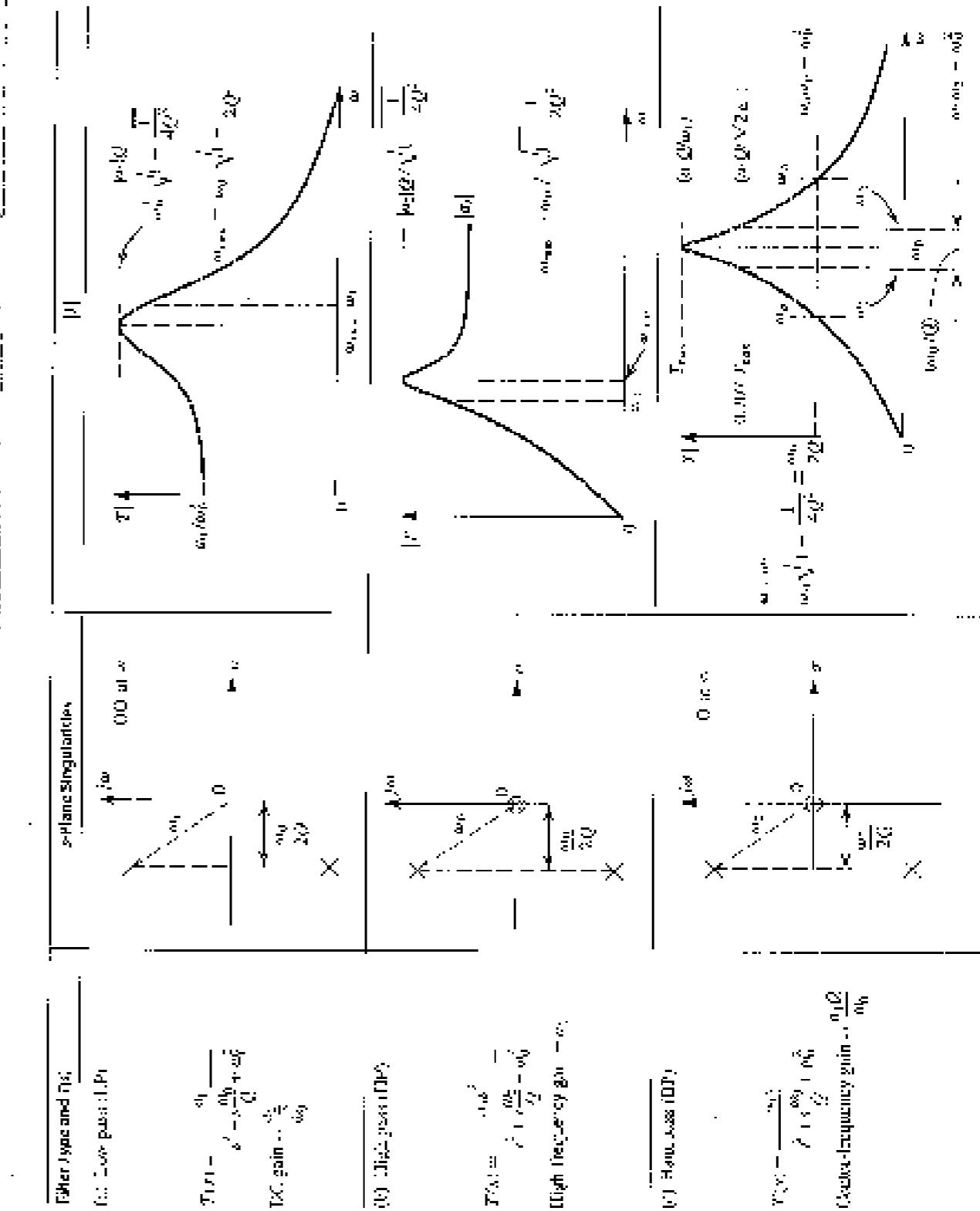


FIGURE 12.16 Second-order filter s -functions.

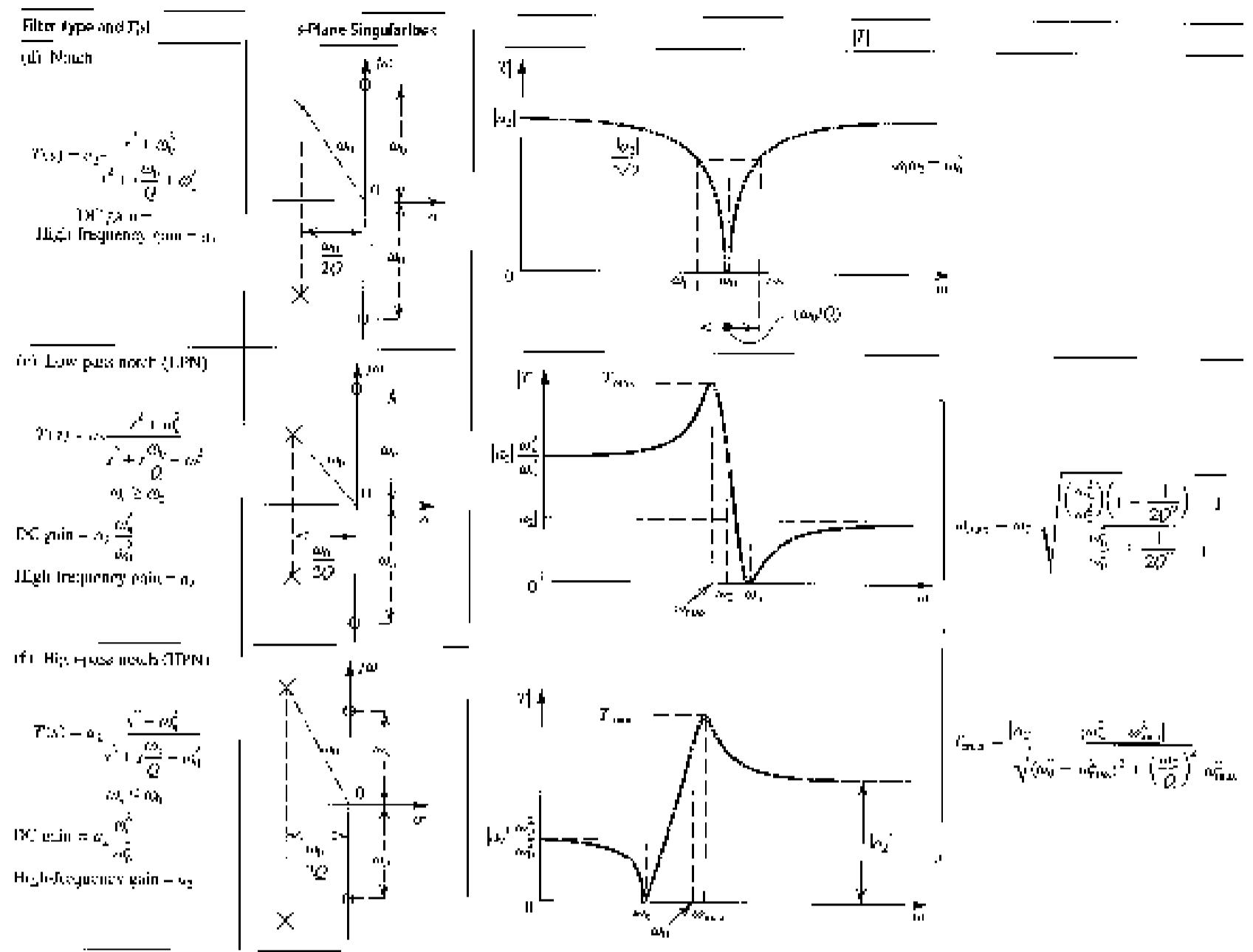


FIGURE 12.7b (Continued)

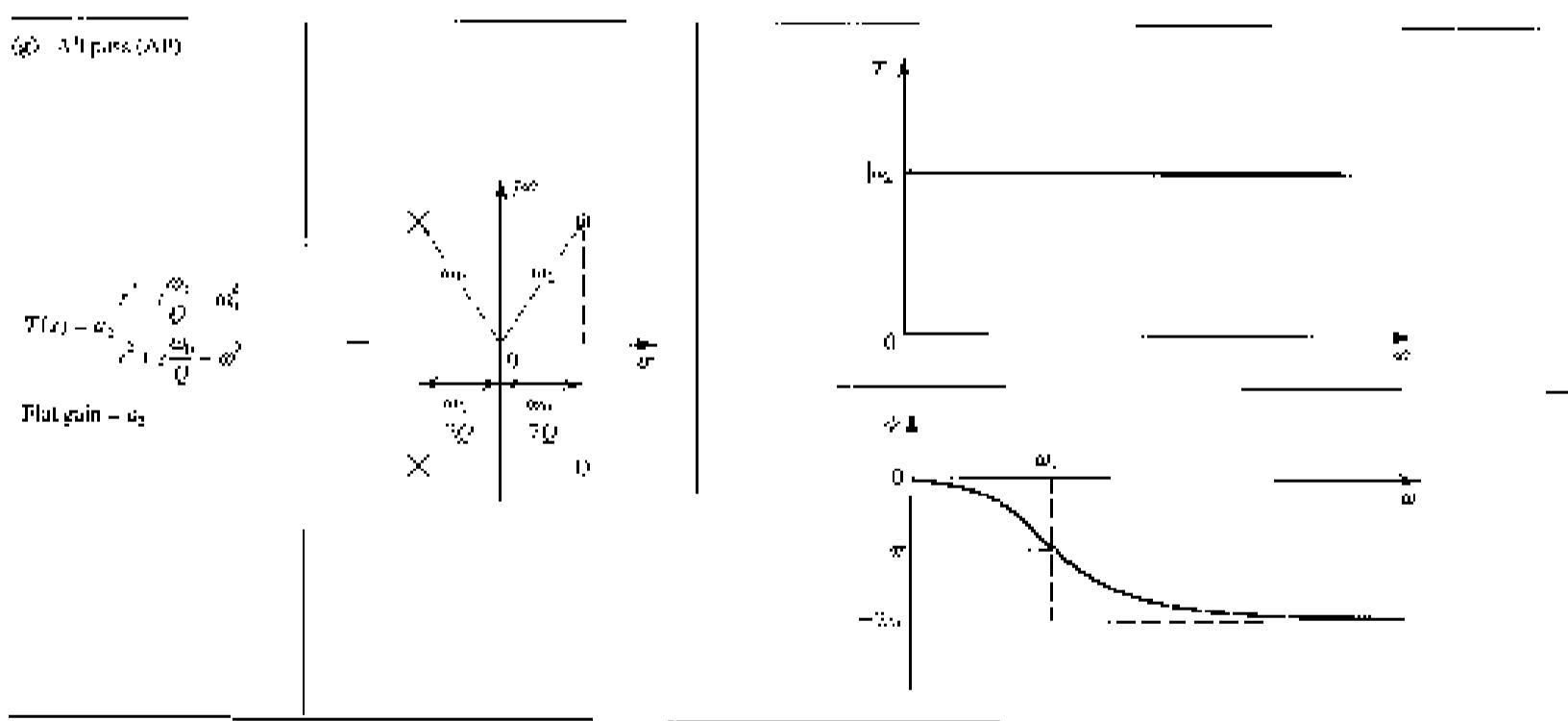


FIGURE 12.16 (Continued)

EXERCISES

- 12.13 For a maximally flat-pass filter with $\text{BW} = 1/\sqrt{2}$, show that $\omega_0 = \omega_c$. Use the results of Exercise 12.12 for the solution.
- 12.14 Given the transfer function of a second-order bandpass filter with a corner frequency of 10^3 rad/s, determine the transfer function of a second-order bandpass filter with a corner frequency of 10^4 rad/s having a center-frequency ratio of 10 (and ω_c unchanged).

ANSWER

- 12.15 At $\omega = 10^3$ rad/s, the corner frequencies are $\omega_0 = 10^3$ rad/s and $\omega_c = 10^4$ rad/s. The transfer function is given by

$$\frac{V_o}{V_i} = \frac{10^4}{10^3 + s^2}$$

- (a) Show that any frequencies, ω_0 and ω_c , at which $|T|$ is the same, are related by $\omega_0\omega_c = \omega_b^2$.

- 12.16 Consider a low-pass network with $\omega_0 = 10^3$ rad/s, $Q = 10$, $\omega_c = 10^4$ rad/s, and $\omega_b = 10^5$ rad/s. Find the frequency and magnitude of the transmission peak. Also find the 3dB -width of the passband (in rad/s).

12.5 THE SECOND-ORDER LCR RESONATOR

In this section we shall study the second-order LCR resonator shown in Fig. 12.17(a). The use of this resonator to derive circuit realizations for the various second-order filter functions will be demonstrated. It will be shown in the next section that replacing the inductor L by a simulated inductance obtained using an op-amp RC resonator, the latter forms the basis of an important class of active-RC filters to be studied in Section 12.6.

12.5.1 The Resonator Natural Modes

The natural modes of the parallel resonance circuit of Fig. 12.17(a) can be determined by applying an excitation that does not change the natural structure of the circuit. Two possible ways of exciting the circuit are shown in Fig. 12.17(b) and (c). In Fig. 12.17(b) the resonator

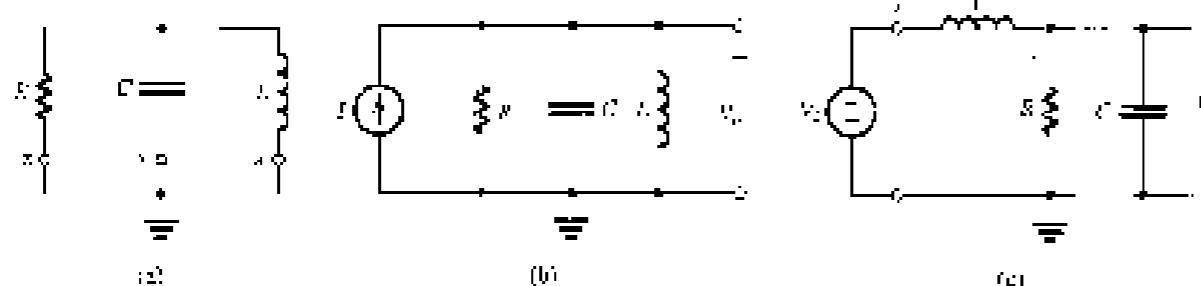


FIGURE 12.17 (a) The second-order parallel LCR resonator. (b) Two ways of exciting the resonator of (a). (c) Its natural resonator poles are those poles of V_o/V_i and V_i/V_o .

is excited with a current source I_s connected in parallel. Since, as far as the natural response of the circuit is concerned, an independent ideal current source is equivalent to an open circuit, the excitation of Fig. 12.17(b) does not alter the natural structure of the resonator. Thus the circuit in Fig. 12.17(b) can be used to determine the natural modes of the resonator by simply finding the poles of any response function. We can for instance take the voltage V_o across the resonator as the response and thus obtain the response function $V_o/V_i = Z$, where Z is the impedance of the parallel resonance circuit. It is obviously more convenient, however, to work in terms of the admittance B ; thus,

$$\begin{aligned} \frac{V_o}{I} &= \frac{1}{Z} = \frac{1}{(1/sL) + sC + (1/R)} \\ &= \frac{s/C}{s^2 + s(C/R) + (1/LC)} \end{aligned} \quad (12.31)$$

Equating the denominator to the standard form $s^2 + 2\omega/Q + \omega_0^2$ we have

$$\omega_0^2 = 1/LC \quad (12.32)$$

and

$$\omega_b/Q = 1/CR \quad (12.33)$$

Thus,

$$\omega_b = 1/\sqrt{LC} \quad (12.34)$$

$$Q = \omega_b CR \quad (12.35)$$

These expressions should be familiar to the reader from studies of parallel resonance circuits in introductory courses on circuit theory.

An alternative way of exciting the parallel LCR resonator for the purpose of determining its natural modes is shown in Fig. 12.17(c). Here, node a of inductor L has been disconnected from ground and connected to an ideal voltage source V_s . Now, since as far as the natural response of the circuit is concerned, an ideal independent voltage source is equivalent to a short circuit, the excitation of Fig. 12.17(c) does not alter the natural structure of the resonator. Thus we can use the circuit in Fig. 12.17(c) to determine the natural modes of the resonator. These are the poles of any response function. For instance, we can select V_o as the response variable and find the transfer function V_o/V_i . The reader can easily verify that this will lead to the natural modes determined earlier.

In a design problem, we will be given ω_0 , but Q and will be asked to determine L , C , and R . Equations (12.34) and (12.35) are two equations in the three unknowns. The one available degree-of-freedom can be utilized to set the impedance level of the circuit to a value that results in practical component values.

12.5.2 Realization of Transmission Zeros

Having selected the component values of the LCR resonator to realize a given pair of complex-conjugate natural modes, we now consider the use of the resonator to realize a desired filter type (e.g., LP, HP, etc.). Specifically, we wish to find out where to inject the input voltage signal V_i so that the transfer function V_o/V_i is the desired one. Toward that end, note that in the resonator circuit in Fig. 12.17(a), any of the nodes labeled x , y , or z can be disconnected.

from ground and connected to V_2 without affecting the circuit's natural modes. When it is so done the circuit takes the form of a voltage divider, as shown in Fig. 12.18(a). Thus the transfer function realized is

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}. \quad (12.36)$$

We observe that the transmission zeros are the values of s at which $Z_1(s) = 0$, provided $Z_2(s)$ is not simultaneously zero, and the values of s at which $Z_2(s) = 0$, provided $Z_1(s)$ is not simultaneously infinite. This statement makes physical sense. The output will be zero either when $Z_2(s)$ behaves as a short circuit or when $Z_1(s)$ behaves as an open circuit. If there is a value of s at which both Z_1 and Z_2 are zero, then V_o/V_i will be finite and no transmission zero is obtained. Similarly, if there is a value of s at which both Z_1 and Z_2 are infinite, then V_o/V_i will be finite and no transmission zero is realized.

12.5.3 Realization of the Low-Pass Function

Using the scheme just outlined we see that to realize a low-pass function, node x is disconnected from ground and connected to V_2 , as shown in Fig. 12.18(c). The transmission zeros of this circuit will be at the value of s for which the series impedance becomes infinite (sL becomes infinite at $s = \infty$) and the value of s at which the shunt impedance becomes zero [$(1/sC + 1/R)$ becomes zero at $s = \infty$]. Thus this circuit has two transmission zeros at $s = \infty$, as an LP is supposed to. The transfer function can be written either by inspection or by using the voltage-divider rule. Following the latter approach, we obtain

$$\begin{aligned} T(s) &= \frac{V_o}{V_i} = \frac{Z_2}{Z_1 + Z_2} = \frac{Y_1}{Y_1 + Y_2} = \frac{1/sL}{(1/sL) + sC + (1/R)} \\ &= \frac{1/L}{s^2 + s(1/R) + (1/LC)} \end{aligned} \quad (12.37)$$

12.5.4 Realization of the High-Pass Function

To realize the second-order high-pass function, node y is disconnected from ground and connected to V_2 , as shown in Fig. 12.18(c). Here the series capacitor introduces a transmission zero at $s = 0$ (LP), and the shunt inductor introduces another transmission zero at $s = 0$ (LP). Thus, by inspection, the transfer function may be written as

$$T(s) = \frac{V_o}{V_i} = \frac{Q_2 s^2}{s^2 + s(\omega_0/Q_2) + \omega_0^2} \quad (12.38)$$

where ω_0 and Q are the natural mode parameters given by Eqs. (12.24) and (12.35) and ω_0 is the high-frequency transmission. The value of ω_0 can be determined from the circuit by observing that as s approaches ∞ , the capacitor approaches a short circuit and V_o approaches V_i , resulting in $\omega_0 = 1$.

12.5.5 Realization of the Bandpass Function

The bandpass function is realized by disconnecting node x from ground and connecting it to V_2 , as shown in Fig. 12.18(c). Here the series impedance is negative and thus does not introduce any transmission zeros. These are obtained as follows: One zero at $s = 0$ is

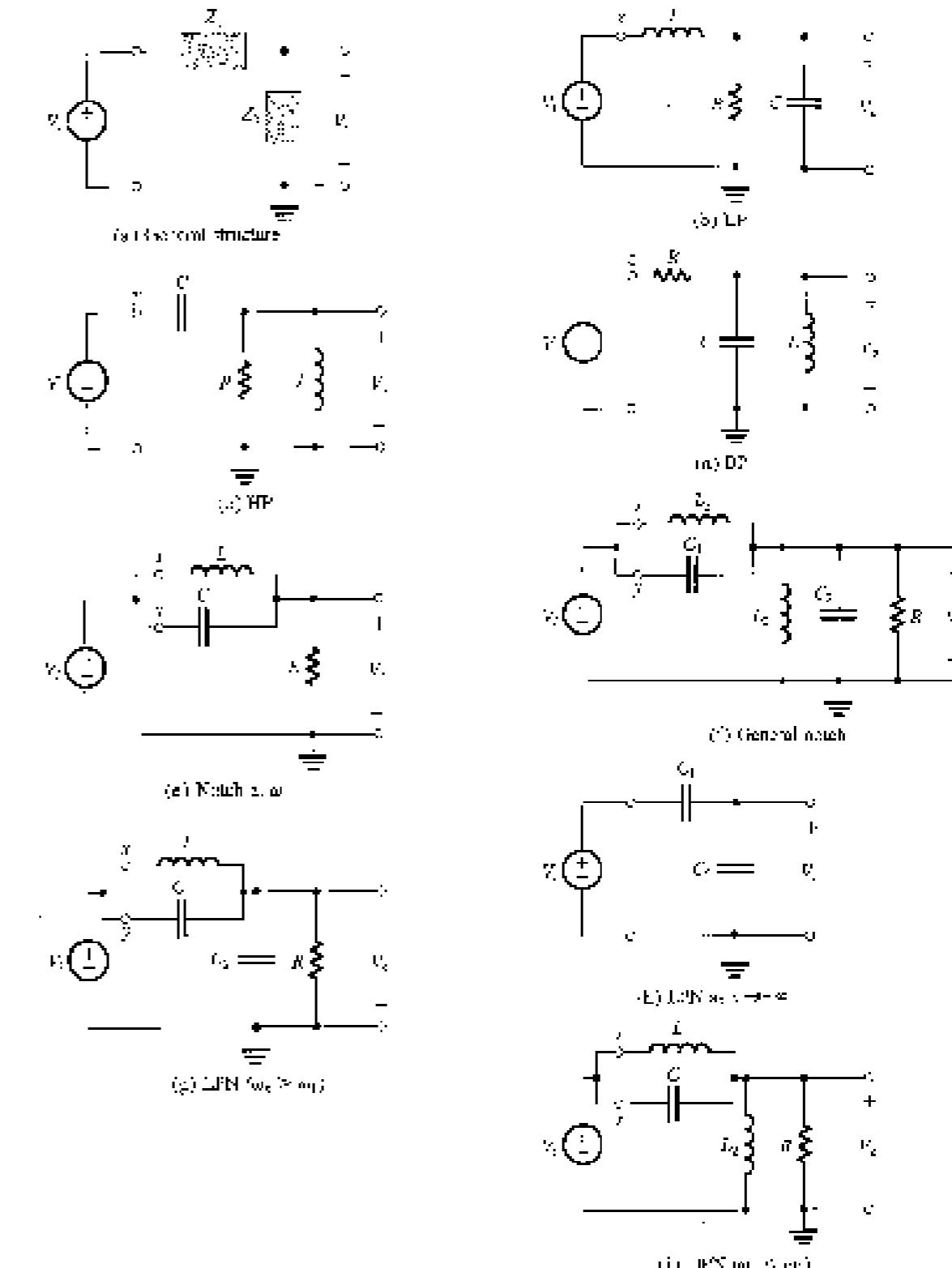


FIGURE 12.18 Realization of various basic second-order functions using the LCR circuit of Fig. 12.17(c). (a) general structure; (b) LP; (c) HP; (d) notch at ω_0 ; (e) general notch; (f) LPN ($\omega_c > \omega_0$); (g) LPN ($\omega_c < \omega_0$); (h) BPF ($\omega_c < \omega_0$); (i) BPF ($\omega_c > \omega_0$).

realized by the short inductor, and one zero at $s = -\omega_0$ is realized by the shunt capacitor. At the center frequency ω_0 , the parallel LC-trunk circuit exhibits an infinite impedance, and thus no current flows in the circuit. It follows that at $\omega = \omega_0$, $V_2 \approx V_1$. In other words, the center-frequency gain of the bandpass filter is unity. Its transfer function can be obtained as follows:

$$\begin{aligned} T(s) &= \frac{V_2}{V_1} = \frac{1/R}{(1/R) + (1/sL_1) + sC} \\ &= \frac{s(L_1CR)}{s^2 + s(1/CR) + 1/LC} \end{aligned} \quad (12.39)$$

12.5.6 Realization of the Notch Functions

To obtain a pair of transmission zeros on the $j\omega$ -axis we use a parallel resonance circuit in the series arm, as shown in Fig. 12.18(e). Observe that this circuit is obtained by disconnecting both nodes x and y from ground and connecting them together to V_1 . The impedance of the LC circuit becomes infinite at $\omega = \omega_0 = 1/\sqrt{LC}$, thus causing zero transmission at this frequency. The shunt impedance is resistive and thus does not introduce transmission zeros. It follows that the circuit in Fig. 12.18(e) will realize the notch transfer function

$$T(s) = \omega_0 \frac{s^2 + \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (12.40)$$

The value of the high-frequency gain, ω_0 , can be found from the circuit to be unity.

To obtain a notch filter realization in which the notch frequency ω_0 is arbitrarily placed relative to ω_0 , we adopt a variation on the scheme above. We shall use a parallel LC circuit in the series branch, as shown in Fig. 12.18(f) where L_2 and C_2 are selected so that

$$L_2C_2 = 1/\omega_0^2 \quad (12.41)$$

Then the L_2C_2 tank circuit will introduce a pair of transmission zeros at ω_0/ω_0 , provided the L_2C_2 tank is not resonant at ω_0 . Apart from this restriction, the values of L_2 and C_2 must be selected to ensure that the output modes have not been altered, that is,

$$C_1 + C_2 = C \quad (12.42)$$

$$L_1 \parallel L_2 = L \quad (12.43)$$

In other words, when V_1 is replaced by a short circuit, the circuit should reduce to the original LCR resonator. Another way of thinking about the circuit of Fig. 12.18(f) is that it is obtained from the original LCR resonator by lifting part of L and part of C off ground and connecting them to V_1 .

It should be noted that in the circuit of Fig. 12.18(f), L_2 does not introduce a zero at $s = 0$ because at $s = 0$, the L_2C_2 circuit also has a zero. In fact, at $s = 0$ the circuit reduces to an inductive voltage divider with the dc transmission being $L_2/(L_1 + L_2)$. Similar comments can be made about L_2 and the fact that it does not introduce a zero at $s = \infty$.

The LPN and HPN filter realizations are special cases of the general notch circuit of Fig. 12.18(f). Specifically, for the LPN,

$$\omega_0 > \omega_0$$

and thus

$$L_2C_2 < (L_1 + L_2)(C_1 + C_2)$$

This condition can be satisfied with L_2 eliminated (i.e., $L_2 = \infty$ and $L_1 = L$), resulting in the LPN circuit in Fig. 12.18(g). The transfer function can be written by inspection as

$$T(s) = \frac{V_2}{V_1} = \omega_0 \frac{s^2 + \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (12.44)$$

where $\omega_0^2 = 1/LC_1$, $\omega_0 = 1/\sqrt{L(C_1 + C_2)}$, $\omega_0/Q = 1/CR$, and ω_0 is the high-frequency gain. From the circuit we see that as $s \rightarrow \infty$, the circuit reduces to that in Fig. 12.18(h), for which

$$\frac{V_2}{V_1} = \frac{L}{C_1 + C_2}$$

That is

$$\omega_0 = \frac{C_1}{C_1 + C_2} \quad (12.45)$$

To obtain an HPN realization we start with the circuit of Fig. 12.18(i) and use the fact that $\omega_0 < \omega_0$ to obtain

$$L_2C_1 > (L_1 + L_2)(C_1 + C_2)$$

which can be satisfied while selecting $C_2 = 0$ (i.e., $C_1 = C$). This we obtain the reduced circuit shown in Fig. 12.18(j). Observe that as $s \rightarrow \infty$, V_2 approaches V_1 , and thus the high-frequency gain is unity. Thus, the transfer function can be expressed as

$$T(s) = \frac{V_2}{V_1} = \frac{s^2 + 1/L_1C_1}{s^2 + s(1/CR) + 1/L_1L_2C_1} \quad (12.46)$$

12.5.7 Realization of the All-Pass Function

The all-pass transfer function

$$T(s) = \frac{s^2 + s(\omega_0/Q) + \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (12.47)$$

can be written as

$$T(s) = 1 + \frac{s^2 + s(\omega_0/Q) + \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (12.48)$$

The second term on the right-hand side is a bandpass function with a center-frequency gain of 2. We already have a bandpass circuit (Fig. 12.18(l)) but with a center-frequency gain of unity. We shall therefore attempt an all-pass realization with a flat gain of 0.5, that is,

$$T(s) = 0.5 + \frac{s(\omega_0/Q)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

This function can be realized using a voltage divider with a transmission ratio of 0.5 together with the bandpass circuit of Fig. 12.18(l). To effect the subtraction, the output of the all-pass circuit is taken between the output terminal of the voltage divider and that of the

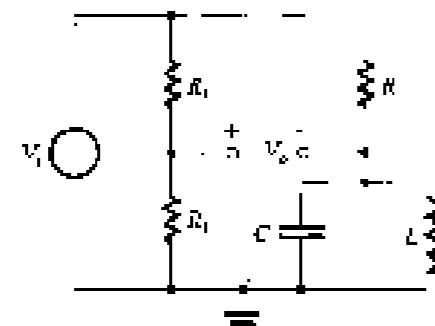


FIGURE 12.19 Realization of the second-order all-pass transfer function using a voltage divider and an LCR resonator.

bandpass filter, as shown in Fig. 12.10. Unfortunately this circuit has the disadvantage of lacking a common ground terminal between the input and the output. An op-amp-RC realization of the all-pass function will be presented in the next section.

EXERCISES

- (12.17) Design a second-order low-pass filter based on the inductance theory with a -3-dB frequency of 100 Hz.
 (12.18) Design a second-order high-pass filter with a corner frequency of 100 Hz.
 (12.19) Design a third-order low-pass filter from a given inductor value of $L = 10 \mu H$.
 (12.20) Design a third-order high-pass filter from a given capacitor value of $C = 10 pF$.
 (12.21) Use $\omega_c = 2\pi f_c$ and $\omega = 2\pi f$ to show that the values obtained from the normalized filters are proportional in low-frequency applications.

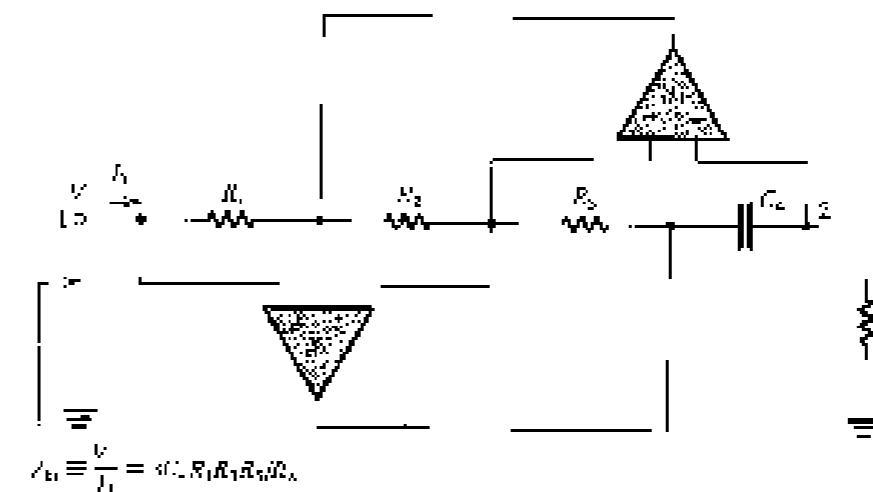
12.6 SECOND-ORDER ACTIVE FILTERS BASED ON INDUCTOR REPLACEMENT

In this section, we study a family of op-amp-RC circuits that realize the various second-order filter functions. The circuits are based on an op-amp-RC resonator obtained by replacing the inductor L in the LCR resonator with an op-amp-RC circuit that has an inductive input impedance.

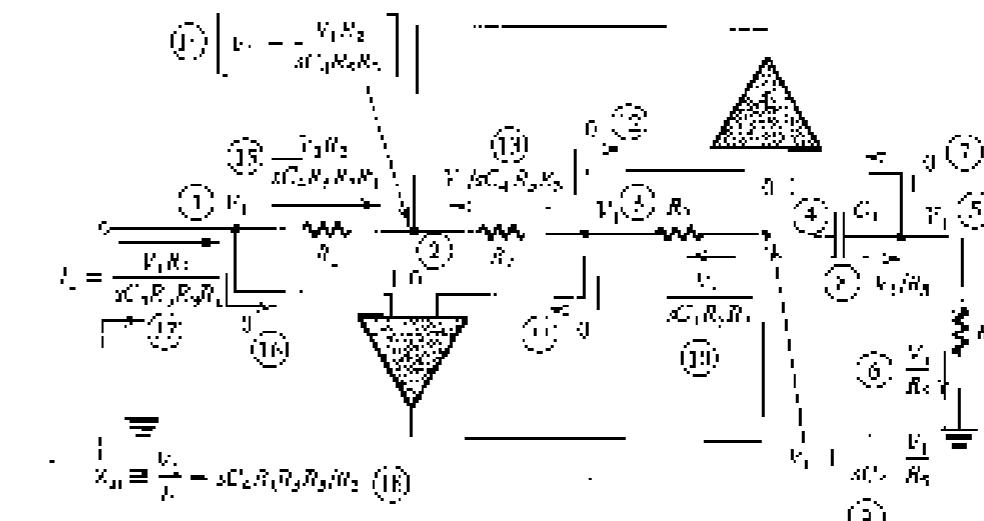
12.6.1 The Antoniou Inductance-Simulation Circuit

Over the years, many op-amp-RC circuits have been proposed for simulating the operation of an inductor. Of these, one circuit invented by A. Antoniou⁷ (see Antoniou (1969)) has proved to be the "best." By "best" we mean that the operation of the circuit is very linear, of the nonideal properties of the op-amps, in particular their finite gain and bandwidth. Figure 12.20(a) shows the Antoniou inductance-simulation circuit. If the circuit is fed at its input (node 1) with a voltage source V_1 and the input current is denoted I_1 , then for ideal

⁷ Antoniou Antonis Antoniou Antoniou (born 1930) is a member of the faculty of the University of Victoria, British Columbia.



(a)



(b)

FIGURE 12.20 (a) The Antoniou inductance-simulation circuit; (b) analysis of the circuit assuming ideal op-amps. The order of the analysis steps is indicated by the circled numbers.

op-amps the input impedance can be shown to be

$$Z_{in} = V_1/I_1 = sC_2R_1R_3R_6/R_2 \quad (12.49)$$

which is that of an inductance L given by

$$L = C_2R_1R_3R_6/R_2 \quad (12.50)$$

Figure 12.20(b) shows the analysis of the circuit assuming that the op-amps are ideal and thus that a virtual short circuit appears between the two input terminals of each op-amp, and assuming also that the input currents of the op-amps are zero. The analysis begins at node 1.

which is assumed to be fed by a voltage source V_1 , and proceeds step by step, with the order of the steps indicated by the circled numbers. The result of the analysis is the expression shown for the input current I , from which, Z_m is found.

The design of this circuit is usually based on selecting $R_1 = R_2 = R_3 = R_4 = R$ and $C_1 = C_2$, which leads to $\beta = 0.707$. Convenient values are then selected for C and R to yield the desired inductance value L . More details on this circuit and the effect of the nonidealities of the op-amps on its performance can be found in Selsor and Brucke (1978).

12.6.2 The Op-Amp-RC Resonator

Figure 12.21(a) shows the LCR resonator we studied in detail in Section 12.5. Replacing the inductor L with a simulated inductance realized by the Autotuner circuit of Fig. 12.23(a) results in the op-amp-RC resonator of Fig. 12.21(b). Figures for the inductor the add tuned amplifier drawn with broken lines.) The circuit of Fig. 12.21(b) is a second-order resonator having a pole frequency

$$\omega_0 = 1/\sqrt{LC} = 1/\sqrt{C_1 C_2 R_1 R_2 / R_3} \quad (12.51)$$

where we have used the expression for L given in Eq. (12.50), and a pure Q factor,

$$Q = \omega C_2 R_3 / R_2 = \frac{C_2}{C_1} \frac{R_3}{R_1 R_2} \quad (12.52)$$

Usually one selects $C_1 = C_2 = C$ and $R_1 = R_2 = R_3 = R_4 = R$, which results in

$$\omega_0 = 1/CR \quad (12.53)$$

$$Q = R_3 / R \quad (12.54)$$

Thus, if we select a practically convenient value for C , we can use Eq. (12.53) to determine the value of R to realize a given ω_0 , and then use Eq. (12.54) to determine the value of R to realize a given Q .

12.6.3 Realization of the Various Filter Types

The op-amp-RC resonator of Fig. 12.21(b) can be used to generate circuit realizations for the various second-order filter sections by following the approach described in detail in Section 12.5 in connection with the LCR resonator. Thus to obtain a bandpass function we disconnect node x from ground and connect it to the signal source V_1 . A high-pass function is obtained by injecting V_1 to node y . To realize a low-pass function using the LCR resonator, the inductor terminal is disconnected from ground and connected to V_1 . The corresponding node is the active resonator is the node at which R_3 is connected to ground,⁵ labeled as node x in Fig. 12.21(b). A regular notch function ($\omega_n = \omega_0$) is obtained by feeding V_1 to nodes x and y . In all cases the output can be taken as the voltage across the resonance capacitor V_2 . However, this is not a convenient node to use as the filter output terminal because capacitively load here would change the filter characteristics. The problem can be solved easily by adding a buffer amplifier. This is the amplifier of gain K , drawn with broken lines in Fig. 12.21(b).

⁵This point might not be obvious. The reader, however, can show that when V_1 is fed to this node the transfer V_2/V_1 is indeed low pass.

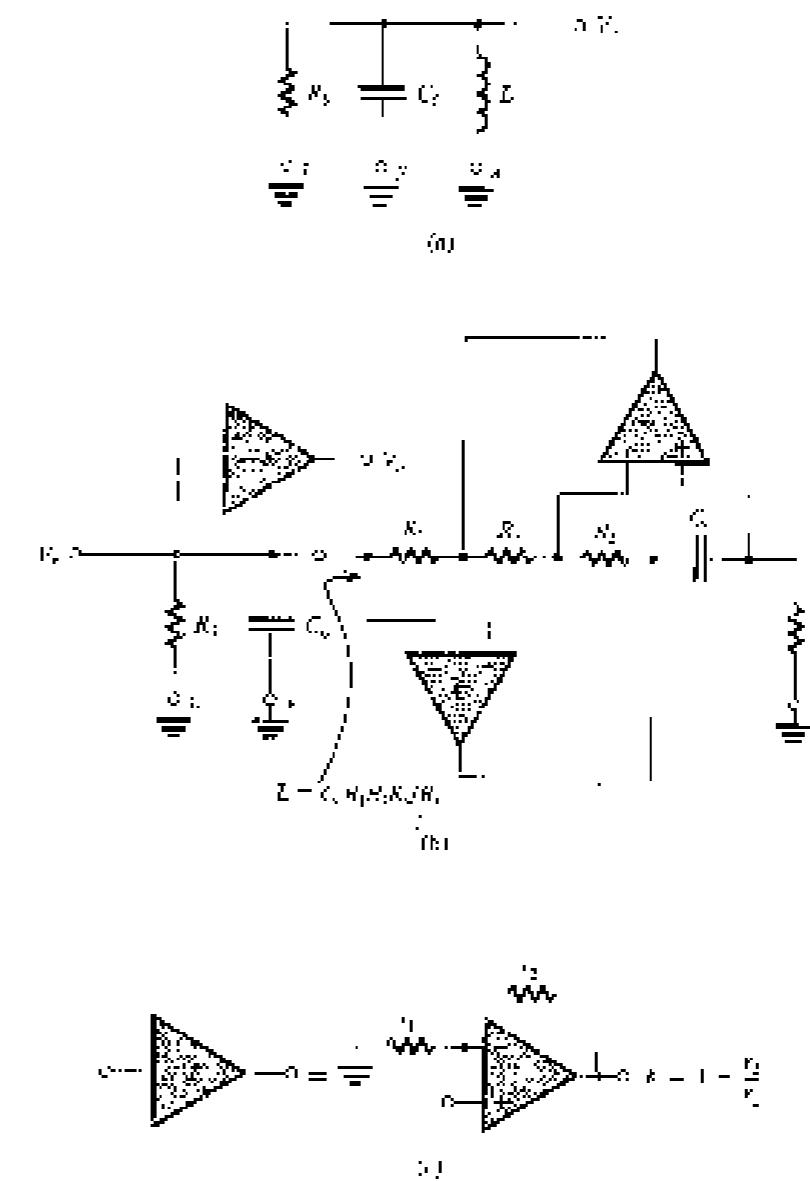
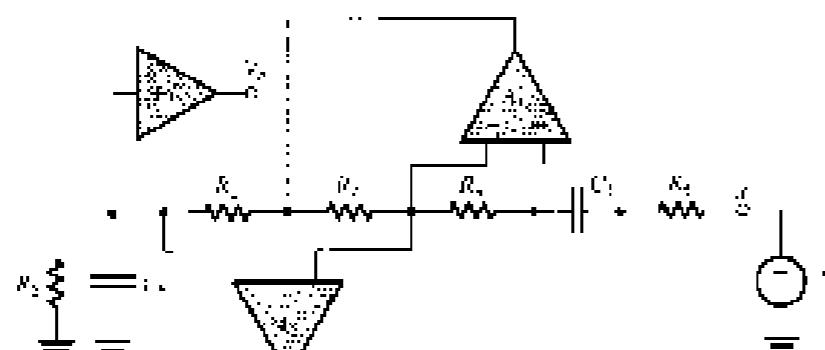


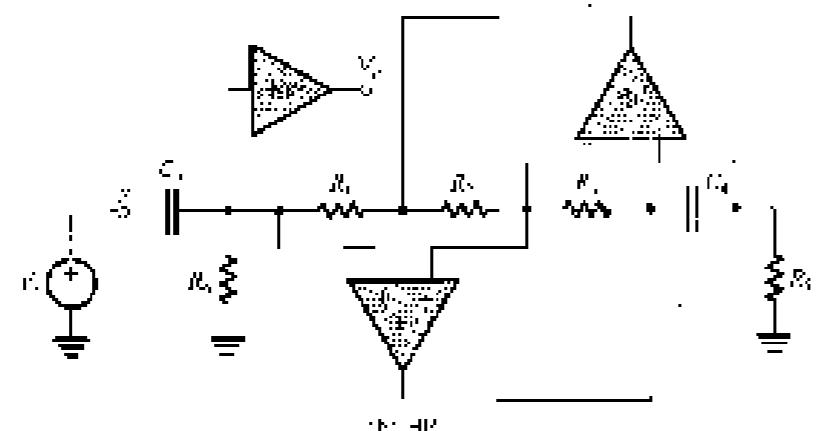
FIGURE 12.21 (a) An LCR resonator. (b) An op-amp-RC resonator obtained by replacing the inductor L in the LCR resonator of (a) with a simulated inductance realized by the autotuner circuit of Fig. 12.23(a). (c) Implementation of the buffer amplifier K .

Figure 12.21(c) shows how this amplifier can be simply implemented using an op-amp connected in the noninverting configuration. Note that not only does the amplifier buffer the output of the filter, but it also allows the designer to set the filter gain to any desired value by appropriately selecting the value of K .

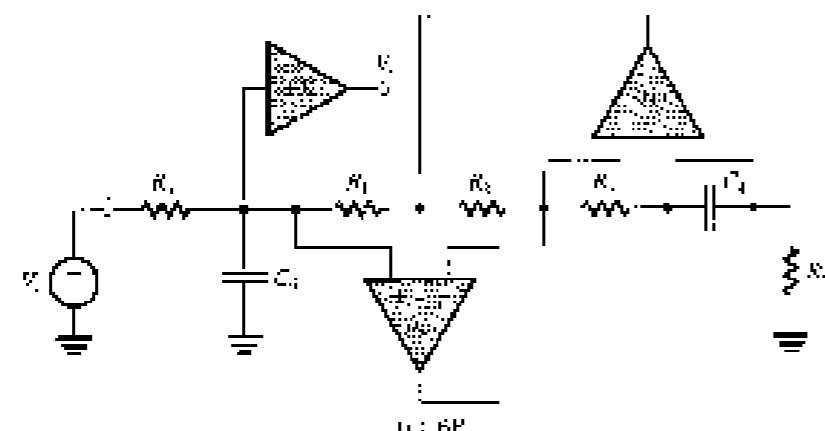
Figure 12.22 shows the various second-order filter circuits obtained from the resonator of Fig. 12.21(b). The transfer functions and design equations for these circuits are given in



(a) LP



(b) HP



(c) BP

FIGURE 12.22 Realizations of the various second-order filter functions using the op-amp-RC ladder of Fig. 12.21(a). (a) LP, (b) HP, (c) BP.

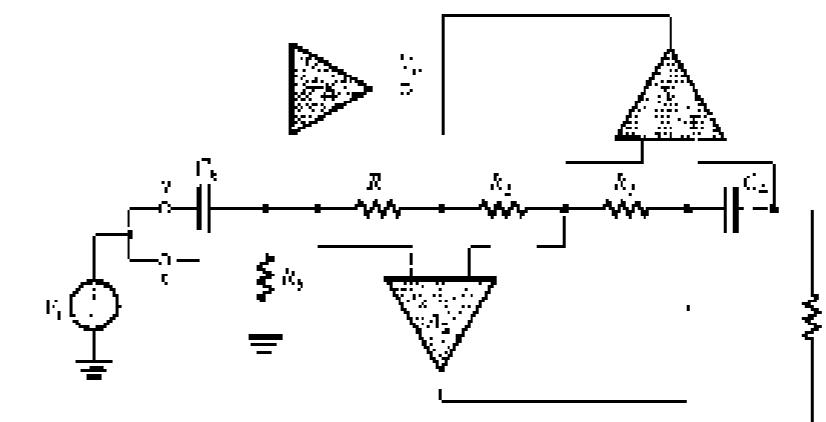
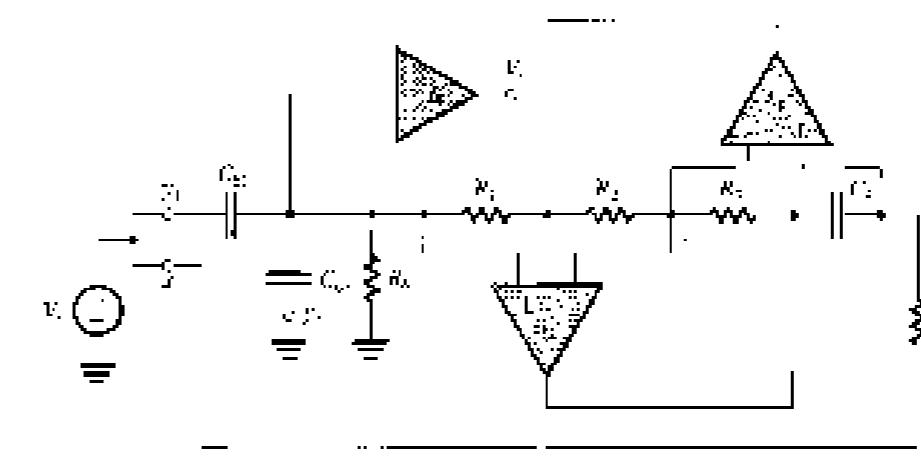
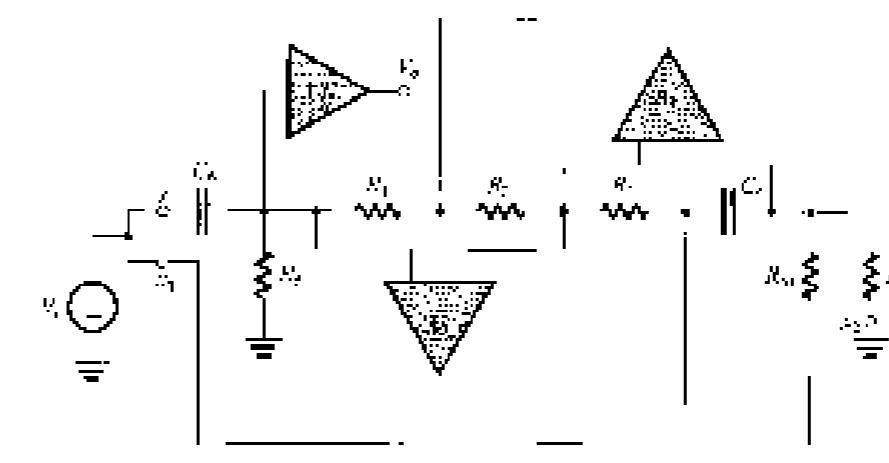
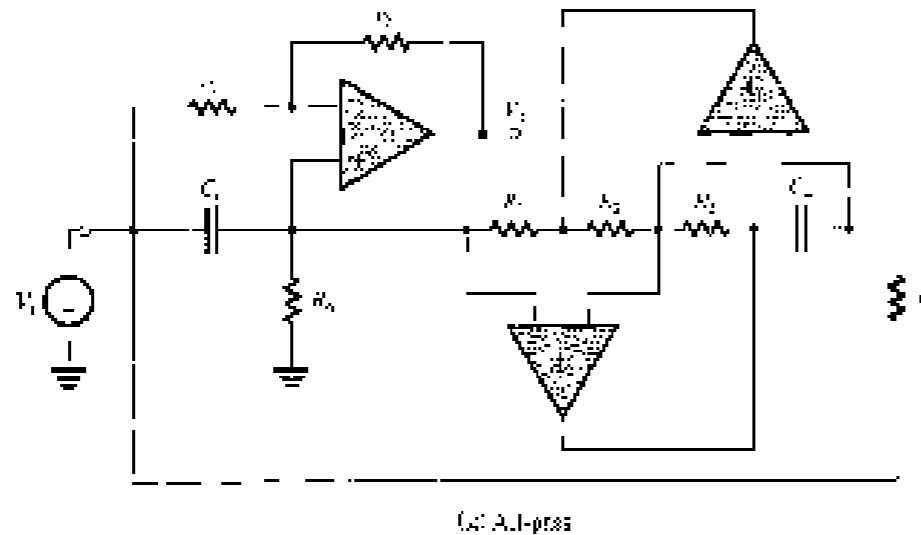
(d) Notch at w_p (e) LPN, $m_1 > m_0$ (f) HPN, $m_1 < m_0$

FIGURE 12.23 Realizations of (d) notch at w_p , (e) LPN, (f) HPN, if $m_1 \leq m_0$, and



(a) All-pass

FIGURE 12.22 (Continued) (g) all-pass. The circuits are based on the LCR circuits in Fig. 12.18. Design equations are given in Table 12.1.

Table 12.1. Note that the transfer functions can be written by analogy to those of the LCR resonator. We have already commented on the LP, HP, BP, and complex-match circuits given in Fig. 12.22(a) to (d). The LPN and HPN circuits in Fig. 12.22(e) and (f) are obtained by direct analogy to their LCR counterparts in Fig. 12.18(g) and (h), respectively. The all-pass circuit in Fig. 12.22(g), however, deserves some explanation.

12.5.4 The All-Pass Circuit

An all-pass function with a flat gain of unity can be written as

$$AP = \frac{1}{s} (RP \text{ with a center frequency gain of } 2) \quad (12.55)$$

(see Eq. 12.48). Two circuits whose transfer functions are related in this fashion are said to be complementary.⁷ Thus the all-pass circuit with unity flat gain is the complement of the bandpass circuit with a center-frequency gain of 2. A simple procedure exists for obtaining the complement of a given linear circuit. Disconnect all the circuit nodes that are connected to ground and connect them to V_0 , and disconnect all the nodes that are connected to V_0 and connect them to ground. That is, interchanging input and ground in a linear circuit generates a circuit whose transfer function is the complement of that of the original circuit.

Returning to the problem at hand, we can use the circuit of Fig. 12.22(e) to realize a BP with a gain of 2 by simply selecting $K = 2$ and implementing the filter amplitude with the circuit of Fig. 12.22(e) with $n = 2$. We then interchange input and ground and thus obtain the all-pass circuit of Fig. 12.22(g).

Finally, in addition to being simple to design, the circuits in Fig. 12.22 exhibit excellent performance. They can be used on their own to realize second-order filter functions, or they can be cascaded to implement higher-order filters.

⁷ More about complementary circuits will be presented later in conjunction with Fig. 12.31.

TABLE 12.1 Design Details—Circuits in Fig. 12.22

Circuit	Trans. Function and Other Parameters	Design Equations
Resonator Fig. 12.22(b)	$\omega_0 = 1/\sqrt{C_1 C_2 R_1 R_2 / K}$ $Q = 0, \frac{\omega_0}{\sqrt{C_1 R_1 R_2 K}}$	$C_L = C_1 + C_2$ (parallel value) $R_1 + R_2 - R_s = R_1 + 1/(2\omega_0^2)$ $R_s = Q/\omega_0 C$
Low-pass (LP) Fig. 12.22(b)	$T(s) = \frac{K R_s / C_1 C_2 R_1 R_2}{s^2 + s \frac{R_1}{C_1 R_2} + \frac{R_2}{C_1 C_2 R_1 R_2 R_s}}$	$K = DC$ gain
High-pass (HP) Fig. 12.22(b)	$T(s) = \frac{K R_s}{s^2 + s \frac{1}{C_1 R_2} + \frac{s}{C_1 C_2 R_1 R_2 R_s}}$	$K = \text{High frequency gain}$
Bandpass (BP) Fig. 12.22(c)	$T(s) = \frac{K s / C_1 R_2}{s^2 + s \frac{1}{C_1 R_2} + \frac{s}{C_1 C_2 R_1 R_2 R_s}}$	$K = \text{Center-frequency gain}$
Notchfilter Fig. 12.22(d)	$T(s) = \frac{K (s^2 + (R_2/C_1 C_2 R_1 R_2 R_s))}{s^2 + s \frac{1}{C_1 R_2} + \frac{s}{C_1 C_2 R_1 R_2 R_s}}$	$K = \text{res. and notch-frequency gain}$
Low-pass notch (LPN) Fig. 12.22(e)	$T(s) = K \frac{C_m}{C_m + C_K}$ $\propto \frac{s^2 + (R_2/C_1 C_2 R_1 R_2 R_s)}{s^2 + s \frac{1}{C_m R_s} + \frac{1}{C_m C_K R_s} (R_1 R_2 R_s)}$	$K = DC$ gain $C_L = C_K = C_1 = C^*$ $C_m = C_1 (2\omega_0^2 R_s)^{-1}$ $C_K = C_1 C_2 R_s^{-1}$
High-pass notch (HPN) Fig. 12.22(f)	$T(s) = K \frac{s^2 + (R_2/C_1 C_2 R_1 R_2 R_s)}{s^2 + s \frac{1}{C_m R_s} + \frac{1}{C_m C_K R_s} (\frac{1}{R_1} + \frac{1}{R_2})}$	$K = \text{High frequency gain}$ $\omega_0 = 1/\sqrt{C_1 C_2 R_1 R_2 R_s / K}$ $\omega_b = \sqrt{\frac{R_1}{4 C_1 C_2 R_1 R_2 R_s}} (\frac{1}{R_1} + \frac{1}{R_2})$ $Q = R_2 \sqrt{\frac{C_m}{C_1 C_2 R_1 R_2 R_s}} \frac{R_s}{R_1 R_2 R_s}$ $\frac{R_1}{R_2} = \frac{1}{\omega_b^2} = \frac{1}{K^2} = \omega_0^2$ $R_{s1} = R_s (\omega_b / \omega_0)^2$ $R_{s2} = R_s (1 + (\omega_0 / \omega_b)^2)$
All-pass (AP) Fig. 12.22(g)	$T(s) = \frac{s^2 + s \frac{1}{C_1 R_1} + \frac{R_2}{C_1 C_2 R_1 R_2}}{s^2 + s \frac{1}{C_1 R_2} + \frac{R_2}{C_1 C_2 R_1 R_2}}$	$\omega_0 = \omega_b = 1/(2\omega_0^2)$ $\text{Flat gain} = 1$ Actual ω_0 or make $Q_s = 0$

EXERCISES

- 12.19. Consider the circuit of Fig. 12.23(a) to design a second-order bandpass filter with a center frequency of 10 Hz and a Q factor of 10.
- 12.20. Given $\omega_c = 2\pi \times 10^3$, $R_1 = 100\Omega$, $C_1 = 1\mu F$, $R_2 = 100\Omega$, and $C_2 = 1\mu F$, calculate the center frequency and the Q factor of the filter.
- 12.21. Calculate the center frequency of the filter shown in Fig. 12.23(b) based on the component values given in Table 12.1(a). Note that you can make the center frequency equal to 10 Hz if the resistor values in Fig. 12.1(a), where the gain is unity, are equal to 100 Ω .
- 12.22. Design a second-order filter with a center frequency of 10 Hz and a Q factor of 10. The circuit is to be realized with two integrators, each with a gain of 100, and no feedback.
- 12.23. Design a second-order filter with $\omega_c = 10\pi$ rad/s and $Q = 10$ using two integrators, each with a gain of 100, and no feedback. Hint: The transfer function of the filter is $\frac{V_{op}}{V_i} = \frac{K}{s^2 + 2\zeta\omega_c s + \omega_c^2}$. If we let $\zeta = 10$, then $\omega_c = 10\pi$ rad/s and $K = 100$. Note that $\omega_c = 10\pi$ rad/s is equivalent to 10 Hz.

12.7 SECOND-ORDER ACTIVE FILTERS BASED ON THE TWO-INTEGRATOR-LOOP TOPOLOGY

In this section, we study another family of op-amp RC circuits that realize second-order filter functions. The circuits are based on the use of two integrators connected in cascade in an overall feedback loop and are thus known as two-integrator-loop circuits.

12.7.1 Derivation of the Two-Integrator-Loop Biquad

To derive the two-integrator-loop biquadratic circuit, or biquad as it is commonly known,⁸ consider the second-order high-pass corner function

$$\frac{V_{op}}{V_i} = \frac{Ks^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} \quad (12.56)$$

where K is the high-frequency gain. Cross-multiplying Eq. (12.56) and dividing both sides of the resulting equation by s^2 to get all the terms involving s in the form $1/s$, which is the transfer function of an integrator, gives

$$v_{in} - \frac{1}{Q\sqrt{s}} v_{op} = \left(\frac{d^2}{dt^2} v_{op} \right) - K v_i \quad (12.57)$$

In this equation we observe that the signal $(1/Q\sqrt{s})V_{op}$ can be obtained by passing V_{op} through an integrator with a time constant equal to $1/Q\sqrt{s}$. Furthermore, passing the resulting signal through another identical integrator results in the third signal mentioned, V_{op} , in Eq. (12.57)—namely, $(1/Q\sqrt{s})^2 V_{op}$. Figure 12.23(a) shows a block diagram for such a two-integrator arrangement. Note that in anticipation of the use of the inverting op-amp Miller integrator circuit to implement each integrator, the integrator blocks in Fig. 12.23(a) have been assigned negative signs.

The problem still remains, however, of how to find V_{op} , the input signal feeding the two cascaded integrators. Toward that end, we rearrange Eq. (12.57), expressing V_{op} in terms of its single and double integrated versions and of V_{in} :

$$V_{op} = KV_i - \frac{1}{Q^2 s} V_{op} - \frac{\omega_c^2}{s} V_{op} \quad (12.58)$$

⁸ The name biquad comes from the fact that this circuit is the most general form of a way of realizing a biquadratic transfer function, that is, one that is the ratio of two quadratic polynomials.

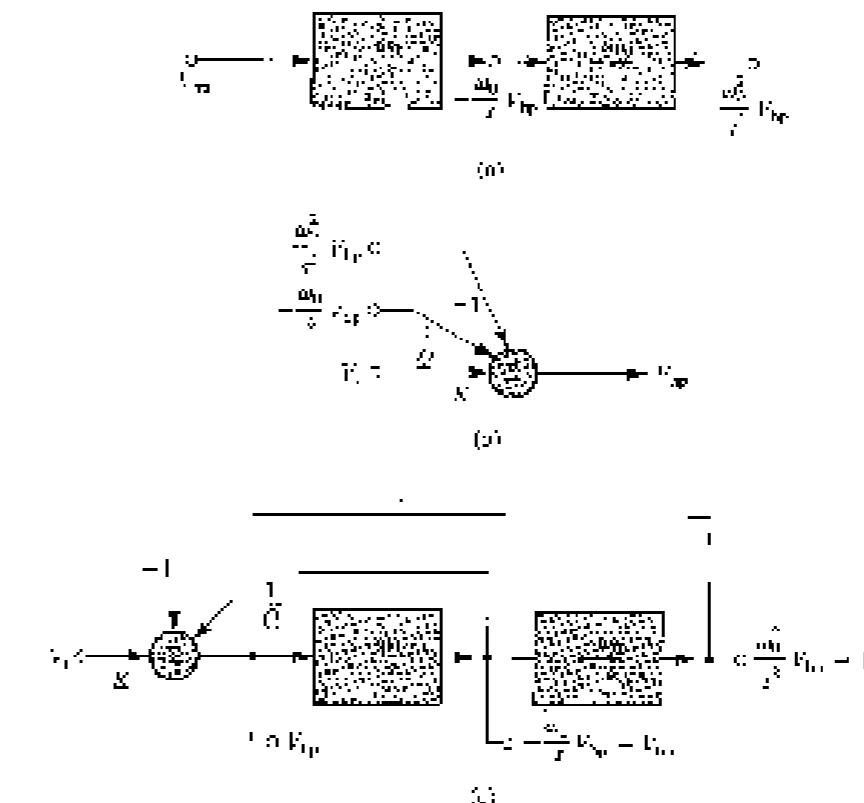


FIGURE 12.23 Derivation of a block diagram realization of the two-integrator-loop topology.

which suggests that V_{op} can be obtained by using the weighted summer of Fig. 12.22(b). Now it should be easy to see that a complete block diagram realization can be obtained by combining the integrator blocks of Fig. 12.23(a) with the summer block of Fig. 12.23(b), as shown in Fig. 12.23(c).

In the realization of Fig. 12.23(c), V_{op} , obtained at the output of the summer, realizes the high-pass transfer function $V_{op}/V_i = V_{op}/V_i$ of Eq. (12.56). The signal at the output of the first integrator is $(1/Q\sqrt{s})V_{op}$, which is a bandpass function:

$$\frac{(1/Q\sqrt{s})V_{op}}{V_i} = \frac{K\omega_c s}{s^2 + 2\zeta\omega_c s + \omega_c^2} = T_1(s) \quad (12.59)$$

Therefore the signal at the output of the first integrator is labeled V_p . Note that the center-frequency gain of the bandpass filter realized is equal to $-KQ$.

In a similar fashion, we can show that the corner function realized at the output of the second integrator is the low-pass function:

$$\frac{(1/Q^2 s^2) V_{op}}{V_i} = \frac{K\omega_c^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} = T_2(s) \quad (12.60)$$

Thus the output of the second integrator is labeled V_n . Note that the dc gain of the low-pass filter realized is equal to K .

We conclude that the two-integrator-loop formed shown in block diagram form in Fig. 12.23(c) realizes the three basic second-order filtering functions, LP, BP, and HP.

simultaneously. This versatility has made the circuit very popular and has given it the name *universal active filter*.

12.7.2 Circuit Implementation

To obtain an op-amp circuit implementation of the two-in, one-out-loop (Eq. 12.23c), we replace each integrator with a Miller integrator circuit having $C_R = 1/\omega_0$, and we replace the virtual ground with a op-amp summing circuit that is capable of assigning both positive and negative weights to its inputs. The resulting circuit, known as the KHN biquad or KHN biquad after its inventors, is shown in Fig. 12.24(a). Given ω_0 , Q , and K , the design of the circuit is straightforward. We select suitable values for R_1 , R_2 , and R_3 so that $C_R = 1/\omega_0$. To practical values for the components of the integrators C and R so that $C_R = 1/\omega_0$. To determine the values of the resistors associated with the summer, we first use superposition to express the output of the summer V_{sum} in terms of its inputs. $V_{\text{in}} = 1/\omega_0/C_R V_{\text{in}}$ and $V_{\text{p}} = \omega_0^2/3 V_{\text{in}}$ give

$$V_{\text{sum}} = \frac{R_1}{R_1 + R_2} V_{\text{in}} + \frac{R_2}{R_1 + R_2} \left(1 + \frac{R_3}{R_1} \right) \cdot \frac{\omega_0}{\omega_0 + Q} V_{\text{in}} + \frac{R_2}{R_1 + R_2} \left(\frac{\omega_0}{\omega_0 + Q} V_{\text{in}} \right) - \frac{R_2}{R_1 + R_2} \left(\frac{\omega_0}{\omega_0 + Q} V_{\text{in}} \right) \quad (12.65)$$

Equating the last right-hand-side terms of Eqs. (12.51) and (12.58) gives

$$R_2/R_1 = 1 \quad (12.66)$$

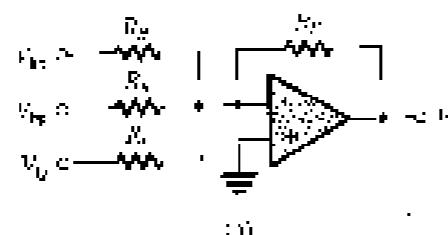
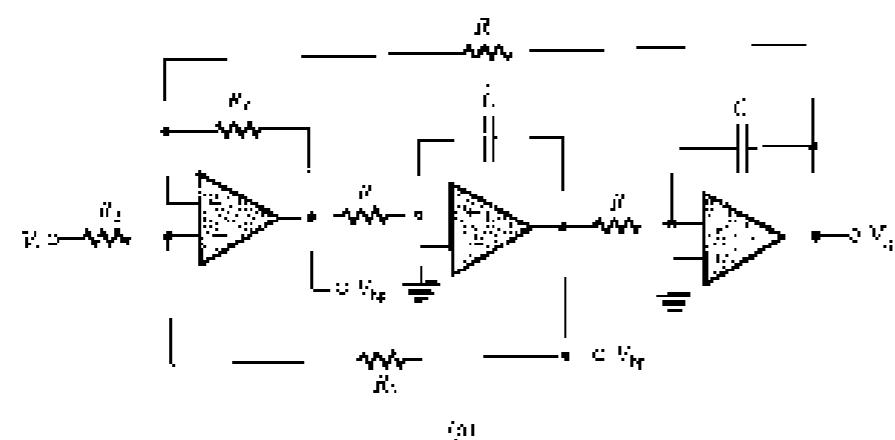


FIGURE 12.24 (a) The KHN biquad circuit obtained by direct implementation of the block diagram of Fig. 12.23(c). The three low-pass filtering functions, BP, HP, and LP, are simultaneously realized. (b) The circuit of Fig. 12.23(c). In this version, filtering functions BP, HP, and LP are simultaneously realized. The three cut-offs are realized with appropriate weights using this op-amp model and all-pass mode.

which implies that we can select arbitrary but practically convenient values for R_1 and R_2 . Then, equating the second-to-last terms on the right-hand side of Eqs. (12.61) and (12.58) and setting $R_1 = R_2$ yields the ratio R_3/R_1 required to realize a given Q as

$$R_3/R_1 = 2Q + 1 \quad (12.67)$$

Thus an arbitrary but convenient value can be selected for either R_1 or R_2 , and the value of the other resistance can be determined using Eq. (12.67). Finally, equating the coefficients of V_{in} in Eqs. (12.61) and (12.58) and substituting $R_3 = R_1$ and for R_3/R_1 from Eq. (12.67) results in

$$K = 2 + 1/Q \quad (12.68)$$

Thus the gain parameter K is fixed to this value.

The KHN biquad can be used to realize notch and all-pass fractions by employing weighted versions of the three outputs, LP, BP, and HP. Such an op-amp realization is shown in Fig. 12.24(b); for this structure we find that

$$\begin{aligned} V_{\text{sum}} &= -\left(\frac{R_1}{R_1 + R_2} V_{\text{in}} + \frac{R_2}{R_1 + R_2} V_{\text{in}} - \frac{R_3}{R_1 + R_2} V_{\text{in}} \right) \\ &= -V_{\text{in}} \left(\frac{R_2}{R_1 + R_2} + \frac{R_3}{R_1 + R_2} + \frac{R_1}{R_1 + R_2} \right) \end{aligned} \quad (12.69)$$

Substituting for T_{LP} , T_{BP} , and T_{HP} from Eqs. (12.56), (12.59), and (12.60), respectively, gives the overall transfer function

$$\frac{V_{\text{out}}}{V_{\text{in}}} = K \frac{(R_1/R_2)^2 - s(R_2/R_3)\omega_0 + (R_1/R_2)\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (12.70)$$

from which we can see that different transmission zeros can be obtained by the appropriate selection of the values of the summing resistors. Tearing since, a notch is obtained by selecting $R_3 = \infty$ and

$$\frac{R_3}{R_1} = \left(\frac{\omega_0}{\omega_n} \right)^2 \quad (12.71)$$

12.7.3 An Alternative Two-Integrator-Loop Biquad Circuit

An alternative two-integrator-loop biquad circuit in which all three op-amps are used in a single-ended mode can be developed as follows. Rather than using the input summer to add signals with positive and negative coefficients, we can introduce an additional inverter, as shown in Fig. 12.25(a). Now all the coefficients of the summer have the same sign, and we can dispense with the summing amplifier altogether and perform the summation at the virtual-ground input of the first integrator. The resulting circuit is shown in Fig. 12.25(b), from which we observe that the high-pass function is no longer available. This is the price paid for obtaining a circuit that utilizes all op-amps in a single-ended mode. The circuit of Fig. 12.25(b) is known as the Tow-Thomson biquad, after its originators.

Rather than using a fourth op-amp to realize the finite transmission zeros required for the notch and all-pass functions, as was done with the KHN biquad, an economical feedforward scheme can be employed with the 10 × 1-beam mixer. Specifically, the virtual ground available at the input of each of the three op-amps in the Tow-Thomson circuit permits the input signal to be fed to all three op-amps, as shown in Fig. 12.26. If V_{in} is taken at the output

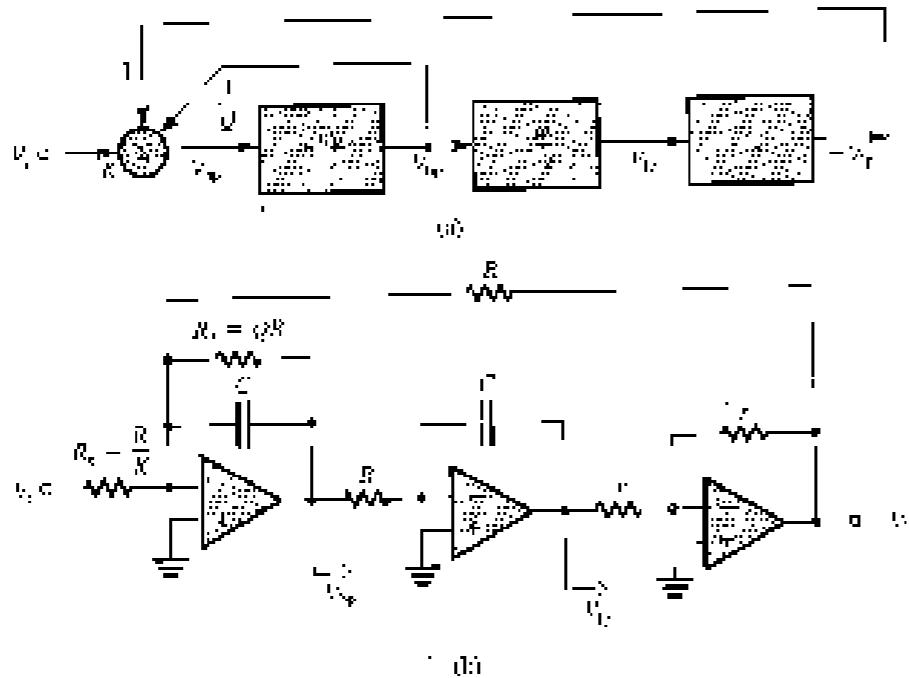


FIGURE 12.25 (a) Alternative two-integrator-loop input in \$w_1, b_1\$ form; (b) the resulting circuit known as the Tere-Termin biquad.

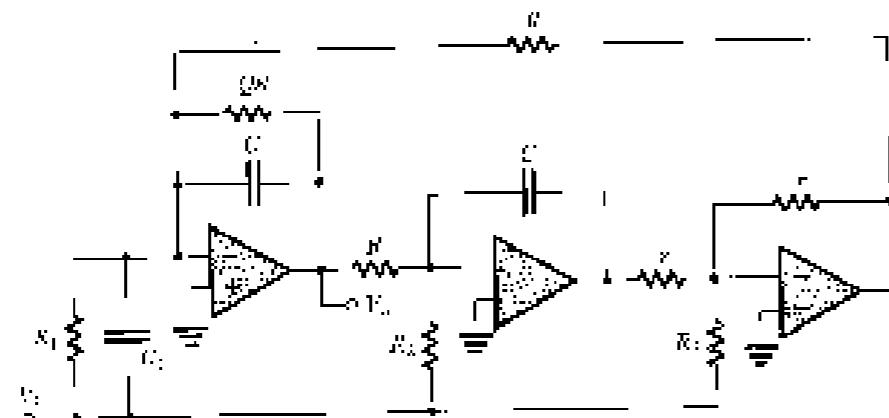


FIGURE 12.26 The new biquad circuit with feedback. The transfer function of Eq. (12.4c) is realized by feeding the input signal through appropriate resistors to the inputs of the three op-amps. This circuit is called an active two-integrator biquad. The design equations are given in Table 12.2.

In the discrete-integrator straightforward analysis yields the filter transfer function

$$\frac{V_3}{V_1} = -\frac{s(C)}{s(C) + \frac{1}{\omega R_1} + \frac{r}{R_2 C}} \cdot \frac{1}{s(C) + \frac{1}{\omega R_3}} \quad (12.58)$$

which can be used to obtain the design data given in Table 12.2.

TABLE 12.2 Design Data for the Circuit of Fig. 12.26

All cases	$C = \text{arbitrary}$, $R = \text{arbitrary}$
LP	$C = 0$, $R_1 = \infty$, $R_2 = \text{load}$ ω , $R_3 = \infty$
Positive BP	$C = 0$, $R_1 = \infty$, $R_2 = \infty$, $\omega = 1/\sqrt{\text{center frequency}}$
Negative BP	$C_1 = 0$, $R_1 = \omega$, $\text{center frequency} \leq \omega$, $R_2 = \infty$, $R_3 = \infty$
HP	$C_1 = \omega$, $\text{high-frequency gain}$, $R_1 = \infty$, $R_2 = \infty$, $R_3 = \infty$
Notch	$C_1 = C$, $\text{high-frequency gain}$, $R_1 = \infty$
AP (pass)	$R_2 = R_1 \omega^2 C_1^2$, $\text{high-frequency gain}$, $R_3 = \infty$
AP	$C_1 = C$, low-gain , $R_1 = \infty$, $R_2 = R_3$, $R_3 = \omega R_2$

12.7.4 Final Remarks

Two-integrator-loop circuits are extremely versatile and easy to design. However, their performance is adversely affected by the finite bandwidth of the op-amps. Special techniques exist for compensating the circuit for such effects [see the SPICE simulation in Section 12.12 and Sochi and Brackbill (1978)].

EXERCISES

- 012.21 Design the Tere-Termin biquad of Fig. 12.26 to realize a low-pass filter with a corner frequency of $\omega_c = 1000 \text{ rad/sec}$. The desired passband gain is $A_p = 10$ and the stopband gain is $A_s = 0.1$. The load resistance is $R_L = 500 \text{ k}\Omega$; $\omega = R_L C = 100 \text{ rad/sec}$.
- 012.22 Use the Tere-Termin biquad of Fig. 12.26 to realize a second-order bandpass filter with a center frequency of $\omega_c = 1000 \text{ rad/sec}$, a bandwidth of $BW = 100 \text{ rad/sec}$, and a stopband gain of $A_s = 0.1$. The load resistance is $R_L = 500 \text{ k}\Omega$; $\omega = R_L C = 100 \text{ rad/sec}$; $R_1 = 10 \text{ k}\Omega$; $R_2 = 10 \text{ k}\Omega$; $R_3 = 10 \text{ k}\Omega$.
- 012.23 Use the Tere-Termin biquad (Fig. 12.26) to realize a second-order low-pass filter with a corner frequency of $\omega_c = 1000 \text{ rad/sec}$, a stopband gain of $A_s = 0.1$, and a passband gain of $A_p = 10$. The load resistance is $R_L = 500 \text{ k}\Omega$; $\omega = R_L C = 100 \text{ rad/sec}$; $R_1 = 10 \text{ k}\Omega$; $R_2 = 10 \text{ k}\Omega$; $R_3 = 10 \text{ k}\Omega$.
- 012.24 Use the data of Table 12.2 to design the biquad circuit of Fig. 12.26 to realize an all-pass filter with $\omega_c = 10^4 \text{ rad/sec}$, $A_p = 1$, and a stopband gain of $A_s = 10$ if $C = 0.01 \text{ F}$ and $\tau = 10 \text{ k}\Omega$.
- 012.25 Use the Tere-Termin biquad of Fig. 12.26 to realize a bandpass filter with a center frequency of $\omega_c = 1000 \text{ rad/sec}$, a bandwidth of $BW = 100 \text{ rad/sec}$, and a stopband gain of $A_s = 0.1$. The load resistance is $R_L = 500 \text{ k}\Omega$; $\omega = R_L C = 100 \text{ rad/sec}$; $R_1 = 10 \text{ k}\Omega$; $R_2 = 10 \text{ k}\Omega$; $R_3 = 10 \text{ k}\Omega$.

12.8 SINGLE-AMPLIFIER BIQUADRATIC ACTIVE FILTERS

The open-pole RC biquadratic filter is studied in the two preceding sections. Open-pole performance, are versatile, and are easy to design and to adjust simply after final assembly. Unfortunately, however, they are not economic in their use of op-amps, requiring three or four amplifiers per second-order section. This can be a problem, especially in applications where power-supply current is to be conserved. For instance, in a battery-operated instrument. In this section we shall study a class of second-order filter circuits that requires only one op-amp per section. These minimal realizations, however, suffer a greater dependence

on the desired gain and bandwidth of the op amp and can also be more sensitive to the unavoidable tolerances in the values of resistors and capacitors than the multiple-op-amp biquads of the preceding sections. The single-amplifier biquads (SABs) are therefore limited to the less stringent filter specifications—for example, pole-Q factor less than about 30.

The synthesis of SAB circuits is based on the use of feedback to move the poles of an RC circuit from the negative real axis, where they naturally lie, to the complex conjugate positions required to provide selective filter response. The synthesis of SABs follows a two-step process:

1. Synthesis of a feedback loop that realizes a pair of complex-conjugate poles characterized by a frequency ω_0 and a Q factor Q .
2. Injecting the input signal in a way that realizes the desired transmission zeros.

12.8.1 Synthesis of the Feedback Loop

Consider the circuit shown in Fig. 12.27(a), which consists of a two-port RC network a placed in the negative-feedback path of an op amp. We shall assume that, except for having a finite gain A , the op-amp is ideal. We shall denote by $\pi(s)$ the open-circuit voltage transfer function of the RC network a , where the definition of $\pi(s)$ is illustrated in Fig. 12.27(b). The transfer function $\pi(s)$ can in general be written as the ratio of two polynomials $N(s)$ and $D(s)$:

$$\pi(s) = \frac{N(s)}{D(s)}$$

The roots of $N(s)$ are the transmission zeros of the RC network, and the roots of $D(s)$ are its poles. Study of network theory shows that while the poles of an RC network are restricted to lie on the negative real axis, the zeros can in general lie anywhere in the s -plane.

The loop gain $L(s)$ of the feedback circuit in Fig. 12.27(a) can be determined using the method of Section 8.7. It is simply the product of the op-amp gain A and the transfer function $\pi(s)$:

$$L(s) = A\pi(s) = \frac{A N(s)}{D(s)} \quad (12.69)$$

Substituting for $L(s)$ into the characteristic equation

$$1 - L(s) = 0 \quad (12.70)$$

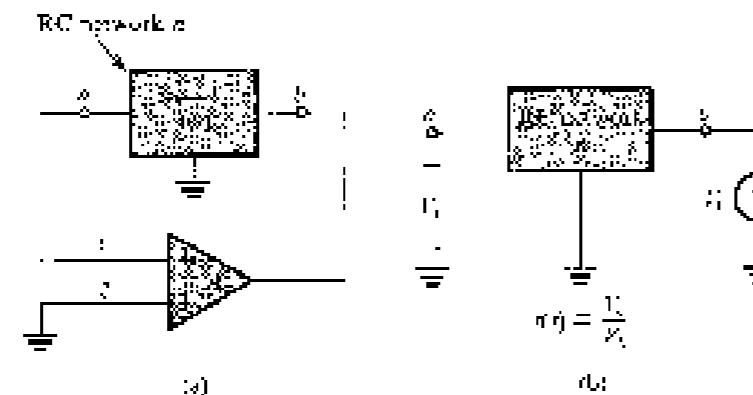


FIGURE 12.27 (a) Feedback loop realized by placing a two-port RC network a in the feedback path of an op-amp. (b) Definition of the open-circuit transfer function $\pi(s)$ of the RC network.

results in the poles s_p of the closed-loop circuit obtained as solutions to the equation:

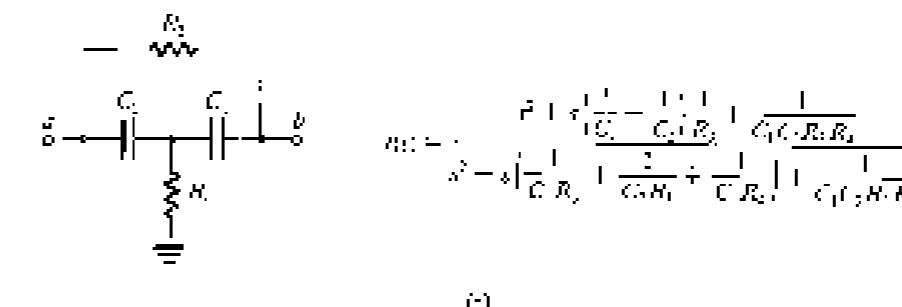
$$D(s_p) = -\frac{1}{A} \quad (12.71)$$

In the ideal case, $A = \infty$ and the poles are obtained from

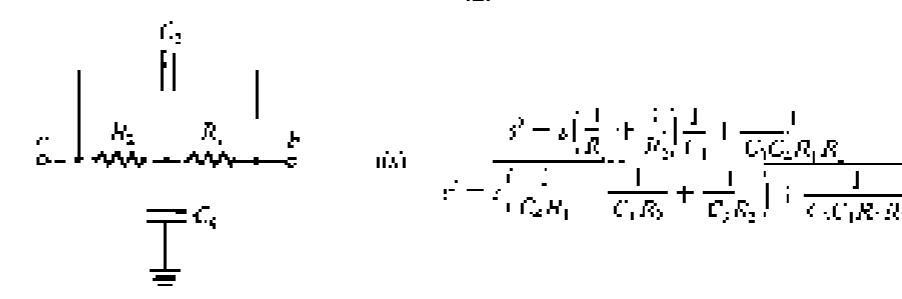
$$N(s_p) = 0 \quad (12.72)$$

That is, the filter poles are identical to the zeros of the RC network.

Since our objective is to realize a pair of complex-conjugate poles, we should select an RC network that can have complex-conjugate transmission zeros. The simplest such networks are the bridged-T networks shown in Fig. 12.28 together with their transfer functions $\pi(s)$ from b to a , with a open-circuited. As an example, consider the circuit generated by placing the bridged-T network of Fig. 12.28(a) in the negative feedback path of an op-amp, as shown in Fig. 12.29.



(a)



(b)

FIGURE 12.28 (a) RC networks (called bridged-T networks) that can have complex-conjugate transmission zeros. The transfer functions given are from b to a , with a open-circuited.



FIGURE 12.29 An active filter feedback loop generated using the bridged-T network of Fig. 12.28(a).

The pole polynomial of the active-filter circuit will be equal to the numerator polynomial of the bridge-C network; thus,

$$\omega^2 + \frac{\alpha}{Q} = \omega^2 - \frac{1}{\sqrt{C_1 C_2}} \frac{1}{R_1 R_2 R_3 R_4}$$

which enables us to obtain α and Q :

$$\alpha = -\frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \quad (12.73)$$

$$Q = \left[\frac{\sqrt{C_1 C_2 R_1 R_2}}{R_1} \cdot \frac{1}{C_1} + \frac{1}{C_2} \right]^{1/2} \quad (12.74)$$

If we are designing this circuit, α and Q are given and Eqs. (12.73) and (12.74) can be used to determine C_1 , C_2 , R_2 , and R_3 . It follows that there are two degrees of freedom. Let us exhaust one of these by selecting $C_1 = C_2 = C$. Let us also denote $R_3 = R$ and $R_4 = R/\alpha$. By substituting in Eqs. (12.73) and (12.74) and with some manipulation, we obtain

$$\alpha = 1/Q \quad (12.75)$$

$$CR = \frac{2R}{\alpha} \quad (12.76)$$

Thus if we are given the value of Q , Eq. (12.75) can be used to determine the ratio of the two resistances R_2 and R_3 . Once the given values of α and Q can be substituted in Eq. (12.76) to determine the time constant CR . There remains one degree of freedom—the value of C to R . This can be arbitrarily chosen in the actual design. Its value, which sets the importance level of the circuit, should be chosen so that the resulting component values are practical.

EXERCISES

- 12.25 Design the circuit of Fig. 12.29 with $\omega_p = 10^3$ rad/s and $Q = 0.707$.
- 12.26 Design the circuit of Fig. 12.29 with $\omega_p = 10^3$ rad/s and $Q = 0.414$.
- 12.27 Design the circuit of Fig. 12.29 with $\omega_p = 10^3$ rad/s and $Q = 0.283$.
- 12.28 Design the circuit of Fig. 12.29 with $\omega_p = 10^3$ rad/s and $Q = 0.200$.
- 12.29 Design the circuit of Fig. 12.29 with $\omega_p = 10^3$ rad/s and $Q = 0.141$.

12.8.2 Injecting the Input Signal

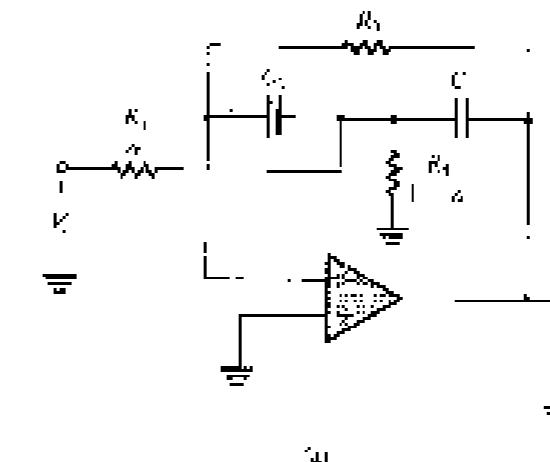
Having synthesized a feedback loop that realizes a given pair of poles, we now consider connecting the input signal source to the circuit. We wish to do this, of course, without altering the poles.

Since, for the purpose of finding the poles of a circuit, an ideal voltage source is equivalent to a short circuit, it follows that any circuit node that is connected to ground can instead be connected to the input voltage source without causing the poles to change. Thus the method of injecting the input voltage signal into the feedback loop is simply to place a component (or several components) that is first connected to ground and connect it (them) to the input source. Depending on the component(s) through which the input signal is injected,

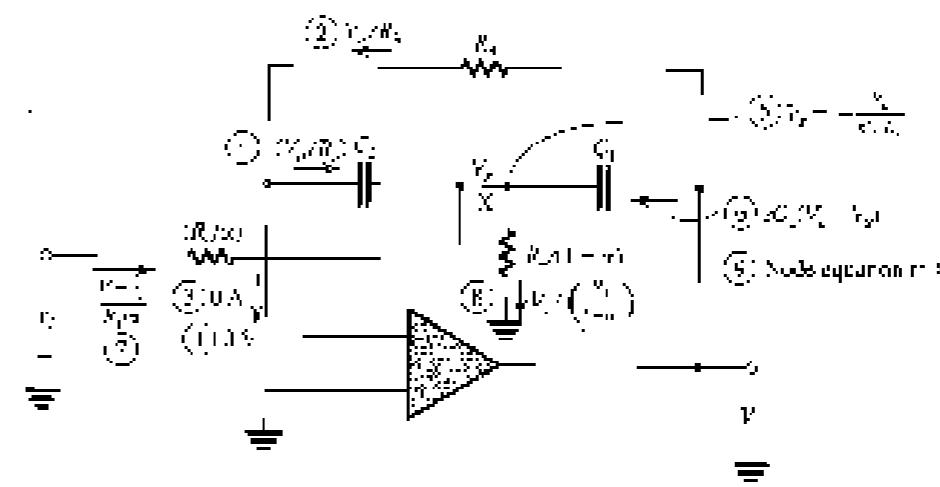
different transmission zeros are obtained. This is, of course, the same method we used in Section 12.5 with the LCR resonator, and in Section 12.6 with the biquad based on the LCR resonator.

As an example, consider the feedback loop of Fig. 12.29. Here we have two grounded nodes: the terminal of R_2 and the positive input terminal of the op-amp; that can serve for injecting the input signal. Figure 12.30(a) shows the circuit with the input signal injected through part of the resistor R_2 . Note that the two resistances R_2/α and $R_2(1-\alpha)$ are parallel equivalents to R_2 .

Analysis of the circuit to determine its voltage transfer function $T(s) = V_o(s)/V_i(s)$ is illustrated in Fig. 12.30(b). Note that we have assumed the op-amp to be ideal, and have indicated the order of the analysis steps by the circled numbers. The final step, number 9,



(a)



(b)

FIGURE 12.30 (a) The feedback loop of Fig. 12.29 with the input signal injected through part of resistance R_2 . This illustrates the injection location. (b) Analysis of the circuit in (a) to determine its voltage transfer function. Between the 1 and 9, the values kept constant by the circled numbers.

consists of writing a loop equation at X and substituting for V_1 by the value determined in step 5. The result is the transfer function

$$\frac{V_o}{V_i} = \frac{s(C_1 R_1)}{s^2 + s(\frac{1}{C_1} + \frac{1}{C_2 R_2}) + \frac{1}{C_1 C_2 R_1 R_2}}$$

We recognize the s -characteristic function whose center-frequency pole can be controlled by the value of α . As expected, the denominator polynomial is identical to the numerator polynomial of $\eta(s)$ given in Fig. 12.28(a).

EXERCISE

- 12.8.1 Use the s -characteristics obtained in Exercise 12.25 to design the bandpass according to Fig. 12.28(a). Calculate the values of R_1 , R_2 , and C_1 to obtain a center frequency of 10 Hz .

12.8.3 Generation of Equivalent Feedback Loops

The complementary transformation of feedback loops is based on the property of linear networks as illustrated in Fig. 12.31 (a) (two-port (three-terminal) network a). In Fig. 12.31(b), terminal c is grounded and a signal V_b is applied to terminal b . The transfer function from b to a with c grounded is denoted η . Then, in Fig. 12.31(b), terminal b is grounded and the input signal is applied to terminal c . The transfer function from c to a with b grounded can be shown to be the complement of η —that is, $1 - \eta$. (Recall that we used this property in generating a circuit realization for the all-pass function in Section 12.6.)

Application of the complementary transformation to a feedback loop to generate an equivalent feedback loop is a two-step process:

1. Nodes of the feedback network and any of the op-amp inputs that are connected to ground should be disconnected from ground and connected to the op-amp output. Conversely, those nodes that were connected to the op-amp output should be new connected to ground. That is, we simply interchange the op-amp output terminal with ground.
2. The two input terminals of the op-amp should be interchanged.

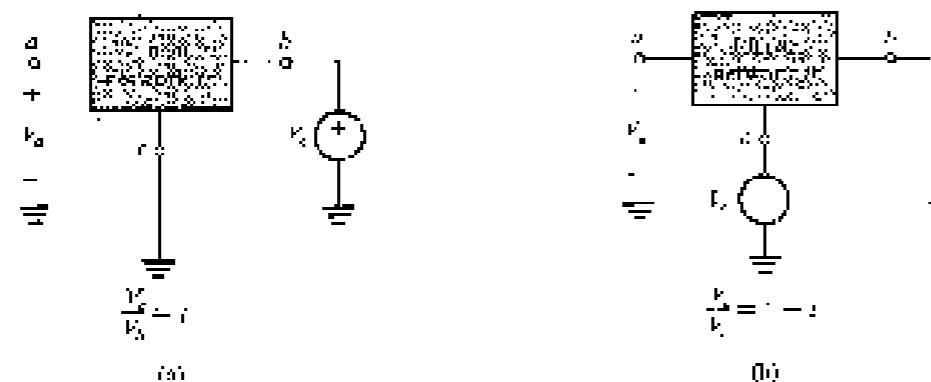


FIGURE 12.31 Generating η from $1 - \eta$ results in the complement of the transfer function.

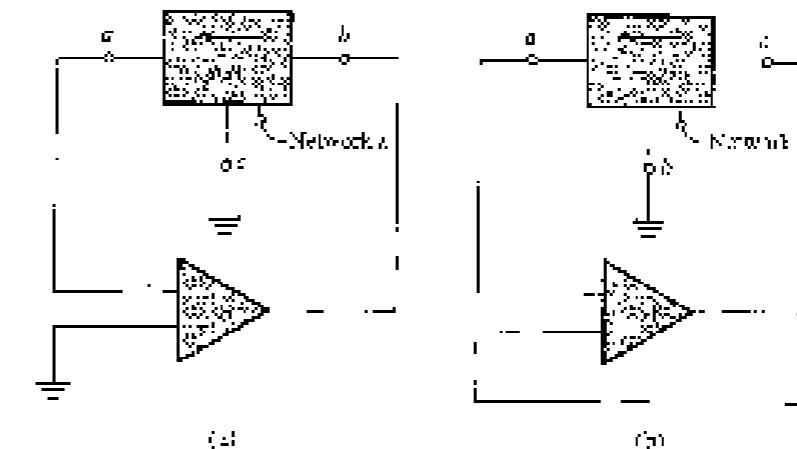


FIGURE 12.32 Application of the complementary transformation to the feedback loop in (a) results in the circuit in (b).

The feedback loop generated by this transformation has the same characteristic equation, and hence the same poles, as the original loop.

To illustrate, we show in Fig. 12.32(a) the feedback loop formed by connecting a two-port RC network to the negative-feedback path of an op-amp. Applying our of the complementary transformation to this loop results in the feedback loop of Fig. 12.32(b). Note that in the latter loop the op-amp is used in the unity-gain follower configuration. We shall now show that the two loops of Fig. 12.32 are equivalent.

If the op-amp has an open-loop gain A , the follower in the circuit of Fig. 12.32(b) will have a gain of $A/(A+1)$. This, together with the fact that the transfer function of network a from c to a is $1 - \eta$ (see Fig. 12.31), enables us to write for the circuit in Fig. 12.32(b) the characteristic equation

$$1 + \frac{A}{A+1}(1 - \eta) = 0$$

This equation can be manipulated to the form

$$1 + A\eta = 0$$

which is the characteristic equation of the loop in Fig. 12.32(a). As an example, consider the application of the complementary transformation to the feedback loop of Fig. 12.29: The feedback loop of Fig. 12.33(a) results. Injecting the input signal through C_1 results in the circuit in Fig. 12.33(b), which can be shown (by direct analysis) to realize a second-order low-pass function. This circuit is one of a family of Sallen-and-Key circuits, after their originators. The design of the circuit in Fig. 12.33(b) is based on Eqs. (12.73) through (12.76); namely, $R_1 = R_2 = R/4Q^2$, $C_1 = C_2 = C$, $CR = 2Q/R_2$, and the value of C is arbitrarily chosen to be practically convenient.

As another example, Fig. 12.34(c) shows the feedback loop generated by placing the two-port RC network of Fig. 12.28(b) in the negative-feedback path of an op-amp. For an ideal op-amp, this feedback loop realizes a pair of complex conjugate natural modes having the same location as the zeros of $\eta(s)$ of the RC network. Thus, using the expression for R_N

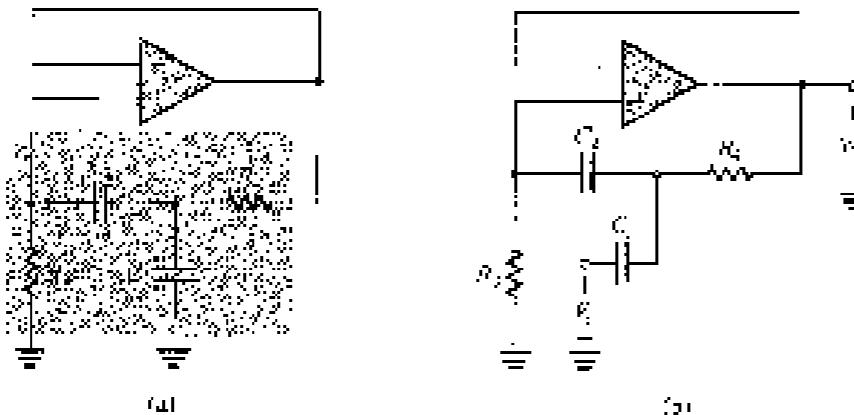


FIGURE 12.33 (a) Sallen-Key low-pass filter obtained by applying the complementary design method to the top in Fig. 12.29; (b) injecting the input signal through C_1 realizes the low-pass function. This is one of the Sallen and Key forms of circuits.

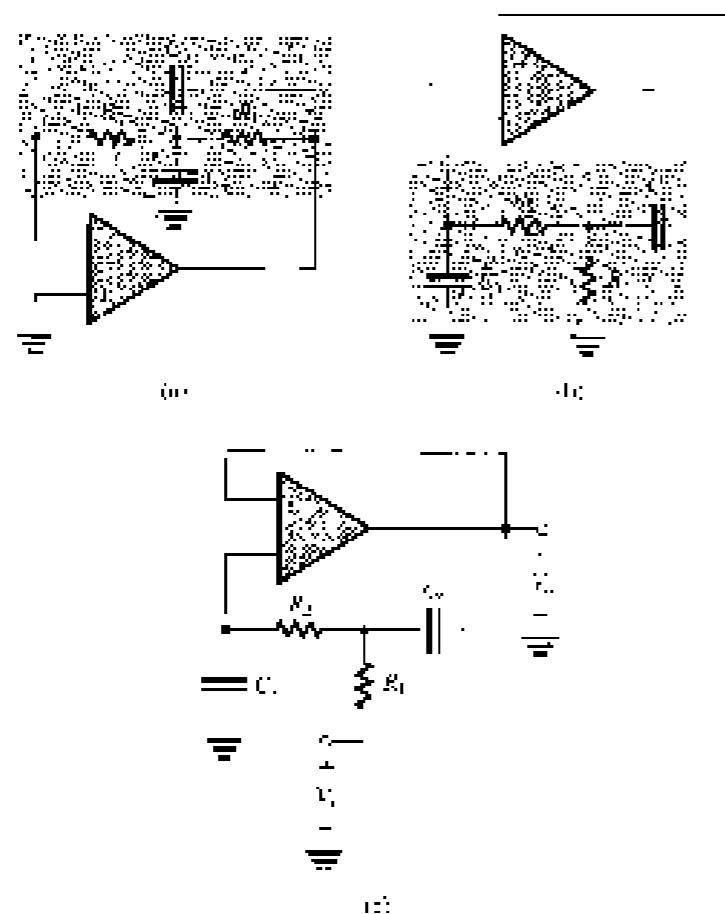


FIGURE 12.34 (a) Feedback op-amp circuit by placing the bridged-T network of Fig. 12.28(a) in the negative feedback op-amp circuit; (b) Equivalent feedback op-amp circuit by applying the complementary compensation method to the top in (a); (c) A low-pass filter circuit realized by injecting V_{in} through R_1 into the loop in (b).

given in Fig. 12.23(b), we can write for the active-filter poles

$$\omega_n = \frac{1}{\sqrt{R_1 C_1 R_2 R_3}} \quad (12.77)$$

$$Q = \frac{\sqrt{R_1 C_1 R_2}}{C_2} \left[\frac{1}{R_1} + \frac{1}{R_3} \right] \quad (12.78)$$

Normally the design of this circuit is based on selecting $R_1 = R_2 = R$, $C_1 = C$, and $C_2 = C/2$. When substituted in Eqs. (12.77) and (12.78), these yield

$$\omega_n = 4\sqrt{R C} \quad (12.79)$$

$$Q = 2\sqrt{R/C} \quad (12.80)$$

with the remaining degree of freedom (the value of C or R) left to be designed to choose.

Injecting the input signal to the C_2 terminal, that is, connected to ground and to be shown to result in a bandpass realization. If, however, we apply the complementary compensated method to the feedback loop in Fig. 12.34(a), we obtain the equivalent loop in Fig. 12.34(b). The loop equivalence means that the circuit of Fig. 12.34(b) has the same poles and, thus, the same ω_n and Q and the same design equations (Eqs. 12.77 through 12.80). The new loop in Fig. 12.34(b) can be used to realize a low-pass function by injecting the input signal as shown in Fig. 12.34(c).

EXERCISES

- (12.28) Calculate ω_n and Q of Fig. 12.34(b) for the values of $R_1 = R_2 = 100 \Omega$, $C_1 = C_2 = 100 \text{ pF}$, and $R_3 = 10 \text{ k}\Omega$ (values in Figs. 12.29 and 12.30). Also show that the design is valid.
- (12.29) Design the circuit of Fig. 12.34(b) for a low-pass filter with $\omega_n = 100 \text{ rad/sec}$ and $Q = 0.707$. Use $R_1 = R_2 = 10 \text{ k}\Omega$, $C_1 = 2.81 \text{ nF}$, $C_2 = 2.81 \text{ pF}$, and $R_3 = 100 \text{ }\Omega$.

12.9 SENSITIVITY

Because of the tolerances in component values and because of the finite op-amp gain, the response of the actual assembled filter will deviate from the ideal response. As a means for predicting such deviations, the filter designer employs the concept of sensitivity. Specifically, for second-order filters one is usually interested in finding how sensitive their poles are relative to variations (both initial tolerances and future drifts) in RC component values and op-amp gain. These sensitivities can be quantified using the classical sensitivity function S'_i , defined as

$$S'_i = \frac{1}{\omega_n} \frac{\partial \omega_n}{\partial x_i} \quad (12.81)$$

Thus,

$$S'_i = \frac{\partial \omega_n}{\partial x_i} \quad (12.82)$$

Here, x denotes the value of a component (a resistor, a capacitor, or an amplifier gain) and y denotes a circuit parameter of interest (ω , y , a_3 , or Q). For small changes

$$\delta_x \approx \frac{\Delta x/\epsilon_x}{\Delta x/x} \quad (12.82)$$

Thus we can use the value of S_x to determine the percent change in y due to a given percent change in x . For instance, if the sensitivity of Q relative to a particular resistance R_1 is 5, then a 1% increase in R_1 results in a 5% increase in the value of Q .

Example 12.3
For the feedback loop of Fig. 12.29, find the sensitivities of a_3 and Q relative to all the passive components and the op-amp gain. Evaluate these sensitivities for the design considered in the preceding section for which $C = C_1$.

Solution

To find the sensitivities with respect to the passive components, called **passive sensitivities**, we assume that the operating gain is infinite. In this case, a_3 and Q are given by Eqs. (12.73) and (12.74). Thus for a_3 we have

$$a_3 = \frac{R_1 R_2 R_3}{jC_1 C_2 R_1 R_2}$$

which can be used along with the sensitivity definition of Eq. (12.82) to obtain

$$\delta_{a_3}^{(P)} + \delta_{a_3}^{(T)} + \delta_{a_3}^{(A)} + \delta_{a_3}^{(Q)} = \frac{1}{j}$$

For $Q \gg 1$ we have

$$Q = \sqrt{jC_2 R_2 R_3 / C_1} \left[\frac{1}{A} + \frac{1}{jC_1 R_1} \right]^{-1}$$

to which we apply the sensitivity definition to obtain

$$\delta_Q^{(P)} = \frac{jC_1 \sqrt{C_2}}{2(A jC_1) + jC_2} - \frac{jC_1}{jC_1 R_1} = \frac{jC_1}{jC_1 R_1}$$

For the design with $C_1 = C_2$ we see that $\delta_Q^{(P)} = 0$. In fact, we can show that

$$\delta_{a_3}^{(P)} = 0, \quad \delta_{a_3}^{(Q)} = \frac{1}{j}, \quad \delta_{a_3}^{(A)} = \frac{1}{j}$$

It is important to remember that the sensitivity expression should be derived before values corresponding to a particular design are substituted.

Next we consider the sensitivities relative to the amplifier gain. If we assume the op-amp to have a finite gain A , the characteristic equation for the loop becomes

$$1 + A(s) = 0 \quad (12.83)$$

where $\zeta(s)$ is given in Fig. 12.28(a). To simplify matters we can substitute for the passive components by their design values. This causes no errors in evaluating sensitivities since we are now finding the sensitivity with respect to the amplifier gain. Using the design values obtained

earlier—namely, $C_1 = C_2 = C$, $R_2 = R$, $R_3 = R/2Q^2$, and $CR = 2Q/a_3$ —we get

$$\zeta(s) = \frac{s^2 + j(\omega_0/Q + \omega_0^2)}{s^2 + j(\omega_0/Q)(2\omega_0^2 + 1) + \omega_0^2} \quad (12.84)$$

where ω_0 and Q denote the nominal or design values of the pole frequency and Q factor. The actual values are obtained by substituting Eq. (12.83) in Eq. (12.84):

$$1 + \frac{\omega_0}{A} (2Q^2 - 1) + \omega_0^2 - A \left[s^2 + j \frac{\omega_0}{Q} + \omega_0^2 \right] = 0$$

Assuming the gain A to be real and dividing both sides by $A - 1$, we get

$$s^2 + j \frac{\omega_0}{Q} + \frac{2Q^2}{A+1} + \omega_0^2 = 0 \quad (12.85)$$

From this equation we see that the actual pole frequency, ω_0 , and the pole Q , Q_A , are

$$\omega_0 = \omega_0 \quad (12.86)$$

$$Q_A = \frac{Q}{1 - 2Q^2/(A+1)} \quad (12.87)$$

Thus

$$\delta_{\omega_0}^{(P)} = 0$$

$$\delta_{Q_A}^{(P)} = \frac{Q}{A+1} \frac{2Q^2/(A+1)}{1 - 2Q^2/(A+1)}$$

For $A \gg 2Q^2$ and $A \gg 1$ we obtain

$$\delta_{Q_A}^{(P)} \approx \frac{2Q^2}{A}$$

It is usual to drop the subscript P in this expression and write

$$\delta_Q^{(A)} \approx \frac{2Q^2}{A} \quad (12.88)$$

Note that if Q is high ($Q \geq 5$), its sensitivity relative to the amplifier gain can be quite high.⁷

12.9.1 A Concluding Remark

The results of Example 12.3 indicate a serious disadvantage of single-amplifier biquads—the sensitivity of Q relative to the amplifier gain is quite high. Although a technique exists for reducing $\delta_Q^{(A)}$ in SABs [see Seira et al. (1980)], this is one of the expenses of increased passive sensitivities. Nevertheless, the resulting SABs are useful diodes in many applications. However, for filters with Q factors greater than about 10, one usually opts for one of the multiamplifier biquads studied in Sections 12.6 and 12.7. For these circuits $\delta_Q^{(A)}$ is proportional to Q , rather than to Q^2 as in the SAB case (Eq. 12.88).

⁷ Because the open-loop gain A of op-amps usually has wide tolerance, it is important to keep $\delta_Q^{(A)}$ and $\delta_Q^{(P)}$ very small.

EXERCISE

1250.0% increase in the 2008 U.S. design rate of 10.0% with U.S. lag. The corresponding percentage changes in oil and gas prices under conditions that (a) oil is 10% higher, (b) oil is 10% lower, (c) gas is 25% higher, and (d) gas is 25% lower are 2% low-end price increases and 2% high-end price decreases.

12.10 SWITCHED-CAPACITOR FILTERS

The active RCL filter circuits presented above have two properties that make their practical implementation difficult, if not practically impossible. These are the need for large valued capacitors and the requirement of accurate RC time constants. The search therefore has continued for a method of filter design that would lend itself more naturally to IC implementation. In this section we shall introduce one such method.

12.1D.1 The Basic Principle

The switched-capacitor filter technique is based on the realization that a capacitive switch between two circuit nodes at a sufficiently high rate is equivalent to a resistor connecting these two nodes. To be specific, consider the active-R/C integrator of Fig. 12.15(c). This is the familiar Miller integrator, which we used in the two-integrator leap-frogged in Section 12.7. In Fig. 12.23(b) we have replaced the input resistor R_1 by a capacitor of value C_1 .

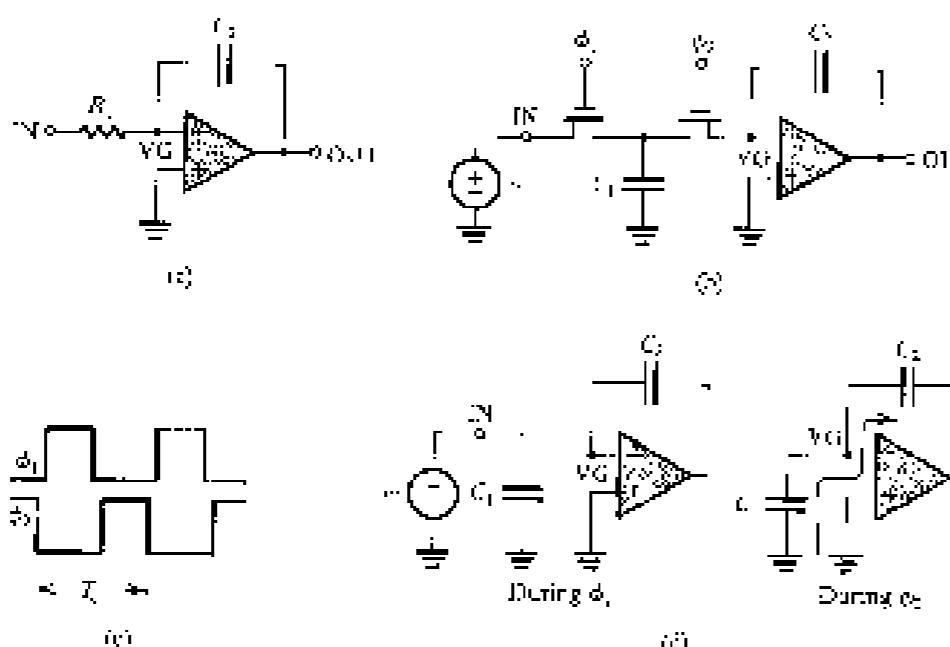


FIGURE 12.35 Multi-projectile of the stacked-diamond FAB technique for $\text{Al} + \text{Au}/\text{Si}$ interconnects. (a) Switched capacitors integrated. (b) Two-point check (no overlapapping). (c) $\text{Au} + \text{SiO}_2 + \text{C}_1$ clusters up to a current value of I_{th} , and then current I_0 discharges into C_2 .

together with two MCMS instances acting as verifiers. In some circuits, more elaborate switch configurations are used. But such features are beyond our present need.

The two MOS switches in Fig. 12.35(b) are driven by a nonoverlapping two-phase clock. Figure 12.35(c) shows the clock waveforms. We shall assume in this introductory exposition that the clock frequency f_c ($f_c \ll f_s$) is much lower than the frequency of the signal being filtered. Thus during clock phase ϕ_1 , when C_1 is connected across the input signal source v_i , the variations in the input signal are negligibly small. It follows that during ϕ_1 capacitor C_1 charges up to the voltage v_o .

$$y_{\infty} = C_2$$

Then, during work phase Δ_1 , capacitor C_1 is connected to the virtual-ground input of the op-amp, as indicated in Fig. 12.25(a). Capacitor C_1 is then forced to discharge, and its previous charge q_1 is transferred to C_2 in the direction indicated in Fig. 12.25(d).

From the description above we see that during each clock period T , an amount of charge $q_{in} - C_1 v_s$ is extracted from the input source and supplied to the integrator capacitor C_2 . Thus, the average current flowing between the input node (IN) and the virtual ground node (VG) is

$$A_{\text{eff}} = \frac{C}{T}$$

If τ_1 is sufficiently short, one can think of this process as almost continuous and define an equivalent resistance R_{eq} that is in effect present between nodes 1N and 1V0.

$$R_{\alpha} = R/\beta$$

Thru

$$K_{\alpha} = T_{\alpha}/C \quad (12.70)$$

Using K_0 , we obtain an equivalent rate constant for the integration:

$$\text{Phase selection} = C \cdot R_{\alpha_1} - \tau_i \frac{C_\alpha}{C_1} \quad (3.31)$$

This time constant T determines the frequency response of the filter is established by the clock period T , and the capacitor ratio C_2/C_1 . Both these parameters can be well controlled in an IC process. Specifically, note the dependence on capacitor ratios rather than on absolute values of capacitors. The accuracy of capacitor ratios in MOS technology can be controlled to within 0.1%.

Another point worth observing is that with a renewable clocking frequency (such as 100 kHz) and not too large capacitor ratios (say, 10), one can obtain reasonably large time constants (such as 10^{-4} s) suitable for audio applications. Since capacitors typically occupy relatively large areas on the IC chip, one attempts to minimize their values. In this context, it is important to note that the ratio accuracies quoted earlier are obtainable with the smallest capacitive value as low as 0.1 pF.

12.10.2 Practical Circuits

The switched-capacitor (SC) circuit in Fig. 12.36(b) realizes an inverting integrator (note the direction of charge flow through C_2 in Fig. 12.36d). As we saw in Section 12.7, a two-pole ladder is an active filter composed of one inverting and one noninverting integrator.

¹⁰ In the two investigated loops of Fig. 12-25(a) the auto-restarting magnetron is realized by the cascade effect of two magnetrons operating in series connection.

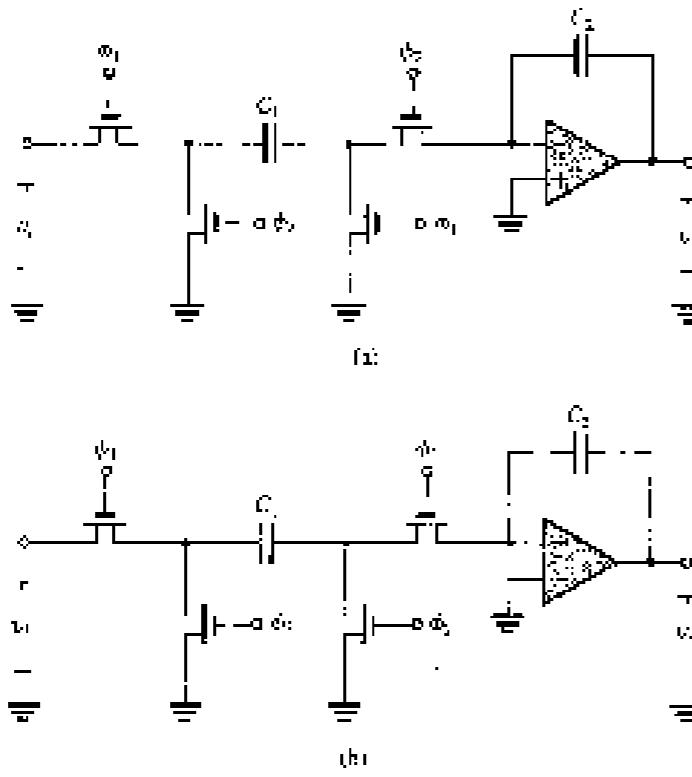


FIGURE 12.36 A pair of complementary switch-capacitor integrators. (a) Non-inverting switch capacitor integrator; (b) inverting switch capacitor integrator.

To realize a switched-capacitor biquad filter we therefore need a pair of complementary switched-capacitor integrators. Figure 12.36(a) shows a noninverting, or positive, integrator circuit. The reader is urged to follow the operation of the circuit during the two clock phases and thus show that it operates in much the same way as the basic circuit of Fig. 12.35(a), except for a sign reversal.

In addition to realizing a noninverting integrator function, the circuit in Fig. 12.36(b) is insensitive to stray capacitances; however, we shall not explore this point any further. The interested reader is referred to Schenmann, Ghosh, and Laker (1980). By reversal of the clock phases on two of the switches, the circuit in Fig. 12.36(b) is obtained. This circuit realizes the inverting integrator function, like the circuit of Fig. 12.35(b), but is insensitive to stray capacitances (which the original circuit of Fig. 12.35(b) is not). The pair of complementary integrators of Fig. 12.36 has become the standard building block in the design of switched capacitor filters.

Let us now consider the realization of a complete biquad circuit. Figure 12.37(a) shows the active-RC two-integrator-loop circuit studied earlier. By considering the cascade of integrator 2 and the inverter as a positive integrator, and then simply replacing each resistor by its switched-capacitor equivalent, we obtain the circuit in Fig. 12.37(b). Ignore the dot ping around the first integrator (i.e., the switched capacitor C_1) for the time being and note that the feedback loop indeed consists of one inverting and one noninverting integrator. Then note the phasing of the switched capacitor used for damping. Reversing the phases here would change the feedback to positive and move the poles to the right half of the s -plane.

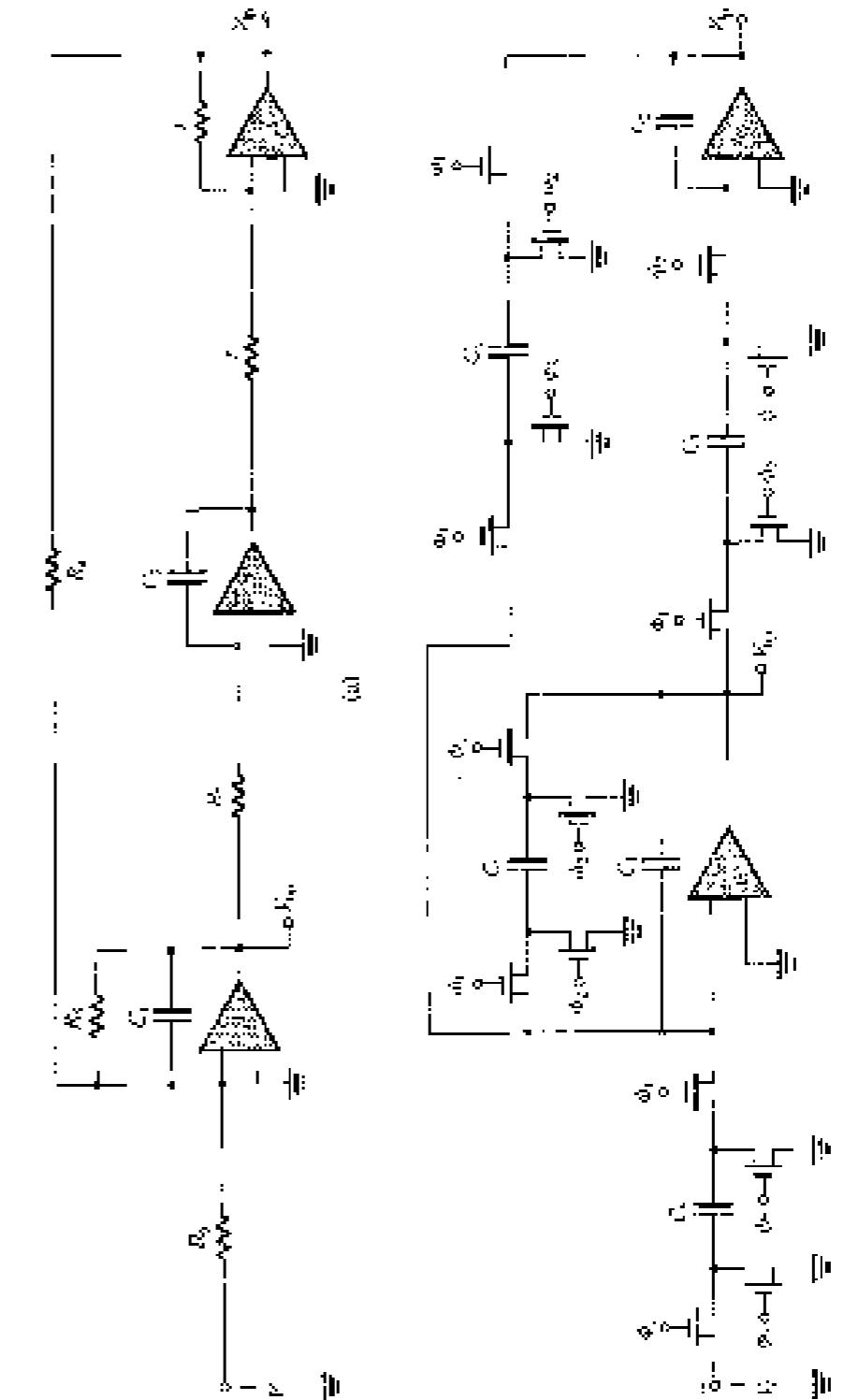


FIGURE 12.37 (a) A two-integrator-loop active-RC circuit and (b) its switched capacitor counterpart.

On the other hand, the phasing of the feed-in switched capacitor (C_2) is not that important; a reversal of phases would result only in an inversion in the sign of the function realized.

Having identified the correspondences between the active-RC biquad and the switched-capacitor biquad, we can now derive design equations. Analysis of the circuit in Fig. 12.37(a) yields

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_1}} \quad (12.92)$$

Replacing R_2 and R_1 with their SC equivalent values, that is,

$$R_2 = T_1/C_1 \quad \text{and} \quad R_1 = T_2/C_2$$

gives us of the SC equation

$$\omega_0 = \frac{1}{T_1 T_2 \sqrt{C_1 C_2}} \quad (12.93)$$

It is usual to select the time constants of the two integrators to be equal; that is,

$$\frac{T_1}{C_1} = \frac{T_2}{C_2} \quad (12.94)$$

If, further, we select the two integrating capacitors C_1 and C_2 to be equal,

$$T_1 = C_1 = C \quad (12.95)$$

then

$$C_1 + C_2 = KC \quad (12.96)$$

where from Eq. (12.93);

$$K = \alpha_1 T_1 \quad (12.97)$$

For the case of equal time constants, the Q factor of the circuit in Fig. 12.37(b) is given by K_2/R_2 . Thus the Q factor of the corresponding SC circuit in Fig. 12.37(c) is given by

$$Q = \frac{T_1/C_1}{T_2/C_2} \quad (12.98)$$

Thus C_2 should be selected from

$$C_2 = \frac{C_1}{Q} = \frac{KC}{Q} = \alpha_1 T_1 \frac{C}{Q} \quad (12.99)$$

Finally, the center frequency gain of the bandpass function is given by

$$\text{Center-frequency gain} = \frac{C_2}{C_1} = Q \frac{C_2}{\alpha_1 T_1 C} \quad (12.100)$$

12.10.9 A Final Remark

We have attempted to provide only an introduction to switched-capacitor filters. We have made it very simplifying assumptions, the most important being the switched-capacitor-to-resistor equivalence (Eq. 12.90). This equivalence is correct only at $f_s = \infty$ and is approximately correct for $f_s \gg f$. Switched-capacitor filters are, in fact, sampled-data networks whose analysis and design can be carried out exactly using z-transform techniques. The interested reader is referred to the bibliography.

12.11 TUNED AMPLIFIERS

In this section, we study a special kind of frequency-selective network, the LC-tuned amplifier. Figure 12.38 shows the general shape of the frequency response of a tuned amplifier. The techniques discussed apply to amplifiers with center frequencies in the range of a few hundred kilohertz to a few hundred megahertz. Tuned amplifiers find application in the radio-frequency (RF) and intermediate frequency (IF) sections of communications receivers and in a variety of other systems. It should be noted that the tuned-amplifier response of Fig. 12.38 is similar to that of the bandpass filter discussed in earlier sections.

As indicated in Fig. 12.38, the response is characterized by the center frequency ω_0 , the 3-dB bandwidth B , and the Q factor, which is usually measured as the ratio of the 3-dB bandwidth to the 3-dB bandwidth. In many applications, the 3-dB bandwidth is less than 5% of ω_0 . This narrow-band property makes possible certain approximations that can simplify the design process, as will be explained later.

The tuned amplifiers studied in this section are small-signal voltage amplifiers in which the transistors operate in the "class A" mode that is, the transistors conduct at all times. Tuned power amplifiers based on class C and other switching modes of operation are not studied in this book. For a discussion on the classification of amplifiers, refer to Section 4.1.

12.11.1 The Basic Principle

The basic principle underlying the design of tuned amplifiers is the use of a parallel LCR circuit as the load, or as the input of a BPF or a FB filter. This is illustrated in Fig. 12.39 with a MOSFET amplifier having a tuned-circuit load. For simplicity, the bias details are not included. Since this circuit uses a single tuned circuit, it is known as a single-tuned amplifier. The amplifier equivalent circuit is shown in Fig. 12.39(b). Here R denotes the

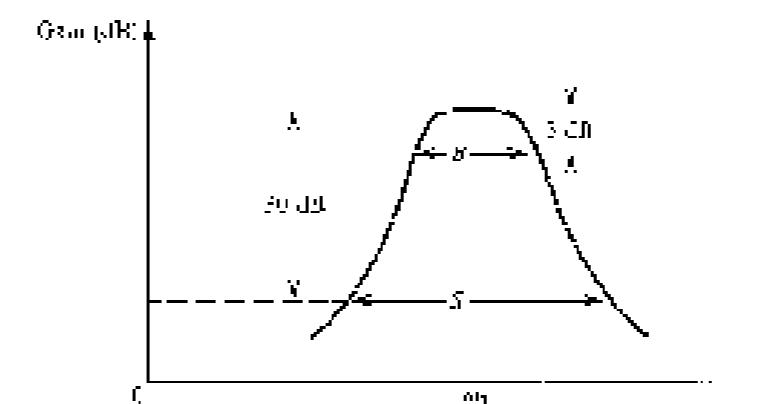


FIGURE 12.38. Frequency response of a tuned amplifier.

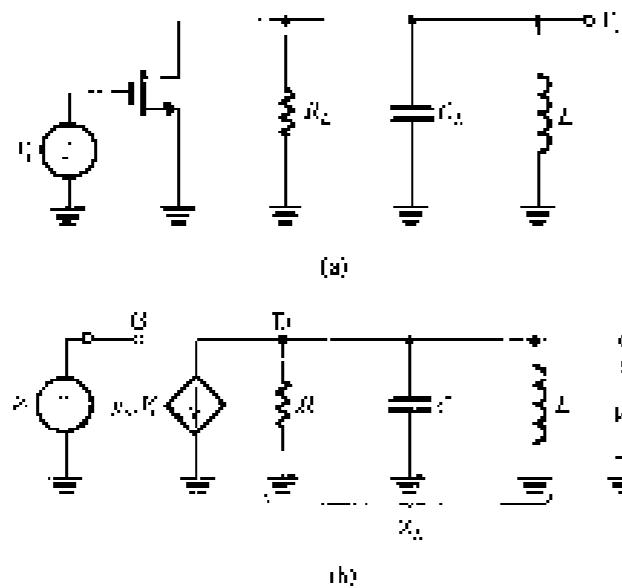


FIGURE 12.39 The basic principle of tuning a circuit is illustrated using a MOSFET with a non-linear load. Bias details are not shown.

parallel equivalent of R_o and the output resistance r_o of the FET, and C is the parallel equivalent of C_o and the FET output capacitance (usually very small). From the equivalent circuit we can write

$$\frac{V_o}{V_s} = \frac{-g_m C}{R_o} = \frac{-g_m V_i}{(R_o + 1/C + 1/L)}$$

Thus the voltage gain can be expressed as

$$\frac{V_o}{V_s} = \frac{g_m}{C} \frac{s}{s^2 + (1/CR) + 1/LC} \quad (12.101)$$

which is a second-order analysis function. Thus the tuned amplifier has a center frequency of

$$\omega_0 = 1/\sqrt{LC} \quad (12.102)$$

a 2-dB bandwidth of

$$B = \frac{1}{CR} \quad (12.103)$$

a Q factor of

$$Q = \omega_0/B = \omega_0/CR \quad (12.104)$$

and a center-frequency gain of

$$\frac{V_o(\omega_0)}{V_s(\omega_0)} = -g_m R \quad (12.105)$$

Note that the expression for the center-frequency gain could have been written by inspection. At resonance the reactances of L and C cancel one and the impedance of the parallel LC circuit reduces to R .

It is now left to design a tuned amplifier of the type shown in Fig. 12.30, having $\omega_0 = 1.5\text{MHz}$, 2.4kHz bandwidth, -10dB ad center frequency gain $= -10\text{dB}$. The FET available has at the bias point $x_s = 5\text{mA/V}$ and $r_o = 10\text{k}\Omega$. The output capacitance is negligibly small. Determine the values of R_2 , C , and L .

Solution

Center frequency gain $= -10 = -g_m R$. Thus $R = 2\text{k}\Omega$, since $k = R_1/r_o$, then $R_1 = 15\text{k}\Omega$.

$$L = 2\pi \times 10^6 = \frac{1}{C \omega_0}$$

Thus

$$C = \frac{1}{2\pi \times 10^6 \times 2 \times 10^6} = 7958 \text{ pF}$$

Since $\omega_0 = 2\pi \times 10^6 = 1/0.44$, we obtain

$$L = \frac{1}{4\pi^2 \times 7958 \times 10^{-12}} = 3.18 \mu\text{H}$$

12.11.2 Inductor Losses

The power loss in the inductor is usually represented by a series resistance r_s as shown in Fig. 12.40(a). However, rather than specifying the value of r_s , the usual practice is to specify the inductor Q factor at the frequency of interest.

$$Q_s = \frac{\omega_0 L}{r_s} \quad (12.106)$$

Typically, Q_s is in the range of 50 to 200.

The analysis of a tuned amplifier is greatly simplified by representing the inductor loss by a parallel resistance R_s as shown in Fig. 12.40(b). The relationship between R_s and Q_s can be found by writing for the admittance of the circuit in Fig. 12.40(a).

$$\begin{aligned} Y(j\omega_0) &= \frac{1}{r_s + j\omega_0 L} \\ &= \frac{1}{j\omega_0 L} \frac{1}{1 - j(1/Q_s)} = \frac{1}{j\omega_0 L} \frac{1 + j(1/Q_s)}{1 + (1/Q_s)^2} \end{aligned}$$

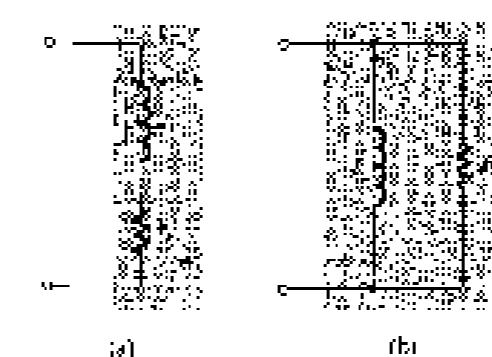


FIGURE 12.40 Inductor equivalent circuits.

For $Q_0 \gg 1$,

$$V_{T1}(j\omega_0) = \frac{1}{jQ_0 L} \left(1 + j\frac{1}{Q_0} \right) \quad (12.107)$$

Equating this to the admittance of the circuit in Fig. 12.40(b) gives

$$Q_0 = \frac{R_L}{\omega_0 L} \quad (12.108)$$

or, equivalently,

$$R_L = \omega_0 L Q_0 \quad (12.109)$$

Finally, it should be noted that the coil Q factor places an upper limit on the value of Q achievable by the tuned circuit.**EXERCISE**

12.11.2 The circuit in Example 12.4 has $Q_0 = 50$, $R_L = 1000 \Omega$, and $\omega_0 = 10^4 \text{ rad/s}$. Find the value of L required to obtain the required selectivity. Assume that the load is matched and losses in components ignored.

12.11.3 Use of Transformers

In many cases it is found that the required value of inductance is not practical, in the sense that coils with the required inductance might not be available with the required high values of Q . A simple solution is to use a transformer to effect an impedance change. Alternatively, a tapped coil, known as an autotransformer, can be used, as shown in Fig. 12.41. Provided the two parts of the inductor are tightly coupled, which can be achieved by winding on a ferrocore, the transformation ratio n is shown bold. The result is that the tuned circuit seen between terminals 1 and 1' is equivalent to that in Fig. 12.39(b). For example, if the ratio $n = 3$ is used in the amplifier of Example 12.4, then a coil with a inductance $L = 1.9 \times 1.18 = 2.36 \mu\text{H}$ and a capacitance $C = 7358/3 = 2460 \text{ pF}$ will be required. Both these values are more practical than the original ones.

In applications that involve coupling the output of a tuned amplifier to the input of another amplifier, the tapped coil can be used to raise the effective input resistance of the latter amplifier stage. In this way, one can avoid reduction of the overall β . This point is illustrated in Fig. 12.42 and in the following exercises.

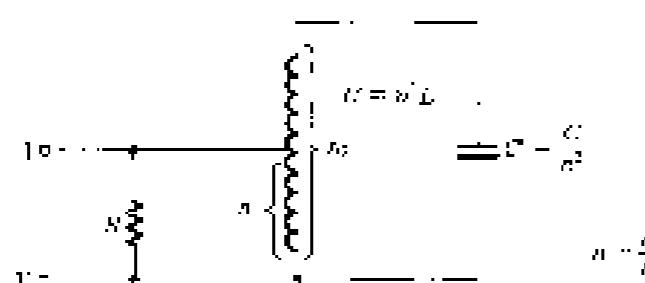


FIGURE 12.41 A tapped-coil circuit is used as an impedance transformer to allow a low-Q coil inductor, L_1 , and a parallel capacitance, C_1 .

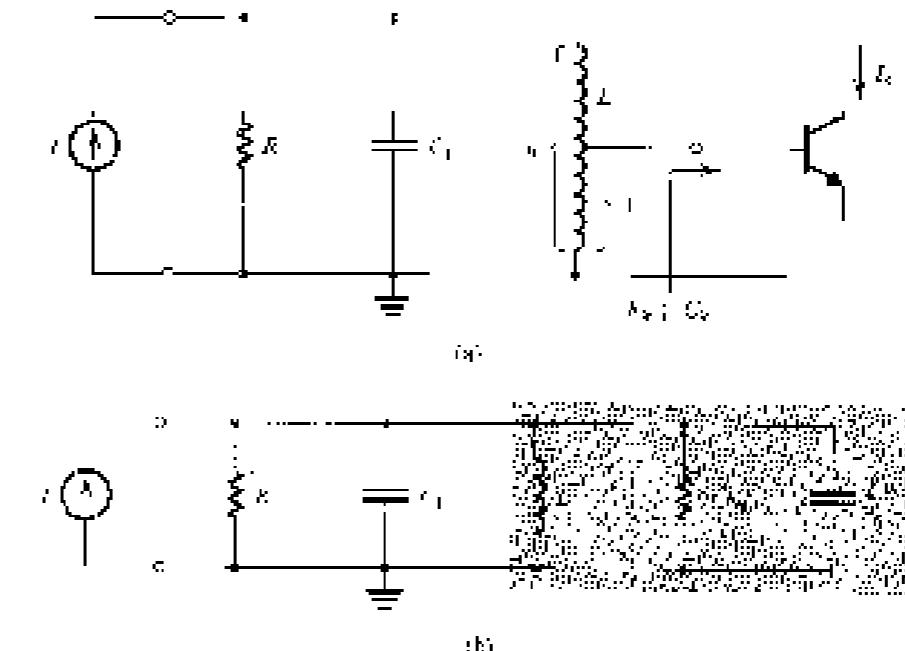


FIGURE 12.42 (a) The output of a tuned amplifier is coupled to the input of another amplifier via a tapped coil. (b) An equivalent circuit. Note that the use of a tapped coil increases the effective load β -value of the second amplifier stage.

EXERCISE

12.11.4 Consider the circuit in Fig. 12.42(a), with all coupling being unity. Let $\omega_0 = 2 \pi \times 10^4 \text{ rad/s}$, $R_A = 100 \Omega$, $R_L = 1000 \Omega$, and $C_1 = 100 \text{ pF}$. What is the required value of L to obtain a selectivity of 100? Assume that the β -value of the BJT is 100, and that the load β -value is 1000. Hint: Use the method of Example 12.4.

12.11.5 The circuit in Fig. 12.42(a) is exactly the same, except the source V_A is replaced by a signal source in Fig. 12.42(b). Find the value of V_A that allows the conditions to be met.

12.11.6 Use the method of Exercise 12.11 to find the required value of L and the current gain β of a second-stage BJT in a BPF. Assume that the load β -value is 1000. Hint: Use the method of Example 12.4.

12.11.4 Amplifiers with Multiple Tuned Circuits

The selectivity achieved with the single-tuned circuit of Fig. 12.41 is not sufficient in many applications, in particular, in the IF amplifier of a radio or a TV receiver. Greater selectivity is obtained by using additional tuned stages. Figure 12.43 shows a BPF with tuned circuits at the input and the output.¹ In this circuit the bias details are shown, from which we note that biasing is quite similar to the classical arrangement employed in low-frequency

¹ Note that because the output of one of a cascade of tuned circuits, an input current (and its partner, the voltage across it) is utilized.

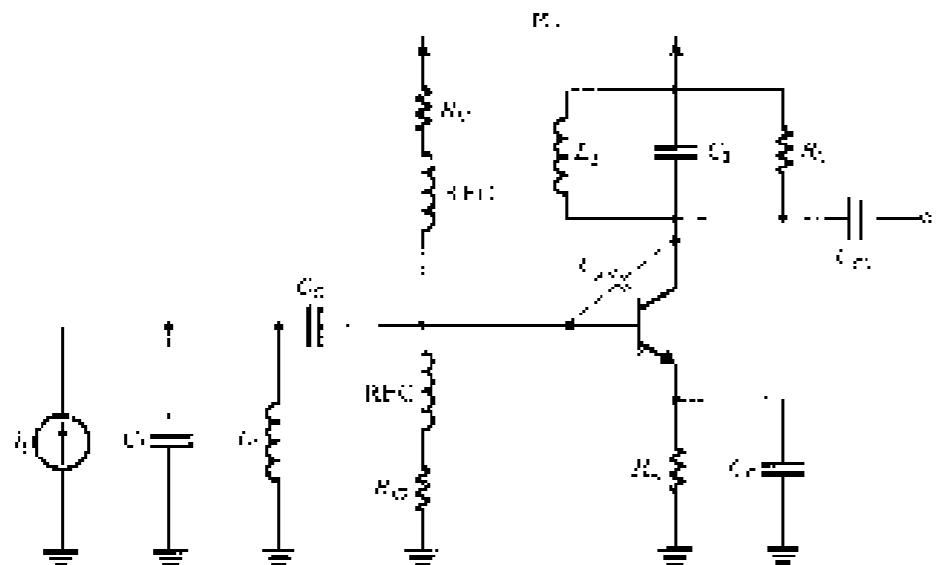


FIGURE 12.43 A BJT amplifier with tuned circuits at the input and the output.

discrete-circuit design. However, to avoid the loading effect of the bias resistors R_B and R_E on the input tuned circuit, a radio-frequency choke (RFC) is inserted in series with each resistor. Such chokes have high impedances at the frequencies of interest. The use of RFCs in biasing tuned RF amplifiers is common practice.

The analysis and design of the double-tuned amplifier of Fig. 12.43 is complicated by the Miller effect¹² due to capacitance C_E . Since the load is not simply resistive, as was the case in the amplifiers studied in Section 6.4.4, the Miller impedance at the input will be complex. This reflected impedance will cause detuning of the input circuit as well as "skewing" of the response of the input circuit. Needless to say, the coupling introduced by C_F makes tuning for alignment of the amplifier quite difficult. Worse still, the capacitor C_F can cause oscillations to occur [see Gray and Searle (1969) and Problem 12.75].

Methods exist for neutralizing the effect of C_F using additional circuits arranged to feed back a current equal and opposite to that through C_F . An alternative, and preferred, approach is to use circuit configurations that do not suffer from the Miller effect. These are discussed later. Before leaving this section, however, we wish to point out that circuits of the type shown in Fig. 12.43 are usually designed utilizing the parameter model of the BJT (see Appendix B). This is done because here, in view of the fact that C_E plays a significant role, the y -parameter model makes the analysis simpler (in comparison to that using the hybrid π model). Also, the y parameters can easily be measured at the particular frequency of interest (ω_0). For narrow-band amplifiers, the assumption is usually made that the y parameters remain approximately constant over the passband.

12.11.5 The Cascode and the CC-CB Cascade

From our study of amplifier frequency response in Chapter 6 we know that two amplifier configurations do not suffer from the Miller effect. These are the cascode configuration and

¹² Here we use "Miller effect" to refer to the effect of the feedback capacitor C_F in reflecting back an input impedance that is a function of the input frequency in radians.

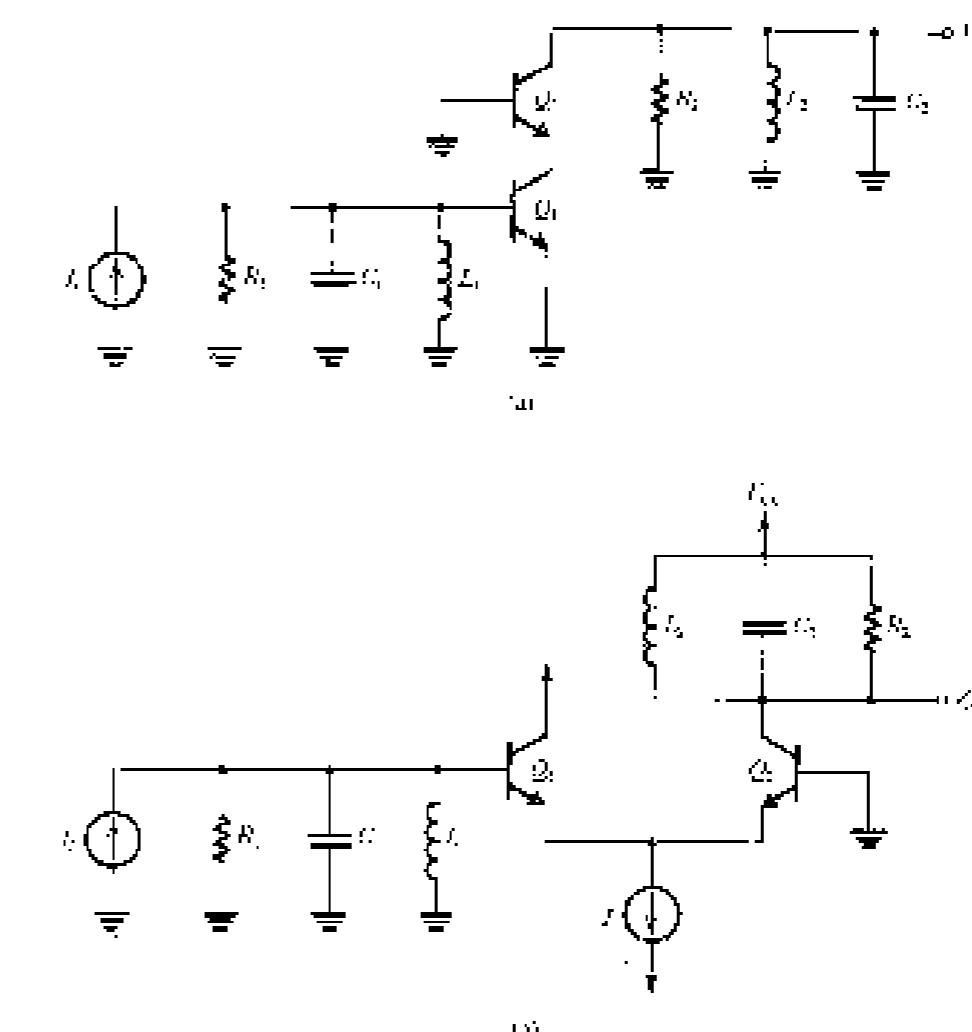


FIGURE 12.44 Two tuned amplifier configurations that do not suffer from the Miller effect. (a) cascode and (b) a current-coupled common-base cascade. (Once the bias circuitry is established, it is not shown.)

the common-collector configuration base circuit. Figure 12.44 shows tuned amplifiers based on these two configurations. The CC-CB cascade is usually preferred in IC implementations because its differential structure makes it suitable for IC biasing techniques. (Note that the biasing details of the cascode circuit are not shown in Fig. 12.44(a). Biasing can be done using arrangements similar to those discussed in earlier chapters.)

12.11.6 Synchronous Tuning

In the design of a tuned amplifier with multiple tuned circuits the question of the frequency to which each circuit should be tuned arises. The objective, of course, is for the overall response to exhibit high-passband flatness and sharp selectivity. To investigate this question, we shall assume that the overall response is the product of the individual responses, in other words, that the stages do not interact. This can easily be achieved using circuits such as those in Fig. 12.4.

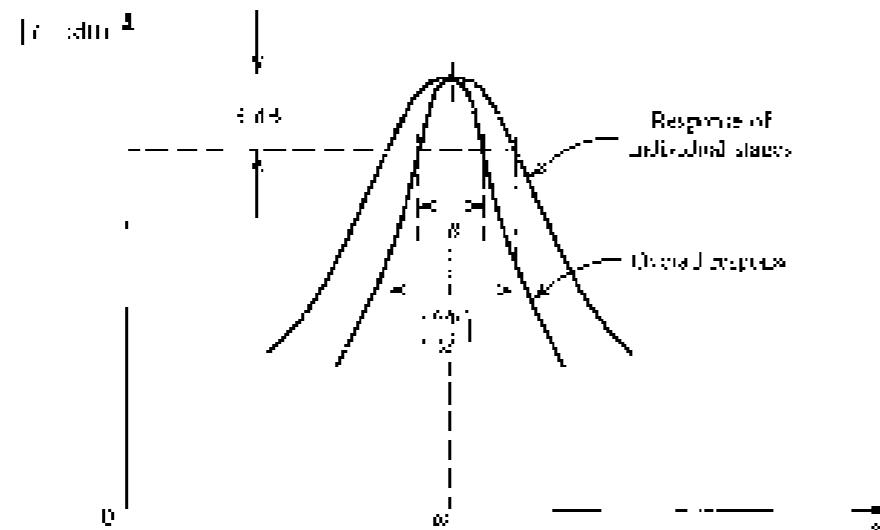


FIGURE 12.45 Frequency response of a synchronously tuned filter.

Consider first the case of N identical resonant circuits, known as the synchronously tuned case. Figure 12.45 shows the response of an individual stage and that of the cascade. Observe the bandwidth "shrinkage" of the overall response. The 3-dB bandwidth B of the overall amplifier is related to that of the individual tuned circuit, ω_0/Q , by (see Problem 12.15)

$$B = \frac{\omega_0}{Q} \sqrt{2^{1/N} - 1} \quad (12.110)$$

The factor $\sqrt{2^{1/N} - 1}$ is known as the narrow-band shrinkage factor. Given B and N , we can use Eq. (12.110) to determine the bandwidth required of the individual stages, ω_0/Q .

EXERCISE

12.11.6 Design a bandpass filter with a center frequency of $\omega_0 = 10^4 \text{ rad/s}$ and a bandwidth of $B = 1000 \text{ rad/s}$. The filter is to be implemented using $N = 4$ identical second-order sections. Using the narrow-band approximation, determine the required value of ω_0/Q .
Ans: $2\sqrt{2}(10^4 + 1000)/10^4 = 2.85 \times 10^3$

12.11.7 Stagger-Tuning

A much better overall response is obtained by stagger-tuning the individual stages, as illustrated in Fig. 12.46. Stagger-tuned amplifiers are usually designed so that the overall response exhibits *resonance/interference* around the center frequency ω_0 . Such a response can be obtained by transforming the response of a maximally flat Butterworth low-pass filter up the frequency axis to ω_0 . We show how this can be done.

The transfer function of a second-order bandpass filter can be expressed in terms of its poles as

$$T(s) = \frac{\omega_0^2}{\left(s + \frac{\omega_0}{2Q} + j\omega_0\right)\left(s + \frac{\omega_0}{2Q} - j\omega_0\right)} \quad (12.111)$$

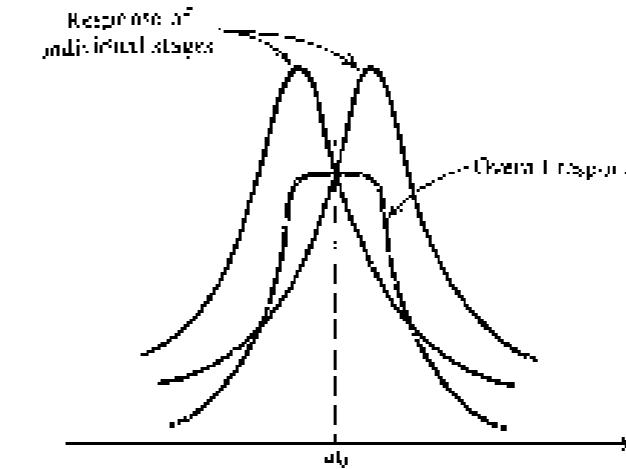


FIGURE 12.46 Stagger tuning: the individual resonant circuits can result in an overall response which is much narrower than that obtained with synchronous tuning (Fig. 12.45).

For a narrow-band filter, $Q \approx 1$, and for values of s in the neighborhood of $j\omega_0$ (see Fig. 12.47): the second factor in the denominator is approximately $(s + j\omega_0 - 2i)$. Hence Eq. (12.111) can be approximated in the neighborhood of $j\omega_0$ by

$$T(s) \approx \frac{\omega_0^2/2}{s + \omega_0/2 + j\omega_0} = \frac{\omega_0^2/2}{(s - j\omega_0) + \omega_0/2Q} \quad (12.112)$$

This is known as the narrow-band approximation.⁵ Note that the magnitude response, for $s = j\omega$, has a peak value of $\omega_0/(2\sqrt{1 + 1/Q}) = \omega_0$, as expected.

Now consider a first-order low-pass network with a single pole at $p = -\omega_0/2Q$ (we use p to denote the complex frequency variable for the low-pass filter). Its transfer function is

$$T(p) = \frac{K}{p + \omega_0/2Q} \quad (12.113)$$

where K is a constant. Comparing Eqs. (12.112) and (12.113) we note that they are identical for $p = s - j\omega_0$, or, equivalently,

$$s = p + j\omega_0 \quad (12.114)$$

This result implies that the response of the second-order bandpass filter in the neighborhood of its center frequency $s = j\omega_0$ is identical to the response of a first-order low-pass filter with a pole at $(-\omega_0/2Q)$ in the neighborhood of $p = 0$. Thus the bandpass response can be obtained by shifting the pole of the low-pass prototype and adding the complex conjugate pole, as illustrated in Fig. 12.17(a). This is called a low-pass-to-bandpass transformation for narrow-band filters.

The transformation $p = s - j\omega_0$ can be applied to low-order filters of order greater than one. For instance, we can transform a maximally flat second-order low-pass filter ($Q = 1/\sqrt{2}$) to

⁵ The bandpass response is symmetrically symmetrical around the center frequency ω_0 . That is, each pair of frequencies ω_0 and $\omega_0 + \Delta\omega$ of the magnitude response is equal in magnitude by $\omega_0/\omega_0 + \Delta\omega$. For high Q , the symmetry becomes increasingly distorted as frequency increases. Then, certain frequencies with the same magnitude response are more equally spaced. Even so, this is not true for high-order bandpass filters designed using the transformation presented in this section.

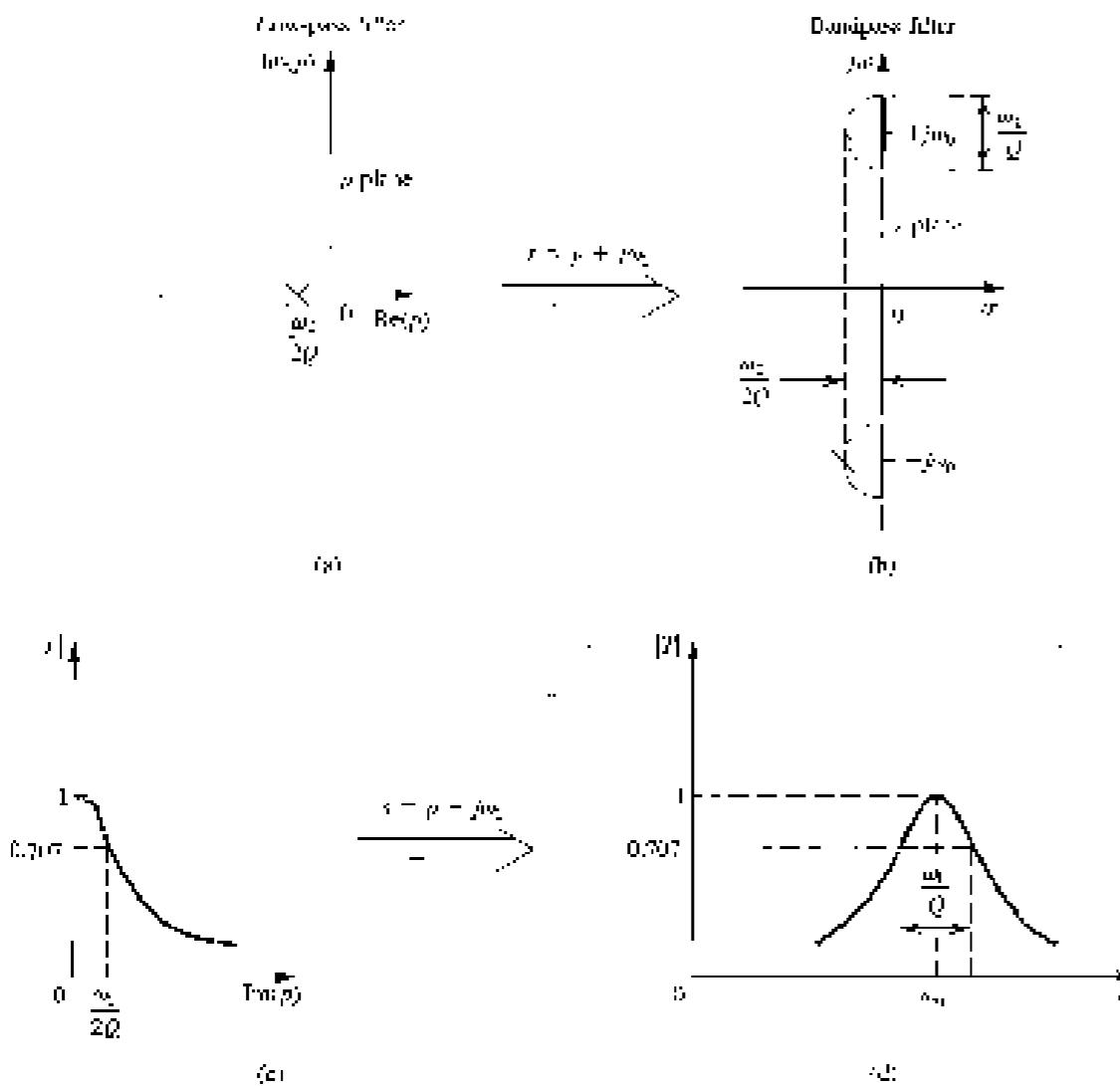


FIGURE 12.47 Obtaining a second-order narrow-band bandpass filter by transforming a first-order low-pass filter: (a) Pole of the first-order filter in the p -plane. (b) Applying the transformation $p = p - j\omega_0$, i.e., $j\omega_0$ is preconjugate pole, results in the poles of the second-order bandpass filter. (c) Magnitude response of the first-order low-pass filter. (d) Magnitude response of the second-order bandpass filter.

obtain a maximally flat bandpass filter. If the 3 dB bandwidth of the bandpass filter is to be R rad/s, then the low-pass filter should have a 3 dB frequency (and thus a pole frequency) of $(R/\sqrt{2})$ rad/s, as illustrated in Fig. 12.48. The resulting fourth-order bandpass filter will be a stagger-tuned one, with its two tuned circuits (refer to Fig. 12.18) having

$$\omega_0 = \omega_0 - \frac{R}{2\sqrt{2}} \quad R = \frac{\theta}{\sqrt{2}} \quad Q_1 = \frac{\sqrt{2}\theta}{R} \quad (12.115)$$

$$\omega_0 = \omega_0 - \frac{R}{2\sqrt{2}} \quad R = \frac{\theta}{\sqrt{2}} \quad Q_2 = \frac{\sqrt{2}\theta}{R} \quad (12.116)$$

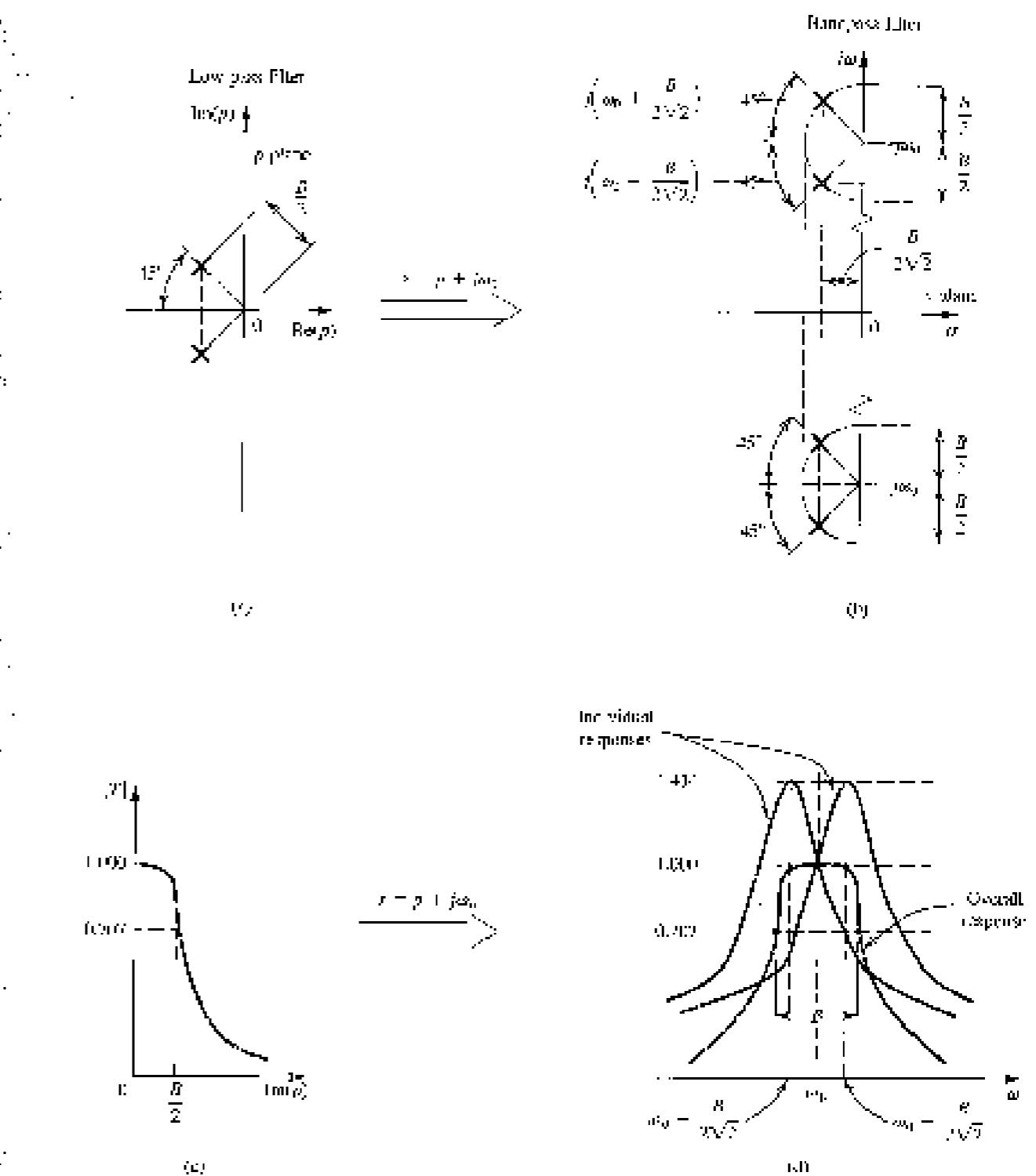


FIGURE 12.48 Obtaining the poles and the frequency response of a four-tuned staggered narrow-band bandpass amplifier for obtaining a second-order low-pass, maximally flat response.

Note that for the overall response to have a normalized center-frequency gain of unity, the individual responses to have equal center-frequency gains of $\sqrt{2}$, as shown in Fig. 12.8(a).

EXERCISES

- 12.56 A compensator is required for the feedback capacitors in Example 12.20. It is required that the overall voltage gain of 1000 for each of the two stages, (Recall that ideal op-amps are used.)
 12.57 Consider the two-stage filter design in Example 12.20. If the second stage is replaced by a single operational amplifier, the total filter order will be reduced to three. Design the circuit and determine the individual pole frequencies.

12.12 SPICE SIMULATION EXAMPLES

Circuit simulation is employed in filter design for at least three purposes: (1) to verify the correctness of the design using ideal components, (2) to investigate the effects of the nonideal characteristics of the op-amps on the filter response, and (3) to determine the percentage of circuits fabricated with practical components, whose values have specified tolerance characteristics, that meet the design specifications (this percentage is known as the yield). In this section, we present two examples that illustrate the use of SPICE for the first two purposes. The third area of computer-aided design, though very important, is a rather specialized topic, and is considered beyond the scope of this textbook.

VERIFICATION OF THE DESIGN OF A FIFTH-ORDER CHEBYSHEV FILTER

Our first example shows how SPICE can be utilized to verify the design of a fifth-order Chebyshev filter. Specifically, we simulate the operation of the circuit whose component values were obtained in Example 12.20. The complete circuit is shown in Fig. 12.49(a). It consists of a cascade of two second-order simulated LCR resonators using the *Analog* circuit and a first-order op-amp-RC circuit. Using PSpice, we would like to compare the magnitude of the filter response with that computed analytically from its transfer function. Here, we note that PSpice can also be used to perform the latter task by using the Laplace transfer function block in the *Advanced-models* library.

Since the purpose of the simulation is simply to verify the design, we assume ideal components. For the op-amps, we utilize a near ideal model, namely, a voltage-controlled voltage source (VCVS) with a gain of 10^6 V/V, as shown in Fig. 12.49(b).¹⁴

¹⁴ SPICE models for the op-amps are described in Section 2.3.

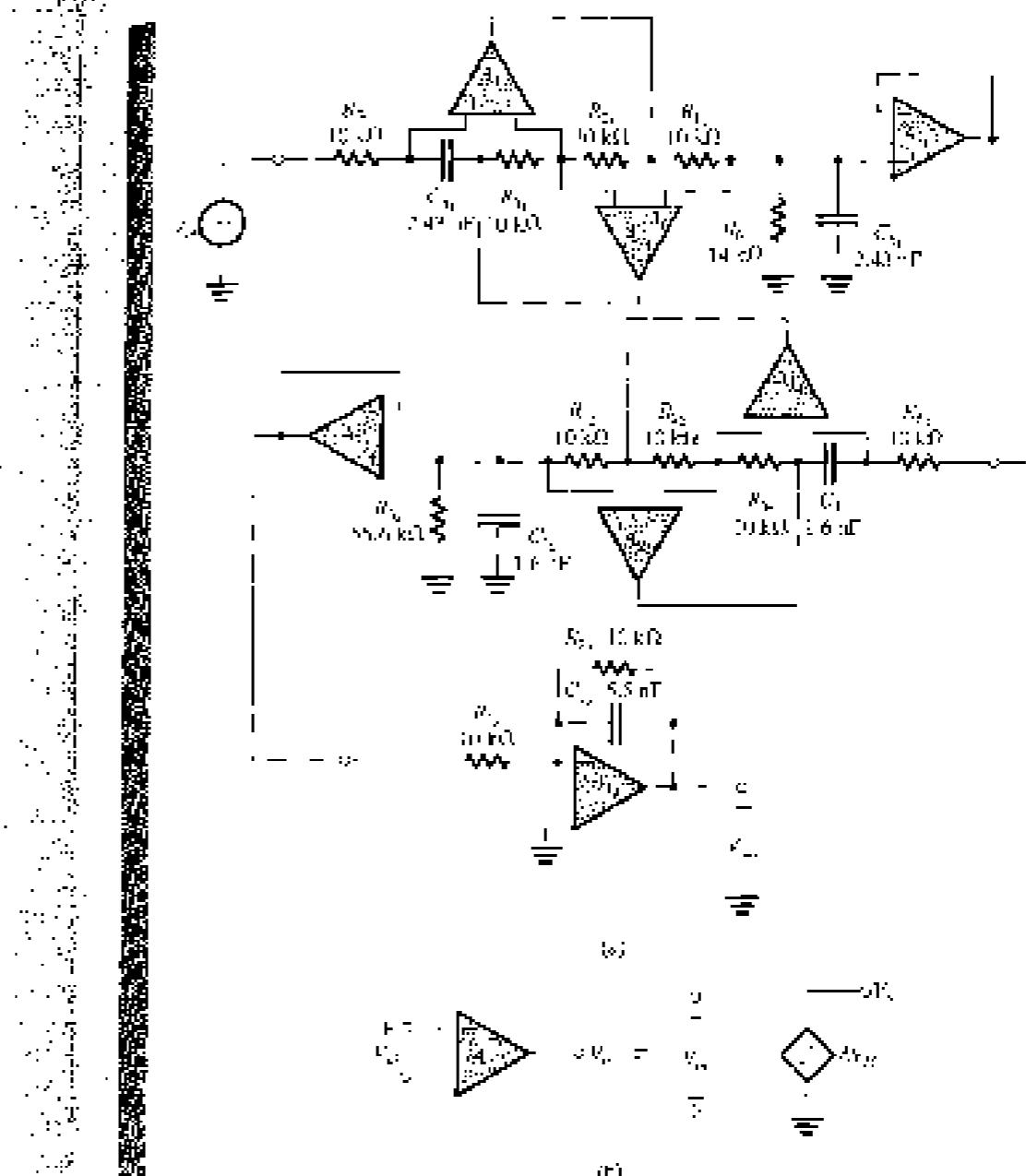


FIGURE 12.49 Circuits for Example 12.5. (a) Filter for Chebyshev filter implemented by a cascade of two second-order LCR resonators and a single first-order op-amp-RC circuit. (b) Op-amp model using a VCVS.

In SPICE, we apply a 1-V ac signal at the filter input, perform an ac-analysis simulation over the range 1 Hz to 20 kHz, and plot the output voltage magnitude versus frequency, as shown in Fig. 12.50. Both an expanded view of the passband and a view of the entire magnitude response are shown. These results are almost identical to those computed directly from the loop transfer function, thereby verifying the correctness of the design.

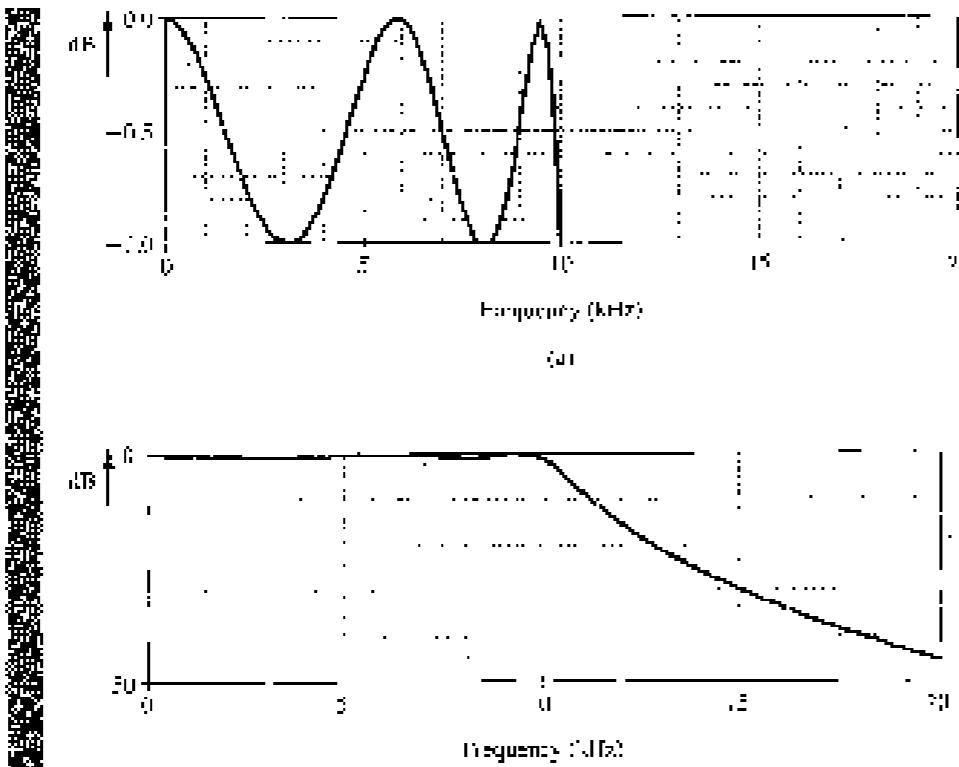


FIGURE 12.50 Magnitude response of the fifth-order lowpass filter circuit shown in Fig. 12.29(b) for an expanded view of the passband region. (b) A plot of both the passband and stopband regions.

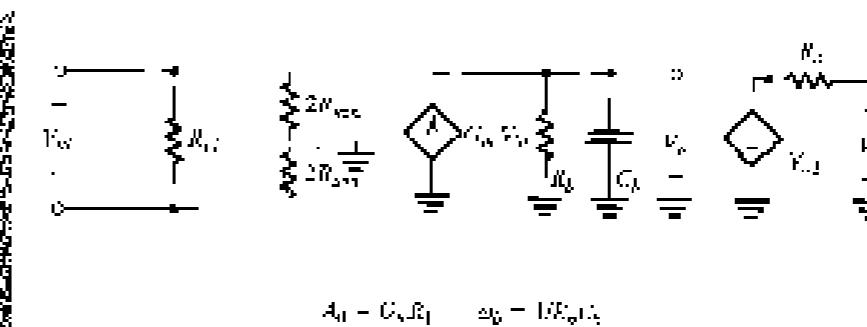


FIGURE 12.51 One-pole equivalent circuit model of an op-amp operated within its linear region.

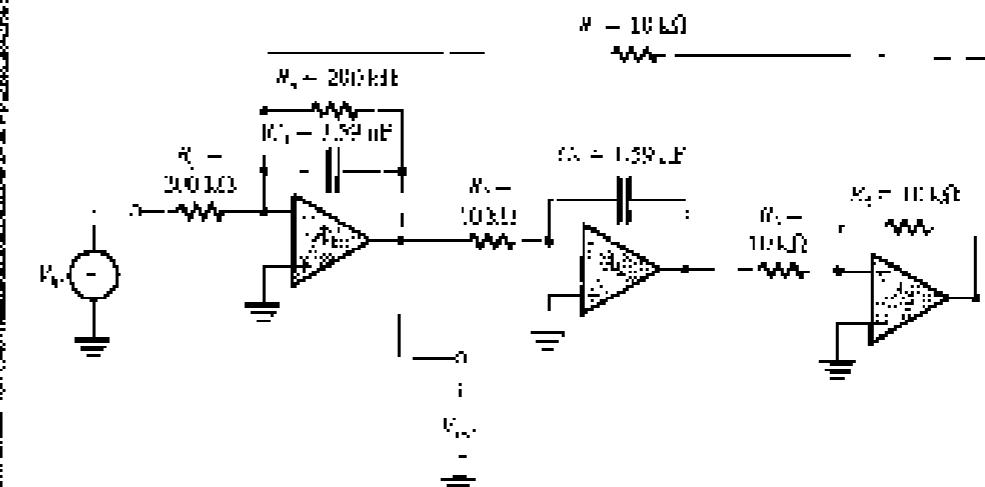


FIGURE 12.52 Circuit for Example 12.5. Second-order bandpass filter implemented with a Tait-Bethune circuit having $f_L = 10\text{ kHz}$, $Q = 20$, and unity center-frequency gain.

INVESTIGATING THE EFFECT OF FINITE OP-AMP BANDWIDTH ON THE OPERATION OF THE TWO-INTEGRATOR-LOOP FILTER

In this example, we investigate the effect of the finite bandwidth of practical op-amps on the response of a two-integrator-loop bandpass filter utilizing the Tait-Bethune circuit of Fig. 12.25(b). The circuit is designed to provide a bandpass response with $f_L = 10\text{ kHz}$, $Q = 20$, and a unity center-frequency gain. The op-amps are assumed to be of the 741 type. Specifically, we model the terminal behavior of the op-amp with the single time constant linear network shown in Fig. 12.51. Since the analysis performed here is a small-signal (ζ) and uses that ignores nonlinearities, no nonlinearities are included in this op-amp representation. (In the event of op-amp nonlinearities are to be investigated, a transient analysis should be performed.) The following values are used for the parameters of the op-amp model used in Fig. 12.51:

$$\begin{aligned} R_o &= 2\text{ M}\Omega & R_{in} &= 500\text{ M}\Omega & R_s &= 75\text{ k}\Omega \\ \omega_n &= 0.09\text{ rad/V} & R_v &= 1.12 \times 10^7\text{ }\Omega & C_v &= 30\text{ pF} \end{aligned}$$

These values result in the specified input and output resistance of the 741-type op-amp. Further, they provide a dc gain $A_0 = 3.52 \times 10^3$ V/V and a 3-dB frequency (f) of 11 Hz, again equal to the values specified for the 741. Note that the selection of the individual values of R_{in} , R_o , and C_v is immaterial as long as $C_v R_o = A_0$ and $C_v R_{in} = 1/2\pi f_0$.

The Tait-Bethune circuit simulator is shown in Fig. 12.53. The circuit is simulated in PSPice for two cases: (1) assuming 741-type op-amps and using the linear model specified in Fig. 12.51; and (2) assuming ideal op-amps with dc gain of $A_0 = 10^5$ V/V and using the near-ideal model in Fig. 12.49. In both cases, we apply a 1-V ac signal at the filter input, perform an ac analysis simulation over the range 8 kHz to 12 kHz, and plot the output-voltage magnitude versus frequency.

The simulation results are shown in Fig. 12.53, from which we observe the significant deviation between the response of the filter using the 741 op-amp and that using the near-ideal op-amp model. Specifically, the response with practical op-amps shows a deviation in the center

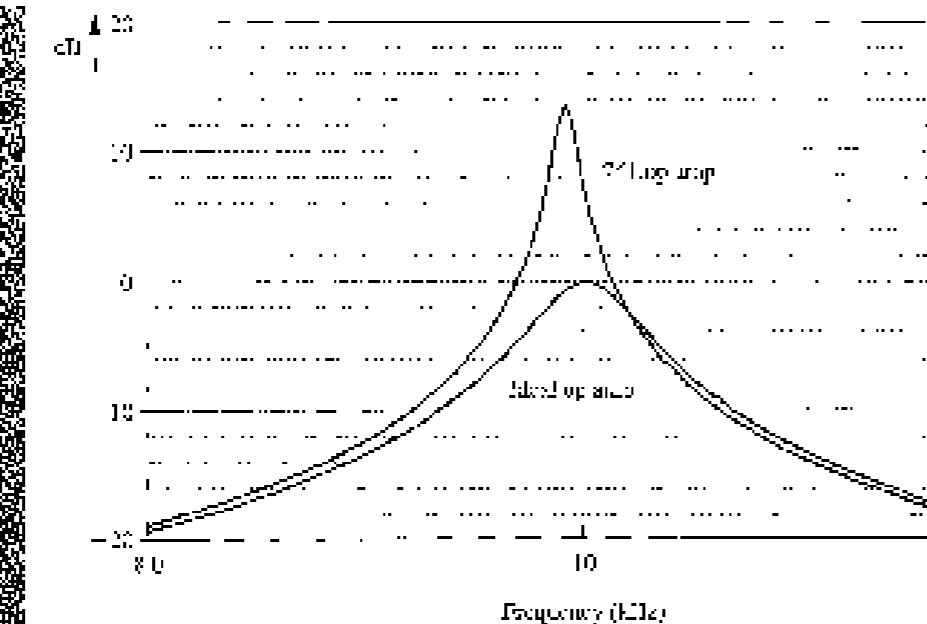
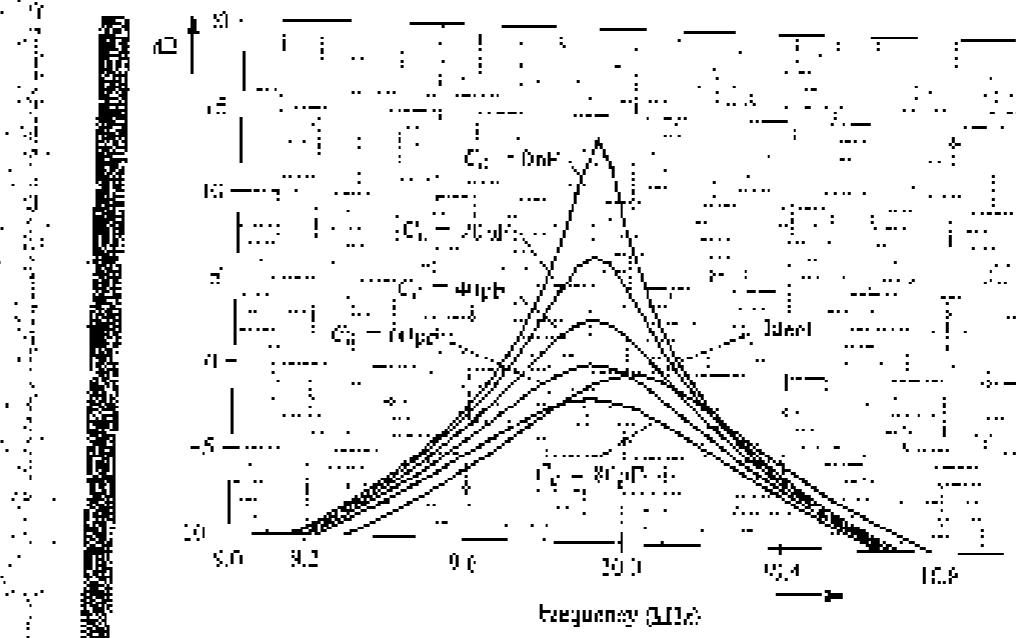
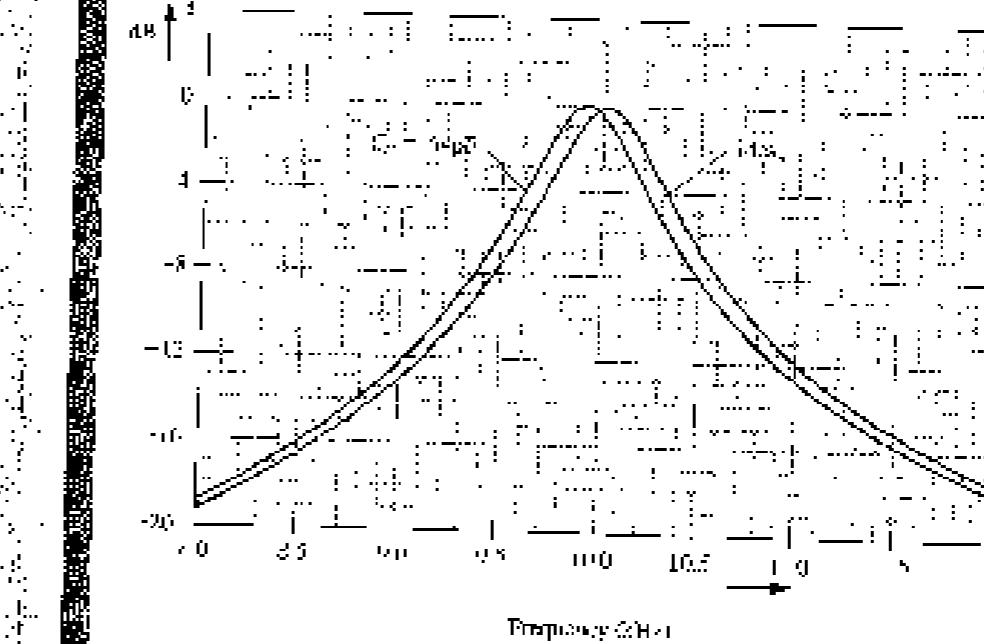


FIGURE 12.53 Comparing the magnitude response of the Tow-Thomas biquad ($\omega_0 = 2\pi$) (shown in Fig. 12.40) with two op-amps, with the ideal magnitude response. This is due to the effect of finite gain and bandwidth of the op-amp on the frequency response of the Tow-Thomas biquad circuit.

frequency of about -300 Hz, and a reduction in the -3-dB bandwidth from 500 Hz to about 110 Hz. Thus, in effect, the filter Q factor has increased from the ideal value of $\sqrt{2}$ to about 22 . This phenomenon, known as Q enhancement, is predictable from an analysis of the two-interactive-loop biquad with the finite op-amp bandwidth taken into account (see Sodha and Baschek (1978)). Such an analysis shows that Q enhancement occurs as a result of the excess phase lag introduced by the finite op-amp bandwidth. The theory also shows that the Q enhancement effect can be compensated for by introducing a compensation capacitor across resistor R_1 . To investigate the potential of such a compensation technique, we repeat the PSpice calculation with various compensation values. The results are displayed in Fig. 12.54(a). We observe that as the compensation capacitor is increased from 0 pF, both the filter Q and the resonance peak of the filter response move closer to the desired values. It is evident, however, that a compensation capacitance of 60 pF causes the response to deviate further from the ideal. Thus, optimum compensation is obtained with a capacitance value between 60 and 80 pF. Further experimentation using PSpice enabled us to determine that such an optimum is obtained with a compensation capacitance of 64 pF. The corresponding response is shown, together with the ideal response, in Fig. 12.54(b). We note that although the filter Q has been reduced to its ideal value, 127° remains a deviation in the center frequency. We shall not pursue this matter any further as we only intend to use it to present a detailed study of the design of two-interactive-loop biquads, rather than to illustrate the application of SPICE in investigating the nonideal performance of active filters, which is beyond the scope of this book.



(a)



(b)

FIGURE 12.54 (a) Magnitude response of the Tow-Thomas biquad circuit with different values of compensation capacitors. For comparison, the ideal response is also shown. (b) Comparing the magnitude response of the Tow-Thomas biquad circuit using a 64 -pF compensation capacitor with the ideal response.

SUMMARY

- A third-order low-pass filter with a transfer function $T(s) = V_o(s)/V_i(s)$. For physical frequencies, the total transmission is expressed as $|T(j\omega)| = |T(j\omega)|e^{-j\theta(\omega)}$. The magnitude of transmission can be expressed in decibels, relating either the gain margin $\text{margin} = -20 \log|T|$ or the attenuation function $A(\omega) = -20 \log|T|$.
- The transmission characteristics of filters are specified in terms of the edges of the passbands and the stopbands; the maximum allowed variation in passband transmission, A_{max} (dB); and the minimum attenuation required in the stopband, A_{min} (dB). In some applications, the phase characteristics are also specified.
- The filter transfer function can be expressed as the ratio of two polynomials in s ; the degree of the denominator polynomial, N , is the filter order. The N roots of the denominator polynomial are the poles (natural modes).
- To obtain a highly selective response, the poles are complex and appear in conjugate pairs (except for one real pole when N is odd). The zeros are placed on the $j\omega$ axis in the stopband(s) including $\omega = 0$ and $\omega = \infty$.
- The Butterworth filter approximation provides a low-pass response that is maximally flat at $\omega = 0$. The transmission decreases monotonically as ω increases, reaching 0 dB at $\omega = \omega_c$, where all transmission zeros lie. Eq. (12.11) gives $|T|$, where ϵ is given by Eq. (12.14) and the corner N is determined using Eq. (12.13). The poles are found using the graphical construction of Fig. 12.10, and the quality factor is given by Eq. (12.6).
- The Chebyshev filter approximation provides a low-pass response that is minimum in the passband with the transmission decreasing monotonically in the stopband. All the transmission zeros are $\omega = \infty$. Eq. (12.17) gives $|T|$ in the passband and Eq. (12.15) gives $|T|$ in the stopband, where ϵ is given by Eq. (12.2). The order N can be determined using Eq. (12.23). The poles are given by Eq. (12.21) and the transfer function by Eq. (12.24).
- Figures 12.13 and 12.14 provide a summary of first-order filter functions and their realizations.
- Figure 12.16 provides the characteristics of seven special second-order filtering functions.
- The second-order LCR resonator of Fig. 12.13c realizes a pair of complex-conjugate poles with $\omega_p = 1/\sqrt{LC}$ and $Q = \omega_p/RC$. This resonator can be used to realize the various special second-order filtering functions as shown in Fig. 12.18.
- By replacing the inductor or an LCR resonator with a compensated inductor, one can design the 4^{th} -order equivalent of

Fig. 12.20(a), the op-amp RC resonator of Fig. 12.20(b) is a corner. This resonator can be used to realize the various second-order filter functions as shown in Fig. 12.19. The design equations for these circuits are given in Table 12.1.

- Biquads based on the two-mesh-loop topology are the most versatile and popular active-filter filter structures. There are two varieties: the KHN circuit of Fig. 12.24(c), which realizes the LP, BP, and HP functions simultaneously and can be combined with a voltage-controlled amplifier of Fig. 12.28(b) to realize the notch and all-pass functions; and the Tow–Chebyshev circuit of Fig. 12.25(c), which also realize BP and LP functions simultaneously. Both biquads can be applied to the Tow–Chebyshev circuit to obtain the circuit of Fig. 12.26, which can be designed to realize any of the second-order functions (see Table 12.2).
- Single-output filters ($V_o(s)/V_i(s)$) are obtained by placing a bridged-T network in the negative feedback path of an op-amp. If the op-amp is ideal, the poles realized are at the same locations as the zeros of the RC network. The compensation information can be applied to the feedback loop to obtain single-pole feedback loops having identical poles. Differential-mode crossover is best avoided by keeping the input signal to circuit nodes that are connected to ground. SOTs are economical in their use of op-amps, but are sensitive to the op-amp nonidealities and are thus limited in low-Q applications ($Q < 10$).
- The classical sensitivity function

$$S_T = \frac{\partial \omega_p}{\partial \omega_p}$$

is a very useful tool in investigating how tolerate a filter circuit is to the unavoidable fixed values of component values and/or the nonidealities of the op-amps.

- State-space (St.) filters are based on the principle that a capacitor C , periodically switched between two circuit nodes at a frequency f_s , is equivalent to a resistance $R = 1/f_s$, connecting the two circuit nodes. St. filters can be fabricated in monolithic form using CMOS IC technology.
- Tuned couplers of the LC ladder circuits as loads or in the input of transistor amplifiers may be used in the design of the RF tuner and the IF amplifier in communication receivers. The cascode and the CC–CB cascade coupling topologies are frequently used in the design of mixers, up-converters, down-converters, and local oscillator circuits.
- By replacing the inductor or an LCR resonator with a compensated inductor, one can design the 4^{th} -order equivalent of

PROBLEMS

SECTION 12.1: FILTER TRANSMISSION, TYPES AND SPECIFICATION

- 12.1** The transfer function of a first-order low-pass filter (as that realized by an RC circuit) can be expressed as $T(s) = \omega_0/(s + \omega_0)$, where ω_0 is the 3-dB frequency of the filter. Given in Table 12.1 are the values of T , ω_0 , G , and margin at $0.3\omega_0$, ω_0 , $2\omega_0$, $5\omega_0$, $10\omega_0$, and $100\omega_0$.

- *12.2** A filter has the transfer function $T(s) = 1/(s + 1)(s + 10)$. Show that $T|_s=0 = 1/1 + 10^2$ and find an expression for its phase response $\phi(s)$. Calculate the values of ω and $\theta(\omega)$ at $\omega = 0.1$, 1, and 10 rad/s and then find the output corresponding to each of the following input signals:

- 3 sin 0.1 (value)
- 2 sin 2 (value)
- 2 sin 20 (value)

- 12.3** For the filter whose magnitude response is sketched (as the shaded curve) in Fig. 12.1 find T at $\omega = 0$, $\omega = \omega_0$, and $\omega = 10$, $A_{\text{max}} = 0.5$ dB, and $A_{\text{min}} = -40$ dB.

- 12.4** A low-pass filter is required to pass all signals within its passband, exceeding from 1 to 4 kHz, with a transmission variation of at most 10% (i.e., the ratio of the maximum to minimum transmission in the passband should not exceed 1.1). The transmission in the stopband, which extends from 5 kHz to ∞ , should not exceed 10% of the maximum passband transmission. What are the values of A_{max} , A_{min} , and the selectivity factor for this filter?

- 12.5** A low-pass filter is specified to have $A_{\text{max}} = 1$ dB and $A_{\text{min}} = 10$ dB. It is found that these specifications can be met with a single-coupled constant-RK circuit having a time constant of 1 ms. Use the approximation of unity. What must ω_0 and ω_1 of this filter be? What is the selectivity factor?

- 12.6** Sketch transmission specifications for a high-pass filter having a passband defined by $1/2$ to 2 kHz and a stopband defined by $f > 1, $A_{\text{max}} = 0.5$ dB, and $A_{\text{min}} = 50$ dB.$

- 12.7** Sketch transmission specifications for a bandstop filter that is required to pass signals over the bands $0 \leq f \leq 10$ kHz and 30 kHz $\leq f \leq \infty$ with $A_{\text{max}} = 0.1$ dB. The stopband extends from $f = 12$ kHz to $f = 16$ kHz with a minimum required attenuation of 40 dB.

SECTION 12.2: THE FILTER TRANSFER FUNCTION

- 12.8** Consider a 500-nHz filter whose poles are all at a radial distance from the origin of $10^{1/2}/\sqrt{2}$. One pair of complex-conjugate poles is at 30° angles from the $j\omega$ axis, and the other pair is at 30° angles. Give the transfer function in each

of the following cases:

- The transmission zeros are all at $\omega = 0$ and the dc gain is unity.
- The transmission zeros are all at $\omega = 0$ and the high-frequency gain is unity.

What type of filter results in each case?

- 12.9** A third-order low-pass filter has transmission zeros at $\omega = 2$ rad/s and $\omega = \infty$. Its corner frequencies are $\omega = -1$ and $\omega = -3.5 \pm j\sqrt{8}$. The dc gain is unity. Find $T(s)$.

- 12.10** For the order N and the form of $T(s)$ of a bandpass filter having transmission zeros as follows: one at $\omega = 0$, one at $\omega = 0.2$ rad/s, one at $\omega \times 10^3$ rad/s, one at $\omega = 10^3$ rad/s, and one at $\omega = \infty$. If this filter has a monotonic (exponential) passband transmission with a peak at the center frequency of 2×10^3 rad/s, and a stopband response, in the stopband, sketch the shape of $|sT|$.

- *12.11** Analyze the RLC network of Fig. 12.11 to determine A_{max} , A_{min} , ω_c , ω_0 , margin , and hence its poles and corner frequencies. Begin the analysis at the output and work your way back to the input.

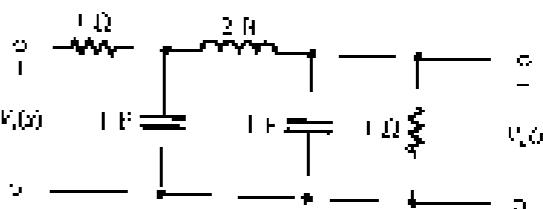


FIGURE P12.11

SECTION 12.3: BUTTERWORTH AND CHEBYSHEV FILTERS

- 12.12** Determine the order N of the Butterworth filter for which $A_{\text{max}} = 1$ dB, $A_{\text{min}} = 20$ dB, and the selectivity ratio $\omega_c/\omega_0 = 1/10$. What is the desired value of minimum stopband attenuation if A_{min} is to be exactly 20 dB, in what value should A_{max} be reduced?

- 12.13** Calculate the value of attenuation obtained at a frequency 1.6 times the 3-dB frequency of a seventh-order Butterworth filter.

- 12.14** Find the natural modes of a Butterworth filter with a 1-dB bandwidth of 10^4 rad/s and $N = 5$.

- 12.15** Design a Butterworth filter that meets the following low-pass specifications: $f_p = 0.1$ Hz, $A_{\text{max}} = 2$ dB, $f_c = 15$ kHz, and $A_{\text{min}} = 15$ dB. Find N , the natural modes, and $T(s)$. What is the attenuation provided at 20 kHz?

***12.16** Sketch [2] for a seventh-order low-pass Chebyshev filter with $\omega_0 = 1$ rad/s, $A_{\text{peak}} = +4\text{dB}$. Use Eq. (12.18) to determine the values of ϕ at which $|T| = 1$, and the values of ϕ at which $|T| = \sqrt{2}/2 = 0.707$. Indicate these values on your sketch. Use Eq. (12.12) to determine ω_1 at $\omega = 2$ rad/s and indicate this value on your sketch. For what values of ω is the peak (in dB) greater than the transmission amplitude?

12.17 Consider the attenuation provided by a fifth-order Chebyshev filter at $\omega = 2\omega_0$ to that provided by a Butterworth filter of equal order. For both, $A_{\text{peak}} = 1\text{dB}$. Sketch [1] the ratio from one to the other.

D*12.18 It is required to design a low-pass filter to meet the following specifications: $f_c = 4\text{ kHz}$, $A_{\text{peak}} = 1\text{dB}$, $\delta = +4\text{dB}$, $A_{\text{stop}} = -40\text{dB}$.

- Find the required order of Chebyshev filter. What is the excess rolloff in the stopband attenuation obtained?
- Find the poles and their locations.

SECTION 12.4: FIRST-ORDER AND SECOND-ORDER FILTER FUNCTIONS

D12.19 Use the information displayed in Fig. 12.13 to design a low-order up-imp RC low-pass filter having a 3-dB frequency of 20 kHz, a dc gain magnitude of 10³, and an input resistance of $10\text{ k}\Omega$.

12.20 Use the information given in Fig. 12.14 to design a two-order up-imp RC high-pass filter with a 3-dB frequency of 100 kHz, and a dc gain magnitude of unity. The low-frequency input resistance is $10\text{ k}\Omega$. What is the high-frequency gain that results? Sketch the anticipated behavior of the transfer function vs frequency.

D*12.21 Use the filter given in Fig. 12.17 to design a three-order up-imp RC passive π -shaping network with a low-cut corner frequency of 1 kHz, a pass frequency of 100 kHz, and a dc gain magnitude of unity. The low-frequency input resistance is $10\text{ k}\Omega$. What is the high-frequency gain that results? Sketch the anticipated behavior of the transfer function vs frequency.

D*12.22 By cascading a three-order up-imp RC low-pass circuit with a three-order up-imp RC high-pass circuit one can design a wide-swing bandpass filter. Consider such a design for the case in which the center gain is 12 dB and the 3-dB bandwidth extends from 100 Hz to 10 kHz. Select appropriate component values under the constraint that no resistors higher than 100 k Ω are to be used, and show the load resistance is to be as high as possible.

12.23 Design first for the up-imp RC circuit in Fig. 12.14. We wish to use the circuit as a variable phase shifter by adjusting R . If the input signal frequency is 10⁴ rad/s and if $C = 1.1\text{ pF}$, find the values of R required to obtain phase shifts of 0°, 90°, 180°, 270°, and -180°.

12.24 Show that by interchanging R and C in the up-imp RC circuit of Fig. 12.14, the resulting phase shift equals the

range 0 to 180° (with 0° at high frequencies and 180° at low frequencies).

12.25 Use the information in Fig. 12.16(a) to obtain the transfer function of a second-order low-pass filter with $\omega_0 = 1\text{ rad/s}$, $Q = 1$, and $C_{\text{peak}} = 1$. At what frequency does $|T| = 0.5$? What is the peak transmission value?

D*12.26** Use the information in Fig. 12.16(c) to obtain the transfer function of a second-order low-pass filter that just meets the specifications defined in Fig. 12.3 with $\omega_0 = 1\text{ rad/s}$ and $A_{\text{peak}} = 2.44$. Note that there are two possible solutions. For each, find ω_1 and ϕ . Assume if $\omega_2 = 2$ rad/s, find the value of A_{stop} obtained in each case.

D*12.27** Use two first-order up-imp π -all-pass circuits in cascade to design a filter that provides a set of three-phase 60-Hz voltages, each separated by 120° and $\pm 180^\circ$ magnitude, as shown in the phasor diagram of Fig. P12.27. These voltages simulate those used in three-phase power transmission systems. Use 1-pole asymptotes.

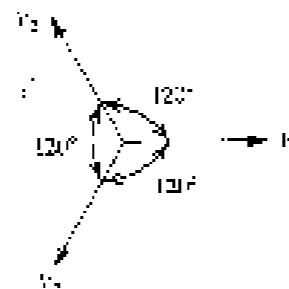


FIGURE P12.27

12.28 Use the information given in Fig. 12.16(b) to find the transfer function of a second-order high-pass filter with external modes $\omega = 0.5 \pm j\sqrt{2}/2$ and a high-frequency gain of unity. The low-frequency input resistance is $10\text{ k}\Omega$. What is the high-frequency gain that results? Sketch the anticipated behavior of the transfer function vs frequency.

D12.29** (a) Show that [7] of a second-order bandpass function is geometrically symmetric about the center frequency ω_0 . That is, the condition that each pair of frequencies ω_1 and ω_2 for which $|T|(\omega_1) = |T|(\omega_2) = 0$ is related by $\omega_2/\omega_1 = 10^{\pm 1}$.

(b) Find the transfer function of the second-order bandpass filter that meets specifications of problem 12.14 where $\omega_0 = 2100\text{ rad/s}$, $\omega_1 = 0.03\text{ rad/s}$, and $A_{\text{peak}} = 1\text{dB}$. If $\omega_2 = 2000\text{ rad/s}$ then $A_{\text{stop}} = 40\text{dB}$.

D*12.30 Use the result of Exercise 12.15 to find the transfer function of a filter that is required to eliminate a harmonics interference of 60-Hz for a 100-Hz sine. Since the frequency of the interference is not stable, the filter should be designed to provide a tolerance of 2.0 dB over a 4-Hz band centered around 50 Hz. The corner frequency of the filter is to be unity.

12.31 Consider a second-order all-pass circuit in which values of the component values result in the frequency of the

poles being slightly lower than that of the zeros. Roughly sketch the expected $|T|$. Repeat for the case of the frequency of the zeros slightly higher than the frequency of the poles.

12.32 Consider a second-order all-pass filter in which zeros occur in the complex ω plane, values result in the ϕ value of the zeros being smaller than the ϕ value of the poles. Roughly sketch the expected $|T|$. Repeat for the case of the ϕ value of the zeros lower than the ϕ value of the poles.

SECTION 12.5: THE SECOND-ORDER LCR RESONATOR

D12.33 Design the LCR resonator of Fig. 12.17(a) to obtain desired modes with $\omega_0 = 10^3\text{ rad/s}$ and $Q = 2$. Use $R = 10\text{ k}\Omega$.

12.34 For the LCR resonator of Fig. 12.17(a), find the change in ω_0 that results in (a)

- Increasing L by 1%
- Increasing C by 1%
- Increasing R by 1%

12.35 Derive the expression for $V_2(s)/V_1(s)$ of the high-pass circuit of Fig. 12.18(c).

12.36 Use the values of Fig. 12.18(h) to design a low-pass filter with $\omega_0 = 1\text{ rad/s}$ and $Q = 1/\sqrt{2}$, i.e., with a 0.1-pF capacitor.

12.37 Modify the bandpass circuit of Fig. 12.18(j) to change its center-frequency gain from 1 to 10^3 vs. ω , changing ω_0 vs. Q .

12.38 Consider the LCR resonator of Fig. 12.17(a) with $100\text{ }\mu\text{H}$ disconnected from ground and connected to an input signal source V_1 , node 1 disconnected from ground and connected to an input signal source V_2 , and node 2 disconnected from ground and connected to a third input signal source V_3 . Use superposition to find the voltage that develops across L connecting V_2 to node 1 (V_L). V_1 , V_2 , and V_3

12.39 Consider the notch filter shown in Fig. 12.18(l). For what values of L_1 to L_2 does the notch occur at $0.9\omega_0$? For this case, what is the magnitude of the transmission of the filter at $\omega = 0.1\omega_0$? At $\omega = 0.9\omega_0$?

SECTION 12.6: SECOND-ORDER ACTIVE FILTERS BASED ON INDUCTOR REPLACEMENT

D12.40 Design the circuit in Fig. 12.20 utilizing available component values, to result in an impedance of (a) 100, (b) 10, or (c) 0.1 k Ω .

***12.41** Starting from first principles and assuming ideal opamps, derive the transfer function of the circuit in Fig. 12.22(d).

D*12.42 It is required to design a three-order Butterworth filter having a 3-dB bandwidth of 10 Hz. Use the π -topology. Give the complete circuit and specify all component values. What value of center frequency gain is obtained?

Fig. 12.20(a) shows a wide-band up-imp RC circuit of the type shown in Fig. 12.18(a). Select appropriate component values.

D12.43 Design the circuit of Fig. 12.22(e) to realize an LPN function with $\omega_0 = 1\text{ kHz}$, $f_c = 5\text{ Hz}$, $Q = 10$, and a unity dc gain. Select $C_1 = 10\text{ nF}$.

D12.44 Design the all-pass circuit in Fig. 12.22(g) to provide a phase shift of 180° at $f_c = 1\text{ kHz}$ and to have $Q = 1$ as 1-mF capacitors.

12.45 Consider the π -circuit circuit of Fig. 12.20(a) with R_2 eliminated, a capacitor C_2 connected between nodes 1 and 3 instead, and a voltage source V_2 connected to node 2. Show that the input impedance seen by V_1 is $R_1 R_2 C_2 S_1 S_2$. How does this impedance relate to physical frequencies ($\omega = 100\text{ rad/s}$)? (This impedance is known as a frequency-dependent negative resistance, or FDNR.)

D12.46 Using the transfer function of the LPN filter given in Table 12.1, derive the design equations also given.

D12.47 Using the transfer function of the BPF filter given in Table 12.1, derive the design equations also given.

D*12.48** It is required to design a third-order low-pass filter whose LPN is equiipole in both the passband and the stopband to the memory shown in Fig. 12.3, except that the response shown is not $N = 3$. The filter passband extends from $\omega = 0$ to $\omega = 1\text{ rad/s}$, and the passband transmission varies between 1 and 10. The stopband edge is at $\omega = 2\text{ rad/s}$. The following transfer function was obtained using MATLAB calculations:

$$T(s) = \frac{3.1506s^2 + .4966}{(s + 1.724s^2)(s^2 + 1.273s + 1.0504)}$$

The center of the passband is to have $\omega_0 = 10^3\text{ rad/s}$.

(a) Obtain the transfer function of the actual filter by replacing s by $s/10^3$.

(b) Recast the filter as the cascade connection of a low-order LP up-imp RC circuit of the type shown in Fig. 12.18(a) and a second-order LP circuit of the type shown in Fig. 12.22(e). Such sections will have a dc gain of unity. Select appropriate component values. What is the filter with an equivalent response T , both the passband and the stopband to the original LPN filter?

SECTION 12.7: SECOND-ORDER ACTIVE FILTERS BASED ON THE TWO-INTEGRATOR-LOOP TOPOLOGY

D12.49 Design the XTN circuit of Fig. 12.24(a) to realize a bandpass filter with a center frequency of 1 kHz and a 3-dB bandwidth of 50 Hz. Use the π -topology. Give the complete circuit and specify all component values. What value of center frequency gain is obtained?

- D12.50** (a) Using the KHN biquad with the capacitor summing amplifier (Fig. 12.34c), show that an all-pass function is realized by selecting $R_1 = R_2 = R_3 = Q_1/\omega_0$. Also show that the flux gain decreases as $R_1 > R_3$.
- (b) Design the all-pass circuit, assuming $\omega_0 = 10^4$ rad/s, $Q = 2$, and flux gain = 10. Select appropriate component values.

- D12.51** Consider a switch node with $\omega_0 = \omega_1$ realized using a KHN biquad with an output-summing amplifier. If the switching elements used have 1% tolerances, what is the worst-case percentage deviation between ω_0 and ω_1 ?

- D12.52** Design the circuit of Fig. 12.36 as real or a low-pass notch filter, with $\omega_0 = 10$ rad/s, $Q = 10$, $\omega_{\text{notch}} = 1.1$, and $\omega_1 = 2 \times 10^4$ rad/s. Use $C = 10 \text{ nF}$ and $V = 20 \text{ VDC}$.

- D12.53** Is the a-pass realization using the circuit of Fig. 12.36, which components does one need to tune to agree with (a) ω_0 and (b) only Q ?

- D12.54** Repeat Problem 12.46 using the Top-T common-emitter layout of Fig. 12.26 to realize the second-order section in the cascade.

SECTION 12.8: SINGLE-AMPLIFIER BIQUADRATIC ACTIVE FILTERS

- D12.55** Design the circuit of Fig. 12.26 to realize a $\sqrt{2}$ -pole filter with $\omega_0 = 10^4$ rad/s, $Q = \sqrt{2}$. Use $C = C_1 = 1 \text{ pF}$.

- D12.56** Consider the bridge-T network of Fig. 12.26(b) with $R_1 = R_2 = R$ and $C_1 = C_2 = C$, and denote $CR = R$ (low-pass and poles of the bi-quad-T network). If the network is placed in the negative feedback path of an ideal infinite-gain op amp, as in Fig. 12.29, find the poles of the closed-loop amplifier.

- D12.57** Consider the bridge-T network of Fig. 12.26(b) with $R_1 = R_2 = R$, $C_1 = C$, and $C_2 = C/16$. Let the network be placed in the negative feedback path of an ideal infinite-gain op amp and let C be disconnected from ground and connected to the input signal source V . Analyze the resulting circuit to determine its transfer function V_o/V (i.e., when V is the voltage), the transimpedance, the open-loop gain, a bandpass filter, and finally ω_0 , Q , and the energy-frequency gain.

- D12.58** Consider the bandpass circuit shown in Fig. 12.30. Let $C_1 = C_2 = C$, $R_1 = R_2 = 4Q^2$, $CR = 2Q/\omega_0$, and $Q = 1$. Disconnect the positive input feed-back of the op-amp from ground and apply V through a voltage divider R_1, R_2 to the positive input terminal. Analyze the circuit to find its transfer function V_o/V . Find the voltage divide ratio $R_2/(R_1 + R_2)$ so that (a) it will realize (a) a low-pass function and (b) a notch function. Assume the op-amp is ideal.

- D12.59** Derive the transfer function of the circuit of Fig. 12.35, assuming the op-amp to be ideal. Then show that the circuit has a high-pass function. What is the high-

frequency gain of the circuit? Design a circuit for a maximally flat response with a 3-dB loss over $\omega_0/10^4$ rad/s. Use $C_1 = C_2 = 10 \text{ nF}$. Then (a) a maximally flat response ($G = 1/\sqrt{2}$) and (b) $\omega_0 = 10^4$.

- D12.60** Design a fifth-order Butterworth low-pass filter with a 3-dB bandwidth of 5 kHz. Use a ladder realization using the two-stage connection of two Sallen-and-Key circuits (Fig. 12.36e) and a 1-quarter-section (Fig. 12.19a). Use a 10 k Ω value for C_1 resistors.

- D12.61** Try problems of drawing the complementary-symmetry transfer function by interchanging input and ground, as illustrated in Fig. 12.31, applied to any second-order filter, just RC networks as shown. Show that if S is between 0 and ω_0 a bandpass with a constant-frequency gain of unity, then the complement obtained is a notch. Verify this by using the RLC circuit of Fig. 12.18(c) and (d).

SECTION 12.9: SENSITIVITY

- D12.62** Evaluate the sensitivities of ω_0 and Q relative to R , C , and G of the bandpass circuit in Fig. 12.18(d).

- D12.63** Verify the following sensitivity identities:

- (a) If $y = xA$, then $\delta_y^2 = \delta_x^2 + \delta_A^2$.
 (b) If $y = x + A$, then $\delta_y^2 = \delta_x^2 + \delta_A^2$.
 (c) If $y = Ax$, where A is a constant, then $\delta_y^2 = A^2 \delta_x^2$.
 (d) If $y = A/x$, where x is a constant, then $\delta_y^2 = A^2 \delta_x^2$.

- D12.64** For the high-pass filter of Fig. 12.33(b), work out the sensitivities of ω_0 and Q to a amplifier gain β .

- D12.65** For the feedback loop of Fig. 12.34(a), use the expressions in Eqs. (12.77) and (12.78) to determine the sensitivities of ω_0 and Q relative to all passive components for the design in which $R = R_1$.

- D12.66** For the op-amp-RC realization of Fig. 12.21(b), use the expressions for ω_0 and Q given in the top row of Table 12.1 to calculate the sensitivities of ω_0 and Q to all resistors and capacitors.

SECTION 12.10: SWITCHED-CAPACITOR FILTERS

- D12.67** For the switched-capacitor opamp circuit of Fig. 12.35(b), in which a clock frequency of 10 kHz is used, what equivalent values correspond to capacitance C_1 values of 1 pF and 10 pF?

- D12.68** For a voltage $v^2(t)$ supplied to the summing junction of the circuit of Fig. 12.35(b), in which C_1 is 1 pF, what charge is transferred for each cycle of the two-phase clock? If a 100-kHz clock, what is the average current drawn along the input source? For a feedback capacitance of 10 pF, what change

would you expect in the output (on each cycle of the clock)? For an amplitude that saturates at ± 10 V and the feedback capacitor initially discharged, how many clock cycles would it take to saturate the amplifier? What is the average slope of the increase output voltage profile?

- D12.69** Repeat Exercise 12.31 for a clock frequency of 10 kHz.

- D12.70** Repeat Exercise 12.31 for $G = 10$.

- D12.71** Design the circuit of Fig. 12.37(a) to realize, at the output of the second integrator/filter/integrator, a maximally flat low-pass function with $\omega_0 = 10^4$ rad/s and unity dc gain. Use a clock frequency $f = 10^4$ kHz and set $C_1 = C_2 = 10 \text{ pF}$. Give the values of C_3 , C_4 , and C_5 (Hint: This is maximally flat response, $Q = 1/\sqrt{2}$ and $\omega_0 = \omega_1$).

SECTION 12.11: TUNED AMPLIFIERS

- D12.72** A voltage signal source with a resistance $R_s = 10 \text{ k}\Omega$ is connected to the input of a common-emitter RLC amplifier between base and emitter is connected in series with $L = 1 \mu\text{H}$ and $C = 200 \text{ pF}$. The transistor is biased at 1 mA and has $\beta = 200$, $C_v = 10 \text{ fF}$, and $C_b = 1 \text{ pF}$. The transistor load is a resistor of $2.5 \text{ k}\Omega$. Find ω_0 , G , the 3-dB bandwidth, and the center frequency gain of this single-sided amplifier.

- D12.73** A coil having an inductance of $10 \mu\text{H}$ is intended for applications around 1 MHz frequency. It is specified to be 20 dB. Find the equivalent parallel resistance R_p . What is the value of the shunt capacitor to produce resonance at 1 MHz? What additional parallel resistance is required to produce a 3-dB bandwidth of 10 kHz?

- D12.74** A inductance of $30 \mu\text{H}$ is associated with a 100 pF capacitor. If the inductor is tapped at one-third of its arms and a $1-\text{k}\Omega$ resistor is connected across the one-third arm, find ω_0 and Q of the resonator.

- D12.75** Consider a common-emitter tuned amplifier loaded with an inductance L . Ignoring r_e and r_c , show that for $\omega C_L \ll 1/Q^2$, the a input to load admittance is given by

$$Y_{in} = \left(\frac{1}{C_L} - \frac{\omega^2 C_L L g_m}{\omega^2 + \omega^2 Q^2} \right)^{-1} = \frac{1}{C_L + C_{load}}$$

Note: The real part of the input admittance can be negative. This can lead to oscillations.

- D12.76** (a) Substituting $s = j\omega$ in the transfer function of a second-order bandpass filter (see Fig. 12.16a) for $|T(j\omega)|$ and in the expression of ω_1 , ω_2 , ω_0 , Q , and ω_0 , where $\omega_0 = 1/\omega_0$, $\omega_1^2 = \omega_1^2 + 2Q^2\omega_0^2$, $\omega_2^2 = \omega_2^2 + 2Q^2\omega_0^2$, show that $\omega_1 < Q < 1$.

$$|T(j\omega)| \approx \frac{|T(j\omega_0)|}{\sqrt{1 + Q^2(\omega/\omega_0)^2}}$$

- (b) Use the result obtained in (a) to show that the 3-dB bandwidth B of a synchronously tuned section is related to ω_0 as

$$B = \omega_0 / \sqrt{2} \sqrt{1 + Q^2}$$

- D12.77** (a) Using the fact that, for $Q > 1$, the second-order bandpass response in the neighborhood of ω_0 is the same as the response of a first-order low-pass with 3 dB frequency of $(\omega_0/2)\sqrt{2}$, show the 3-dB bandwidth response at $\omega = \omega_0$. For this, if $\omega_0 = \omega_1$, is given by

$$|T(j\omega)| \approx \frac{|T(j\omega_0)|}{\sqrt{1 + Q^2(\omega/\omega_0)^2}}$$

- (b) Use the relationship derived in (a) together with Eqs. (12.113) to show that a bandpass amplifier with a 3-dB bandwidth B , designed using a synchronously tuned stage, has an overall transmission T_0 given by

$$T_0(\omega_0) = \frac{C_1 \omega_0 |T(j\omega_0)|}{[1 + (1/2)^{1/2} (\omega_0/B)]^{1/2}}$$

- (c) Use the relationship derived in (b) to find the attenuation (in decibels) obtained at a bandwidth of 20 for $N = 1$ to 5. Also find the ratio of the 3-dB bandwidth to the 5-dB bandwidth for $N = 1$ to 5.

- D12.78** This problem investigates the selectivity of maximally flat staggered-tuned composition derived in the manner described in Fig. 12.28.

- (a) Use low-pass unity-gain (unity-gain) filter having a 3-dB bandwidth $B/2$ and center ω_0 to find the magnitude response

$$|T| = 1 / \sqrt{1 + \left(\frac{\omega}{B/2} \right)^2}$$

where $B = 1/\omega_0$ is the frequency of the low-pass dominant. This relationship can be obtained using the information provided in Section 12.3 on Butterworth filters. Use this expression to obtain the corresponding bandwidth $\omega_0 = \omega_1 + \omega_2$, where $\omega_1 < \omega_2$, the relations

$$T = 1 / \sqrt{1 + \left(\frac{\omega}{B/2} \right)^2}$$

- (b) Use the formula in (a) in (a) to find the attenuation (in decibels) at a bandwidth of 20 for $N = 1$ to 5. Also find the ratio of the 3-dB bandwidth to the 5-dB bandwidth for $N = 1$ to 5.

- D12.79** Consider a sixth-order staggered-tuned bandpass amplifier with center frequency ω_0 and 3-dB bandwidth B . The poles are to be obtained by shifting three of the Butterworth maximally flat low-pass filter, given in Fig. 12.13b. For the three resonant circuits, find ω_1 , ω_2 , ω_0 , the 3-dB bandwidth, and Q .

CHAPTER 13

Signal Generators and Waveform-Shaping Circuits

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INTRODUCTION

In the design of electronic systems the need frequently arises for signals having prescribed standard waveforms, for example, sinusoidal, square, triangular, or pulse. Systems in which standard signals are required include computers and control systems where clock pulses are needed for, among other things, timing, communication systems where signals of a variety of waveforms are utilized as information carriers, and test and measurement systems where signals again of a variety of waveforms are employed for testing and characterizing electronic devices and circuits. In this chapter we study signal-generation circuits.

There are several fairly different approaches to the generation of waveforms, perhaps the most commonly used of the standard waveforms. The first approach, studied in Sections 13.1

to 13.5, employs a positive-feedback loop consisting of an amplifier and an RC or LC frequency-selective network. The amplitude of the generated sine waves is limited, in so, using a nonlinear mechanism implemented either with a separate circuit or using the nonlinearities of the amplifying device itself. In spite of this, these circuits, which generate sine waves without resonance phenomena, are known as *linear oscillators*. The name clearly distinguishes them from the circuits that generate sinusoids by way of the second approach. In these circuits, a sine wave is obtained by appropriately shaping a triangular waveform. We study waveform-shaping circuits in Section 13.9, following the study of triangular-waveform generators.

Circuits that generate square, triangular, pulse (etc.) waveforms, called *multivibrators*, oscillators or function generators, employ circuit building blocks known as *multivibrators*. There are three types of multivibrator: the *bistable* (Section 13.4), the *astable* (Section 13.5), and the *monostable* (Section 13.6). The multivibrator circuits presented in this chapter employ op-amps and are intended for precision analog applications. Multivibrator circuits using digital logic gates were covered in Chapter 11.

A general and versatile scheme for the generation of square and triangular waveforms is obtained by combining a bistable multivibrator and an op-amp integrator in a feedback loop (Section 13.5). Similar results can be obtained using a commercially available versatile IC chip, the 555 timer (Section 13.7). The chapter includes also a study of precision circuit that implement the rectifier functions introduced in Chapter 9. The circuit studied here (Section 13.9), however, are intended for applications that demand precision, such as in instrumentation systems, including waveform generation. The chapter concludes with examples illustrating the use of SPICE in the simulation of oscillators.

13.1 BASIC PRINCIPLES OF SINUSOIDAL OSCILLATORS

In this section, we study the basic principles of the design of linear sine-wave oscillators. In spite of the *non-linear oscillators*, some form of nonlinearity has to be employed to provide control of the amplitude of the output sine wave. In fact, all oscillators are essentially nonlinear circuits. This complicates the task of analysis and design of oscillators; no longer is one able to apply transform-frequency methods directly. Nevertheless, techniques have been developed by which the design of sinusoidal oscillators can be performed in two steps. The first step is a linear one, and frequency-domain methods of circuit analysis can be readily employed. Subsequently, a nonlinear mechanism for amplitude control can be provided.

13.1.1 The Oscillator Feedback Loop

The basic structure of a sinusoidal oscillator consists of an amplifier and a frequency-selective network connected in a positive-feedback loop, such as that shown in block diagram form in Fig. 13.1. Although in an actual oscillator circuit, no input signal will be present, we include an input signal here to help explain the principle of operation. It is important to note that unlike the negative-feedback loop of Fig. 8.1, here the feedback signal x_f is summed with a *positive sign*. Thus the gain with feedback is given by

$$A_f(x) = \frac{A(x)}{1 - A(x)\beta(x)} \quad (13.1)$$

where we note the negative sign in the denominator.



FIGURE 13.1 The basic structure of a sinusoidal oscillator. A positive-feedback loop is formed by an amplifier and a frequency-selective network. In an actual oscillator circuit, no input signal will be present, so an input signal x_i is employed to help explain the principle of operation.

According to the definition of loop gain in Chapter 8, the loop gain of the circuit in Fig. 13.1 is $-A(x)\beta(x)$. However, for our purposes here it is more convenient to drop the minus sign and define the loop gain $\beta(x)$ as

$$\beta(x) = A(x)\beta(x) \quad (13.2)$$

The characteristic equation is therefore

$$1 - \beta(x) = 0 \quad (13.3)$$

Note that this new definition of loop gain corresponds directly to the actual gain seen around the feedback loop of Fig. 13.1.

13.1.2 The Oscillation Criterion

At a specific frequency ω_0 , the loop gain $\beta(\omega_0)$ is equal to unity, if follows from Eq. (13.1) that A_f will be infinite. That is, at this frequency the circuit will have a finite output for zero input signal. Such a circuit is by definition an oscillator. Thus the condition for the feedback loop of Fig. 13.1 to produce sustained oscillations of frequency ω_0 is

$$1/\beta(\omega_0) = 1/(A(\omega_0)\beta(\omega_0)) - 1 \quad (13.4)$$

That is, at ω_0 , the *pole* of the loop gain should be zero and the *resonance* of the loop gain should be unity. This is known as the Barkhausen criterion. Note, however, that for the circuit to oscillate at one frequency, the oscillation criterion should be satisfied only at one frequency (ω_0), otherwise the resulting waveform will not be a simple sinusoid.

An intuitive feeling for the Barkhausen criterion can be gained by considering once more the feedback loop of Fig. 13.1. For this purpose consider an output voltage with no input applied ($x_i = 0$), the feedback signal x_f ,

$$x_f = \beta x_o$$

should be sufficiently large that when multiplied by A it produces x_o , that is,

$$A x_f = x_o$$

For both the negative-feedback loop in Fig. 8.1(a) and the positive-feedback loop in Fig. 13.1, the loop gain is $A - A\beta$. However, the negative sign with which the feedback signal x_f is summed in the negative-feedback loop results in the characteristic equation being $1 - \beta = 0$. In the positive-feedback loop, the feedback signal is summed with a positive sign, thus resulting in the characteristic equation $1 - \beta = 0$.

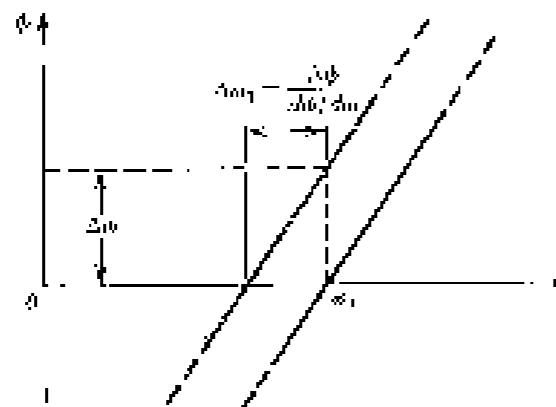


FIGURE 13.2 Dependence of the oscillation-frequency stability on the slope of the phase response. A steep phase response (i.e., large $\Delta\omega_0$) results in a small change in phase offset due to a small change in frequency (for example, in load variation in a circuit example will

then be,

$$\Delta\beta\omega_0 = \Delta\omega_0$$

which results in

$$\Delta\beta = 1$$

It should be noted that the frequency of oscillation ω_0 is determined solely by the phase characteristics of the feedback loop; the 'loop oscillates at the frequency for which the phase is zero. It follows that the stability of the frequency of oscillation will be determined by the manner in which the phase $\phi(\omega)$ of the feedback loop varies with frequency. A "steep" function $\phi(\omega)$ will result in a more stable frequency. This can be seen if one imagines a change in phase $\Delta\phi$ due to a change in one of the circuit components. If $\Delta\phi/\Delta\omega_0$ is large, the resulting change in ω_0 will be small, as illustrated in Fig. 13.2.

An alternative approach to the study of oscillator circuits consists of examining the circuit poles, which are the roots of the characteristic equation (Eq. 13.5). For the circuit to produce sustained oscillations at a frequency ω_0 the characteristic equation has to have roots at $\omega = \pm j\omega_0$. Thus $1 - \Delta(\omega)\beta(\omega)$ should have a factor of the form $s^2 + \omega_0^2$.

EXERCISE

- 13.1 Consider a constant-frequency source of 10 Hz with a voltage of 10 mV. If the output voltage of the filter is 100 mV, find the required value of the filter output power and the filter quality factor.

Ans: 1.11 mW

13.1.3 Nonlinear Amplitude Control

The oscillation condition, the Barkhausen criterion, just discussed, guarantees sustained oscillations in a mathematical sense. It is well known, however, that the parameters of any physical system cannot be maintained constant for any length of time. In other words, suppose we were able to make $\Delta\beta = 1$ at $\omega_0 = \omega_0$, and then the temperature changes and $\Delta\beta$ becomes slightly less than unity. Obviously, oscillations will cease in this case. Conversely,

if $\Delta\beta$ exceeds unity, oscillations will grow in amplitude. We therefore need a mechanism for forcing $\Delta\beta$ to remain equal to unity at the desired value of output amplitude. This task is accomplished by providing a nonlinear circuit for gain control.

Basically, the function of the gain control mechanism is as follows: First, to ensure that oscillations will start, one designs the circuit such that $\Delta\beta$ is slightly greater than unity. This corresponds to designing the circuit so that the poles are in the right half of the s -plane. Once as the power supply is turned on, oscillations will grow in amplitude. When the amplitude reaches the desired level, the nonlinear network comes into action and causes the loop gain to be reduced to exactly unity. In other words, the poles will be "pulled back" to the $j\omega$ -axis. This action will cause the circuit to sustain oscillations at this desired amplitude. If, for some reason, the loop gain is reduced below unity, the amplitude of the sine wave will diminish. This will be detected by the nonlinear network, which will cause the loop gain to increase to exactly unity.

As will be seen, there are two basic approaches to the implementation of the nonlinear amplitude-stabilization mechanism. The first approach makes use of a limiter circuit (see Chapter 4). Oscillations are allowed to grow until the amplitude reaches the level to which the limiter is set. When the limiter comes into operation, the amplitude remains constant. Obviously, the limiter should be "soft" to minimize nonlinear distortion. Such distortion, however, is reduced by the filtering action of the frequency-selective network in the feedback loop. In fact, in one of the oscillator circuits studied in Section 13.2, the sine waves are hard limited, and the resulting square waves are applied to a bandpass filter present in the feedback loop. The "purity" of the output sine waves will be a function of the selectivity of this filter. That is, the higher the Q of the filter, the less the harmonic content of the side-wave output.

The other mechanism for amplitude control utilizes an element whose resistance can be controlled by the amplitude of the output signal. By placing this element in the feedback circuit so that its resistance determines the loop gain, the circuit can be designed to ensure that the loop gain reaches unity at the desired steady amplitude. Diodes, or JFETs operated in the triode region,¹ are commonly employed to implement the controlled resistance element.

13.1.4 A Popular Limiter Circuit for Amplitude Control

We conclude this section by presenting a limiter circuit that is frequently employed for the amplitude control of spinoidal oscillators, as well as in a variety of other applications. The circuit is more precise and versatile than those presented in Chapter 4.

The limiter circuit is shown in Fig. 13.3(a), and its transfer characteristic is depicted in Fig. 13.3(b). To see how the transfer characteristic is obtained, consider first the case of a small (close to zero) input signal v_i and a small output voltage v_o , so that v_2 is positive and v_1 is negative. It can be easily seen that both diodes D_1 and D_2 will be off. Thus all of the input current i_1 (i_2) flows through the feedback resistance R_2 , and the output voltage is given by

$$v_o = -(R_2/R_1)v_i \quad (13.5)$$

This is the linear portion of the limiter transfer characteristic in Fig. 13.3(b). We now can use superposition to find the voltages at nodes A and B in terms of v_{ik} and v_{oL} :

$$v_A = V \frac{R_1}{R_2 + R_1} v_{oL} \frac{R_2}{R_2 + R_1} \quad (13.6)$$

$$v_B = -V \frac{R_2}{R_1 + R_2} v_{oL} \frac{R_1}{R_1 + R_2} \quad (13.7)$$

¹We have not studied JFETs in this book. However, the CD accompanying the book includes material on JFETs and MOSFET circuits. The same material can also be found on the book's website.

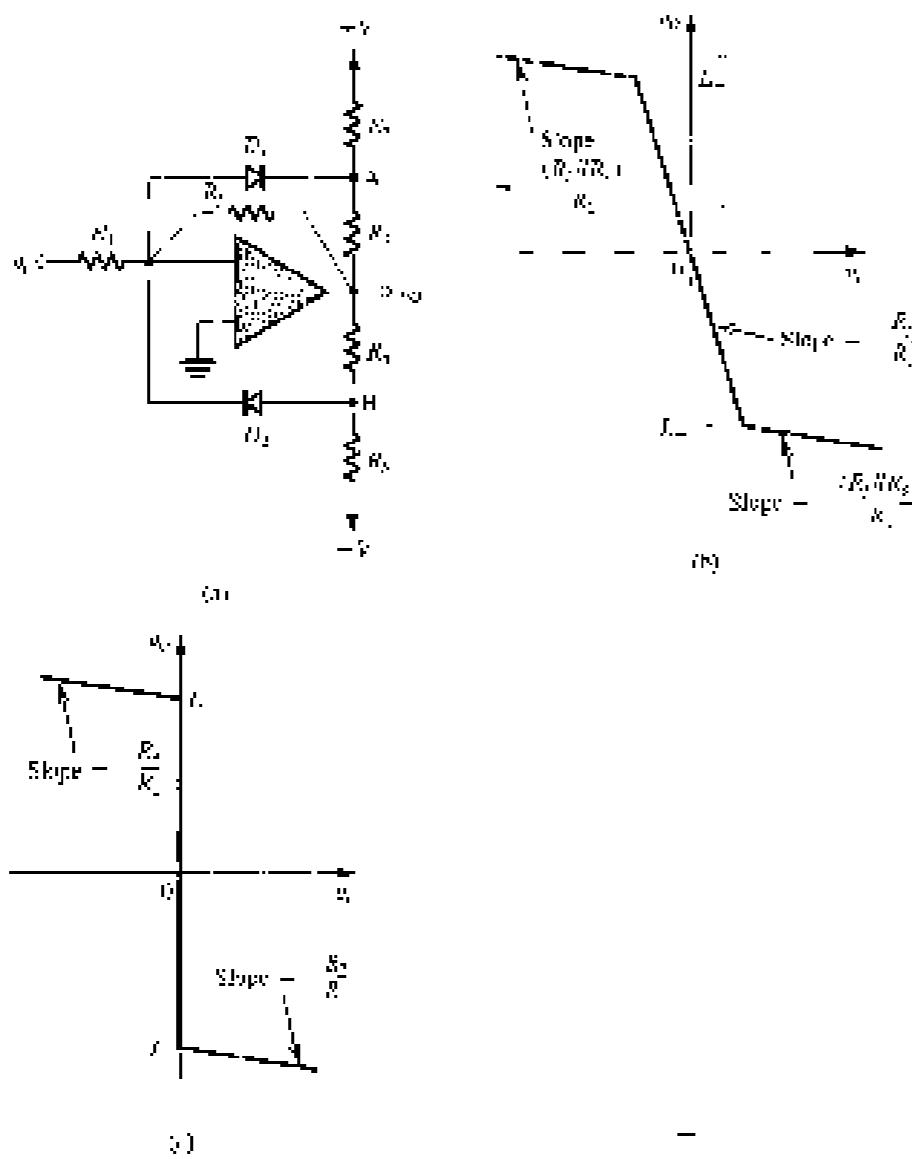


FIGURE 13.3 (a) A popular limiter circuit. (b) Transfer characteristic of the circuit; where \$L_+\$ and \$L_-\$ are given by Eqs. (13.8) and (13.9), respectively. (c) When \$R_3\$ is removed, the limiter function is a linear power \$v_o\$ vs. \$v_i\$ linearized \$v_i\$-slope.

As \$v_i\$ goes positive, \$v_o\$ goes negative (Fig. 13.5), and we see from Eq. (13.7) that \$v_o\$ will become more negative, thus keeping \$D_1\$ off. Equation (13.6) shows, however, that \$v_o\$ becomes less positive. Then, if we continue to increase \$v_i\$, a negative value of \$v_o\$ will be reached at which \$v_o\$ becomes \$-0.7\$ V or so and diode \$D_1\$ conducts. If we use the constant-voltage-drop model for \$D_1\$ and denote the voltage drop \$V_D\$, the value of \$v_o\$ at which \$D_1\$ conducts can be found from Eq. (13.6). This is the negative-limiting level, which we denote \$L_-\$

$$L_- = -\frac{R_2}{R_1} V_D \left(1 + \frac{R_2}{R_{12}}\right) \quad (13.8)$$

The corresponding value of \$v_o\$ can be found by dividing \$I_o\$ by the limiting gain \$-R_2/R_1\$. If \$v_i\$ is increased beyond this value, more current is injected into \$D_1\$, and \$v_o\$ remains at approximately \$-V_D\$. Thus the current through \$R_2\$ remains constant until the additional diode current flows through \$R_1\$. Thus \$R_1\$ appears in effect in parallel with \$R_2\$, and the incremental gain (ignoring DC diode resistance) is \$-(R_2 \parallel R_1)/R_1\$. To make the slope of the transfer characteristic small in the limiting region, a low value should be selected for \$R_1\$.

The transfer characteristic for negative \$v_i\$ can be found in a manner identical to that just employed. It can be easily seen that for negative \$v_i\$, diode \$D_2\$ plays an identical role to that played by diode \$D_1\$ for positive \$v_i\$. The positive-limiting level \$L_+\$ can be found to be

$$L_+ = V_D \frac{R_1}{R_2} + V_D \left(1 + \frac{R_1}{R_{12}}\right) \quad (13.9)$$

and the slope of the transfer characteristic in the positive-limiting region is \$-(R_1/R_2)/R_1\$. We thus see that the circuit of Fig. 13.3(a) functions as a soft limiter, with the limiting levels \$L_+\$ and \$L_-\$ and the limiting gains independently adjustable by the selection of appropriate resistor values.

Finally, we note that increasing \$R_1\$ results in a higher gain in the linear region while keeping \$L_+\$ and \$L_-\$ unchanged. In the limit, removing \$R_1\$ together results in the transfer characteristic of Fig. 13.3(c), which is that of a comparator. That is, the circuit compares \$v_i\$ with the comparator reference value of \$0\$ V; \$v_i > 0\$ results in \$v_o = L_+\$, and \$v_i < 0\$ yields \$v_o = L_-\$.

EXERCISE

- 13.2. For the circuit of Fig. 13.3(a), with \$V_D = 12\$ V, \$R_1 = 20\$ k\$\Omega\$, \$R_2 = 10\$ k\$\Omega\$, and \$R_{12} = 10\$ k\$\Omega\$, find the limiting levels and the value of each of the three resistors required to obtain the same gain and the same slope of the transfer characteristic in the positive and negative-limiting regions.

13.2 OP AMP-RC OSCILLATOR CIRCUITS

In this section we shall study some practical oscillator circuits utilizing op-amps and RC networks.

13.2.1 The Wien-Bridge Oscillator

One of the simplest oscillator circuits is based on the Wien bridge. Figure 13.4 shows a Wien bridge oscillator without the nonlinear gain-control network. The circuit consists of an op-amp connected in the noninverting configuration, with a closed-loop gain of \$1 + R_2/R_1\$. In the feedback path of this positive-gain amplifier an RC network is connected. The loop gain can be easily obtained by multiplying the transfer function \$Y(s)/V(s)\$ of the feedback network by the amplifier gain.

$$L(s) = \left|1 + \frac{R_2}{R_1} \frac{Z_2}{Z_1 + Z_2}\right|$$

Thus,

$$L(s) = \frac{1 + R_2/R_1}{S + aCR + 1/\omega CR} \quad (13.10)$$

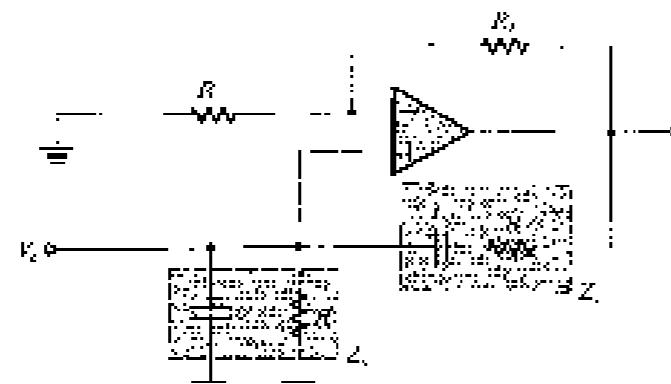


FIGURE 13.4 A Wien bridge oscillator without amplitude stabilization.

Substituting $s = j\omega$ results in

$$\frac{v_1(j\omega)}{v_2(j\omega)} = \frac{1 + R_2/R}{j + j\omega(R_1C_1 + R_2C_2)} \quad (13.11)$$

The loop gain will be a real number (i.e., the phase will be zero) at one frequency given by

$$\omega_0CR = \frac{1}{R_1C_1R_2}$$

That is,

$$\omega_0 = 1/CR \quad (13.12)$$

To obtain sustained oscillations at this frequency, one should set the magnitude of the loop gain to unity. This can be achieved by selecting

$$R_2/R_1 = 2 \quad (13.13)$$

To ensure that oscillations will start, one chooses R_2/R_1 slightly greater than 2. The reader can easily verify that if $R_2/R_1 = 2 + \delta$, where δ is a small number, the roots of the characteristic equation $|T(s)| = 0$ will lie in the right half-plane.

The amplitude of oscillation can be determined and stabilized by using a nonlinear control network. Two different implementations of the amplitude-controlling function are shown in Figs. 13.5 and 13.6. The circuit in Fig. 13.5 employs a symmetric diode limiter of the type studied in Section 13.1. It is formed by diodes D_1 and D_2 together with resistors R_3 , R_4 , R_5 , and R_6 . The limiter operates in the following manner. At the positive peak of the output voltage v_o , the voltage at node 5 will exceed the voltage v_1 (which is about $v_{o(0)}$) and diode D_2 conducts. This will clamp the positive peak to a value determined by R_5 , R_6 , and the negative power supply. The value of the positive output peak can be calculated by setting $v_5 = v_1 + V_{DD}$ and writing a node equation at node 5 while neglecting the current through D_2 . Similarly, the negative peak of the output sine wave will be clamped to the value that causes diode D_1 to conduct. The value of the negative peak can be determined by setting $v_5 = v_1 - V_{DD}$ and writing an equation at node 5 while neglecting the current through D_1 . Finally, note that to obtain a symmetrical output waveform, R_3 is chosen equal to R_4 , and R_5 equal to R_6 .

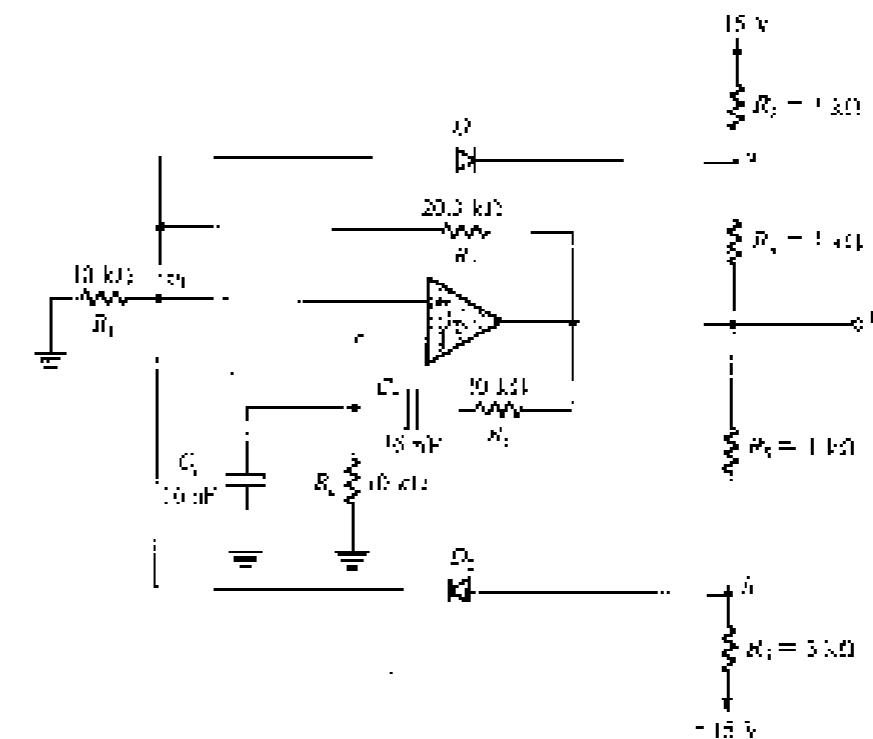


FIGURE 13.5 A Wien-bridge oscillator with a diode limiter for amplitude control.

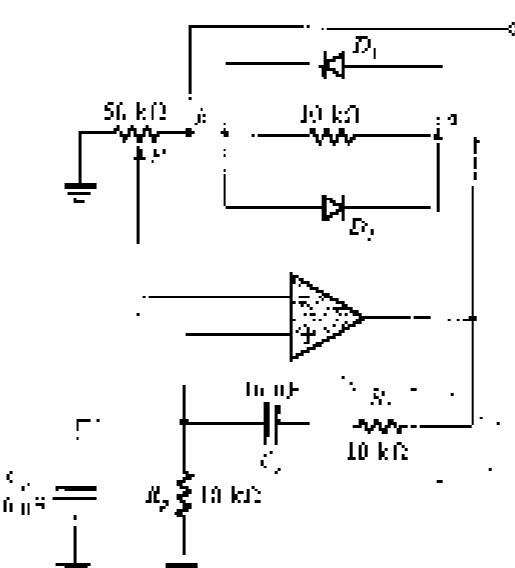


FIGURE 13.6 A Wien-bridge oscillator with an alternative method for amplitude stability.

EXERCISE:

- 13.7 In the circuit in Fig. 13.6, if the value of the loop gain is increased, the frequency of oscillation will increase. Explain why.
- 13.8 For the frequency-selecting circuit in Fig. 13.6, find the angular phase of the output sine wave (assume that the diodes are ideal) at the frequency where the loop gain is unity. Hint: Use the expression for the output voltage of a diode in exponential form.

The circuit of Fig. 13.6 employs an inexpensive implementation of the parameter variation mechanism of amplitude control. Potentiometer P is adjusted until oscillations just start to grow. As the oscillations grow, the diodes start to conduct, causing the effective resistance between a and b to decrease. Equilibrium will be reached at the output amplitude that causes the loop gain to be exactly unity. The output amplitude can be varied by adjusting potentiometer P .

As indicated in Fig. 13.6, the output is taken at point b rather than at the op-amp output terminal because the signal at b has lower distortion (and thus ω_a). To apparent to this point, note that the voltage at b is proportional to the voltage at the op-amp input terminals and that the latter is a filtered (by the RC network) version of the voltage at node a . Node b , however, is a high-frequency node, and a buffer will be needed if a load is to be connected.

EXERCISE:

- 13.9 Calculate the output voltage for the following signal. The output voltage is given by $v_o = 10 \sin(\omega t + 0.23)$ and the op-amp has a gain of 1000. The output voltage is to be fed into a circuit with a load of 100Ω . The output voltage is to be fed into a circuit with a load of 100Ω .

13.2.2 The Phase-Shift Oscillator

The basic structure of the phase-shift oscillator is shown in Fig. 13.7. It consists of a negative gain amplifier ($-K$) with a three-section (high-order) RC ladder network at the feedback. The circuit will oscillate at the frequency for which the phase shift of the RC network is 180° . Only at this frequency will the total phase shift around the loop be 0° or 360° . Here we should note that the reason for using a three-section RC network is that there is the minimum number of sections (i.e., lowest order) that is capable of producing a 180° phase shift at a finite frequency.

For oscillations to be sustained, the value of K should be equal to the inverse of the magnitude of the RC network transfer function at the frequency of oscillation. However, to ensure that oscillations start, the value of K has to be chosen slightly higher than the value



FIGURE 13.7 A phase-shift oscillator.

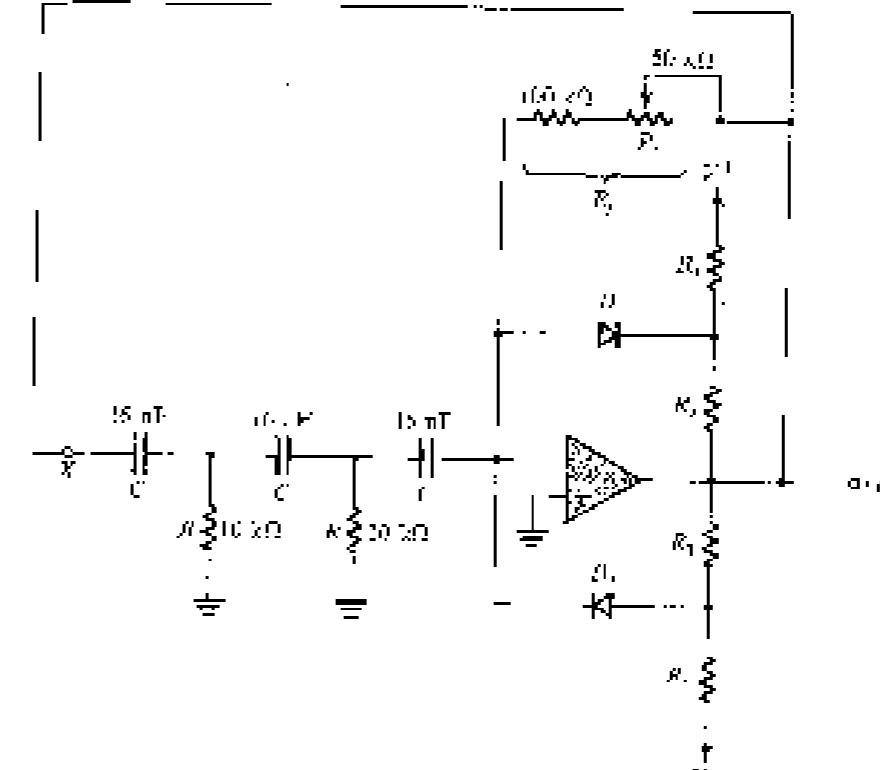


FIGURE 13.8 A practical phase-shift oscillator with amplitude stabilization.

that satisfies the unity-loop-gain condition. Oscillations will then grow in amplitude until dictated by some non-linear control mechanism.

Figure 13.8 shows a practical phase-shift oscillator with a feedback bridge, consisting of diodes D_1 and D_2 and resistors R_8 , R_9 , R_{10} , and R_{11} for amplitude stabilization. To start oscillations, R_8 has to be made slightly greater than the minimum required value. Although the circuit stabilizes more rapidly, and provides sine waves with a one-stable-arm mode, if R_8 is made much larger than this minimum, the price paid is an increased output distortion.

EXERCISES:

- 13.10 Design a phase-shift oscillator with a frequency of 1000 rad/s and a loop gain of 1000 . The op-amp has a gain-bandwidth product of 100 rad/s . To start oscillation, use the minimum required value of R_8 and assume that the other resistors are much smaller than R_8 . The output voltage is to be fed into a circuit with a load of 100Ω .
- 13.11 Use the expressions derived in Problem 13.9 to find the required values of R_8 and the required value of the feedback resistor R_7 for the circuit in Fig. 13.8.
- 13.12 If $R_8 = 100 \Omega$, $R_9 = 100 \Omega$, $R_{10} = 100 \Omega$, and $R_{11} = 100 \Omega$, calculate the frequency of oscillation.

13.2.3 The Quadrature Oscillator

The quadrature oscillator is based on the two-integrator loop studied in Section 12.7. As an active filter, the loop is clamped to locate the poles in the left half of the s plane. Here, the self-clamping will be used, since we wish to locate the poles on the $j\omega$ axis to provide sustained oscillations. To that, we ensure that oscillations start, the poles are initially located in the right half-plane and then "pulled back" by the negative gain control.

Figure 13.9 shows a practical quadrature oscillator. Amplifier 1 is connected as an inverting Miller integrator with a limiter in the feedback for amplitude control. Amplifier 2 is connected as a noninverting integrator (thus bypassing the cascade connection of the Miller integrator and the inverter in the two-integrator loop of Fig. 12.28(a)). To understand the operation of this noninverting integrator, consider the equivalent circuit shown in Fig. 13.9(b). Here, we have replaced the integrated input voltage v_{o1} and the series resistance $2R$ by the Norton equivalent composed of a current source $v_{o1}/2R$ and a parallel resistance $2R$. Now, since $v_{o2} = 2v$, where v is the voltage at the input of opamp 2, the current through R_2 will be $(2v - v_{o1})/R_2 = v/R_2$, in the direction from output to input 2. Thus, R_2 gives rise to a negative input resistance, $-R_2$, as indicated in the equivalent circuit of Fig. 13.9(b). Normally, R_2 is made equal to $2R$, and thus $-R_2$ cancels $2R$, and at the input we are left with a current source $v_{o1}/2R$ feeding a capacitor C . The result is that $v = \frac{1}{j\omega RC}$ and $v_{o2} = 2v = \frac{1}{j\omega RC}v_{o1}$. Thus, for $R_2 = 3R$, the circuit functions as a perfect noninverting integrator. If, however, R_2 is made smaller than $2R$, a net negative resistance appears in parallel with C .

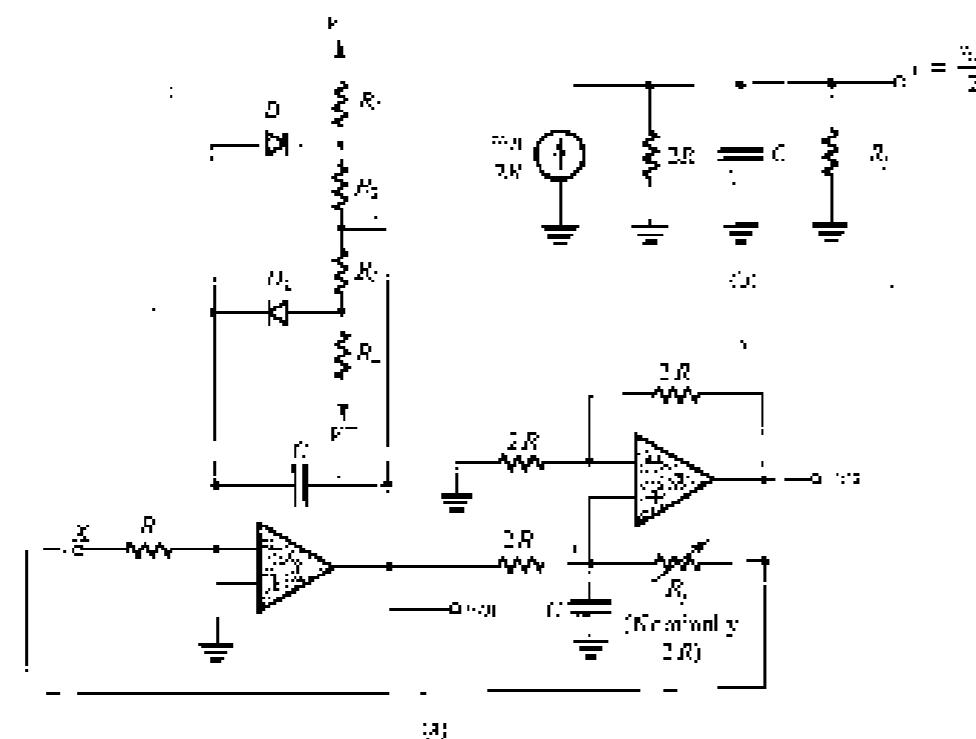


FIGURE 13.9 (a) A quadrature oscillator circuit. (b) Equivalent circuit of the input of opamp 2.

Referring to the oscillator circuit in Fig. 13.9(a), we note that the resistance R_2 in the positive-feedback path of opamp 2 is made variable, with a nominal value of $2R$. Decreasing the value of R_2 moves the poles to the right in s -plane (Problem 13.19) and ensures that the oscillations start. Too much positive feedback, although it results in better amplitude stability, also results in higher output distortion (because the buffer has to operate "harder"). In this regard, note that the output v_{o2} will be "purer" than v_{o1} because of the filtering action provided by the second integrator on the peak-limited output of the first integrator.

If we disregard the limiter and focus the loop at X , the loop gain can be obtained as

$$L(s) = \frac{V_{o2}}{V_i} = -\frac{1}{s^2 C^2 R^2} \quad (13.14)$$

Thus, the loop will oscillate at frequency ω_0 , given by

$$\omega_0 = \frac{1}{CR} \quad (13.15)$$

Finally, it should be pointed out that the name *quadrature oscillator* is used because the circuit provides two sinusoids with 90° phase difference. This should be obvious, since v_{o2} is the integral of v_{o1} . There are many applications for which quadrature sinusoids are required.

13.2.4 The Active-Filter-Tuned Oscillator

The last oscillator circuit that we shall discuss is quite simple both in principle and in design. Nevertheless, the approach is general and versatile and can result in high-quality (i.e., low-distortion) output sine waves. The basic principle is illustrated in Fig. 13.10. The circuit consists of a high-Q bandpass filter connected in a positive feedback loop with a hard limiter. To understand how this circuit works, assume that oscillations have already started. The output of the bandpass filter will be a sine wave whose frequency is equal to the center frequency of the filter, f_0 . The sine-wave signal v is fed to the limiter, which produces at its output a square-wave voltage whose levels are determined by the limiting levels and whose

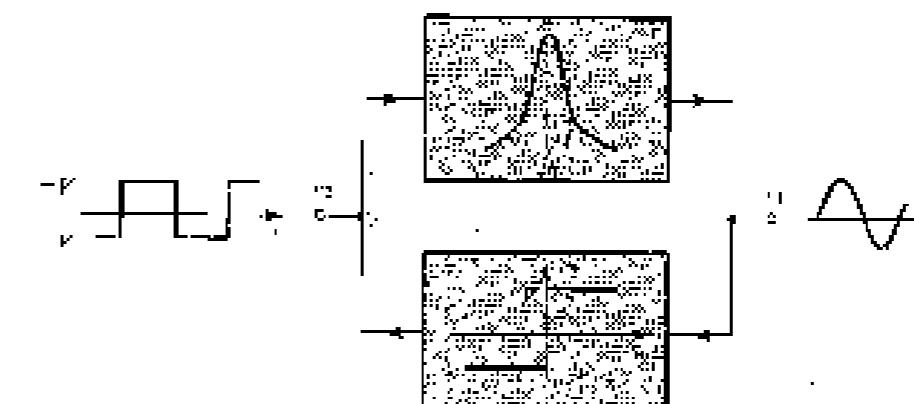


FIGURE 13.10 Block diagram of the active-filter-tuned oscillator.

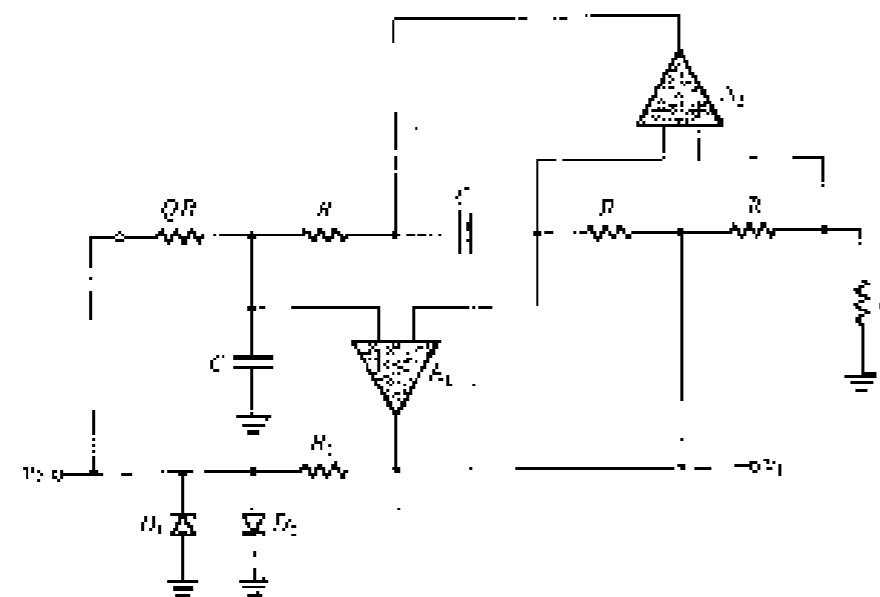


FIGURE 13.11 A voltage implementation of the active RC sine-wave oscillator.

frequency is f_0 . The square wave in turn is fed to the bandpass filter, which filters out the harmonics and provides a sinusoidal output v_o at the fundamental frequency f_0 . Obviously, the purity of the output sine wave will be a direct function of the selectivity (or Q factor) of the bandpass filter.

The simplicity of this approach to oscillator design should be apparent. We have independent control of frequency and amplitude as well as of distortion of the output waveform. Any filter circuit with positive gain can be used to implement the bandpass filter. The frequency stability of the oscillator will be directly determined by the frequency stability of the bandpass filter circuit. Also, a variety of timer circuits (see Chapter 3) with different degrees of sophistication can be used to implement the timer block.

Figure 13.11 shows one possible implementation of the active-filter-tuned oscillator. This circuit uses a variation on the bandpass circuit based on the Armstrong inductance simulation circuit (see Fig. 12.22c). Here resistor R_2 and capacitor C_1 are interchanged. This makes the output of the lower op amp directly proportional to (in fact, twice as large as) the voltage across the resonator, and we can therefore dispense with the buffer amplifier A_2 . The timer used is a very simple one consisting of a resistor R_1 and two diodes.

EXERCISE

13.11 Design an active-filter-tuned oscillator of the type shown in Figure 13.11. Use an LM356 op amp and a 10-pF ceramic resonator. The required frequency is 100 Hz. Assume a peak-to-peak output voltage of 1 V. The required Q factor is 10. The required amplitude is 10 mV. The required distortion is less than 1%.

13.12 Design an active-filter-tuned oscillator of the type shown in Figure 13.11. Use an LM356 op amp and a 10-pF ceramic resonator. The required frequency is 100 Hz. Assume a peak-to-peak output voltage of 1 V. The required Q factor is 10. The required amplitude is 10 mV. The required distortion is less than 1%.

13.2.5 A Final Remark

The op-amp RC oscillator circuits studied are useful for operation in the range 10 Hz to 100 kHz (or perhaps 1 MHz at most). Whereas the lower frequency limit is dictated by the size of passive components required, the upper limit is governed by the frequency-response and slew-rate limitations of op-amps. For higher frequencies, circuits that employ transistors together with LC-tuned circuits or crystals are frequently used.⁷ These are discussed in Section 13.3.

13.3 LC AND CRYSTAL OSCILLATORS

Oscillators utilizing transistors (JFETs or BJT's), with LC-tuned circuits or crystals as feedback elements, are used in the frequency range of 100 kHz to hundreds of megahertz. They exhibit higher Q than the RC types. However, LC oscillators are difficult to tune over wide ranges, and crystal oscillators operate at a single frequency.

13.3.1 LC-Tuned Oscillators

Figure 13.12 shows two commonly used configurations of LC-tuned oscillators. They are known as the Colpitts oscillator and the Hartley oscillator. Both utilize a parallel LC circuit connected between collector and base (or between drain and gate if a FET is used) with a fraction of the tuned-circuit voltage fed to the emitter (thus giving it a FET). The feedback is achieved by way of a capacitive divider in the Colpitts oscillator and by way of an inductive divider in the Hartley circuit. To focus attention on the oscil. board's structure, the bias details are not shown. In both circuits, the resistor R models the combination of the losses of the inductors, the bias resistance of the open base, and the output resistance of the transistor.

If the frequency of operation is sufficiently low that we can neglect the reactive capacitances, the frequency of oscillation will be determined by the resonance frequency of the parallel-tuned circuit (also known as a tank circuit because it behaves as a reservoir for energy).

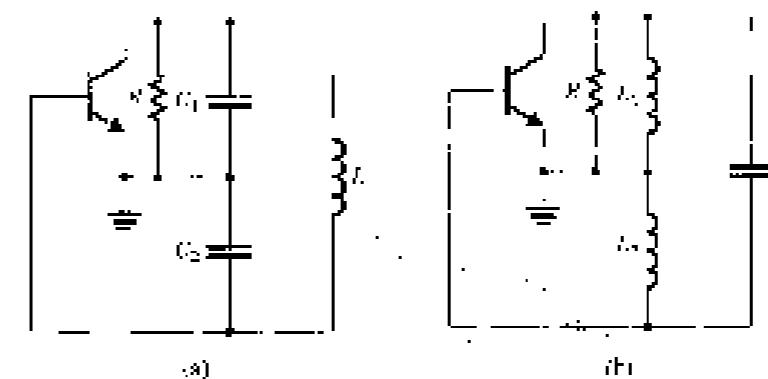


FIGURE 13.12 Two standard configurations of LC-tuned oscillators: (a) Colpitts and (b) Hartley.

⁷ Colpitts oscillators can be used in place of the op-amps in the circuits just studied. At higher frequencies, however, better results are obtained with LC-tuned circuit and crystals.

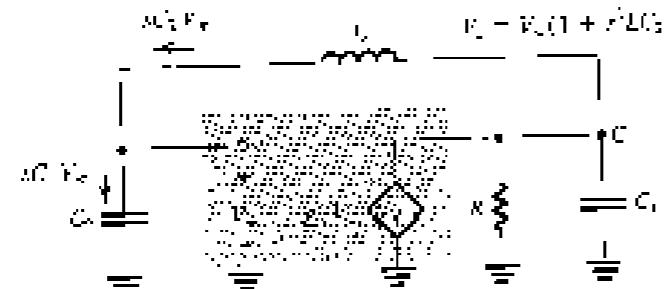


FIGURE 13.13 Schematic circuit of the Colpitts oscillator (a BJT). To simplify the analysis, C_1 and R are neglected. We can consider C_2 to be equal to C_3 , and we can neglect r_e in g_m .

energy storage). Thus for the Colpitts oscillator we have

$$\omega_0 = \frac{1}{\sqrt{L(C_1 + C_2)}} \quad (13.20)$$

and for the Hartley oscillator we have

$$\omega_0 = 1/\sqrt{(L_1 + L_2)C} \quad (13.21)$$

The ratio L_1/L_2 or C_1/C_2 determines the feedback factor and thus must be adjusted in conjunction with the transistor gain, to ensure that oscillations will start. To determine the oscillation condition for the Colpitts oscillator, we replace the transistor with its equivalent circuit, as shown in Fig. 13.13. To simplify the analysis, we have neglected the transistor shunt load, as shown in Fig. 13.13. To simplify the analysis, we have neglected the transistor capacitance C_{ce}/C_{cb} for a FET. Capacitance C_{ce} (C_{cb} for a FET), although not shown, can be considered in parallel with C_2 . The intrinsic resistance r_e (intrinsic r_{ds} for a FET) has also been neglected, assuming that at the frequency of oscillation $r_e \gg (1/g_m C_1)$. Finally, by neglecting R , the resistance R includes r_s of the transistor.

To find the loop gain, we apply an input voltage V_{in} and find the returned voltage that appears across the drain terminals of the transistor. We then equate the loop gain to unity. An alternative approach is to analyze the circuit and then determine all current and voltage variables, and then write one equation that governs circuit operation. Oscillations will start if this equation is satisfied. Thus the resulting equation will give us the conditions for oscillation.

A small deviation of the transistor collector current (I_C) in the circuit of Fig. 13.13 yields

$$\Delta C_1 V_{in} - g_m V_{in} + \frac{1}{R} + \omega_0^2 (1 - \omega^2 L C_2) V_{in} = 0$$

Since V_{in} and ΔV_{in} have already been eliminated, this equation can be rearranged as follows:

$$\omega_0^2 L C_2 + \omega_0^2 (L C_2/R) + 2(C_1 - C_2) - \left(g_m - \frac{1}{R}\right) = 0 \quad (13.22)$$

Substituting $\omega = j\omega_0$ gives

$$\left(g_m - \frac{1}{R} - \frac{\omega_0^2 L C_2}{R}\right) + j\omega(C_1 + C_2) - \omega^2 L C_2 = 0 \quad (13.23)$$

For oscillations to start, both the real and imaginary parts must be zero. Equating the imaginary part to zero gives the frequency of oscillation as

$$\omega_0 = \frac{1}{\sqrt{L(C_1 + C_2)}} \quad (13.24)$$

which is the resonance frequency of the tank circuit, as anticipated.⁴ Equating the real part to zero together with using Eq. (13.20) gives

$$C_2/C_1 = g_m R \quad (13.25)$$

which has a simple physical interpretation: For sustained oscillations, the magnitude of the gain from base to collector ($g_m R$) must be equal to the inverse of the voltage to be provided by the resistive divider, which from Fig. 13.13(a) can be seen to be $(1/g_m)(1 - C_1/C_2)$. Of course, for oscillations to start, the loop gain must be made greater than unity, a condition that can be stated in the equivalent form:

$$g_m R > C_2/C_1 \quad (13.26)$$

As oscillations grow in amplitude, the transistor's nonlinear characteristics reduce the effective value of g_m and, correspondingly, reduce the loop gain to unity, thus sustaining the oscillations.

Analysis similar to the foregoing can be carried out for the Hartley circuit (see Exercise 13.20). At high frequencies, more accurate transistor models must be used. Alternatively, the parameters of the transistor can be measured at the intended frequency ω_0 , and the analysis can then be carried out using the y -parameter model (see Appendix B). This is usually simpler and more accurate, especially at frequencies above about 10% of the transistor's f_T .

As an example of a practical LC oscillator we show in Fig. 13.14 the circuit of a Colpitts oscillator, complete with bias details. Here the radio-frequency choke (RFC) provides a high impedance to dc but a low dc resistance.

Finally, a few words are in order on the mechanism that determines the amplitude of oscillations in the LC-tuned oscillators discussed above. Unlike the ordinary oscillators that incorporate special amplitude-control circuitry, LC-tuned oscillators utilize the nonlinear $i-v-i$ characteristics of the BJT (the $i-v-i$ characteristics of the FETs for amplitude control). Thus these LC-tuned oscillators are known as self-sustaining oscillators. Specifically, as the oscillations grow in amplitude, the effective gain of the transistor is reduced below its small-signal value. Eventually, an amplitude is reached at which the effective gain is reduced to the point that the Barkhausen criterion is satisfied exactly. The amplitude then remains constant at this value.

Reliance on the nonlinear characteristics of the BJT (or the FET) implies that the collector (drain) current waveform will be nonlinearly distorted. Nevertheless, the output voltage signal will still be a sinusoid of high purity because of the filtering action of the LC tuned circuit. Detection and loss of amplitude control, which makes use of nonlinear-circuit techniques, is beyond the scope of this book.

⁴If r_s is taken into account, the frequency of oscillation can be shown to drift slightly from the value given by Eq. (13.24).

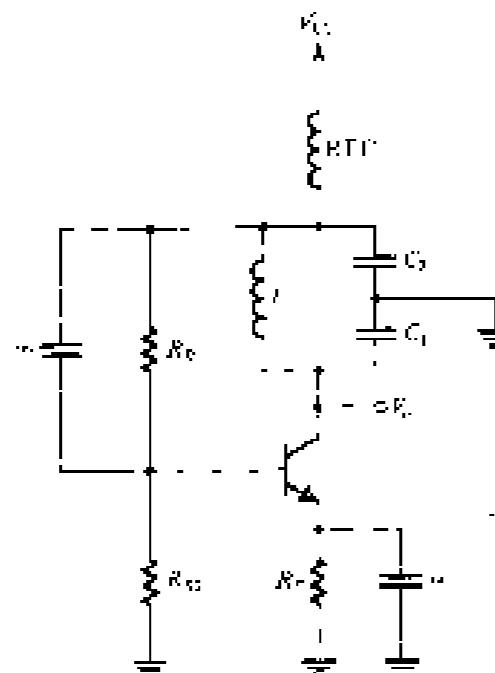


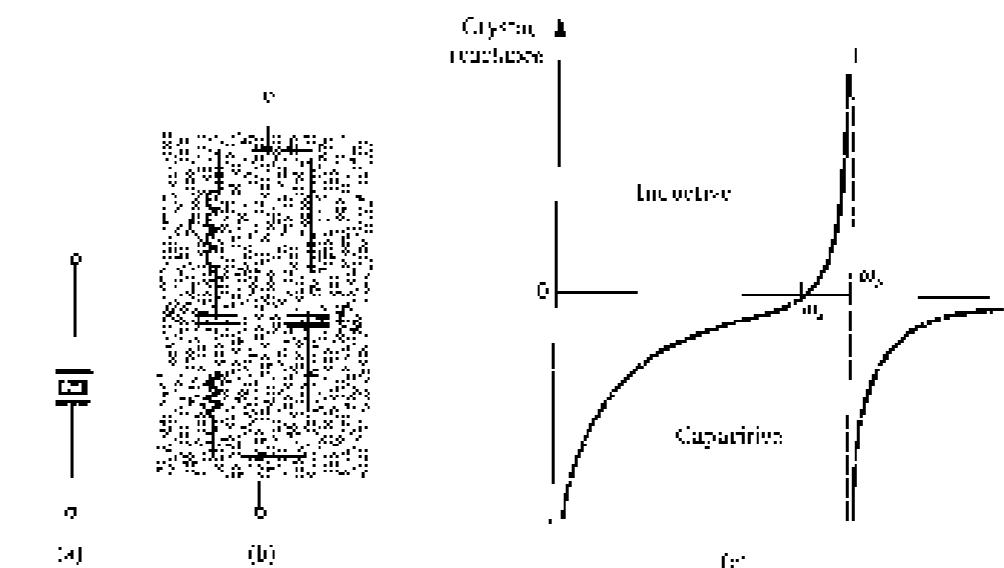
FIGURE 13.14 Coupled-circuit LC voltage oscillator.

EXERCISES

- 13.3.1 Sketch the tank circuit equivalent circuit for the circuit shown in Fig. 13.14. Calculate the parallel resonance frequency ω_0 and the Q factor.
- 13.3.2 If the crystal has a series resistance $r = 10 \Omega$, calculate the Q factor of the circuit. Assume $C_s = 100 \text{ pF}$, $C_p = 10 \text{ pF}$, $L = 10 \mu\text{H}$, and $\omega_0 = 10^6 \text{ rad/s}$. Express your answer in terms of the Q factor.
- 13.3.3 If the crystal has a series resistance $r = 10 \Omega$, calculate the Q factor of the circuit. Assume $C_s = 100 \text{ pF}$, $C_p = 10 \text{ pF}$, $L = 10 \mu\text{H}$, and $\omega_0 = 10^6 \text{ rad/s}$. Express your answer in terms of the Q factor.
- 13.3.4 If the crystal has a series resistance $r = 10 \Omega$, calculate the Q factor of the circuit. Assume $C_s = 100 \text{ pF}$, $C_p = 10 \text{ pF}$, $L = 10 \mu\text{H}$, and $\omega_0 = 10^6 \text{ rad/s}$. Express your answer in terms of the Q factor.

13.3.2 Crystal Oscillators

A piezoelectric crystal, such as quartz, exhibits electromechanical-resonance characteristics that are very stable (with time and temperature) and highly selective (having very high Q factors). The circuit symbol of a crystal is shown in Fig. 13.15(a), and its equivalent circuit model is given in Fig. 13.15(b). The resonance properties are characterized by a large inductance L (as high as hundreds of henrys), a very small series capacitance C_s (as small as 0.0005 pF), a series resistance r (representing a Q factor Q_{crystal} that can be as high as a few hundred thousand), and a parallel capacitance C_p (a few picofarads). Capacitor C_s represents the electrostatic capacitance between the two parallel plates of the crystal. Note that $C_s \ll C_p$.

FIGURE 13.15 (a) Piezoelectric crystal. (b) Circuit symbol. (c) Equivalent circuit. (d) Crystal resistance versus frequency (ω) is flat, except at resonance, ω_0 ; $Z_{\text{crystal}}(\omega_0) = Q_{\text{crystal}}(X_{\text{crystal}})$.

Since the Q factor is very high, we may neglect the resistance r and express the crystal impedance as

$$Z(\omega) = j \left[\frac{1}{j\omega C_s} + \frac{1}{j\omega L + 1/jC_p} \right]$$

which can be manipulated to the form

$$Z(\omega) = \frac{j\omega^2 - j/(LC_p)}{\omega^2 + [(C_s + C_p)/LC_p] \omega^2} \quad (13.23)$$

From Eq. (13.23) and from Fig. 13.15(b) we see that the crystal has two resonance frequencies: a series resonance at ω_0 ,

$$\omega_0 = 1/\sqrt{LC_p} \quad (13.24)$$

and a parallel resonance at ω_1 ,

$$\omega_1 = 1/\sqrt{\left(\frac{C_s C_p}{C_s + C_p} \right)} \quad (13.25)$$

Thus, for $\omega = j\omega_0 \omega_0$ we write

$$Z(j\omega) = \frac{1}{j\omega C_p} \left[\frac{\omega_0^2 - \omega^2}{\omega^2 + \omega_0^2} \right] \quad (13.26)$$

From Eqs. (13.24) and (13.25) we note that $\omega_0 > \omega_1$. However, since $C_s \gg C_p$ the two resonance frequencies are very close. Expressing $Z(j\omega) = R(j\omega)$, the crystal resistance $R(j\omega)$ will

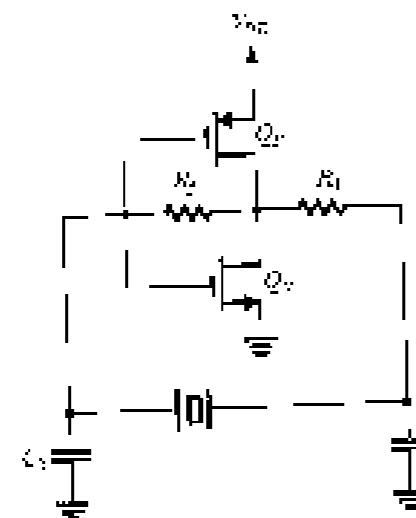


FIGURE 13.15 A three-stage oscillator built by Okko's investors and engineer.

have the shape shown in Fig. 13.15(c). We observe that the crystal resonance is inductive over the very narrow frequency band between ω_1 and ω_2 . For a given crystal, this frequency band is well defined. Thus we may use the crystal to replace the inductor of the Colpitts oscillator (Fig. 13.12(a)). The resulting circuit will oscillate at the resonance frequency of the crystal inductance L with the series combination of C_1 and $(C_2 + C_{\text{cr}})/C_2(C_1 + C_{\text{cr}})$. Since C_{cr} is much smaller than the sum of other capacitances, it will be dominant and

$$q_1 \in \mathcal{C}_1 \cap \mathcal{C}_2 \equiv q_2 \quad (13.26)$$

In addition to the basic Colpitts oscillator, a variety of configurations exist for crystal oscillators. Figure 13.16 shows a popular configuration (called the Pierce oscillator) utilizing a CMOS inverter (see Section 4.10) as amplifier. Resistor R_2 determines a dc operating point at the high-gain region of the CMOS inverter. Resistor R_1 together with capacitor C_1 provides a low-pass filter that discourages the circuit from oscillating at a higher harmonic of the crystal frequency. Note that this circuit also is based on the Colpitts configuration.

The extremely stable resonance characteristics and the very high Q factors of quartz crystals result in oscillators with very accurate and stable frequencies. Crystal oscillators available with resonance frequencies in the range of few kilohertz to hundreds of megahertz have temperature coefficients of Δf of ± 2 parts per million (ppm) per degree Celsius or better. Unfortunately, however, crystal oscillators, being mechatronic resonators, are high-frequency circuits.

13.4 BISTABLE MULTIVIBRATORS

In this section we begin the study of waveform-generating circuits of the other type — nonlinear oscillators or function generators. These devices make use of a special class of circuits known as multivibrators. As mentioned earlier, there are three types of multivibrator: bistable, monostable, and astable. This section is concerned with the first, the bistable multivibrator.

As its name indicates, the bistable multivibrator has two stable states. The circuit can remain in either stable state indefinitely and moves to the other stable state only when appropriate triggering.

13.4.1 The Feedback Loop

Bistability can be obtained by connecting a dc amplifier in a positive-feedback loop having a loop gain greater than unity. Such a feedback loop is shown in Fig. 13-17; it consists of an op amp and a resistive voltage divider in the positive-feedback path. To see how bistability is obtained, consider operation with the positive input terminal of the op amp near ground potential. This is a reasonable starting point since the circuit has no external excitation. Assume that the electrical noise, v_n , inevitably present in every electronic circuit causes a small positive increment in the voltage v_1 . This incremental signal will be amplified by the large open-loop gain A of the op amp, with the result that a much greater signal will appear in the op amp's output voltage v_0 . The voltage divider (R_1, R_2) will feed a fraction $\beta = R_1/(R_1 + R_2)$ of the output signal back to the positive input terminal of the op amp. If $A\beta >$ greater than unity, as is usually the case, the fed-back signal will be greater than the original increment in v_1 . This regenerative process continues until eventually the op amp saturates with its output voltage at the positive supply level, V_+ . When this happens, the voltage at the positive input terminal, v_1 , becomes $V_+R_2/(R_1 + R_2)$, which is positive and thus keeps the op amp in positive saturation. This is one of the two stable states of the circuit.

In the description above we assumed that when v_1 was near zero volts, a positive measurement occurred in v_2 . Had we assumed the equally probable situation of a negative measurement, the op amp would have ended up saturated in the negative direction with $v_{o2} = b_2$ and $v_1 = k_1 B_1 (B_2 + B_3) \cdot 1/k_2$ (i.e., the initial steady state).

We thus conclude that the circuit of Fig. 13.17 has two stable states, one with the op-amp in positive saturation and the other with the op-amp in negative saturation. The circuit can exist in either of these two states indefinitely. We also note that the circuit cannot exist in the state for which $v_+ = 0$ and $v_- = 0$ for very long of time. This is a state of unstable equilibrium (also known as a metastable state); any disturbance, such as that caused by a slight variation

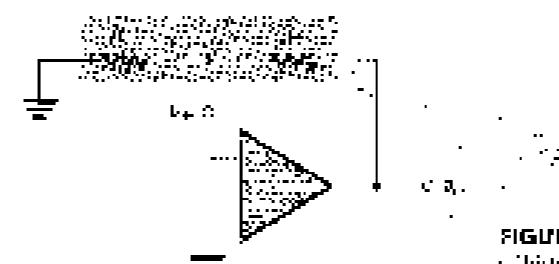


FIGURE T3.17 A positive feedback loop with self-limiting output.

² Dual implementations of dual derivatives were presented in Chapter 11. Here, we are interested in implementations utilizing optionals.

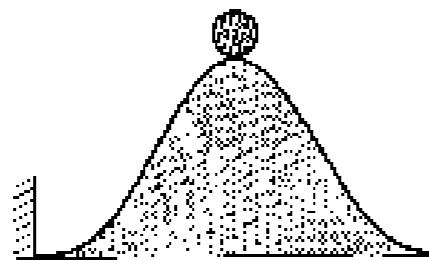


FIGURE 13.18 A physical analogy for the operation of the bistable circuit. The ball can't return to the top of the hill for any length of time if it's set in motion (equilibrium is metastable); a small, temporary, perturbation will cause the ball to fall to one side or the other, where it can remain indefinitely (the two stable states).

causes the bistable circuit to switch to one of its two stable states. This is in sharp contrast to the case where the feedback is negative, causing a virtual short circuit to appear between the op amp's input terminals and maintaining this virtual short circuit in the face of disturbances. A physical analogy for the operation of the bistable circuit is depicted in Fig. 13.18.

13.4.2 Transfer Characteristics of the Bistable Circuit

The question naturally arises as to how we can make the bistable circuit of Fig. 13.17 change state. To help answer this crucial question, we derive the transfer characteristics of the bistable. Reference to Fig. 13.17 indicates that either of the two circuit nodes that are connected to ground can serve as an inverter terminal. We investigate both possibilities.

Figure 13.19(a) shows the bistable circuit with a voltage v_2 applied to the inverting input terminal of the op amp. To derive the transfer characteristic v_0 vs. v_2 , assume that v_0 is at one of its two possible levels, say L_+ , and thus $v_1 = \beta L_+$. Now as v_2 is increased from 0 V, we can see from the circuit that nothing happens until v_2 reaches a value equal to v_1 (i.e., βL_+). As v_2 begins to exceed this value, a net negative voltage develops between the input terminals of the op amp. This voltage is amplified by the open-loop gain of the op amp, and thus v_0 goes negative. The voltage divider circuit causes v_1 to go negative, thus inverting the net negative input to the op amp...and keeping the regenerative process going. This process culminates in the op amp saturating in the negative direction; that is, with $v_2 = L_+$ and, correspondingly, $v_0 = \beta L_+$. It is easy to see that increasing v_2 further has no effect on the acquired state of the bistable circuit. Figure 13.19(b) shows the transfer characteristic for increasing v_2 . Observe that the characteristic is that of a comparator with a threshold voltage denoted V_{th+} , where $V_{th+} = \beta L_+$.

Next consider what happens as v_2 is decreased. Since now $v_2 = \beta L_+$, we see that the circuit remains in the negative-saturation state until v_2 goes negative to the point that it equals βL_- . As v_2 goes below this value, a net positive voltage appears between the op amp's input terminals. This voltage is amplified by the open-loop gain and thus gives rise to a positive voltage at the op amp's output. The regenerative action of the positive-feedback loop then sets in and causes the circuit eventually to go to its positive-saturation state, in which $v_0 = L_+$ and $v_1 = \beta L_-$. The transfer characteristic for decreasing v_2 is shown in Fig. 13.19(c). Here again we observe that the characteristic is that of a comparator, but with a threshold voltage $V_{th-} = \beta L_-$.

The complete transfer characteristics, v_0 vs. v_2 , of the circuit in Fig. 13.19(a) can be obtained by combining the characteristics in Fig. 13.19(b) and (c), as shown in Fig. 13.19(d). As indicated, the circuit changes state at di. crit. values of v_2 , depending on whether v_2 is increasing or decreasing. Thus the circuit is said to exhibit hysteresis; the width of the hysteresis is the difference between the high threshold V_{th+} and the low threshold V_{th-} . Also note that the bistable circuit is in effect a comparator with hysteresis. As will be shown shortly, adding hysteresis to a comparator's characteristics can be very beneficial in certain applications. Finally, observe that because the bistable circuit of Fig. 13.19 switches from the positive state ($v_0 = L_+$) to the negative state ($v_0 = L_-$) as v_2 is increased past the positive threshold V_{th+} , the circuit is said to be nonresetting. A bistable circuit with a nonresetting transfer characteristic will be presented shortly.

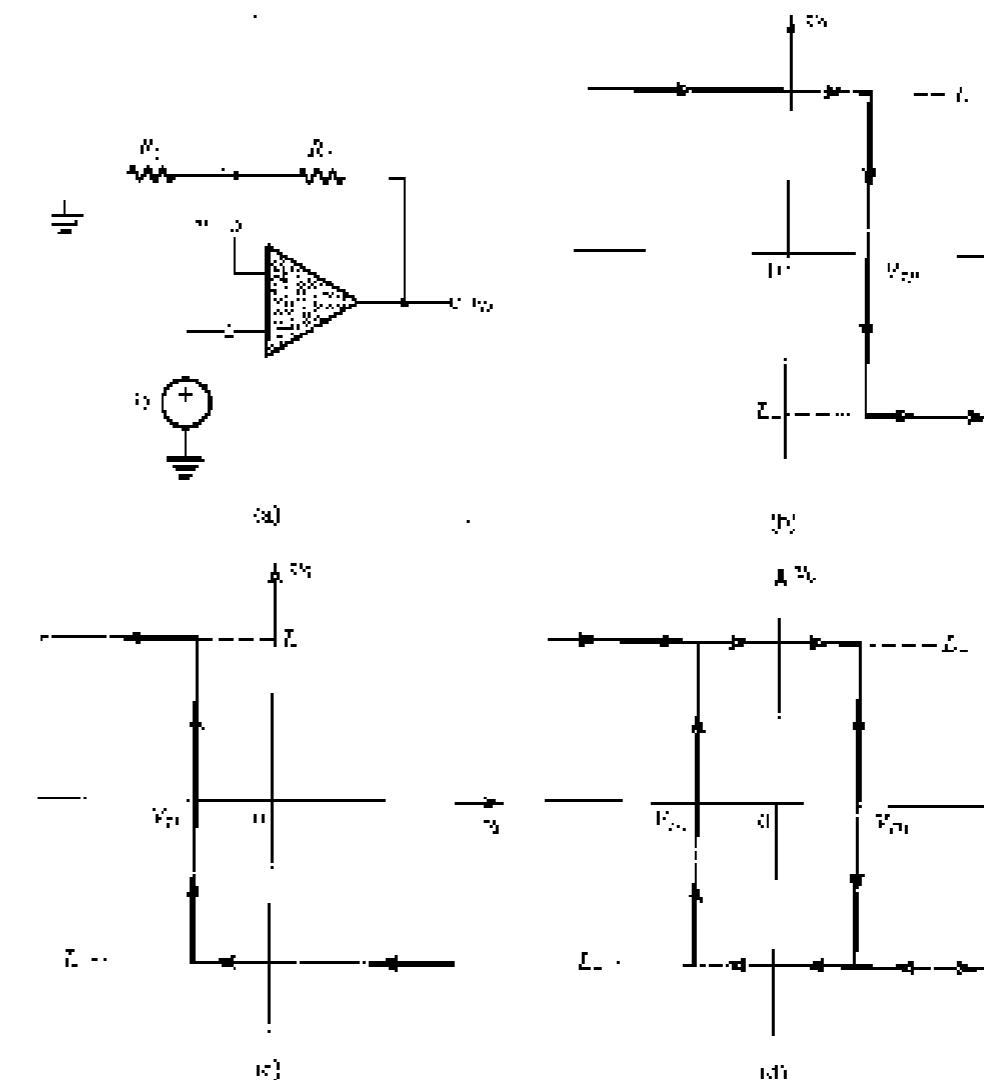


FIGURE 13.19 (a) The bistable circuit of Fig. 13.17 with the inverting input terminal of the op amp disconnected from ground and connected to an input signal v_2 . (b) The transfer characteristic of the circuit in (a) for increasing v_2 ; (c) the transfer characteristic for decreasing v_2 ; (d) the complete hysteresis.

13.4.3 Triggering the Bistable Circuit

Returning now to the question of how to make the bistable circuit change state, we observe from the transfer characteristics of Fig. 13.19(d) that if the circuit is in the L_+ state, it can be switched to the L_- state by applying an input v_2 of value greater than $V_{th-} = \beta L_-$. Such an input causes a net negative voltage to appear between the input terminals of the op amp, which initiates the regenerative cycle that culminates in the circuit switching to the L_- stable state. Here it is important to note that the input is merely initiates or triggers reactivation. Thus we can conceive of v_2 with no effect on the regeneration process. In other words, v_2 can be simply a pulse of short duration. The input signal v_2 is thus referred to as a trigger signal, or simply a trigger.

The characteristics of Fig. 13.19(d) indicate also that the bistable circuit can be switched to the positive state ($v_0 = L_+$) by applying a negative trigger signal v_2 of magnitude greater than that of the negative threshold V_{th-} .

13.4.4 The Bistable Circuit as a Memory Element

We observe from Fig. 13.19(c) that for input voltages in the range $V_{IN} < v_I < V_{TH}$ the output can be either L_+ or L_- , depending on the state that the circuit is already in. Thus, for this input range, the output is determined by the previous value of the trigger signal (the trigger signal that caused the circuit to be in its current state). Thus the circuit exhibits memory. Indeed, the bistable multivibrator is the basic memory element of digital systems, as we have seen in Chapter 11. Finally, note that in analog circuit applications, such as the ones of concern to us in this chapter, the bistable circuit is also known as a **Schmitt trigger**.

13.4.5 A Bistable Circuit with Noninverting Transfer Characteristics

The basic bistable feedback loop of Fig. 13.17 can be used to derive a circuit with noninverting transfer characteristics by applying the input signal v_I (the trigger signal) to the terminal of R_1 that is connected to ground. The resulting circuit is shown in Fig. 13.20(a). To obtain the transfer characteristic we first employ superposition to the linear circuit formed by R_1 and R_2 , thus expressing v_O in terms of v_I and v_T as

$$v_O = v_T \frac{R_2}{R_1 + R_2} + v_T \frac{R_1}{R_1 + R_2} \quad (13.28)$$

From this equation we see that if the circuit is in the positive stable state with $v_O = L_+$, positive values for v_I will have no effect. To trigger the circuit from the L_- state, v_I must be made negative and of such a value as to make v_O decrease below zero. Thus the low threshold V_{TH} can be found by substituting in Eq. (13.28) $v_O = L_-, v_I = 0$, and $v_T = V_T$. The result is

$$V_{TH} = -L_+ (R_1/R_2) \quad (13.29)$$

Similarly, Eq. (13.28) indicates that when the circuit is in the negative-output state ($v_O = L_-$), negative values of v_I will make v_O more negative with no effect on operation. To initiate the regeneration process that causes the circuit to switch to the positive state, v_I must be made

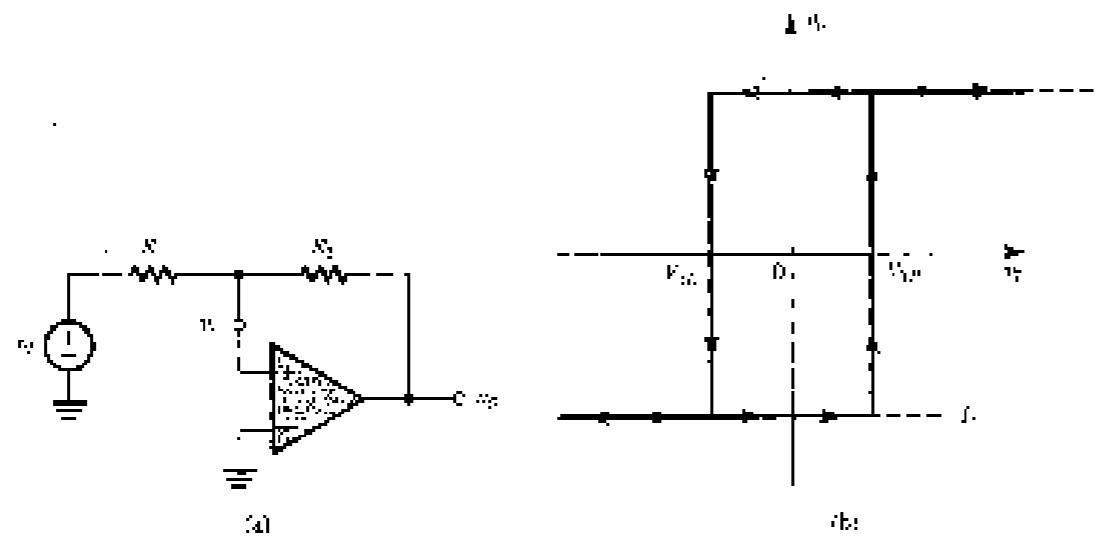


FIGURE 13.20 (a) A block diagram of the positive-feedback loop of Fig. 13.17 by applying v_I through R_1 (b) The transfer characteristic of the circuit in (a) is noninverting. (Compare it to the inverting characteristic in Fig. 13.20c.)

to go slightly positive. The value of v_I that causes this to happen is the high threshold voltage V_{TH} , which can be found by substituting in Eq. (13.28) $v_O = L_+$ and $v_T = 0$. The result is

$$V_{TH} = -L_+ (R_1/R_2) \quad (13.29)$$

The complete transfer characteristic of the circuit of Fig. 13.20(a) is displayed in Fig. 13.20(b). Observe that a positive triggering signal v_I (of value greater than V_{TH}) causes the circuit to switch to the positive state (v_O goes from L_- to L_+). Thus the transfer characteristic of this circuit is noninverting.

13.4.6 Application of the Bistable Circuit as a Comparator

The comparator is an analog-circuit building block that is used in a variety of applications ranging from detecting the level of an input signal relative to a pre-set threshold value, to the design of analog-to-digital (A/D) converters (see Section 9.5). Although we normally think of the comparator as having a single threshold value (see Fig. 13.21a), it is useful in many applications to add hysteresis to the comparator characteristics. If this is done, the comparator exhibits two threshold values, V_{TH} and $V_{TH'}$, symmetrically placed about the

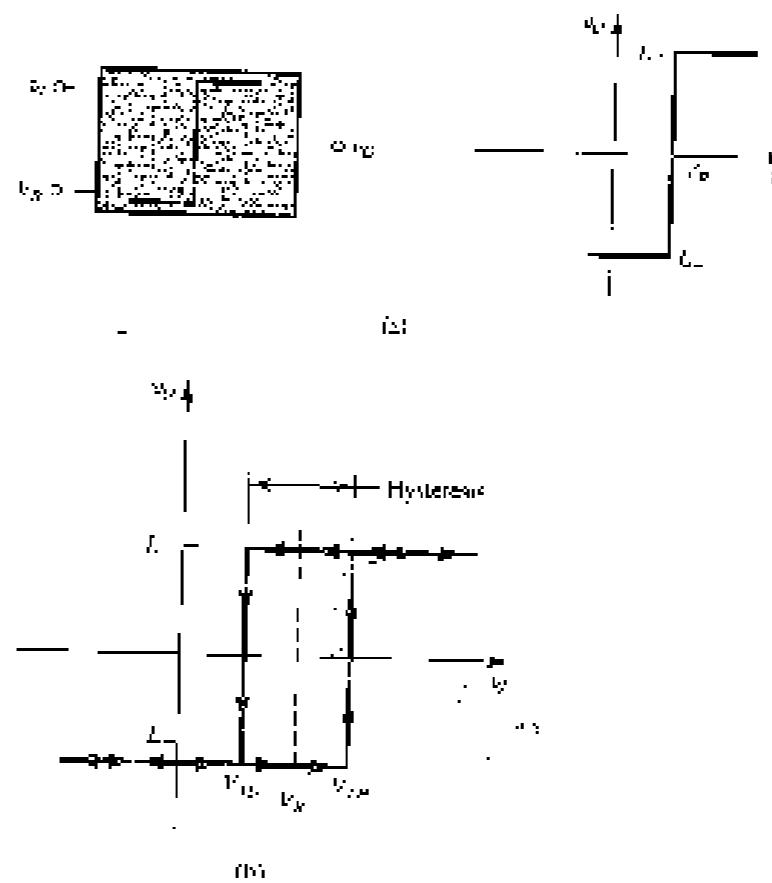


FIGURE 13.21 (a) Block diagram representing the transfer characteristic for a comparator having a unique threshold voltage V_{TH} . (b) Transfer characteristic with hysteresis.

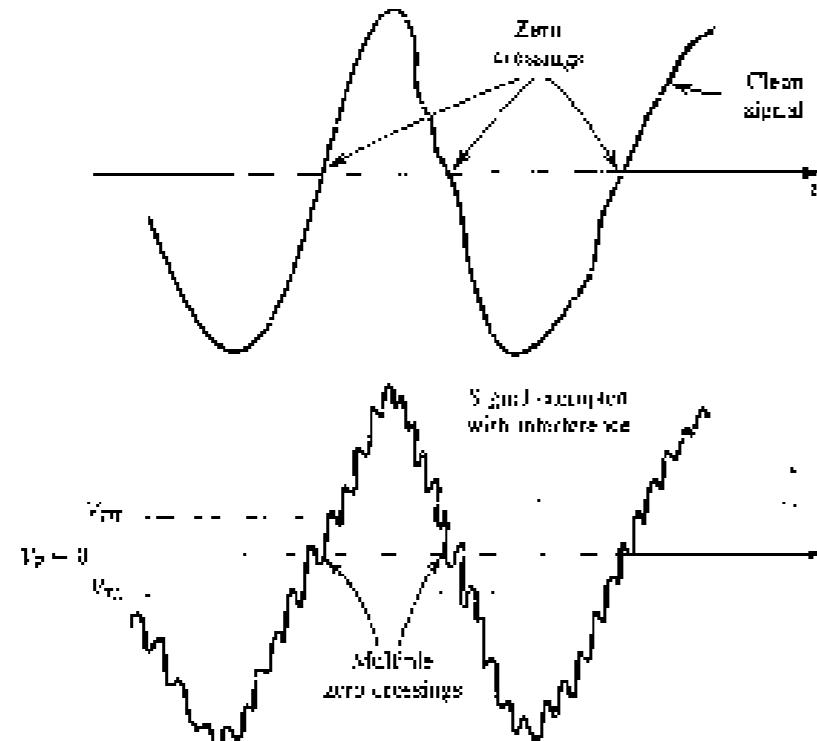


FIGURE 13.22 Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference.

desired reference level, as indicated in Fig. 13.21(B). Usually V_{D1} and V_{D2} are separated by a small amount, say 100 mV.

To demonstrate the need for hysteresis we consider a common application of comparators. It is required to design a circuit that detects and counts the zero crossings of an arbitrary waveform. Such a function can be implemented using a comparator whose threshold is set to 0 V. The comparator provides a step change in its output every time a zero crossing occurs. Each step change can be used to generate a pulse, and the pulses are fed to a counter circuit.

Imagine now what happens if the signal being processed has—a signal that usually does have—interference superimposed on it, say of a frequency much higher than that of the signal. It is known that the signal might cross the zero axis a number of times around each of the zero-crossing points we are trying to detect, as shown in Fig. 13.22. The comparator would thus change state a number of times at each of the zero crossings, and our count would obviously be in error. However, if we have an idea of the expected peak-to-peak amplitude of the interference, the problem can be solved by introducing hysteresis of appropriate width in the comparator characteristic. Then, if the input signal is increasing in magnitude, the comparator with hysteresis will remain in the low state until the input level exceeds the high threshold V_{D1} . Subsequently the comparator will remain in the high state even if, owing to interference, the signal decreases below V_{D1} . The comparator will switch to the low state only if the input signal is decreased below the low threshold V_{D2} . The situation is illustrated in Fig. 13.22, from which we see that including hysteresis in the comparator characteristics provides an effective means for rejecting interference (thus providing another form of filtering).

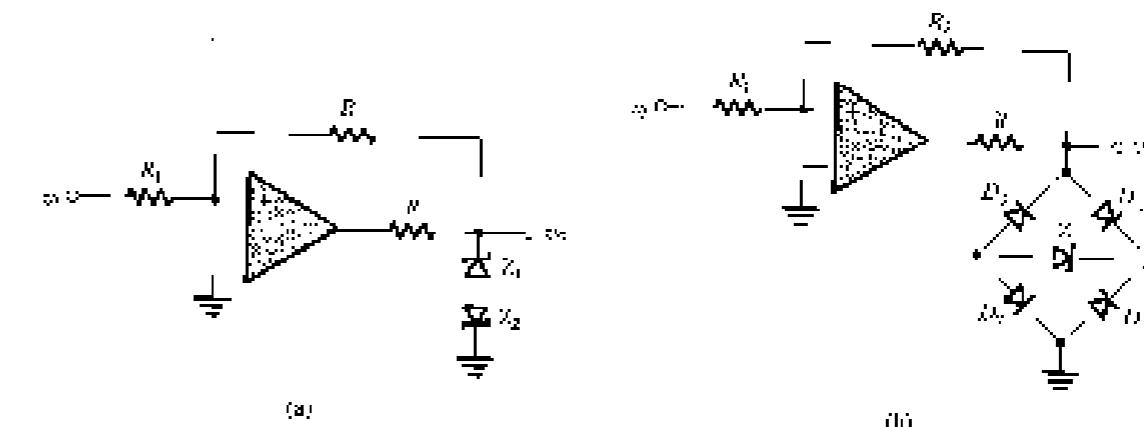


FIGURE 13.23 Higher circuits are used to obtain more positive output levels in the bistable circuit. In (a) the value of R and Z_1 be chosen to yield the current required for the proper operation of the circuit. (b) For this circuit $I_1 = V_{D1} - V_{D2}$ and $I_2 = -(V_{D2} + V_{D3})$, where V_D is the forward diode drop.

13.4.7 Making the Output Levels More Precise

The output levels of the bistable circuit can be made more precise than the saturation voltages of the op-amps by cascading the op-amp with a limiter circuit (see Section 3.6 for a discussion of limiter circuits). Two such arrangements are shown in Fig. 13.23.

EXERCISES

- (13.72) Design the circuit shown in Fig. 13.21(B) so that the output voltage after the first op-amp is a triangular waveform. This should be done by using the circuit of Fig. 13.23, first. The circuit required for this exercise is given in Fig. 13.24.
- (13.72.1) Using a single operational amplifier, design a circuit that will produce a sawtooth waveform. This may be done by using the circuit of Fig. 13.23, first.
- (13.73) Consider the bistable circuit with a trapezoidal threshold characteristic shown in Fig. 13.21(B). If the input voltage is a sinusoidal wave with a 1-V peak-to-peak amplitude, calculate the output voltage. Assume the values of V_{D1} and V_{D2} are 1.2 V and 0.8 V, respectively. The output voltage must be constant during the flat portions of the threshold characteristic.
- (13.74) Consider the circuit of Fig. 13.21(B) with a trapezoidal threshold characteristic. If the input voltage is a sinusoidal wave with a 1-V peak-to-peak amplitude, calculate the output voltage. Assume the values of V_{D1} and V_{D2} are 1.2 V and 0.8 V, respectively. The output voltage must be constant during the flat portions of the threshold characteristic.
- (13.75) Consider the circuit of Fig. 13.21(B) with a trapezoidal threshold characteristic. If the input voltage is a sinusoidal wave with a 1-V peak-to-peak amplitude, calculate the output voltage. Assume the values of V_{D1} and V_{D2} are 1.2 V and 0.8 V, respectively. The output voltage must be constant during the flat portions of the threshold characteristic.
- (13.76) Consider the circuit of Fig. 13.21(B) with a trapezoidal threshold characteristic. If the input voltage is a sinusoidal wave with a 1-V peak-to-peak amplitude, calculate the output voltage. Assume the values of V_{D1} and V_{D2} are 1.2 V and 0.8 V, respectively. The output voltage must be constant during the flat portions of the threshold characteristic.
- (13.77) Consider the circuit of Fig. 13.21(B) with a trapezoidal threshold characteristic. If the input voltage is a sinusoidal wave with a 1-V peak-to-peak amplitude, calculate the output voltage. Assume the values of V_{D1} and V_{D2} are 1.2 V and 0.8 V, respectively. The output voltage must be constant during the flat portions of the threshold characteristic.
- (13.78) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 100-mV width.
- (13.79) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 200-mV width.
- (13.80) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 300-mV width.
- (13.81) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 400-mV width.
- (13.82) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 500-mV width.
- (13.83) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 600-mV width.
- (13.84) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 700-mV width.
- (13.85) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 800-mV width.
- (13.86) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 900-mV width.
- (13.87) In the circuit of Fig. 13.21(B), if $V_{D1} = 1.2$ V and $V_{D2} = 1.02$ V, and the hysteresis is 100 mV, find the output voltage for a 1000-mV width.

13.5 GENERATION OF SQUARE AND TRIANGULAR WAVEFORMS USING ASTABLE MULTIVIBRATORS

A square waveform can be generated by arranging for a bistable multivibrator to switch states periodically. This can be done by connecting the bistable multivibrator, with an RC circuit in a feedback loop, as shown in Fig. 13.24(a). Observe that the bistable multivibrator has an inverting transfer characteristic and can thus be replaced using the circuit of Fig. 13.10(a). This results in the circuit of Fig. 13.24(b). We shall show shortly that this circuit has no stable states and thus is appropriately named an **astable multivibrator**.

13.5.1 Operation of the Astable Multivibrator

To see how the astable multivibrator operates, refer to Fig. 13.24(b) and let the output of the bistable multivibrator be at one of its two possible levels, say L_+ . Capacitor C will charge toward this level through resistor R . Thus the voltage across C , which is applied to the negative input terminal of the op amp and thus is denoted v_C , will rise exponentially toward L_+ with a time constant $\tau = CR$. Meanwhile, the voltage at the positive input terminal of the op amp is $v_{in} = \beta v_{out}$. This situation will continue until the capacitor voltage reaches the positive threshold $V_{th+} = \beta L_+$, at which point the bistable multivibrator will switch to the other stable state in which $v_{out} = L_-$ and $v_C = \beta L_-$. The capacitor will then start discharging, and its voltage, v_C , will decrease exponentially toward L_- . This new state will prevail until v_C reaches the negative threshold $V_{th-} = -\beta L_+$, at which time the bistable multivibrator switches to the positive-output state, the capacitor begins to charge, and the cycle repeats itself.

From the preceding description we see that the astable circuit oscillates and produces a square waveform at the output of the op amp. This waveform, and the waveforms at the two input terminals of the op amp, are displayed in Fig. 13.24(c). The period T of the square

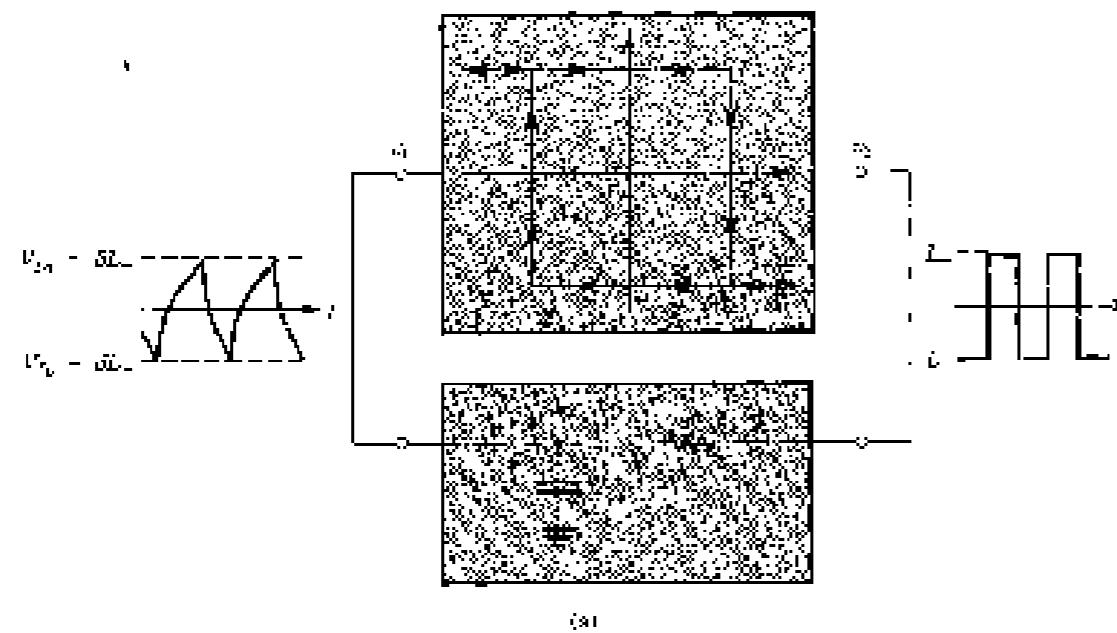


FIGURE 13.24 (a) Constructing a bistable multivibrator with inverting transfer characteristics in a feedback loop with an RC circuit results in a square wave generator.

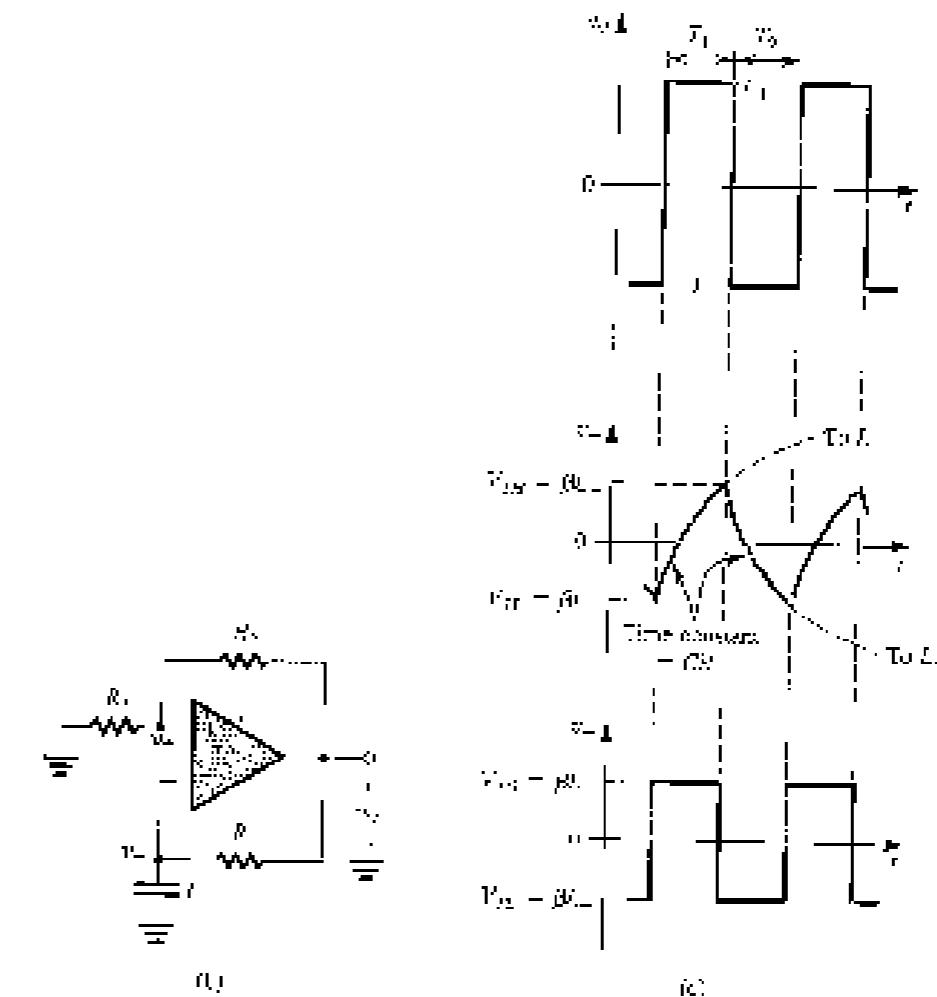


FIGURE 13.24 (b) The circuit obtained when a bistable multivibrator is built around the circuit of Fig. 13.10(a). (c) Waveforms at the various nodes of the circuit in (b). This circuit is called an **astable multivibrator**.

Waveform can be found as follows: During the charging interval T_1 , the voltage v_C across the capacitor at any time t , with $t = 0$ at the beginning of T_1 , is given by (see Appendix D)

$$v_C = L_+ - (L_+ - \beta L_-) e^{-t/\tau}$$

where $\tau = CR$. Substituting $v_C = \beta L_+$ at $t = T_1$ gives

$$T_1 = \tau \ln \frac{1 + \beta(L_+/L_-)}{1 - \beta} \quad (13.30)$$

Similarly, during the discharge interval T_2 , the voltage v_C at any time t , with $t = 0$ at the beginning of T_2 , is given by

$$v_C = L_- + (L_+ - \beta L_-) e^{t/\tau}$$

Substitution $\phi = \theta T$, $0 \leq T \leq 1$, gives

$$T_2 = \left(\ln \frac{B(T_c/T)}{S} \right)^{-1} \quad (13.3)$$

Equations (13,14) and (15,16) can be combined to obtain the period $T = T_1 + T_2$. Notably, $L = -L_1$, resulting in symmetrical square waves of period T given by:

$$f = 2\pi \ln \frac{1 + g}{1 - g} \quad (13.3)$$

Note that this single-phase generator can be made to have variable frequency by switching different capacitors C (usually in decades) and by continuously adjusting R (to obtain continuous frequency control within each decade of frequency). Also, the waveform is active, can be made almost triangular by using a small value for the parameter β . However, though the waveforms of superior linearity can be easily generated using the scheme discussed next.

Before leaving this section, however, note that although the membre circuit has no stable states, it has two quasi-stable states and contains a clock for a fixed interval determined by the time constant of the RCL network and the thresholds of the bistable n -attractor.

EXERCISES

- 13.18 The frequency of the H_2O_2 molecule is $6.3 \times 10^{13} \text{ Hz}$. At what temperature will the frequency be $1.0 \times 10^{14} \text{ Hz}$?

Ans: 294 K

13.19 Consider the modification of the circuit of Fig. 13.2(10) in which the capacitor is replaced by parallel resistors, each having a resistance of 15Ω , and $R = 20 \Omega$. Calculate the current in the parallel branch. Find an expression for the frequency in terms of the voltage V , the value of C , and the value of R . Make the following assumptions:
 i) the circuit is in series with a 100Ω resistor; and
 ii) the temperature is constant.

Ans: $I = 2V \cdot 10^{-12} + V \cdot 10^{-12} \cdot R \cdot C \cdot \ln(1 + R \cdot C \cdot 10^9)$

13.5.2 Generation of Triangular Waveform

The exponential waveforms generated at the switch circuit of Fig. 13.21 can be changed to triangular by replacing the low-pass RCL circuit with an integrator. (The integrator is, after all, a two-pole circuit with a corner frequency at $\Delta\omega$.) The integration causes linear charging and discharging of the capacitor, thus providing a triangular waveform. The resulting circuit is shown in Fig. 13.25(a). Observe that because the integrator is inverting, it is necessary to invert the characteristics of the bistable circuit. Thus the bistable circuit used here is of the non-inverting type and can be implemented using the circuit of Fig. 13.2.

We now proceed to show how the feedback loop of Fig. 13.25(a) oscillates and generates a triangular waveform v_1 at the output of the integrator and a square waveform v_2 at the output of the bistable circuit. Let the output of the bistable circuit be at I_+ . A current equal to L_+/R will flow into the resistive R and through capacitor C , causing the output of the integrator to decrease linearly with a slope of $-L_+/CR$, as shown in Fig. 13.25(c). This will continue until the integrator output reaches the lower threshold V_{D-} of the bistable circuit, at which point the bistable circuit will switch states, its output becoming negative and equal to

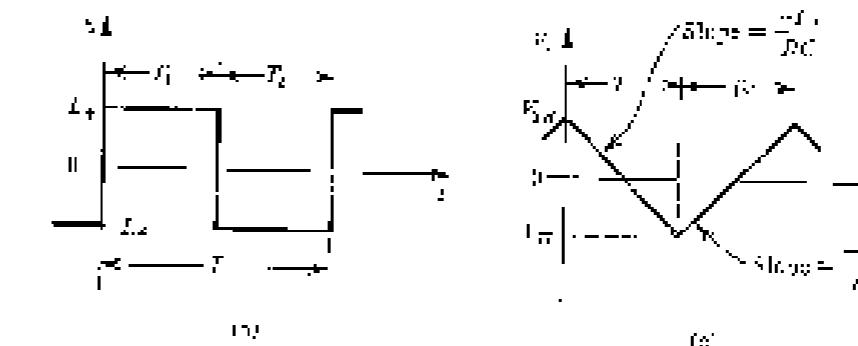
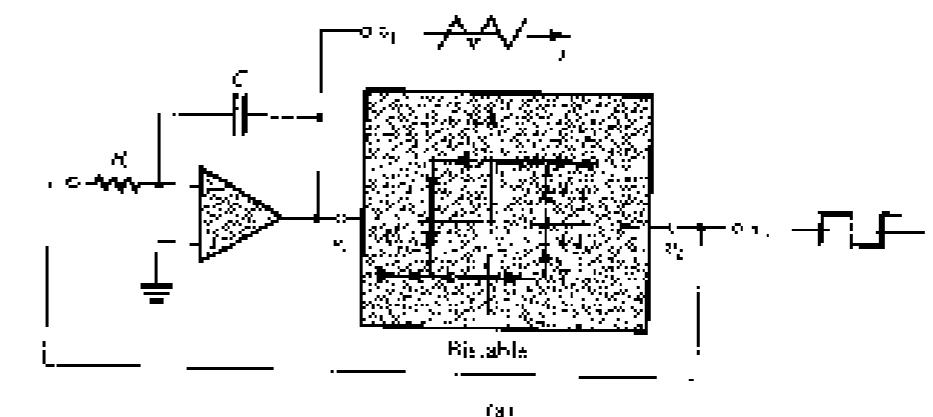


FIGURE 13.35 A central nervous system regeneration pathway involving microglia.

At this instant the current through R and C will reverse direction, and its value will become equal to $-L_1/R$. It follows that the integrator output will start to increase linearly with a positive slope equal to L_1/RC . This will continue until the integrator output voltage reaches the positive threshold of the bistable circuit, V_{TH} . At this point the bistable circuit switches, its output becomes negative (I_4). The current into the integrator reverses direction, and the output of the integrator starts to decrease linearly, decreasing again.

During the discussion above it is not very easy to derive an expression for the period T_0 , the source and triangular waveforms. During the interval T_0 we have $\theta = \omega_0 t + \phi_0$.

$$\frac{V_{\text{eff}} - V_0}{T_0} = \frac{\mu}{C}$$

first which we saw

$$T_1 = CR \frac{|\beta_H - \beta_W|}{\beta} \quad (13)$$

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$$\frac{V_{2B} - V_{2r}}{V_2} = \frac{-2}{1}$$

from which we obtain

$$T_1 = \frac{1}{f_R} \frac{V_{DD} - V_{TH}}{+L_1} \quad (13.35)$$

Thus to obtain symmetrical square waves we design the bistable circuit to have $L_1 = -L_2$.

EXERCISE

(13.18) Consider the circuit of Fig. 13.21(b). If the output voltage is to be a square wave with a period of $T = 10\text{ ms}$, determine the values of R_1 and C_1 . Assume $V_{DD} = 10\text{ V}$, $V_{TH} = 0.5\text{ V}$, and $f_R = 100\text{ Hz}$. (Ans.: $R_1 = 100\text{ k}\Omega$, $C_1 = 10\text{ nF}$)

13.6 GENERATION OF A STANDARDIZED PULSE—THE MONOSTABLE MULTIVIBRATOR

In some applications the need arises for a pulse of known height and width generated in response to a trigger signal. Because the width of the pulse is predictable, its trailing edge can be used for timing purposes—that is, to initiate a particular task at a specified time. Such a standardized pulse can be generated by the DTL type of multivibrator, the monostable multivibrator.

The monostable multivibrator has one stable state in which it can remain indefinitely. It also has a quasi-stable state to which it can be triggered and in which it stays for a predetermined interval equal to the desired width of the output pulse. When this interval expires, the monostable multivibrator returns to its stable state and remains there, awaiting another triggering signal. The action of the monostable multivibrator has given rise to its alternative name, the one shot.

Figure 13.26(a) shows an op-amp monostable circuit. We observe that this circuit is an untriggered form of the astable circuit of Fig. 13.21(b). Specifically, a clamping diode D_1 is added across the capacitor C_1 , and a trigger circuit composed of capacitor C_2 , resistor R_1 , and diode D_2 is connected to the noninverting input terminal of the op-amp. The circuit operates as follows: In the static state, which prevails in the absence of the triggering signal, the output of the op-amp is at L_1 and diode D_1 is conducting through R_1 , and thus clamping the voltage v_2 to one diode drop above ground. We select R_1 much larger than R_2 , so that diode D_2 will be conducting a very small current and the voltage v_1 will be very closely determined by the voltage divider R_1/R_2 . Thus $v_1 = \beta L_1$, where $\beta = R_2/(R_1 + R_2)$. The stable state is maintained because βL_1 is greater than V_{DD} .

Now consider the application of a negative going step; the trigger condition refers to the signal waveforms shown in Fig. 13.26(b). The negative triggering edge will be coupled to the cathode of diode D_2 via capacitor C_2 , and thus D_2 conducts heavily and pulls node C down. If the trigger signal is of sufficient height to cause v_1 to go below v_{DD} , the op-amp will see a net negative input voltage and its output will switch to L_2 . This in turn will cause v_2 to go negative to βL_2 , keeping the op-amp in its heavily saturated state. Note that D_1 will then cut off, thus isolating the circuit from any further changes at the trigger input terminal.

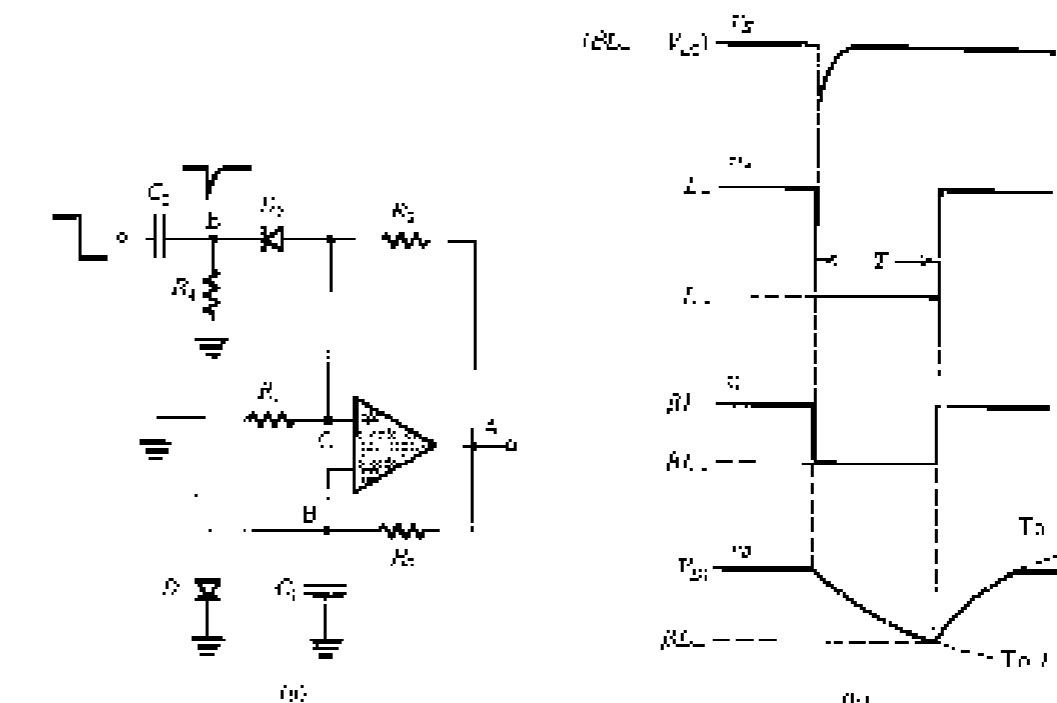


FIGURE 13.26 (a) An op-amp monostable circuit. (b) Signal waveforms in the circuit of (a).

The negative voltage at A causes D_2 to cut off, and C_2 begins to discharge exponentially toward L_2 with a time constant $C_2 R_1$. The monostable multivibrator is now in its quasi-stable state, which will prevail until the declining v_2 goes below the voltage v_1 , node C, which is βL_1 . At this instant the op-amp's output switches back to L_1 , and the voltage at node C goes back to βL_1 . Capacitor C_1 then charges toward L_1 until diode D_1 turns on and the circuit returns to its stable state.

From Fig. 13.26(b), we observe that a negative pulse is generated at the output during the quasi-stable state. The duration T of the negative pulse is determined from the exponential waveform of v_2 ,

$$v_2(t) = L_2 - (L_2 - V_{DD})e^{-t/C_2 R_1}$$

By substitution in $v_2(T) = \beta L_1$,

$$\beta L_1 = L_2 - (L_2 - V_{DD})e^{-T/C_2 R_1}$$

which yields

$$T = C_2 R_1 \ln \left(\frac{V_{DD} - L_1}{\beta L_1 - L_2} \right) \quad (13.36)$$

For $L_1 \ll |L_2|$, this equation can be approximated by

$$T \approx C_2 R_1 \ln \left(\frac{1}{1 - \beta} \right) \quad (13.37)$$

Finally, note that the monostable circuit should not be triggered again until capacitor C has been recharged to V_{DD} ; otherwise the resulting output pulse will be shorter than normal. This recharging time is known as the recovery period. Circuit techniques exist for shortening the recovery period.

EXERCISE

For the monostable circuit of Fig. 13.26, if the voltage at Comp_1 is 0.5 V, determine the time constant $T = RC$ if $R = 12.8 \text{ k}\Omega$ and $C = 10 \text{ nF}$. Assume $V_{DD} = 12 \text{ V}$.

13.7 INTEGRATED-CIRCUIT TIMERS

Commercially available integrated-circuit packages exist that contain the bulk of the circuitry needed to implement monostable and astable multivibrators with precise characteristics. In this section we discuss the most popular of such ICs, the 555 timer. Introduced in 1971 by the Signetics Corporation as a bipolar integrated circuit, the 555 is also available in CMOS technology and in a number of packages.

13.7.1 The 555 Circuit

Figure 13.27 shows a block-diagram representation of the 555 internal circuit (or the actual circuit, refer to Gummel [1984]). The circuit consists of two comparators, an SR flip-flop, and a transistor Q_1 that operates as a switch. One power supply (V_{DD}) is required for operation, with its supply voltage typically 5 V. A resistive voltage divider, consisting of the three equal-valued resistors labeled R_1 , is connected across V_{DD} and establishes the reference (threshold) voltage for the two comparators. These are $V_{TH1} = \frac{1}{3}V_{DD}$ for comparator 1 and $V_{TH2} = \frac{2}{3}V_{DD}$ for comparator 2.

We studied SR flip-flops in Chapter 11. For our purposes here we note that an SR flip-flop has either a latched or set/reset state, having complementary outputs, denoted \bar{Q} and Q . In the set state, the output at \bar{Q} is "high" (approximately equal to V_{DD}) and that at Q is "low" (approximately equal to 0 V). In the other state, termed the reset state, the output at Q is low and that at \bar{Q} is high. The flip-flop is set by applying a high level (V_{DD}) to its set input terminal, labeled S . To reset the flip-flop, a high level is applied to the reset input terminal, labeled R . Note that the reset and set input terminals of the flip-flop in the 555 circuit are connected to the outputs of comparator 1 and comparator 2, respectively.

The positive input terminal of comparator 1 is brought out to an external terminal of the 555 package, labeled Threshold. Similarly, the negative-input terminal of comparator 2 is connected to an external terminal labeled Trigger, and the collector of transistor Q_1 is connected to a terminal labeled Discharge. Finally, the Q output of the flip-flop is connected to the output terminal of the chip package, labeled Out.

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The positive input terminal of comparator 1 is brought out to an external terminal of the 555 package, labeled Threshold. Similarly, the negative-input terminal of comparator 2 is connected to an external terminal labeled Trigger, and the collector of transistor Q_1 is connected to a terminal labeled Discharge. Finally, the Q output of the flip-flop is connected to the output terminal of the chip package, labeled Out.

13.7.2 Implementing a Monostable Multivibrator Using the 555 IC

Figure 13.28(a) shows a monostable multivibrator implemented using the 555 IC together with an external resistor R and an external capacitor C . In the stable state the flip-flop will be in the reset state, and thus the \bar{Q} output will be high, turning on transistor Q_1 . Transistor Q_1 will be saturated, and thus v_1 will be close to 0 V, resulting in a low level at the output of comparator 1. The voltage at the trigger input terminal, labeled v_T , must be kept high (greater than V_{TH2}), and thus the output of comparator 2 also will be low. Finally, note that since the flip-flop is in the reset state, Q will be low and thus v_2 will be close to 0 V.

To trigger the monostable multivibrator, a negative-going pulse is applied to the trigger input terminal. As v_T goes below V_{TH2} , the output of comparator 2 goes to the high level, thus setting the flip-flop. Output Q of the flip-flop goes high, and thus v_2 goes high, and output \bar{Q} goes low, turning off transistor Q_1 . Capacitor C now begins to charge up through resistor R , and its voltage v_1 rises exponentially toward V_{DD} as shown in Fig. 13.28(b). The monostable multivibrator is now in its quasi-stable state. This state continues until v_1 reaches a value that exceeds the threshold of comparator 1, at which time the output of comparator 1 goes high, resetting the flip-flop. Output Q of the flip-flop now goes high and turns on transistor Q_1 , in turn, transistor Q_1 rapidly discharges capacitor C , causing v_1 to go to 0 V. At 0 V, when the flip-flop is reset, its Q output goes low, and thus v_2 goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.

From the description above we see that the monostable multivibrator produces an output pulse v_1 as indicated in Fig. 13.28(c). The width of the pulse, T , is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 13.28(b) as follows. Denoting the instant at which the trigger pulse is applied as $t = 0$, the exponential waveform of v_1 can be expressed as

$$v_1 = V_{DD}(1 - e^{-t/T}) \quad (13.58)$$

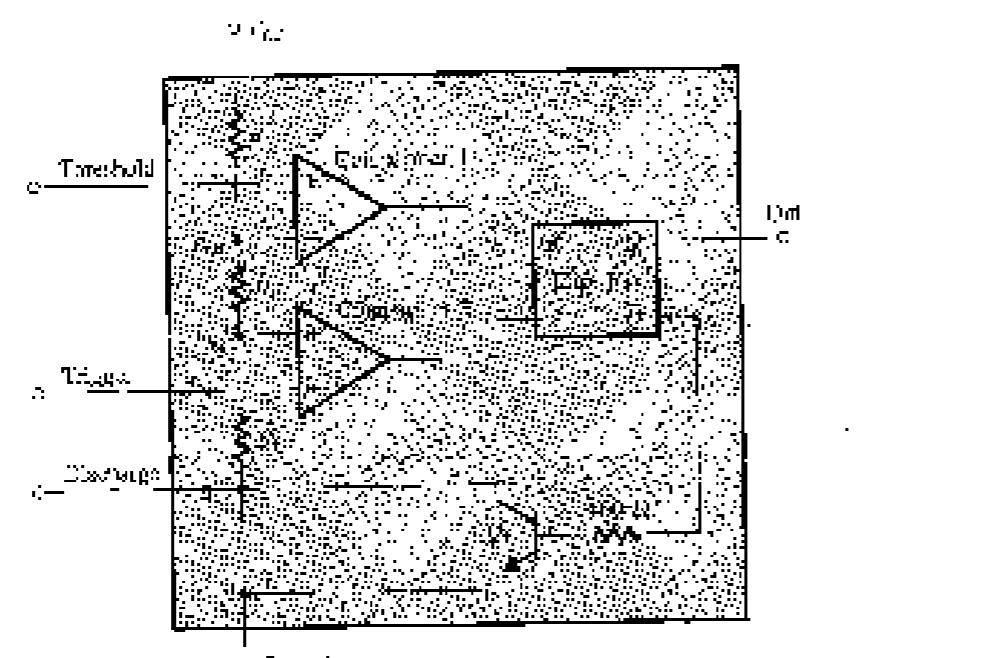


FIGURE 13.27 A block diagram representation of the internal circuit of the 555 integrated circuit.

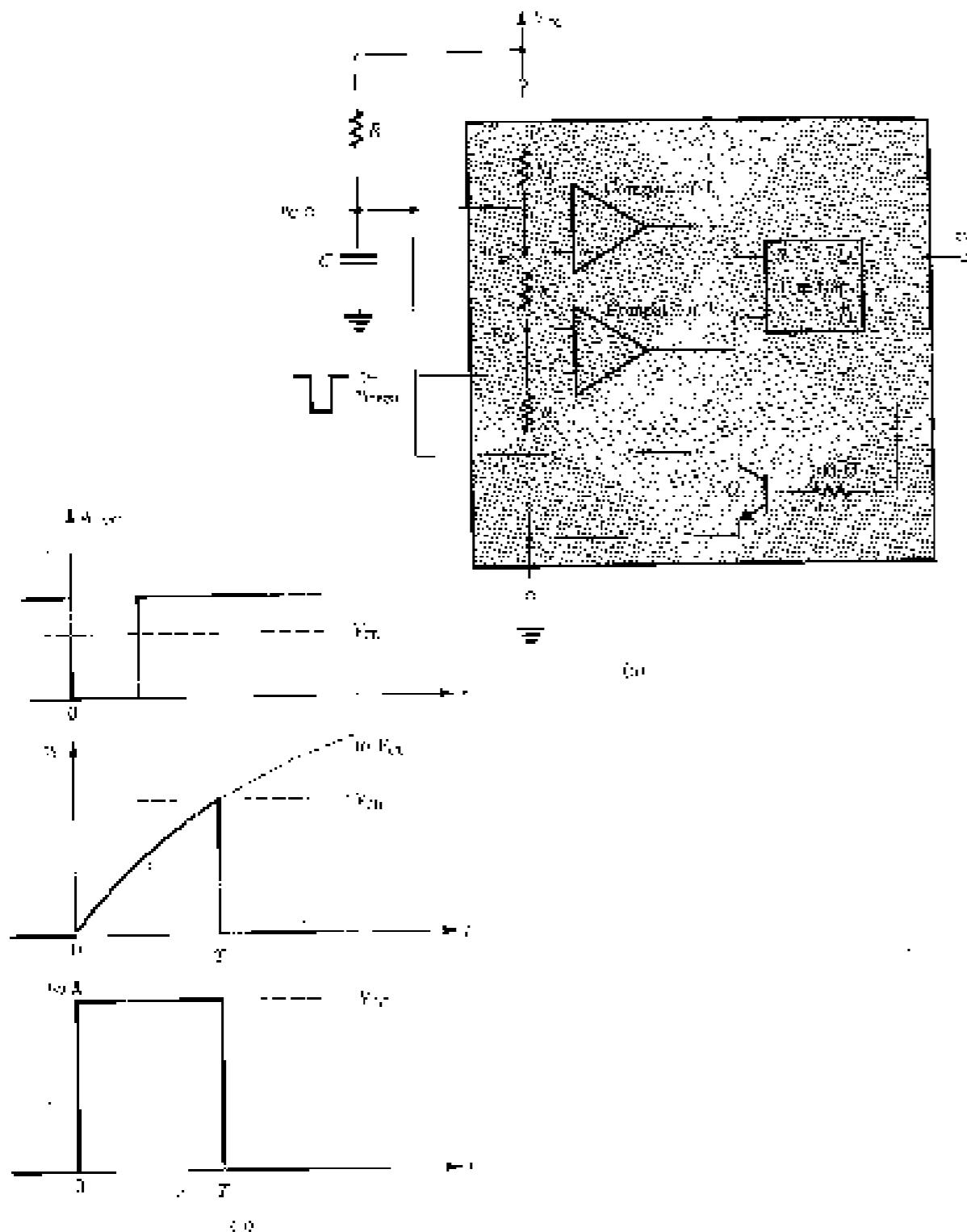


FIGURE 13.28 (a) The 555 IC connected as a current-controlled multivibrator. (b) Waveforms of the circuit in (a).

Substituting $v_C = V_{DD} - \frac{1}{2}V_{DD}$ in Eq. (13.38) gives

$$T_1 = CR \ln 2 = 1.1CR \quad (13.39)$$

Thus the pulse width is determined by the external components C and R , which can be selected to have values as precise as desired.

13.7.3 An Astable Multivibrator Using the 555 IC

Figure 13.29(a) shows the circuit of an astable multivibrator employing a 555 IC, two external resistors, R_A and R_B , and an external capacitor C . To see how the circuit operates, refer to the waveforms depicted in Fig. 13.29(b). Assume that initially Q_1 is discharged and the flip-flop is set. Thus v_Q is high and Q_1 is off. Capacitor C will charge up through the series combination of R_A and R_B , and the voltage across it, v_C , will rise exponentially toward V_{DD} . As v_C crosses the level equal to $V_{DD}/2$, the output of comparator 2 goes low. This, however, has no effect on the circuit operation, and the flip-flop remains set. Instead, this state continues until v_C reaches and begins to exceed the threshold of comparator 1, $V_{DD}/3$. At this instant of time, the output of comparator 1 goes high and resets the flip-flop. Thus v_Q goes low, \bar{Q} goes high, and transistor Q_1 is turned on. The saturated transistor Q_1 causes a voltage of approximately zero volts to appear at the common node of R_A and R_B . Thus C begins to discharge through R_A and the collector of Q_1 . The voltage v_C decreases exponentially with a time constant $C(R_A + R_B)$ toward 0 V. When v_C reaches the threshold of comparator 2, $V_{DD}/3$, the output of comparator 2 goes high and sets the flip-flop. The output v_Q then goes high, and Q_1 goes low, turning off Q_1 . Capacitor C begins to charge through the series equivalent of R_A and R_B , and its voltage rises exponentially toward V_{DD} , with a time constant $C(R_A + R_B)$. This continues until v_C reaches $V_{DD}/2$, at which time the output of comparator 1 goes high, resetting the flip-flop, and the cycle continues.

From the description above we see that the circuit of Fig. 13.29(a) oscillates and produces a square waveform at the output. The frequency of oscillation can be determined as follows. Reference to Fig. 13.29(b) indicates that the output will be high during the interval T_1 , in which v_C rises from $V_{DD}/3$ to $V_{DD}/2$. The exponential rise of v_C can be described by

$$v_C = V_{DD} - (V_{DD} - V_{DD})e^{-t/C(R_A + R_B)} \quad (13.40)$$

where $t = 0$ is the instant at which the interval T_1 begins. Substituting $v_C = V_{DD}/2$ at $t = T_1$ and $V_{DD} = \frac{1}{3}V_{DD}$ results in

$$T_1 = C(R_A + R_B) \ln 2 \approx 0.69 C(R_A + R_B) \quad (13.41)$$

We also note from Fig. 13.29(b) that v_C will be low during the interval T_2 , in which v_C falls from $V_{DD}/2$ to $V_{DD}/3$. The exponential fall of v_C can be described by

$$v_C = V_{DD} e^{-t/C(R_A + R_B)} \quad (13.42)$$

where we have taken $t = 0$ as the beginning of the interval T_2 . Substituting $v_C = V_{DD}/3$ at $t = T_2$ and $V_{DD} = \frac{1}{3}V_{DD}$ results in

$$T_2 = CR_A \ln 2 \approx 0.69 CR_A \quad (13.43)$$

Equations (13.41) and (13.43) can be combined to obtain the period T of the output square wave:

$$T = T_1 + T_2 = 0.69 C(R_A + 2R_B) \quad (13.44)$$

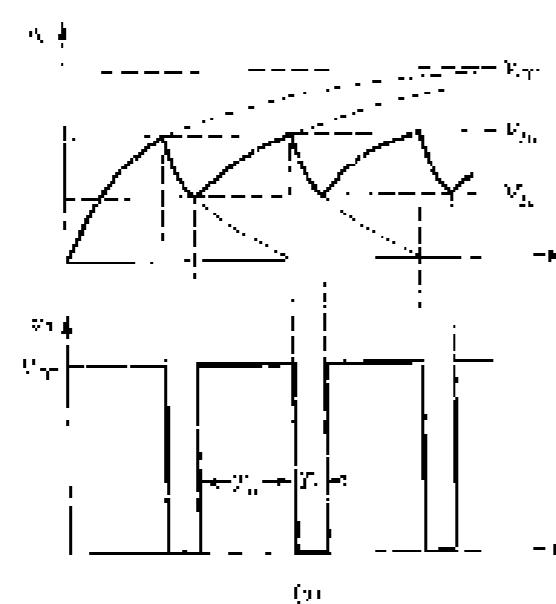
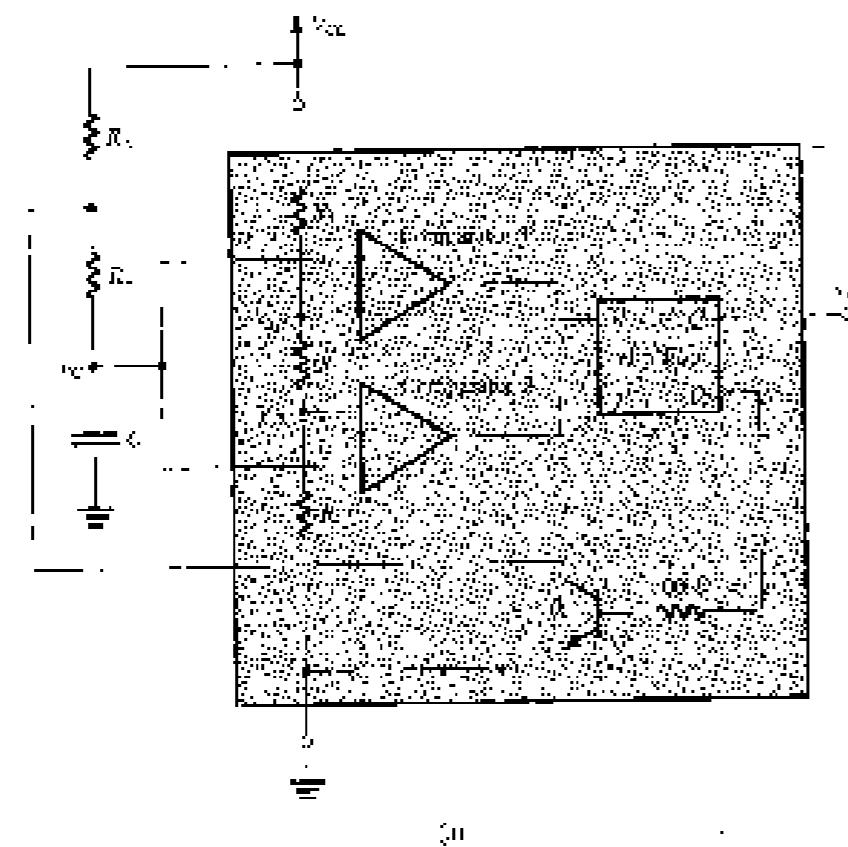


FIGURE 13.28 (a) Two triodes connected to implement an enable waveform shaper. (b) Waveforms at the circuit terminals.

Also, the duty cycle of the output square wave can be found from Eqs. (13.7) and (13.43).

$$\text{Duty cycle} = \frac{T_2}{T_1 + T_2} = \frac{R_1 + R_2}{R_1 + 2R_2} \quad (13.45)$$

Note that the duty cycle will always be greater than 0.5 (50%); if R_2 approaches 0.5, R_1 is selected to be much smaller than R_2 (unfortunately, at the expense of supply current).

EXERCISES

- 13.20 Using a 100-V supply, calculate the value of R_2 that yields an output voltage of 100 V in the circuit of Fig. 13.28(a). *(Ans. 100 kΩ)*
- 13.21 If $R_1 = 100\ \Omega$, $R_2 = 200\ \Omega$, and $C = 1\ \mu F$, calculate the period of oscillation. *(Ans. 1.41 ms)*

13.9 NONLINEAR WAVEFORM-SHAPING CIRCUITS

Diodes or transistors can be combined with resistors to synthesize two-port networks having arbitrary nonlinear transfer characteristics. Such two-port networks can be employed in waveform shaping—that is, changing the waveform of an input signal in a prescribed manner to produce a waveform of a desired shape at the output. In this section we illustrate this application by a concrete example, the sine-wave shaper. This is a circuit whose purpose is to change the waveform of an input triangular-wave signal to a sine wave. Though simple, the sine-wave shaper is a practical building block used extensively in function generators. This method of generating sine waves will be contrasted to that using linear oscillators (Sections 13.1–13.3). All-four linear oscillators produce sine waves of high purity; they are most convenient at very low frequencies. Also, linear oscillators are in general more difficult to tune over wide frequency ranges. In the following we discuss two distinctly different techniques for designing sine-wave shapers.

13.9.1 The Breakpoint Method

In the breakpoint method the desired nonlinear transfer characteristic (for our case the sine function shown in Fig. 13.30) is implemented as a piecewise linear curve. Diodes are utilized as switches that turn on at the various breakpoints of the transfer characteristic; thus switching into the circuit a diode or resistor that cause the transfer characteristic to change slope.

Consider the circuit shown in Fig. 13.31(a). It consists of a chain of resistors connected across the entire symmetrical voltage supply V_1 – V_2 . The purpose of this voltage divider is to generate reference voltages that will serve to determine the breakpoints in the transfer characteristic. In our example three reference voltages are defined: $V_3 = V_1 - V_2$, $-V_2$, $-V_1$. Note that the entire circuit is symmetrical, driven by a symmetrical triangular-wave input. The circuit approximates each quarter-cycle of the sine wave by three straight-line segments; the breakpoints between these segments are determined by the reference voltages V_3 and $-V_2$.

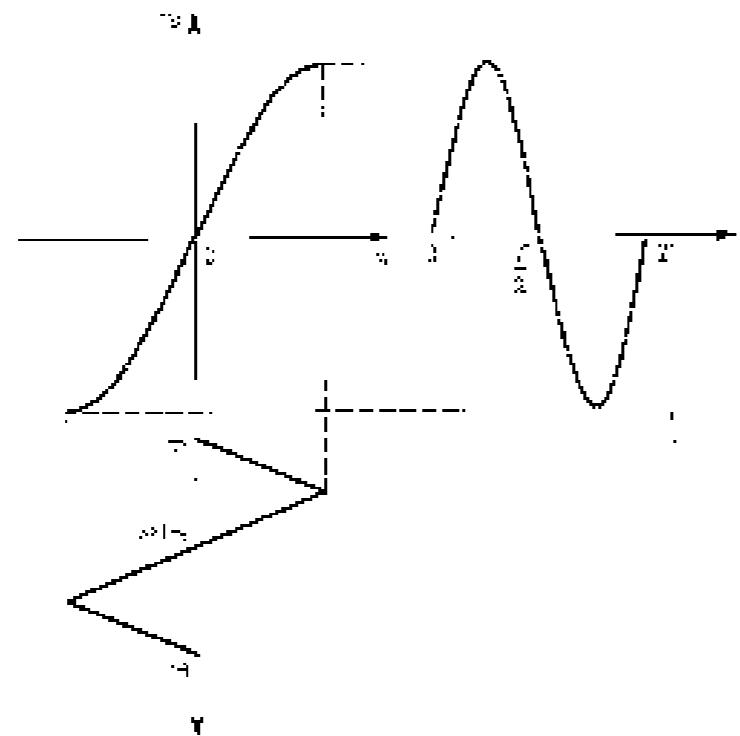


FIGURE 13.30 Using a nonlinear (exponential) transfer characteristic to shape a triangular wave. In (a), the input is inverted.

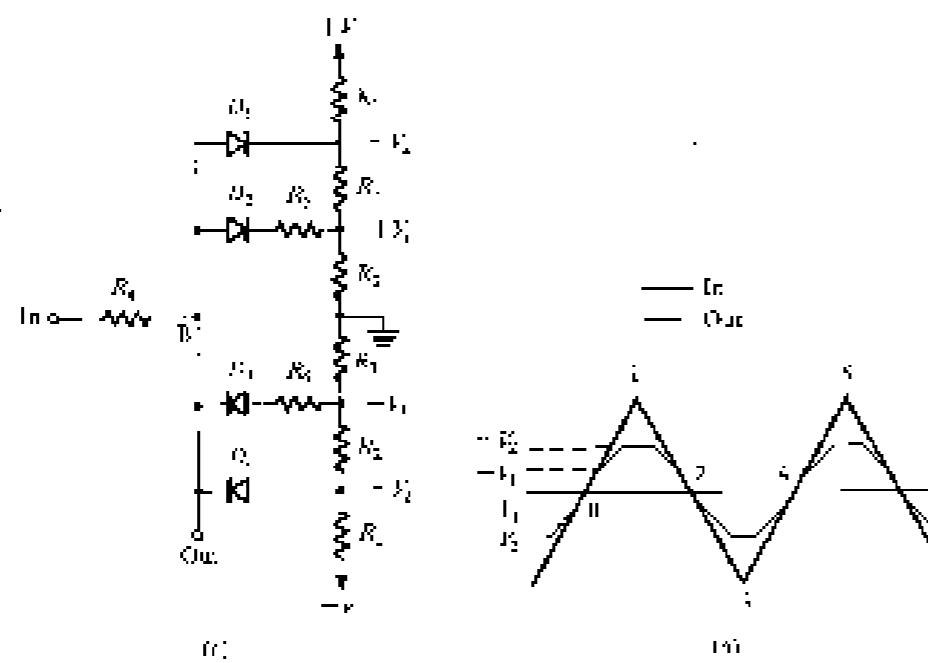


FIGURE 13.31 (a) A three-point sine-wave shaper. (b) The input triangular waveform and the output sinusoidally modulated waveform.

The circuit works as follows: Let the input be the triangular wave shown in Fig. 13.31(a), and consider first the quiescent state defined by the two points labeled 0 and 1. When the input signal is less in magnitude than V_1 , point 0 of the diodes conducts. Thus zero current flows through R_2 and the output voltage v_o is zero, equal to the input voltage. But as the input rises to V_1 and inverse D_2 (assumed ideal) begins to conduct, assuming that the conducting D_2 behaves as a short circuit, we see that, for $v_o > V_1$,

$$v_o = V_1 + (v_o - V_1) \frac{R_2}{R_2 + R_1}$$

This implies that as the input continues to rise above V_1 , the output follows but with a reduced slope. This gives rise to the second segment in the output waveform, as shown in Fig. 13.31(b). Note that in developing the equation above we have assumed that the resistances in the voltage dividers are *large* enough in value to cause the voltages V_1 and V_2 to be constant independent of the current coming from the input.

Next consider what happens as the voltage at point 1 reaches the second breakpoint determined by V_2 . At this point, D_1 conducts, thus limiting the output v_o to V_2 (unless, of course, the voltage drop across D_1 is not assumed to be ideal). This gives rise to the third segment, which is flat, in the output waveform. The overall result is to "bend" the waveform and shape it into an approximation of the first quarter-cycle of a sine wave. Then, beyond the peak of the input triangular wave, as the input voltage decreases, the process unfolds, the output becoming progressively more like the input. Finally, when the input goes sufficiently negative, the process begins to repeat at $-V_1$ and $-V_2$ for the negative half-cycle.

Although the circuit is relatively simple, its performance is surprisingly good. A measure of goodness usually taken is to quantify the purity of the output sine wave by specifying the percentage total harmonic distortion (THD). This is the percentage ratio of the rms voltage of all harmonic components above the fundamental frequency (which is the frequency of the triangular wave) to the rms voltage of the fundamental (see also Chapter 11). Interestingly, one reason for the good performance of the diode shaper is the beneficial effects produced by the nonideal, *i-e*, characteristics of the diodes—that is, the exponential knee of the junction diode as it goes into forward conduction. The consequence is a relatively smooth transition from one line segment to the next.

Practical implementations of the breakpoint sine-wave shaper employ six to eight segments (truncated with the three used in the example above). Also, transistors are readily employed to provide more versatility in the circuit, with the goal being increased precision and lower THD. [See Gribenc (1984), pages 590–595.]

13.8.2 The Nonlinear-Amplification Method

The other method we discuss for the conversion of a triangular wave into a sine wave is based on feeding the triangular wave to the input of an amplifier having a nonlinear transfer characteristic that approximates the sine function. One such amplifier circuit consists of a differential pair with a resistance connected between the two emitters, as shown in Fig. 13.32. With appropriate choice of the values of the bias current I and the resistance R , the differential amplifier can be made to have a transfer characteristic closely approximating that shown in Fig. 13.33. Observe that the small-signal transfer characteristic of the circuit of Fig. 13.32 is almost linear, as a sine wave signal is near its zero crossings. At large values of v_i , the nonlinear characteristics of the BJTs reduce the gain of the amplifier and cause the transfer characteristic to bend, approximating the sine wave as it approaches its peak. [More details on this circuit can be found in Gribenc (1984), pages 595–597.]

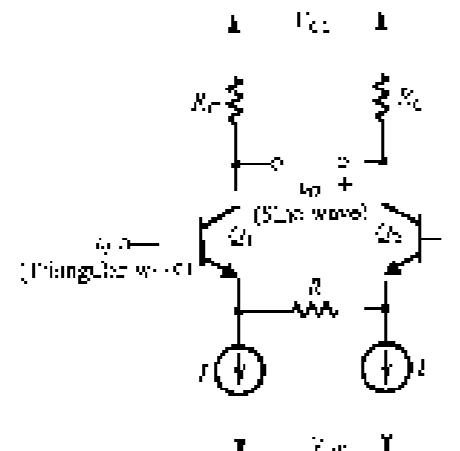
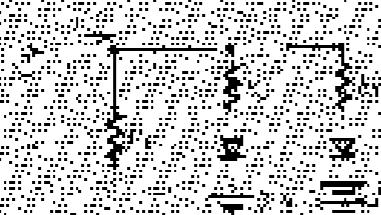


FIGURE 13.32 A differential pair with an interconnection resistance used to implement a triangular wave to a current-steering register. Operation of the circuit can be explained as described in Fig. 13.10.

EXERCISES

- 11&12 The next day, at 12:30 pm, we got our first glimpse of the Great Barrier Reef. It was a bit of a let down, as the reef was very far away from the boat.



卷之三

19. *Leucosia* *leucostoma* *leucostoma* *leucostoma* *leucostoma*

الآن، يُمكننا إثبات أن $\mathcal{L}(G)$ هو مولود من G .
نحو ذلك، نحن نعلم أن G هو مولود من $\mathcal{L}(G)$.
لذلك، $G \cong \mathcal{L}(\mathcal{L}(G))$.
لذلك، $\mathcal{L}(G) \cong \mathcal{L}(\mathcal{L}(G))$.
لذلك، $\mathcal{L}(G)$ هو مولود من G .

13.9 PRECISION RECTIFIER CIRCUITS

Rectifier circuits were studied in Chapter 4, where the emphasis was on their application in power-supply design. In such applications the voltages being rectified are usually no greater than the diode voltage drop, rendering the exact value of the diode drop unimportant in the proper operation of the rectifier. Other applications exist, however, where this is

In the case of instrumentation applications, the signal to be received can be of a very small amplitude, say 0.1 V, making it impossible to employ the conventional rectifier circuits. Also, in instrumentation applications, the need arises for rectifier circuits with very precise transfer characteristics.

In this section we study circuits that combine diodes and op amps to implement a variety of rectifier circuits with precise characteristics. Precision rectifiers, which can be considered a special class of wave-shaping circuits, find application in the design of instrumentation systems. An introduction to precision rectifiers was presented in Chapter 3. This material, however, is repeated here for the reader's convenience.

13.9.1 Precision Half-Wave Rectifier-The "Superdiode"

Figure 19.33(a) shows a precision half-wave-rectifier circuit consisting of a diode placed in the negative-feedback path of an op amp, with R_f being the rectifier load resistance. The circuit works as follows: If v_1 gets positive, the output voltage v_o of the op amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op amp's output terminal and the negative input terminal. This negative feedback path will cause a virtual short circuit to appear between the two input terminals of the op amp. Thus the voltage at the negative input terminal, which is also the output voltage v_o , will remain (try with a few test inputs) at the positive input terminal, which is the input voltage v_1 .

$$z_0 = z_0 - \alpha_0/2$$

Note that the offset voltage (± 0.5 V) exhibited at the sample half-wave rectifier circuit is no longer present. For the op-amp circuit to start operation, v_{in} has to exceed only a negligibly small voltage equal to the diode drop divided by the op-amp's open-loop gain. In other words, the straight line transfer characteristic $v_{\text{out}} = v_{\text{in}}$ almost passes through the origin. This makes this circuit suitable for applications involving very small v_{in} gains.

Consider now the case when v_2 goes negative. The op-amp's output voltage v_3 will tend to fall and go negative. This will reverse-bias the diode, and no current will flow through resistance R_1 , causing v_3 to remain equal to 0 V. Thus for $v_2 < 0$, $v_3 = 0$. Since in this case the diode is off, the op-amp will be operating in an open-loop fashion and its output will be at the negative saturation level.

The transfer characteristic of the circuit will be that shown in Fig. 13.3.9(e), which is almost identical to the ideal characteristic of a half-wave rectifier. The nonidealities

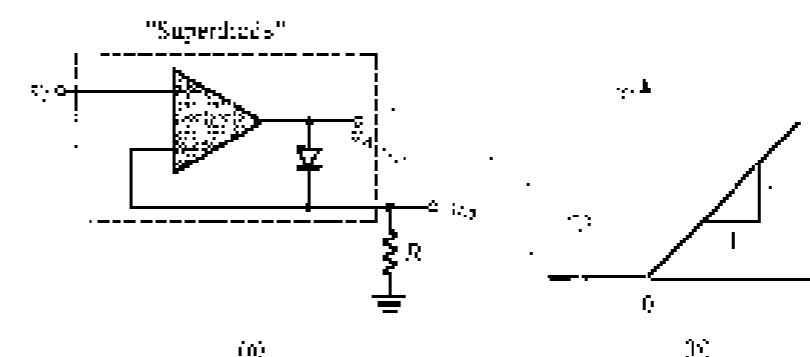


FIGURE 13.33 (a) The “magnoreson” precision Hall probe is electrically cool. (b) In almost ideal magnetic insulation, note at what $\psi = 0$ and the divide conductors, the pump supplies the load current, and the voltage conversion by b_1 is exact, an absolute advantage.

diode series have been almost completely masked by placing the diode in the negative-feedback path of an op amp. This is another dramatic application of negative feedback. The combination of diode and op amp, shown in the dashed box in Fig. 13.33(a), is appropriately referred to as a "superdiode."

As usual, though, not all is well. The circuit of Fig. 13.33 has some disadvantages. When v_2 goes negative and $v_3 = 0$, the output magnitude of v_1 appears between the two input terminals of the op amp. If this magnitude is greater than few volts, the op amp may be damaged unless it is equipped with what is called "overvoltage protection" (a feature that most modern IC op amps have). Another disadvantage is that when v_2 is negative, the op amp will be saturated. Although not intended to do so, op amp saturation should usually be avoided, since getting the op amp out of the saturation region and back into its linear region of operation requires some time. This time delay will obviously slow down circuit operation and limit the frequency of operation of the superdiode half-wave rectifier circuit.

13.9.2 An Alternative Circuit

An alternative precision rectifier circuit that does not suffer from the disadvantages mentioned above is shown in Fig. 13.34. The circuit operates in the following manner. For positive v_2 , diode D_2 conducts and closes the negative-feedback loop around the op amp. A virtual ground therefore will appear at the inverting input terminal, and the op amp's output will be clamped to one diode drop below ground. This negative voltage will keep diode D_1 off, and no current will flow in the feedback resistance R_2 . It follows that the rectifier output voltage will be zero.

As v_2 goes negative, the voltage at the inverting input terminal will tend to go negative, causing the voltage at the op amp's output terminal to go positive. This will cause D_2 to be reverse biased and hence cut off. Diode D_1 , however, will conduct through R_2 , thus establishing a negative-feedback path around the op amp and leaving a virtual ground to appear at the inverting input terminal. The current through the feedback resistance R_2 will be equal to the current through the input resistance R_1 . Thus for $R_1 = R_2$ the output voltage v_1 will be

$$v_1 = -v_2 \quad v_2 \leq 0$$

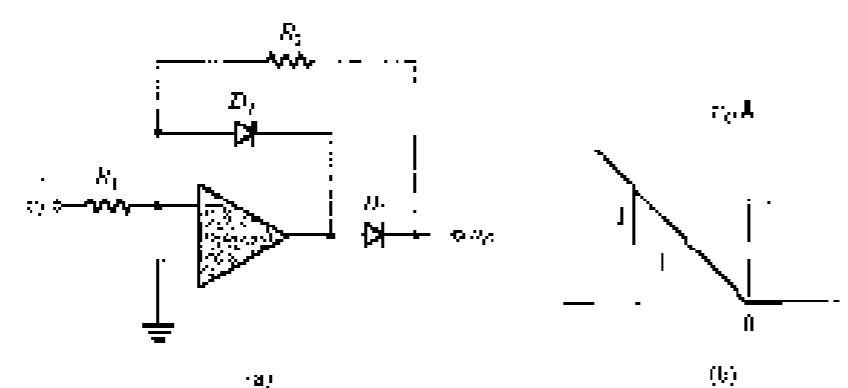


FIGURE 13.34 (a) Improved version of the precision half-wave rectifier. Diode D_2 is included to keep the feedback loop closed around the op amp during the turn-on of the rectifier diode, D_1 , thus preventing the op amp from saturating. (b) The transfer characteristic, i.e., v_1 vs v_2 .

The transfer characteristic of the circuit is shown in Fig. 13.34(b). Note that unlike the situation for the circuit shown in Fig. 13.33, here the slope of the characteristic can be set to any desired value, including unity, by selecting appropriate values for R_1 and R_2 .

As mentioned before, the major advantage of the improved half-wave-rectifier circuit is that the feedback loop around the op-amp terminals closes at all times. Hence the op-amp "turns on" in its linear operating region, avoiding the possibility of saturation and the associated time delay required to "get out" of saturation. Diode D_2 "catches" the op-amp output voltage if it goes negative and clamps it to one diode drop below ground; hence D_2 is called a "clamping diode."

13.9.3 An Application: Measuring AC Voltages

As one of the many possible applications of the precision rectifier circuits discussed in this section, consider the basic ac voltmeter circuit shown in Fig. 13.35. The circuit consists of a half-wave rectifier—formed by op amp A_1 , diodes D_1 and D_2 , and resistors R_1 and R_2 —and a first-order low-pass filter—formed by op amp A_2 , resistors R_3 and R_4 , and capacitor C . For an input sinusoid having a peak amplitude V_p , the output v_1 of the rectifier will consist of a half-sine wave having a peak amplitude of $V_p R_2 / R_1$. It can be shown using Fourier series analysis that the waveform of v_1 has an average value of $(V_p / \pi) R_2 / R_1$. In addition to harmonics of the frequency ω of the input signal, to reduce the amplitudes of all three harmonics to negligible levels, the corner frequency of the low-pass filter should be chosen such that it is lower than the lowest expected frequency ω_{\min} of the input sine wave. This leads to

$$\frac{1}{C R_2} < \omega_{\min}$$

Hence the output voltage v_2 will be mostly dc, with a value

$$V_r = -\frac{V_p R_2 R_4}{\pi R_1 R_3}$$

where R_2/R_1 is the dc gain of the low-pass filter. Note that this voltmeter essentially measures the average value of the negative parts of the input signal but can be calibrated to provide true readings for input v_1 waveforms.

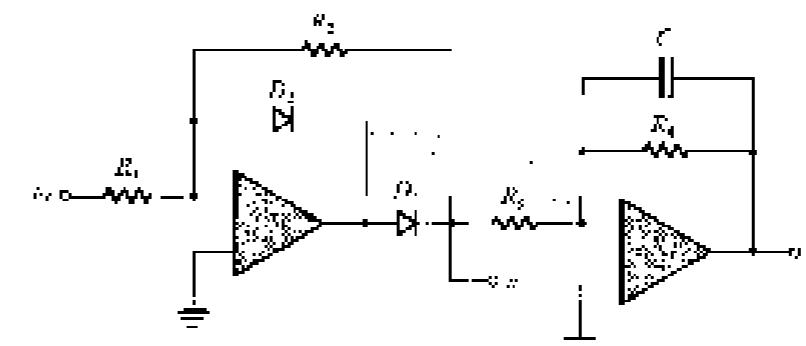


FIGURE 13.35 A simple ac voltmeter, consisting of a precision half-wave rectifier followed by a first-order low-pass filter.

EXERCISES

13.24 Consider the equations for the super-Gaussian of Fig. 13.23(a), with $A = 10 \text{ mV}$, $V_0 = 2 \text{ V}$, and $R_1 = R_2 = 1 \text{ k}\Omega$. At the output terminals at the top of the circuit, assume that the input voltage is 0.1 mV and that the output voltage is -0.2 V . The outputs A and B are fed into a full-wave rectifier with a load resistor $R_L = 1 \text{ k}\Omega$. Determine the output voltage.

Ans.: 0.1 mV, -0.2 V

13.25 Define the concept of a half-wave rectifier. State its transfer characteristic and draw its graph.

Ans.: A half-wave rectifier is a circuit that converts an AC voltage into a DC voltage. It consists of an AC voltage source connected to a diode and a load resistor. The output voltage is zero during the negative half-cycle and reaches a maximum during the positive half-cycle. The output voltage is given by $v_o = v_s + D(v_s)R_L$, where $D(v_s)$ is the diode current-voltage characteristic.

13.26 In the circuit shown in Fig. 13.26, with $V_s = 10 \text{ mV}$, $R_1 = 1 \text{ k}\Omega$, and the voltage across the diodes is 0.1 V , determine the output voltage v_o and the voltage across the load resistor R_L .

Ans.: 0.1 mV, 0.2 V

13.27 If the diode D_1 in circuit of Fig. 13.26 were reversed, what is the transfer characteristic of the circuit?

Ans.: $v_o = 10 \text{ mV} - 0.1 \text{ V} = 9.9 \text{ mV}$

13.28 Find the transfer characteristic of the circuit in Fig. 13.28.

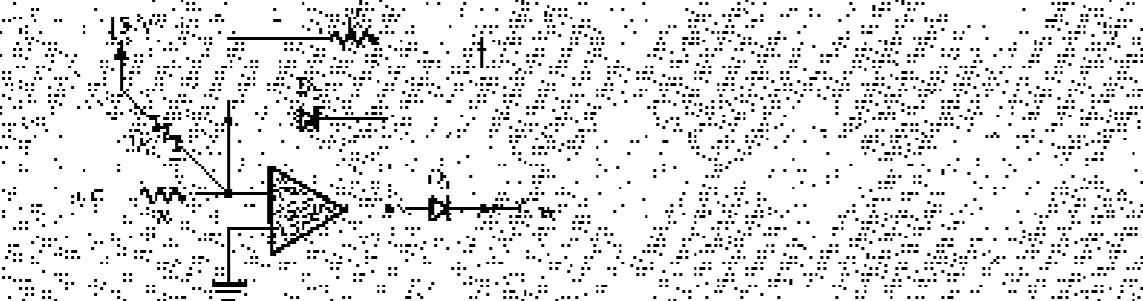


FIGURE 13.28

Ans.: $v_o = 10 \text{ mV} - 0.1 \text{ V} = 9.9 \text{ mV}$

13.8.4 Precision Full-Wave Rectifier

We now derive a circuit for a precision full-wave rectifier. From Chapter 3 we know that full-wave rectification is achieved by inverting the negative halves of the super-signal waveform and applying the resulting signal to another diode (cliff). The outputs of the two rectifiers are then joined to a common load. Such an arrangement is depicted in Fig. 13.36, which also shows the waveforms at various nodes. Note replacing diode D_1 with a zepdiode, and replacing diode D_2 with the inverting amplifier with the inverting precision full-wave rectifier of Fig. 13.35(b); without the coupling diodes, we obtain the precision full-wave rectifier circuit of Fig. 13.37(a).

To see how the circuit of Fig. 13.37(a) operates, consider first the case of positive input at A. The output of A_1 will be positive, turning D_2 on, which will conduct through R_1 and thus close the feedback loop around A_2 . A virtual short circuit will thus be established between

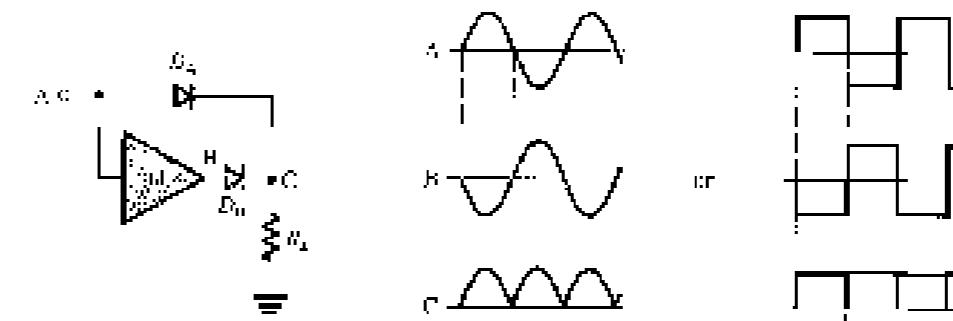


FIGURE 13.36 Precision full-wave rectifier.

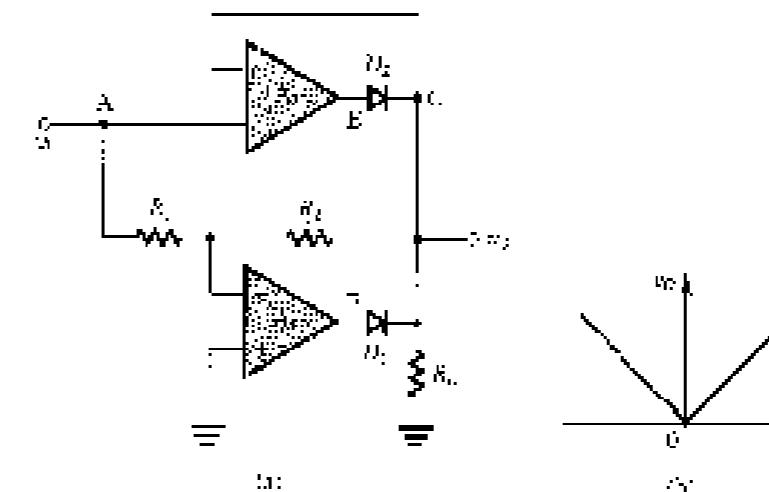


FIGURE 13.37 (a) Precision full-wave rectifier based on the conceptual circuit of Fig. 13.36. (b) Transfer characteristic of the circuit in (a).

The two input terminals of A_1 , and the voltage at the negative-input terminal, which is the output voltage of the circuit, will be the equal to the input. Thus no current will flow through R_1 and R_2 , and the voltage at the inverting input of A_1 will be equal to the input and hence positive. Therefore the output terminal (the o/p of A_1) will be negative until A_1 saturates. This causes D_2 to be turned off.

Next consider what happens when A goes negative. The tendency for a negative voltage at the negative input of A_1 causes E to rise, making D_1 conduct to supply R_2 , and allowing the feedback loop around A_2 to be closed. Thus a virtual ground appears at the negative input of A_2 , and the two equal resistances R_1 and R_2 force the voltage at C, which is the output voltage, to be equal to the negative of the input voltage at A and thus positive. The combination of positive voltage at C and negative voltage at A causes the o/p of A_2 to saturate in the negative direction, thus keeping D_2 off.

The overall result is a perfect full-wave rectifier, as represented by the transfer characteristic in Fig. 13.37(b). This precision is, of course, a result of placing the diodes in open-loop feedback loops, thus masking their nonidealities. This circuit is one of many possible precision full-wave-rectifier or absolute-value circuits. Another related implementation of this function is examined in Exercise 13.30.

EXERCISES

13.29 A full-wave bridge rectifier with four diodes having $V_{DSS} = 10\text{ V}$ and $I_{F} = 100\text{ mA}$ is connected across an AC voltage source of 10 V_{rms} . The output voltage is measured to be $8.4\text{ V}_{\text{rms}}$. What is the peak reverse voltage across each diode? Assume $R_{\text{load}} = 10\text{ k}\Omega$.

13.30 The bridge-diode circuit of Fig. 13.38 gives another possible measurement for the peak-to-average ratio of an AC voltage source. The circuit is identical to Fig. 13.30(b), except that the precision op-amp is replaced by the unity-gain follower of Fig. 13.30(c). The output voltage is measured to be $8.4\text{ V}_{\text{rms}}$. What is the peak-to-average ratio? Assume $R_{\text{load}} = 10\text{ k}\Omega$.



FIGURE 13.38

13.9.5 A Precision Bridge Rectifier for instrumentation Applications

The bridge rectifier circuit studied in Chapter 9 can be combined with an op-amp to provide useful precision circuits. One such arrangement is shown in Fig. 13.39. This circuit causes a current equal to v_A / R to flow through the moving-coil meter M. Thus the meter provides

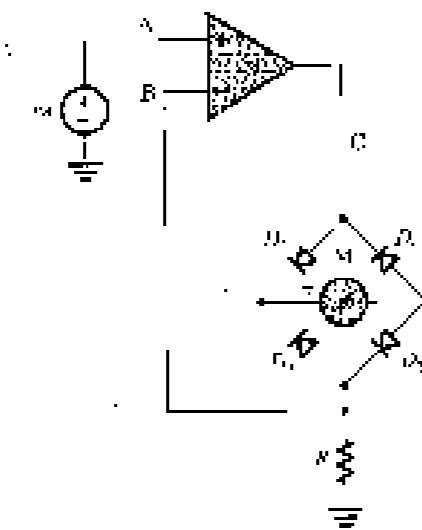


FIGURE 13.39 Use of the bridge in half-wave mode.

a reading that is proportional to the average of the absolute value of the input voltage v_A . All the terminals of the meter and of the diodes are isolated by placing the bridge circuit in the negative feedback loop of the op-amp. Observe that when v_A is positive, current flows from the op-amp output through D_1 , M, D_3 , and K. When v_A is negative, current flows into the op-amp output through D_2 , D_4 , M, and K. Thus the feedback loop remains closed for both polarities of v_A . The resulting virtual short circuit at the input terminals of the op-amp causes a reading of v_A to appear across R. The circuit of Fig. 13.39 provides a relatively accurate, high-input-impedance ac voltmeter using an inexpensive moving-coil meter.

EXERCISE

13.31 In the circuit of Fig. 13.39, if the value of R is increased, what will happen to the output voltage? If R is decreased, what will happen to the output voltage? What would be the minimum and maximum possible values of the output voltage if the diodes have a reverse breakdown voltage of 10 V ?

13.9.6 Precision Peak Rectifiers

Including the diode of the peak detector studied in Chapter 9 inside the negative-feedback loop of an op-amp, as shown in Fig. 13.39, results in a precision peak rectifier. The diode-op-amp combination will be recognized as the superdiode of Fig. 13.23(a). Operation of the circuit in Fig. 13.39 is quite straightforward. For v_A greater than the output voltage, the op-amp will drive the diode on, thus closing the negative-feedback path and causing the op-amp to act as a follower. The output voltage will therefore follow that of the input, with the op-amp supplying the capacitor-charging current. This process continues until the input reaches its peak value. Beyond the positive peak, the op-amp will see a negative voltage between its input terminals. Thus its output will go negative to the saturation level and the diode will turn off. Except for possible discharge through the load resistance, the capacitor will retain a voltage equal to the positive peak of the input. Incorporation of a load resistance is essential if the circuit is required to detect reductions in the magnitude of the positive peak.

13.9.7 A Buffered Precision Peak Detector

When the peak detector is required to hold the value of the peak for a long time, the capacitor should be buffered, as shown in the circuit of Fig. 13.40. Here op-amp A_2 , which should have high input impedance and low input bias current, is connected as a voltage follower. The remainder of the circuit is quite similar to the half-wave-rectifier circuit of Fig. 13.34.

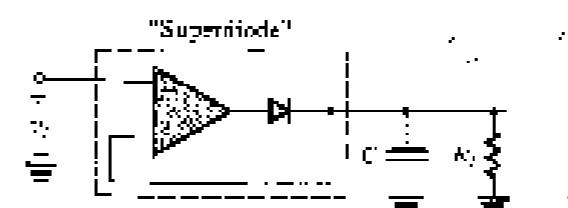


FIGURE 13.40 A precision peak detector obtained by placing the diode in the feedback loop of an op-amp.

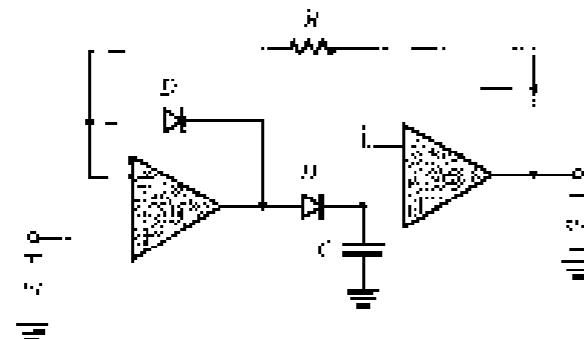


FIGURE 13.40 A modified precision peak detector.

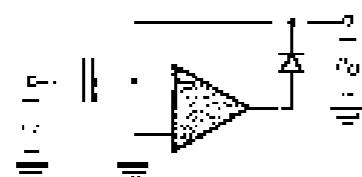


FIGURE 13.41 A precision clamping circuit.

While diode D_1 is the external diode for the peak-saturation operation, diode D_2 acts as a clamping diode to prevent negative saturation, and the associated delay, of an op-amp A_1 . During the falling edge, follower A_2 supplies D_2 with a small current through R . The output of op-amp A_1 will then be clamped at a 0.7 diode drop below the input voltage. Note if the input voltage exceeds above the saturation level, C , which is equal to the output voltage, goes into op-amp A_2 sees a net positive input that drives its output toward the positive saturation level, turning off diode D_2 . Diode D_2 is then turned on and capacitor C is charged to the new positive peak of the input, after which time the circuit returns to the holding state. Finally, note that this circuit has a low-impedance output.

13.9.8 A Precision Clamping Circuit

By replacing the diode in the clamping circuit studied in Chapter 3 with a "superdiode," the precision clamp of Fig. 13.41 is obtained. Operation of this circuit should be self-explanatory.

13.10 SPICE SIMULATION EXAMPLES

The circuits studied in this chapter make use of the nonlinear operation of devices to perform a variety of tasks, such as the stabilization of the amplitude of a sine-wave oscillator and the shaping of a triangular waveform into a sawtooth. Although we have been able to devise simulation methods for the analysis and design of these circuits, a complete pencil-and-paper analysis is nearly impossible. The designer must therefore rely on computer simulation to obtain greater insight into detailed circuit operation, to experiment with different component values, and to optimize the design. In this section, we present two examples that illustrate the use of SPICE in the simulation of oscillator circuits.

13.10.1 Wien-Bridge Oscillator

In our first example, we shall simulate the operation of the Wien bridge oscillator whose circuit schematic is shown in Fig. 13.42. The component values are selected to yield oscillations at 1 kHz. We would like to investigate the operation of the circuit for different settings of R_1 and R_2 , with $R_{10} = R_{11} = 50 \text{ k}\Omega$. Since our discussion starts when $(R_1 - R_{10})/R_{11} > 2$ (see Exercise 13.4), that is, when $R_{11} = 20 \text{ k}\Omega$ and $R_1 = 40 \text{ k}\Omega$, we consider three possible settings: (a) $R_{11} = 15 \text{ k}\Omega$, $R_1 = 35 \text{ k}\Omega$; (b) $R_{11} = 18 \text{ k}\Omega$, $R_1 = 32 \text{ k}\Omega$; and (c) $R_{11} = 20 \text{ k}\Omega$, $R_1 = 25 \text{ k}\Omega$. These settings correspond to loop gains of 1.83, 1.1, and 0.8, respectively.

In PSPice, a 741-type op-amp and 1N814A-type diode are used to simulate the circuit in Fig. 13.42.² A transient analysis simulation is performed with the excitation voltage initially set to zero. This demonstrates that the op-amp offset voltage is sufficient to cause the oscillations to start without the need for special start-up circuitry. Figure 13.43 shows the simulation results.

PARAMETERS:

$C_3 = 16\text{n}$
 $C_2 = 10\text{n}$
 $R_{10} = 18\text{k}$
 $R_{11} = 50\text{k} \times (R_{11})$
 $R_1 = 13\text{k}$
 $R_2 = 10\text{k}$
 $R_3 = 1\text{k}$
 $R_4 = 10\text{k}$
 $V_{CC} = 15$
 $V_{EE} = -15$

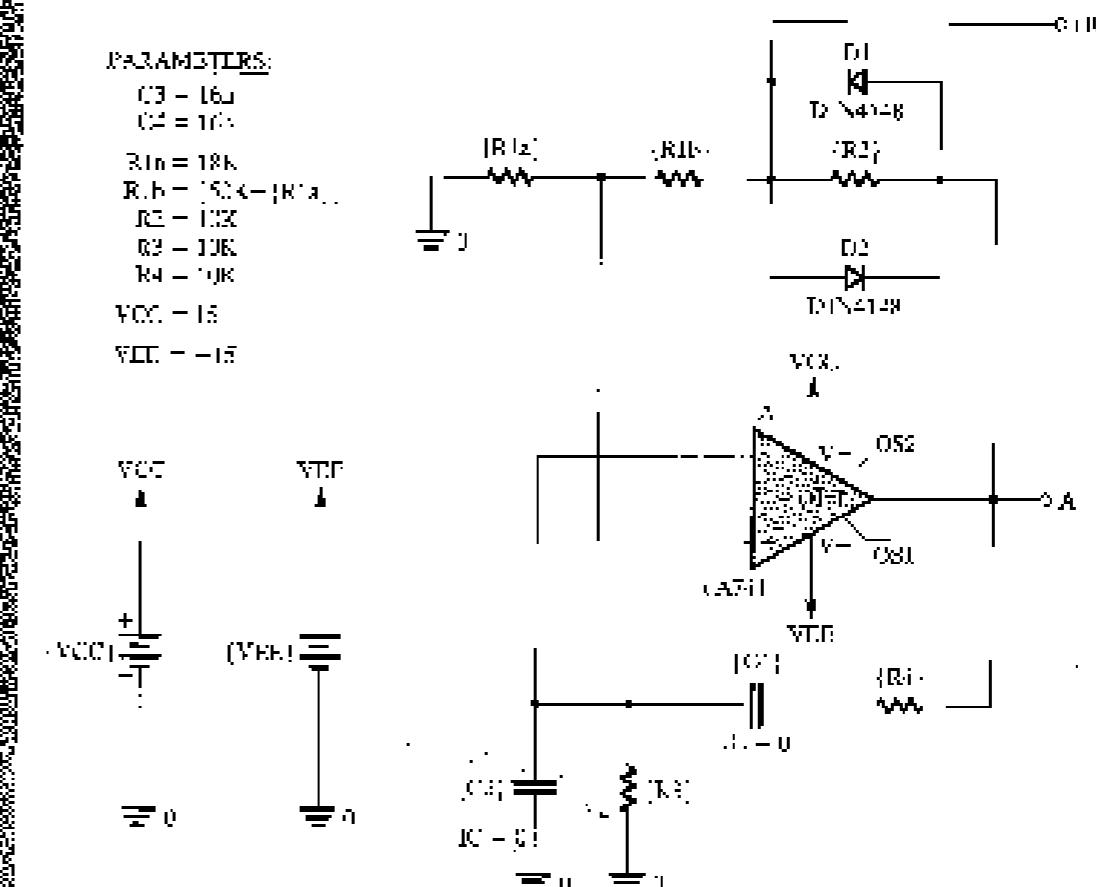


FIGURE 13.42 Example 13.1: Schematic diagram of a Wien bridge oscillator.

²The SPICE models for the 741 op-amp and the 1N814A diode are available in PSPice. The 741 op-amp was implemented in Example 2.9. The 1N814A diode was used in Example 2.10.

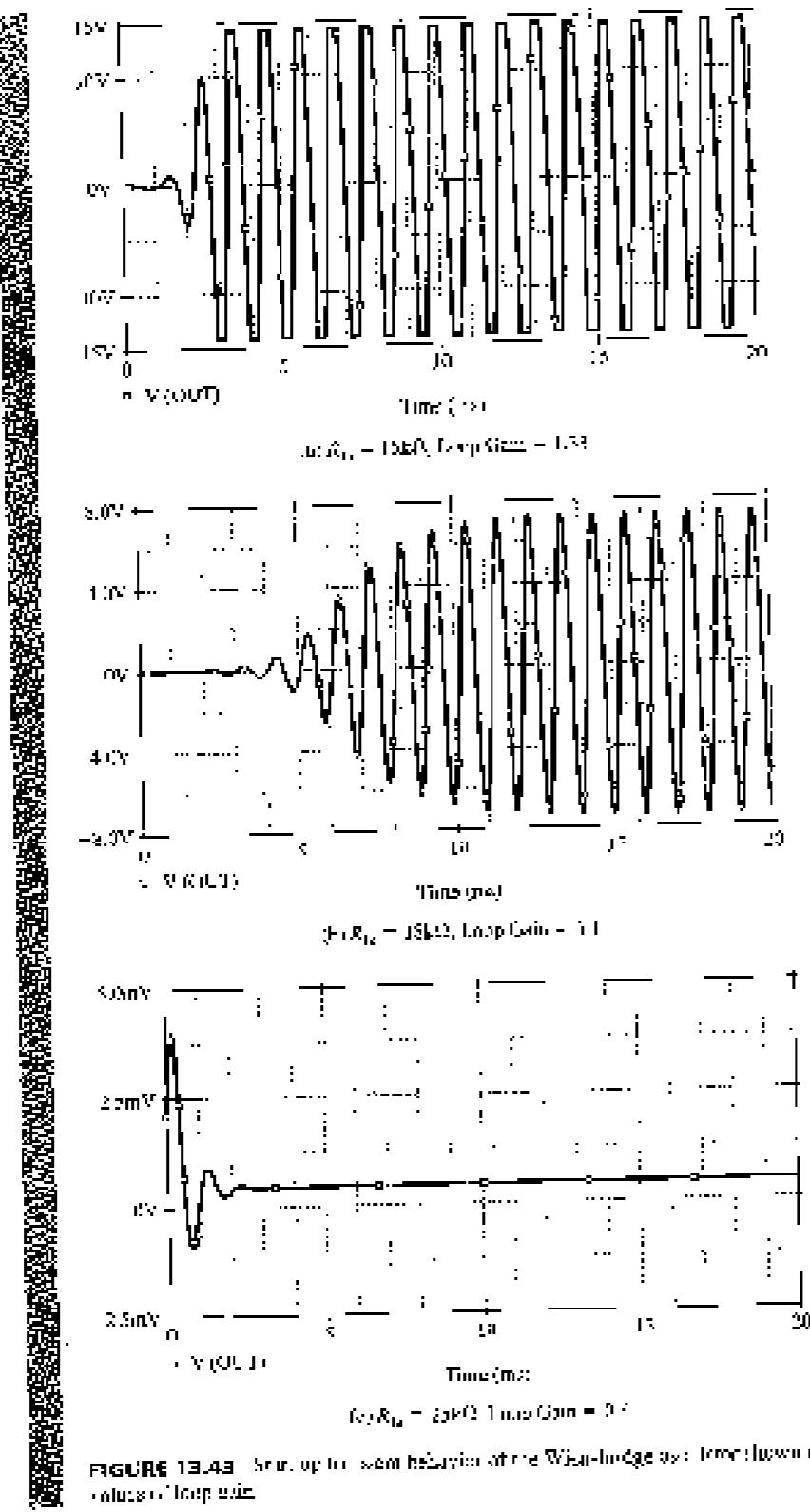


FIGURE 13.43 Start-up transient behavior of the Wien-bridge op-amp (shown in Fig. 13.42) for various values of loop gain.

The graph in Fig. 13.43(a) shows the output waveform obtained for a loop gain of 1.53. Observe that although the oscillations grow and stabilize rapidly, the distortion is considerable. The output obtained for a loop gain of 1.1, shown in Fig. 13.43(b), is much less distorted. However, as expected, as the loop gain is reduced toward unity, it takes longer for the oscillations to build up and for the amplitude to stabilize. Notice also the frequency is 983.6 Hz, which is reasonably close to the design value of 1 kHz, and the amplitude is 7.37 V. Finally, for a loop gain of 0.8, the output shown in Fig. 13.43(c) confirms our expectation that sustained oscillations cannot be obtained when the loop gain is less than unity.

PSpice can be used to investigate the spectral purity of the output sine wave. This is achieved using the Fourier analysis facility. It is found that in the steady state the output for the case of a loop gain of 1.1 has a THD figure of 1.8%. When the oscillator output is taken at the op-amp output (voltage v_o), a THD of 2.37% is obtained, which is expected to be higher than 1% for the voltage v_{out} , but not by very much. The poor reward of the op-amp is reflected in much more current draw to take the output.

ACTIVE-FILTER-TUNED OSCILLATOR

In this example, we use PSpice to verify our contention that a superior op-amp oscillator can be realized using the active-filter-tuned circuit of Fig. 13.11. We also investigate the effect of changing the value of the filter Q factor on the spectral purity of the output sine wave.

Consider the circuit whose component schematic is shown in Fig. 13.44. For this circuit, the center frequency is 1 kHz, and the Q factor Q is 5 when $R_1 = 50 \text{ k}\Omega$ and 20 when $R_1 = 200 \text{ k}\Omega$. As in the case of the Wien-bridge circuit (Example 13.1, 741-type op-amp and 1N-1481 diodes), we utilize in PSpice a transient-analysis simulation to perform with the capacitor voltages initially set to zero. To be able to compute the Fourier components of the output, the analysis interval chosen must be long enough to allow the oscillator to reach a steady state. The time to reach a steady state is in turn determined by the value of the filter Q; the higher the Q, the longer it takes the output to settle. For Q = 5, it was determined, through a combination of approximate calculations and experimentation using PSpice, that 20 ms is a reasonable estimate for the analysis time interval. For plotting purposes, we use 200 points per period of oscillation.

The results of the transient analysis are plotted in Fig. 13.45. The upper graph shows the sinusoidal waveform at the output of op-amp A_1 (voltage v_1). The lower graph shows the waveform across the diode limiter (voltage v_2). The frequency of oscillation is found to be very close to the design value of 1 kHz. The amplitude of the sine wave is determined using Probe (the graphical interface of PSpice) to be 1.13 V (or 2.1 V p-p). Note that this is lower than the 2.6-V estimated in Exercise 13.7. The latter value, however, was based on an estimate of 0.7-V drop across each conducting diode in the limiter. The Invert waveform in Fig. 13.45 indicates that the diode drop is closer to 0.5 V, i.e., a 1-V peak-to-peak amplitude of the pseudo-square wave. We should therefore expect the peak-to-peak amplitude of the output sinusoid to be lower than 2.6 V by the same factor, and indeed it is approximately the case.

In PSpice, the Fourier analysis of the output sine wave indicates that THD = 1.5%. Repeating the simulation with Q increased to 20 (by increasing R_1 to 200 k Ω), we find that the value of THD is reduced to 0.01%. Thus, one again confirms that the value of the filter Q can be used as an effective means for controlling the THD of the output waveform and justified.

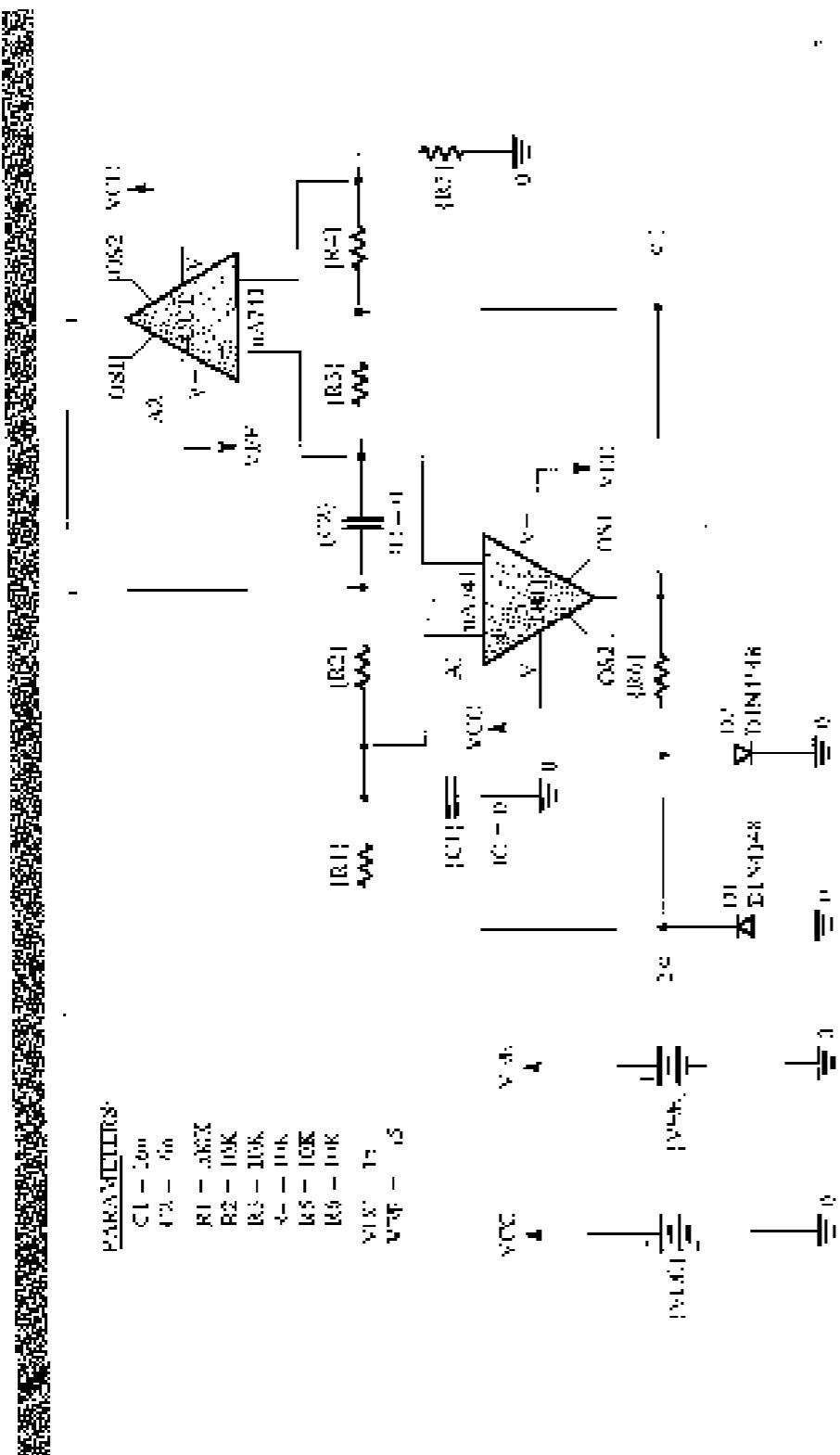


FIGURE 13.44 Example 13.2: Wien bridge oscillator with active filter and control for which the Q of the filter is adjustable by a potentiometer.

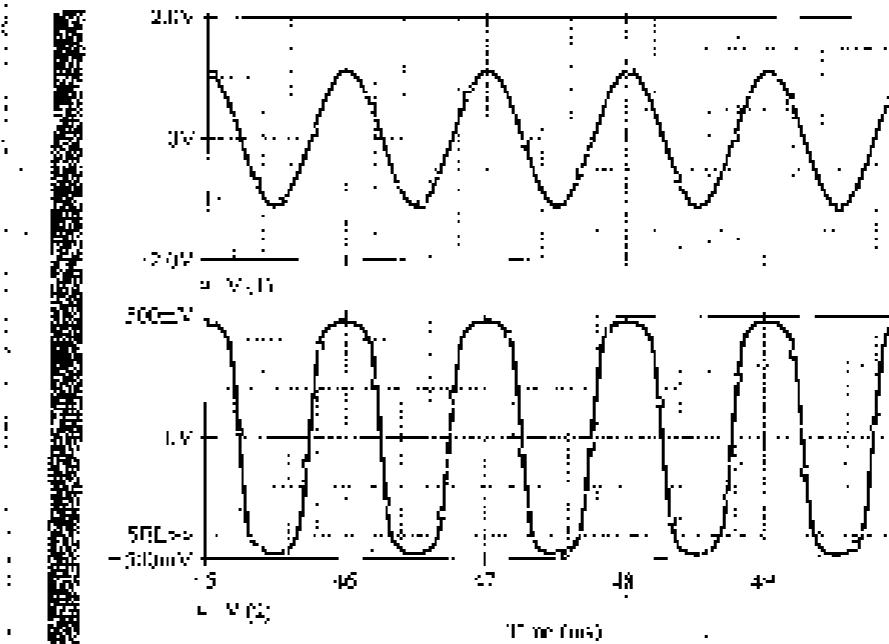


FIGURE 13.45 Output waveforms of the active filter-based oscillator shown in Fig. 13.44 for $P = 5$ ($R_1 = 50\text{ k}\Omega$).

SUMMARY

- There are two distinctly different types of signal generation: linear and non-linear, which utilize sinusoidal waveforms and continuous oscillations or frequency generation, which employ a switching mechanism implemented with a multivibrator circuit.
- A linear oscillator can be realized by placing a frequency-selective network in the feedback path of an amplifier (an op-amp or a transistor). The circuit will oscillate at the frequency ω if the total phase shift around the loop is 2π , provided that the magnitude of loop gain at this frequency is equal to, or greater than, unity.
- If the oscillator, the magnitude of loop gain is greater than unity, the amplitude will increase until a point near amplitude control mechanism is activated.
- The Wien bridge oscillator, the phase-shift oscillator, the quadrature oscillator, and the active-filter-based oscillator are regular oscillators, i.e., frequency ω is $\approx 1/\sqrt{LC}$. These circuits employ RC networks together with nonlinear transmission. For higher frequencies, LC-based or crystal-based oscillators are utilized. A popular configuration is the Colpitts circuit.
- Unstable oscillators provide the highest possible frequency accuracy and stability.
- There are three types of multivibrator: bistable, monostable, and astable. Open-loop driven implementation of multivibrator and closed-loop coupled multivibrators that require high precision. Implementations using digital logic gates are studied in Chapter 14.
- The bistable multivibrator has two stable states and can remain in either one indefinitely. It changes state when triggered. A component will stay in a stable state.
- A monostable multivibrator, also known as a one-shot multivibrator, has one stable state in which it can remain indefinitely. When triggered, it goes into a quasi-stable state in which it remains for a predetermined interval, thus generating a one-shot pulse of known width.
- An astable multivibrator has no stable state; it oscillates between two quasi-stable states, remaining in each for a predetermined interval. It thus generates a periodic waveform at the output.

- (g) A feedback loop consisting of an inductor and a variable voltage source can be used to generate triangular and square waveforms.
- (h) The first timer, a unidirectionally controlled R_s , can be used with external resistors and a capacitor to implement high-quality sine-wave and astable multivibrators.
- (i) A sine waveform can be generated by feeding a single-frequency waveform to a sine-wave shaper. A sine-wave shaper

can be implemented either by using diodes (or transistors) and resistors, or by using an amplifier having a non-linear transfer characteristic that approximates the sine function.

- (j) Diodes can be combined with op-amps to implement precision rectifier circuits in which negative feedback serves to mask the nonidealities of the diode characteristics.

PROBLEMS

SECTION 13.1: BASIC PRINCIPLES OF SINUSOIDAL OSCILLATORS

- P13.1** Consider a sinusoidal oscillator consisting of an amplifier having a frequency-independent gain A (where A is positive), and a second-order lowpass filter with a pole frequency ω_h , a pole Q derived from ω_h , and a corner frequency ω_m .

(a) Find the frequency of oscillation, and the condition such that A must rapidly decrease after oscillation begins.

- (b) Derive an expression for $d\phi/d\omega$, evaluated at $\omega = \omega_h$.
- (c) Use the result of (b) to find an expression for ω_m without knowing ω_h , the frequency of oscillation resulting from a phase-angle change of $\Delta\phi$, and the amplitude of the output function.

$$\text{Answer: } \frac{d\phi}{d\omega} \Big|_{\omega = \omega_h} = \frac{1 - \omega_h^2}{1 + \omega_h^2}$$

- P13.2** For the oscillator described in Problem 13.1, assume that, independent of the values of A and ω_h , the poles of the circuit lie in a radial distance of ω_h from the origin of the complex plane. Find the value of $A\omega_m$ that results in poles appearing on the $j\omega$ axis, ω_m being the rightmost of the $j\omega$ plane, at a horizontal distance from the $j\omega$ axis of $\omega_h/2Q$.

- P13.3** Sketch a circuit for a sinusoidal oscillator formed by an op-amp configured in the noninverting configuration and a bandpass filter implemented by an RLC resonator such as that in Fig. 13.1(d). What should the amplifier gain be to obtain sustained oscillation? What is the frequency of oscillation? Find the percentage change in the oscillation frequency from a change of $\pm 10\%$ in the value of R_2 , L , C , R_1 , and G .

- P13.4** An oscillator is formed by loading a transconductance-amplifier having a positive gain with a parallel RLC circuit, and connecting the output directly to the input (thus applying positive feedback with a factor $\beta = 1$). Let the transconductance amplifier have an input resistance of $10\text{ k}\Omega$ and an output resistance of $10\text{ k}\Omega$. The LC resonator has $L = 10\text{ }\mu\text{H}$, $C = .001\text{ }\mu\text{F}$, and $G = 100$. For what value of

transconductance G_m will the circuit oscillate? At what frequency?

- P13.5** In a particular oscillator, one governed by the structure of Fig. 13.1, the frequency-selective network exhibits a loss of 20 dB and a phase shift of 180° at ω_h . What is the minimum value of the phase shift that the amplifier must have for oscillation to begin?

- P13.6** Consider the circuit of Fig. 13.5(a) with R_2 removed to realize the configuration shown in Fig. 13.5(b). Find suitable values for R_1 and R_3 so that the compensation voltage across 10 V and the slope of the limiting characteristic is 0.1 V/V power supply voltage $v = 10\text{ V}$ and assume the voltage drop of Δv is bounded to double its DC value.

- P13.7** Consider the circuit of Fig. 13.5(a) with R_2 removed to realize the configuration shown in Fig. 13.5(b). Sketch the forward characteristic by connecting a dc source V_b to the virtual ground of the op-amp (1000 μA) and resistor R_2 ; the transfer characteristic is defined where $b = \omega/\omega_h$ as the poles $\omega_h = 0.01\sqrt{K_1 K_2}$. Utilizing available $\pm 15\text{-V}$ dc supplies for V_b , V_a , V_o , and an AC component of 10 V so that the limiting levels are $\pm 5\text{ V}$ and the compensation threshold is at $b = -5$. Neglect the diode voltage ($v_{DSS} = 0$), assume $V_D = 0$. The input resistance of the compensation is to be $100\text{ }\Omega$, and the sum of the limiting regions is to be $30/05\text{ V/V}$. Use standard SPICE notation (see Appendix C).

- P13.8** Sketching the zero voltages of Z_1 and Z_2 by V_{Z1} and V_{Z2} and requiring that in the forward direction the voltage drop is approximately 0.1 V , sketch and clearly label the transfer characteristic v_o/v_i of the circuit in Fig. P13.8. Assume the op-amp to be ideal.

SECTION 13.2: OP-AMP-RC OSCILLATOR CIRCUITS

- P13.9** For the Wien bridge oscillator circuit in Fig. 13.4, show that the transfer function of the feedback network

Circuit 13.1

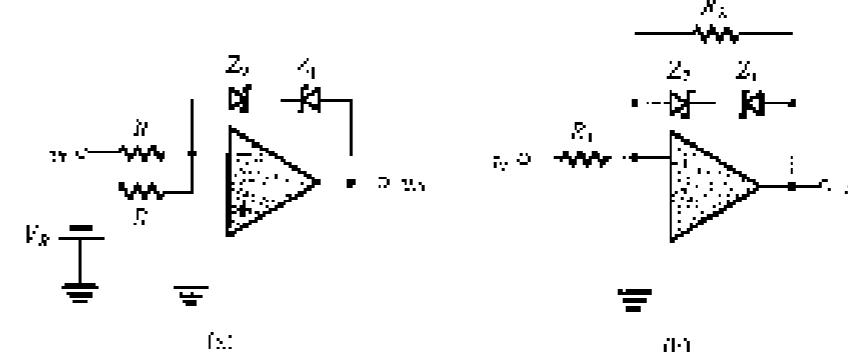


FIGURE P13.9

- $V_o(s)/V_{in}(s)$ is that of a compensated ω -windup Q of the poles, and find the corner-frequency ratio.

- P13.10** For the Wien-bridge oscillator of Fig. 13.4, let the closed-loop amplitude obtained by the op-amp and the resistors R_1 and R_2 exhibit a phase shift of 0.1° rad in the neighborhood of $\omega = 1/\sqrt{CR}$. Find the frequency at which oscillations can occur in this case in terms of $1/\sqrt{CR}$. (Hint: Use Eq. 13.1.1.)

- P13.11** For the Wien-bridge oscillator of Fig. 13.4, use the expression for $b = \omega/\omega_h$ in Eq. 13.10(a) to find the poles of the closed-loop system. Give the expression for the pole Q , and use it to show that ω locates the poles in the right half of the s plane. R_1/R_2 must be selected to be greater than 2.

- P13.12** Reconsider Exercise 13.1 with R_1 and R_2 increased to reduce the output voltage. What values are needed for a peak-to-peak output of 10 V ? What results if R_2 and R_1 are open circuited?

- P13.13** For the circuit in Fig. P13.13 find ω_m . Given the frequency for zero-loop phase, and R_2/R_1 , find oscillation.

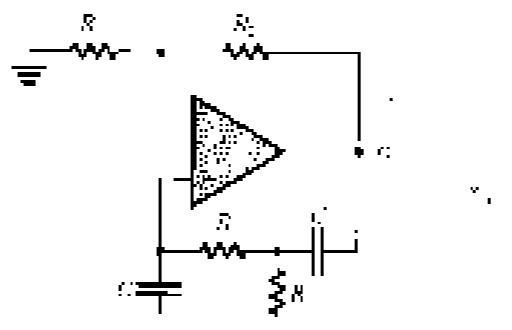


FIGURE P13.13

- 13.14 Refer to Problem 13.12. See the circuit in Fig. P13.14.

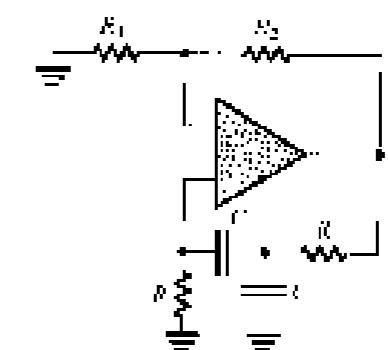


FIGURE P13.14

- P13.15** Consider the circuit of Fig. 13.6 with the $10\text{ k}\Omega$ potentiometer replaced by two fixed resistors: $10\text{ k}\Omega$ between the op-amp's negative input and ground, and $18\text{ k}\Omega$. Modeling each diode as a diode voltage in series with a $100\text{ }\Omega$ resistor, find the peak-to-peak amplitude of the output signal.

- P13.16** Recalculate the circuit of Fig. 13.6 for operation at 10 kHz using the same values of resistance. If $\omega = 10\text{ kHz}$ the op-amp provides an excess phase shift (Digital 8.1), what will be the frequency of oscillation? Assume that the phase shift is increased by the op-amp's negative conductance for frequencies above 10 kHz . To achieve operation at 10 kHz , what assumption must be made in the shunt resistor of the Wien bridge? Also, to what value must R_2/R_1 be changed?

- P13.17** For the circuit of Fig. 13.8, connect an additional $R = 10\text{ k}\Omega$ resistor in series with the rightmost capacitor C_1 . For this modification (and ignoring the amplitude stabilization circuitry) find the frequency ω by breaking the circuit at node A , and A_1 's open-loop gain to begin, and find t_0

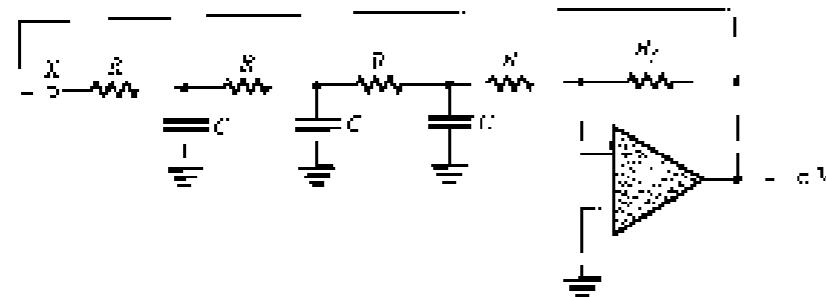


FIGURE P13.18

- P13.18** For the circuit in Fig. P13.18, neglect the losses of the X and the op amp's working bandwidth for simplicity. (a) Find V_2 in terms of V_{in} . For $R = 10 \text{ k}\Omega$, find C and R_2 so that ω_m oscillates at 10 kHz .

- P13.19** Consider the quadrature oscillator circuit of Fig. 13.9 without the limiter. Let the resistance R_i be equal to $2\pi f_i C_i (\Delta/4)^{1/2}$, where $i = 1, 2$. Show that the poles of the characteristic equation lie in the right-half plane and given by $\lambda = \pm 1/\sqrt{C_1 C_2}(\Delta/4)^{1/2}$.

- P13.20** Assuming that the overshoot waveform in Exercise 13.7 is nearly an ideal square wave and that the resonator Q is 20, provide an estimate of the distortion in the output sine wave by comparing the amplitude relative to the fundamental: (a)

- (a) the second harmonic
- (b) the third harmonic
- (c) the 10th harmonic
- (d) the rms of derivatives to the tenth

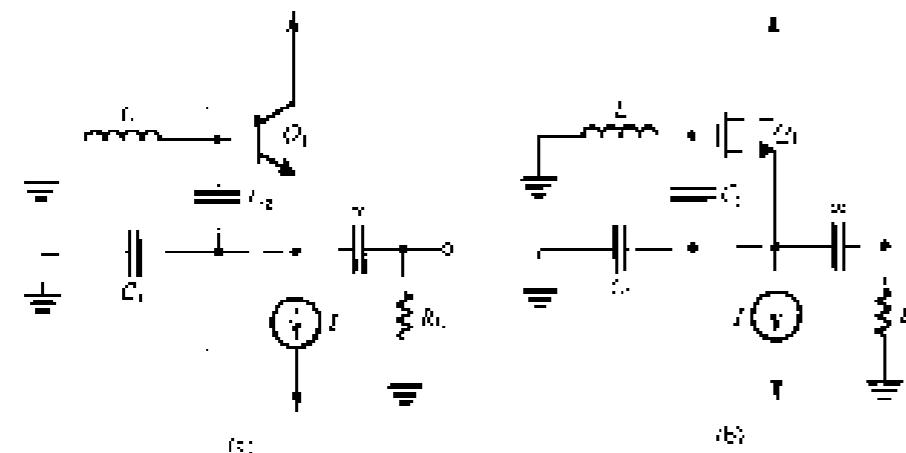


FIGURE P13.21

Note that a sine wave of amplitude 1 and frequency ω is represented by two series:

$$\frac{4V}{\pi} \cos \omega t + \frac{1}{3} \sin 3\omega t - \frac{1}{5} \cos 5\omega t + \dots$$

SECTION 13.3: LC AND CRYSTAL OSCILLATORS

- S13.21** Figure P13.21 shows four oscillator circuits of the Colpitts type, complete with bias circuit. For each circuit, derive an equation governing start-up operation, and find the frequency of oscillation and the gain condition that causes the oscillations start.

- S13.22** Consider the oscillator circuit in Fig. P13.22, and assume for simplicity that $\beta = \infty$:

- (a) For the frequency of oscillation and the maximum value of R_2 (in terms of the bias current I_b) for oscillation to occur,

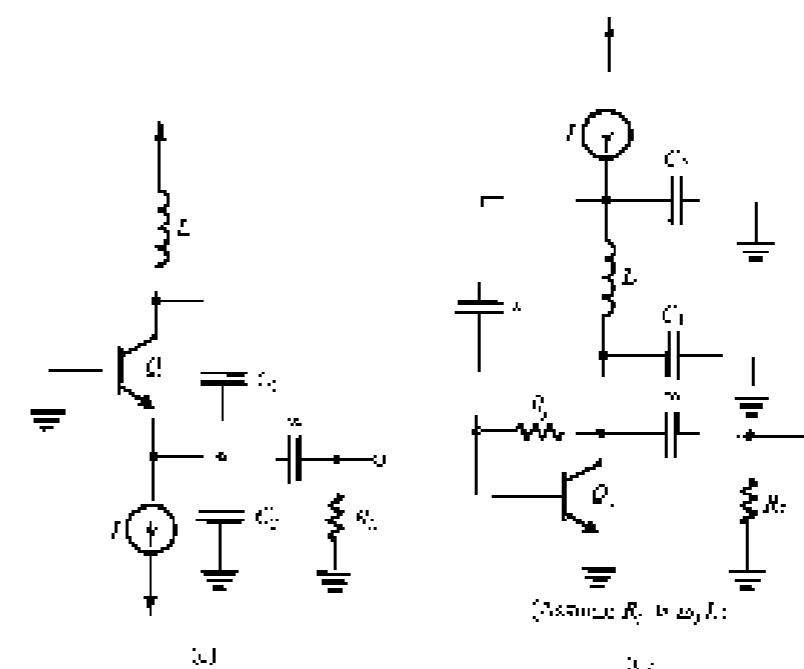


FIGURE P13.21 (Continued)

- (b) If R_2 is selected equal to $4 V$, make it in the right-hand sense, convince yourself that oscillations will start. In which biasing does the point that V_c is large enough to turn the BJTs on and off, when the voltage at the collector of Q_1 will be a square wave of 1 V peak-to-peak. Estimate the peak-to-peak amplitude of the output sine wave V_o .

- P13.23** Consider the Pierce crystal oscillator of Fig. 13.17, with the crystal as specified in Exercise 13.4. Let C_1 be variable in the range 1 pF to 10 pF, and let C_2 be fixed at 10 pF. Find the range over which the oscillation frequency can be varied. (Hint: Use the result in the caption leading to the expression in Eq. 13.27.)

SECTION 13.4: BISTABLE MULTIVIBRATORS

- P13.24** Consider the bistable circuit of Fig. 13.20(a) with the op amp's positive input terminal connected to a positive-voltage source V through a resistor R_2 :

- (a) Derive expressions for the threshold voltages V_{T1} and V_{T2} in terms of the op amp's saturation levels L_1 and L_2 , V , R_1 , R_2 , and V_s .
- (b) Let $L_1 = -L_2 = 1.5 \text{ V}$, $V = 15 \text{ V}$, and $R_1 = 10 \text{ k}\Omega$. Find the values of R_2 and R_3 that result in $V_{T1} = -4.0 \text{ V}$ and $V_{T2} = -5.1 \text{ V}$.

- P13.25** Consider the bistable circuit of Fig. 13.20(b) with the op amp's negative input terminal disconnected from ground and connected to a reference voltage V_s :

- (a) Derive expressions for the threshold voltages V_{T1} and V_{T2} in terms of the op amp's saturation levels L_1 and L_2 , R_1 , R_2 , and V_s .
- (b) Let $L_1 = -L_2 = 1$ and $R_1 = 10 \text{ k}\Omega$. Find R_2 and V_s that result in threshold voltages of 1 and $-1/12$.

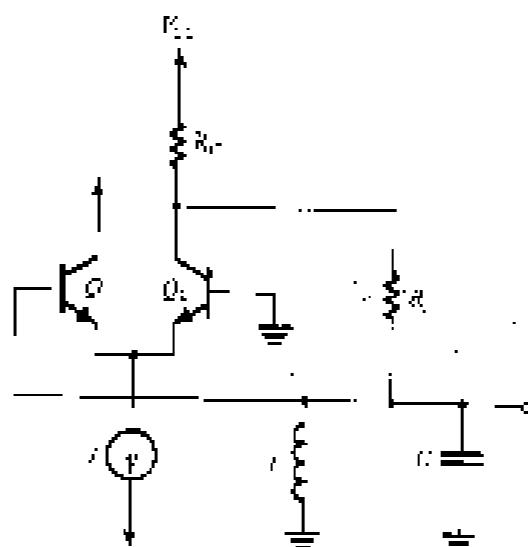


FIGURE P13.22

- P13.26** For the circuit in Fig. P13.26, sketch and label the transfer characteristic $v_o - v_i$. The diodes are assumed to have a constant 0.7-V drop when conducting, set the op-amp saturation at +12 V. What is the maximum diode current?

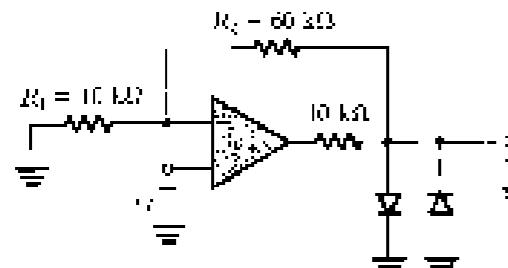


FIGURE P13.26

- P13.27** Consider the circuit of Fig. P13.26 with R_f short-circuited and R_i short-circuited. Sketch and label the transfer characteristic $v_o - v_i$. Assume that the diodes have a constant 0.7-V drop when conducting and that the op-amp saturates at ±12 V.

- P13.28** Consider a bistable circuit having a noninverting transfer characteristic with $L = -L = 12$ V, $V_{D1} = 1$ V, and $V_{D2} = +1$ V.

- (a) For a 0.5-V amplitude sine-wave input having zero average, what is the output?
 (b) Describe the output if a sinusoidal of frequency f and amplitude of 1.1 V is applied to the input. By how much can the average of the sinusoidal input shift before the output becomes a constant value?

- P13.29** Design the circuit of Fig. P13.29(a) so that its transfer characteristic with 10-V output levels has ±7.5-V

threshold values. Design so that when $v_i = 0$ V a current of 0.1 mA flows in the feedback resistor and a current of 1 mA flows through the zener diode. Assume that the output saturation levels of the op amp are ±12 V. Specify the voltages of the zener diodes and give the values of all resistors.

SECTION 13.5: GENERATION OF SQUARE AND TRIANGULAR WAVEFORMS USING ASTABLE MULTIVIBRATORS

- P13.30** Find the frequency of oscillation of the circuit in Fig. 13.24(b) for the case $R_1 = 10\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $C = 20\text{ nF}$, and $R = 50\text{ k}\Omega$.

- P13.31** Augment the astable multivibrator circuit of Fig. 13.24(b) with an output limiter of the type shown in Fig. 13.30(b). Design the circuit to obtain an output square wave with 5-V amplitude and 1-kHz frequency using a transmission capacitor C . Use $\beta = 0.1\mu A$ and design for a current in the resistive diode approximately equal to the zener current in the R3 network over half cycle. Assuming +12-V op-amp saturation voltages, arrange for the circuit to operate at a current of 1 mA.

- P13.32** Using the scheme of Fig. 13.23, design a circuit to provide square waves of 10-V peak-to-peak and triangular waves of 10 V peak-to-peak. The frequency is to be 1-kHz. Implement the bistable circuit with the circuit of Fig. 13.28(d). Use a 0.01-μF capacitor, and specify the values of all resistors and the required zener voltage. Design for a minimum zener current of 1 mA and for a minimum current in the resistive diode of 0.2 mA. Assume that the op-amp saturation levels of the op-amps are ±12 V.

- P13.33** The circuit of Fig. P13.33 consists of an inverting bistable multivibrator with an output limiter and a noninverting integrator. Using equal values for all resistors except R , and a 0.01-F capacitor, design the circuit to obtain a square

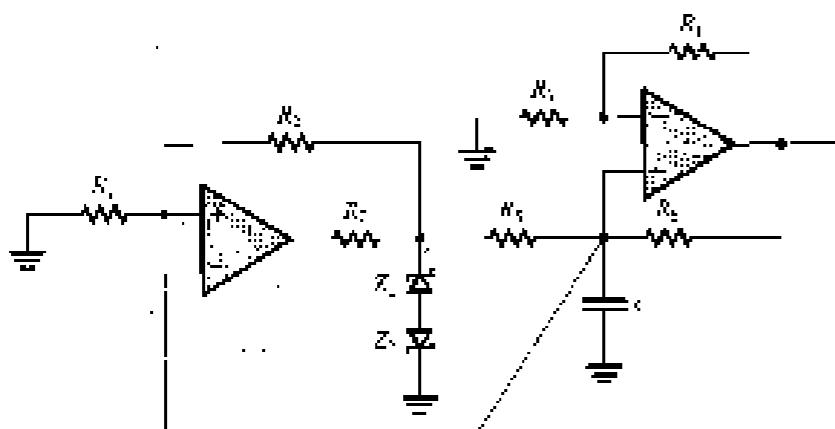


FIGURE P13.33

wave at 1 V off-set of the bistable multivibrator of 10-V peak-to-peak amplitude and 10-kHz frequency. Sketch and label the waveform at the integrator output. Assuming 1.3-V op-amp saturation levels, design for a minimum current of 1 mA. Specify the zener voltage demands, and give the values of all resistors.

SECTION 13.6: GENERATION OF A STANDARDIZED PULSE—THE MONOSTABLE MULTIVIBRATOR

- P13.34** Figure P13.34 shows a monostable multivibrator circuit. In the stable state, $v_o = J_2 - v_1 = 10$ and $v_2 = -V_{DD}$. The circuit can be triggered by applying a positive input pulse of height greater than V_{DD} . In normal operation, $C_1R_1 > CR$. Show the resulting waveforms of v_2 and v_o . Also, show that the pulse generated at the output will have a width t_p given by

$$t_p = CR \ln \frac{CL + L}{CL - L}$$

Note that this circuit has the interesting property that the pulse width can be controlled by changing V_{DD} .

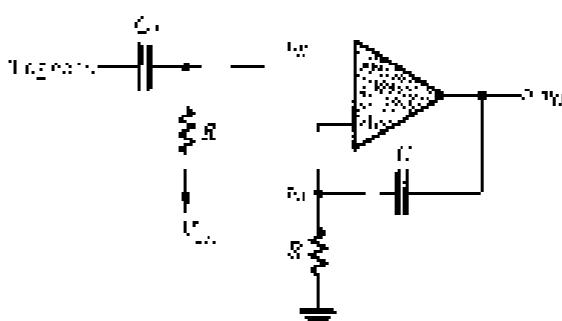


FIGURE P13.34

- P13.35** For the monostable circuit considered in Exercise 13.9, calculate the recovery time.

- P13.36** Using the circuit of Fig. 13.26, with a unity-gain op amp for which the saturation levels are ±12 V, design a monostable multivibrator to provide a negative output pulse of 100-μs duration. Use a zener of 0.1 μF and 1 kΩ. When over-saturation occurs, choose resistors of 100 kΩ in your design. Diodes have a drop of 0.7 V. What is the minimum current step size that will ensure triggering? How many times the circuit must be triggered in a series in which multiplying is possible to obtain a pulse?

SECTION 13.7: INTEGRATED-CIRCUIT TIMERS

- P13.37** Consider the 555 timer of Fig. 13.20 where the Threshold and the Trigger input terminals are joined together

and connected to an input voltage v_i . Verify that the transfer characteristic $v_o - v_i$ is that of an inverting bistable circuit with threshold $V_{D1} = (V_{DD} - V_{TH})/2$ and $V_{D2} = (V_{DD} + V_{TH})/2$ and output levels of 0 and V_{DD} .

- P13.38** (a) Using a 1-nF capacitor C in the circuit of Fig. 13.28(c), find the value of R that results in an output pulse of 100 microseconds.

- (b) If the 555 timer used in (a) is powered with $V_{DD} = 12$ V and assuming that V_{DD} can be varied continuously (i.e., it need not remain equal to V_{DD}), find its required value so that the pulse width is increased to 20 μs, with other conditions the same as in (a).

- P13.39** Using a Graphical expression, design the basic circuit of Fig. 13.29(c) to obtain a square wave with a 10-kHz frequency and a 75% duty cycle. Specify the values of R and C .

- P13.40** The node in the 555 timer at which the voltage is $V_{DD}/2$, i.e., the inverting input terminal of a comparator, is usually connected to an external terminal. This allows the user to change V_{DD} externally (i.e., V_{DD} no longer remains at $\frac{1}{2}V_{DD}$). Note, however, that whatever the value of V_{DD} becomes, V_{DD} always remains $\frac{1}{2}V_{DD}$.

- (a) For the astable circuit of Fig. 13.29, derive the expressions for V_{DD} and t_p , expressing them in terms of V_{DD} and V_{DD} .
 (b) For the case $C = 1\text{ nF}$, $R_1 = 7.2\text{ k}\Omega$, $R_2 = 1.6\text{ k}\Omega$, and $V_{DD} = 5$ V, find the frequency of oscillation and the duty cycle of the resulting square wave when no external voltage is applied at the terminal V_{DD} .

- (c) For the design in (b), for a sine-wave signal of a much lower frequency than that found in (b) and a 1-V peak amplitude be capacitive coupled to the circuit, since V_{DD} is a digital signal will cause V_{DD} to change around its quiescent value of 1.5 Vdc and thus V_{DD} will change correspondingly—a modulation process. Find t_p and the frequency of oscillation and the duty cycle at the two extreme values of V_{DD} .

SECTION 13.8: NONLINEAR WAVEFORM-SHAPING CIRCUITS

- P13.41** The two-diode circuit shown in Fig. P13.41 can produce a crude approximation to a sine-wave output when driven by a triangular waveform. To obtain a good approximation, we select the peak of the triangular wave to be V_s so that the slope of the desired sine wave at the zero-crossings is equal to that of the triangular wave. Also, the value of R is selected so that when $v_o = 0$, each the output voltage is 0 or V_s to the desired peak of the sine wave. If the diodes exhibit a voltage drop of 0.7 V at 1-mA current, operating at the rate of 0.1 V per decade, find the value of V_s and R that will yield an approximation to a sine wave of 0.7-V peak amplitude. Then find the angles θ (where $\theta = 90^\circ$) when v_o is at its peak in which the output of the circuit is 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.75, 0.8, 0.9, 0.95, and 1.0. Use the angle

values obtained to determine the values of the other sine wave (i.e., $0.7 \sin \theta$), and thus find the percentage error of this circuit as a sine shaper. Provide your results in tabular form.

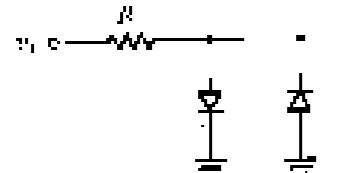


FIGURE P13.41

P13.42 Design a two-segment sine wave shaper using a 10-kΩ input resistor, two diodes, and two clamping voltages. The circuit, fed by a 10-V peak-to-peak triangular wave, should limit the amplitude of the output signal via a 0.7 V peak-to-a-value curve, resulting in that of a sine wave whose zero-crossing slope matches that of the triangle. What are the clamping voltages you have chosen?

P13.43 Show that the output voltage of the circuit in Fig. P13.43 is given by

$$v_0 = -n F_2 \ln \left(\frac{V_1}{I_d R_1} \right) \quad n > 0$$

where I_d and n are the diode parameters and V_1 is the

thermal voltage. Since the output voltage is proportional to the logarithm of the input voltage, the circuit is known as a logarithmic amplifier. Such amplifiers find application in situations where it is desired to compress the signal voltage.

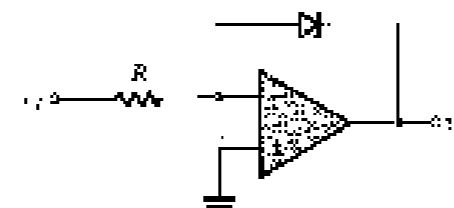


FIGURE P13.43

P13.44 Verify that the circuit in Fig. P13.24 implements the transfer characteristic $v_0 = v_1 v_2$ for $v_1, v_2 > 0$. Such a circuit is known as an analog multiplier. Check the circuit's performance for various combinations of input voltage of values, say 0.5 V, 1 V, 2 V, and 3 V. Assume all resistors to be identical with 500-mΩ value and $I_d = 1$ mA. Note that a square can easily be produced using a single input (e.g., v_1) connected via a 0.5-kΩ resistor (inverter load, i.e., 1-kΩ resistor shown).

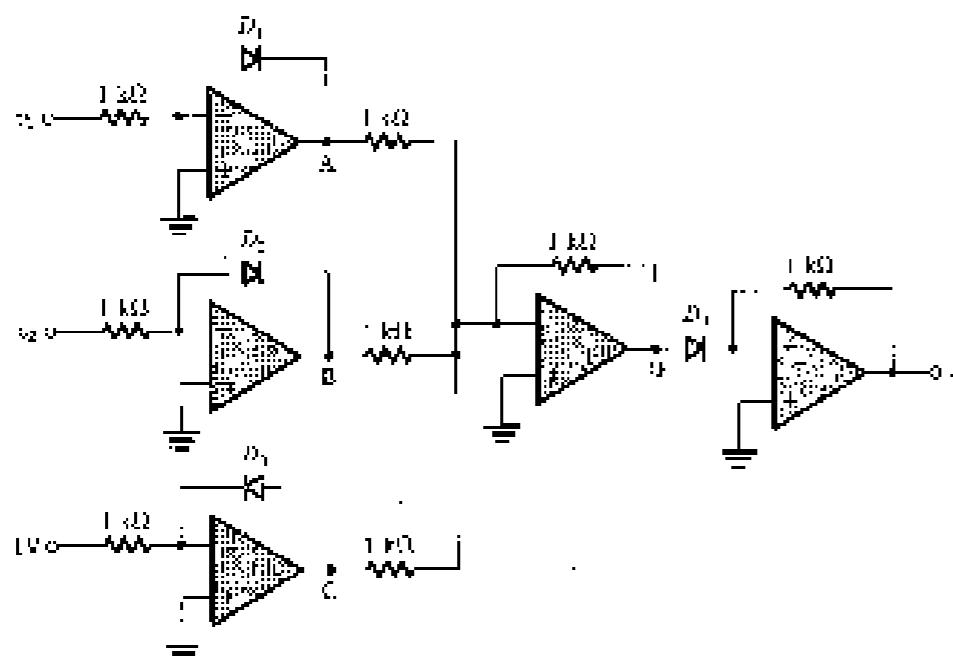


FIGURE P13.44

***P13.45** Preliminary analysis of the circuit in Fig. 13.42 shows that optimum performance (i.e., no shaping errors) when the values of R and R_1 are selected so that $R_1 = 2.5R$, where V_T is the thermal voltage, and the peak amplitude of the input triangular wave is 5.6 V. If the output is taken across R (v_0), between the two emitters, find v_0 corresponding to $v_1 = 0.25V_T$, 0.5V_T, 1.5V_T, 2V_T, 3.4V_T, and 2.42V_T. Plot v_0 , v_1 and current i_1 in the first emitter given by

$$i_1 = 0.42 V_1 \sin \left(\frac{\pi v_1}{6.6 V_T} \times 90^\circ \right).$$

SECTION 13.9: PRECISION RECTIFIER CIRCUITS

P13.46 Two simple diode circuits connected to a common load resistor and taking the same input signal have their diodes reversed, one with cathode to the load, the other with anode to the load. For a sine-wave input of 10-V peak-to-peak, what is the output waveform? Note that lower half cycle of the load current is provided by a separate amplifier, and that while one amplifier supplies the load current, the other amplifies it. This idea, called class B operation (see Chapter 14), is important in the implementation of power amplifiers.

P13.47 The superdiode circuit of Fig. 13.20(a) can be made to have gain by connecting a resistor R_{12} in place of the short circuit between the cathode of the diode and the negative input terminal of the inverter, and a resistor R_{13} between the negative input terminal and ground. Design the circuit for a gain of 2. For a 10-V peak-to-peak input sine wave, what is the average output voltage resulting?

P13.48 Provide a design of the in-circuit precision rectifier shown in Fig. 13.4-(a) in which the gain is +2 for negative inputs and +1 otherwise, and the input resistance is 100 kΩ. What values of R_1 and R_2 do you choose?

***P13.49** Provide a design for a voltmeter circuit similar to the one in Fig. 13.25, which is intended to function at frequencies of 1 KHz and above. It should be calibrated for sine-wave input signals to provide an output of 10 V for an input of 1 V rms. The input resistance should be as high as possible. To extend the bandwidth of operation, keep the gain in the in-circuit of the circuit reasonably small. As well, the design should result in reduction of the size of the capacitor C required. The largest value of resistor may safely be 1 MΩ.

P13.50 Plot the transfer characteristic of the circuit in Fig. P13.50.

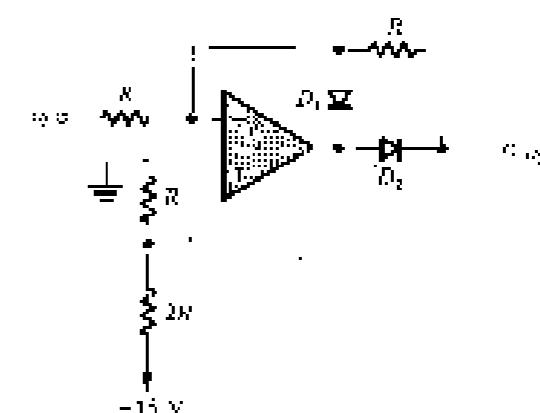


FIGURE P13.50

P13.51 Plot the transfer characteristics of $v_{01}-v_1$ and $v_{02}-v_2$ of the circuit in Fig. P13.51.

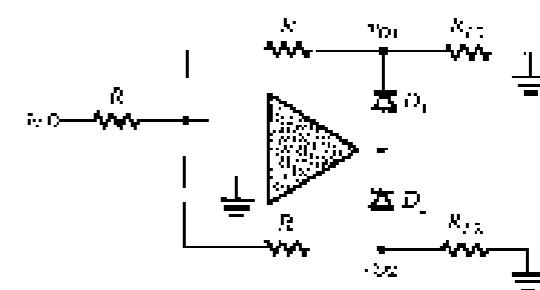


FIGURE P13.51

P13.52 Sketch the transfer characteristics of the circuit in Fig. P13.52.

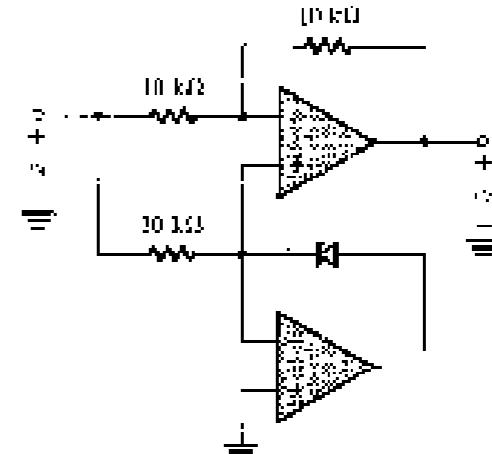


FIGURE P13.52

P13.53 A circuit related to that in Fig. 13.48 is to be used to generate a current proportional to v_2/v_3 ($v_2 \geq 0$) to a light-emitting diode (LED). The value of the current is to be independent of the LED's machine rating and variability. Suggest how this may be done easily.

P13.54 In the precision oscillator of Fig. 13.38, the resistor R is bypassed by a capacitor C . What happens? For equivalent performance with a sine-wave input of 60 Hz frequency with $R = 1\text{ k}\Omega$, what value of C is ideal? What is the response of the modified circuit at 120 Hz? At 100 Hz? If the amplitude of v_3 is kept fixed with new frequencies, does this circuit perform? Now consider the effect of a waveform change on both streams (the one with R and the one with C). For a triangular-wave input of 60 Hz frequency that produces an average power current of 1 mA in the circuit with R , what does the average wave current

become when R is replaced with no C (whose value was just calculated)?

P13.55 A positive peak voltage in living a fast rise and fall junction diode in a superdiode configuration, with a 10 μF capacitor initially uncharged, is driven by a series of 10-V pulses of 0.1 μs duration. If the maximum output voltage that the supply can supply is 10 mA, what is the charge on the capacitor following one pulse? Two pulses? Ten pulses? How many pulses are required to reach 0.5 V? 1.0 V? 2.0 V?

P13.56 Consider the C_{av} -buffered precision wave oscillator shown in Fig. 13.47 when connected to a triangular input of 1-V peak-to-peak amplitude and 1000 Hz frequency. It requires a load current whose bias current (directed into A_2) is 10 mA and drives a source whose reverse leakage current is 1 nA. What is the smallest capacitor that can be used to guarantee an output voltage less than 1%?

CHAPTER 14

Output Stages and Power Amplifiers

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INTRODUCTION

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. Since the output stage is the final stage of the amplifier, it usually deals with relatively large signals. Thus the small-signal approximations and models either are not applicable or must be used with care. Nevertheless, linearity remains a very important requirement. In fact, a measure of goodness of the design of the output stage is the total harmonic distortion (THD) it introduces. This is the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental. A high-fidelity audio power amplifier features a THD of the order of a fraction of a percent.

The most challenging requirement in the design of the output stage is that it deliver the required amount of power to the load in an efficient manner. This implies that the power dissipated in the output-stage transistors must be as low as possible. This requirement stems mainly from the fact that the power dissipated in a transistor raises its internal junction temperature, and there is a maximum temperature (in the range of 150°C to 200°C for silicon).

device above which the transistor is destroyed. A high power-conversion efficiency also may be required to prolong the life of batteries employed in battery-powered circuits, to permit a smaller, lower-cost power supply, or to obviate the need for cooling fans.

We begin this chapter with a study of the various output stage configurations currently in use that handle both low and high power. In this context, "high power" generally means greater than 1 W. We then consider the specific requirements of BJTs catalogued in the design of high-power output stages, called power transistors. Special attention will be paid to the thermal properties of such transistors.

A power amplifier is simply an amplifier with a high-power output stage. Examples of discrete- and integrated-circuit power amplifiers will be presented. Also included is a brief discussion of MOSFET structures that are currently finding application in power-circuit design. The chapter concludes with an example illustrating the use of SPICE simulation in the analysis and design of output stages.

14.1 CLASSIFICATION OF OUTPUT STAGES

Output stages are classified according to the collector current waveform that results when an input signal is applied. Figure 14.1 illustrates the classification for the case of a sinusoidal input signal. The class A stage, whose associated waveform is shown in Fig. 14.1(a), is biased at a current I_c greater than the amplitude of the signal current, i_s . Thus the transistor is a class A stage conduct for the entire cycle of the input signal; that is, the conduction angle is 360° . In contrast, the class B stage, whose associated waveform is shown in Fig. 14.1(b), is biased at zero dc current. Thus a transistor in a class B stage conducts for only half the cycle of the input sine wave, resulting in a conduction angle of 180° . As will be seen later, the negative halves of the sinusoid will be supplied by another transistor that also operates in the class B mode and conducts during the alternate half-cycles.

An intermediate mode between A and B, appropriately termed class AB, involves biasing the transistor at a nonzero dc current much smaller than the peak current of the sine-wave signal. As a result, the transistor conducts for an interval slightly greater than half a cycle, as illustrated in Fig. 14.1(c). The resulting conduction angle is greater than 180° but much less than 360° . The class AB stage has another transistor that conducts for an interval slightly greater than that of the negative half-cycle, and the currents from the two transistors are combined in the load. It follows that during the intervals near the zero crossings of the input sinusoid, both transistors conduct.

Figure 14.1(d) shows the collector-current waveform for a transistor operated as a class C amplifier. Observe that the transistor conducts for an interval shorter than that of a half-cycle; that is, the conduction angle is less than 180° . The result is the periodically pulsating current waveform shown. To obtain a sinusoidal output voltage, this current is passed through a parallel LC circuit tuned to the frequency of the input sinusoid. The tuned circuit acts as a bandpass filter and provides an output voltage proportional to the amplitude of the fundamental component in the Fourier series representation of the current waveform.

Class A, AB, and C amplifiers are studied in this chapter. They are employed as output stages of operational and audio-power amplifiers. In the latter application, class AB is the preferred choice, for reasons that will be explained in the following sections. Class C amplifiers are usually employed for radio-frequency (RF) power amplifiers required, e.g., in microwave phoners and audio and TV transmitters. The design of class C amplifiers is a matter specialized region and is not included in this book.

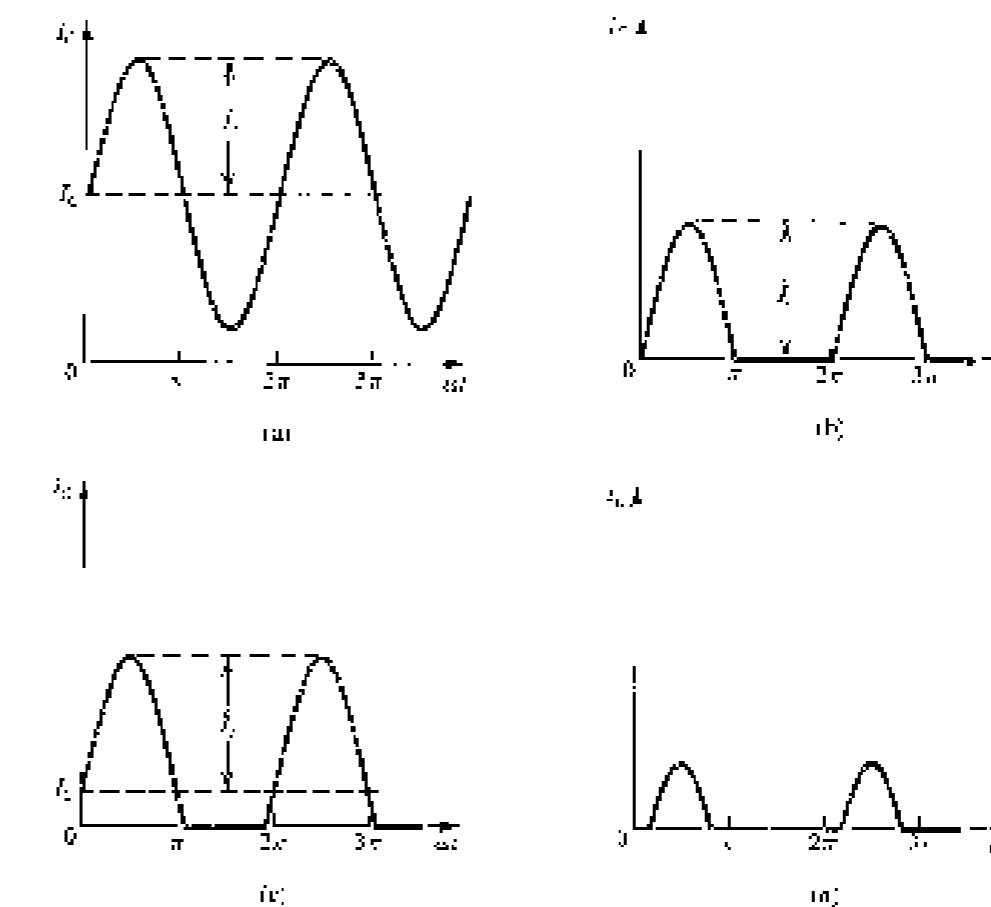


FIGURE 14.1 Collector-current waveforms for (a) class A, (b) class B, (c) class AB, and (d) class C output stages.

Although the BJT has been used to illustrate the definition of the various output stage classes, the same classification applies to output stages implemented with MOSFETs. Furthermore, the classification above extends to output stages other than those used at the output. In this regard, all the common-emitter, common-base, and common-collector amplifiers (and their FET counterparts) studied in earlier chapters fall into the class A category.

14.2 CLASS A OUTPUT STAGE

Because of its low output resistance, the emitter follower is the most popular class A output stage. We have already studied the emitter follower in Chapters 5 and 6; in the following we consider its large-signal operation.

14.2.1 Transfer Characteristic

Figure 14.2 shows an emitter follower \bar{Q}_1 biased with a constant current I supplied by transistor \bar{Q}_2 . Since the emitter current $i_E = I + i_B$, the bias current I must be greater than the

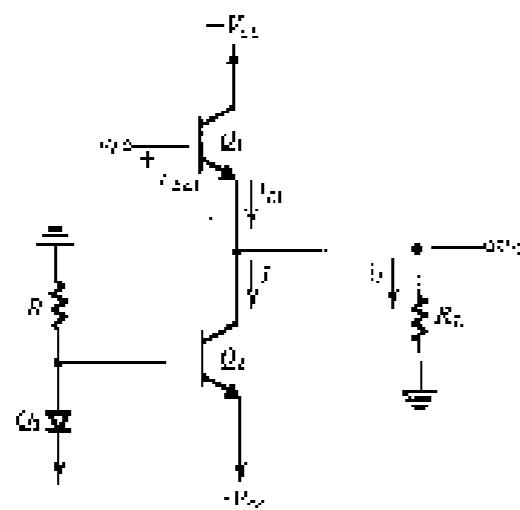


FIGURE 14.2 An emitter follower (Q2) biased with a constant current supplied by transistor Q1.

largest negative load current; otherwise, Q_2 cuts off and class A operation will no longer be maintained.

The transfer characteristic of the emitter follower of Fig. 14.2 is described by

$$v_{out} = v_{in} - v_{BEQ2} \quad (14.1)$$

where v_{BEQ2} depends on the emitter current i_{E1} and thus on the load current i_L . If we neglect the relatively small changes in v_{BE} (60 mV for every factor-of-10 change in emitter current), the linear transfer curve shown in Fig. 14.3 results. As indicated, the positive limit of the linear region is determined by the saturation of Q_1 ; that

$$v_{out\max} = V_{CC} - V_{BEQ2} \quad (14.2)$$

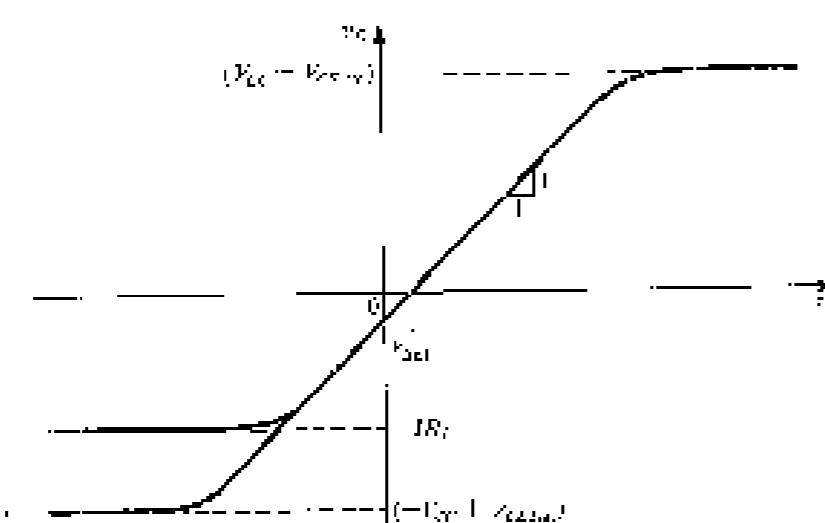


FIGURE 14.3 Transfer characteristic of the emitter follower in Fig. 14.2. This linear characteristic is obtained by neglecting the change in v_{BE} with i_L . The maximum positive output is determined by the value of Q_1 . In the negative direction, the slope of the linear region is determined either by Q_1 (if $i_E > I_BQ1$) or by Q_2 , depending on the values of β and R_L .

In the negative direction, depending on the values of β and R_L , the limit of the linear region is determined either by Q_1 turning off,

$$v_{out\min} = -V_{BEQ2} \quad (14.3)$$

or by Q_2 saturating,

$$v_{out\min} = -V_{BEQ2} + V_{satQ2} \quad (14.4)$$

The absolutely lowest output voltage is also given by Eq. (14.4) if and is achieved provided the bias current I is greater than the magnitude of the corresponding load current.

$$I > \frac{|-V_{BEQ2} + V_{satQ2}|}{R_L} \quad (14.5)$$

EXERCISES

- 14.1. The circuit of Fig. 14.2 has $V_{CC} = 12$ V, $R_L = 1000 \Omega$, $R_F = 1000 \Omega$, $R_B = 100 \Omega$, $\beta = 100$, $V_{BEQ2} = 0.7$ V, and $V_{satQ2} = 0.2$ V. If the quiescent value of i_L is 1 mA, determine the resulting output signal voltage, output current, and the instantaneous collector currents.

Ans.: $v_{out} = 11.3$ V, $i_L = 1.002$ mA, $i_{C1} = 1.002$ mA, $i_{C2} = 0.002$ mA

- 14.2. For the circuit shown in Fig. 14.2, consider the case in which the load resistance is $R_L = 100 \Omega$ and $V_{CC} = 12$ V. If $V_{BEQ2} = 0.7$ V and $V_{satQ2} = 0.2$ V, find the quiescent value of i_L and the corresponding i_{C1} and i_{C2} . Note that the dependent source guarantees that along the linear portion of the characteristic, $i_{C1} = i_{C2}$.

Ans.: $i_L = 0.6$ mA, $i_{C1} = 0.598$ mA, $i_{C2} = 0.002$ mA

14.2.2 Signal Waveforms

Consider the operation of the emitter-follower circuit of Fig. 14.2 for sine-wave input. Neglecting V_{BEQ2} ; or see Ex. 14.1 if the bias current I is properly selected, the output voltage can swing from $-V_{BEQ2}$ to $|V_{CC}|$ with the quiescent value being zero, as shown in Fig. 14.4(a). Figure 14.4(b) shows the corresponding waveform of $v_{BEQ2} = V_{CC} - v_{out}$. Now, assuming that the bias current I is selected to allow a maximum negative load current of V_{CC}/R_L , the collector current of Q_1 will have the waveform shown in Fig. 14.4(c). Finally, Fig. 14.4(d) shows the waveform of the instantaneous power dissipation in Q_1 .

$$P_D = v_{out} i_{C1} \quad (14.6)$$

14.2.3 Power Dissipation

Figure 14.4(d) indicates that the maximum instantaneous power dissipation in Q_1 is $V_{CC} I$. This is equal to the quiescent power dissipation in Q_1 . Thus the emitter-follower dissipates the largest amount of power when $v_{in} = 0$. Since this condition can easily prevail for prolonged periods of time, transistor Q_1 must be able to withstand a continuous power dissipation of $V_{CC} I$.

The power dissipation in Q_1 depends on the value of R_L . Consider the extreme case of an output open circuit, that is, $R_L \rightarrow \infty$. In this case, $i_{C1} \rightarrow I$ is constant and the instantaneous power dissipation in Q_1 will depend on the instantaneous value of v_{in} . The maximum power dissipation will occur when $v_{in} = V_{CC}$, for in this case v_{out} is a maximum of $|V_{CC}|$, and $i_{C1} = 2V_{CC}/R_L$. This condition, however, would not normally persist for a prolonged interval, so the

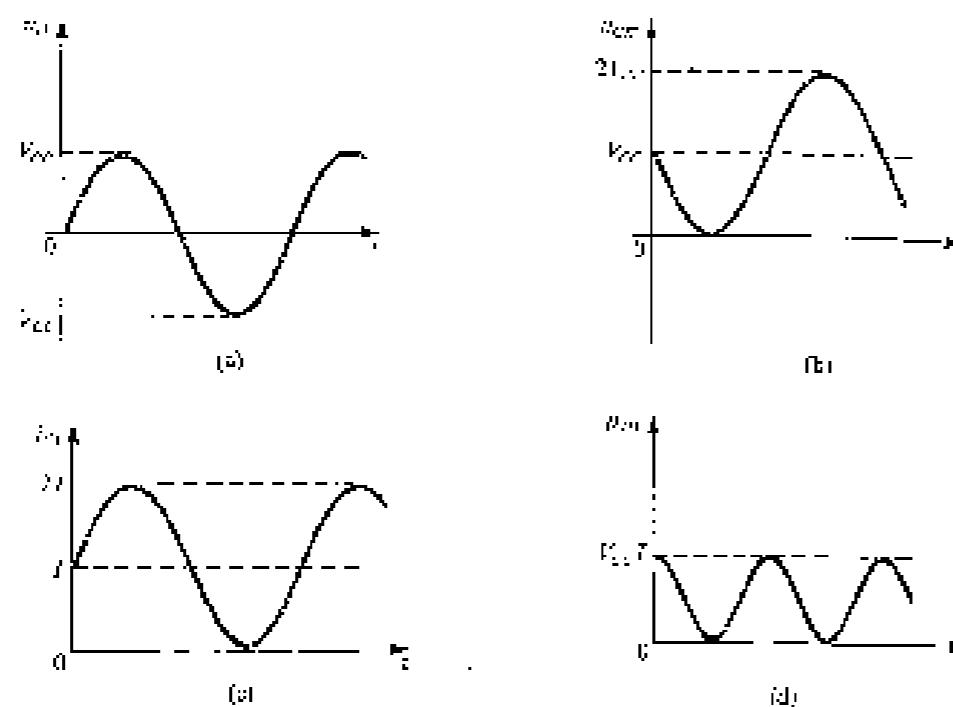


FIGURE 14.4 Maximum signed waveform in the class A output stage of Fig. 14.2 under the condition $i = V_{DD}/R_2$, or equivalently, $R_2 = V_{DD}/I_2$.

design need not be that conservative. Observe that with an open-circuit load the average power dissipation in Q_1 is $V_{DD}I_1$. A far more dangerous situation occurs at the other extreme of R_L ,—specifically, $R_L = 0$. In the event of an output short circuit, a positive drain voltage would then readily result in an infinite drain current. In practice, a very large current may flow through Q_1 , and if the short-circuit condition persists, the resulting large power dissipation in Q_1 can raise its junction temperature beyond the specified maximum rating Q_1 to burn up. To guard against such a situation, output stages are usually equipped with short-circuit protection, as will be explained later.

The power dissipation in Q_1 also must be taken into account in designing an inverter follower output stage. Since Q_1 conducts a constant current I , and the maximum value of V_{CE} is $2V_{CC}$, the maximum instantaneous power dissipation in Q_1 is $2V_{CC}I$. This maximum, however, occurs when $v_L = V_{CC}$, a condition that we did not normally prevail for a prolonged period of time. A more significant quantity for design purposes is the average power dissipation in Q_1 , which is $V_{CC}I$.

EXERCISE

184. *Coniopteryx tibialis* (Herrich-Schäffer) (Fig. 12). Length 60-65 mm. - 185. *Proctotrupes* sp. (Fig. 13). Length 10-12 mm. - 186. *Proctotrupes* sp. (Fig. 14). Length 10-12 mm. - 187. *Proctotrupes* sp. (Fig. 15). Length 10-12 mm. - 188. *Proctotrupes* sp. (Fig. 16). Length 10-12 mm. - 189. *Proctotrupes* sp. (Fig. 17). Length 10-12 mm.

14.2.4 Power-Conversion Efficiency

The power spectrum of an output signal is defined as

$$\eta = \frac{\text{Lead power } (P_1)}{\text{Sample power } (P_s)} \quad (4.7)$$

See the emitter load power of Fig. 14.2, assuming that the output voltage is a sineoid with the peak value V_{pk} , the average load power will be

$$P_L \sim \frac{\langle \hat{N}_L \rangle \langle \hat{N}_R \rangle}{\langle \hat{N} \rangle^2} = \frac{1}{2} \theta_L \quad (12.3)$$

Since the current in ψ_2 is constant, i_2 , the power drawn from the negative supply is $V_{2d} i_2$. The average current in ψ_1 is equal to i_1 , and thus the average power drawn from the positive supply is $V_{1d} i_1$. Thus the total average supply power is

$$E_2 = 2 E_{\text{eff}} I \quad (12.9)$$

Equations (14.8) and (14.9) can be combined to yield

$$\eta = \frac{1}{4} \frac{\dot{V}^2}{B_0 V_{c,r}^2} - \frac{1}{2} \left(\frac{\dot{V}_r}{B_0 V_{c,r}} + \frac{\dot{V}_{\perp r}}{V_{c,r}} \right)^2 \quad (4.10)$$

Since $\ell_1 \leq \ell_2$, and $\ell_2 \leq \ell_K$, matching efficiency is obtained when

$$V_0 = V_{\infty} = \{X_0\} \quad (24.1)$$

The maximum efficiency achievable is 20%. Because this is a rather low figure, the class A output voltage is rarely used in high-power applications (>1 W). Note also that in practice the output voltage swing is limited to lower values to avoid transistor saturation and associated switching distortion. Thus far efficiency increases sharply in the 10% to 20% range.

第10章

With the exception of the first two, the remaining four were all obtained from the same source, and it is likely that they are all derived from the same original material.

لیونز چاپ و منتشر کنند
و این روزهای بسیار خوب است

14.3 CLASS B OUTPUT STAGE

Figure 14.5 shows a class A output stage. It consists of a complementary pair of transistors (T_1 and T_2) connected in such a way that both cannot conduct simultaneously.

¹ This case was heard by the commissioners by Mr. H. J. Wilson of and the successor-Commissioner.

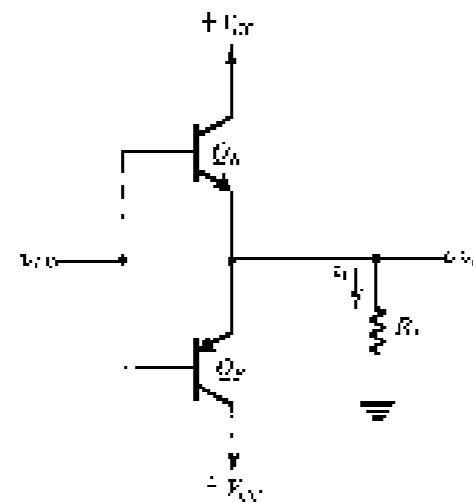


FIGURE 14.5 A class B output stage.

14.3.1 Circuit Operation

When the input voltage v_i is zero, both transistors are cut off and the output voltage v_o is zero. As v_i goes positive and exceeds about 0.5 V, Q_1 conducts and operates as an emitter follower. In this case v_o follows v_i (i.e., $v_o = v_i - v_{BE1}$) and Q_2 supplies the load current. Meanwhile, the emitter-base junction of Q_2 will be reverse-biased by the V_{BE1} of Q_1 , which is approximately 0.7 V. Thus Q_2 will be cut off.

If the input goes negative by more than about 0.5 V, Q_2 turns on and acts as an emitter follower. Again v_o follows v_i (i.e., $v_o = v_i - v_{BE2}$), but in this case Q_1 supplies the load current and Q_2 will be cut off.

We conclude that the transistors in the class B stage of Fig. 14.5 are biased at zero current and conduct only when the input signal is present. The circuit operates in a **push-pull** fashion: Q_1 provides (sources) current to the load when v_i is positive and Q_2 pulls (drains) current from the load when v_i is negative.

14.3.2 Transfer Characteristic

A sketch of the transfer characteristic of the class B stage is shown in Fig. 14.6. Note that there exists a range of v_i centered around zero where both transistors are cut off and v_o is zero. This dead band results in the crossover distortion illustrated in Fig. 14.7 for the case of an input sine wave. The effect of crossover distortion will be most pronounced when the amplitude of the input signal is small. Crossover distortion in radio power amplifiers gives rise to unpleasant sounds.

14.3.3 Power-Conversion Efficiency

To calculate the power-conversion efficiency, η , of the class B stage, we neglect the crossover distortion and consider the case of an output sinusoid of peak amplitude \hat{v}_o . The average load power will be

$$P_L = \frac{1}{2} \frac{\hat{v}_o^2}{R_L} \quad (14.12)$$

The current drawn from each supply will consist of half-sine waves of peak amplitude (\hat{v}_o / R_L) . Thus the average current drawn from each of the two power supplies will be

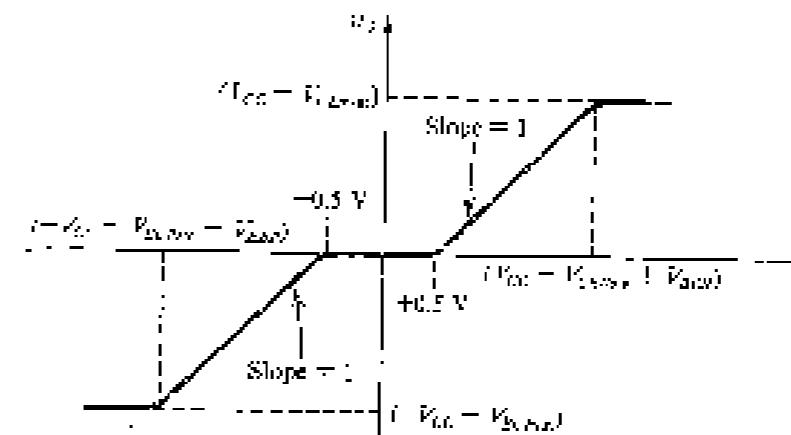


FIGURE 14.6 Transfer characteristic for the class B output stage in Fig. 14.5.

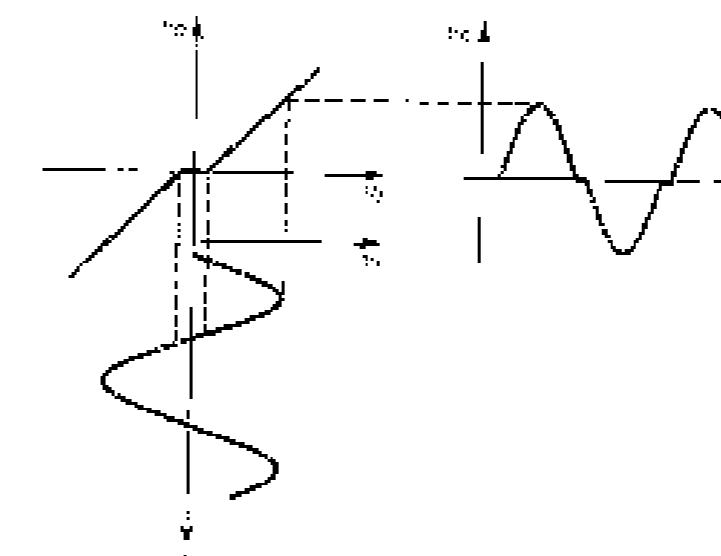


FIGURE 14.7 It is striking how the dead band in the class B transfer characteristic results in crossover distortion.

\hat{v}_o / R_L . It follows that the average power drawn from each of the two power supplies will be the same:

$$P_{L1} = P_{L2} = \frac{1}{2} \frac{\hat{v}_o^2}{R_L} V_{DD} \quad (14.13)$$

and the total supply power will be

$$P_T = \frac{2}{\pi} \frac{\hat{v}_o}{R_L} V_{DD} \quad (14.14)$$

Thus the efficiency will be given by

$$\eta = \frac{P_D}{V_2 R_L / \pi R_L} = \frac{\pi V_2^2}{2 R_L} \quad (14.15)$$

It follows that the maximum efficiency is obtained when V_2 is at its maximum. This maximum is limited by the saturation of Q_2 and Q_1 at $V_{ce} = V_{max} = V_{cc}$. At this value of peak output voltage, the power conversion efficiency is

$$\eta_{max} = \frac{\pi}{2} = 78.5\% \quad (14.16)$$

This value is much larger than that obtained in the class A stage (25%). Finally, we note that the maximum average power available from a class B output stage is obtained by substituting $C_o = V_{cc}$ in Eq. (14.12),

$$P_{Dmax} = \frac{1}{2} \frac{V_2^2}{R_L} \quad (14.17)$$

14.3.4 Power Dissipation

Unlike the class A stage, which dissipates maximum power under quiescent conditions ($i_o = 0$), the quiescent power dissipation of the class B stage is zero. When an input signal is applied, the average power dissipated in the class B stage is given by

$$P_A = P_D - P_1 \quad (14.18)$$

Substituting for P_1 from Eq. (4.14) and for P_D from Eq. (14.17) results in

$$P_A = \frac{2}{\pi} \frac{V_2^2}{R_L} V_{ce} - \frac{1}{2} \frac{V_2^2}{R_L} \quad (14.19)$$

From symmetry we see that half of P_A is dissipated in Q_2 , and the other half in Q_1 . Thus Q_2 and Q_1 are capable of safely dissipating $\frac{1}{2} P_A$ watts. Since P_A depends on V_{ce} , we must find the worst-case power dissipation, P_{Dmax} . Differentiating Eq. (14.18) with respect to V_{ce} and equating the derivative to zero gives the value of V_{ce} that results in maximum average power dissipation as

$$V_{ce,max} = \frac{2}{\pi} V_{cc} \quad (14.20)$$

Substituting this value in Eq. (14.19) gives

$$P_{Dmax} = \frac{2}{\pi} \frac{V_2^2}{R_L} \quad (14.21)$$

Thus,

$$P_{Dmax} = P_{1max} = \frac{V_2^2}{\pi R_L} \quad (14.22)$$

At the point of maximum power dissipation the efficiency can be evaluated by substituting for V_{ce} from Eq. (14.20) into Eq. (14.15); hence, $\eta = 50\%$.

Figure 14.8 shows a sketch of P_D (Eq. 14.10) versus the peak output voltage V_{ce} . Curves such as this are usually given on the data sheets of IC power amplifiers. (Usually, however, P_D is plotted versus P_{cc} , as $P_D = \frac{1}{2}(V_2^2/R_L)$, rather than V_{ce} .) An interesting observation follows from Fig. 14.8: Increasing R_L beyond $2V_{cc}/\pi$ decreases the power dissipated in the class B

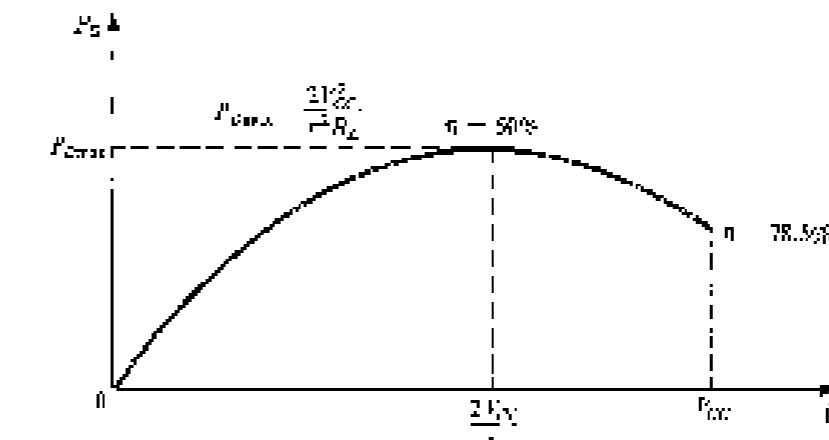


FIGURE 14.8 Power dissipation of a class B output stage versus amplitude of the output sinusoid.

stage while increasing the total power. The price paid is an increase in nonlinear distortion as a result of approaching the saturation region of operation of Q_2 and Q_1 . Transistor saturation occurs at the peaks of the output sine waveform. Unfortunately, this type of distortion cannot be significantly reduced by the application of negative feedback (see Section 14.2), and thus transistor saturation should be avoided in applications requiring low THD.

PROBLEMS

It is required to design a class B output stage to deliver an average power of 20 W to an 8-Ω load. The power supply is to be selected such that V_{cc} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including circuit protection circuitry. (The latter will be discussed in Section 14.7.) Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

Solution

Since

$$P_D = \frac{1}{2} \frac{V_2^2}{R_L}$$

then

$$\begin{aligned} V_2 &= \sqrt{2} P_{cc} R_L \\ &= \sqrt{2} \times 20 \times 8 = 17.9 \text{ V} \end{aligned}$$

Therefore we select $V_{cc} = 21 \text{ V}$.

The peak current drawn from each supply is

$$I_2 = \frac{V_2}{R_L} = \frac{17.9}{8} = 2.24 \text{ A}$$

The average power drawn from each supply is

$$P_{Q_1} = P_{Q_2} = \frac{1}{2} \times 1.24 \times 22 = 10.4 \text{ W}$$

From total supply power of 20.8 W, the power conversion efficiency is

$$\eta = \frac{P_t}{P_s} = \frac{20.8}{42.8} \times 100 = 48\%$$

The maximum power dissipated in each transistor is given by Eq. (14.29); thus

$$\begin{aligned} P_{Q_{\text{max}}} = P_{Q_{\text{diss}}} &= \frac{V_{CE}^2}{\pi^2 R_L} \\ &= \frac{(12.1)^2}{\pi^2 \times 6} = 0.7 \text{ W} \end{aligned}$$

14.3.5 Reducing Crossover Distortion

The crossover distortion of a class B output stage can be reduced substantially by employing a high-gain op amp and overall negative feedback, as shown in Fig. 14.9. The 10-V ideal bias is reduced to $10/2A_v$ volts, where A_v is the dc gain of the op amp. Nevertheless, the slew rate limitation of the op amp will cause the adverse turning-on and off of the output transistors to be noticeable, especially at high frequencies. A more practical method for reducing and almost eliminating crossover distortion is found in the class AB stage, which will be studied in the next section.

14.3.6 Single-Supply Operation

The class B stage can be oriented from a single power supply, in which case the load is capacitively coupled, as shown in Fig. 14.10. Note that to make the formulas derived in Section 14.3.4 directly applicable, the single power supply is denoted $2V_{CC}$.

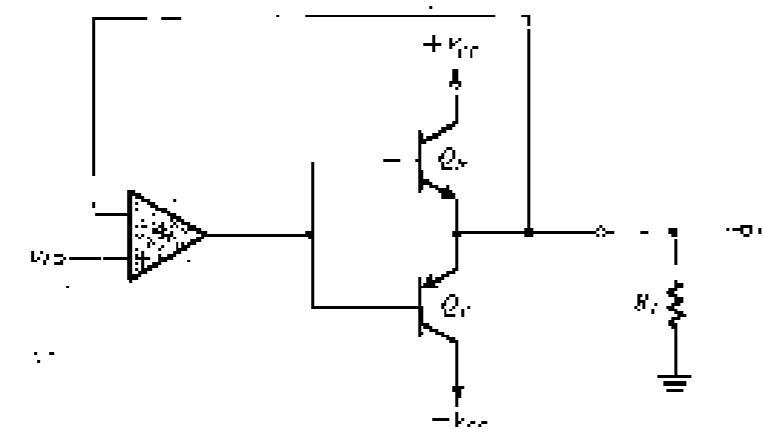


FIGURE 14.9 Class B circuit with an op amp connected in a negative feedback loop to reduce crossover distortion.

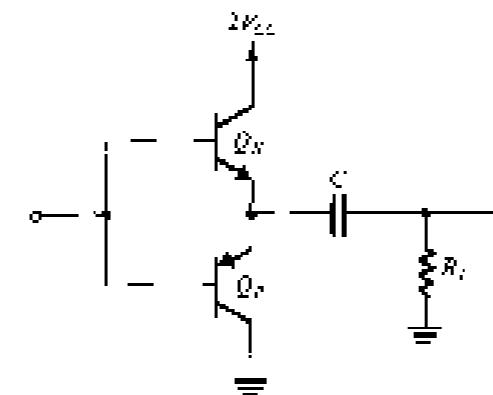


FIGURE 14.10 Class B output stage operated with a single power supply.

14.4 CLASS AB OUTPUT STAGE

Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small collector current. The result is the class AB output stage shown in Fig. 14.11. A bias voltage V_{BB} is applied between the bases of Q_1 and Q_2 . The $v_i = 0$, $v_o = 0$, and a voltage $V_{BE}/2$ appears across the base-emitter junction of each of Q_1 and Q_2 . Assuming

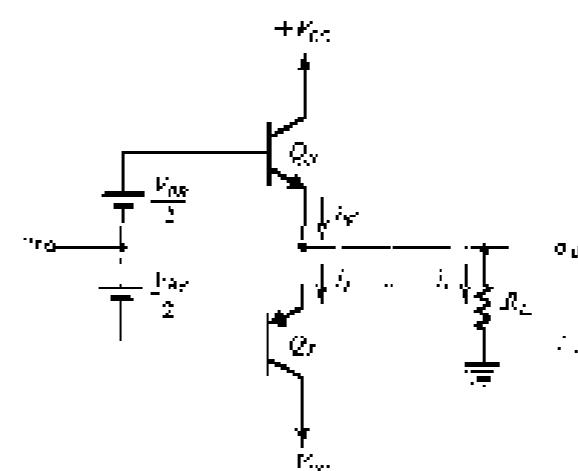


FIGURE 14.11 Class AB output stage. A bias voltage, V_{BB} , is applied between the bases of Q_1 and Q_2 , giving rise to a bias current I_B , given by eq. (14.21). Thus, for small v_i , no crossover distortion and crossover distortion is almost completely eliminated.

related devices.

$$i_2 = i_T + I_2 = I_{Q2} e^{\frac{V_{BE2}}{V_T}} \quad (14.21)$$

The value of V_{BE} is selected to yield the required quiescent current i_Q .

14.4.1 Circuit Operation

When v_i goes positive by a certain amount, the voltage at the base of Q_2 increases by the same amount and the output becomes positive at an altered equal value.

$$v_o = v_i + \frac{R_{L2}}{2} = v_{oQ} \quad (14.22)$$

The positive v_i causes a current i_2 to flow through R_{L2} and base b_2 to rise (increase); that is,

$$i_2 = i_T + i_2 \quad (14.23)$$

The increase in i_2 will be accompanied by a corresponding increase in v_{BE2} (above the quiescent value of $V_{BE}/2$). However, since the voltage between the two bases remains constant at V_{BE} , the increase in v_{BE2} will result in an equal decrease in v_{BE1} and hence in i_1 . The relationship between v_i and i_1 can be derived as follows:

$$\begin{aligned} v_{BE1} - v_{BE2} &= V_{BE} \\ V_T \ln \frac{i_1}{I_{Q1}} + V_T \ln \frac{i_2}{I_{Q2}} &= 2V_T \ln \frac{i_1}{I_{Q1}} \\ i_1 i_2 &= I_{Q1} I_{Q2} \end{aligned} \quad (14.24)$$

Thus, as i_2 increases, i_1 decreases by the same ratio while the product remains constant. Equations (14.23) and (14.24) can be combined to yield i_1 for a given i_2 as the solution to the quadratic equation

$$i_1^2 - i_1 i_2 - i_2 = 0 \quad (14.25)$$

From the equations above, we can see that for positive output voltages, the load current is supplied by Q_{2N} which acts as the output emitter follower. Meanwhile, Q_1 will be conducting a current that decreases as v_i increases; for large v_i , the current in Q_1 can be ignored altogether.

For negative input voltages the opposite occurs. The load current will be supplied by Q_1 which acts as the output emitter follower; while Q_{2N} conducts a current that gets smaller as v_i becomes more negative. Equation (14.25), relating i_1 and i_2 , holds for negative inputs as well.

We conclude that the class AB stage operates in much the same manner as the class B circuit, with one important exception: For small v_i , both transistors conduct, and as v_i is increased or decreased, one of the two transistors takes over the operation. Since the transistor is a current-controlled device, crossover distortion will be almost totally eliminated. Figure 14.12 shows the transfer characteristic of the class AB stage.

The power relationships in the class AB stage are almost identical to those derived for the class B circuit in Section 14.2. The only difference is that under quiescent conditions the class AB circuit dissipates a power of $V_{BE} I_Q$ per transistor. Since I_Q is usually much smaller than the peak load current, the quiescent power dissipation is usually small. Nevertheless, it can be taken into account easily. Specifically, we can simply add the quiescent designation to the transistor to its maximum power dissipation with no input signal applied, to obtain the total power dissipation that the transistor must be able to handle safely.

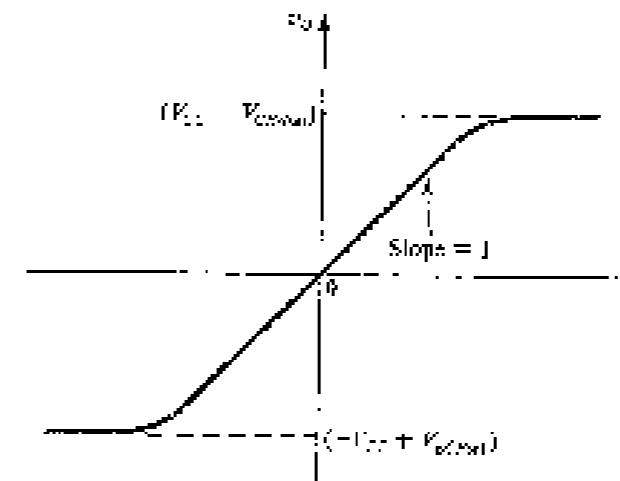


FIGURE 14.12 Transfer characteristic of the class AB stage in Fig. 14.11.

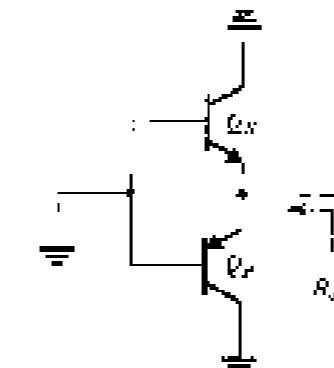


FIGURE 14.13 Determining the small-signal output resistance of the class AB circuit of Fig. 14.11.

14.4.2 Output Resistance

If we assume that the source supplying v_i is ideal, then the output resistance of the class AB stage can be determined from the circuit in Fig. 14.13 as

$$R_{out} = r_{e1} || r_{e2} \quad (14.26)$$

where r_{e1} and r_{e2} are the small-signal emitter resistances of Q_1 and Q_{2N} , respectively. At a given input voltage, the currents i_1 and i_2 can be determined, and r_{e1} and r_{e2} are given by

$$r_{e1} = \frac{V_T}{I_{Q1}} \quad (14.27)$$

$$r_{e2} = \frac{V_T}{I_{Q2}} \quad (14.28)$$

$$R_{out} = \frac{V_T}{I_{Q1}} \left| \frac{V_T}{I_{Q1}} + \frac{V_T}{I_1 - I_2} \right| \quad (14.29)$$

Since as i_b increases, i_p decreases, and vice versa, the output resistance remains approximately constant in the region around $i_b = 0$. This, in effect, is the reason for the virtual absence of crossover distortion. At larger load currents, at higher i_b or i_p , will be significant, and R_{out} decreases as the load current increases.

EXERCISE

- 14.4 Consider a class AB circuit with $V_{CC} = 25\text{ V}$, $i_b = 2\text{ mA}$, and $\beta = 100$. Determine the quiescent collector voltage V_{CQ} and the collector-to-emitter voltage V_{CEQ} versus the load current i_L of $0.1\text{ A}, 0.2\text{ A}, 0.5\text{ A}, 1\text{ A}$, and 2 A . Assume $\alpha = 0.95$ and $\beta = 100$. Use the large-signal model and assume $i_b = 0$ for the small-signal equivalent circuit. Plot the load current i_L versus the load voltage V_{OL} and the load resistance R_L .

Ans: $i_L = 0.1664\text{ A}$; $V_{OL} = 19.6\text{ V}$; $R_L = 117.6\text{ }\Omega$

i_L	V_{OL}	R_L
0.1	19.600	196.00
0.2	19.000	95.00
0.5	17.600	35.20
1.0	16.640	16.64
2.0	15.000	7.50
4.0	13.600	3.40
8.0	12.500	1.62
16.0	11.600	0.75
32.0	10.800	0.375
64.0	10.000	0.1875
128.0	9.200	0.09375
256.0	8.400	0.046875
512.0	7.600	0.0234375
1024.0	6.800	0.01171875
2048.0	6.000	0.005859375
4096.0	5.200	0.0029296875
8192.0	4.400	0.00146484375
16384.0	3.600	0.000732421875
32768.0	2.800	0.0003662109375
65536.0	2.000	0.00018310546875
131072.0	1.200	9.15527234375E-05
262144.0	0.400	4.577636171875E-05
524288.0	-0.400	2.2888180859375E-05
1048576.0	-1.200	1.14440904296875E-05
2097152.0	-2.000	5.72204521484375E-06
4194304.0	-3.600	2.861022607421875E-06
8388608.0	-4.400	1.4305113037109375E-06
16777216.0	-5.200	7.152556518554688E-07
33554432.0	-6.000	3.576278259277344E-07
67108864.0	-7.600	1.788139129638672E-07
134217728.0	-8.400	8.94069564819336E-08
268435456.0	-9.200	4.47034782409668E-08
536870912.0	-10.000	2.23517391204834E-08
1073741824.0	-11.200	1.11758695622417E-08
2147483648.0	-12.000	5.58793478112085E-09
4294967296.0	-13.200	2.79396739056042E-09
8589934592.0	-14.000	1.39698369528021E-09
17179869184.0	-15.200	6.98491847640105E-10
34359738368.0	-16.000	3.49245923820052E-10
68719476736.0	-17.200	1.74622961910026E-10
137438953472.0	-18.000	8.73114809550131E-11
274877856944.0	-19.200	4.36557404775065E-11
549755713888.0	-20.000	2.18278702387532E-11
1099511427776.0	-21.200	1.09139351193766E-11
2199022855552.0	-22.000	5.45696755968831E-12
4398045711104.0	-23.200	2.72848377984415E-12
8796091422208.0	-24.000	1.36424188992207E-12
17592182844416.0	-25.200	6.82120944961035E-13
35184365688832.0	-26.000	3.41060472480518E-13
70368731377664.0	-27.200	1.70530236240259E-13
140737462755328.0	-28.000	8.52651181201295E-14
281474925510656.0	-29.200	4.26325590600647E-14
562949851021312.0	-30.000	2.13162795300324E-14
1125899702042624.0	-31.200	1.06581397650162E-14
2251799404085248.0	-32.000	5.32906988250081E-15
4503598808170496.0	-33.200	2.66453494125041E-15
9007197616340992.0	-34.000	1.33226747062521E-15
18014395232681984.0	-35.200	6.66133735312511E-16
36028790465363968.0	-36.000	3.33066867656255E-16
72057580930727936.0	-37.200	1.66533433828127E-16
14411516186145972.0	-38.000	8.32667169140638E-17
28823032372291944.0	-39.200	4.16333584570319E-17
57646064744583888.0	-40.000	2.08166792285159E-17
11529212948916776.0	-41.200	1.04083396142579E-17
23058425897833552.0	-42.000	5.20416980712895E-18
46116851795667104.0	-43.200	2.60208490356447E-18
92233703591334208.0	-44.000	1.30104245178224E-18
184467407182668416.0	-45.200	6.5052122589112E-19
368934814365336832.0	-46.000	3.2526061294556E-19
737869628730673664.0	-47.200	1.6263030647278E-19
147573925746134732.0	-48.000	8.131515323639E-20
295147851492269464.0	-49.200	4.0657576618195E-20
590295702984538928.0	-50.000	2.03287883090975E-20

14.5 BIASING THE CLASS AB CIRCUIT

In this section we discuss two approaches for generating the voltage V_{BE} required for biasing the class AB output stage.

14.5.1 Biasing Using Diodes

Figure 14.14 shows a class AB circuit in which the bias voltage V_{BE} is generated by passing a constant current I_{bias} through a pair of diodes, or diode-connected transistors, D_1 and D_2 . In order to deliver large amounts of power, the output transistors are large-area devices. The biasing diodes, however, need not be large devices, and thus the quiescent collector current I_C established at Q_1 and Q_2 will be $I_C = \alpha I_{bias}$, where α is the ratio β/γ . The collector-to-emitter area of the output devices is the junction area of the biasing diodes. In other words, the sum of the collector currents I_C of the output transistors is α times that of the biasing diodes. Area ratios α are simple to implement in integrated circuits but difficult to realize in discrete-circuit designs.

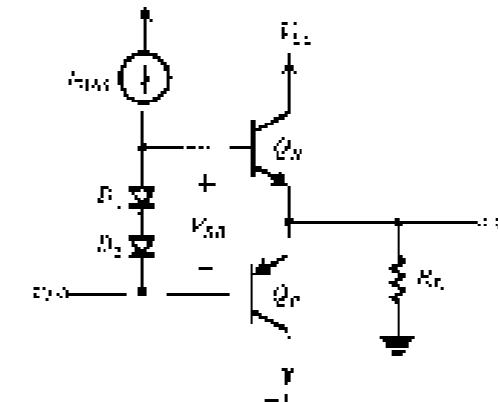


FIGURE 14.14 A class AB output stage utilizing diodes for biasing. The junction areas of the two diodes, D_1 and D_2 , is α times that of the output devices Q_1 and Q_2 , and the quiescent current ($\gamma = 1$) is the same in the output devices.

When the output stage of Fig. 14.14 is sourcing current to the load, the base current of Q_2 increases from $(\gamma/\beta)I_C$ (which is usually small) to approximately I_C/β . The base current must be supplied by the current source I_{bias} . It follows that I_{bias} must be greater than the maximum anticipated base drive for Q_2 . This sets a lower limit on the value of I_{bias} . Now, since $\gamma = \alpha/\beta$ and since I_C is usually much smaller than the peak load current ($<10\%$), we see that we cannot make α a large number. In other words, we cannot make the diodes much smaller than the output devices. This is a disadvantage of the diode biasing scheme.

From the discussion above we see that the current through the biasing diodes will decrease when the output stage is sourcing current to the load. Thus the bias voltage V_{BE} will also decrease, and the analysis of Section 14.4 must be modified to take this effect into account.

The diode biasing arrangement has no important advantages. It can provide thermal stabilization of the quiescent current in the output stage. To appreciate this point recall that the class AB output stage dissipates power under quiescent conditions. Power dissipation raises the internal temperature of the BJTs. From Chapter 3 we know that a rise in transistor temperature results in a decrease in β (approximately $-2\text{ mV}/^\circ\text{C}$) if the collector current is held constant. Alternatively, if V_{BE} is held constant and the temperature increases, the collector current increases. The increase in collector current increases the power dissipation, which in turn increases the collector current. Thus a positive-feedback mechanism exists that can result in a phenomenon called **thermal runaway**. Careless thermal runaway can lead to the ultimate destruction of the BJT. Diode biasing can provide a compensating effect that can protect the output transistors against thermal runaway under quiescent conditions. Specifically, if the diodes are in close thermal contact with the output transistors, their temperature will increase by the same amount as that of Q_1 and Q_2 . Thus V_{BE} will decrease at the same rate as $V_{ESAT} - V_{SSAT}$, with the result that I_C remains constant. Close thermal contact is easily achieved in IC fabrication. It is obtained in discrete circuits by mounting the bias diodes on the metal case of Q_1 or Q_2 .

PROBLEMS

Consider the class AB output stage under the conditions that $V_{CC} = 15\text{ V}$, $R_L = 10\text{ }\Omega$, and the output is sustained with a maximum amplitude of 10 V . Let Q_1 and Q_2 be matched with $I_C = 10\text{ mA}$ and $\beta = 50$. Assume that the biasing diodes have one-tenth the junction area of the output devices. Find the value of I_{bias} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors ($\beta = 50$, $T_0 = 25^\circ\text{C}$). Also find V_{BE} for $i_0 = 0$, -10 V , and $+10\text{ V}$.

Solution

The maximum current through Q_2 is approximately equal to $I_{max} = 4 \text{ V} / 1.422 = 2.82 \text{ mA}$. Thus the maximum base current in Q_1 is approximately 2 mA. To minimize a minimum of 1 mA through the diodes, we select $I_{bias} = 3 \text{ mA}$. The area ratio of 1 yields a quiescent current of 5 mA through Q_1 and Q_2 . The quiescent power dissipation is:

$$P_{\text{tot}} = 2 \times 15 \times 9 = 270 \text{ mW}$$

For $v_0 = 0$, the base current of Q_1 is $10 \times 51 = 0.18 \text{ mA}$, leaving a current of $2 - 0.18 = 1.82 \text{ mA}$ to flow through the diodes. Since the diode bias $I_D = 1 \times 10^{-12} \text{ A}$, the voltage V_{BE} will be

$$V_{03} = 2 V_1 \cdot n^{2.83 \text{ mA}} = 1.26$$

At $v_2 = +10$ V, the current through the diodes will decrease to 1 mA, resulting in $V_{D2} \approx 0.21$ V. At the other extreme of $v_2 = -10$ V, Q₂ will be conducting a very small current; thus, the bias current will be negligibly small and all of $I_{T-BS} (3$ mA) flows through the diodes, resulting in $V_{D2} \approx 1.26$ V.

EXERCISES

14.5.2 Biasing Using the V_{SE} Multiplier

An alternative biasing arrangement that provides the designer with considerably more flexibility in both discrete and integrated designs is shown in Fig. 14.15. The bias circuit consists of transistor Q_1 with a resistor R_1 connected between base and emitter and a feedback resistor R_2 connected between collector and base. The resulting two-terminal network is fed with a constant-current source I_{bias} . If we neglect the base current of Q_1 , then R_1 and R_2 will carry the same current I_b , given by

$$f_A = \frac{r_{ext}}{\delta_0} \quad (14.3)$$

and the voltage V_{be} across the bias network will be

$$V_{\text{eff}} = T_h(R_1 - R_2) \quad (14.33)$$

Thus the credit supply multiplies V_{adv} by the factor $(1 + R_E/R_C)$ and is known as the "V_{cr} multiplier". The firm's output in practice is thus mostly ranked for designer's credits, and can be

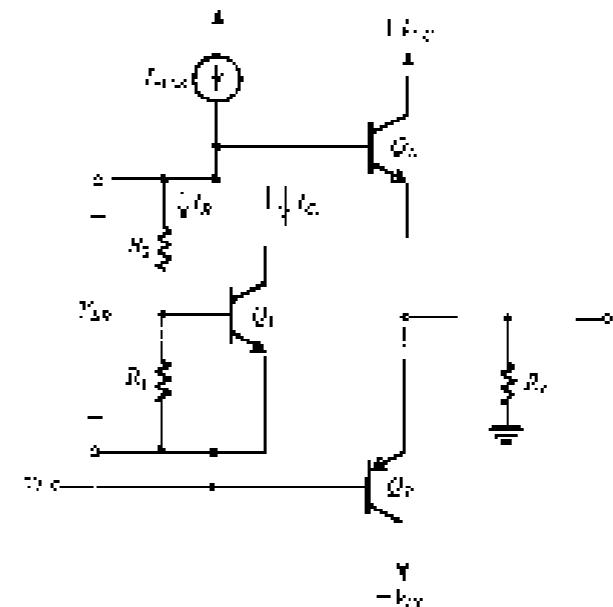
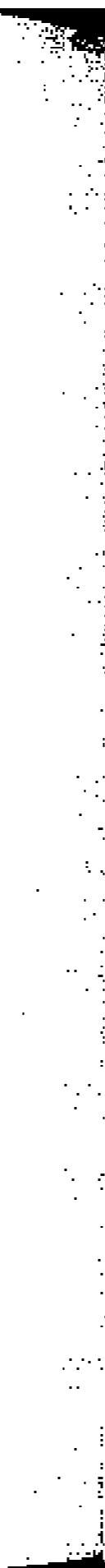


FIGURE 14.33 A $\lambda = 437\text{ nm}$ pulsed-laser line $\pm 1\%$ multiplier for hetero-

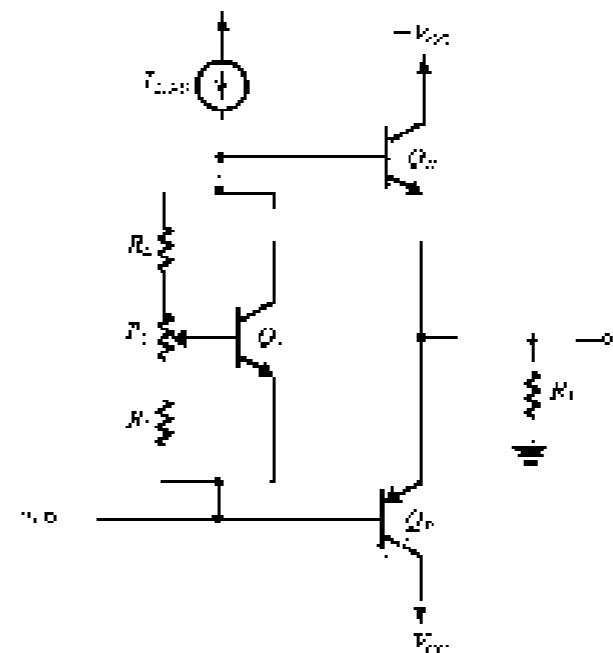


FIGURE 14-16 A Class A circuit uses AB output stages with a pentode load, and the V_G multiplies the pentode current to yield the desired value of current in I_1 , which is G_1 and G_2 .

used to establish the value of V_{sd} required to yield a desired saturation current I_s . In IC design it is relatively easy to control accurately the ratio of two resistances. In discrete circuit design, a potentiometer can be used, as shown in Fig. 14-16, and is manually set to provide the desired value of I_s .

The value of V_{BE} in Eq. (14.45) is determined by the portion of I_{BE} that flows through the collector of Q_2 ; that is,

$$I_{B2} = I_{BE} - I_B \quad (14.51)$$

$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_{B2}} \quad (14.52)$$

where we have neglected the base current of Q_3 , which is normally small under quiescent conditions and when the output voltage is swinging negative. However, for positive v_o , especially in and near its peak value, the base current of Q_3 can become sizable and will reduce the current gain factor for the V_{BE} multiplier. Nevertheless, since large changes in I_B correspond to only small changes in V_{BE} , the decrease in current will be mostly absorbed by Q_3 , leaving I_B , and hence V_{BE} , almost constant.

EXERCISE

Consider the circuit shown in Fig. 14.46, where $R_1 = R_2 = 10\text{k}\Omega$. Assuming a transistor with $\beta = 100$ and $V_T = 26\text{mV}$, determine the value of I_B required if the output voltage is to swing from 0 to 10 V. Assume that the value of I_B is constant in the negative voltage range. The value of I_B will result in the negative voltage being limited to about 1.5 V. Assume $V_{BE} = 0.66\text{V}$ and $V_{CE} = 20\text{V}$.

Like the diode biasing network, the V_{BE} multiplier can provide thermal stability around I_B . This is especially true if Q_1 , Q_2 , and Q_3 are in close thermal contact with the output transistors.

It is required to redesign the output stage of Example 14.2 using a V_{BE} multiplier for biasing. Use a small-signal transistor for Q_3 with $I_C = 10^{-4}\text{A}$ and design for a quiescent current $I_Q = 2\text{mA}$.

Solution

Since the peak positive current is 100 mA, the base current of Q_3 can be as high as 2 mA. We shall therefore select $I_{B3Q} = 2\text{mA}$, thus providing the multiplier with a quiescent current of 1 mA.

Under quiescent conditions ($v_o = 0$ and $b = 0$) the base current of Q_3 can be neglected since all of I_{BE3} flows through the multiplier. We now must decide on how this current (1 mA) is to be divided between I_{C3} and I_B . If we take I_B greater than 1.0 mA, the transistor will be almost cut off at the positive peak of v_o . Therefore, we shall set $I_B = 1.0\text{mA}$, leaving 0.5 mA for I_{C3} .

To obtain a quiescent current of 2 mA in the output transistors, V_{BE} should be

$$V_{BE} = 26\text{mV} \cdot \frac{2 \times 10^3}{10^4} = 1.06\text{V}$$

We can now determine $R_1 + R_2$ as follows:

$$R_1 + R_2 = \frac{V_{BE}}{I_B} = \frac{1.06}{0.5} = 2.12\text{k}\Omega$$

At a collector current of 2.5 mA, Q_3 has

$$V_{CE} = V_T \ln \frac{2.5 \times 10^3}{0.5} = 0.66\text{V}$$

The value of R_1 can now be determined as

$$R_1 = \frac{0.66}{0.5} = 1.32\text{k}\Omega$$

and R_2 is

$$R_2 = 2.12 - 1.32 = 0.8\text{k}\Omega$$

14.6 POWER BJTs

Transistors that are designed to conduct currents in the ampere range and withstand power dissipation in the kilowatt and megawatt ranges differ in their physical structure, packaging, and specification from the small-signal transistors considered in earlier chapters. In this section we consider some of the important properties of power transistors, especially those aspects that pertain to the design of circuits of the type discussed earlier. There are, of course, other important applications of power transistors, such as their use as switching elements in power inverters and motor-control circuits. Such applications are not studied in this book.

14.6.1 Junction Temperature

Power transistors dissipate large amounts of power in their collector-base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature T_j must not be allowed to exceed a specified maximum, T_{Jmax} , otherwise the transistor could suffer permanent damage. For silicon devices, T_{Jmax} is in the range of 150°C to 200°C.

14.6.2 Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating P_J watts, the temperature rise of the junction relative to the surrounding ambient can be expressed as

$$T_j - T_A = \theta_{JA} P_J \quad (14.61)$$

where θ_{JA} is the thermal resistance between junction and ambient, having the units of degrees Celsius per watt. Note that θ_{JA} simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipate large amounts of power without raising the junction temperature above T_{Jmax} , it is desirable to have, for the thermal resistance θ_{JA} , as small a value as possible. For operation in free air,

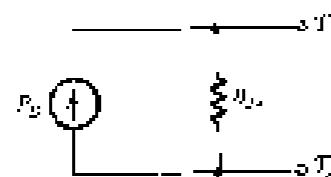


FIGURE 14.17 Electric circuit model of the thermal conduction process: $T_J = T_A + P_D \theta_{JA}$

θ_{JA} depends primarily on the type of case in which the transistor is packaged. The value of θ_{JA} is usually specified on the transistor data sheet.

Equation (14.36), which describes the thermal conduction process, is analogous to Ohm's law, which describes the electrical-conductor process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage drop, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal conduction process by the electric circuit shown in Fig. 14.17.

14.6.3 Power Dissipation Versus Temperature

The transistor manufacturer usually specifies the maximum junction temperature T_{Jmax} , the maximum power dissipation at a particular ambient temperature T_{A0} (usually, 25°C), and the thermal resistance θ_{JA} . In addition, a graph such as that shown in Fig. 14.18 is usually provided. The graph simply states that for operation at ambient temperatures below T_{A0} , the device can safely dissipate the rated value of P_D ; walls. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be reduced according to the straight-line shown in Fig. 14.18. The power-dissipation curve is a graphical representation of Eq. (14.36). Specifically, note that if the ambient temperature is T_A and the power dissipation is at the maximum allowed (P_{Dmax}), then the junction temperature will be T_{Jmax} . Substituting these quantities in Eq. (14.36) results in

$$\theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{Dmax}} \quad (14.37)$$

which is the inverse of the slope of the power-dissipation straight line. At an ambient temperature T_A higher than T_{A0} , the maximum allowable power dissipation P_{Dmax} can be obtained from Eq. (14.36) by substituting $T_J = T_{Jmax}$ there:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} \quad (14.38)$$

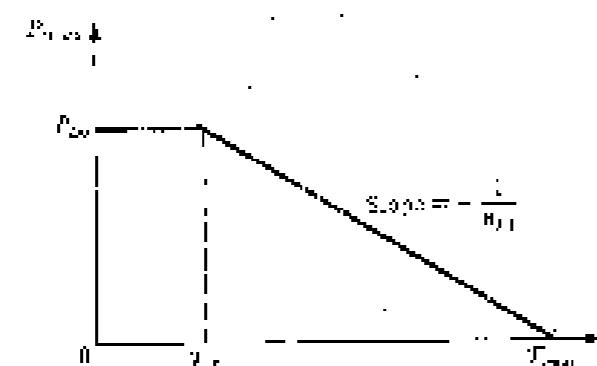


FIGURE 14.18 Maximum allowable power dissipation versus ambient temperature. (A 60-T transistor in plastic TO-3 package.) "power-dissipating" curve.

Observe that as T_A approaches T_{Jmax} , the allowable power dissipation decreases; the larger the thermal resistance θ_{JA} , the amount of heat that can be removed from the junction. In the extreme situation, if $T_A = T_{Jmax}$, no power can be dissipated because no heat can be removed from the junction.

14.6.4 Transistor Case and Heat Sink

A BJT is specified to have a maximum power dissipation P_{Dmax} of 2 W at an ambient temperature T_{A0} of 25°C, and a maximum junction temperature T_{Jmax} of 150°C. Find the following:

- (a) The thermal resistance θ_{JA} .
- (b) The maximum power that can be safely dissipated at an ambient temperature of 50°C.
- (c) The junction temperature if the device is operating at $T_A = 25^\circ\text{C}$ and is dissipating 1 W.

Solution:

$$(a) \theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{Dmax}} = \frac{150 - 25}{2} = 62.5^\circ\text{C/W}$$

$$(b) P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

$$(c) T_J = T_A + \theta_{JA}P_D = 25 + 62.5 \times 1 = 87.5^\circ\text{C}$$

14.6.4 Transistor Case and Heat Sink

The thermal resistance between junction and ambient, θ_{JA} , can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (14.39)$$

where θ_{JC} is the thermal resistance between junction and transistor case (package) and θ_{CA} is the thermal resistance between case and ambient. For a given transistor, θ_{JC} is fixed by the device design and packaging. The device manufacturer can reduce θ_{CA} by encapsulating the device in a relatively large metal case and placing the collector (where most of the heat is dissipated) in direct contact with the case. Most high-power transistors are packaged in this fashion. Figure 14.19 shows a sketch of a typical package.

Although the circuit designer has no control over θ_{JC} (once a particular transistor has been selected), the designer can considerably reduce θ_{CA} below its free-air value (specified by the manufacturer as part of θ_{JA}). Reduction of θ_{CA} can be effected by providing means to facilitate heat transfer from case to ambient. A popular approach is to bolt the transistor to the chassis or to an extended metal surface. Such a metal surface then functions as a heat sink. Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance θ_{CA} is usually very small. Also, heat is efficiently transferred by convection and



FIGURE 14.19 The popular TO-3 package in power transistor. The case is metal with a diameter of about 2.5 in. The side dimension of the "square" part is about 4 cm. The leading pin has two holes for screws to hold it to the heat sink. The collector is electrically connected to the case. Therefore, an electrically "hot" case is thermally conducting, since it moves between the transistor case and the heat sink.

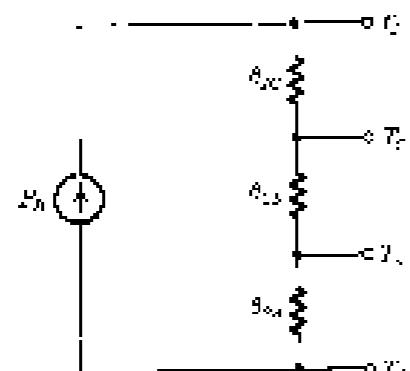


FIGURE 14.20 Electrical circuit of the Central conductor power when heat sink is fixed.

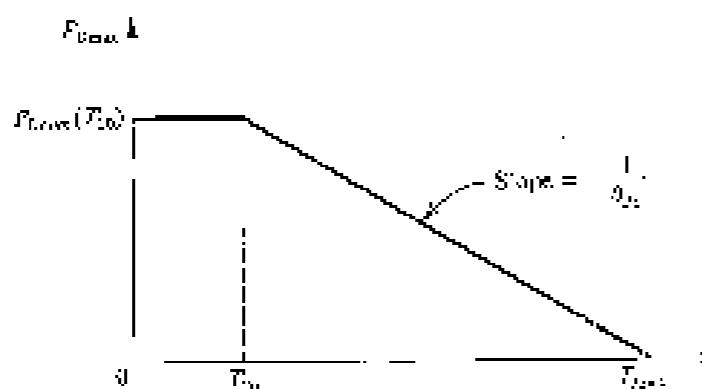


FIGURE 14.21 Maximum allowable power dissipation versus case temperature.

dissipating from the heat sink to the ambient, resulting in a low thermal resistance θ_{th} . Thus, if a heat sink is utilized, the case-to-ambit temperature is given by

$$\theta_{th} = \theta_{thc} + \theta_{thh} \quad (14.40)$$

can be small because its two components can be made small by the choice of an appropriate heat sink.² For example, in very high-power applications the heat sink is usually equipped with fins that further facilitate cooling by radiation and convection.

The electrical analog of the thermal-conduction process when a heat sink is employed is shown in Fig. 14.20, from which we can write

$$T_c - T_a = I_h (\theta_{thc} + \theta_{thf} + \theta_{thh}) \quad (14.41)$$

As well as specifying θ_{th} , the device manufacturer usually supplies a derating curve for P_{max} versus the case temperature, T_c . Such a curve is shown in Fig. 14.21. Note that the slope of the power-decaying straight line is $-1/\theta_{th}$. For a given transistor, the maximum

² At most, one side of a power transistor is electrically connected to the exterior. This is an electrically insulating material such as mica it usually placed between the metal case and the metal heat sink. Also, insulating washers and washers are generally used in isolating the transistor to the heat sink.

power dissipation at a case temperature T_c (usually 25°C) is much greater than that at an ambient temperature T_a (usually 35°C). If the device can be maintained at a case temperature T_c , $T_{th} \leq T_c \leq T_{thm}$, then the maximum safe power dissipation is obtained when $T_c = T_{thm}$:

$$P_{max} = \frac{T_{thm} - T_a}{\theta_{th}} \quad (14.42)$$

A BJT is specified to have $T_{thm} = 150^\circ\text{C}$ and to be capable of dissipating maximum power as follows:

$$70 \text{ W at } T_c = 25^\circ\text{C}$$

$$2 \text{ W at } T_c = 25^\circ\text{C}$$

Above 25°C, the maximum power dissipation is to be derived linearly with $\theta_{th} = 3.12^\circ\text{C/W}$ and $\theta_{thh} = 0.5^\circ\text{C/W}$. Find the following:

(a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_c = 50^\circ\text{C}$.

(b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 55°C, but with a heat sink for which $\theta_{th} = 0.5^\circ\text{C/W}$ and $\theta_{thh} = 4^\circ\text{C/W}$. Find the temperature of the base end of the heat sink.

(c) The maximum power that can be dissipated safely if an infinite heat sink is used and $T_a = 50^\circ\text{C}$.

Solution

(a)

$$P_{max} = \frac{T_{thm} - T_a}{\theta_{th}} = \frac{150 - 25}{3.12} = 41.6 \text{ W}$$

(b) With a heat sink, θ_{th} becomes

$$\begin{aligned} \theta_{th} &= \theta_{thc} + \theta_{thf} + \theta_{thh} \\ &= 3.12 + 0.5 + 4 = 7.63^\circ\text{C/W} \end{aligned}$$

Thus,

$$P_{max} = \frac{150 - 55}{7.63} = 13.1 \text{ W}$$

Figure 14.22 shows the thermal equivalent circuit with the various temperatures indicated.

(c) An infinite heat sink, if it existed, would cause the case temperature T_c to equal the ambient temperature T_a . The infinite heat sink has $\theta_{th} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-dissipation curve of Fig. 14.21. The selection is then "infinite 2," and the curve is called "power dissipation versus ambient temperature with an infinite heat sink." For our example, with infinite heat sink,

$$P_{max} = \frac{T_{thm} - T_a}{\theta_{th}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

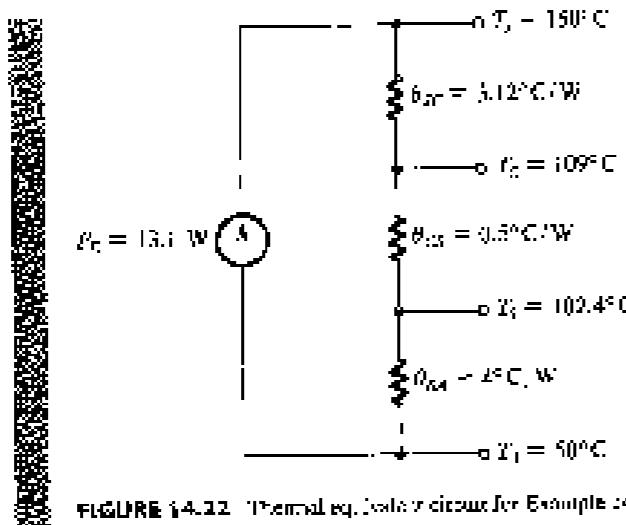


FIGURE 14.22 Thermal equivalent circuit for Example 14.5.

The advantage of using a heat sink is clearly evident from Example 14.5. With a heat sink, the maximum allowable power dissipation increases from 1.6 W to 13.1 W. Also note that although the transistor considered can be called a "40-W transistor," this level of power dissipation cannot be achieved in practice; it would require an infinite heat sink and an ambient temperature $T_A \leq 25^\circ\text{C}$.

EXERCISE

14.70 For 2N3906 power transistors specified ($\beta = 50$, $V_{CE(sat)} = 0.2$ V), $\theta_{CA} = 2^\circ\text{C}/\text{W}$, $\theta_{CB} = 0.5^\circ\text{C}/\text{W}$, $\theta_{JT} = 0.12^\circ\text{C}/\text{W}$. If in a particular application the device is to dissipate 50 W and is to be mounted on a heat sink with a thermal resistance of 0.1°C/W, determine the heat sink junction temperature. (Assume $\theta_{CS} = 0.05^\circ\text{C}/\text{W}$ neglect of the case temperature.)

14.6.5 The BJT Safe Operating Area

In addition to specifying the maximum power dissipation at different case temperatures, power-transistor manufacturers usually provide a plot of the boundary of the safe operating area (SOA) in the i_C - v_{CE} plane. The SOA specification takes the form illustrated by the sketch in Fig. 14.23; the following paragraph numbers correspond to the boundaries of the sketch.

1. The maximum allowable current I_{Cmax} . Exceeding this current in a continuous mode can result in melting the wires that bond the device to the package terminals.
2. The maximum power-dissipation hyperbola. This is the locus of the points for which $v_{CE} = P_{Dmax}$ (at T_{case}). For temperatures $T_{case} > T_{case}$, the power-dissipation curves $v_{CE} = P_{Dmax}$ (at T_{case}) should be used to obtain the applicable P_{Dmax} and draw a correspondingly lower hyperbola. Although the operating point can be allowed to move temporarily above the hyperbola, the average power dissipation should not be allowed to exceed P_{Dmax} .

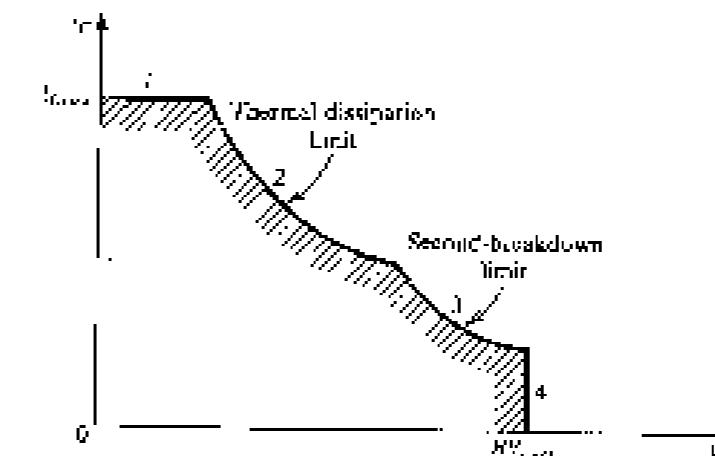


FIGURE 14.23 Safe operating area (SOA) of a BJT.

3. The second-breakdown limit. Second breakdown is a phenomenon that results because current flow across the collector-base junction is not uniform. Rather, the current density is greatest near the periphery of the junction. This "current crowding" gives rise to increased localized power dissipation and hence temperature rise (at locations called hot spots). Since a temperature rise causes an increase in current, a localized form of thermal runaway can occur, leading to junction destruction.
4. The collector-to-emitter breakdown voltage, BV_{CEO} . The instantaneous value of v_{CE} should never be allowed to exceed BV_{CEO} ; otherwise, avalanche breakdown of the collector-base junction may occur (see Section 5.2.5).

Finally, it should be mentioned that logarithmic scales are usually used for i_C and v_{CE} , leading to an SOA boundary that consists of straight lines.

14.6.6 Parameter Values of Power Transistors

Owing to their large geometry and high operating currents, power transistors display typical parameter values that can be quite different from those of small-signal transistors. The important differences are as follows:

1. At high currents, the exponential i_C – v_{CE} relationship exhibits a constant $\alpha = 2$; that is, $i_C = i_{C0} e^{\alpha(v_{CE}-V_{CE(sat)})}$.
2. β is low, typically 50 to 80, but can be as low as 5. Here, it is important to note that β has a positive temperature coefficient.
3. At high currents, r_e becomes very small (a few ohms) and r_o becomes important (r_o is defined and explained in Section 5.8.4).
4. f_T is low (a few megahertz), C_{ce} is large (hundreds of picofarads), and C_{cb} is even larger. (These parameters are defined and explained in Section 5.8.)
5. I_{CBO} is large (a few tens of microamps) and, as usual, doubles for every 10°C rise in temperature.
6. BV_{CEO} is typically 50 to 100 V but can be as high as 500 V.
7. i_{C0ss} is typically in the ampere range but can be as high as 100 A.

14.7 VARIATIONS ON THE CLASS AB CONFIGURATION

In this section, we discuss a number of circuit improvement and protection techniques for the class A/B output stage.

14.7.1 Use of Input Emitter Followers

Figure 14.24 shows a class AB circuit biased using transistors Q_1 and Q_2 , which also function as emitter followers, thus providing the circuit with a high input resistance. In effect, the circuit functions as a unity-gain buffer amplifier. Since all four transistors are usually matched, the quiescent current ($i_b = 0$, $I_C = 0$) in Q_1 and Q_2 is equal. In that in Q_1 and Q_2 , Resistors R_3 and R_4 are usually very small and are included to compensate for possible mismatching between Q_1 and Q_2 and to guard against the possibility of thermal runaway due to temperature differences between the top, i.e., output-stage transistors. The latter point can be appreciated by noting that an increase in the current of, say, Q_1 causes an increase in the voltage drop across R_3 and a corresponding decrease in V_{BE1} . Thus, R_3 provides negative feedback that helps stabilize the current through Q_1 .

Because the circuit of Fig. 14.24 requires high-current power resistors, it is an infinite-five implementation in conventional monolithic IC technology. However, excellent results have been obtained with this circuit implemented in hybrid thick-film technology (Wong and Sherman, 1979). This technology permits component minimization, for instance, to minimize the output offset voltage. The circuit can be used alone or together with an op-amp to

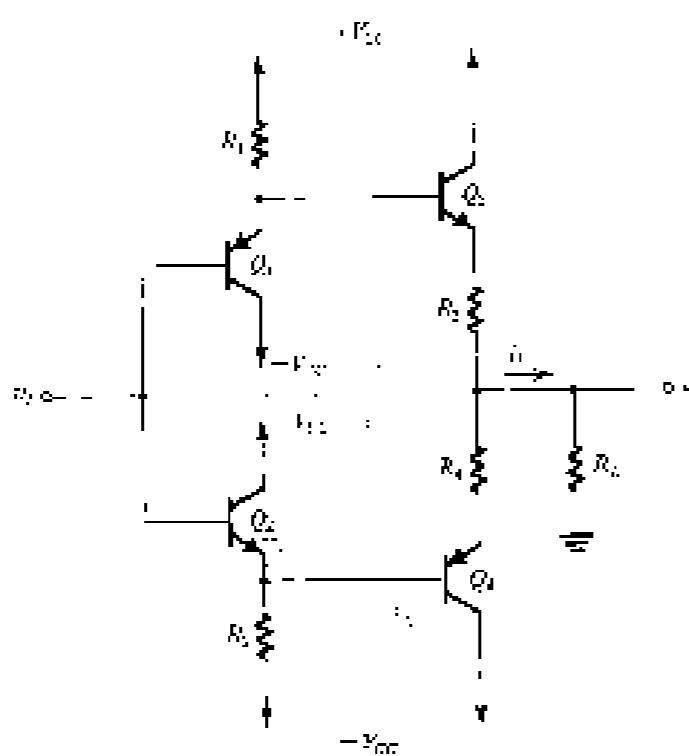


FIGURE 14.24 A class *AP* ... (cont.) implements an interface *B*. In addition to providing a *highInput* resource, the *lowInput*, constraint P , and Q bits, the unit also maintains $Q \rightarrow \neg Q$.

provided increased output driving capability. The latter application will be discussed in the next section.

ANSWER

15.11 The following properties of a diode are given. Calculate the value of R_s , $14.21 \text{ m}\Omega$, if $V_{BE} = 0.7 \text{ V}$ at $I_D = 10 \text{ mA}$. The saturation current is $I_0 = 5 \times 10^{-12} \text{ A}$, $n = 1$, $\eta = 0.1$, and the values used in the Ebers-Moll model are the same as in Example 15.10 except that $A = 3$ instead of 1. Therefore, $\beta = \infty$, and the quiescent current is one-third of the forward current. This gives $I_S = 3 \times 10^{-12} \text{ A}$, $I_D = 10 \text{ mA}$, $V_D = -10 \text{ V}$, and -0.2 V for V_{BE} at $I_D = 10 \text{ mA}$.

14.7.2 Use of Compound Devices

To increase the current gain of the output-stage transistors, and thus reduce the required base current drive, the Darlington configuration shown in Fig. 14.29 is frequently used to replace the open transistor of the class AB stage. The Darlington configuration (Section 6.11.2) is equivalent to a single MOS transistor having $\beta = \beta_1\beta_2$, but almost twice the value of V_{DS} .

The Darlington configuration can be also used for pnp transistors, and this is indeed done in discrete-circuit design. In IC design, however, the lack of good-quality pnp transistors prompted the use of the alternative compound configuration shown in Fig. 14.26. This compound device is equivalent to a single pnp transistor having $\beta = \beta_1\beta_2$. When fabricated with standard IC technology, β_1 is usually a bipolar pnp having a low $\beta_1(\beta_1=5-10)$ and poor high-frequency response ($f_T < 5$ MHz); see Appendix A. The compound device, although it has a relatively high equivalent β , still suffers from a poor high-frequency response. It also suffers from another problem: The feedback loop formed by Q_1 and Q_2 is prone to high-frequency oscillations (with frequency near f_T) of the pnp device, i.e., about 5 MHz. Methods used to prevent such oscillations, the subject of feedback-amplifier stability, was studied in Chapter 8.

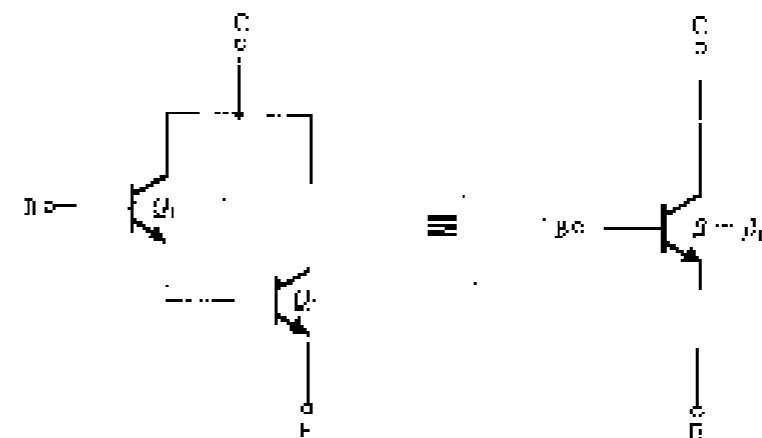


FIGURE 14.25 The Duration matrix.

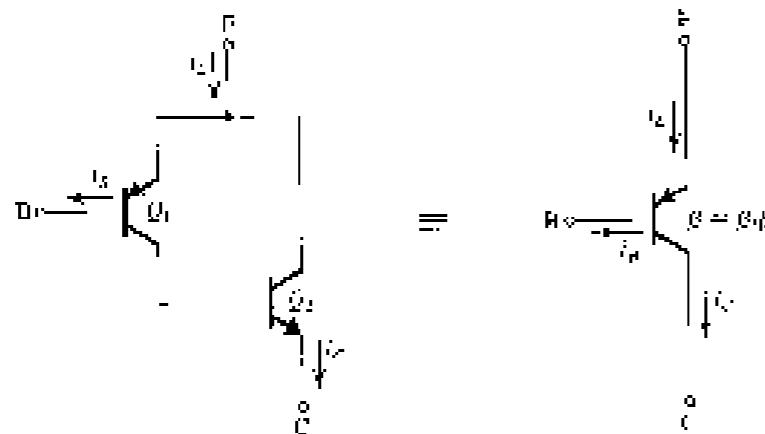
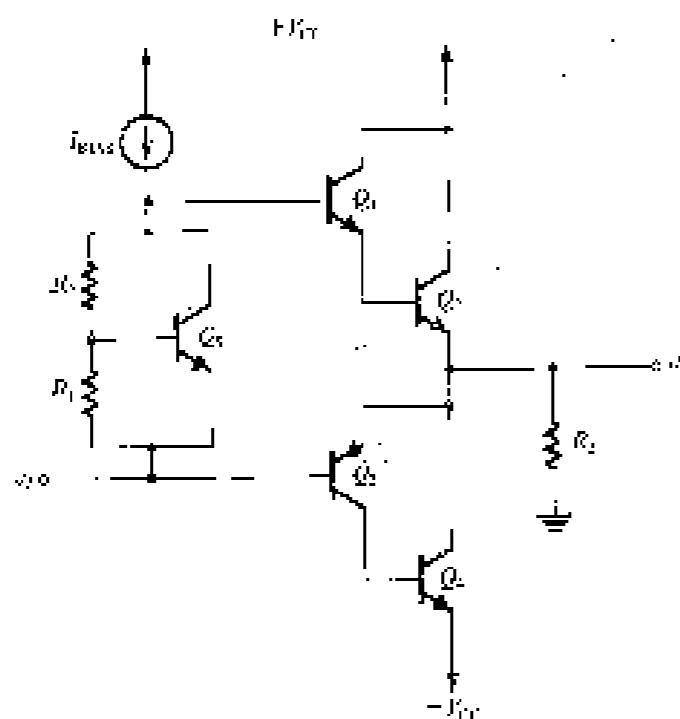


FIGURE 14.26 The compound-pair configuration.

To illustrate the application of the Darlington configuration and of the compound pair, we show in Fig. 14.27 an output stage utilizing both. Class AB biasing is achieved using a V_{BE} multiplier. Note that the Darlington pair adds one more V_{BE} drop, and thus the V_{BE} bias Epitac is required to provide a bias voltage of about 2 V. The design of this class AB stage is investigated in Problem 14.39.

FIGURE 14.27 A class AB output stage utilizing a Darlington pair and a compound pair. Biasing is done using a V_{BE} multiplier.

EXERCISE

14.7.1. For the circuit in Fig. 14.28, find the composite β of the pair.

Solution: The circuit is a Darlington pair. The total current is $I_C = I_B$. The current through Q_1 is I_B , and the current through Q_2 is $I_B \beta_2$.

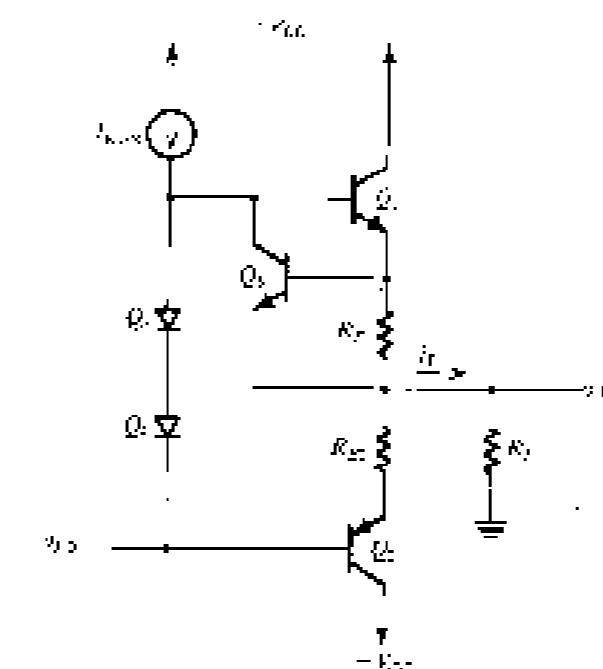
The total current is $I_C = I_B + I_B \beta_2 = I_B(1 + \beta_2)$. The composite β is $\beta = 1 + \beta_2$.

14.7.2. For the circuit in Fig. 14.29, find the collector current of the compound pair, assuming $\beta_1 = 20$, $\beta_2 = 50$, $I_B = 70 \mu A$, and the collector current of the Q_1 Darlington is $I_B \beta_1$, where $I_B = 300 \mu A$; $I_B \beta_1 = 1$.

Solution: By Ohm's law, $I_B = 300 \mu A$. The current through Q_1 is $I_B \beta_1 = 300 \mu A \cdot 20 = 6 \text{ mA}$. The current through Q_2 is $I_B \beta_2 = 6 \text{ mA} \cdot 50 = 300 \text{ mA}$.

14.7.3 Short-Circuit Protection

Figure 14.28 shows a class AB output stage equipped with protection against the effect of short-circuiting the output, while the stage is sourcing current. The large current that flows through Q_1 in the event of a short circuit will develop a voltage drop across R_{L1} of sufficient

FIGURE 14.28 A class AB output stage with short-circuit protection. The protection circuit is added to the event of an output short circuit with v_{o1} positive.

value to turn Q_3 on. The collector of Q_3 will then conduct most of the current $I_{R_{23}}$, turning Q_2 off at its base node. The current through Q_1 will thus be reduced to a safe operating level.

This method of short-circuit protection is effective in ensuring device safety, but it has the disadvantage that under normal operation about 0.5 V drop might appear across each R_L . This means that the voltage swing at the output will be reduced by that much in each direction. On the other hand, the inclusion of emitter resistors provides the additional benefit of protecting the output transistors against thermal runaway.

EXERCISE

- 14.13 In the circuit of Fig. 14.28 let $I_{C1} = 10 \text{ mA}$ and the value of R_L be reduced to 0. Calculate the output voltage at all 250 K when the output current is held constant at 100 mA. Let $V_{BE} = 0.7 \text{ V}$ and $\alpha = 0.95$. Assume a peak-to-peak current of 100 mA, and the load-line diagram for R_L and the collector currents of Q_1 and Q_2 is given in Fig. 14.29. What is the output voltage?

14.7.4 Thermal Shutdown

In addition to short-circuit protection, most IC power amplifiers are usually equipped with a circuit that senses the temperature of the chip and turns off a transistor in the event that the temperature exceeds a safe preset value. The turned-on transistor is connected in such a way that it shorts the bias current to the amplifier, thus virtually shutting down its operation.

Figure 14.29 shows a thermal-shutdown circuit. Here, transistor Q_2 is normally off. As the chip temperature rises, the combination of the positive temperature coefficient of the zener diode Z_1 and the negative temperature coefficient of V_{BE2} causes the voltage at the emitter of Q_2 to rise. This in turn raises the voltage at the base of Q_2 to the point at which Q_2 turns on.

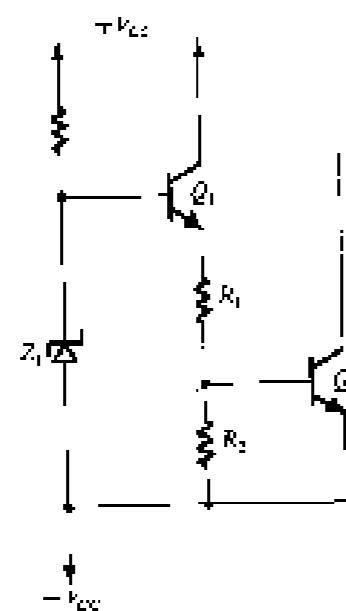


FIGURE 14.29 Thermal shutdown circuit

14.8 IC POWER AMPLIFIERS

A variety of IC power amplifiers are available. Most consist of a high-gain small-signal amplifier followed by a class AB output stage. Some have overall negative feedback already applied, resulting in a fixed closed-loop voltage gain. Others do not have on-chip feedback and are, in effect, op amps with large output-power capability. In fact, the output-current driving capability of any general-purpose op amp can be increased by cascading it with a class B or class AB output stage and applying overall negative feedback. The individual output stage can be either a discrete circuit or a hybrid IC such as the buffer discussed in the preceding section. In the following we discuss some power-amplifier examples.

14.8.1 A Fixed-Gain IC Power Amplifier

Our first example is the LM380 (a product of National Semiconductor Corporation), which is a fixed-gain monolithic power amplifier. A simplified version of the internal circuit of the amplifier⁷ is shown in Fig. 14.30. The circuit consists of an input differential amplifier utilizing Q_1 and Q_2 as emitter followers for input buffering, and Q_3 and Q_4 as a differential pair with an emitter resistor R_3 . The two resistors R_4 and R_5 provide dc paths to ground for the base circuits of Q_3 and Q_4 , thus enabling the input signal source to be capacitively coupled to either of the two input terminals.

The differential amplifier transistors Q_3 and Q_4 are biased by two separate direct currents: Q_3 is biased by a current from the dc supply V_2 through the diode-connected transistor Q_{10} and resistor R_1 ; Q_4 is biased by a dc current from the output terminal through R_6 . Under quiescent conditions (i.e., with no input signal applied) the two bias currents will be equal, and the current through and the voltage across R_1 will be zero. For the emitter current of Q_3 we can write

$$I_3 = \frac{V_2 - V_{BE3} - V_{BE4} - V_{Z1}}{R_1}$$

where we have neglected the small dc voltage drop across R_4 . Assuming, for simplicity, all V_{BE} to be equal,

$$I_3 = \frac{V_2 - 3V_{BE}}{R_1} \quad (14.43)$$

For the emitter current of Q_4 we have

$$\begin{aligned} I_4 &= V_2 - \frac{V_{BE4} - V_{BE3}}{R_2} \\ &= V_2 - \frac{2V_{BE}}{R_2} \end{aligned} \quad (14.44)$$

where V_{Z1} is the dc voltage at the output and we have neglected the small drop across R_5 . Equating I_3 and I_4 and using the fact that $R_1 = 2R_2$, results in

$$V_{Z1} = \frac{1}{2}V_2 + \frac{1}{2}V_{BE} \quad (14.45)$$

Thus the output is biased at approximately half the power-supply voltage, as desired for maximum output voltage swing. An important feature is the dc feedback from the output to

⁷ The main objective of showing it is not to go into great engineering nitty-gritty. The circuit is not a detailed schematic diagram of what is actually on the chip.

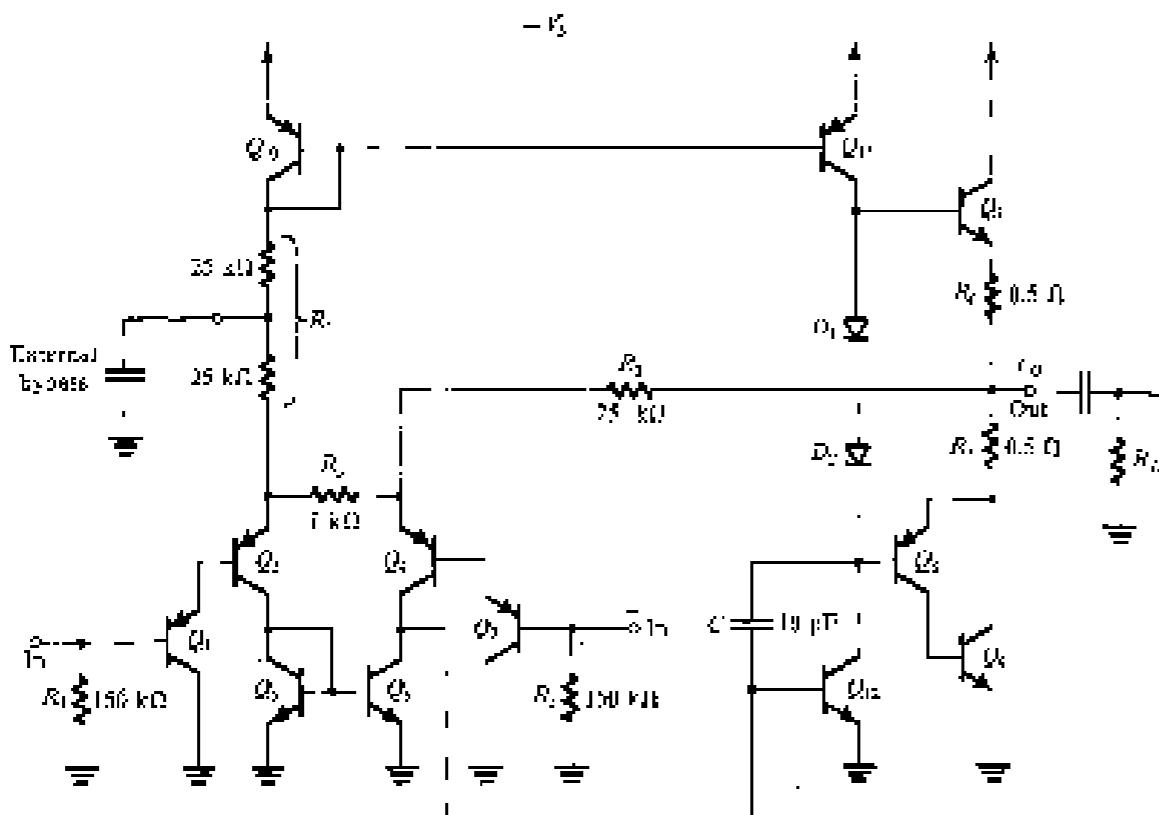


FIGURE 14.30 The simplified circuit diagram of the LM396 power amplifier. (Courtesy: National Semiconductor Corporation.)

the emitter of Q_4 , through R_8 . This dc feedback acts to stabilize the output dc bias voltage at the value in Eq. (14.35). Qualitatively, the dc feedback function is as follows: If for some reason V_o increases, a corresponding current increase will flow through R_2 and into the collector of Q_4 . Thus, the collector current of Q_4 increases, resulting in a positive increment in the voltage at the base of Q_{12} . Thus, in turn, causes the collector current of Q_{12} to increase, thus bringing down the voltage at the base of Q_4 and hence V_o .

Continuing with the description of the circuit in Fig. 14.30, we observe that the differential amplifier (Q_1 , Q_2) has a current mirror load consisting of Q_3 and Q_4 (refer to Sec. 7.5.3 for a discussion of active loads). The single-ended output voltage signal of the first stage appears at the collector of Q_3 and this is applied to the base of the second-stage common-emitter amplifier (Q_5). Transistor Q_{12} is biased by the constant-current source Q_9 , which also acts as its active load. In actual operation, however, the load of Q_{12} will be dominated by the reflected resistance due to R_6 . Capacitor C provides frequency compensation (see Chapter 8).

The output stage is class AB, utilizing a complementary pair transistor (Q_7 and Q_8). Negative feedback is applied from the output to the emitter of Q_7 via resistor R_2 . To find the closed-loop gain consider the small-signal equivalent circuit shown in Fig. 14.31. Here, we have replaced the second-stage common-emitter amplifier and the output stage with an inverting amplifier block with gain A . We shall assume that the amplifier A has high gain and high input resistance, and thus the input signal current into β is negligibly small. Under this assumption, Fig. 14.31 shows the analysis details with an input signal v_i applied to the inverting input

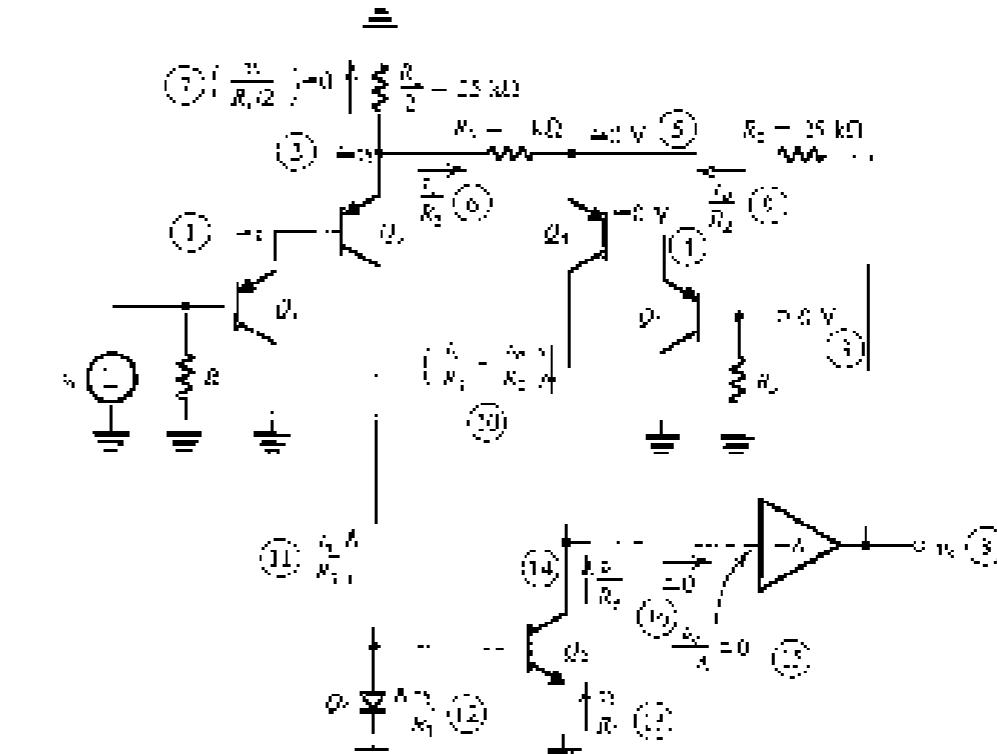


FIGURE 14.31 Small-signal analysis of the circuit in Fig. 14.30. The circled numbers indicate the order of the analysis steps.

terminal. The order of the analysis steps is indicated by the circled numbers. Note that since the input differential amplifier has a relatively large resistance, R_1 , in the emitter circuit most of the applied input voltage appears across R_1 . In other words, the signal voltages across the emitter-base junctions of Q_1 , Q_2 , Q_3 , and Q_4 are small in comparison to the voltage across R_1 . Accordingly, the voltage gain can be found by writing a node equation at the collector of Q_6 :

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = 0$$

which yields

$$\frac{V_3}{V_1} = -\frac{R_2}{R_1} = -50 \text{ V/V}$$

EXERCISE

- 14.8-1 Consider the circuit in Fig. 14.30. Assume that the second-stage common-emitter amplifier has a voltage gain of $A = 100$ and a low input resistance of 100Ω . The output stage has a voltage gain of $A = 1000$ and a low input resistance of 10Ω . The input voltage is $v_i = 10 \mu\text{V}$. Find the output voltage V_o and the collector currents of Q_1 through Q_8 .

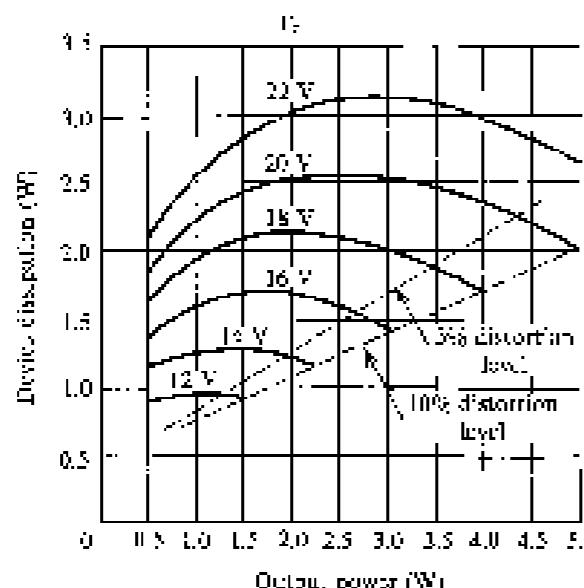


FIGURE 14.32 Power absorption (P_{abs}) vs. bias voltage (V_{bias}) for the MOSFET with $R_L = 8 \Omega$. (From National Semiconductor Corporation.)

As was demonstrated in Chapter 8, one of the advantages of negative feedback is the reduction of unclipped saturation. This is the case in the circuit of the LM380.

The LM1880 is designed to operate from a single supply V_S in the range of 12 V to 22 V. The selection of supply voltage depends on the value of R_L and the required output power P_o . The manufacturer supplies curves for the device power dissipation versus output power for a given load resistance and various supply voltages. One such set of curves for $R_L = 4 \Omega$ is shown in Fig. 14.32. Note the similarity to the class B power dissipation curve in Fig. 14.31. In fact, the reader can easily verify that the location and value of the peaks of the curves in Fig. 14.32 are accurately predicted by Eqs. (14.20) and (14.21), respectively (where $V_{BR} = 15V$). The line labeled "5% distortion level" in Fig. 14.32 is the locus of the points on the various curves at which the distortion [Eq.(14.10)] reaches 5%. A THD of 5% represents the onset of peak clipping due to output-transistor saturation.

The main parameter for supplies curves for maximum power dissipation versus temperature (deriving at 2020) similar to those discussed in Section 14.5 for discrete power MOSFETs.

EXERCISES

- 014.15 The man, who is good for his word, will make arrangements to have 25 C. the U.S. Army, delivered to the
head of the U.S. Consular Mission at the earliest date. It is further arranged to have the
pork sent direct to the U.S. Consul with a copy to the Adjutant General of the U.S. Cavalry, who
will see that it reaches us as soon as possible. It is requested to have 50 C. sent from the regimental store
house, and possibly 100 C. to be supplied by the Adjutant General to the 25 C.

Ans. 25 C. M.

014.16 It is requested that 25 C. be sent to the Consul at the earliest date. It is further arranged that the
ministering general will furnish the Adjutant General of the U.S. Cavalry with a copy of the
order regarding the 25 C. to be sent to the Consul at the earliest date. It is also requested that the Adjutant General
Ans. 25 C. M. S. F.

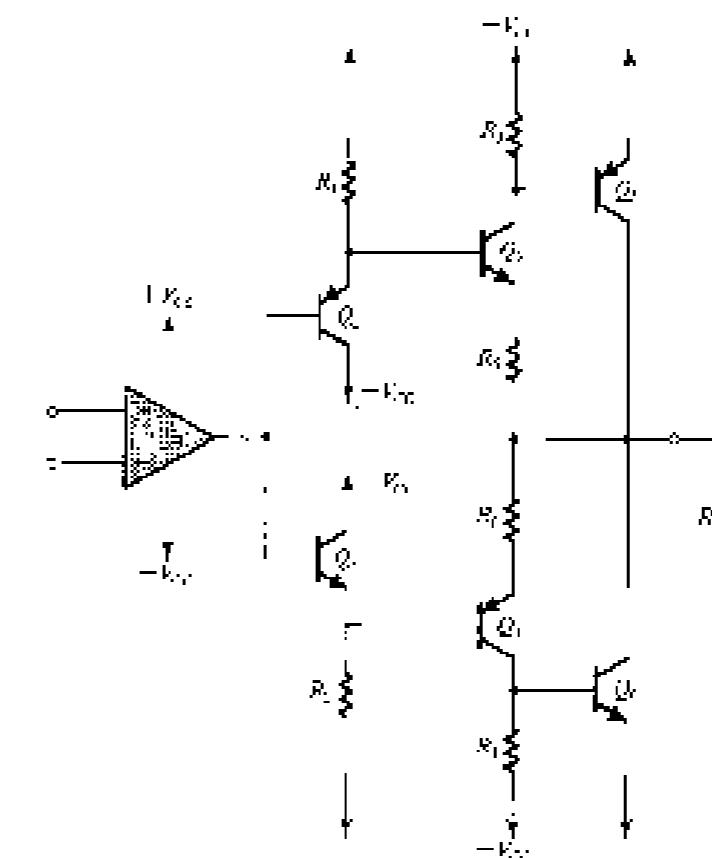


FIGURE 14.33 Structure of a boost op-amp. The circuit consists of an op-amp followed by a class AB buffer similar to that discussed in Section 14.3.1. The output voltage capability of the converter, considering the G_1, G_2, G_3, G_4 , and G_5 gains, is limited by $G_{out} \cdot G_2$.

14.9.2 Power Op Amp

Figure 14.39 shows the general structure of a power op-amp. It consists of a low-power op-amp followed by a class AB buffer similar to that discussed in Section 14.7.1. The buffer consists of transistors Q_1 , Q_2 , Q_3 , and Q_4 , with bias resistors R_1 and R_2 and anti-degeneration resistors R_3 and R_4 . The tail or supplies the required load current until the current increases to the point that the voltage drop across R_3 (in the current-sourcing mode) becomes sufficiently large to turn Q_3 on. Transistor Q_4 then supplies the additional load current required. In the current-sinking mode, Q_2 supplies the load current until sufficient voltage develops across R_4 to turn Q_3 off. Then, Q_4 sinks the additional load current. Thus the stage formed by Q_3 and Q_4 acts as a current booster. The power op-amp is intended to be used with negative feedback in the usual closed-loop configurations. A circuit based on the structure of Fig. 14.39 is numerically available from National Semiconductor as UJD1011. This chip is capable of providing a continuous output current of 2 A, and with appropriate heat sinking can provide 40 W of output power (Wing and Johnson, 1974). The UJD1011 is fabricated using hybrid thick-film technology.

14.8.3 The Bridge Amplifier

We conclude this section with a discussion of a circuit configuration that is popular in high-power applications. This is the bridge-amplifying configuration shown in Fig. 14.37 utilizing

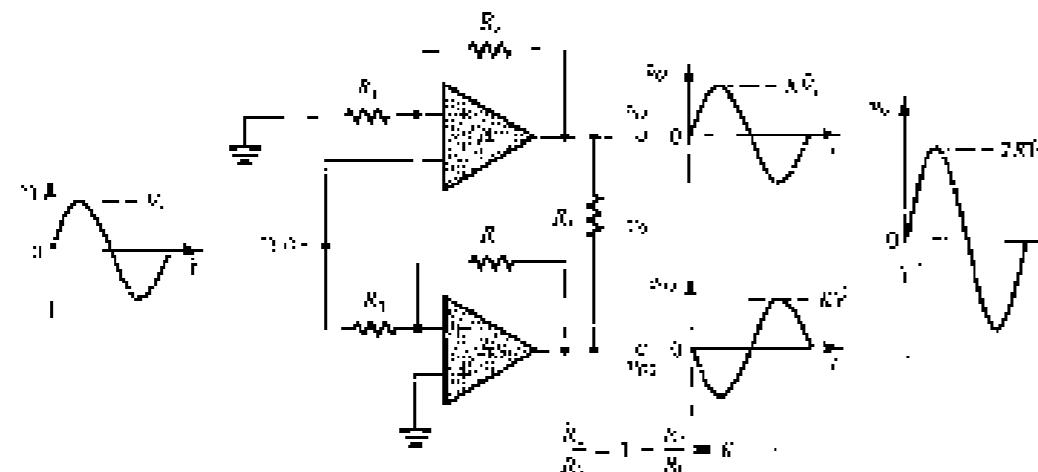


FIGURE 14.34 Two bridge amplifier configurations.

two power op-amps, A_1 and A_2 . While A_1 is connected in the noninverting configuration with a gain $K = 1 + (R_2/R_1)$, A_2 is connected as an inverting amplifier with a gain of A_{2A} magnitude $K = R_1/R_2$. The total K is favoring and is connected between the output terminals of the two op-amps.

If v_1 is a sinusoid with amplitude V_1 , the voltage swing at the output of each op-amp will be $\pm KV_1$, and that across the load will be $\pm 2KV_1$. Thus, with op-amps operated from 15-V supplies and capable of providing, say, ± 12 -V output swing, an output swing of 124 V is obtained across the load of the bridge amplifier.

In designing bridge amplifiers, note should be taken of the fact that the peak current drawn from each op-amp is $\pm KV_1/R_2$. This effect can be taken into account by considering the load seen by each op-amp (to ground) to be $R_2/2$.

EXERCISE

- 14.7 Consider the circuit of Fig. 14.34 with $K = 3$, $A_{2A} = 5$, $R_1 = 10\text{ k}\Omega$, $R_2 = 20\text{ k}\Omega$, $R_3 = 10\text{ k}\Omega$, and $R_4 = 20\text{ k}\Omega$. If the peak-to-peak voltage at the output of the first op-amp is 10 V , what is the peak-to-peak voltage at the load? What is the total power?

14.9 MOS POWER TRANSISTORS

Although, thus far in this chapter we have dealt exclusively with BJT circuits, there exist MOS power transistors with specifications that are quite competitive with those of BJTs. In this section we consider the structure, characteristics, and application of power MOSFETs.

14.9.1 Structure of the Power MOSFET

The MOSFET structure studied in Chapter 4 (Fig. 4-1) is not suitable for high-power applications. To appreciate this fact, recall that the drain current of an n-channel MOSFET

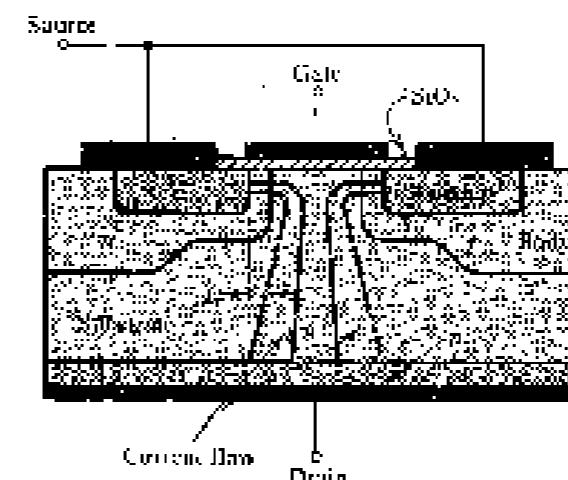


FIGURE 14.35 Cross-sectional view of MOS transistor JW328.

operating in the saturation region is given by

$$i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (v_{GS} - v_T)^2 \quad (14.40)$$

It follows that to increase the current capability of the MOSFET, its width W should be made large and its channel length L should be made as small as possible. Unfortunately, however, reducing the channel length of the standard MOSFET structure results in a drastic reduction in its breakdown voltage. Specifically, the depletion region of the reverse-biased body-to-drain junction spreads into the short channel, resulting in breakdown at a relatively low voltage. Thus the resulting device would not be capable of handling the high voltages typical of power-transistor applications. For this reason, new techniques had to be found for fabricating short-channel (1 - to 2 - μm) MOSFETs with high breakdown voltages.

At the present time the most popular structure for a power MOSFET is the double-diffused or DMOS transistor shown in Fig. 14.35. As indicated, the device is fabricated on a lightly doped n-type substrate with a heavily doped region as the broken line for the drain contact. Two diffusions⁴ are employed, one to form the p-type body region and another to form the n-type source region.

The DMOS device operates as follows. Application of a positive gate voltage, v_{GS} , greater than the threshold voltage v_T induces a lateral n channel in the p-type body region underneath the gate oxide. The resulting channel is short, its length is denoted L in Fig. 14.35. Current is then conducted by electrons from the source traveling through the resulting short channel to the substrate and then vertically down the substrate to the drain. This should be contrasted with the lateral current flow in the standard small-signal MOSFET structure (Chapter 4).

Even though the DMOS transistor has a short channel, its breakdown voltage can be very high (as high as 600 V). This is because the depletion region between the substrate and the body extends mostly in the lightly doped substrate and does not spread into the channel. The result is a MOS transistor that simultaneously has a high current capability (50 A is possible)

⁴See Appendix A for a description of the IC fabrication process.

as well as the high breakdown voltage just mentioned. Finally, we note that the vertical structure of the device provides efficient utilization of the silicon area.

An earlier structure used for power MOS transistors concerned moderation. This is the V-groove MOS device [see Szevers (1984)]. Although still in use, the V-groove MOSFET has lost application ground to the vertical DMOS structure of Fig. 14.33, except possibly for high-frequency applications. Because of space limitations, we shall not describe the V-groove MOSFET.

14.9.2 Characteristics of Power MOSFETs

In spite of their radically different structure, power MOSFETs exhibit characteristics that are quite similar to those of the small-signal MOSFETs studied in Chapter 4. Impurity differences exist, however, and these are discussed next.

Power MOSFETs have threshold voltages in the range of 1.2 V to 4 V. In saturation, the drain current is related to V_{DS} by the square-law characteristic of Eq. (14.46). However, as shown in Fig. 14.36, the I_D - V_{DS} characteristic becomes linear for larger values of V_{DS} . The linear portion of the characteristic occurs as a result of the high electric field along the drain channel, causing the velocity of charge carriers to reach an upper limit, a phenomenon known as velocity saturation. The drain current is then given by

$$I_D = \gamma C_s W U_{DS} (V_{DS} - V_t) \quad (14.47)$$

where U_{DS} is the saturated velocity value (5×10^6 cm/s for electrons in silicon). The linear I_D - V_{DS} relationship implies a constant γ . In the velocity-saturation region, it is interesting to note that γ is proportional to W , which is usually large for power devices; thus power MOSFETs exhibit relatively high transconductance values.

The I_D - V_{DS} characteristic shown in Fig. 14.36 includes a segment labeled "subthreshold." Though of little significance for power devices, the subthreshold region of operation is of interest in very-low-power applications (see Section 14.8).

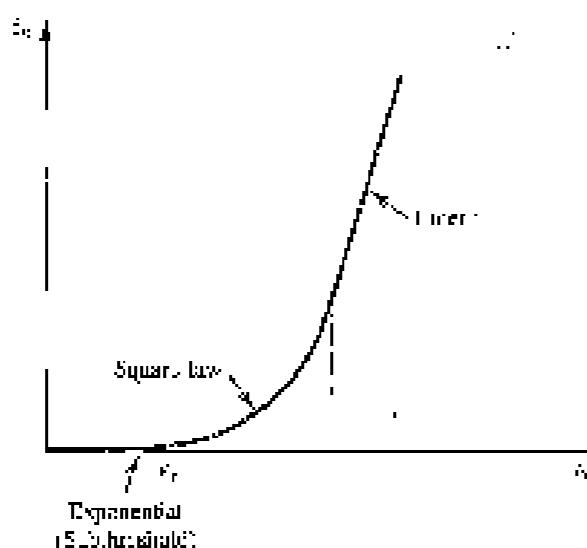


FIGURE 14.36 Typical I_D - V_{DS} characteristic for a power MOSFET.

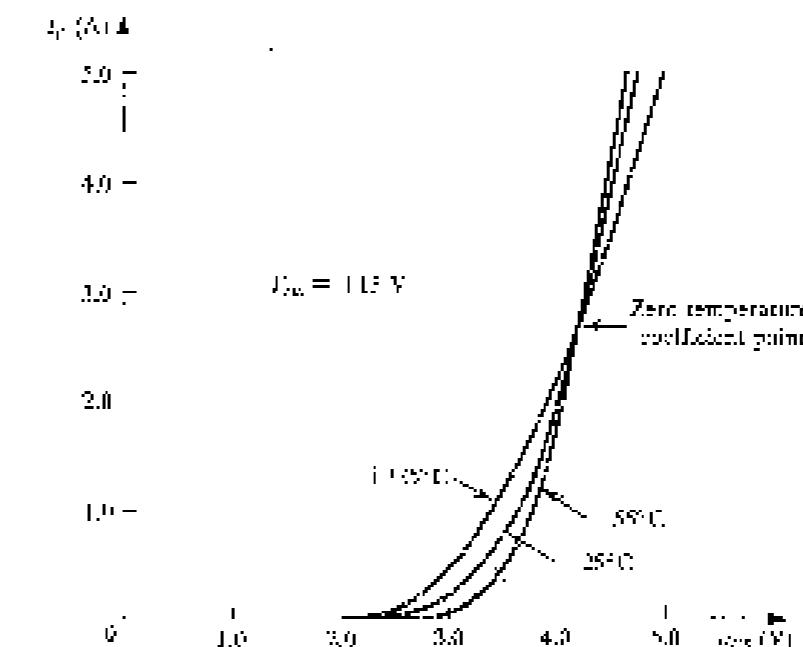


FIGURE 14.37 The I_D - V_{DS} characteristic curve of a power MOS transistor (IRL 630), collected at case temperatures of -25°C, +25°C, and +125°C. (Courtesy of Intertec, Inc.)

14.9.3 Temperature Effects

Of considerable interest in the design of MOS power circuits is the variation of the MOSFET characteristics with temperature, illustrated in Fig. 14.37. Observe that there is a value of V_{DS} in the range of 4 V to 6 V for most power MOSFETs at which the temperature coefficient of I_D is zero. At higher values of V_{DS} , I_D exhibits a negative temperature coefficient. This is a significant property. It implies that a MOSFET operating beyond the zero-temperature-coefficient point does not suffer from the possibility of thermal runaway. This is not the case, however, at low currents (i.e., lower than the zero-temperature-coefficient point). In the (relatively) low-current region, the temperature coefficient of I_D is positive, and the power MOSFET can easily suffer thermal runaway (with unhappy consequences). Since class AB output stages are biased at low currents, care must be provided to guard against thermal runaway.

The reason for the positive temperature coefficient of I_D at low currents is that $\alpha_{DS} = (dI_D/dT)/I_D$ is relatively low, and the temperature dependence is dominated by the negative temperature coefficient of V_t (in the range of -3 mV/C to -6 mV/C) which causes α_{DS} to rise with temperature.

14.9.4 Comparison with BJTs

The power MOSFET does not suffer from second breakdown, which limits the safe operating area of BJTs. Also, power MOSFETs do not require the large dc base-drive currents of power BJTs. Note, however, that the driver stage in a MOS power circuit should be capable of supplying sufficient current to charge and discharge the MOSFET's large and nonlinear input capacitance in the time allotted. Finally, the power MOSFET features, in general, a

higher speed of operation than the power BJT. This makes MOS power transistors especially suited to switching applications—for instance, in motor-control circuits.

14.9.5 A Class AB Output Stage Utilizing MOSFETs

As an application of power MOSFETs, we show in Fig. 14.38 a class AB output stage utilizing a pair of complementary MOSFETs and employing BJTs for biasing and in the driver stage. The latter consists of complementary Darlington emitter followers formed by Q_1 through Q_4 , and has the low output resistance necessary for driving the output MOSFETs at high speeds.

Of special interest in the circuit of Fig. 14.38 is the bias circuit utilizing two V_{GS} multipliers formed by Q_3 and Q_4 and their associated resistors. Transistor Q_2 is placed in direct thermal contact with the output transistors; this is achieved by simply mounting Q_2 on their common heat sink. Thus, by the appropriate choice of the V_{GS} multiplication factor of Q_3 , the drain voltage V_{DS} (between the gates of the output transistors) can be made to decrease with temperature at the same rate as that of the sum of the threshold voltages ($V_{th} + V_{th2}$)

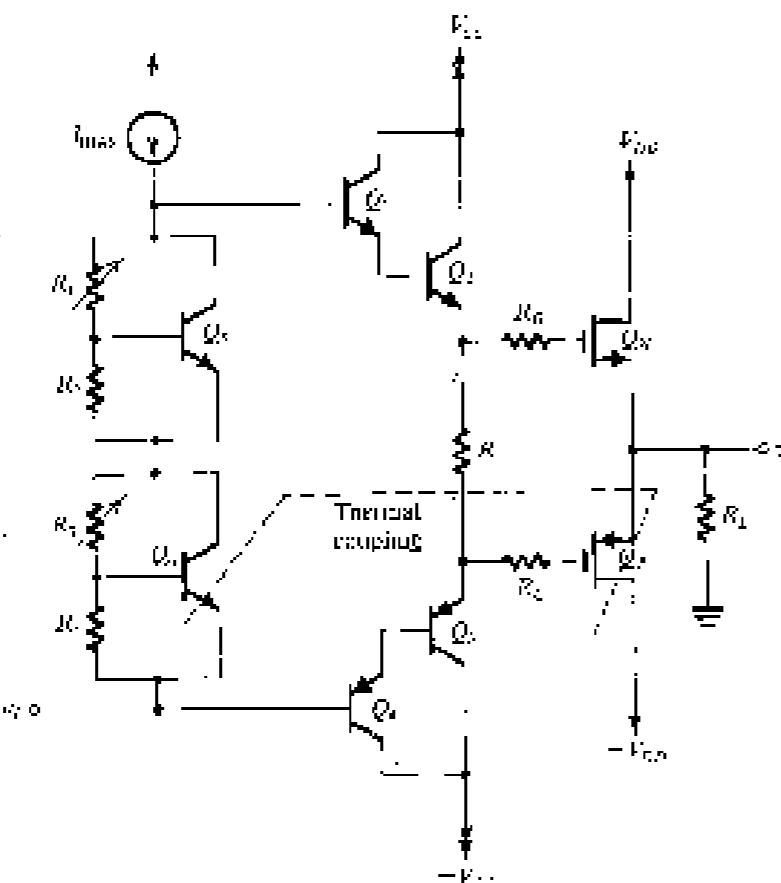


FIGURE 14.38 A Class AB amplifier with MOS output transistors and BJT drivers. Resistor R_2 is adjusted to provide temperature compensation so that R_1 is adjusted to yield the desired value of quiescent current in the output transistors. Resistors R_5 are used to suppress parasitic oscillations at high frequencies—typically, $R_5 = 100\ \Omega$.

of the output MOSFETs. In this way the quiescent current of the output transistors can be stabilized against temperature variations.

Analytically, V_{DS} is given by

$$V_{DS} = \left(1 - \frac{R_1}{R_2}\right)V_{GS} + \left(1 - \frac{R_3}{R_4}\right)V_{GS} - 2V_{BE} \quad (14.48)$$

Since V_{GS} is feedbackly coupled to the output voltages while the other BJTs remain at constant temperature, we have

$$\frac{\partial V_{DS}}{\partial T} = \left(1 - \frac{R_1}{R_2}\right)\frac{\partial V_{GS}}{\partial T} \quad (14.49)$$

which is the relationship needed to determine R_2/R_1 so that $\partial V_{DS}/\partial T = \partial V_{GS}/\partial T = (V_{GS})\partial T$. The other V_{GS} multiplier is then adjusted to yield the value of V_{GS} required for the desired quiescent current in Q_1 and Q_2 .

EXERCISES

- 14.18 For the circuit in Fig. 14.38, find the value of R_2 that provides temperature stabilization of the quiescent current. Assume that the BJTs have a temperature coefficient of $2\text{ mV}/^\circ\text{C}$ and that $\partial V_{BE}/\partial T = 2\text{ mV}/^\circ\text{C}$. Ans. 2
- 14.19 For the circuit in Fig. 14.38 assume that the BJTs have a temperature coefficient of $2\text{ mV}/^\circ\text{C}$ and the MOSFETs have $10\text{ mV}/^\circ\text{C}$ and that $\partial V_{GS}/\partial T = 10\text{ mV}/^\circ\text{C}$. If a quiescent current of 100 mA is desired, determine the drain voltage and $2\text{ mV}/^\circ\text{C}$ in the driver stage. Find V_{GS} , V_{GS2} , R_1 and R_2 . (See the values of R_1 and R_2 in Exercise 14.18.)
- Ans. 5.32 V ; 6.61 V ; $332\text{ }\Omega$; $9.5\text{ }\Omega$

14.10 SPICE SIMULATION EXAMPLE

We conclude this chapter by presenting an example that illustrates the use of SPICE in the analysis of output circuits.

CLASS B OUTPUT STAGE

We investigate the operation of the class B output stage whose Capture schematic is shown in Fig. 14.39. For the power transistors, we use the discrete BJTs MJE245 and MJE253 (from ON Semiconductor), which are rated for a maximum continuous collector current $I_{Cmax} = 4\text{ A}$ and a maximum collector-emitter voltage of $V_{CEmax} = 100\text{ V}$. To perform comparison with the hand analysis performed in Example 14.1, we use, in the simulation, component and voltage values identical

In PSpice, we have created BJT models for these power transistors based on the values of the SPICE model parameters available on the data sheets available from ON Semiconductor. Readers can find these in ModelLib (MJE245 and MJE253) in the ATLAS library, or ModelLib is available on the CD accompanying this book as well as at www.ednsearch.com.

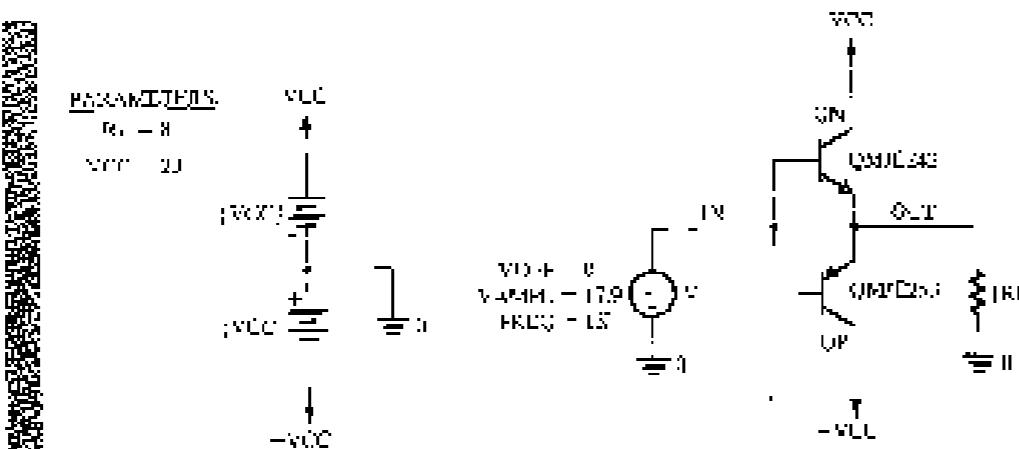


FIGURE 14.39 Capture schematic of the class-B output stage in Example 14.4.

on class-B those of the circuit designed in Example 14.1. Specifically, we use a load resistance of $8\ \Omega$, an input sine-wave signal of 17.9 V peak and 1-kHz frequency, and 21-V power supplies. In PSpice, a transient-analysis simulation is performed over the interval 0 ms to 7 ms, and the waveforms of various node voltages and branch currents are plotted. In this example, Probe (the graphical interface in PSpice) is utilized to compute various power-dissipation values. Some of the resulting waveforms are displayed in Fig. 14.40. The upper and middle graphs show the load voltage and current, respectively. The peak voltage amplitude is 16.9 V, and the peak current

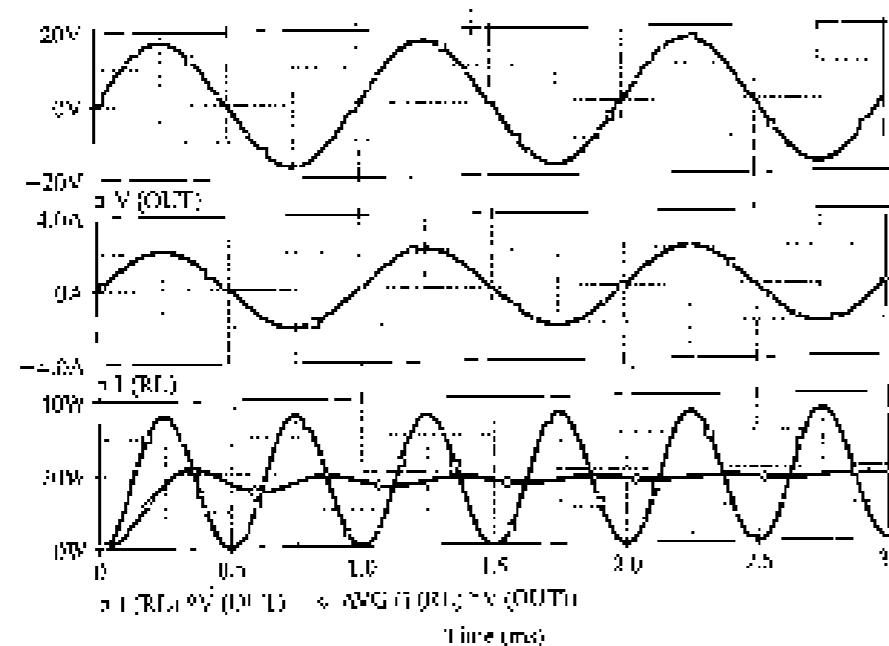
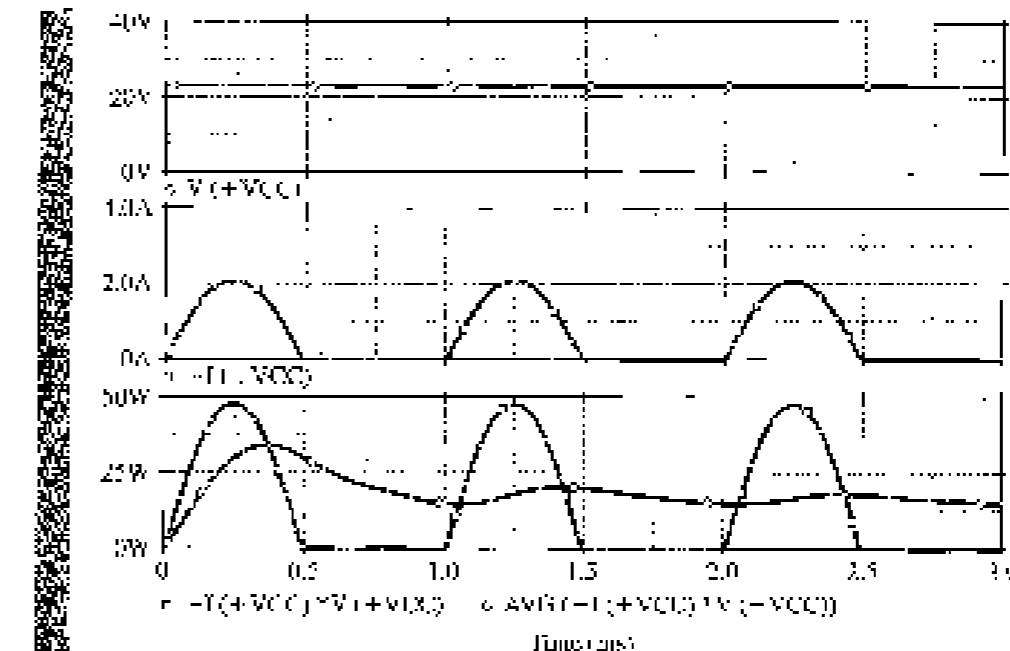


FIGURE 14.40 Several waveforms associated with the class-B output stage (shown in Fig. 14.39) when excited by a 17.9 V, 1-kHz sinusoidal signal. The top graph displays the voltage across the load resistance, excited by a 17.9 V, 1-kHz sinusoidal signal. The middle graph displays the load current, and the bottom graph displays the instantaneous and average power dissipated by the load.

FIGURE 14.41 The voltage (top graph), current (middle graph), and instantaneous and average power (bottom graph) supplied by the positive voltage supply ($+V_{CC}$) in the circuit of Fig. 14.39.

amplitude is 2.1 A. If one looks carefully, one can observe that both exhibit a sawtooth distortion. The bottom graph displays the instantaneous and the average power dissipated in the load resistance as computed using Probe by multiplying the voltage and current values to obtain the instantaneous power, and taking a running average for the average load power P_2 . The transient behavior of the averaged load power, which eventually settles into a quasi-constant steady-state of about 17.6 W, is an artifact of the PSpice algorithm used to compute the running average of a waveform.

The upper two graphs of Fig. 14.41 show the voltage and current waveforms, respectively, of the positive supply, $+V_{CC}$. The bottom graph shows the instantaneous and average power supplied by $+V_{CC}$. Similar waveforms can be plotted for the negative supply, $-V_{CC}$. The average power provided by each supply is found to be given 15 W, for a total supply power P_S of 30 W. Thus, the power conversion efficiency can be calculated to be

$$\eta = P_S / P_T = \frac{30\text{W}}{60\text{W}} = 50.0\%$$

Figure 14.42 shows plots of the voltage, current, and power waveforms associated with transistor Q_2 . Similar waveforms can be obtained for Q_1 . As expected, the voltage waveform is a sinusoid, and the current waveform consists of anti-sinusoids. The waveform of the instantaneous power, however, is rather unusual. It indicates the presence of some distortion as a result of driving the transistors rather hard. This can be verified by reducing the amplitude of the input signal. Specifically, by reducing the amplitude to about 17 V, the "dip" in the power waveform vanishes. The average power dissipated in each of Q_1 and Q_2 can be computed by Probe and are found to be approximately 8 W.

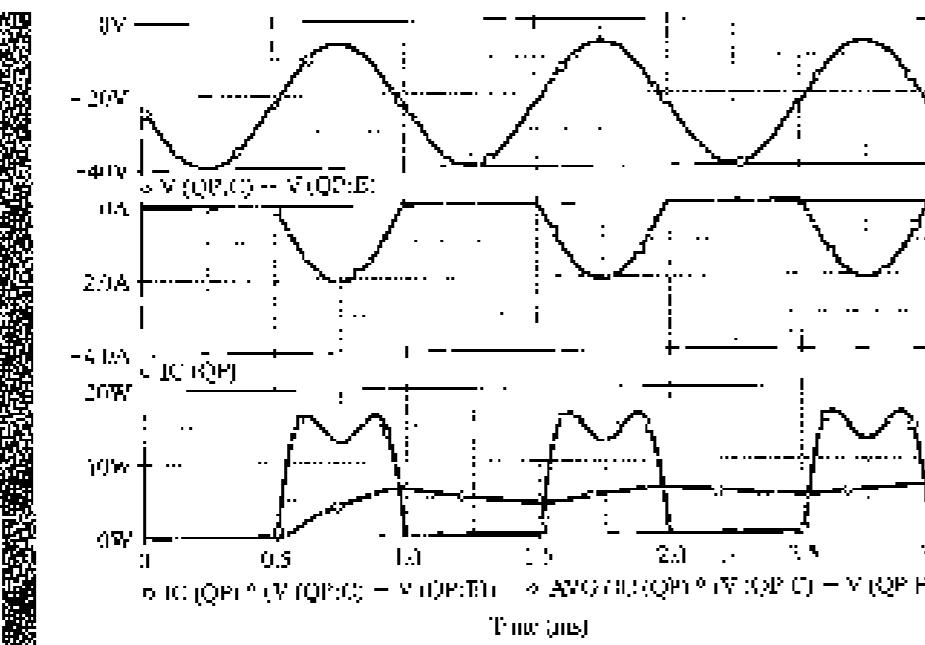


FIGURE 14.42 Waveforms of the voltage across the output load, the dc power dissipated in the power transistor Q_1 , and power dissipated in the power transistor Q_2 for the circuit shown in Fig. 14.39.

TABLE 14.1 Power and Efficiency Calculated with the Circuit of Figure 14.39

Power/Efficiency	Equation	Hand Analysis (Example 14.1)	Pspice	Error % ^a
P_1	$\frac{2}{\pi} I_{Q1}^2 R_L$	31.2 W	30.0 W	-4
P_2	$\frac{2 I_{Q2} V_{CE2}}{\pi R_L} + \frac{V_{CE2}^2}{2 R_L}$	13.0 W	12.4 W	+4.6
P_3	$\frac{V_{CE1}^2}{2 R_L}$	18.2 W	17.6 W	+3.4
η	$\frac{P_1}{P_1 + P_2 + P_3}$	56.3%	55.6%	+1.3

^aRelative percentage difference between the values predicted by hand and by PSpice.

Table 14.1 provides a comparison of the results from from the PSpice simulation and the corresponding values obtained using hand analysis in Example 14.1. Observe that the two sets of results are quite close.

To investigate the crossover distortion further, we present, in Fig. 14.43 a plot of the voltage transfer characteristic (VTC) of the class B output stage. This plot is obtained through a dc analysis simulation with V_{DC} swept over the range -15 V to -10 V in 1.0 mV increments. Using

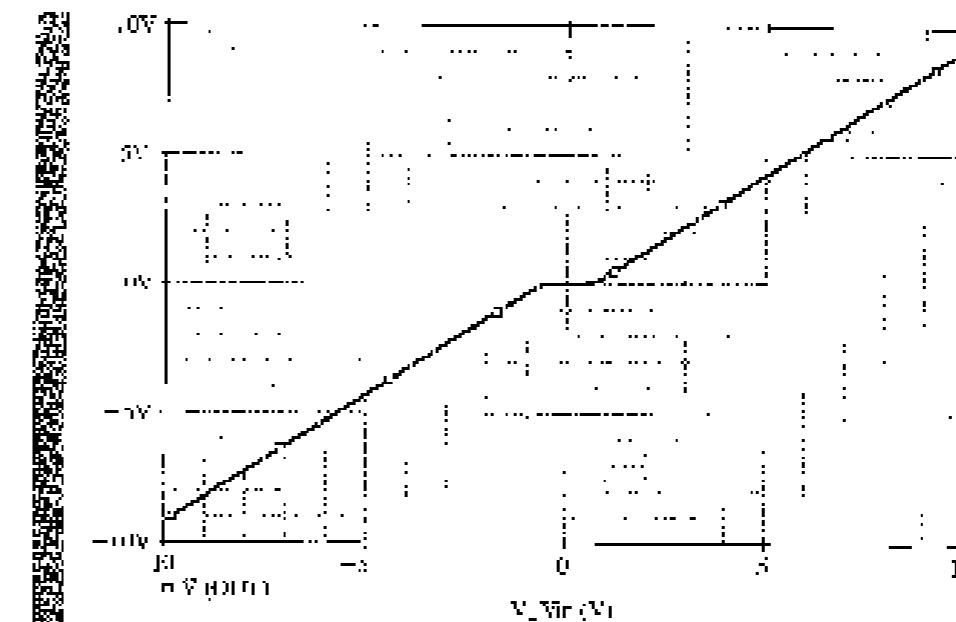


FIGURE 14.43 Time-domain characteristic of the class B output stage of Fig. 14.39.

probe we determine that the slope of the V_{DC} is nearly unity and that the dead band extends from -0.60 to -0.58 V . The error of the crossover distortion can be quantified by performing a Fourier analysis on the output voltage waveform in PSpice. This analysis decomposes the waveform generated through a transient analysis into its Fourier-series components. Further, PSpice computes the total harmonic distortion (THD) of the output waveform. The results obtained from the simulation output file are as follows:

ANALYZED COEFFICIENTS OF TRANSIENT RESPONSE (V_{DC}, mV)					
DC COMPONENT = 1.525223e+01					
L000000.0	EFFICIENCY (%)	POWER (W)	VOLTS (V)	AMPS (A)	VOLTS (V)
1	1.000000e+00	1.525223e+01	1.525223e+01	1.000000e+00	1.525223e+01
2	2.000000e+00	9.126470e+00	9.126470e+00	2.000000e+00	9.126470e+00
3	3.000000e+00	5.750000e+00	5.750000e+00	3.000000e+00	5.750000e+00
4	4.000000e+00	4.074e-00	4.074e-00	4.000000e+00	4.074e-00
5	5.000000e+00	2.7787e-00	2.7787e-00	5.000000e+00	2.7787e-00
6	6.000000e+00	2.000000e-00	2.000000e-00	6.000000e+00	2.000000e-00
7	7.000000e+00	1.428571e-00	1.428571e-00	7.000000e+00	1.428571e-00
8	8.000000e+00	1.000000e-00	1.000000e-00	8.000000e+00	1.000000e-00
9	9.000000e+00	6.666667e-01	6.666667e-01	9.000000e+00	6.666667e-01
10	1.000000e+01	4.000000e-01	4.000000e-01	1.000000e+01	4.000000e-01

THD = 14.9031e-01 = 14.9031% = 2.140217e-01 = 0.2140217

These Fourier components are used to find the line spectrum shown in Fig. 14.44. We note that the output waveform is rather rich in odd harmonics and that the resulting THD is rather high (2.14%).

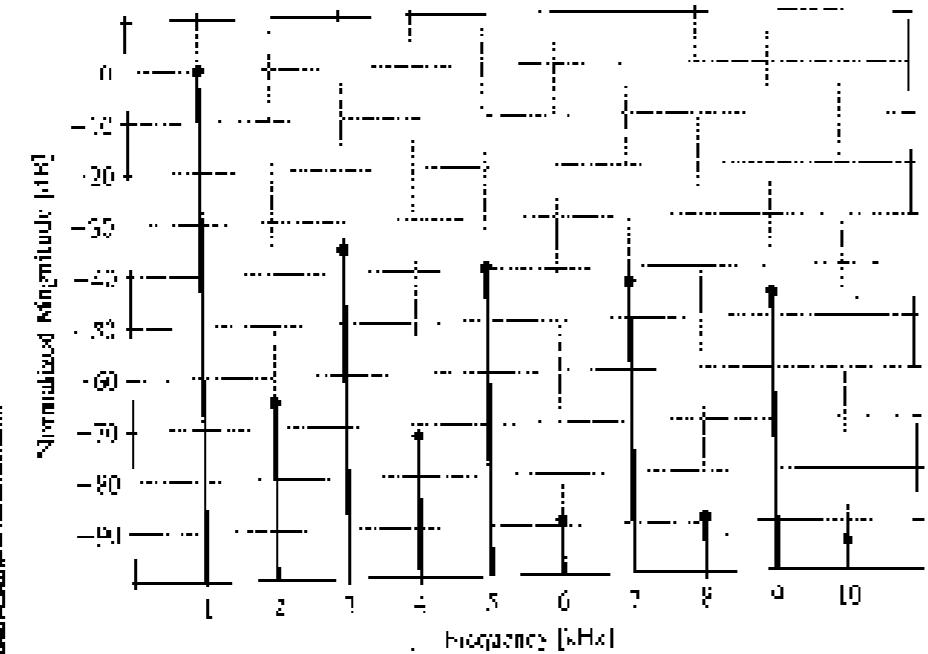


FIGURE 14.44 Log-log plot of normalized magnitude vs frequency for the class B output stage in Fig. 14.39.

SUMMARY

- Output stages are classified according to the transistor conduction angles: class A (>90°), class AB (slightly more than 180°), class B (180°), and class C (less than 180°).
- The most common class A output stage is the emitter-follower. It is biased at a current greater than the peak load current.
- The class A output stage dissipates its maximum power under no-load conditions ($\beta = 0$). To achieve a maximum power conversion efficiency of 50%,
- The class B stage is biased at zero current, and thus of no use as a power amplifier.
- The class B stage can achieve a power conversion efficiency as high as 78.5%. It dissipates its maximum power for $V_o = 12 \text{ V}$.
- Two class B stages reduce total crossover distortion.
- The class AB output stage is biassing the transistors: the two transistors conduct for small ($< 180^\circ$) signals, and crossover distortion is virtually eliminated.
- Except for class A and class AB, quasi-symmetrical power dissipation, the power relationships of the class AB stages are similar to those in class B.
- To guard against the possibility of thermal runaway, the bias voltage of the class AB circuit is made to vary with temperature in the active transistors—does V_B of the output transistors
- To determine the current of T_{out} from the β , the output power devices are usually mounted on heat sinks. The maximum power that can safely dissipate in a device is given by
$$P_{max} = \frac{T_{max} - T_A}{R_{th} + R_{ds(on)} \cdot \beta_{avg}}$$
- where T_{max} and R_{th} are specified by the manufacturer. While R_{th} and β_{avg} depend on the heat sink design,
- Use of the Darlington configuration in the class AB output stage reduces the base current drive requirement. In heterojunction circuits, the compound-junction configuration is commonly used.

- Output stages are usually equipped with circuitry that in the event of a short circuit turns on and limit the base-current drive, and hence the output current, of the output transistors.
- Power amplifiers consist of a two-stage voltage amplifier cascade with a high-power output stage. Overall feedback is applied either on-chip or externally.
- The buffer amplifier (preamplifier) provides access to a floating load, a peak-to-peak output voltage which is

twice that possible from a classic amplifier with a ground load.

- The DMOS transistor is a short-channel power device capable of high-side-current and high-voltage operation.
- The drain current of a power MOSFET exhibits a positive temperature coefficient at low currents, and thus the device can suffer thermal runaway. At high currents, the term in the α -term of β_{DSAT} is negative.

PROBLEMS

SECTION 14.2: CLASS A OUTPUT STAGE

- 14.1 A class A emitter follower, biased using the circuit shown in Fig. 14.3, uses $V_{DD} = 5 \text{ V}$, $R = R_1 = 1 \text{ k}\Omega$, with all transistors (including Q_2) identical. Assume $V_{BE} = 0.7 \text{ V}$, $V_{DS(on)} = 0.1 \text{ V}$, and β to be very large. For linear operation, what are the upper and lower limits of output voltage, and the corresponding input? How do these values change if the emitter-base junction area of Q_1 is reduced to one-half that of Q_2 (half as $R_{DS(on)}$)?

- 14.2 A source-follower circuit using NMOS transistors is constructed following the pattern shown in Fig. 14.3. All three transistors used are trenchable, with $V_t = 1 \text{ V}$ and $\mu_s C_{ox} W/L = 20 \text{ mA/V}^2$; $V_{DD} = 5 \text{ V}$, $R = R_1 = 1 \text{ k}\Omega$. For linear operation, what are the upper and lower limits of the output voltage, and the corresponding inputs?

- 14.3 Using the following β_{DSAT} curve shown in Fig. 14.2 with $\pm 9 \text{ V}$ supplies, provide a class A capable of $\pm 5 \text{ V}$ outputs with a $1\text{-k}\Omega$ load, using the smallest possible load supply voltage. You are provided with four identical, high- β JFETs and a resistor of your choice.

- 14.4 An emitter follower using the circuit of Fig. 14.2, for which the output voltage range is $\pm 5 \text{ V}$, is required using $V_{DD} = 10 \text{ V}$. The circuit is to be designed such that the current variation in the emitter-follower transistor is no greater than a factor of 10, nor load resistance is less than $100 \text{ }\Omega$. What is the value of R (neglecting the incremental voltage gain of the resulting follower)? $V_t = -0.5 \text{ V}$, and $-V_t = 10 \text{ mA}$ (max). What is the percentage change in gain over this range of V_t ?

- 14.5 Consider the operation of the following circuit of Fig. 14.2 for which $R_1 = V_{DD}/I_1$, when driven by a square wave such that the output ranges from $+V_0$ to $-V_0$. Neglecting

Fig. 14.5, find the minimum value of the equivalent of Fig. 14.2 for $v_{in}(t)$, and p_{avg} . Repeat for a symmetric output that has peak levels of $\pm V_{DD}/2$. What is the average power dissipation in Q_1 in each case? Compare these results to those for sine waves of peak amplitude V_{DD} and $V_{DD}/2$, respectively.

- 14.6 Consider the situation described in Problem 14.5 for square-wave outputs having peak-to-peak values of $2V_0$, and $V_{DD} + 1$ for sine waves of the same peak-to-peak values. Find the associated power loss in the current-source transistor Q_2 .

- 14.7 Reconsider the situation described in Exercise 14.4 for supplies of $\pm V_{DD}$ —specifically 20 V , 12 V , 10 V , and 5 V . Assume $V_{BE(on)}$ is nearly zero. What is the power-conversion efficiency in each case?

- 14.8 The BiCMOS follower shown in Fig. P14.8 uses devices for which $V_{BE} = 0.7 \text{ V}$, $V_{DS(on)} = 0.3 \text{ V}$, $\mu_s C_{ox} W/L = 20 \text{ mA/V}^2$.

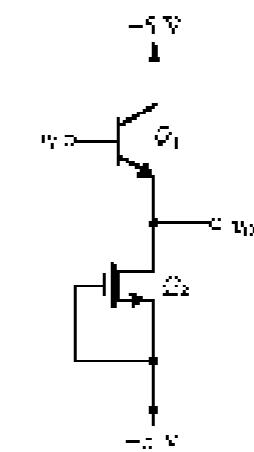


FIGURE P14.8

and $V_{DD} = 2\text{ V}$, for linear operation, what is the range of output voltages obtained with $R_L = 100\text{ }\Omega$? With $R_L = 100\text{ }\Omega$? What is the smallest load resistor allowed for which a 1-V peak sine-wave output is available? What is the corresponding power-conversion efficiency?

SECTION 14.3: CLASS B OUTPUT STAGE

14.10 Consider the circuit of a complementary-BJT class B output stage. For what amplitude of input signal does the crossover distortion represent a 10% rise in peak amplitude?

14.11 Consider the class B output stage with a class B output stage shown in Fig. 14.9. For the amplifier, $\beta_1 = \beta_2 = 100$ mA. Derive an expression for v_o versus v_i assuming that $V_{DD} = 12\text{ V}$. Sketch the transfer characteristic versus v_i to compare it with that without feedback.

14.12 Consider the class B output stage using enhancement-mode MOSFETs shown in Fig. 14.11. Let the devices have $V_t = 1\text{ V}$ and $g_m \cdot R_{DS} = 200\text{ mA/V}^2$. With a 10-kHz sine-wave input of 5-V peak and a 1-k Ω value of load resistance, what peak current would you expect? What fraction of the sine wave voltage does the crossover distortion represent? For what value of load resistor is the peak output voltage reduced to half its input?

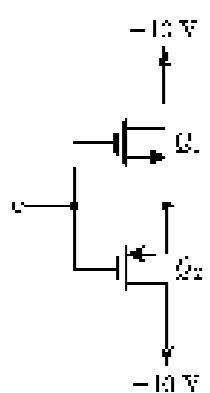


FIGURE P14.11

14.13 Consider the complementary-BJT class B output stage in Fig. 14.9. Neglect the effects of finite V_{BE} and V_{CE} . For a 12-V power supply and a 100- Ω load resistance, what is the maximum sine-wave output power available? What is the power conversion efficiency? For output signals of half this amplitude, find the output power, the supply power, and the power conversion efficiency.

14.14 A class AB output stage similar to that in Fig. 14.11 is to utilize a single supply of +10 V and biased at $V_B = 0\text{ V}$, to be positively coupled to a 100- Ω load. For transistors for which $|V_{BE}| = 0.7\text{ V}$ at 1 mA and for a bias voltage $V_{BB} = 1.4\text{ V}$, what quiescent current results? For a step change in output from 0 to 1 V, what input step is required? Assume a transistor saturation voltage of 250 mV and the largest possible positive going and negative-going steps at the output.

smallest range of load resistance R_L can be tolerated if operation is always in full output voltage? If operation is allowed only to the full output voltage, what is the smallest load permitted? What is the greatest possible output power available, in each case?

14.15 A class B output stage is required to deliver an average power of 100 W to a 10- Ω load. The power-supply voltage is +12 V, greater than the corresponding peak-to-peak output voltage. Determine the power-supply voltage required for the required gain in the appropriate case that the peak current from each supply, the total supply power, and the power-conversion efficiency. Also, determine the minimum possible power dissipation in each transistor for a sine-wave input.

14.16 Consider the class B output stage with a square-wave current voltage of amplitude I_0 across a load R_L are employing power-supply V_{DD} having the effects of I_{DSAT} , V_{DS} , and V_{GS} , determine the load power, the supply power, the power-conversion efficiency, the maximum attainable power-conversion efficiency, and the corresponding value of I_0 , if the maximum available load power. Also find the value of I_0 at which the power dissipation in the main driver reaches its peak, and the corresponding value of power-conversion efficiency.

SECTION 14.4: CLASS AB OUTPUT STAGE

14.17 Design a class AB MOS output stage to be considered. The available devices have $|V_t| = 1\text{ V}$ and $g_m \cdot R_{DS} = 200\text{ mA/V}^2$. What value of gate-to-gate bias voltage V_{BG} is required at most for the incremental output resistance in low-current state to 10 k Ω ?

14.18 A class AB output stage, resembling that in Fig. 14.11 but utilizing a single supply of +10 V and biased at $V_B = 0\text{ V}$, is to be positively coupled to a 100- Ω load. For transistors for which $|V_{BE}| = 0.7\text{ V}$ at 1 mA and for a bias voltage $V_{BB} = 1.4\text{ V}$, what quiescent current results? For a step change in output from 0 to 1 V, what input step is required? Assume a transistor saturation voltage of 250 mV and the largest possible positive going and negative-going steps at the output.

SECTION 14.5: BIASING THE CLASS AB CIRCUIT

14.19 Consider the diode-biased class AB circuit of Fig. 14.11. For $\beta_1 = 100$ mA. Find the relative value (α) that should be used for the output devices (in comparison to the biasing devices) to obtain an output resistance of 1000 ohms.

B14.20 A class AB output stage using a two-diode bias network as shown in Fig. 14.11 utilizes diodes having the same junction area as the output transistors. For $V_{DD} = 10\text{ V}$, $\beta_1 = 100$ mA, $R_L = 100\text{ }\Omega$, $R_D = 50\text{ }\Omega$ and $|V_{DSAT}| = 0\text{ V}$, what is the quiescent current? What is the largest possible positive and negative output signal level? To achieve a positive peak output level equal to the negative peak level, what value of β_2 is needed? If β_2 is too changed? What value of β_2 is needed if β_1 is held at 50? For this value, what does β_2 become?

***14.21** A class AB output stage using a two-diode bias network as shown in Fig. 14.11 utilizes diodes having the same junction area as the output transistors. At a room temperature of about 20°C, the quiescent current is 1 mA and $|V_{DS}| = 0.6\text{ V}$. Through a manufacturing error, the $\beta_1 = \beta_2$ coupling network, the output transistors and the diode-coupled transistors is smaller. After some output activity, the output devices heat up to 70°C while the biasing devices remain at 20°C. β_1 , while the V_{DS} of each one of remains unchanged, the quiescent current in the output devices increases. To calculate the new quiescent value, recall that there are two effects: β_1 increases by about 10%/ $^{\circ}\text{C}$; and V_{DS} decreases with $T = (273)^{\circ}\text{C}$ – temperature in $^{\circ}\text{C}$, and $V_{DS} = 25\text{ mV}$ only at 20°C. However, you may assume that β_2 remains almost constant. The assumption is based on the fact that β increases with temperature but decreases with current (see Fig. 5.3). What is the new value of β_2 ? If the power-supply is +20 V, what additional power is dissipated? If thermal runaway occurs, and the temperature of the output transistors increases by 10°C for every watt of additional power dissipation, what additional temperature increase is likely to result?

14.22 Figure P14.22 shows a MOSFET class AB output stage. All the sources have $|V_t| = 1\text{ V}$ and $i_s = n_s = 0\text{ A}$.

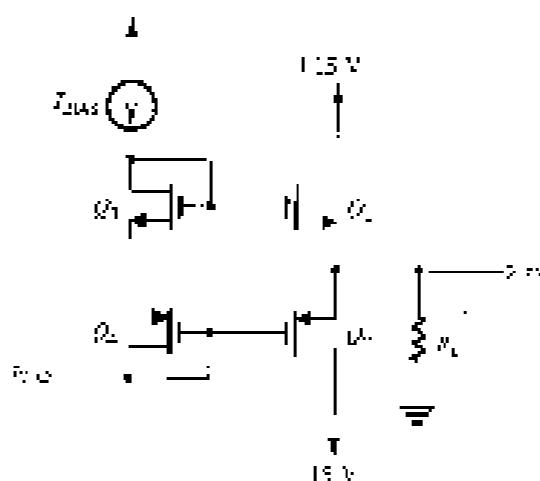


FIGURE P14.22

where $\beta = \alpha/\sqrt{4\pi L}$ is the MOSFET transconductance parameter; A_{on} , $A_c = 2\text{ mA/V}^2$. For $\beta_{Q1} = 100$ mA and $R_L = 100\text{ }\Omega$ find the value of α that results in a small-signal gain of 0.99 for input voltages around zero, and the corresponding value of i_s .

14.23 Repeat Example 14.3 for the situation in which the peak positive output is less than 200 mA. Use the same general approach to safety margins. What is the value of R_L and R_S you have chosen?

***14.24** A FET multiplier is designed with equal resistances for continual operation at a terminal current of 1 mA, with half the current flowing in the bias network. The initial design is based on $\beta = \infty$ and $V_{DD} = 0.7\text{ V}$ at 1 mA.

- Find the required new bias values and the terminal voltage.
- Find the terminal voltage that results when the terminal current increases to 2 mA. Assume $\beta = \infty$.
- Repeat (i) but use the terminal current becomes 0.5 mA.
- Repeat (i) using the more realistic value of $\beta = 100$.

SECTION 14.6: POWER BJTs

14.25 A particular transistor having a thermal resistance $\theta_{JC} = 2\text{ }^{\circ}\text{C/W}$ is operating at an ambient temperature of 20°C with a collector-emitter voltage of 20 V. If long-life requires a maximum junction temperature of 150°C, what is the safe operating device power rating? What is the 2-volt average collector current that should be considered?

14.26 A particular transistor has a power rating of 200 mW, and it rises from a junction temperature of 100°C. What is the thermal resistance? What is its power rating when operating at an ambient temperature of 100°C? What is the junction temperature when dissipating 100 mW at an ambient temperature of 50°C?

14.27 A power transistor operating at an ambient temperature of 50°C, and an average emitter current of 3A, dissipates 30 W. If the thermal resistance of the transistor is known to be less than 40°C/W, what is the greatest junction temperature you can expect? If the transistor $V_{CE(on)} = 1\text{ V}$ at a primary collector current of 3 A at a junction temperature of 25°C is 0.80 V, what value V_{CE} would you expect under normal operating conditions? (Use a temperature coefficient of $-2\text{ mV/}^{\circ}\text{C}$.)

14.28 For a particular application of the transistor specified in Example 14.4, α and β are essential. To improve reliability the maximum junction temperature is to be limited to 100°C. What are the consequences of this decision for the conditions specified?

14.29 A power transistor is specified to have a maximum junction temperature of 120°C. When the device is mounted on the junction temperature with a heat sink, the case temperature

is found to be 60°C. If one is attached to the load sink with a heat sinking resistance $R_h = 0.5\text{ }^{\circ}\text{C/W}$ and the thermal resistance of the heat sink $\theta_{hs} = 0.1^{\circ}\text{C/W}$, at 25°C ambient temperature is 50°C \Rightarrow Let us do power being dissipated in the device? What is the thermal resistance of the device, θ_{ds} , from junction to case?

14.30 A power transistor for which $T_{Jmax} = 180^{\circ}\text{C}$ can dissipate 50 W at a case temperature of 50°C. It is connected to a heat sink using an insulating wedge for which the thermal resistance is 0.7°C/W, after how much temperature increase is necessary to ensure safe operation at 50°C? Assume an ambient temperature of 35°C, what junction thermal resistance is required? If, for a particular extruded-aluminum-finned heat sink, the thermal resistance in still air is 4.5°C/W per centimeter of length, how long a heat sink is needed?

14.31 An npn power transistor operating at $i_c = 10\text{ mA}$ is found to have a base current of 0.5 A and an inverse β base input resistance of 0.05 Ω. What value of r_s do you suspect? (At this high current density $\alpha = 1.1$)

14.32 A base spreading resistance (r_s) of 0.8 Ω has been measured for an npn power transistor operating at $i_c = 7\text{ mA}$, with a base-emitter voltage of 1.18 V and a base current of 150 μA. Assuming that $\alpha = 3$ for high-current density operation, a 3-V base-emitter voltage would you expect for operation at $i_c = 7\text{ mA}$?

SECTION 14.7: VARIATIONS ON THE CLASS AB CONFIGURATION

14.33 Use the results given in the answers to Exercise 14.31 to determine the input current of the circuit in Fig. 14.21 for $i_c = 3$ and +10 V with tripling and 100-mA loads.

14.34 Consider the circuit of Fig. 14.21 in which Q_1 and Q_2 are matched, and Q_3 and Q_4 are matched but have twice the junction area of the others. For $V_{BE} = 10\text{ mV}$, find values for resistors R_1 through R_4 which allow for a base current of at least 10 mA in Q_1 and Q_2 at $v_o = +5\text{ V}$ (when a load demands it) without more than a 2-in-1 variation in currents in Q_1 and Q_2 , and a no-load quiescent current of 40 mA in Q_3 ($\beta_{31} > 150$ and $\beta_{41} \geq 30$). Use input voltage around 0 V, calculate the output resistance of the circuit, follow it driven by a source having zero resistance. For an input voltage of +10 V and a load resistance of 2 Ω, what output voltage results? (Q_3 and Q_4 have $|V_{AO}|$ of 0.7 V at a current of 10 mA and an inverse $\beta = 1$.)

14.35 A circuit resembling that in Fig. 14.21 uses four matched transistors for which $|V_{AO}| = 0.1\text{ V}$, $\alpha = 0.2\text{ mA/V}$, $n = 1$, and $\beta > 50$. Resistors R_1 and R_2 are replaced by 2 kΩ constant-current sources, and $R_3 = R_4 = 0$. What quiescent current flows in the output transistors? What bias current flows in the bases of

the input transistors? Where does all the DC work in i_c as input current (the offset current) for a 1% mismatch of 10%? For a load resistance $R_L = 100\text{ }\Omega$, what is the input resistance? What is the small-signal voltage gain?

14.36 Consider a Dizophone (decoupled transistors formed from two npn HBTs for which $\beta > 50$, $V_{AO} = 0.7\text{ V}$, $\alpha = 0.1\text{ mA}$, and $n = 1$). For operation at 10 mA, what values would you expect for R_1 , R_2 , R_3 , R_4 , and R_L ?

14.37 To the circuit in Fig. 14.27 in which two transistors have $V_{BE} = 0.7\text{ V}$ and $\beta = 100$, find i_b , i_{c1} , i_{c2} , and R_{out} .

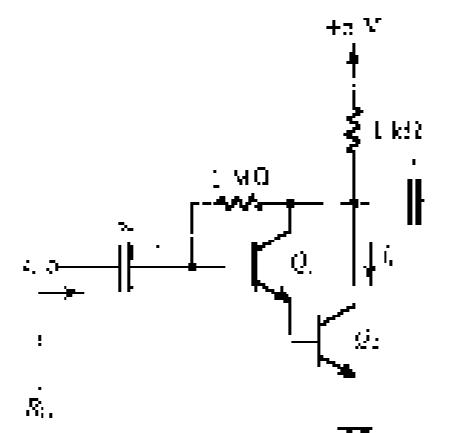


FIGURE P14.37

14.38 The DUTs used in Fig. P14.38 have $\beta = 10$, $\beta = 0.0$, $V_{AO} = 0.7\text{ V}$, and $|V_{AO}| \sim 0.01\text{ V}$.

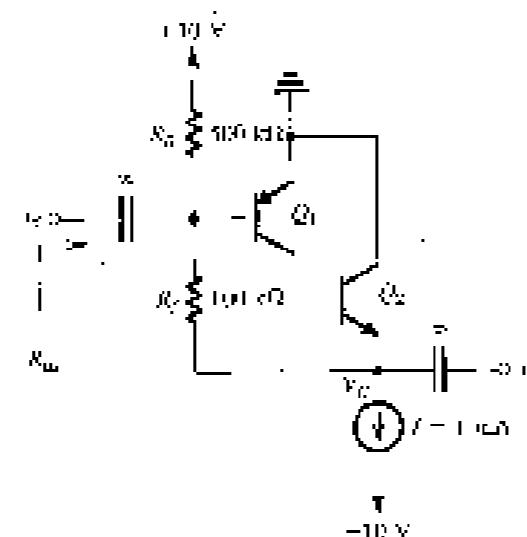


FIGURE P14.38

(a) Find the dc collector current of each transistor and the value of V_{CE} .

(b) Replacing one L-BJT with its h-parameter model, show that

$$\frac{i_b}{i_c} = g_m (V_{BE} - i_c R_s)$$

(c) Find the values of v_{o1}/v_{o2} and A_{v1} .

D*14.39** Consider the complementary-emitter-class AB output stage shown in Fig. 14.27 in which Q_1 and Q_2 are matched transistors with $V_{BE} = 0.7\text{ V}$ at 10 mA and $\beta = 100$, Q_3 and Q_4 have $V_{BE} = 0.7\text{ V}$ at 1-mA currents and $\beta = 100$, and Q_1 has $V_{BE} = 0.7\text{ V}$ at a 1-mA current and $\beta = 10$. All transistors have $n = 1$. Design the circuit for a quiescent current of 2 mA in Q_3 and Q_4 , I_{Q1} that is 100 times the standby bias current in Q_1 , and a current in Q_2 that is nine times that in the associated resistors. Find the values of the input voltage required to produce outputs of $\pm 10\text{ V}$ for a 1-Ω load. Use V_{cc} of 15 V.

14.40 Repeat Exercise 14.13 for a design variation in which transistor Q_3 is increased in size by 5 times of Q_1 , all other conditions remaining the same.

14.41 Repeat Exercise 14.13 for a design in which the limiting maximum output and internal peak currents are 30 mA and 3.0 mA, respectively.

14.42 The circuit shown in Fig. P14.42 operates in a manner analogous to that in Fig. 14.28 to limit the output

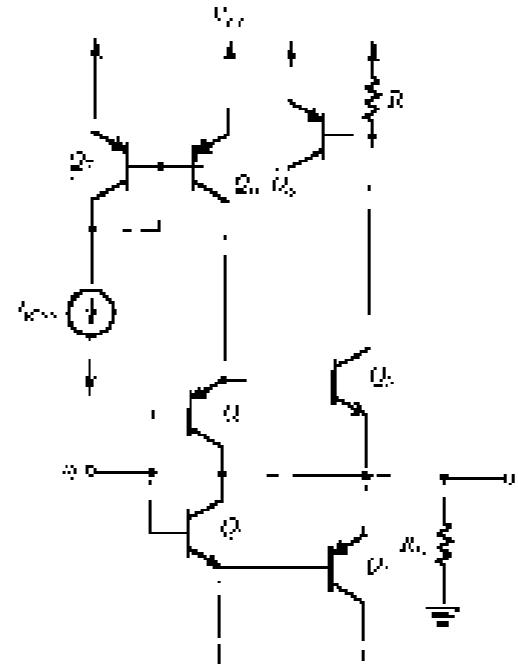


FIGURE P14.42

current from Q_3 (the effect of a short circuit on stage 1 is to keep it bias the anode voltage over the current-limiting resistor R does not appear directly at the output). Find the value of R that causes Q_3 to turn on and absorb all of $I_{Q1} = 2\text{ mA}$ when the current flowing through reaches 150 mA. For $\beta_3 = 10^{10}\text{ A/s}$ and $n = 1$, if the normal peak output current is 100 mA, find the voltage drop across R and the collector current in Q_3 .

14.43 Consider the biotransistor addition circuit shown in Fig. 14.39. At 25°C, Z_1 is a 0.6-V zener diode with a TC of 2 mV/°C, and Q_1 and Q_2 are BJTs that display V_{BE} of 0.7 V at a current of 100 mA and have a TC of 1 mV/°C. Design the circuit so that at 125°C, a current of 100 μA flows in each of Q_1 and Q_2 . What is the current in Q_2 at 25°C?

SECTION 14.8: IC POWER AMPLIFIERS

14.44 In the power-amplifier circuit of Fig. 14.40 two resistors are important in controlling the overall voltage gain. Which are they? Which controls the gain more? Which Z is to both the dc output level and the gain? In your design is Z to be considered in reducing the output dc level to approximately V_{cc} (which has approximately $\frac{1}{2}V_{cc}$) with a gain of 10 times before Z ? What changes are needed?

14.45 Consider the front end of the circuit in Fig. 14.30. For $V_{cc} = 20\text{ V}$, calculate approximate values for the bias currents in Q_1 through Q_4 . Assume $V_{BE} = 100\text{ mV}$, $\beta_{31} = 20$, and $V_{AO} \sim 0.7\text{ V}$ A, so find the dc voltage at the output.

***14.46** Assume that the output voltage in the circuit of Fig. 14.30 is in single-ground mode (thus the signal feedback is determined by Z and the differential and common-mode input resistances). For this purpose, do not include R_1 and R_2 . For $V_{cc} = 20\text{ V}$, $\beta_{31} = 100$, and $\beta_{41} = 20$, find the transconductance from the input to the output (at the collector of the collectors of Q_1 and Q_2 and the base of Q_{12}).

14.47 It is required to use the LM380 power amplifier to drive an 8-Ω car speaker while drawing the maximum possible dc-to-dc dissipation to 1.5 W. In the circuit of Fig. 14.37, to determine the maximum possible power-supply voltage that can be used. Use only the given graphs; do not extrapolate. If the maximum allowed TID is less than 2%, what is the maximum possible load power? To deliver this power to the load, what peak-to-peak output voltage is required?

14.48 Consider the LM380 amplifier. Assume that when the amplifier is operated with a 20-V supply, the transconductance of the first stage is 1.6 mA/V. Find the unity-gain

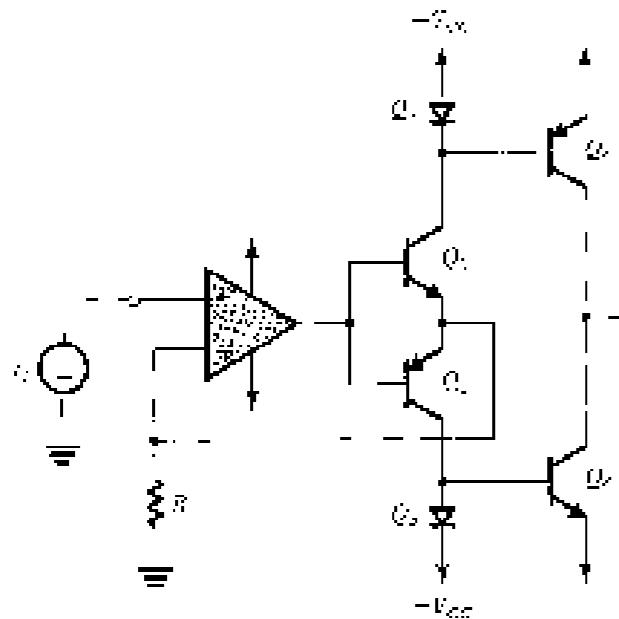


FIGURE P14.50

bandwidth (1). Since the closed-loop gain is approximately 50 V/V, find its 3-dB corner freq.

P14.49 Complete the power-mirror output stage shown in Fig. 14.33. Using a ±15-V supply, provide a design that provides an output of ±11 V or more, with current up to 120 mA, provided primarily by Q_3 and Q_4 , with a 10% contribution by Q_1 and Q_2 , and peak output currents of 1 A. Use 611 output FETs. As far basis in circuit design, use $\beta = 50$ and $|V_{GS|} = 0.7$ V for all devices or all currents. Also use $R_L = R_o = 0$.

14.50 For the circuit in Fig. P14.50, assume all the resistors to have large R . Show that $i_0 = v_o/R$. [This is called a current mirror.] An application of a versatile circuit building block shown in Fig. 14.52 makes it very easy (see Sedra and Roberts (1990)). For $\beta = 100$, by what % is the drain current i_0 actually lower than this ideal value?

P14.51 For the bridge circuit of Fig. 14.44, let $R_1 = R_2 = 10 \text{ k}\Omega$. Find R_3 and R_4 to obtain an overall $A_{v2} = 10$.

P14.52 An unusual bridge output configuration, with V_{GS} input resistance, is shown in Fig. P14.52. Note the similarity of this circuit to the last end-of-the-chapter problem circuit shown in Fig. 14.53(b). What is the gain A_{v2} of? Foramps using ±15 V supplies (thus limited to ±13 V), what is the largest sine wave you can provide across R_2 ?

P14.53 Current does velocity saturation vs. v . For electrons between $V_{ds} = 5 \times 10^6$ cm/s and $\mu \sim 1000$ cm²/V s, what is v_s for this device at high currents?

P14.54 Consider the design of the class AB amplifier of Fig. 14.38 under the following conditions: $V_{cc} = 15$ V, $|m_{ds}|V_{ds} = 200 \text{ }\mu\text{A/V}$, $|V_{gs}| = 2.7$ V, $\beta > 100$, $i_{ds} = i_{dr} = 1.0 \text{ mA}$, $i_{ds,s} = 100 \text{ }\mu\text{A}$, $i_{ds} = i_{dr} = I_{ds,s}/2$.

$R_2 = R_3$, the temperature coefficient of $V_{ds} = -2 \text{ mV/C}$, the temperature coefficient of $\beta = -2 \text{ mV/C}$ in the low-current region. Find the values of R_1 , R_2 , R_3 , R_4 , A_{v2} , i_{ds} , i_{dr} , Q_1 , and Q_2 to be reasonably equal. (Q_1 leads to spurious parasitic oscillation at high frequencies.)

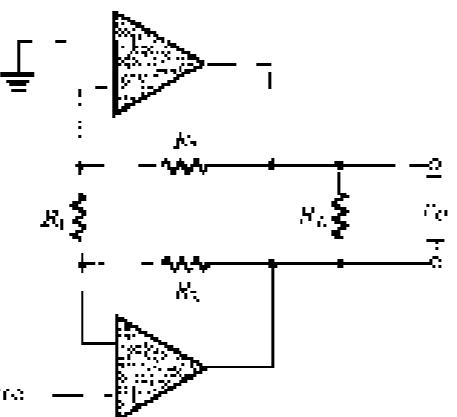


FIGURE P14.52

Using 1 k Ω of the small r_{ds} resistor, find resistor values that make $v_o/v_i = 10$ V/V.

SECTION 14.9: MOS POWER TRANSISTORS

14.55 A particular power DMOS device for which $C_s = 4.0 \text{ }\mu\text{F/cm}^2$, $B = 10^3 \text{ A/cm}^2$, and $V_t = 2$ V, reaches velocity saturation at $v_{ds} = 5$ V. Use Eqs. (14.46) and (14.47) to find an expression for i_{ds} and its value for this transistor. At what value

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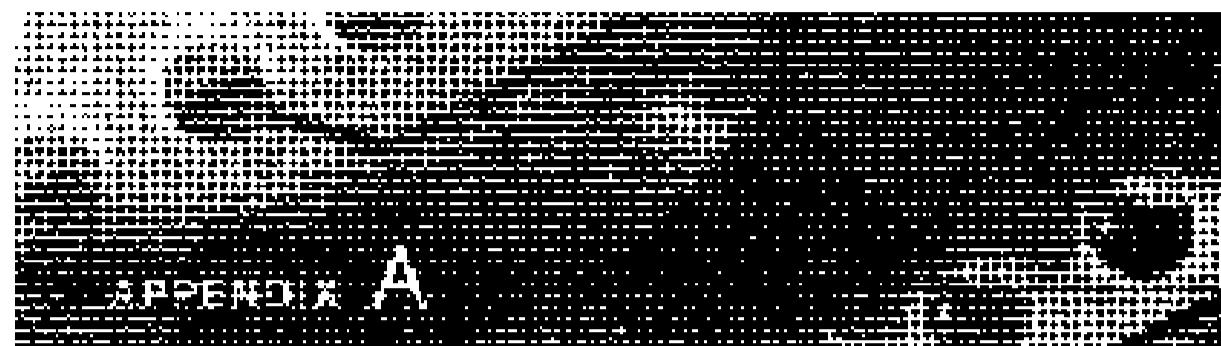
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APPENDIX A

VLSI Fabrication Technology

INTRODUCTION

The purpose of this appendix is to familiarize the reader with VLSI (very large scale integrated circuit) fabrication technology. The 'explorations' of standard silicon VLSI processing steps are given. The characteristics of devices available in CMOS and BiCMOS fabrication technologies are also presented. In particular, the aspects of IC integrated-circuit design that are different from discrete-circuit design will be discussed. To take proper advantage of the economics of integrated circuits, designers have had to overcome some serious device limitations (such as poor uniformity) while exploiting device advantages (such as good current-matching). An understanding of device characteristics is therefore essential at designing good custom VLSIs or application-specific ICs (ASICs). This understanding is also very helpful when selecting commercially available ICs to implement a system design.

This appendix will consider only silicon-based technologies. Although gallium arsenide (GaAs) is also used to implement VLSI chips, silicon (Si) is by far the most popular material, featuring a wide range of cost-performance trade-offs. Recent development in SiGe and quantum-dot technologies will further strengthen the position of Si-based technology processes in the microelectronics industry in the coming years.

Silicon is an abundant element, which occurs naturally in the form of sand. It can be refined using well-established techniques of purification and crystal growth. Silicon also exhibits suitable physical properties for fabricating active devices with good electrical characteristics. Moreover, silicon can be easily oxidized to form an excellent insulator, SiO_2 (glass). This native oxide is useful for constructing capacitors and MOSFETs. It also serves as a lift-off barrier that acts as a mask against the diffusion of unwanted impurities into nearby high-purity silicon material. This masking property of silicon oxide allows the electrical properties of silicon to be easily altered in predefined areas. Therefore, active and passive elements can be built on the same piece of material (or substrate). The components can then be interconnected using metal layers (similar to those used in printed-circuit boards) to form a so-called monolithic IC, which is essentially a single piece of material (wafer).

A.1 IC FABRICATION STEPS

The basic IC fabrication steps will be described in the following subsections. Some of these steps may be carried out many times, in different combinations and under different processing conditions during a complete fabrication run.

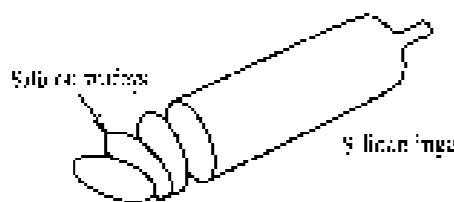


FIGURE A.1 Silicon ingot and wafers.

A.1.1 Wafer Preparation

The starting material for modern integrated circuits is very high-purity silicon. The material is grown as a single-crystal ingot. It takes the form of a steel-gray solid cylinder 10 cm to 20 cm in diameter (Fig. A.1) and can be 1 m to 2 m in length. This crystal is then sawed (like a loaf of bread) to produce circular wafers (diameters 400 µm to 600 µm) with a thickness of micrometer or millimeter (a micron). The surface of the wafer is then finished to a mirror finish using chemical and mechanical polishing (CMP) techniques. Semiconductor manufacturers usually purchase ready-made silicon wafers from a supplier and rarely start their process at the ingot stage.

The basic electrical and mechanical properties of the wafer depend on the orientation of the crystalline planes, as well as the concentration and type of impurities present. These variables are directly controlled during crystal growth. Controlled amounts of impurities can be added to the pure silicon in a process known as doping. This allows the alteration of the electrical properties of the silicon, in particular its resistivity. It is also possible to control the conduction-electron type, either holes (in p-type silicon) or electrons (in n-type silicon), that is responsible for electrical conduction. If a large number of impurity atoms is added, then the silicon is said to be heavily doped (e.g., concentration $> 10^{18}$ atoms/cm³). When describing the relative doping concentrations in semiconductor devices structures, it is common to use + and - symbols. A heavily doped (low-resistivity) n-type silicon wafer would be referred to as n+ material, while a lightly doped region may be referred to as n-. The ability to control the type of impurity and the doping concentration in the silicon permits the formation of diodes, transistors, and resistors in a single integrated circuit chip.

A.1.2 Oxidation

Oxidation refers to the chemical process of silicon reacting with oxygen to form silicon dioxide (SiO_2). To speed up the reaction, it is necessary to use special high-temperature (e.g., 1000–1200°C) vacuum furnaces. To avoid the introduction of even small quantities of contaminants (which could significantly alter the electrical properties of the silicon), it is necessary to maintain a clean environment. This is true for all processing steps involved in the fabrication of an integrated circuit. Specially filtered air is circulated in the processing area, and all personnel must wear special clean-room clothing.

The oxygen used in the reaction can be introduced either as a high-purity gas (in a process referred to as "dry oxidation") or as steam (or "wet oxidation"). In general, wet oxidation has a faster growth rate, but dry oxidation gives better electrical characteristics. In either case, the thermally grown oxide layer has excellent electrical insulation properties. The dielectric strength of SiO_2 is approximately 10¹² V/cm. It has a dielectric constant of about 3.9 and can be used to form excellent capacitors. As noted, silicon dioxide serves as an effective mask against many impurities, allowing the introduction of dopants into the silicon only in regions that are not covered with oxide. This masking property is one of the essential tools of microfabrication of VLSI devices.

Silicon dioxide is a thin transparent film, and the silicon surface is highly reflective. If white light is absorbed on an oxidized wafer, constructive and destructive interference will cause certain colors to be reflected. The wavelengths of the reflected light depend on the thickness of the oxide layer. In fact, by categorizing the color of the wafer surfaces, one can

deduce the thickness of the oxide layer. The same principle is used by sophisticated optical instruments to measure film thickness. On a processed wafer, there will be regions with different oxide thicknesses. The corresponding colors can be quite vivid, and thickness variations are immediately obvious when a finished wafer is viewed with the naked eye.

A.1.3 Diffusion

Diffusion is the process by which atoms move from a high-concentration region to a low-concentration region through the semiconductor crystal. The diffusion process is very much like a drop of ink dispersing through a glass of water except that it occurs much more slowly in solids. In fabrication, diffusion is a method by which to introduce impurity atoms (dopants) in silicon to change its resistivity. The rate at which dopants diffuse in silicon is a strong function of temperature. Thus, for speed, diffusion of impurities is usually carried out at high temperatures (1000–1200°C) to obtain the desired doping profile. When the wafer is cooled to room temperature, the impurities are essentially "frozen" in position. The diffusion process is performed in furnaces similar to those used for oxidation. The depth to which the impurities diffuse depends on both the temperature and the time allocated.

The most common impurities used as dopants are boron, phosphorus, and arsenic. Boron is a p-type dopant, while phosphorus and arsenic are n-type dopants. These dopants can be effectively masked by the silicon dioxide layers. By diffusing boron into an n-type substrate, a p+ junction diode is formed. If the doping concentration is heavy enough, the diffused layer can also be used as a conductor.

A.1.4 Ion Implantation

Ion implantation is another method used to introduce impurity atoms into the semiconductor crystal. An ion implanter produces ions of the desired element, accelerates them by an electric field, and allows them to strike the semiconductor surface. The ions become embedded in the crystal lattice. The depth of penetration is related to the energy of the ion beam, which can be controlled by the accelerating field voltage. The quantity of ions implanted can be controlled by varying the beam current (flow of ions). Since both voltage and current can be accurately measured and controlled, ion implantation results in much more accurate and reproducible impurity profiles than can be obtained by diffusion. In addition, ion implantation can be performed at room temperature. Ion implantation normally is used when accurate control of the doping profile is essential for device operation.

A.1.5 Chemical-Vapor Deposition

Chemical-vapor deposition (CVD) is a process by which gases or vapors are chemically reacted, leading to the formation of solids on a substrate. CVD can be used to deposit various materials on a silicon substrate, including SiO_2 , Si_3N_4 , and polysilicon. For instance, if silicon and oxygen are allowed to react above a silicon substrate, the end product, silicon dioxide, will be deposited as a solid film on the silicon oxide surface. The properties of the CVD oxide layer are not as good as those of a thermally grown oxide, but such a layer is sufficient to act as an electrical insulator. The advantage of a CVD layer is that the oxide deposits at a fast rate and at low temperature (below 600°C).

If silicon dioxide is used, then a silicon layer will be deposited on the wafer. If the reaction temperature is high enough (above 1000°C), the layer deposited will be a crystalline layer (assuming that there is an exposed crystalline silicon substrate). Such a layer is called an epitaxial layer, and the deposition process is referred to as epitaxy, rather than CVD. At lower temperatures, & if the substrate surface is not single-crystal silicon, the atoms will not be able to align in the same crystalline direction. Such a layer is called polycrystalline

silicon (only Si), since it consists of many small crystals of silicon whose crystalline axes are oriented in random directions. These layers are normally doped very heavily to form highly conductive regions that can be used for electrical interconnects.

A.1.6 Metallization

The purpose of metallization is to interconnect the various components (transistors, capacitors, etc.) to form the desired integrated circuit. Metallization involves the initial deposition of a metal over the entire surface of the silicon. The required interconnection pattern is then selectively etched. The metal layer is normally deposited via a sputtering process. A pure metal such as 99.99% aluminum is placed under an argon (Ar) ion gun inside a vacuum chamber. The wafers are also inserted inside the chamber above the target. The Ar ions will interact with the metal, since Ar is a noble gas; however, their ions are much too physically bombarded the target and thereby knock metal ions out of it. Those metal atoms will then coat all the surfaces inside the chamber, including the wafers. The thickness of the metal film can be controlled by the length of time for sputtering, which is normally in the range of 1 to 2 minutes.

A.1.7 Photolithography

The surface geometry of the various integrated-circuit components is defined photographically. First, the wafer surface is coated with a photoresistive layer (called photoresist) using a spin-on technique. After this, a photographic plate with given patterns (e.g., a quartz plate with a checkerboard pattern) will be used to selectively expose the photoresist under ultraviolet (UV) illumination. The exposed areas will become softened (for positive photoresist). The exposed layer can then be removed using a chemical developer, causing the mask图案 to appear on the wafer. Very fine surface geometries can be reproduced accurately by this technique. Photolithography requires some of the most expensive equipment in VLSI fabrication. Currently, we are already approaching the physical limits of the photolithographic process. Deep-UV light or electron beams can be used to define patterns at resolution as fine as 0.1 μm. However, another technology breakthrough will be needed to achieve further geometry decreasing.

The patterned photoresist layer can be used as an effective masking layer to protect materials below from wet chemical etching or reactive ion etching. Correspondingly, silicon dioxide, silicon nitride, polysilicon, and metal layers can be selectively removed using the appropriate etching methods. After the etching steps, the photoresist is stripped away, leaving behind a permanent pattern, as image of the photomask on the wafer surface.

To make this process even more challenging, multiple masking layers (there can be more than 20 layers in advanced VLSI fabrication processes) must be aligned precisely on top of previous layers. This must be done with even greater precision than is associated with the minimum dimensions of the masking patterns. Tiny misalignment imposes very critical mechanical and optical constraints on the photolithography equipment.

A.1.8 Packaging

A finished silicon wafer may contain several hundred to thousands of chips. Each chip may contain from 10 to 10³ or more transistors in a rectangular shape, typically between 1 mm and 0.3 mm on a side. The circuits are first tested electrically (while still in wafer form) using an automatic probing station. Bad circuits are marked for later identification. The circuits are then separated from each other (by dicing), and the good circuits (called dies) are mounted in packages (or headers). Examples of such IC packages are given in Fig. A.2. Fine gold wires are normally used to connect the pins of the package to the metallization patterns on the die. Finally, the package is sealed using plastic or epoxy under vacuum or in an inert atmosphere.

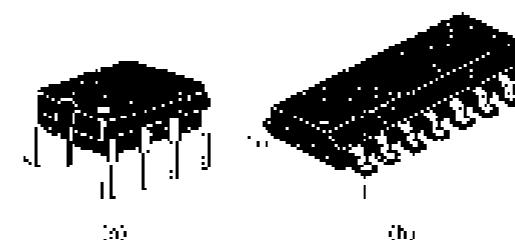


FIGURE A.2 (a) An 8-pin plastic dual inline IC package (DIP). (b) A 16-pin surface-mount IC package (SOIC), shown at a much larger scale than (a).

A.2 VLSI PROCESSES

Integrated-circuit fabrication was originally dominated by bipolar technology. But, by the late 1970s metal-oxide-semiconductor (MOS) technology was perceived to be more promising for VLSI implementation, owing to its higher packing density and lower power consumption. Since the early 1980s, complementary MOS (CMOS) technology has grown prodigiously to almost completely dominate the VLSI scene. earlier bipolar technology is still specialized functions such as digital and high-speed analog and RF circuits. CMOS technologies continue to evolve, and in the late 1980s, the incorporation of bipolar devices led to the emergence of high-performance bipolar-CMOS (BiCMOS) fabrication processes that provided the best of both technologies. However, BiCMOS processes are often very complicated and costly, since they require upward to 17 to 20 masking levels per implementation—by comparison, standard CMOS processes require only 10 to 12 masking levels.

The performance of CMOS and BiCMOS processes continues to improve, offering finer lithographic resolution. However, fundamental limitations on processing techniques and semiconductor properties have prompted the need to explore alternate materials. Silicon germanium (SiGe) and strained Si technologies have emerged as good compromises which improve performance while maintaining manufacturing compatibility (that is, no conflict with existing silicon-based CMOS fabrication equipment).

In the subsections that follow, we will examine, in turn, three aspects of modern IC fabrication, namely: (a) typical CMOS process flow, the performance of the available components, and the inclusion of bipolar devices to form a BiCMOS process.

A.2.1 n-Well CMOS Process

Depending on the choice of starting material (substrate), CMOS processes can be identified as *n*-well, *p*-well, or twin-well processes, the latter being the most complicated but also the most flexible in the optimization of both the *n*- and *p*-channel devices. In addition, many advanced CMOS processes may make use of trench isolation, and silicon-on-insulator (SOI) technology to reduce parasitic capacitance (to achieve higher speed) and to improve packing density.

For simplicity, an *n*-well CMOS process is chosen for discussion. Another benefit of this choice is that it can also be easily extended into a BiCMOS process. The typical process flow is as shown in Fig. A.3. A minimum of 7 masking layers is necessary. However, in practice most CMOS processes will also require additional layers, such as *n* and *p* guards for better LSI chip integrity, a second poly silicon layer for capacitors, and multilevel metals for high-density interconnections. The inclusion of these layers would increase the total number of masking layers from 15 to 20.

The starting material for the *n*-well CMOS is a *p*-type substrate. The process begins with an *n*-well diffusion (Fig. A.3a). The *n*-well is required whenever *p*-type MOSFETs are to be

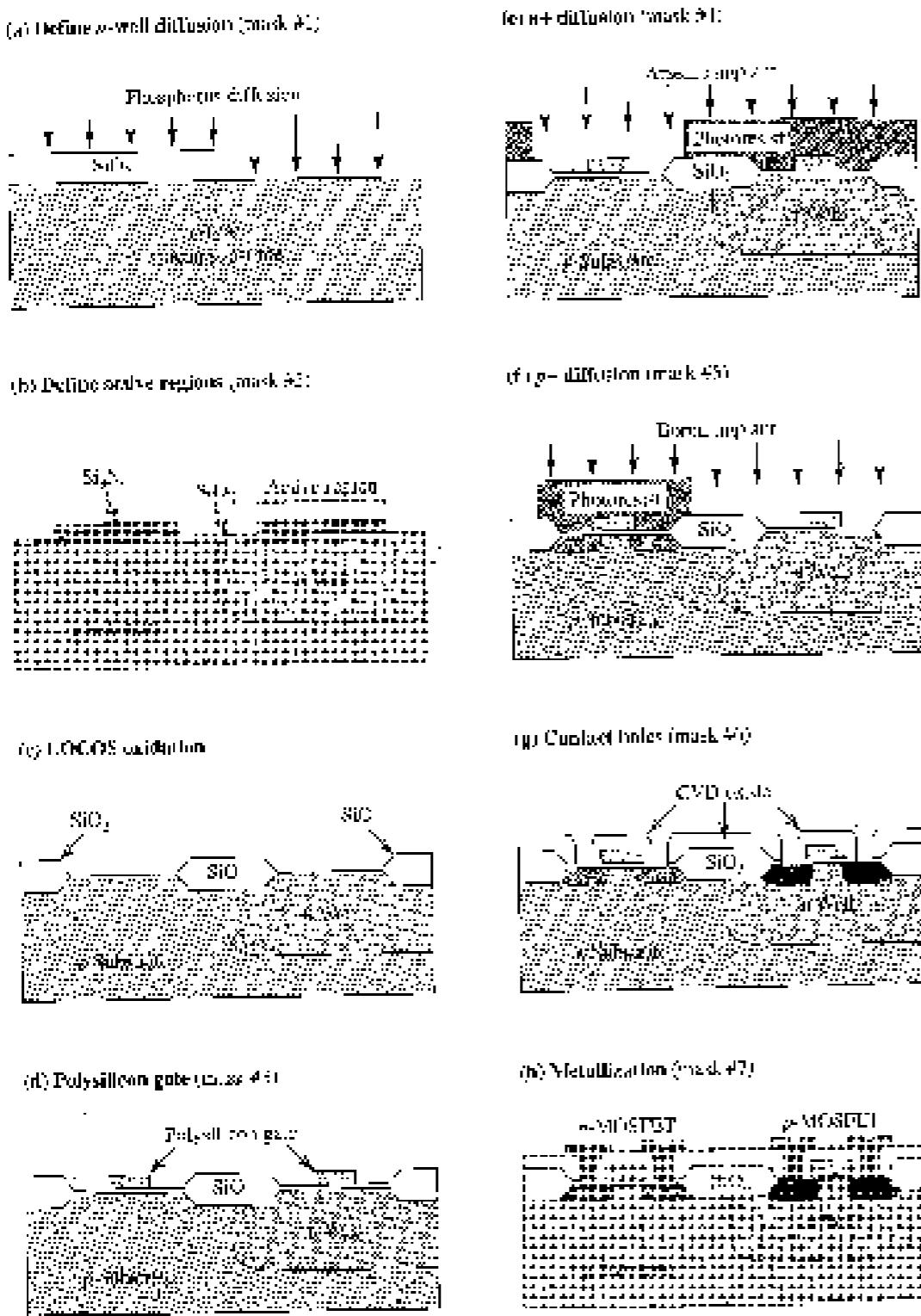


FIGURE A.3 A typical n-well CMOS process flow.

placed. A thick SiO_2 film dioxide layer is etched to expose the regions for n -well diffusion. The unexposed regions will be protected from the n -type phosphorus implant. Phosphorus is usually used for deep diffusions because it has a large diffusion coefficient and can diffuse faster than arsenic into the substrate.

The next step is to define the active regions where transistors are to be placed using a technique called local oxidation (LOCOS). A silicon nitride (Si_3N_4) layer is deposited and patterned relative to the previous n-well regions (Fig. A.3(d)). The nitride-covered regions will not be oxidized. After a long wet-oxidation step, thick-field oxide will appear in regions between two stripes (Fig. A.3(e)). This thick field oxide is necessary for isolating the transistors. It also allows interconnection layers to be oxidized on top of the field oxide without immediately forming a conduction channel in the silicon surface.

The next step is the formation of the polysilicon gate (Fig. A.3(f)). This is one of the most critical steps in the CMOS process. The thin oxide layer in the active region is first removed using wet-etching followed by the growth of a high-quality thin gate oxide. Current 0.13 μm and 0.1 μm processes routinely use oxide thicknesses as thin as 20 \AA to 50 \AA (1 angstrom = 10^{-10} cm). A polysilicon layer, usually arsenic doped (p -type), is then deposited and patterned. The photolithography is most demanding in this step, since the finest resolution is required to produce the shortest possible MOS channel length.

The polysilicon gate is a self-aligned structure and is preferred over the older type of isolated gate structure. A heavy arsenic implant can be used to form the n -source and drain regions of the n -MOSFETs. The polysilicon gate also acts as a barrier for this implant to protect the channel region. A layer of photoresist can be used to block the regions where p -MOSFETs are to be formed (Fig. A.3(g)). The thick-field oxide stops the implant and prevents n -regions from forming outside the active regions. A reversed photolithography step can be used to protect the n -MOSFETs during the p -boron source and drain implant for the n -MOSFETs (Fig. A.3(f)). In both cases the separation between the source and drain implants—the channel length—is defined by the polysilicon gate mask alone, hence the self-alignment.

Before contact holes are opened, a thick layer of CVD oxide is deposited over the entire wafer. A photoresist is used to define the contact window opening (Fig. A.3(g)) followed by a wet or dry oxide etch. A thin aluminum layer is then evaporated or sputtered onto the wafer. A lift-off masking and etching step is used to protect the interconnection (Fig. A.3(h)).

Not shown in the process flow is the final passivation step prior to packaging and wire bonding. A thick CVD oxide or pyrex glass is usually deposited on the wafer to serve as a protective layer.

A.2.2 Integrated Devices

Besides the obvious n - and p -channel MOSFETs, there are other devices that can be obtained by manipulating the masking layers. These include $p-n$ junction diodes, MOS capacitors, and resistors.

A.2.3 MOSFETs

The n -channel MOSFET is preferred over the p -MOSFET (Fig. A.4). The electron surface mobility is the n -channel device is two to four times higher than that for holes. Therefore, with the same device size (W and L), the n -MOSFET offers higher current (drive) for lower on-resistance as well as higher transconductance.

In a standard-electric design environment, MOSFETs are characterized by their threshold voltages and device sizes. Usually the n - and p -channel devices are designed to have threshold voltages of similar magnitude for a particular process. The threshold voltage can be adjusted

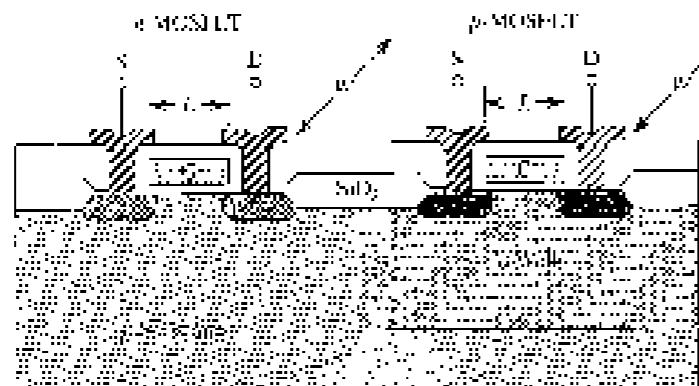


FIGURE A.4 Cross-sectional diagram of an n-on-p-MOSFET.

by changing the device surface dimensions (B and L). This feature is not available for bipolar transistors; thus integrated MOSFET circuits are much more flexible in their design.

A.2.4 Resistors

Resistors in integrated form are not very precise. They can be made from various diffusion regions as shown in Fig. A.5. Different diffusion regions have different resistivity. The n -well is usually used for medium-value resistors, while the $n+$ and $p+$ diffusions are useful for low-value resistors. The actual resistance value can be defined by changing the length and width of diffused regions. The tolerance of the resistor value is very poor (30–50%). However, matching of ten similar resistor values is quite good (5%). Thus circuit designers should design circuits that exploit resistor matching and avoid designs that require a specific resistor value.

All diffused resistors are self-isolated by the reversed-biased pn junctions. However, a serious drawback for these resistors is that they are accompanied by a substantial parasitic junction capacitance, making them not very useful for high-freqency applications. The reversed-biased pn junctions also exhibit a Zener effect, leading to a variation in the resistance value as the applied voltage is changed (a large voltage coefficient [\times multiplier]). Since the resistivities of materials vary with temperature, the resistor also exhibits a significant temperature coefficient.

A more useful resistor can be fabricated using the polysilicon layer that is placed on top of the thick-field oxide. The thin poly-silicon layer provides better surface area matching and

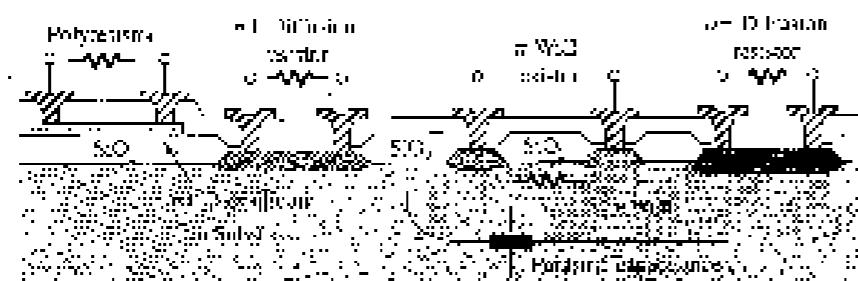


FIGURE A.5 Cross-section of resistors of various types available from a typical n-well CMOS process.

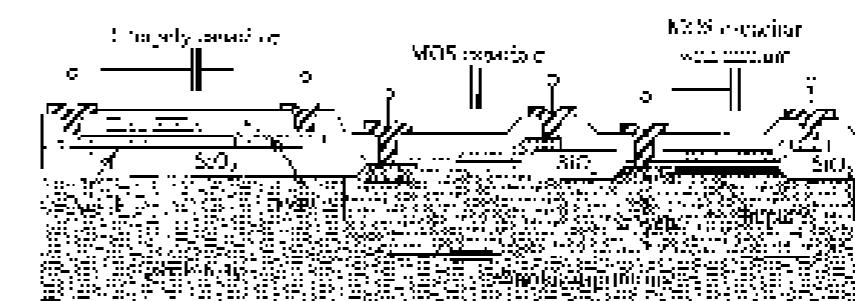


FIGURE A.6 Integrated MOS capacitors in an n-well CMOS process.

more accurate resistor ratios. Furthermore, the poly-resistor is physically separated from the substrate, resulting in much lower parasitic capacitance and voltage coefficient.

A.2.5 Capacitors

Two types of capacitor structure are available in CMOS processes, MOS and interpoly capacitors (also MM—metal-insulator-metal). The cross sections of these structures are as shown in Fig. A.5. The MOS gate capacitance, denoted in the center structure, is basically the gate-to-source capacitance of a MOSFET. The capacitance value is determined by the gate area. The oxide thickness is the same as the gate oxide thickness in the MOSFETs. This capacitor exhibits a large voltage dependence. To eliminate this problem, an additional $n+$ implant is required to form the bottom plate of the capacitor, as shown in the structure on the right. Both these MOS capacitors are physically in contact with the substrate, resulting in a large parasitic junction capacitance at the bottom plate.

The interpoly capacitor exhibits a much smaller capacitance but at the expense of the inclusion of a second poly-silicon layer to the CMOS structure. Since this capacitor is placed on top of the thick-field oxide, parasitic effects are kept to a minimum.

A third and less often used capacitor is the junction capacitor. Any pn junction under reverse bias produces a depletion region that acts as a dielectric between the p and the n regions. The capacitance is determined by geometry and doping levels and has a large voltage coefficient. This type of capacitor is often used as a varactor (variable capacitor) for tuning circuits. However, this capacitor works only with reversed bias voltages.

For interpoly and MOS capacitors, the capacitance values can be controlled to within 1%. Practical capacitated values range from 0.5 pF to a few μ s of picofarads. The matching between similar-size capacitors can be within 0.1%. This property is extremely useful for designing precision analog CMOS circuits.

A.2.6 pn Junction Diodes

Whenever n -type and p -type diffused regions are placed next to each other, a pn junction diode results. A useful structure is the n -well diode shown in Fig. A.7. The diode fabricated in an n -well can provide a high breakdown voltage. This diode is essential for the input clamping circuits for protection against electrostatic discharge. The diode is also very useful as an on-chip temperature sensor by monitoring the variation of its forward voltage drop.

A.2.7 BICMOS Process

An n -on- p vertical bipolar transistor can be integrated into the n -well CMOS process with the addition of a p -base diffusion region (Fig. A.8). The characteristics of this device depend on

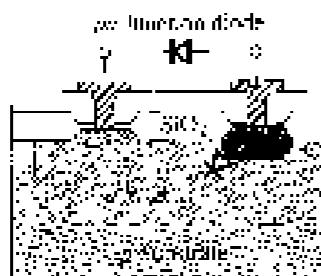


FIGURE A.7 A pn junction diode in a n-well C2405 process.



FIGURE A.8 Cross-sectional diagram of a BiCMOS process.

the base width and the collector area. The base width is determined by the difference in implantation depth between the n- and the p-base diffusions. The emitter area is determined by the junction area of the p+ diffusion at the emitter. The n-well serves as the collector for the n-pn diode. Typically, the gain is measured as β in the range of 50 to 100 and a cutoff frequency greater than 10 GHz.

Normally, an n-buried layer is used to reduce the series resistance of the collector, since the n-well has a very high resistivity. However, this would further complicate the process with the introduction of p -type epitaxy and one more masking step. Other variations on the bipolar transistor include the use of a polyemitter and self-aligned base contact to minimize parasitic effects.

A.2.8 Lateral pnp Transistor

The fact that most BiCMOS processes do not have optimized pnp transistors makes circuit design somewhat difficult. However, in some situations, a parasitic lateral pnp transistor can be used (Fig. A.9).

In this case, the n-well serves as the n-base region with p + diffusions as the emitters and the collector. The base width is determined by the separation between the two p + diffusions. Since the doping profile is not optimized for the base-collector junctions, and because the



FIGURE A.9 A lateral pnp transistor.

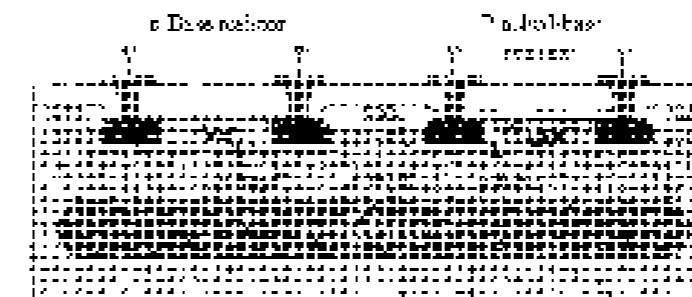


FIGURE A.10 A Hall effect p-base resistor.

base width is limited by the minimum photolithographic resolution, the performance of this device is not very good—typically, β of around 10 with a low cutoff frequency.

A.2.9 p-Base and Pinched-Base Resistors

With the additional p-base diffusion in the BiCMOS process, two additional resistor structures are available. The p-base diffusion can be used to form a straightforward p-base resistor as shown in Fig. A.10. Since the base region is usually at a relatively low doping level and with a moderate junction depth, it is suitable for medium-value resistors (5 to 10 kilohms). If a large resistor value is required, the pinched-base resistor can be used. In this structure, the p-base region is encroached by the n-drift under-reducing the conductive path. Resistor values in the range of 100 k Ω to 1000 k Ω can be obtained. As with the diffusion resistors discussed earlier, resistor values exhibit poor tolerance and temperature drift, with a relatively good matching.

A.2.10 The SiGe BiCMOS Process

With the advent of wireless applications, the demand for high-performance, high-frequency RF integrated circuits is enjoying a tremendous growth. The fundamental limitations of physical material properties initially prevented silicon-based technology from competing with more expensive III-V compound technologies such as GaAs. By incorporating a controlled amount (typically no more than 15 mole %) of germanium (Ge) into crystalline silicon (Si), the energy bandgap can be altered. The specific conduction profile of the Ge can be engineered in such a way that the energy bandgap can be gradually reduced from that in the pure Si, leading to a lower value in the Si:Ge region. This energy-bandgap reduction produces a built-in electric field that facilitates the movement of carriers, hence giving higher operating speed. Therefore, SiGe bipolar transistors can achieve significant higher cutoff frequency (e.g., in the 50–10 GHz range). Another benefit is that the SiGe process is compatible with existing Si-based fabrication technology, ensuring a very favorable cost-performance ratio.

To take advantage of the SiGe material characteristics, the basic bipolar transistor structure must also be modified to further reduce parasitic capacitance (for higher speed) and to improve the injection efficiency (for higher gain). A symmetrical bipolar device structure is shown in Fig. A.11. The device makes use of trench isolation to reduce the collector sidewall capacitance between the n-well/p+ buried layer and the p substrate. The emitter size and the p-base contact size are defined by a self-aligned process to minimize the base-collector junction (Miller) capacitance. This type of device is called a heterojunction bipolar transistor (HBT), since the emitter-base junction is formed from two different types of material, polySilicon emitter and SiGe base. The injection efficiency is significantly better than a homojunction device due to a

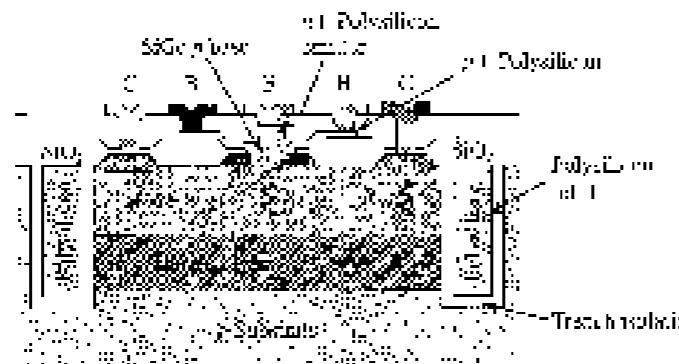


FIGURE A.11 Cross-sectional diagram of a symmetrically doped n+ poly-SiGe heterojunction bipolar transistor (HBT).

conventional BJT). Coupled with the fact that base width is typically only around 50 μm , it is easy to achieve a current gain of more than 100. In addition, as shown in Fig. A.11, multiple layers of metallization can be used to further reduce the device size and interconnect resistance. All these design features are necessary to complement the speed performance of the SiGe material.

A.3 VLSI LAYOUT

Each designed circuit schematic must be transformed into a layout that consists of the geometric representation of the circuit components and interconnections. With the advent of computer-aided design (CAD) tools, many of the conversion steps from schematic to layout can be carried out automatically. However, any good mixed-signal IC designer must have practical rule-making layout at one point or another. To illustrate such a procedure we will consider the synthesis of CMOS inverters.

Similar to the requirement in a printed circuit board layout to reduce crossover paths, the circuit must first be "flattened" and rearranged to eliminate any interconnection crossovers. Each process is made up of a specific set of masking layers. In this case, 7 layers are used. Each layer is usually assigned a unique color and ID pattern for ease of identification in a computer environment or a printed color plot. The layout begins with the placement of the transistors. For illustration purposes (Fig. A.12), the p-MOSFETs are placed in configurations similar to that of the schematic. In practice, the designer is free to choose the most area-efficient layout that she can identify. The MOSFETs are defined by the active areas overlapped by the "Poly 1" layer. The MOSFET length and width are defined by the width of the "Poly 1" strip and that of the active region, respectively. The n-MOSFET is enclosed in a well. For more complex circuits, multiple wells can be used for different groups of p-MOSFETs. The n-MOSFET is enclosed by the $n+$ -diffusion mask to form the source and drain, while the p-MOSFET is enclosed by the $p+$ -diffusion mask. Contact holes are placed at regular intervals to complete connections to the metal layers. Finally, the "Metal 1" layer completes the interconnections.

The corresponding cross-sectional diagram of the CMOS inverter, viewed along the X'X plane is shown in Fig. A.13. The only Si polyes for both transistors are connected together to form the input terminal, X. The drains of both transistors are tied together via "Metal 1" to form the output terminal, Y. The sources of the n- and p-MOSFETs are connected to GND and V_{DD} , respectively. Note that biasing contacts consisting of $n+$ -doped $p+$ -diffusions are used to tie the body potential of the n- and p-MOSFETs to the appropriate voltage levels.

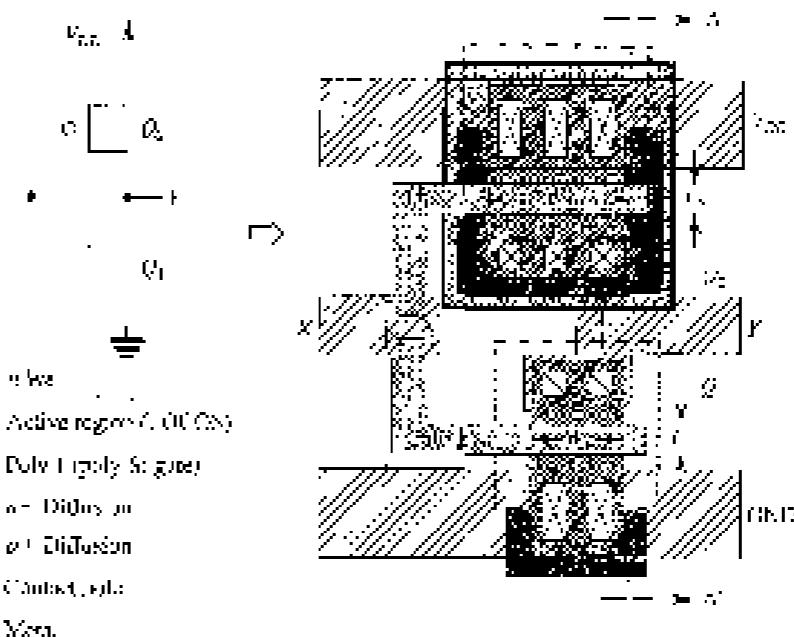


FIGURE A.12 A CMOS inverter schematic and layout.

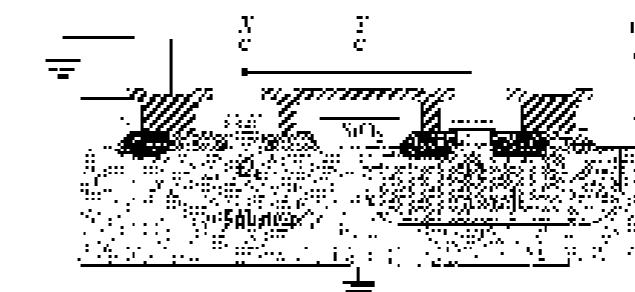


FIGURE A.13 The cross-sectional layout along the X'X plane of a CMOS inverter.

When the layout is completed, the circuit must be verified using appropriate CAD tools including circuit extractor, design rule checker (DRC), and circuit simulator. Once these verifications have been satisfied, the design can be "piped out" to a mask-making facility. A pattern generator (PG machine) can then draw the geometries on a glass or quartz photoplate using electronically driven shutters. Layers are drawn one-by-one onto different photoplates. When these plates have been developed, clear and dark patterns depicting the geometries on the layout will appear. A set of the photoplates for the CMOS inverter example is shown in Fig. A.14. Depending on whether the various geometries are meant to be opened as windows or kept as patterns, the plates can be "positive" or "negative" type with clear or dark fields. Note that these layers must be processed in sequence. In the steps of this sequence, they must be aligned within very fine tolerances to form the transistors and interconnects. Naturally, the greater the number of layers, the more difficult it is to maintain the alignment. A process with more layers also requires better photolithography equipment and possibly results in lower yield. Hence, each additional mask will be reflected in an increase in the final cost of the IC chip.

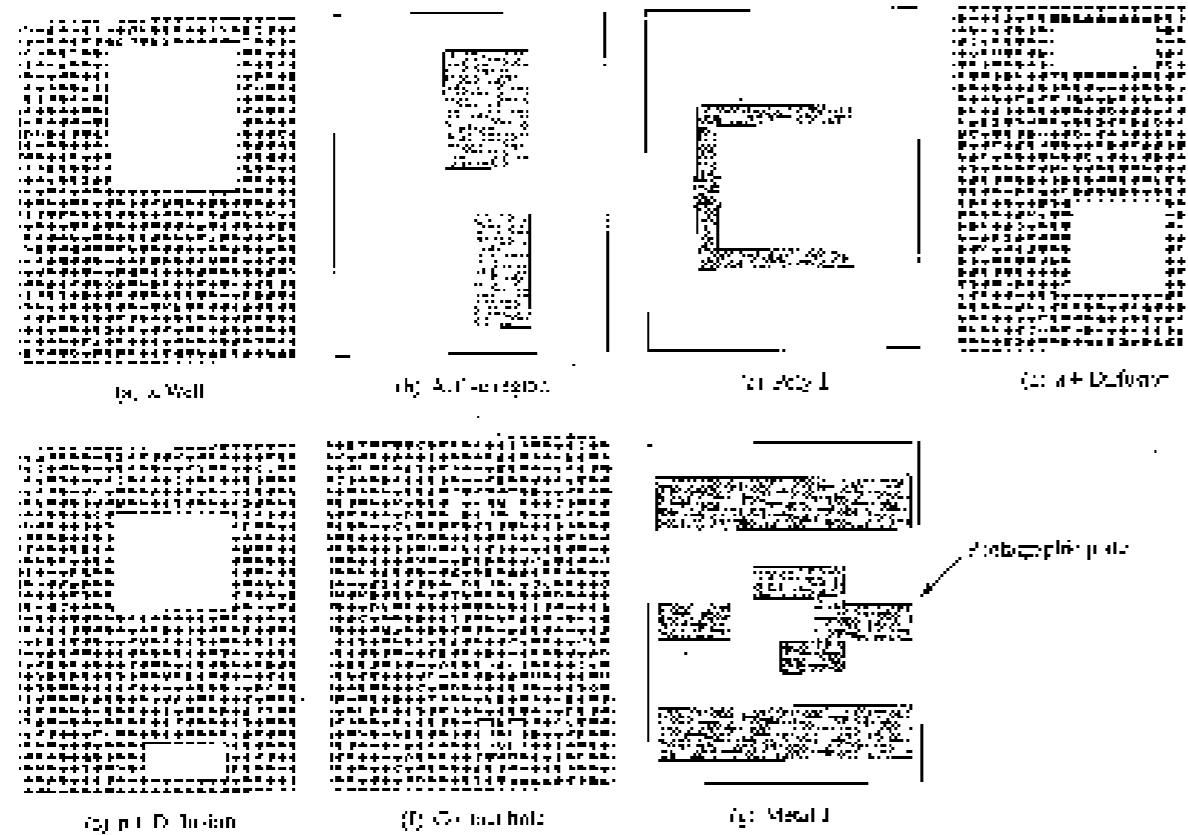


FIGURE A.14 A set of photomasks for the new 100V device. Note that each layer requires a separate photoresist exposure. (d) and (e) are anti-reflective masks; (b), (c), and (g) are layout-defined masks.

SUMMARY

- This appendix presented an overview of the various steps of VLSI fabrication processes. This includes component characteristics, process flows, and layouts. This is by no means a complete account of steps without

VLSI technology. Interested readers should consult reference textbooks on this subject for more detailed discussions.



Two-Port Network Parameters

INTRODUCTION

At various points throughout the text, we make use of some of the different possible ways to characterize linear two-port networks. A summary of this topic is presented in this appendix.

B.1 CHARACTERIZATION OF LINEAR TWO-PORT NETWORKS

A two-port network (Fig. B.1) has four port variables: V_1 , I_1 , V_2 , and I_2 . If the two-port network is linear, we can use two of the variables as excitation variables and the other two as response variables. For instance, the network can be excited by a voltage V_1 at port 1 and a voltage V_2 at port 2, and the two currents I_1 and I_2 can be measured to represent the network response. In this case V_1 and V_2 are independent variables and I_1 and I_2 are dependent variables, and the network operation can be described by the two equations

$$I_1 = y_{11}V_1 + y_{12}V_2 \quad (B.1)$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \quad (B.2)$$

Here, the four parameters y_{11} , y_{12} , y_{21} , and y_{22} are admittances, and their values completely characterize the linear two-port network.

Depending on which pair of the four port variables are used to represent the network excitation, a different set of admittances (and a correspondingly different set of parameters) is required for characterizing the network. We shall present the four parameter sets commonly used in electronics.



FIGURE B.1 The reference directions of the four port variables in a linear two-port network.

B.1.1 y Parameters

The short-circuit admittance for y-parameter characterization is based on exciting the network by V_1 and V_2 , as shown in Fig. B.2(a). The describing equations are Eqs. (B.1) and (B.2). The four admittance parameters can be defined according to their roles in Eqs. (B.1) and (B.2).

Specifically, from Eq. (B.1) we see that y_{11} is defined as

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0} \quad (\text{B.1})$$

Thus y_{11} is the input admittance at port 1 with port 2 short-circuited. This definition is illustrated in Fig. B.2(b), which also provides a conceptual method for measuring the input short-circuit admittance, y_{11} .

The definition of y_{12} can be obtained from Eq. (B.1) as

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} \quad (\text{B.2})$$

Thus y_{12} represents the cross admittance from port 2 to port 1. Since in amplifiers, port 1 represents the input port, and port 2 the output port, y_{12} represents internal feedback in the network. Figure B.2(c) illustrates the definition and the method for measuring y_{12} .

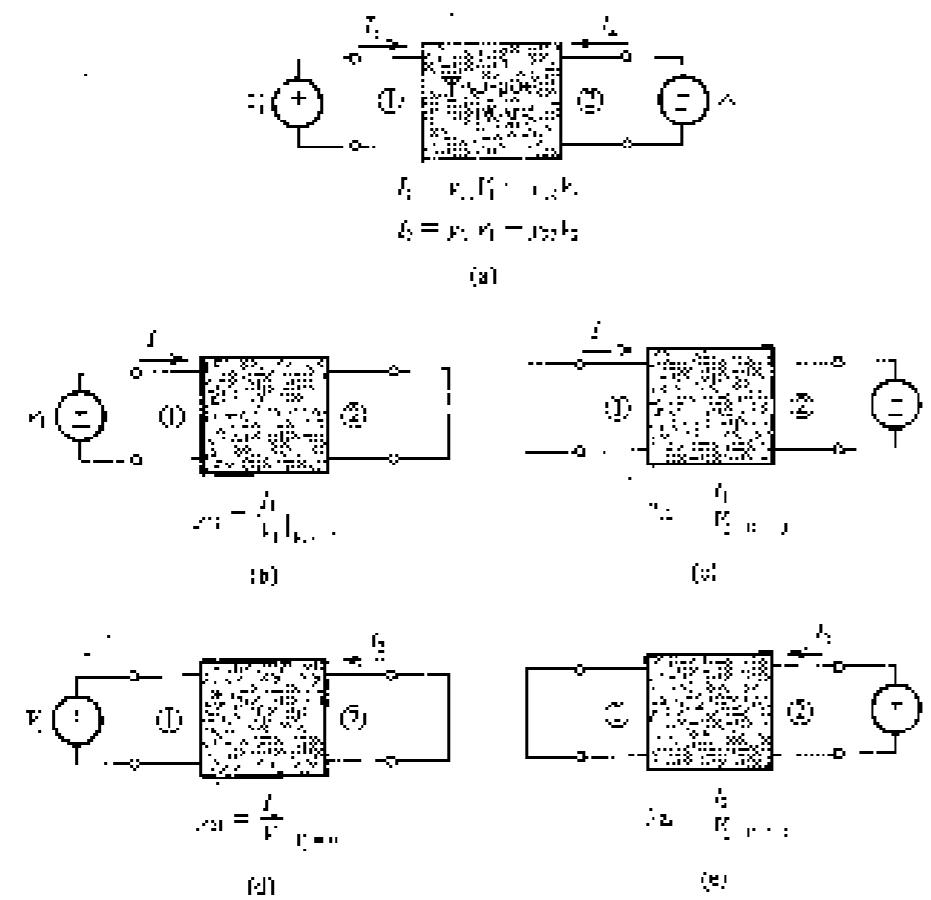


FIGURE B.2 Definition and concept measurement circuits for the y parameters.

The definition of y_{21} can be obtained from Eq. (B.2) as

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} \quad (\text{B.3})$$

Here y_{21} represents transmission from port 1 to port 2. If port 1 is the input port and port 2 the output port of an amplifier, then y_{21} provides a measure of the forward gain of transmission. Figure B.2(d) illustrates the definition and the method for measuring y_{21} .

The parameter y_{22} can be defined, based on Eq. (B.2), as

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0} \quad (\text{B.4})$$

This y_{22} is the admittance looking into port 2 while port 1 is short-circuited. For amplifiers, y_{22} is the output short-circuit admittance. Figure B.2(e) illustrates the definition and the method for measuring y_{22} .

B.1.2 z Parameters

The open-circuit impedance (or z-parameter) characterization of two-port networks is based on exciting the network by I_1 and I_2 , as shown in Fig. B.3(a). The describing equations are

$$V_1 = z_{11}I_1 + z_{12}I_2 \quad (\text{B.5})$$

$$V_2 = z_{21}I_1 + z_{22}I_2 \quad (\text{B.6})$$

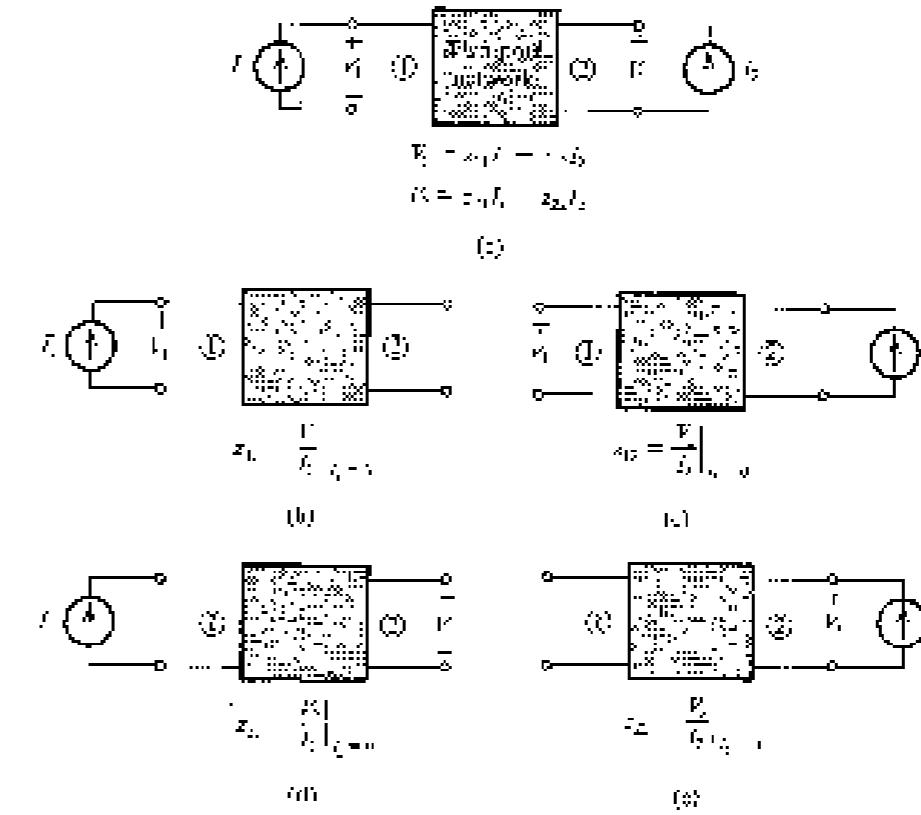


FIGURE B.3 Definition and concept measurement circuits for the z parameters.

Owing to the duality between the α - and β -parameter characterizations, we shall not give a detailed discussion of α parameters. The definition and method of measuring each of the four α parameters are given in Fig. B.3.

B.1.3 α Parameters

The hybrid (α -parameter) characterization of two-port networks is based on exciting the network by V_1 and I_2 , as shown in Fig. B.4(a), using the reason behind the name hybrid). The describing equations are

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad (\text{B.9})$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \quad (\text{B.10})$$

From which the definitions of the four h parameters can be obtained as

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} \quad h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \quad h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

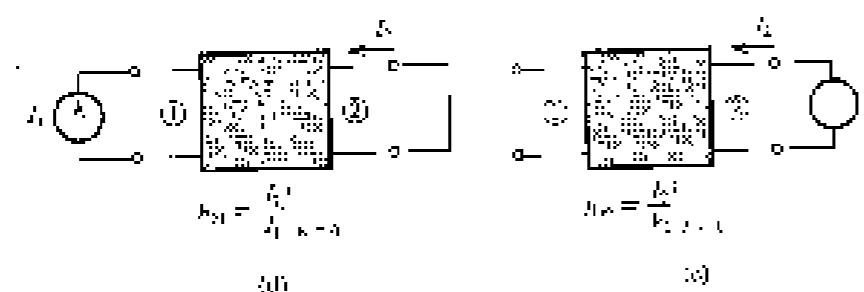
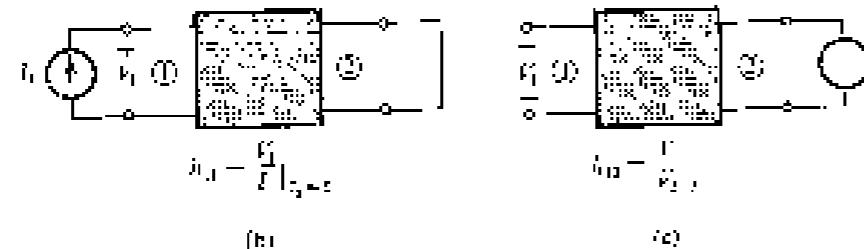
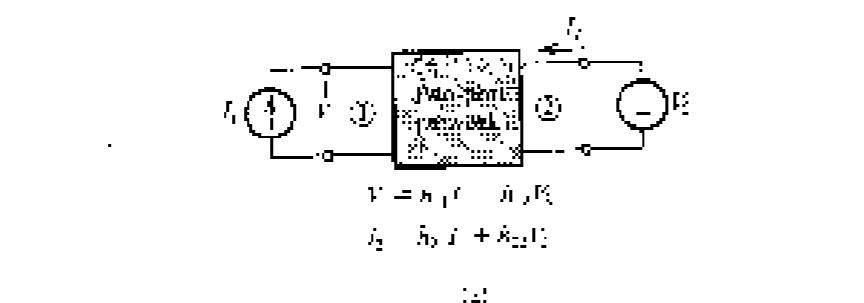


FIGURE B.4 Definition and conceptual measurement circuits for the h parameters.

Thus, h_{11} is the input impedance at port 1 with port 2 short-circuited. The parameter h_{21} represents the reverse or feedback voltage ratio of the network, measured with the input port open-circuited. The forward-transmission parameter h_{12} represents the output gain of the network with the output port short-circuited; for this reason, h_{12} is called the short-circuit current ratio. Finally, h_{22} is the output admittance with the input port open-circuited.

The definitions and conceptual measuring setups of the h parameters are given in Fig. B.4.

B.1.4 g Parameters

The inverse-hybrid (g -parameter) characterization of two-port networks is based on excitation of the network by V_1 and I_2 , as shown in Fig. B.5(a). The describing equations are

$$I_1 = g_{11}V_1 + g_{12}I_2 \quad (\text{B.11})$$

$$V_2 = g_{21}V_1 + g_{22}I_2 \quad (\text{B.12})$$

The definitions and conceptual measuring setups are given in Fig. B.5.

B.1.5 Equivalent-Circuit Representation

A two-port network can be represented by an equivalent circuit based on the set of parameters used for its characterization. Figure B.6 shows four possible equivalent circuits corresponding

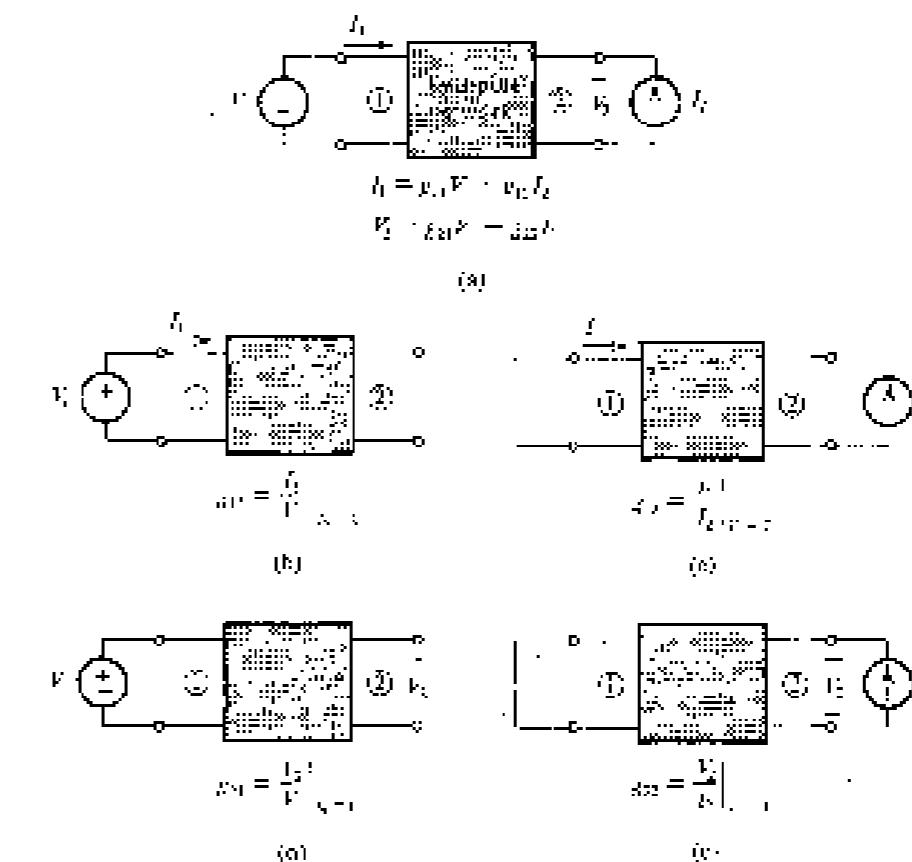
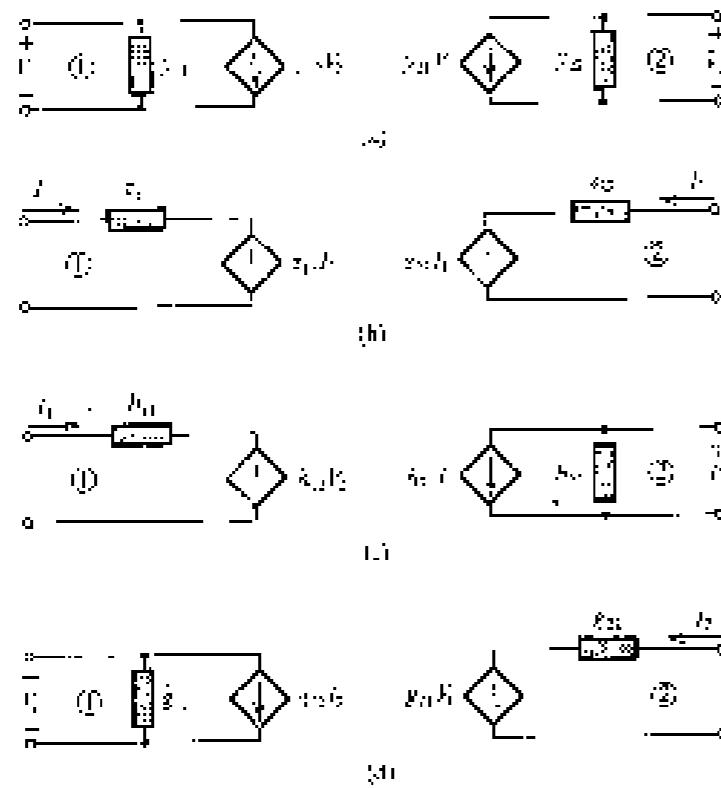


FIGURE B.5 Definition and conceptual measurement circuits for the g parameters.

FIGURE B.6 Equivalent circuits for two-port networks: (a) h ; (b) z ; (c) g ; and (d) y parameters.

to the four parameter types just discussed. Each of these equivalent circuits is a direct pictorial representation of the corresponding two equations describing the network in terms of the particular parameter set.

Finally, it should be mentioned that other parameter sets exist for characterizing two-port networks, but these are not discussed or used in this book.

EXERCISE

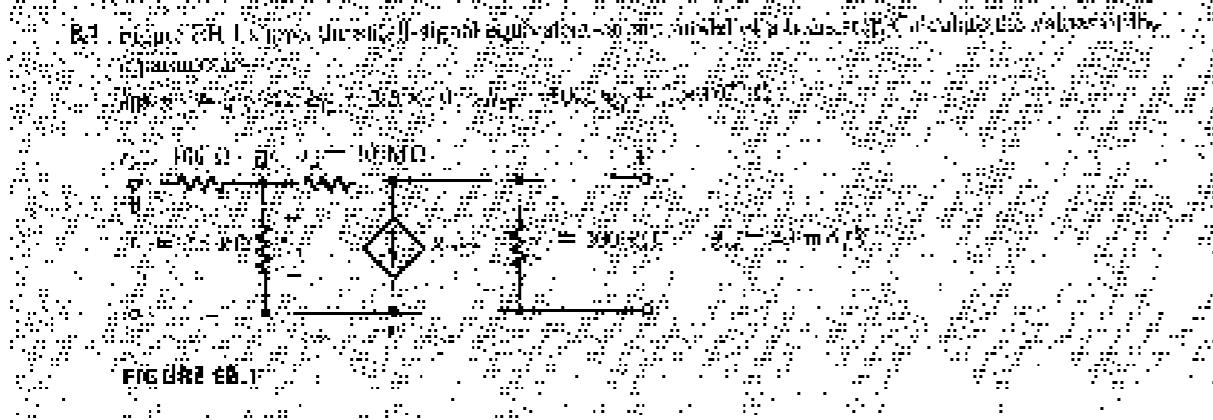


FIGURE B.7

PROBLEMS

- B.1** (a) An h -parameter characterized by the h_{21} value of the equivalent circuit of Fig. B.6(a) is fed with a source having a voltage V_1 and a resistance R_s , and is loaded on a resistance R_L . Show that its voltage gain is given by

$$\frac{V_2}{V_1} = \frac{h_{21}}{(R_s + h_{11})R_L + h_{12}h_{21}}$$

- (b) Use the expression derived in (a) to find the voltage gain of the transistor in Exercise B.1 for $R_s = 1\text{ k}\Omega$ and $R_L = 1\text{ k}\Omega$.

- B.2** The terminal impedances of a two-port network are measured with the following results: With the output short-circuited and an input current of 0.01 mA, the output current is 1.0 mA and the output voltage is 26 mV. With the input open-circuited and a voltage of 10 V applied to the output,

the current in the source is 0.2 mA and the voltage measured at the junction is 2.5 mV. Find values for the h parameters of this network.

- B.3** Figure B.8 shows the high-frequency equivalent circuit of Fig. 2.11. For simplicity, r_o has been omitted. Find the z parameters.

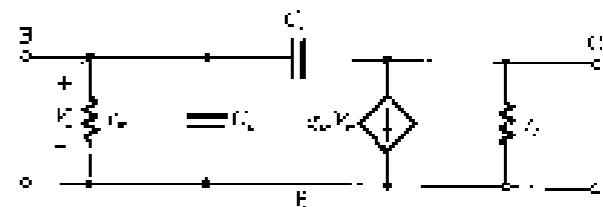
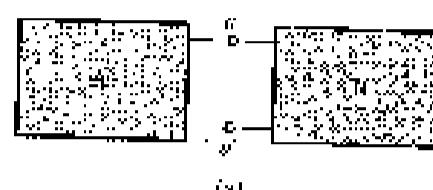
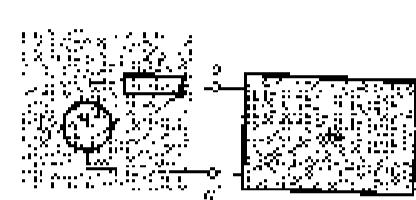


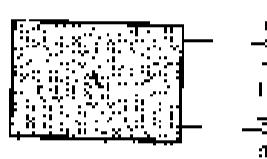
FIGURE B.8



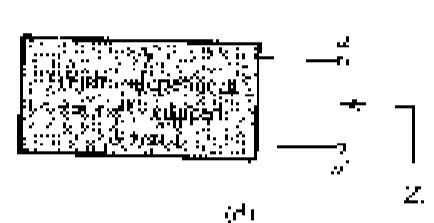
(a)



(b)

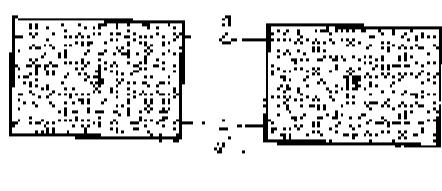


(c)

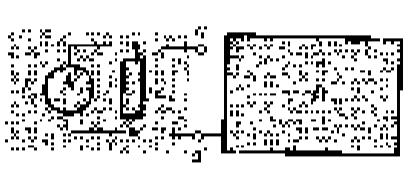


(d)

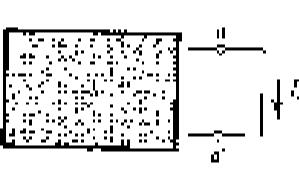
FIGURE C.1 Thévenin's theorem.



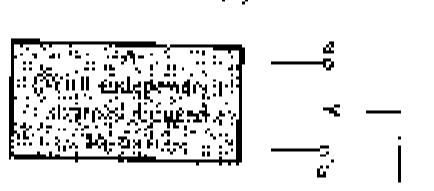
(a)



(b)



(c)



(d)

FIGURE C.2 Norton's theorem.

C.2 NORTON'S THEOREM

Norton's theorem is the dual of Thévenin's theorem. It is used to represent a part of a network by a current source I_A and a parallel impedance Z_A , as shown in Fig. C.2. Figure C.2(a) shows a network divided into two parts, A and B. In Fig. C.2(b) part A of the network has been replaced by its Norton's equivalent: a current source I_A and a parallel impedance Z_A . Figure C.2(c) illustrates how I_A is to be determined. Simply open-circuit the two terminals of network A and measure the current that circulates through the terminals. To determine Z_A , we reduce all external (i.e., independent) sources in network A to zero by short-circuiting voltage sources and opening-circuiting current sources. The impedance Z_A will be equal to the input impedance of network A after this reduction has been performed, as illustrated in Fig. C.2(d).

Solution

Thévenin's theorem can be used at the base side to reduce the network composed of V_B , R_1 , and R_2 to a dc voltage source V_{AB} .

$$V_{AB} = V_B \frac{R_2}{R_1 + R_2}$$

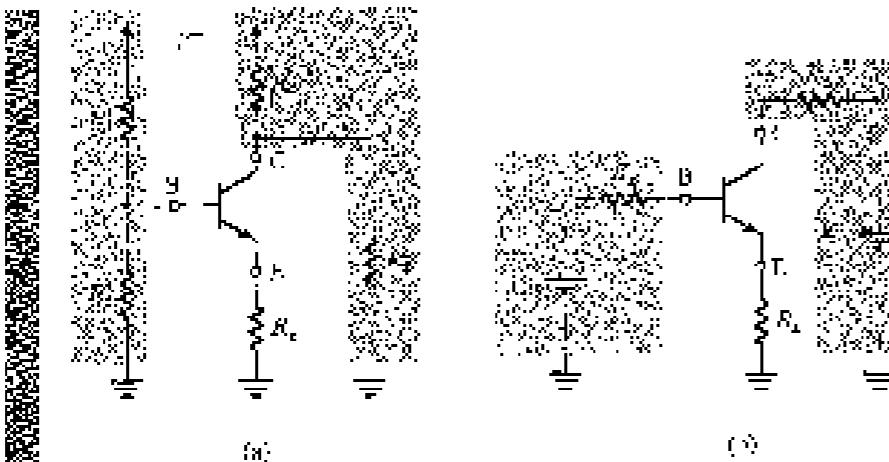


FIGURE C.3 Thévenin's theorem applied to a simple circuit (a) to obtain (b). (See Example C.1.)

and a resistance R_{TH} :

$$R_{\text{TH}} = R_1 \parallel R_2$$

where \parallel denotes "in parallel with." At the collector side, Thévenin's theorem can be applied to reduce the network composed of V_1 , R_2 , and R_1 to a dc voltage source V_{DC} ,

$$V_{\text{DC}} = V_1 \frac{R_1}{R_1 + R_2}$$

and a resistance R_{DC} :

$$R_{\text{DC}} = R_2 / R_1$$

The reduced circuit is shown in Fig. C.3(b).

C.3 SOURCE-ABSORPTION THEOREM

Consider the situation shown in Fig. C.4. In the course of analyzing a network we find a controlled current source I_c appearing between two nodes whose voltage difference is the controlling voltage V_x . That is, $I_c = g_m V_x$ where g_m is a conductance. We can replace this controlled source by an impedance $Z_c = V_x / I_c = 1/g_m$, as shown in Fig. C.4, because the current driven by this impedance will be equal to the current of the controlled source that we have replaced.

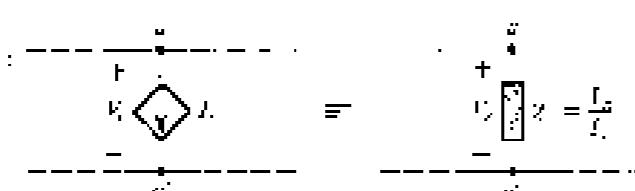


FIGURE C.4 The source-absorption theorem.

Figure C.5(a) shows the small-signal equivalent circuit used in a transistor. We want to find the resistance R_i looking into the emitter terminal E—that is, the resistance between the emitter and ground, with the base B and collector C grounded.

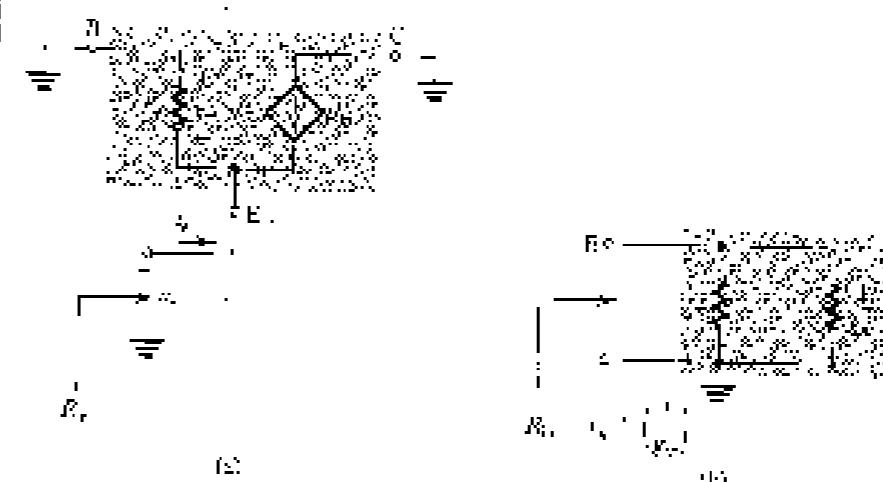


FIGURE C.5 Circuits for Example C.2.

Solution

From Fig. C.5(a) we see that the voltage v_b will be equal to zero. Thus looking between B and ground we see a resistance r_e in parallel with a current source drawing a current $g_m v_e$ away from terminal E. This latter source can be replaced by a resistance $(1/g_m)$, resulting in the input resistance R_i , given by

$$R_i = r_e \parallel (1/g_m)$$

as illustrated in Fig. C.5(b).

EXERCISES

1. A dependent source is connected as shown in the figure. The dependent voltage is $V_x = 10V$ and the dependent current is $I_x = 10A$. Find the value of the dependent source.
- Ans: $V_x = 10V$, $I_x = 10A$
2. In the circuit shown in Fig. C.6, the dependent voltage depends on V_x as $V_x = 10V$. Is this true? Explain.
3. Simplify the circuit and hence calculate the dependent current I_x .
- Ans: $I_x = 10A$

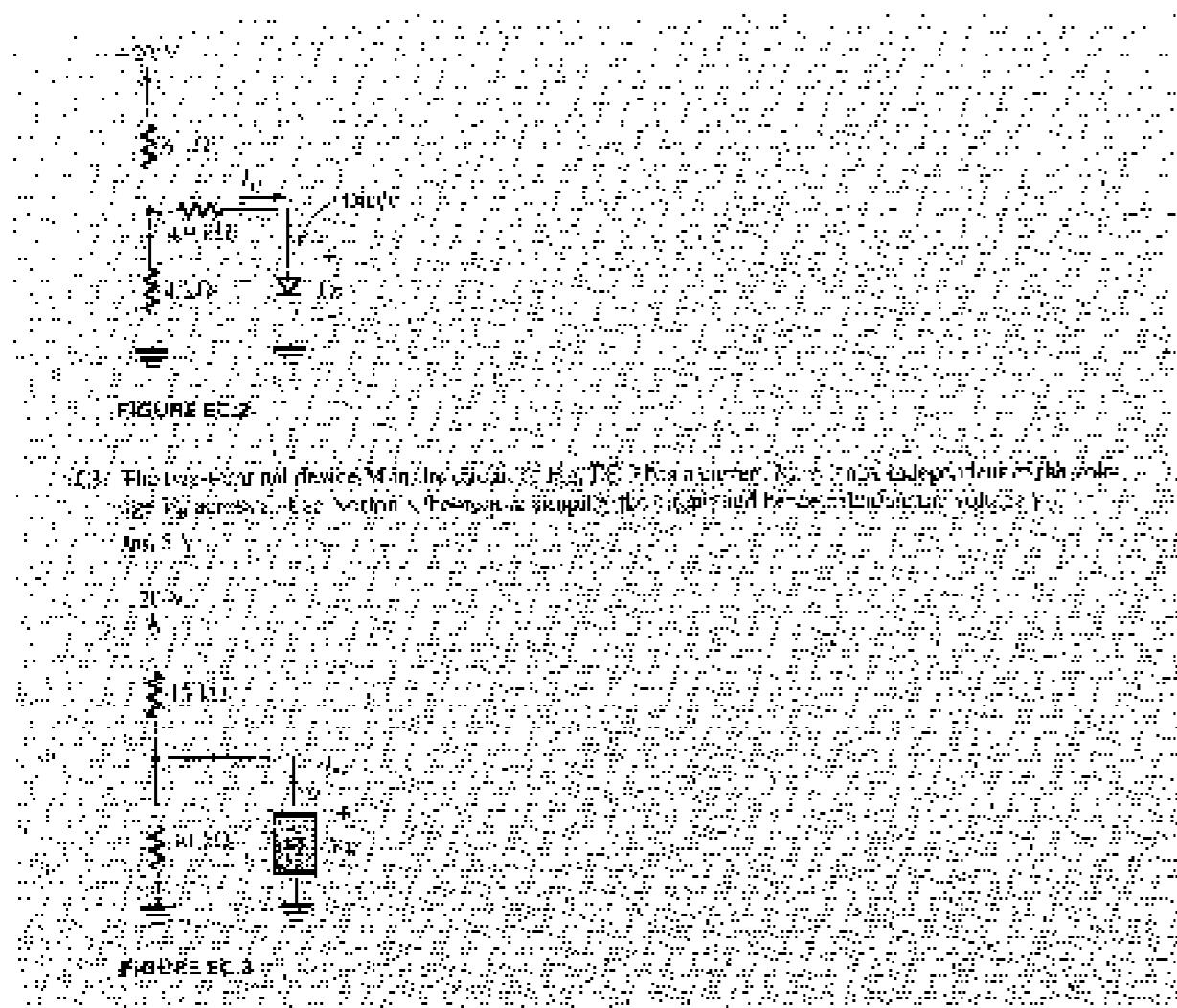
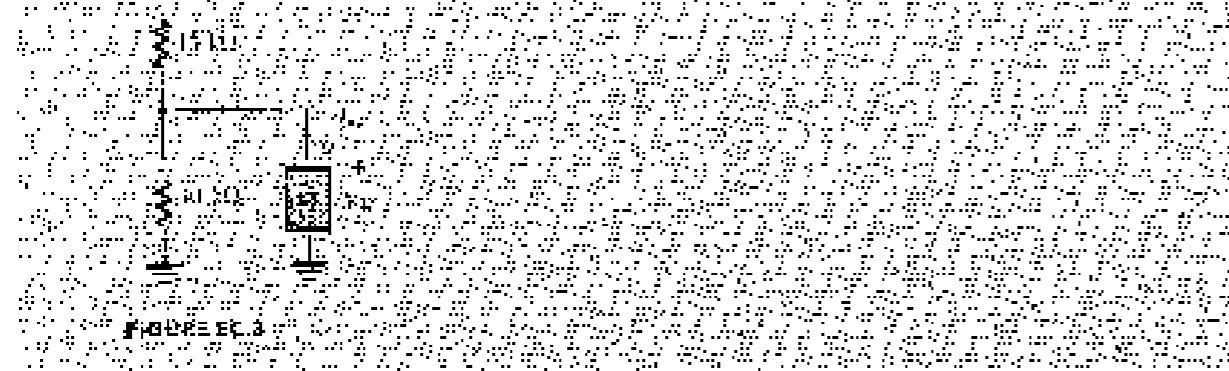


FIGURE PC 3

C.3 The long-channel device shown in Fig. C-3 is a JFET. It has a drain-to-gate voltage V_{DS} , a drain-to-source voltage V_{DS} , and a gate-to-source voltage V_{GS} . The drain current I_D is given by

$$I_D = I_{DSS} \left[2 \frac{V_D}{V_P} - \left(\frac{V_D}{V_P} \right)^2 \right] \quad \text{for } V_D \leq V_P$$

$$I_D = I_{DSS} \quad \text{for } V_D \geq V_P$$



PROBLEMS

C.1 Consider the Thévenin equivalent circuit characteristics of V_T and Z_T . Find the open-circuit voltage V_o , and the short-circuit current I_{SC} , the current that flows when the terminals are shorted together. Express Z in terms of V_T and I_{SC} .

C.2 Repeat Problem C.1 for a Norton equivalent circuit characterized by I_{SC} and Z .

C.3 A voltage divider consists of a 9-kΩ resistor connected to +10V and a resistor of 1 kΩ connected to ground. What is the Thévenin equivalent of this voltage divider?

What output voltage results if it is loaded with 1 kΩ? Calculate this two ways: directly and using your Thévenin equivalent.

C.4 Find the output voltage-to-current resistance of the circuit shown in Fig. PC.3 by employing a succession of Thévenin equivalents.

C.5 Repeat Example C.2 with a resistance R_2 connected between D and ground in Fig. C-5 (i.e., move R_2 directly connecting the bias bias indicated in Fig. C-5).

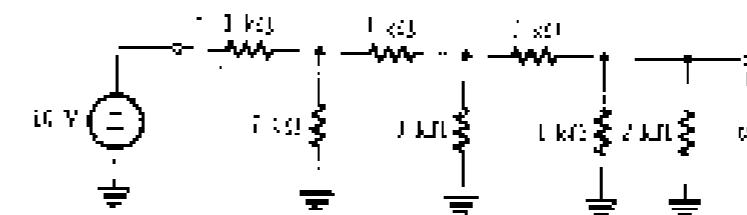
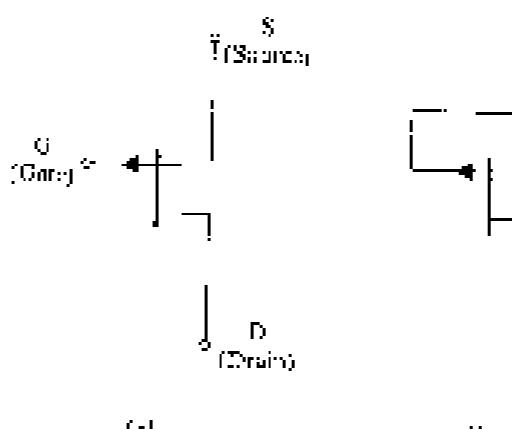


FIGURE PC 4

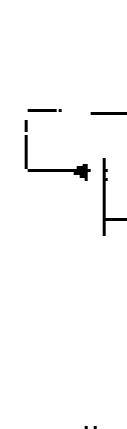
C.6 Figure PC.6(a) shows the π -equivalent symbol of a device known as the junction field-effect transistor (JFET). As indicated, the JFET has three terminals. When the gate terminal G is connected to the source terminal S, the two-terminal device shown in Fig. PC.6(b), with the characteristic given by

$$I = I_{DSS} \left[2 \frac{V_D}{V_P} - \left(\frac{V_D}{V_P} \right)^2 \right] \quad \text{for } V_D \leq V_P$$

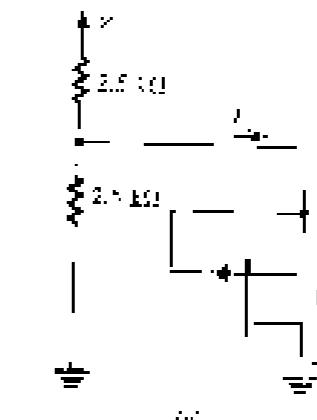
$$I = I_{DSS} \quad \text{for } V_D \geq V_P$$



(a)



(b)



(c)

FIGURE PC 6

where I_{DSS} and V_P are positive constants for the particular JFET. Now consider the circuit shown in Fig. PC.6(c) and let $V_S = 5$ V and $I_{DSS} = 2$ mA. For $V_D = 0$ V show that the JFET is operating in the constant-current mode and find the voltage across it. What is the minimum value of V_D for which this mode of operation is maintained for $V_G = 2$ V and the values of I and V ?

APPENDIX D

Single-Time-Constant Circuits

INTRODUCTION

Single-time-constant (STC) circuits are those circuits that can be reduced to one reactive component (inductance or capacitance) and one resistance. An STC circuit formed of an inductance L and a resistance R has a time constant $\tau = L/R$. The time constant τ of an STC circuit composed of a capacitor C and a resistance R is given by $\tau = CR$.

Although STC circuits are quite simple, they play an important role in the design and analysis of linear and digital circuits. For instance, the analysis of an amplifier circuit can usually be reduced to the analysis of one or more STC circuits. For this reason, we will review in this appendix the process of evaluating the response of STC circuits to sinusoidal and relay input signals such as step and pulse waveforms. The latter signal waveforms are encountered in some amplifier applications but are more important in switching circuits, including digital circuits.

D.1 EVALUATING THE TIME CONSTANT

The first step in the analysis of an STC circuit is to evaluate its time constant τ .

Reduced the circuit of Fig. D-1(a) to an STC circuit and find its time constant.

Solution

The reduction process is illustrated in Fig. D-1 and consists of repeated applications of Thevenin's theorem. From the final circuit (Fig. D-1(c)), we obtain the time constant as

$$\tau = C \left\{ R_2 \left(R_1 + \frac{R_3}{R_4} \right) \right\}$$

D.1.1 Rapid Evaluation of τ

In many instances, it will be important to be able to evaluate rapidly the time constant τ of a given STC circuit. A simple method for accomplishing this goal consists first of reducing the excitation to zero; that is, if the excitation is by a voltage source, short it out; if by a current

D.1 EVALUATING THE TIME CONSTANT D-2

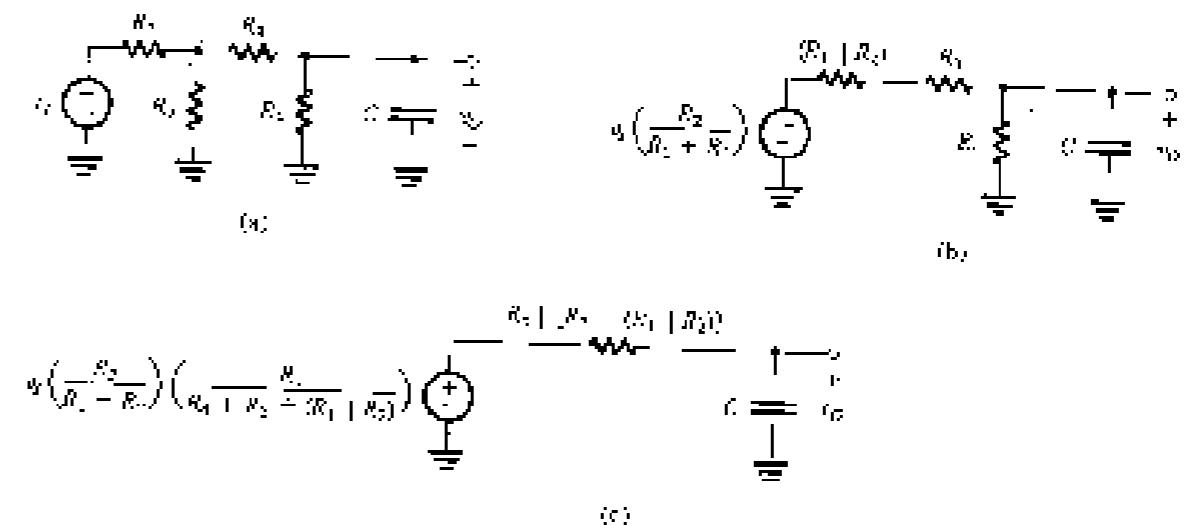


FIGURE D-1 The reduction of the circuit in (a) to the STC circuit in (c) through repeated applications of Thevenin's theorem.

source, open it. Then if the circuit has one reactive component and a number of resistances "grabbled" of the two terminals of the reactive component (resistance or inductance) and find the equivalent resistance R_{eq} easily be convenient. The time constant is then either $C_{eq}R_{eq}$ or CR_{eq} . As an example, in the circuit of Fig. D-1(a) we find that the capacitor C "sees" a resistance R_2 in parallel with the series combination of R_1 and R_3 in parallel with R_4 ; thus

$$R_{eq} = R_2 \left(R_1 + \frac{R_3}{R_4} \right)$$

and the time constant is CR_{eq} .

In some cases it may be found that the circuit has no resistances and a number of capacitors or inductances. In such a case the procedure should be reversed; that is, "grab hold" of the reactance terminals and find the equivalent capacitance C_{eq} or equivalent inductance L_{eq} seen by this resistance. The time constant is then found as $C_{eq}R$ or L_{eq}/R . This is illustrated in Example D-2.

Find the time constant of the circuit in Fig. D-2.

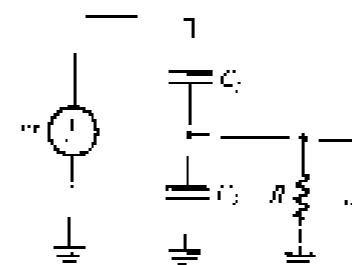


FIGURE D-2 Circuit for Example D-2.

Solution

After connecting the circuit to zero by short-circuiting the voltage source, we see that the total source is "seen" an equivalent capacitance $C_1 + C_2$. The time constant τ is given by

$$C = \{C_i\} = \{c_{ij}\}_{j=1}^m$$

Finally, in some cases an SVC circuit has more than one resistor and more than one inductor (i.e., more than one inductance). Such cases require some criteria used to simplify the circuit, as illustrated by Examples D-3.

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Here we show that the response of the circuit in Fig. 7.3(a) can be obtained using the methods of SFC circuits.

Solutions

The analysis steps are illustrated in Fig. D.2. In Fig. D.2(b) we show the circuit formed by two parallel coupled voltage sources. The transfer L_{out} and conference $L_{\text{in}} + L_{\text{out}}$ or L_{out} of the equivalent single balanced voltage source.

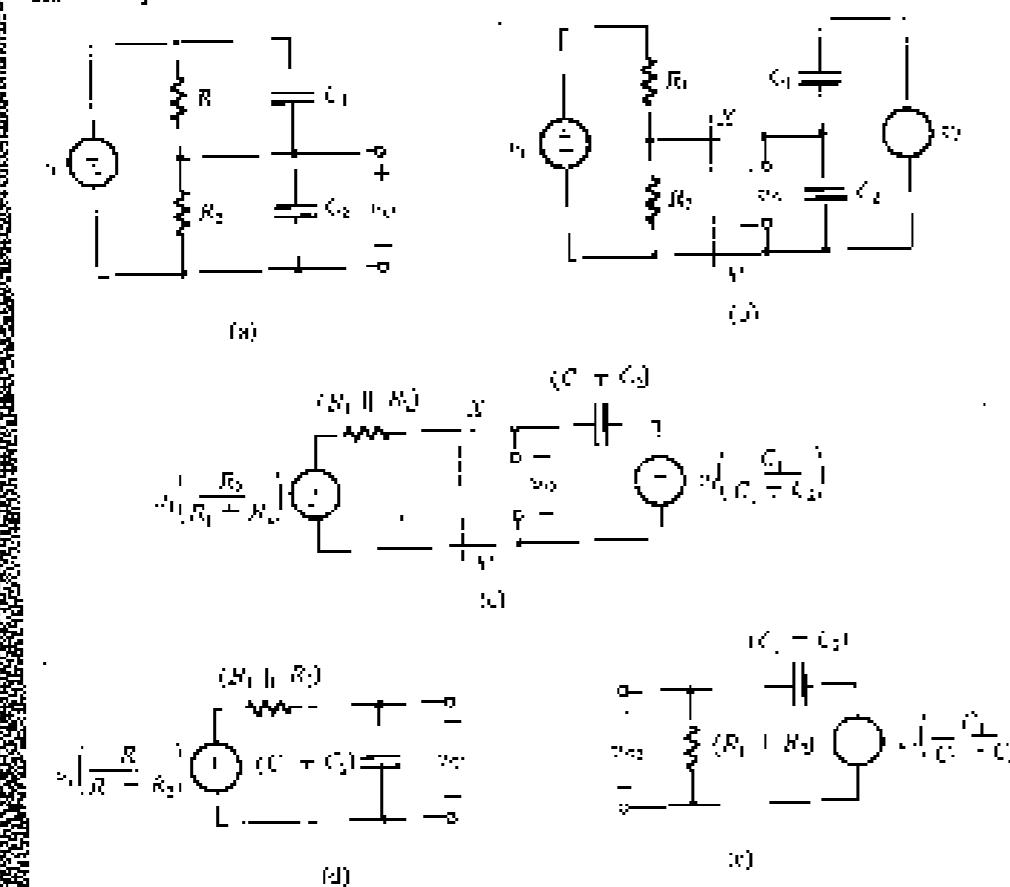


FIGURE D.3 The responses of the circuit in Fig. D.2 can be found by superposition, that is, by summing the responses of the circuit to (D) and (E).

of the currents is in Fig. 10(b), and 21(b). The "brick" employed to obtain the arrangement in Fig. 10(b) is a very useful one.

Application of Faraday's theorem to the circuit to the left of the line A_2A' and then to the circuit to the right of that line results in the circuit of Fig. D.1(c). Since that is a closed circuit, the response may be obtained using the principle of superposition. Specifically, the output voltage v_{21} will be the sum of the two components v_{211} and v_{212} . The first component, v_{211} , is the output due to the left-hand-side voltage source with the other voltage source reduced to zero. The circuit for calculating v_{211} is shown in Fig. D.1(d). It is an RCL circuit with a time constant given by

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Similarly, the second component v_{out} is the output obtained with the left hand side voltage source reduced to zero. It can be calculated from the circuit of Fig. 10.3(c), which is an NTC circuit with the same structure as Fig. 10.3(a).

Finally, it should be observed that the fact that the circuit is an STC one can also be ascertained by setting the independent source v_1 in Fig. 7.6(a) to zero. Now, the time constant is then un-perturbed (see 7.3).

3.2 CLASSIFICATION OF STC CIRCUITS

STC circuits can be classified into two categories, low-pass (LP) and high-pass (HP) types, with each category displaying distinctly different signal responses. The task of determining whether an STC circuit is of LP or HP type may be accomplished in a number of ways, the simplest of which uses the frequency-domain response. Specifically, low-pass circuits have $\text{d.c. signals with zero frequency}$ and attenuate high frequencies, with the transmission being zero at $\omega = \infty$. Thus we can test for the circuit type either at $\omega = 0$ or at $\omega = \infty$. At $\omega = 0$ capacitors should be replaced by open circuits ($1/j\omega C = \infty$) and indicators should be replaced by short circuits ($j\omega L = 0$). Then if the output is zero, the circuit is of the high-pass type, while if the output is finite, the circuit is of the low-pass type. Alternatively, we may test at $\omega = \infty$ by replacing capacitors by short circuits ($j\omega C = 0$) and inductors by open circuits ($j\omega L = \infty$). Then if the output is finite, the circuit is of the LP type, whereas if the output is zero, the circuit is of the HP type. In Table D.1, which provides a summary of these results, c.c. stands for *closed circuit* and o.c. for *open circuit*.

Figure D.4 shows examples of low-pass SIC circuits, and Fig. D.5 shows examples of high-pass SIC circuits. For each circuit we have indicated the input and output variables of interest. Note that a given circuit can be of either category, depending on the input and output variables. The reader is urged to verify, by the methods of Table D.1, that the circuits of Figs. D.4 and D.5 are correctly classified.

TABLE C-1. Results of Preliminary Test of TCE Circuit

Test At	Replace	Circuit Is \oplus If	Circuit Is $\oplus\bar{P}$ If
$x_1 = 1$	0-by-0s 1-by-0s	output is finite	output is zero
$x_1 = 0$	0-by-0s 1-by-0s	output is finite	output is finite

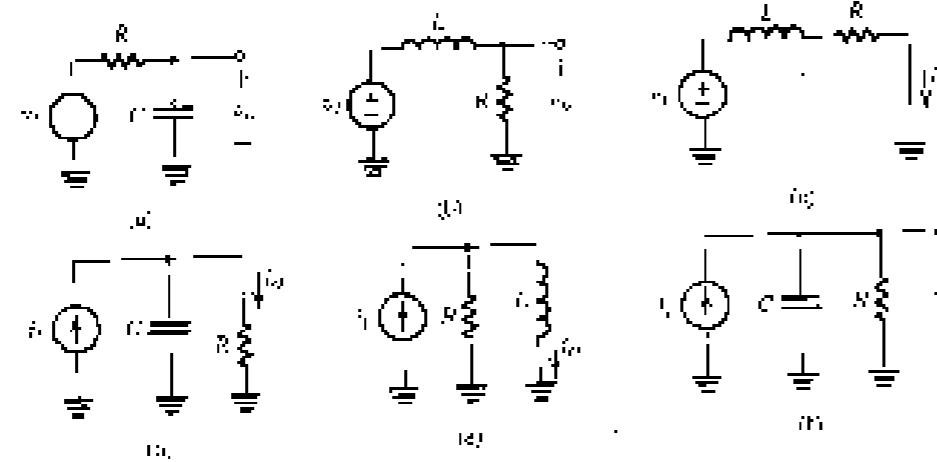


FIGURE D.4 STC circuits of the low-pass type.

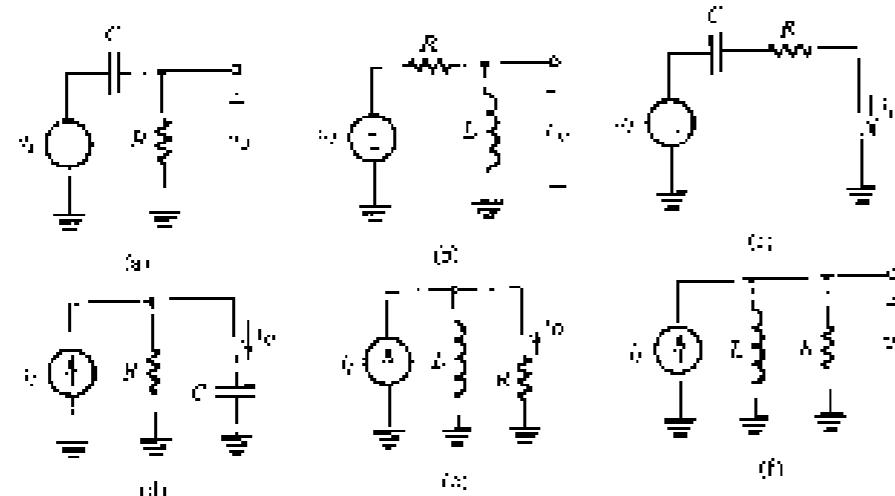
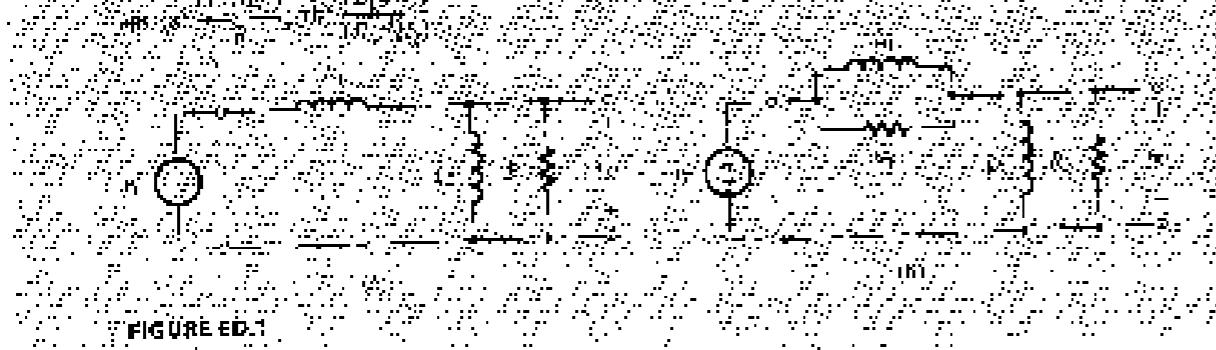


FIGURE D.5 STC circuits of the high-pass type.

EXERCISES

2. Find the transfer function $T(j\omega)$ for each circuit in Fig. D.4. The voltage v_s is the input, and v_o is the output.



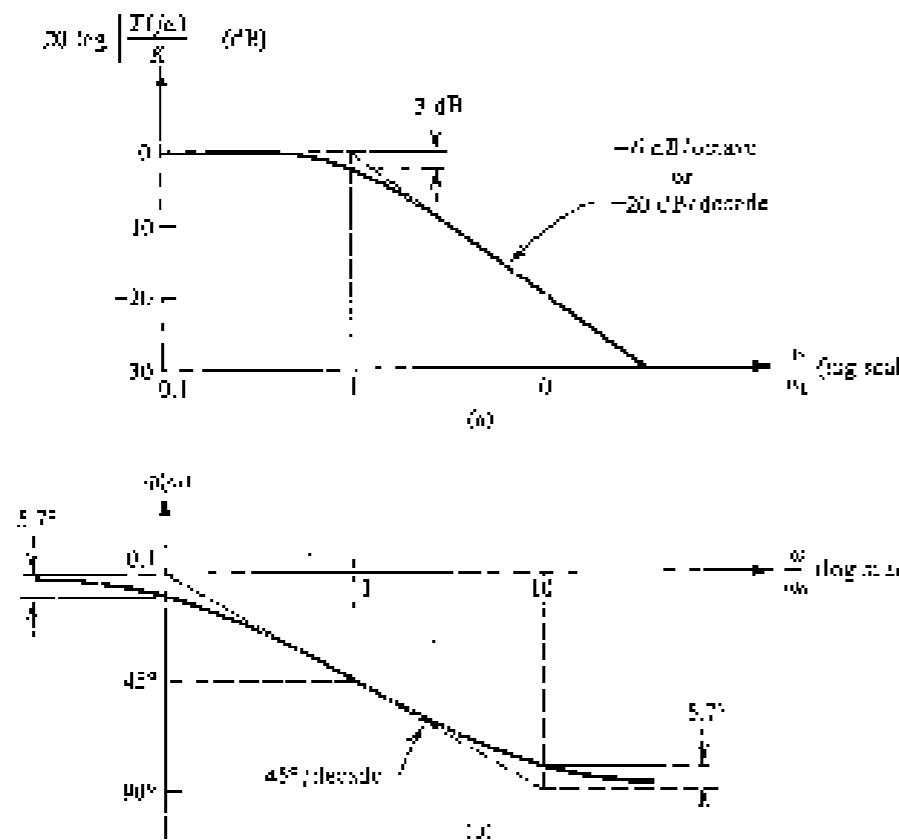


FIGURE D.6 (a) Magnitude and (b) phase response of SPC circuit of the low-pass type.

To verify that this value is correct, simply substitute $\omega = \omega_0$ in Eq. (D.3) to obtain

$$T(j\omega_0) = K \sqrt{2}$$

This is $|K| = \omega_0$, the gain drops by a factor of $\sqrt{2}$ relative to the dc gain, which corresponds to a 3-dB reduction in gain. The corner frequency ω_0 is appropriately referred to as the 3-dB frequency.

Similar to the magnitude response, the phase response curve, shown in Fig. D.6(b), is closely defined by straight-line asymptotes. Note that at the corner frequency the phase is -45° , and the for $\omega > \omega_0$ the phase approaches -90° . Also note that the -45°/decade straight line approximates the phase function, with a maximum error of 5.7°, over the frequency range 0.1 to 100 rad/s.



Consider the circuit shown in Fig. D.7(a), where an ideal voltage amplifier of gain $K = 100$ has a small (10-pF) bypass capacitor connected to its feedback input. The input voltage is fed by a voltage source having a source resistance of 100 kΩ. Show that the frequency response V_o/V_i of this amplifier is equivalent to that of an STC circuit, and sketch its magnitude response.

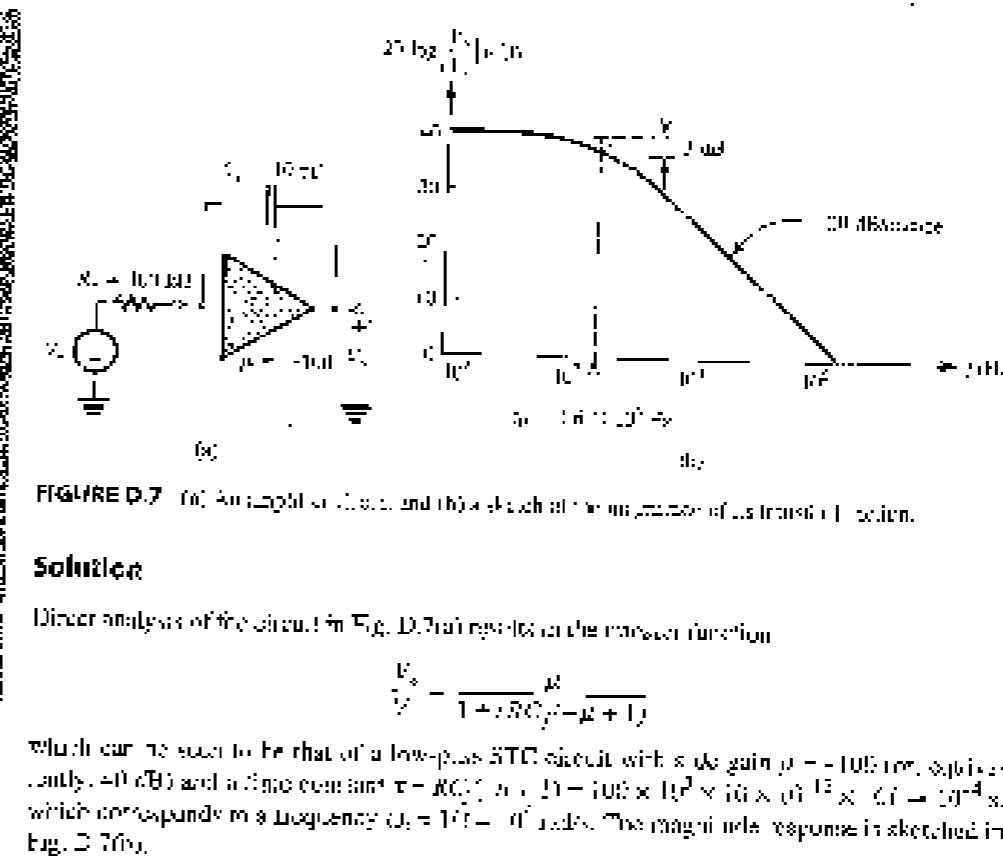


FIGURE D.7 (a) An op-amp circuit, and (b) a sketch of the magnitude of its transfer function.

Solution

Direct analysis of the circuit in Fig. D.7(a) yields the transfer function

$$\frac{V_o}{V_i} = \frac{K}{1 + j\omega RC_f / (K + 1)}$$

which can be seen to be that of a low-pass STC circuit with a dc gain $K = 100$ (or, equivalently, +40 dB) and a time constant $\tau = RC_f / (K + 1) = 100 \times 10^3 \times 10 \times 10^{-12} \times 100 = 10^{-3}$ s, which corresponds to a frequency $\omega_0 = 1/\tau = 10^4$ rad/s. The magnitude response is sketched in Fig. D.7(b).

D.3.2 High-Pass Circuits

The transfer function $T(j\omega)$ of an STC high-pass circuit always can be expressed in the form

$$T(j\omega) = \frac{K}{j + j\omega/\omega_0}, \quad (D.6)$$

where, for physical frequencies $\omega = \text{rad/second}$,

$$T(j\omega) = \frac{K}{1 + j\omega_0/\omega}, \quad (D.6)$$

where K denotes the gain as a of ω approaches infinity and ω_0 is the inverse of the time constant τ :

$$\omega_0 = 1/\tau$$

The magnitude response

$$|T(j\omega)| = \frac{K}{\sqrt{1 + (\omega_0/\omega)^2}}, \quad (D.7)$$

and the phase response

$$\phi(\omega) = \tan^{-1}(\omega_0/\omega) \quad (D.8)$$

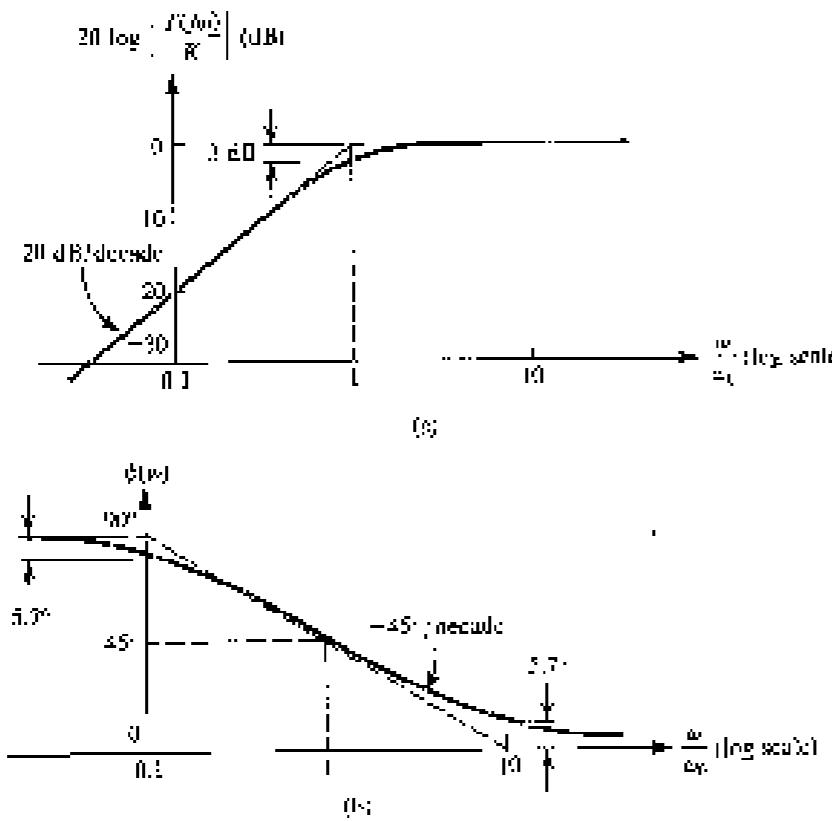


FIGURE D.8 (a) Magnitude and (b) phase response of STC circuits of the high-pass type.

are sketched in Fig. D.8. As in the low-pass case, the magnitude and phase curves are well defined by straight-line asymptotes. Because of the similarity (i.e., more appropriately, duality) with the low-pass case, no further explanation will be given.

EXERCISES

- D.3 Find the step response of the circuit shown in Fig. D.3 if the input voltage is a unit step function of height 5.



FIGURE D.3

- D.4 Find the step response of the circuit in Fig. D.4 if the input voltage is a unit step function of height 5.

$$\text{Ans. } T(s) = \frac{5}{R_1 + R_2 + s(C_1 + C_2)} \text{ sec.}$$

- D.5 From the circuit in Fig. D.5, find the capacitor values that result in a circuit having a high-pass corner frequency $\omega_h = 1/\sqrt{2}$ and a corner frequency $\omega_c = 10/\sqrt{2}$.
Ans. $C_1 = 10\text{nF}$

- D.6 Find the high-frequency gain, the 3-dB frequency f_3 , and the corner $\omega_c = 1/\text{rad/sec}$ of the capacitive coupled amplifier shown in Fig. D.6 assuming the voltage-controlled voltage source to be ideal.



FIGURE D.6

- Ans. (a) $A_H = 100$; (b) $f_3 = 100\text{Hz}$; (c) $\omega_c = 1/\text{rad/sec}$

D.4 STEP RESPONSE OF STC CIRCUITS

In this section we consider the response of STC circuits to the step-function signal shown in Fig. D.9. Knowledge of the step-response enables rapid evaluation of the response to other switching-signal waveforms, such as pulses and square waves.

D.4.1 Low-Pass Circuits

In response to an input step signal of height S , a low-pass STC circuit (with a dc gain $K = 1$) produces the waveform shown in Fig. D.10. Note that, while the input rises from 0 to S at $t = 0$, the output does not respond immediately to this transient; it simply begins to rise exponentially toward the final dc value of the input, S . In the long term—that is, for $t \gg \tau$ —the output approaches the dc value S , a manifestation of the fact that low-pass circuits faithfully pass dc.

The equation of the output waveform can be obtained from the expression

$$y(t) = Y_\infty - (Y_\infty - Y_0) e^{-t/\tau} \quad (\text{D.9})$$

where Y_∞ denotes the final value or the value toward which the output is heading and Y_0 denotes the value of the output immediately after $t = 0$. This equation states that the output of any circuit is equal to the difference between the final value Y_∞ and a quantity that is initially equal to $Y_0 - Y_\infty$ and is "shrinking" exponentially. In our case, $Y_\infty = S$ and $Y_0 = 0$; thus,

$$y(t) = S(1 - e^{-t/\tau}) \quad (\text{D.10})$$

$y(t)$

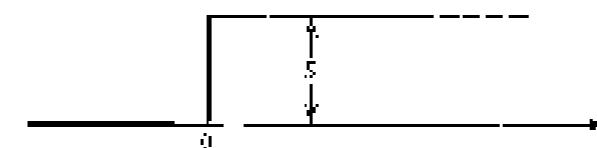
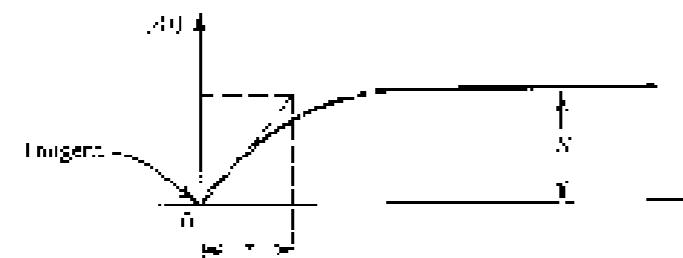
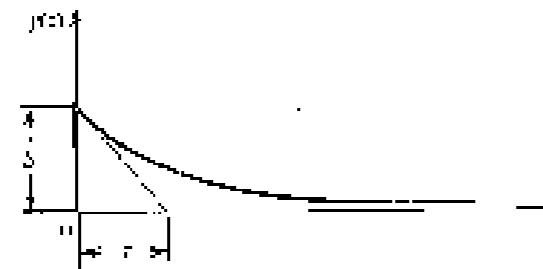


FIGURE D.9 A step-function signal of height 5.

FIGURE D.10 The response of a low-pass SIC circuit excited by a unit step signal S .FIGURE D.11 The response of a high-pass SIC circuit excited by a unit step signal S .

The reader's transient v_0 is drawn to the slope of the tangent to $y(t)$ at $t = 0$, which is indicated in Fig. D.10.

D.4.2 High-Pass Circuits

The response of an SIC high-pass circuit with a high-frequency gain $K = 1$ to an input step of height S is shown in Fig. D.11. The high-pass circuit faithfully tracks the transient part of the input signal (the step change), but blocks the dc. Thus the current $i(t)$ follows the input

$$V_{in} = S$$

and then it decays toward zero:

$$V_{in} = 0$$

Substituting for V_{in} and V_{out} in Eq. (D.9) results in the output $y(t)$:

$$y(t) = S e^{-t/\tau} \quad (D.11)$$

The reader's transient is drawn to the slope of the tangent to $y(t)$, $t = 0$, indicated in Fig. D.11.

This example is a continuation of the problem considered in Example D.3. For an input step that is $> 10\text{V}$ step, find the condition under which the output $y(t)$ is a pure step.

Solution

Following the analysis of Example D.3, with the circuit shown in Fig. D.3, we have

$$v_{in} = k [10(1 - e^{-t/\tau})]$$

where

$$k = \frac{R_2}{R_1 + R_2}$$

and

$$\tau = \frac{C_1}{C_1 + C_2(R_1 + R_2)}$$

and

$$t = (C_1 + C_2)(R_1 + R_2)$$

Thus

$$v_{in} = v_{in}^0 = v_{in}^0 e^{-t/\tau} \\ = 10k = 10e^{-t/\tau}(k_1 - k_2)$$

It follows that the current can be made a perfect step of height 10 if we arrange that

$$k_1 = k_2$$

that is, if the resistive voltage-discriminators make equal to the capacitive voltage-discriminators.

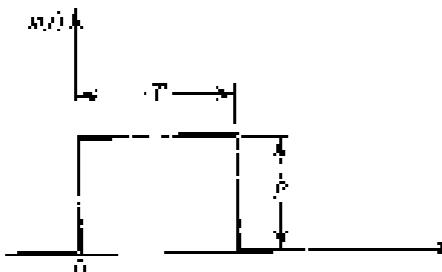
This example illustrates an important technique, namely, use of the "component exchange." An application of this technique to some of the oscillator problems in the oscilloscope probe problem is investigated in Problem D.3.

EXERCISES

- D.5 For the circuit of Fig. D.4(a), find the transient response $y(t)$ if the initial voltage across the capacitor is 10V .
- D.6 In the circuit of Fig. D.5, if $R_1 = 1\text{k}\Omega$, $C_1 = 1\mu\text{F}$, $R_2 = 10\text{k}\Omega$, and $C_2 = 10\mu\text{F}$, find the transient response $y(t)$ if the initial voltage across the capacitor is 10V .
- D.7 The circuit of Fig. D.7 is a differentiator. A signal voltage that is 10V at $t = 0$ and 0V at $t = 10\text{ms}$ is applied to the input. Find the transient response $y(t)$ if the initial voltage across the capacitor is 0V .
- D.8 For the circuit in Fig. D.8 with $C_1 = 1\mu\text{F}$, $R_1 = 1\text{M}\Omega$, $R_2 = 10\text{k}\Omega$, $C_2 = 10\mu\text{F}$, and $R_3 = 10\text{k}\Omega$, find the transient response $y(t)$ if the initial voltage across the capacitor is 0V .
- D.9 For the circuit in Fig. D.9 with $C_1 = 1\mu\text{F}$, $R_1 = 1\text{M}\Omega$, $R_2 = 10\text{k}\Omega$, $C_2 = 10\mu\text{F}$, and $R_3 = 10\text{k}\Omega$, find the transient response $y(t)$ if the initial voltage across the capacitor is 0V .
- D.10 For the circuit in Fig. D.10 with $C_1 = 1\mu\text{F}$, $R_1 = 1\text{M}\Omega$, $R_2 = 10\text{k}\Omega$, $C_2 = 10\mu\text{F}$, and $R_3 = 10\text{k}\Omega$, find the transient response $y(t)$ if the initial voltage across the capacitor is 0V .
- D.11 Show that the transient in Fig. D.11 is equal to the difference of a height S and width τ .

D.5 PULSE RESPONSE OF SIC CIRCUITS

Figure D.12 shows a pulse signal whose height is P and whose width is Z . We wish to find the response of SIC circuits to input signals of this form. Note that the first half of a pulse can be considered as the sum of two steps: a positive one of height P occurring at $t = 0$ and a

FIGURE D-12 A pulse signal with height P and width T .

negative slope of instant P occurring at $t = T$. Thus the response of a linear circuit to the pulse signal can be obtained by summing the responses to the two step signals.

D.5.1 Low-Pass Circuits

Figure D-13(a) shows the response of a low-pass STC circuit (having unity dc gain) to an input pulse of the form shown in Fig. D-12. In this case we have assumed that the time constant τ is in the same range as the pulse width T . As shown, the LP circuit does not respond immediately to the step change at the leading edge of the pulse; rather, the output starts to rise exponentially toward a final value of P . This exponential rise, however, will be stopped at time $t = T$, that is, at the trailing edge of the pulse when the input undergoes a negative step change. Again the output will respond by starting an exponential decay toward the final value of the input, which is zero. Finally, note that the area under the output waveform will be equal to the area under the input pulse waveform, since the LP circuit (in theory) passes dc.

A low-pass effect usually occurs when a pulse signal from one part of an electronic system is connected to another. The low-pass circuit in this case is formed by the output resistance (Thevenin's equivalent resistance) of the system part from which the signal originates and the input capacitance of the system part to which the signal is fed. This unavoidable low-pass filter will cause distortion—of the type shown in Fig. D-13(a)—of the pulse signal. In a well-designed system such distortion is kept to a low value by arranging that the time constant τ be much smaller than the pulse width T . In this case the result will be a slight rounding of the pulse edges, as shown in Fig. D-13(b). Note, however, that the edges are still exponential.

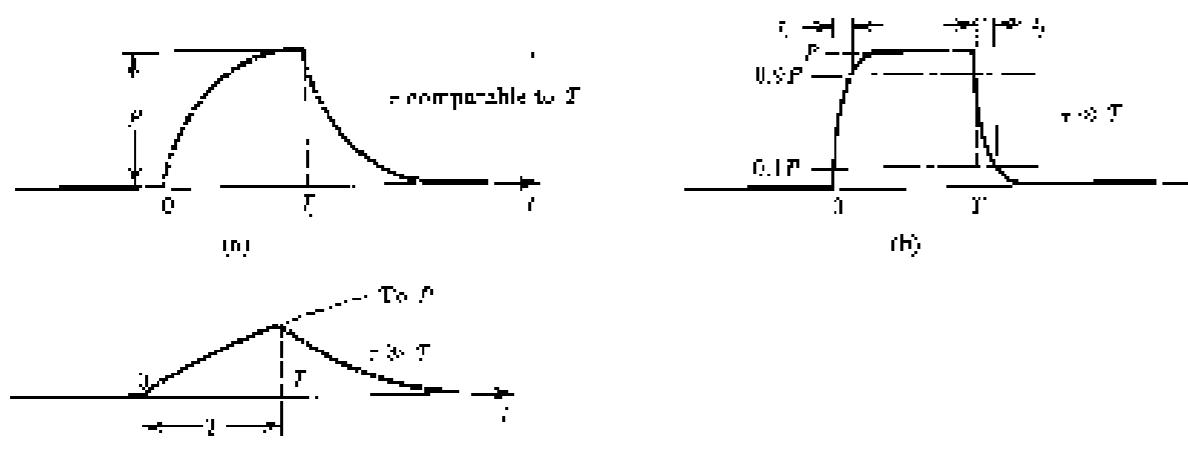


FIGURE D-13 Pulse responses of the S-L low-pass circuit.

The distortion of a pulse signal by a parasitic filter (i.e., unwanted low-pass circuit) is measured by its *rise time* and *fall time*. The rise time is conventionally defined as the time taken by the amplitude to increase from 10% to 90% of the final value. Similarly, the fall time is the time during which the pulse amplitude falls from 90% to 10% of the maximum value. These definitions are illustrated in Fig. D-13(b). By use of the exponential equations of the rising and falling edges of the output waveform, it can be easily shown that

$$t_r = t_f = 2.2\tau \quad (D-12)$$

which can be also expressed in terms of $f_r = \omega/2\pi = 1/2\pi\tau$ as

$$t_r = t_f = \frac{0.35}{f_r} \quad (D-13)$$

Finally, we note that the effect of the parasitic low-pass circuits that are always present in a system is to "slow down" the operation of the system. To keep the signal distortion within acceptable limits, one has to use a relatively large pulse width (or a given low-pass time constant).

The other extreme case—namely, when τ is much larger than T —is illustrated in Fig. D-13(c). As shown, the output waveform rises exponentially toward the level P . However, since $\tau \gg T$, the value reached at $t = T$ will be much smaller than P . At $t = T$ the output waveform starts its exponential decay toward zero. Note that in this case the output waveform bears little resemblance to the input pulse. Also note that because $\tau \gg T$ the portion of the exponential curve from $t = 0$ to $t = T$ is almost linear. Since the slope of this linear curve is proportional to the height of the input pulse, we see that the output waveform approximates the time integral of the input pulse. That is, a low-pass network with a large time constant approximates the operation of an integrator.

D.5.2 High-Pass Circuits

Figure D-14(a) shows the output of an STC HP circuit (with unity high-frequency gain) excited by the unit pulse of Fig. D-12, assuming the τ and T are comparable in value. As shown, the step transition at the leading edge of the input pulse is faithfully reproduced in the output of the HP circuit. However, since the HP circuit blocks dc, the output waveform immediately starts an exponential decay toward zero. This decay process is stopped at $t = T$, when the negative step transition of the input occurs and the HP circuit faithfully reproduces it. Thereafter, at $t = T$ the output waveform exhibits an overshoot. Then it starts an exponential decay toward zero. Finally, note that the area of the output waveform above the zero axis will be equal to that below the axis for a total average area of zero, consistent with the fact that HP circuits block dc.

In many applications an STC high-pass circuit is used to couple a pulse from one part of a system to another part. In such an application it is necessary to keep the distortion in the pulse shape as small as possible. This can be accomplished by selecting the time constant τ to be much larger than the pulse width T . If this is indeed the case, the loss in amplitude during the pulse period T will be very small, as shown in Fig. D-14(b). Nevertheless, the output waveform will swing negatively, and the area under the negative portion will be equal to that under the positive portion.

Consider the waveform in Fig. D-14(b). Since τ is much larger than T , it follows that the portion of the exponential curve from $t = 0$ to $t = T$ will be almost linear and that its slope will be equal to the slope of the exponential curve for $t > 0$, which is P/τ . We can find the value of

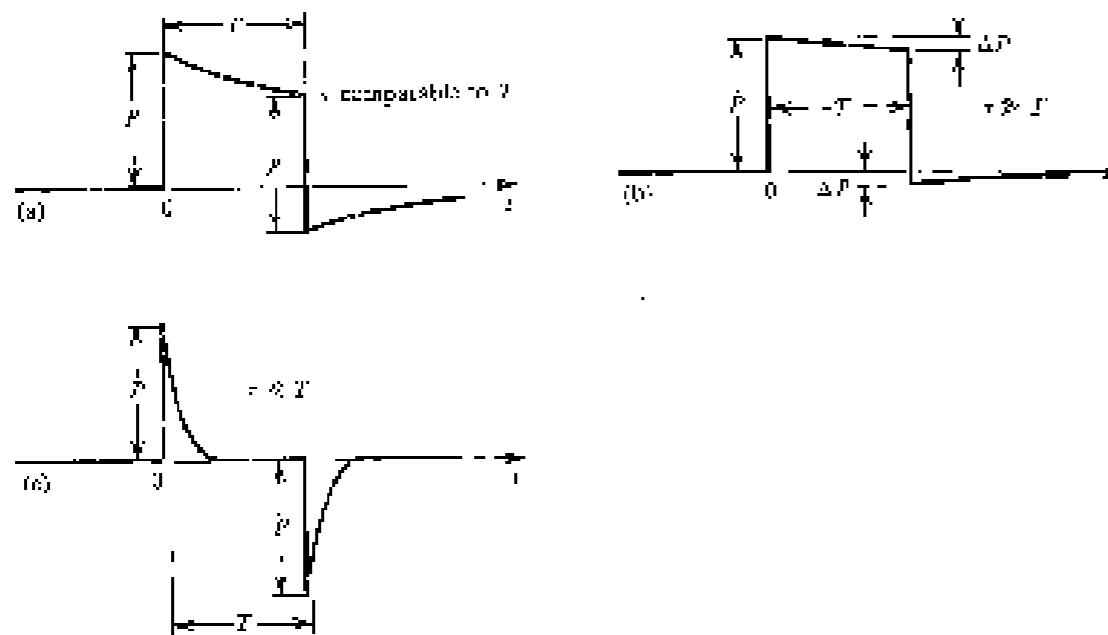


FIGURE D.14 Pulse responses of C-R-NET high-pass circuits.

the slope to determine the loss in amplitude ΔP as

$$\Delta P = \frac{P}{2} T \quad (\text{D.14})$$

The distortion effect of the high-pass circuit on the input pulse is usually specified in terms of the percentage loss in pulse height. This quantity is taken as an indication of the "ring" in the output pulse.

$$\text{Percentage loss} = \frac{\Delta P}{P} \times 100 \quad (\text{D.15})$$

Thus

$$\text{Percentage loss} = \frac{T}{\tau} \times 100 \quad (\text{D.16})$$

Finally, note that the magnitude of the undershoot, $\tau - T$, equals to ΔP .

The other extreme case—namely, $\tau \ll T$ —is illustrated in Fig. D.14(c). In this case the exponential decay is quite rapid, trailing off the output occurring almost zero shortly beyond the leading edge of the pulse. At the trailing edge of the pulse the voltage swing drops rapidly by an amount almost equal to the pulse height P . Thus, the wave form decays rapidly to zero. As seen from Fig. D.14(c), the output waveform bears no resemblance to the input pulse. It consists of two spikes: a positive one at the leading edge and a negative one at the trailing edge. Note that the output waveform is approximately equal to the time derivative of the input pulse. That is, for $\tau \ll T$ an R-C high-pass circuit approximates a differentiator. However, the resulting differentiator is not a true one; an ideal differentiator would produce two harmonics. Nevertheless, high-speed IC circuits with short time constants are employed in some applications to produce sharp pulses or spikes at the beginning of an input waveform.

EXERCISES

- D.12 Find the transfer function of the pulse-shaping circuit of Fig. D.3(a) for the case where the frequencies of the two poles are $\omega_1 = 100$ rad/sec and $\omega_2 = 1000$ rad/sec.
- D.13 Consider the pulse response of the low-pass C-R-NET circuit shown in Fig. D.3(b) for the case where the time constant $\tau = 1$ ms. Compute the error in the shape of the output pulse if the input pulse is a rectangular pulse of width $T = 1$ ms.
- D.14 The output of an input waveform is measured as the input frequency changes from 100 Hz to 1000 Hz. The output voltage V is plotted in the shape of the curve given below. Compute the time constant τ of the circuit.
- D.15 A high-gain C-R-NET circuit has a time constant of 100 ns as excited by a pulse of 1-V peak amplitude. Compute the value of the undershoot in the output waveform.
- D.16 The C-R-NET circuit of Fig. D.3(b) is used to measure the frequency of a signal. The input voltage is a rectangular pulse of width $T = 1$ ms. The output voltage is measured as the input frequency varies from 100 Hz to 1000 Hz. The output voltage V is plotted in the shape of the curve given below. Compute the time constant τ of the circuit.

PROBLEMS

- D.1 Consider the circuit of Fig. D.3(a) and the input voltage shown in (a) and (b). Here, the output, $v_o = v_o(t)$, is the sum of outputs of a low-pass and a high-pass circuit, each with time constant $\tau = (R_1 + R_2)C/2$. What is the condition on ω_1 that makes the contribution of the low-pass circuit at zero frequency equal to the contribution of the high-pass circuit at half the frequency? Show that this condition can be expressed as $C_1R_1 = C_2R_2$. If this condition applies, sketch $|V_o/V|$ versus frequency for the case $R_1 = R_2$.

- D.2 Use the voltage division rule to find the transfer function V_o/V_{in} of the circuit in Fig. D.3(b). Show that the corner frequency can be made independent of frequency if the condition $C_1R_1 = C_2R_2$ applies. Under this condition the circuit is called a compensated attenuator. Find the compensation of the compensated attenuator in terms of R_1 and R_2 .

- D***D.3 The circuit of Fig. D.3(b) is used as a compensated attenuator (see Problems D.1 and D.2) for an oscilloscope. The objective is to derive the output voltage applied to the vertical amplifier of the oscilloscope, with the signal attenuation independent of frequency. The probe line from A_1 , R_1 , and C_1 to the R_1 and C_1 model the test fixture input circuit. The input to the circuit having an input resistance of 1 M Ω and an input capacitance of 20 pF is $V_{in} = 100 \sin(2\pi f t)$ V. For the circuit in the center,

probe" that is, a probe that attenuates the input signal by a factor of 10 and the input impedance of the probe when connected to the oscilloscope, which is the impedance seen by v_o in Fig. D.3(a). Show that a impedance is 10 k Ω , which is higher than that of the test fixture itself. This is the primary advantage of the 10 k Ω probe.

- D.4 In the circuit of Figs. D.1 and D.5, let $C = 30$ pF, $C_1 = 0.01$ μ F, and $R = 1$ k Ω . At what frequency does a phase angle of 90° occur?

- *D.5 Consider a voltage amplifier with an open circuit voltage gain $A_v = 100$ V/V, $R_o = 0$, $R_i = 10$ k Ω , and an input capacitance C_{in} in parallel with R_i of 10 pF. The amplifier has a feedback resistance R_f as shown when connected between output and input C_{in} . That is, the amplifier is fed with a voltage source V_o having a resistance $R_f = 0$ k Ω . From the amplifier transfer function $V_o/V_{in}(f)$ and sketch its magnitude response versus frequency (dB vs. frequency) on a log axis.

- D.6 For the circuit in Fig. D.3(b) assume the voltage V_{in} is fed to the ideal source for transfer function $V_o/V_{in}(f)$. What type of SAW response is it? For $C = 100$ pF and $R = 100$ k Ω , find the circuit parameters.

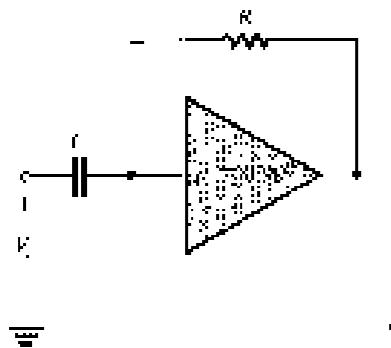


FIGURE D-6

D-7 For the circuits of Types D-6(a) and D-6(b), find $v_o(t)$ if $v_s(t) = 10\text{V}$ step, $R = 1\text{k}\Omega$, $C = 1\mu\text{F}$.

D-8 Consider the exponential response of the STC low-pass circuit in Fig. D-5 with input. In terms of the time constant τ , state the time taken for the output to reach 5V , 3V , 0.6V , and 0.01V .

D-9 The high-frequency response of an oscilloscope is specified to be such that it can STC LP circuit with a 100-MHz corner frequency. If this oscilloscope is used to display a 1-V step waveform, what rise time (10% to 90%) would you expect to observe?

D-10 An oscilloscope which can respond to like 10% of a low-pass STC circuit has a rise time of 0.1 seconds. If an input signal having a rise time of 0.001 seconds is displayed, the waveform user will have a rise time t_2 seconds, which can be found using the empirical formula $t_2 = \sqrt{t_1^2 + t_{\text{osc}}^2}$. If $t_1 = 25\text{ns}$, what is the 5-dB corner of the waveform? What is the observed rise time if the conversion ratio is 100 ns/22 us, and

one? What is the actual measured waveform when displayed for time $> 45.5\text{nS}$?

D-11 A pulse of 10-ms width and 10-V amplitude is transmitted through a system characterized by $L = 2\text{mH}$ an STC high-pass receiver with a corner frequency of 10 Hz. What output level would you expect?

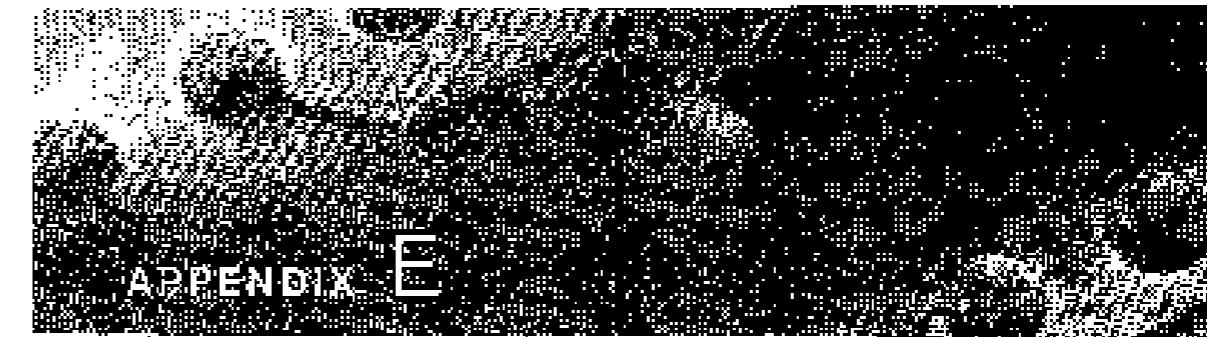
D-12 An RC differentiator having a time constant τ is used to implement a derivative operator. When a long pulse with $V > 0$ is fed to the circuit, the positive and negative peak outputs are of equal magnitude. At what pulse width does the negative output peak differ from the positive one by 10%?

D-13 A Left-pass STC circuit with a time constant of 1 ms is excited by a pulse of 0.1 V height and 1 ms width. Calculate the value of the overshoot in the output waveform. If an undershoot of 1.1 V is desired at step initial, what is the time constant requirement?

D-14 A capacitor C is used to couple the output of one amplifier stage to the input of the next stage. If the first stage has an output resistance of 2 k Ω and the second stage has an input resistance of 3 k Ω , find the value of C so that a 1-ms pulse exhibiting less than 1% step. What is the associated 3-dB frequency?

D-15 An RC differentiator is used to convert a step voltage change V to a single-pulse for a digital-to-analog converter. The logic circuit has the differentiation threshold capability to switch signals above $V/2$ as "high," or below $V/2$ as "low." What value of time constant of the circuit be to convert a step input into a pulse that will be interpreted as "high" for 10 μ s?

D-16 Consider the circuit in Fig. D-7(c) with $\rho = -0.6$, $C_2 = 100\text{ pF}$, and the amplifier being ideal. Find the value of R so that the gain $[V_o/V]$ has a 3-dB frequency of 1 MHz.



s-Domain Analysis: Poles, Zeros, and Bode Plots

In analyzing the frequency response of an amplifier, most of the work involves finding the amplifier voltage gain as a function of the complex frequency s . In this s-domain analysis, a capacitance C is replaced by an admittance sC , or equivalently an impedance $1/sC$, and an inductance L is replaced by an impedance sL . Then, using usual circuit-analysis techniques, one derives the voltage transfer function $T(s) = V_o(s)/V_i(s)$.

EXERCISE

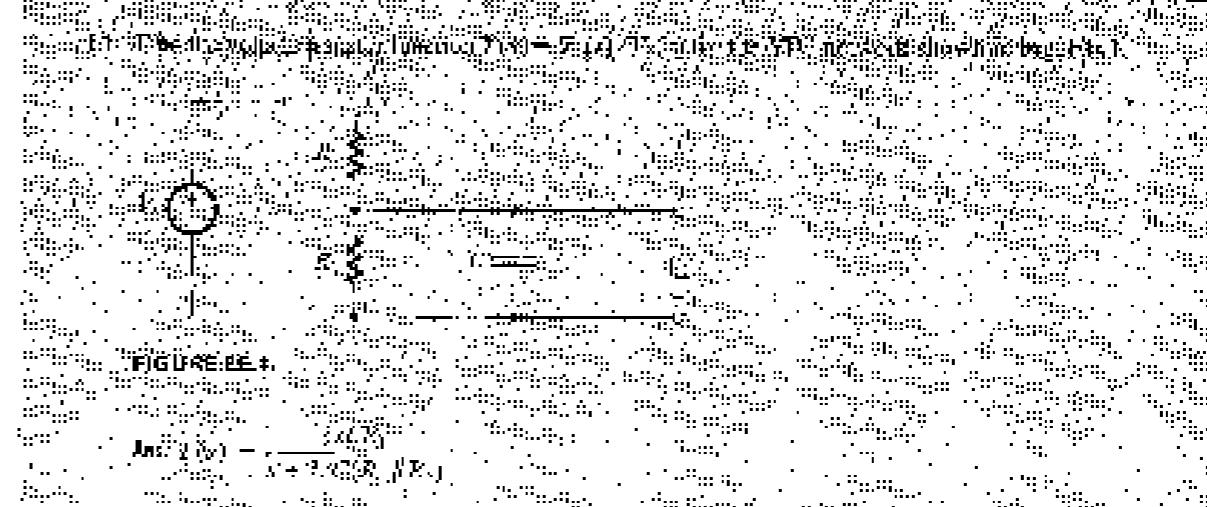


FIGURE E-1

Exercise: Find the transfer function $T(s) = V_o(s)/V_i(s)$ for the circuit shown in Fig. E-1. Assume $R_1 = 10\text{k}\Omega$, $R_2 = 1\text{k}\Omega$, $R_3 = 100\text{ }\mu\text{A}$, $L = 1\text{mH}$, and $C_1 = 10\text{nF}$.

Once the transfer function $T(s)$ is obtained, it can be evaluated for physical frequency by replacing s by $j\omega$. The resulting transfer function $T(j\omega)$ is in general a complex quantity whose magnitude gives the magnitude response (or transmission) and whose angle gives the phase response of the amplifier.

In many cases it will no be necessary to substitute $s = j\omega$ and evaluate $T(j\omega)$; rather, the form of $T(s)$ will reveal many useful facts about the circuit performance. In general, for all

the circuits dealt with in this book, $T(s)$ can be expressed in the form

$$T(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \dots + a_0}{s^n - b_{n-1} s^{n-1} - \dots - b_0} \quad (E.1)$$

where the coefficients a and b are real numbers, and the order n of the numerator is smaller than or equal to the order m of the denominator; the latter is called the order of the network. Furthermore, for a stable circuit—that is, one that does not generate signals on its own—the denominator coefficients should be such that the roots of the denominator polynomial all have negative real parts. The problem of amplitude stability is studied in Chapter 8.

E.1 POLES AND ZEROS

An alternate form for expressing $T(s)$ is

$$T(s) = a_n \frac{(s - Z_1)(s - Z_2) \cdots (s - Z_m)}{(s - P_1)(s - P_2) \cdots (s - P_n)} \quad (E.2)$$

where a_n is a multiplicative constant (the coefficient of s^n in the numerator), Z_1, Z_2, \dots, Z_m are the roots of the numerator polynomial, and P_1, P_2, \dots, P_n are the roots of the denominator polynomial. Z_1, Z_2, \dots, Z_m are called the transfer-function zeros or transmission zeros, and P_1, P_2, \dots, P_n are the transfer-function poles or the natural modes of the network. A transfer function is completely specified in terms of its poles and zeros together with the value of the multiplicative constant.

The poles and zeros can be either real or complex numbers. However, since the a and b coefficients are real numbers, the complex poles (or zeros) must occur in conjugate pairs. That is, if $s - j\beta$ is a zero, then $s + j\beta$ also must be a zero. A zero that is pure imaginary ($j\omega_0$) causes the transfer function $T(s)$ to be exactly zero at $\omega = \omega_0$. This is because the numerator will have the factors $(s + j\omega_0)(s - j\omega_0) = s^2 + \omega_0^2$, which for physical frequencies becomes $(-\omega^2 + \omega_0^2)$, and thus the transfer fraction will be exactly zero at $\omega = \omega_0$. Thus the "trap" one sees at the input of a television set is a circuit that has a transmission zero at the particular interesting frequency. Real zeros, on the other hand, do not produce transmission nulls. Finally, note that for values of s much greater than all the poles and zeros, the transfer function in Eq. (E.1) becomes $T(s) = a_n/s^n$. Thus the transfer function has a $(m-n)$ zeros at $s = \infty$.

E.2 FIRST-ORDER FUNCTIONS

Many of the transfer functions encountered in this book have real poles and zeros and can therefore be written as the product of first-order transfer functions of the general form

$$T(s) = \frac{s/\omega_p + 1}{s + \omega_p} \quad (E.3)$$

where $-\omega_p$ is the location of the real pole. The quantity ω_p , called the pole frequency, is equal to the inverse of the time constant of this single-time-constant (STC) network (see Appendix E). The constants a_0 and a_1 determine the type of STC network. Specifically, we studied in Chapter 1 two types of STC networks, low-pass and high-pass. For the low-pass

first-order network we have

$$T(s) = \frac{a_0}{s + \omega_p} \quad (E.4)$$

In this case the a is a_0 , and ω_p is the corner or 3-dB frequency. Note that this transfer function has one zero at $s = \infty$. On the other hand, the first-order high-pass transfer function has a zero at $s = 0$ and can be written as

$$T(s) = \frac{a_0 s}{s + \omega_p} \quad (E.5)$$

At this point it would be sufficiently urgent to review the material on STC networks and their frequency and pulse responses in Appendix D. Of specific interest are the plots of the magnitude and phase responses of the two special types of STC networks. Such plots can be employed to generate the magnitude and phase plots of a high-order transfer function, as explained below.

E.3 BODE PLOTS

A simple technique exists for obtaining an approximate plot of the magnitude and phase of a transfer function given its poles and zeros. The technique is particularly useful in the case of real poles and zeros. The method was developed by H. Bode, and the resulting diagrams are called Bode plots.

A transfer function of the form depicted in Fig. E.2 consists of a product of factors of the form $s + a$, where such a factor appears once if it corresponds to a zero and twice if it corresponds to a pole. It follows that the magnitude response in decibels vs. the network can be obtained by summing together terms of the form $20 \log s/a + \text{const}$, and the phase response can be obtained by summing terms of the form $\tan^{-1}(a/s)$. In both cases the terms corresponding to poles are summed with negative signs. For convenience, we can extract the constant a and write the typical magnitude term in the form $20 \log \sqrt{1 + (a/s)^2}$. On a plot of decibels versus log frequency this term gives rise to the curve and straight-line asymptotes shown in Fig. E.1. Here the low-frequency asymptote is a horizontal straight line

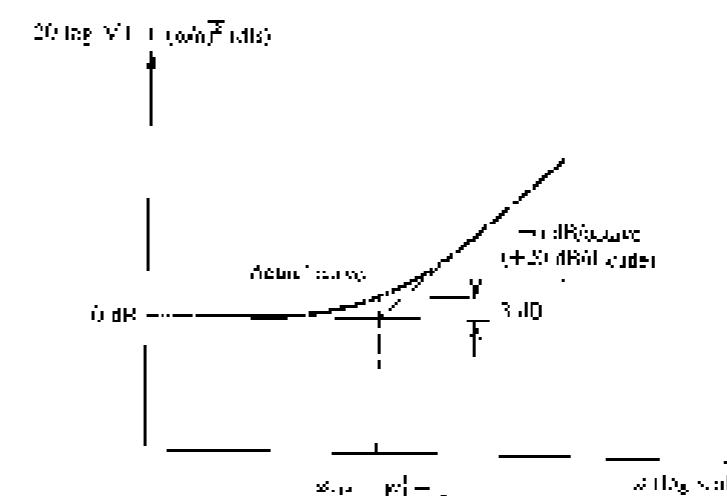


FIGURE E.1 Asymptotic approximation to the typical magnitude term. The curve shown applies for the case of one real pole; the high-frequency asymptote would be drawn with a -20-dB/decade slope.

at 0 dB level) and the high-frequency asymptote is a straight line with a slope of 6 dB/decade or, equivalently, 20 dB/decade. The two asymptotes meet at the frequency $\omega = |\omega_0|$, which is called the corner frequency. As indicated, the actual magnitude plot differs slightly from the value given by the asymptote; the maximum difference is 3 dB and occurs at the corner frequency.

For $\omega = 0$ —that is, a pole on a zero at $s = 0$ —the plot is simply a straight line of 6 dB/octave (slope intersecting the 0-dB line at $\omega = 1$).

In summary, to obtain the Bode plot for the magnitude of a transfer function, the asymptotic plot for each pole and zero is first drawn. The slope of the high-frequency asymptote of the curve corresponding to a zero is $-20, while that for a pole is $+20\text{ dB/decade}$. The various plots are then added together, and the overall curve is shifted vertically by an amount determined by the multiplicative constant of the transfer function.$

Example E.1

An amplifier has the voltage transfer function

$$T(s) = \frac{10}{(1+s/10^2)(1+s/10^4)}$$

Find the poles and zeros and sketch the magnitude of the gain versus frequency. Find approximate values for the gain at $\omega = 10$, 10^2 , and 10^4 rad/s.

Solution

The zeros are as follows: one at $s = 0$ and one at $s = \infty$. The poles are as follows: one at $s = -10^4$ rad/s and one at $s = -10^2$ rad/s.

Figure E.2 shows the asymptotic Bode plots of the different factors of the transfer function. Curve 1, which is a straight line intersecting the ω axis at 1 rad/s and having a $+20\text{ dB/octave}$ slope, corresponds to the term $(s + 10^2)$ in the numerator. The pole at $s = -10^4$ results in curve 2, which consists of two segments intersecting at $\omega = 10^2$. Similarly, the pole at $s = -10^2$ is represented by curve 3, where the intersection of the asymptotes is at $\omega = 10^4$. Finally, curve 4 represents the multiplicative constant of value 10.

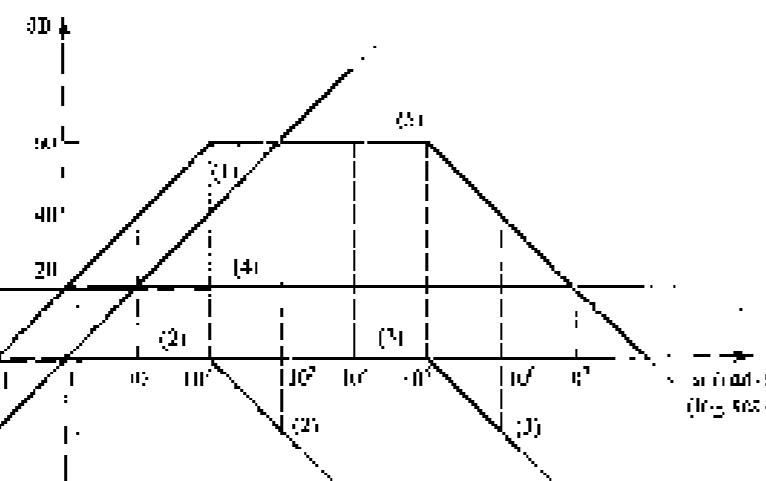


FIGURE E.2 Bode plot for Example E.1

Adding the four curves results in the asymptotic Bode diagram of the amplifier gain (curve 5). Note that since the two poles are widely separated, the gain will be very close to 10^4 dB over the frequency range 10^2 to 10^4 rad/s. At the two corner frequencies (10^2 and 10^4 rad/s) the gain will be approximately 3 dB below the maximum of 60 dB. At the corner frequencies, the values of the gain as obtained from the Bode plot and from exact evaluation of the transfer function are as follows:

ω/ω_0	Approximate Gain	Exact Gain
10^{-1}	-40 dB	-41.36 dB
10^0	0 dB	0 dB
10^1	60 dB	59.53 dB
10^2	-6 dB	-5.93 dB

We shall consider the Bode phase plot. Figure E.3 shows a plot of the typical phase term $\tan^{-1}(ws)$, assuming that w is negative. Also shown is an asymptotic straight-line approximation of the overall function. The asymptotic plot consists of three straight lines. The first is horizontal at $\phi = 0$ and extends up to $\omega = 0.1$ rad/s. The second line has a slope of -45° /decade and extends from $\omega = 0.1$ to $\omega = 10$ rad/s. The third line has a zero slope and a level of $\phi = -90^\circ$. The complete phase response can be obtained by summing the asymptotic linear plots of the phase of all poles and zeros.

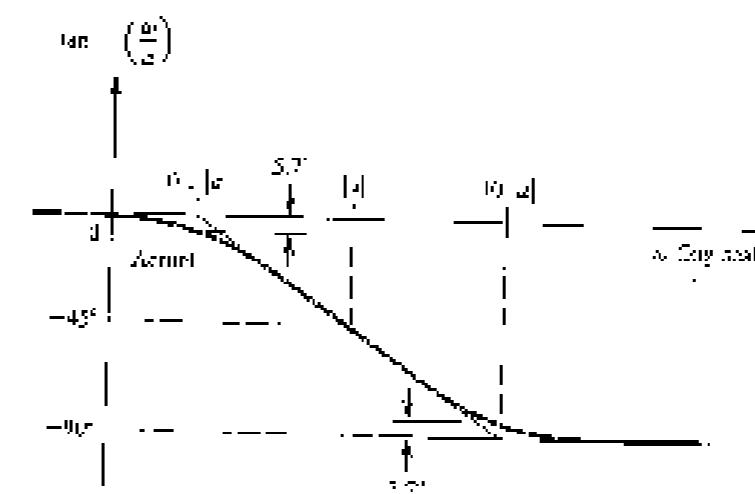


FIGURE E.3 Bode plot of theoretical phase for $\tan^{-1}(ws)$ when w is negative

Find the Bode plot for the phase of the transfer function of the amplifier considered in Example E.

Solution

The case $w < 0$ gives rise to a constant 180° phase function represented by curve 1 in Fig. E.4. The pole at $s = -10^2$ gives rise to the phase function

$$\phi_1 = -180^\circ - \frac{90}{s}$$



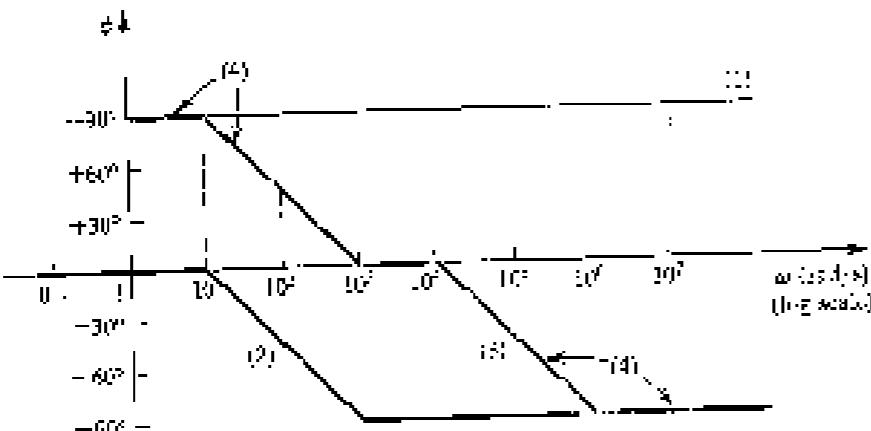


FIGURE E.4 Phase plot for Exercise E.3.

(the leading minus sign is due to the fact that the singularity is a pole). The asymptotic plot for this function is given by curve 2 in Fig. E.1. Similarly, the pole at $\tau = -1/2$ gives rise to the phase factor

$$g_1 = \tan^{-1} \frac{b_1}{a_1}$$

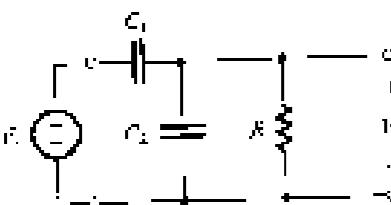
The asymptotic plot is given by curve a. The overall phase response (curve d) is obtained by direct summation of the three plots. We see that at 100 rad/s, the amplitude peaks early by 45° and at 10 rad/s the phase lags by 45°.

E4 AN IMPORTANT REMARK

For constructing Bode plots, it is most convenient to express the transfer function as a ratio of two polynomials in the form (1.1 and 1.2). The material of Figs. E.1 and E.2 and of the preceding two examples is also directly applicable.

PROBLEMS

- E.1 Find the transfer function $T(s) = V_o(s)/V_i(s)$ of the circuit in Fig. E8.1. It is an LC network. If s_0 , of what type? If $C_1 = C_2 = 0.5 \mu\text{F}$, $\omega R = 100 \text{ rad/s}$, draw the lociplot of the poles(s) and zeros(s), and sketch Bode plots for the magnitude response and the phase response.



Q8.2 Use Runge-Kutta method to solve the differential equation $y' = \frac{y}{x} + x^2$.

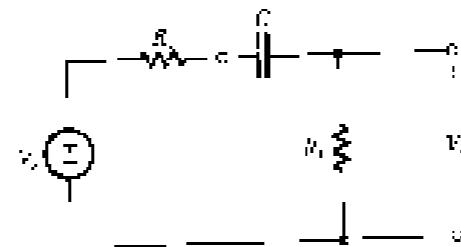


FIGURE PE.2

- (b) In this circuit, capacitor C is used to couple the signal source $V_{1,2}$ having a resistance R_1 , to a load R_L . For $R_1 = 10 \text{ k}\Omega$, set up the circuit, specifying the values of R_2 and C to satisfy the following requirements:

- (i) The load resistance should be as small as possible
 - (ii) The current gain should be at least 10% of the maximum value.
 - (iii) The output should be at least 10% of the input ...
10 Hz

- E.3** Two STC RC circuits, each with a pole at 200 rad/s and a maximum gain of unity, are connected in cascade with an intervening unity-gain buffer that ensures that they function separately. Choose one the possible options to obtain (i) a low-pass filter with a -3dB cut-off of 100 rad/s, (ii) the relevant transfer functions, (iii) the corner gain of 20 dB, (iv) the voltage gain at 100 rad/s, and (v) the voltage gain at 1000 rad/s.

- E.4 Design the transfer function in Eq. (E.5) by specifying ω_1 and ω_2 so that the gain is 10 dB at high frequencies and 1 dB at 10 Hz.

- E.5 An amplifier has a low-pass BPF Frequency response. The midband of the pass is 20 dB with a Q of 10 kHz. What is the corner frequency? At what frequency is the gain 20 dB at what frequency is the phase -60°?

- E.6** A test filter function has poles at $-j5$, $(-j7-j10)\Omega$, and $(-j2)\Omega$, and a zero at $j1-j2\Omega$. Since this function represents an actual physical circuit, where must other poles and zeros be found?

- E-7** An amplifier has a voltage transfer function $T(s) = \frac{10}{s^2 + 10^2}$. Convert this to the form convenient for constructing Bode plots (that is, place the denominator poles in the form $(1 + s/\omega_0)$). Use a \log - \log plot for the magnitude response, and use $\pm 2\text{dB}$ approximate values for

the amp. for $\omega_0 = 1, 10, 10^2, 10^3, 10^4$, and 10^5 rad/s. What would the output gain be at each of the 10^2 rad/s?

- E-8** Find the Bode phase plot of the transfer function of the amplifier considered in Problem E-7, assuming the poles along $s = 1, 10, 10^2, 10^3, \dots, 10^6$ rad/s. For each pole, calculate the actual phase at 1, 10, and 100 rad/s.

- E.3** A transfer function has the following zeros and poles: one zero at $s = 8$ and one zero at $s = -2j$; one pole at $s = -100$ and two poles at $s = -10 \pm j10$. The magnitude of the transfer function at $\omega = 10^2$ rad/s is 100. Find the transient (Section 7.2) and sketch a Bode plot for this system.

- ### **R.1.3 Section Headings for the magnitude and phase of the transfer function**

$$T(\nu) = \frac{10^2(1-\nu)/10^2}{1-\nu/10^2(1-\beta/10^2)}$$

From your sketches, determine approximate values for the magnitude and phase at $\omega = 10^3$ rad/s. What are the exact values obtained from the computer program?

- 1.1.1** A particular amplifier has a voltage transfer function $V_{out} = (0.5V_1) + j(0.5) = 0.5(1 + j0.5)^{-1}$ dB, poles and zeros. Sketch the magnitude of the gain in dB versus frequency on a logarithmic scale, indicating the gain at $10^0, 10^1, 10^2, \dots, 10^6$ Hz.

- E.7.2** A cross-coupled differentiator amplifier has a direct input gain of 100 V/V and a feed-forward gain of -10^4 V/V . The output is an in-phase signal of 10^{-3} V/V with a zero at 10^4 rad/s and a pole at 20^3 rad/s . Sketch the Bode magnitude plot for the differential gain, the common-mode gain, and the CMRR. What is the CMRR at 10^4 rad/s ? The sum of ring ratios corresponds to 3.00×10^6 (3000×10^3).

APPENDIX F

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G

Standard Resistance Values and Unit Prefixes

Discrete resistors come in standard values. Table G.1 provides the multipliers for the standard values of 5% tolerance and 1% tolerance resistors. Thus, in the kilohm range, the standard values are 1 k, 1.1 k, 1.2 k, 1.3 k, ..., 10 k. In the same range, one-tenth 1% resistors of known values of 1.00, 1.02, 1.03, 1.04, ..., 1.08 ...

Table G.2 provides the SI unit prefixes used in the book and in all modern works in English.

TABLE G.1 Standard Resistance Values

1% Resistor Values (Ω)				
5% Resistor Values (Ω)	100-124	178-309	318-549	562-996
10	100	178	319	562
11	102	182	322	576
12	105	187	332	590
13	107	191	349	604
15	110	198	348	619
16	113	200	347	624
18	117	205	365	639
20	118	210	374	665
22	121	215	384	681
24	124	221	392	698
27	129	236	404	715
30	130	237	413	742
33	133	237	422	770
39	139	244	436	768
49	149	249	443	797
44	143	252	451	800
47	147	254	464	823
51	150	267	479	845
55	154	274	487	866
62	158	280	495	887
68	162	287	511	909
74	165	294	523	929
81	169	301	536	949
87	171	309	549	976

STANDARD RESISTANCE VALUES AND UNIT PREFIXES

G-2

range of 5% resistors includes resistances of 1.0, ..., 1.2, 1.3, ..., 10. In the same range, one-tenth 1% resistors of known values of 1.00, 1.02, 1.03, 1.04, ..., 1.08, ...

Table G.2 provides the SI unit prefixes used in the book and in all modern works in English.

TABLE G.2 SI Unit Prefixes

Name	Symbol	Factor
femto	f	$\times 10^{-15}$
atto	a	$\times 10^{-18}$
zepto	z	$\times 10^{-21}$
yocto	y	$\times 10^{-24}$
petro	P	$\times 10^{15}$
exa	E	$\times 10^{18}$
zetta	Z	$\times 10^{21}$
yotta	Y	$\times 10^{24}$
tera	T	$\times 10^{12}$
peta	P	$\times 10^{15}$



Answers to Selected Problems

CHAPTER 1

- 1.1 (a) 10 mA; (b) 100 V; (c) 0.1 A, 1.2 W, 0.9 W; (d) 0.04 W, 1.8 W; (e) 0.121 W, 1.8 W
but noticeably 1/4 W; (f) 17.57, 6.7, 8.0, 8.6, 10, 10.3, 11.1, 12, 23.5, 28, 30.4, 40, 40.7, 50, 60, 70 (all in kΩ)
1.2 2.94 V, 2.23 kΩ; 2.93 V to 3.14 V, 2.11 kΩ to 1.73 kΩ; 1.9, 10.3 V; short the 10-kΩ resistor or a 157-kΩ
resistor; add a series resistor of 200 kΩ; short the 4.7-kΩ resistor with a 157 kΩ and the 10-kΩ resistor with 90 kΩ
resistor; add a series resistor of 250 kΩ; 1.13 short R_1 with a 1.1-kΩ resistor; current divider
1.14 Shunt the 1-kΩ resistor with 250 kΩ; 1.13 short R_1 with a 1.1-kΩ resistor; current divider
1.15 0.73 V and 0.15 kΩ; 0.1 mA; 1.17 1.88 μA, 2.64 V; 1.19 (a) $10^{-3} \times 10^6 \text{ Hz} \times 6.28 \times 10^3 \text{ Hz}$; (f) 10^3 rad/s
1.20 0.73 V and 0.15 kΩ; 0.1 mA; 1.21 1.88 μA, 2.64 V; 1.23 (a) 0.1 V, 10 μA, 10 kΩ
 $1.59 \times 10^3 \text{ Hz} \times 6.28 \times 10^3 \text{ Hz} = 1.21 \text{ GHz}$; (b) 1.13 V, 10 μA, 10 kΩ
1.24 10 kΩ, 1.28 dB; 1.63 V; (b) 24 V, 1.73 dB, 0.1 V; 0 V; 1 V, 1000 Hz, 10^{-3} s , 1.62, 4 kHz; 4 Hz
1.25 0.161, 1000, 1.001, 1.11001, 1.36; (c) 1.1, 4.9 mV, 2.1 mV, 1.38, 7.050 $\times 10^3$ bits per second
1.26 11 V/V or 20.8 dB; 22.8 mA; 26.8 dB, 247 mW or 23.8 dB; 120 mW; 85.8 newt, 30.2%
1.27 9 mV; 57.3 mV; 0.573 V; 1.43; (a) 8.26 mV/V or 18.2 dB; (b) 2.5 mV/V or 8 dB; (c) 0.083 V/V or -2.6 dB
1.28 0.83 V; 1.6 dB; 79.2 dB; 28.8 dB; 1.52 (a) 300 V/V; (b) 90 kΩ, $3 \times 10^4 \text{ mA}$, $9 \times 10^6 \text{ W/W}$; (c) 607 kΩ;
(d) 553.7 V/V; (e) 100 kΩ, 2000, 761 V/V; 1.92 Average amplifier; (f) -100 kΩ, $R_s = 100 \times A_{v2} = 121 \text{ V/V}$
1.30 0.4 V - 1.0 V; 1.69, 0.61 μF, 1.72, 0.51/kΩ, 1.73, 18.3 pF, 0.26 pF, 1.76, 20 dB; 3/4 dB; 40 dB; 0.7 dB;
20 dB; 0.4 dB; -20 dB; 8900 Hz; 1.77, 1.73; $C_s(R_1R_2 + R_1 + 1/(C_s(R_1 + R_2)))$, 50 Hz; 16 kHz
1.31 1.6 V, 1.3 V, 1.82; (a) 1.5 V, 1 V; (b) 2.06 V; (c) -5.5 V, 1.81; (d) 0.4 V, 0.4 V; (b) 8 mW; (c) 1.12 mW;
(d) 32.8 ps; (e) 0.545 V, 3 V, 3 V, 0.455 V; (b) 6; (c) 10.8 mW, 2.88 mW, 1.88, 25 mW, 5.52 A
1.32 0.01 V/V, 2.5 A, $G_vR_o = 100000 \text{ V/V}$; 2.8 (a) -10 V/V, 10 kΩ; (b) -10 V/V, 10 kΩ; (c) -10 V/V, 10 kΩ;
-10 V/V, 10 kΩ; 2.11, 0.0, -1 V/V; (d) -10 V/V; (e) -100 V/V; (f) -10 V/V

CHAPTER 2

- 2.1 .001 V/V, 2.5 A, $G_vR_o = 100000 \text{ V/V}$; 2.8 (a) -10 V/V, 10 kΩ; (b) -10 V/V, 10 kΩ; (c) -10 V/V, 10 kΩ;
-10 V/V, 10 kΩ; 2.11, 0.0, -1 V/V; (d) -10 V/V; (e) -100 V/V; (f) -10 V/V
2.12 $R_1 = 20 \text{ kΩ}$, $R_2 = 100 \text{ kΩ}$, 2.14, $R_1 = 500 \text{ kΩ}$, $R_2 = 10 \text{ kΩ}$; 500 kΩ, 2.16, 2/3%; -110.5 to 90.5
2.18 0 V, 5 V, -4.9 V; -5.1 V; 2.20 (a) $R_1 = 1 \text{ kΩ}$, $R_2 = 100 \text{ kΩ}$; (b) -90.8 V/V; (c) 8.9 kΩ, 2.21, +10 mV
2.23 $R_h = R_1 + R_2/(1 - A)$; 2.26, 500 mV/V, 2.27, A = 1 - R_2/R_1 or $1/(1 - A)/100$; $2 \times 10^4 \text{ V/V}$
2.28 100 kΩ, 100 kΩ; -100 Ω; 2.29 (a) $R_1R_2R_o/A$; (b) $1/2(4R_1R_2)$; (c) - R_1 , -21R₁, -4R₁, -3R₁; 2.31 (a) 0.57 kΩ;
(b) 0.1 to +0.1 mA; (c) 0.02, 20 mA; 2.36 $v_{o1} = v_1 - v_2/2$, 1.5 V, 1.3 V; $R_1 = 20 \text{ kΩ}$, $R_2 = 120 \text{ kΩ}$; $R_o = 40 \text{ kΩ}$
2.39 12.8 kΩ, 246 $R = 100 \text{ kΩ}$; Min. 2.50 $v_{o1} = v_1 - v_2 - 4 \sin(2\pi \times 1000t)$; 2.51 $v_{o1}/v_{o2} = 1/x_1 + 1/x_2$
add 0.5 kΩ to each, with ground tied end-to-end; 2.53 (a) 0.049 V, 0.689 mA; 0.049 mA; (b) 10 V; 10 mA, 0 mA
2.54 $a_x/a_y = 1/(1 + 1/A)$; 0.999, -0.1%, 0.999, -0.1%; 2.56, 6.33 V/V; short R_1 with $R_{o1} = 36 \text{ kΩ}$
0.09 V/V; 11.1 V/V, 2.59, -0.714 mV + 10.711 V; 1.0; 1 V, 2.12, $v_{o1} = v_1 - v_2/2$; $R = 2.61$, $R_1 = R_2$
2.66 6.8 dB, 2.68, 0.1, 0; (b) 5 V to +5 V; (c) 1.0, -50 to -50 V, 2.73; (d) 0.14, -0.12 V; 1.4, 1.14 V
2.76 $R_1 = 100 \text{ kΩ}$ plus 0.5 kΩ fixed; $R_2 = 50 \text{ kΩ}$; $R_3 = 100 \text{ kΩ}$; 2.77 (a) 4.0 V (peak-to-peak);

- 3.0 V (peak-to-peak) of opposite phase, 6.0 V (peak-to-peak); (b) 0 V/V; (c) 56 V (peak-to-peak), 19.8 V (rms);
2.80, 86 dB, $\leq 0.1 \text{ V}$; 16 MHz, 7.33, 47.6 kHz, 13.9 V/V, 1.98 V/V, 3.26, 40 V/V, 3.89, $\tan(\sqrt{2} - 1)^{1/2} / f_1$;
(b) 10 kHz, (d) 61.4 kHz, about six times greater; 2.91 (a) $f_1/(1 - K_1)Rf_1/(1 + K_1)$; (b) f_1/K_1 , f_2 noninverting
preferred at low gains; 2.92 Per each, $f_{inj} = f_1/f_2 = 2.99$ Hz, 31.8 kHz; (b) 0.735 V; (c) 0 to 200 kHz;
(d) 1 V peak, $\geq 10^3$, 1.4 mV, 2.765 to 12.5 to 57.5 mV; Add a 5-kΩ resistor in series with the positive input terminal,
1.0 mV; add 5 kΩ resistor in series with the negative input terminal, 2.167, 4.54 mV, 2.110, 6.0, 10.0 mV;
(b) 0.2 V; (c) 10 kΩ, 10 mV; (d) 110 mV, 2.114, 20 kHz, 1.59 μs, 2.118, 100 pulses, 2.119, V_o/V_i ; (e) 2.119;
 $18_p^2 R_o \cdot 10^3 \cdot 1.4 R_o C_o R_o = 10^3 \text{ kΩ}$; 2.121, 1.29 kHz; 2.121, 1.29 kHz; (f) 29.8 kHz, 2.121, 1.29 kHz; (g) 1 V (peak-to-peak);

CHAPTER 3

- 3.1 The diode can be reversed biased and thus no current would flow; or forward biased where current would flow:
(a) 0 A; 1.5 V; (b) 1.5 A; 0 V; 3.2 (a) -3 V; 0.6 mA; (b) -45 V; 0 mA; (c) 13 V; 0.6 mA; (d) 3 V;
0 mA; 3.5, 100 mA; 3.5 mA; 100 mA; 3.5, 100 mA; 3.5, 50 kΩ; 3.9, 0.1 V; 0.5 mA; (f) 1.67 V; 0 A;
3.10 (a) 4.5 V; 0.225 mA; (b) 2 V; 0 A; 3.11, 3 V; 1.5 V; 40 mA; 1.5, 29.67 V; 2.75 Ω, 0.75 A;
26.82 V, 30 V, 3.54, 29.53; 1.76 mA; 1 A; 27 V; 3.16 red lights; neither lights; green light; 3.18, 31.5 mV;
 1.2×10^6 ; 3.20×10^{11} A; 7.40 mA; 2/3.2 mA, 3.35 mA; 91.65 μA, 51.6 mV; 3.22, 3.81 mA; -22.8 mV
3.26, 3.1142, 3.27, 1.91, 678 mV; (b) 0.49 mV; (c) 511 mV; (d) 6.56 mV; (e) 0.62 mV; 3.29, 6.07 V; 3.7 W;
6.9 GW; 3.34, 0.6608 V; 0.2562 mA; 2.36, $R = 917.12$, 3.37, 0.687 V; 12.8 Ω; +29.5 mV; +14.2 mV
3.39, 0.73 V; 1.7 mA; 0.7 V, 2 mA; 2.41, 0.8 V; 3.15, 0.86 mA; 0 V; 0 A; 3.6 V; 3.16, 0.1, 0.53 mA; 2.3 V;
(f) 0 A; 3 V; (g) 0.53 mA; 2.3 V; (h) 0 A; 1 V; 3.48 (i) 0.20 mA; 0 V; (j) 0 A; 1.5 V; 3.52, 0.1 -49.8
mA; 3.76; (b) -22% to -18%; -2.616 to -2.47 V; (c) 5.3 to -1.8 mV ($a = 2$); 3.56, tan 0 V/V; (d) 0.001 V/V;
(e) 0.01 V/V; (f) 0.1 V/V; (g) 0.5 V/V; (h) 0.9 V/V; (i) 0.99 V/V; (j) 1 V/V; 2.51, 0.1 V (peak);
2.58, 157 μA; -81.3 mV -5.7%; 3.62, 15-mA supply, -10 mV/V mA, for a total output change of -50 mV
3.65, -50.12, -120.12, 3.67, 8.96 V; 0.01 V, 0.46 V, 3.70, 8.83 V; 19.13 mA; 300 Ω, 9.14 V; -6.01 V; -0.12 V;
578 Ω; 8.83 V; 40 mV/V; 37.7 mA/mA; 2.16, 16.2; V; 48.7%; 0.1 N, 5.06 V; 5.06 mA; 3.77, 16.27 V; 97.2%;
10.12 V; 10.12 mA; 3.78, 15.57 V; 94.7%; 9.4 V; 9.1 mA; 3.81, 36 V; 3.80 (m) 100.7 μH; 15.1 V; 7.1%;
23.1 mA; 448 mA; (n) 1667 μF; 16.19 V; 2.23, 1.62 mA; 12.55 mA; 3.85, 60, 83.3 μF; 1.79 V; 14.2%; 119 mA;
222 mA; (o) 833 μF; 15.49 V; 4.45%; 260 mA; 701 mA; 3.87 (p) 23.6 V; (b) 441.1 μF; (q) 32.7 V; 40 V;
(r) 0.73 A; (s) 35 A; 2.98, 0.2 V; 0.7 V; 1.7 V; 10.8 V; 0 V; 0.5 V; -0.7 V; -1.7 V; -10.8 V; trinary band; 1
3.104, 14.14 V; 3.105, 2.75 $\times 10^3$ cm²; 1.58 $\times 10^3$ cm²; 8.76 $\times 10^2$ cm²; 1.56 $\times 10^2$ cm²; 4.79 $\times 10^1$ cm²
3.117, 34 cm²/s; 12 cm²/s; 28 cm²/s; 10 cm²/s; 18 cm²/s; 6 cm²/s; 9 cm²/s; 4 cm²/s; 3.114, 1.27 V, 0.57 μm;
0.78 μm; 45.6 $\times 10^{-12}$ C; 18.2 Hz; 3.116, 16 $\times 10^{-12}$ C; 3.121, 0.72 A; 0.684 V; 2 $\times 10^{-1}$ C; 300 pF

CHAPTER 4

- 4.5 $W_o/V_o = \pm 2$; 4.6 238 Ω, 238 mV; 50, 4.5, 2.38 μm; -1.7 (a) 4.15 mA; (b) 0.8 mA; 0.93 mA; 0.9 mA
4.11 5.5 V; 500 Ω; 100 kΩ; 4.12, 2 V; 2 V, 5 V, 1 V; 4.11, 4 μm; 4.16, 0.7 V; 4.17, 100 mA to 10 kΩ; (a) 200 Ω
to 20 kΩ; (b) 500 Ω to 5 kΩ; (c) 100 Ω to 10 kΩ; 4.19, 20 kΩ; 56 V; 0.028 V⁻¹; 4.20, 500 kΩ; 50 kΩ; 200
kΩ; 1.22, 6.213 mA; 2.7%; (c) 2.6 μm; 1.26, 240 pA; 724 pA; 559 pA; 568 pA; -1.27, -3 V; -2 V; -4 V;
-7 V; -50 V; 0.02 V⁻¹; 1.29 mA/V²; 4.29, 1 V to 1.69 V; 1 V to 3.7 V; (d) -0.23 mC; 4.34, $R_o = 5 \text{ kΩ}$;
 $R_o = 5 \text{ kΩ}$; 4.25 (a) 9.73 kΩ; (b) 20 μm; 4 kΩ; ± 16 , 4.8 μL 30.2 kΩ; 4.27, 8 pμ; 2 μm; 12.5 kΩ; 4.39, 0.4 mA;
7.6 V; 4.44 (a) 2.51 V; -2.79 V; (b) 7.56 V; 5 V; 2.24 V; 1.16 (m) 4.5 pA; 1.5 V; (n) 1.8 pA; 1.4 V; (o) 1.5 V;
7.5 pA; 4.48 (a) 1 V; 1 V; 1.52 V; (b) 0.2 V; 1.8 V; 1.35 V; 4.51, 0.8 V; 2.5; 4.51, 4.4 V; 110 pA to 838 pA;
8.2 kΩ; 40 pA to 0.15 mA; 4.53, 1 mA; 3.8%; 1.89, 1.29 V; 2.37 V; 2.77 pA; 4.60, $R_o = 11 \text{ kΩ}$; $R_o = 7 \text{ kΩ}$
4.63 (a) -2 V; +5 V; 8 V; (b) 3.3 V; 1.5 V; 6.3 V; 4.63, 30 kΩ; 0.121 mA; 7 V; 4.69 (a) 2 mA; 2.8 V;
(b) 2 mA/V; (c) -7.2 V/V; (d) 50 kΩ; -6.7 V/V; 4.73, 20 pμ; 1.7 V; 4.75, 3.9 V/V; 2.5 V; -10.8 V/V
4.76 NMOS: 0.42 mA/V, 160 kΩ, 0.08 mA/V, 0.5 V; PMOS: 0.245 mA/V, 240 kΩ, 0.06 mA/V, 0.8 V
1.79, -11.2 V/V; 4.81, 200 Ω; 3.57 V/V; 100 Ω; 4.76 V/V, 200 Ω; 0.83 V/V; 4.81, 5.1 GHz

4.93 2.7 GHz; 3.1 GHz; 4.96 (0) -15.24 mV/V; 32.1 kHz; -2.93 -10 V/V; 18.6 μ A; -4.100 -16 V/V; $C_{11} = 20 \text{ nF}$; $C_1 = 10 \mu\text{F}$; $C_{12} = 0.5 \mu\text{F}$; 47.7 Hz; 4.106 1.36 V; 1.5 V; 1.54 V; 4.110 1.0 μ m; -4.114 (b) -2.25 V/V; 40.142 4.115 0.50 mA; 5 mA; 4 μ A; 9 μ A; 4.116 320 μ A; 116 μ A; 424 μ A; 190 μ A; 600 μ A; 832 μ A; 343 μ A; 360 μ A; 300 μ A; 416 μ A; 137 μ A; 486 μ A; 4.118 40.586 V

CHAPTER 5

CHAPTER 6

C_{ext} (the second error significance) increases by a factor of 7. A_4 remains unchanged: (a) 1.121 (9.3 MΩ; 14.8 mA; 1 V/V; 0.985 V/V) 6.128 (80 μA; 8 MΩ; 0.9 V) $A = 32.141 - (j + 1)\varphi^2$; (b) 5.132 (5.5 kΩ; 5.135 mA; 1 V) 6.137 (2 μA; 0.2%); (c) 6.141 (in 5.76 kΩ; (d) 5.33 MΩ; 0.15 μA) 6.142 (1 MΩ) 6.144 (in 58.5 kΩ; (e) 200 nA)

CHAPTER 7

7.3 1.19 V; 1.03 mA/V; 0.27 V; $\times 50$ μ A 7.3 -3.5 V; +0.5 V, equal in both cases; 0.05 V, -0.05 V; 0.536 V
 7.19 -2.68 V; 5.52 V; 5.32 V 7.20 -2.083 V; -0.515 V 7.22 -0.1 V 7.24 (at) V_{DD} 0.2 V R_{DS}
 7.25 -0.1/2 R_{DS} +1/2 R_{DS} ; (at) 4 V; (at) 0.4 mA; (at) 0.012 7.27 (at) 200 R_{DS} V/V; (at) V_{DD} = 0.0235A;
 7.28 2.7 mA; 0.5 mA; 10.1 mV 7.29 I_{DS} = 3.6 mA; I_{DS} = 2.4 mA; 10.1 mV 7.30 (at) 4.14 V; (at) 3.15 V;
 (at) 3.525 V; (at) 3.755 V 7.32 1 mA; 10 k Ω 7.34 (at) 0.4 mA; 10 mV; (at) 1.40 mA; 0.60 mA; (at) 2.0 V;
 -2.0 V; (at) 40 V/V 7.37 40 V/V; 50 k Ω 7.38 30 V/V; -25 k Ω 7.41 26.7 V/V; 17.8 k Ω ; 0.003 V/V; 15 k Ω
 7.42 (at) 100 V/V; (at) 200 V/V; (at) 10.1 mA; (at) 0.1 V/V; (at) 0 7.44 1.6 mA; 0.6 V/V; 1.8 μ A; 0.6 V
 7.45 R_{DS} = 25 Ω ; R_{DS} = 10 k Ω ; $R_{DS} \geq 30$ k Ω ; $R_{DS} = 5$ M Ω ; ±12 V would do; ±15 V would be better 7.46 22% mismatch, for example ±13 resistors 7.47 0.002 V/V 7.54 -125 μ V 7.55 $V_{DD} = V_T((Y_{DD}/V_{DD}) - (V_{DD}/V_{DD}))$
 7.57 (at) 0.25; (at) 0.225 7.60 1/2; 3/2; $R_{DS}I/2$; 16.7 nA; 17.3 mV; 0.495 μ A; 0.5 μ A; 0.53 mA
 7.66 R_{DS} ; reduce to 7.37 k Ω ; 41.04 V/V; reduce R_{DS} to 1.12 k Ω 7.69 R_{DS} 7.37 k Ω ; 41.04 V/V; R_D = 1.11 k Ω
 7.103 123.1 $\times 10^3$ V/V 7.101 (at) 4 mA; (at) 3.27 $\times 10^3$ Ω ; 125 Ω ; 2.3 $\times 10^3$ V/V

CHAPTER

8.1×10^{-2} ; 80.9% ; -9% ; 8.2 (b); 11.0 ; 121 ; 20.40 ; 6.0 ; 10 V; 9 mA; 1 mV; $\beta = 2.715$.
 8.12 $A_{xy} = A_{xy}(1 + A_{xy}0)$; $W_{xy} = W_{xy}(1 + A_{xy}0)$; $1 - A_{xy}0 = 8.14 - 100$ kQ; $10.14 = 8.20$ 0.04; $12.74 = 10.1$
 $9.30 \times 10^2 = 10.04(1 - g/100) \cdot 10^{14} - 1.17 \cdot 10^2/100 + 100$ kQ; 14.1 ; $k\Omega$; 10 Ω ; 700.12 ; 3.30 (a); $b_{11} = R_1R_2(R_3 + R_4)/\Omega$
 $b_{12} = R_2(R_1 + R_2)/\Omega$; V/V ; $b_{21} = -R_3R_4(R_1 + R_2)/\Omega$; A/A ; $b_{22} = -b_{12}/b_{11}$; $R_1 = 10$ Ω ; $b_{13} = -0.01$ V/V; $b_{23} = -0.01$ A/V; $b_{31} = 0.049 \times 10^{-1}$ g; 8.31 ; 10 V/V; 9.9 SE; 8.51 ; 0.0 V; 0.7 V; 51.3 V/V; 6.1 V/V; 7.6 V/V; ≈ 163 O
 8.35 ; $\beta V_1 = -1 - (R_1/R_2)$; (a) 1.3 kQ; (b) 1.75 kQ; 628.1 kQ; (c) 23.8 V/V; (d) 1.54 kQ; 0.93 kQ
 8.37 ; 7.52 mA/V; 110.8 kQ; $+51.4$ kQ; $8.41 = -1.7$ V/V; 75 kQ; 8.17 ; 60 μ Hg-edges; 0Ω series-
 resistor; (a) β linear-absent; $8.48 = -5.66$ V/V; $1/2$ kQ; 5.62 kQ; 143.5 kQ; -3.61 V/V; 5.98 kQ; $8.48 = -8.83$ kQ;
 29.71 k; -7.5 A/A; 8.50 ; 9.09 A/A; 90.9 Q; 1.0 ; <1 ; 8.50 ; 5.13 ; 167 Q; 8.61 ; 10^4 rad/s; $\beta = 0.01$ kQ; 500 V/V
 8.63 ; $K < 0.008$; 3.65 ; 9.9 V/V; 1.01 kQ; 10 M Ω ; 101 ; 8.66 ; 6.3 ; 5.5×10^4 Hz; $\beta = 2.025 \times 10^{-1}$; (a) 320.6 V/V; (b) 165.3 V/V; (c) 2.72 ; (d) 1.23 ; 8.58 ; $b_{11} = 1/CQ$; $Q = 1/2.1 \cdot K$; 0.1 ; 0.080 ; $K = 2.1$; 8.59 ; $K > 2$;
 17.3 MHz; 8.30 ; 1 MHz; 9.97 ; 8.72 ; 56.87% ; 54.47% ; 59.24% ; 52.02% ; 8.71 ; 139.2 p.s.; 39.3 ; 20.60 ; 8.70 ; 200 Hz
 8.91 ; 10^2 Hz; 2000 ; 8.78 ; 12 dB/C; $/RC$; $1/100RC$; 2 ; $/RC$; 8.29 ; 16 Hz; 15.9 dB; 8.81 ; 58.3 dB; 28.8 mHz

CHAPTER 9

9.21 36.3 μ A 9.22 0.625 V; for A, 7.2 mA/V², 124.5 k Ω , n=5.142, 274 kHz; for B, 21.9 mA/V, 11.7 Ω , 2.25 kHz.
 9.23 k Ω 9.27 616 mV, 553 mA/V, 162 k Ω 9.29 4.75 μ A; 1.34 k Ω 9.31 56.5 k Ω ; 9.33 μ A 9.34 226 nA/k Ω ,
 150, 9.36 6.57 k Ω ; 270 μ A 9.38 1.68 mA/V, 90.4 mW 9.40 Baseline R₁', R₂' to 4.68 ω O 9.43 1.04 nV
 9.45 25.9 dB 9.48 4.10 M Ω ; 9.38 mA/V 9.50 4.7 V to -3.6 V 9.52 21 mA 9.54 10k dB; 61.9 Ω ; 717.5 dB;
 V_o<4 V 9.56 11.4 MHz 9.58 617 k Ω 9.60 150 kHz; 15.9 MHz 9.62 six bits, 0.155 V; seven bits; seven
 bits: 0.117 V; 0.039 V 9.65 1/16; 7/8; 5/4, 1/2 9.67 Use up ramp with R/2 input; and SQR feedback to drive
 V_o; 15 sine wave amplitudes from 0.625 V peak to 9.375 V peak; an output of 10 V (peak-to-peak) corresponds
 to a digital input of 10001. 9.69 6.15 ms, 4.196 ms; 8.9 V/ms were the sum!

CHAPTER 10

10.1 (5 V); 1.5 V; 1.5 V; 1.0 V; 3 V; 1.5 V; 1.5 V; $\alpha = 10.1$; 0.35 to 0.45 V; 0.75 to 0.82 V; 0 V; 1.2 V; 0.45 to 0.75 V; 0.35 to 0.15 V – 10.1 (8) $\beta_{\text{app}} = 1.6$ vs. $\beta_{\text{app}} = 0.8$ ms⁻¹ (5); $C_1 = 1.48 \mu\text{F}$; $\delta C_1 = 0.04 \mu\text{F}$; $C_2 = 0.53 \mu\text{F}$

(b) 0.436; -0.48 mW. (c) Maximum operating frequency is reduced by a factor of (a) 0.08, (b) 0.44. (d) Decrease by a factor of 0.14 in both cases. (e) 0.9. (f) 1% of changes in device dimensions is to change the performance parameters by the factors: 0.81, 1.11, 0.86, 0.77, 1.40, 1.11, 0.86, 1.09, 10.14, 9.1, 10V; 50 mV. (g) 10.19, 10.61, 1F; 68.5 ps; 10.26, 24, 10.32; $\rho_1 = \rho_2$; $\eta_1 = \eta_2 = 2\pi$; $\eta_3 = \eta_4 = 2\pi$; $\eta_5 = \eta_6 = 2(2\pi) = 4\pi$. (h) While the proportionality η_{ext} is one-quarter the value required with the small-signal model (8.8%), η_{ext} is the same in both cases. (i) 0.38; (j) 0.99; (k) 0.5C₂; (l) 0.5C₁, for a 21.5% reduction. (m) 10.39, 1.152, 1.70 V; 3.25 V; 3.70 V; 5.0 V; 0.58 V; 1.75 V; 10.10, 2.1 F; 10.5 F; 63.5 ps; 21.2 ps; 52.4 ps; 9.6, 11, 24.0 F; 72.5 ps; 72.5 ps; 72.5 ps; 10.41; $\tau = 2$; $M_{\text{eff},\text{ext}} = 1.28$; V = 0.13, 1.51; 0.92 V; 10.53; (n) 1.52 V; 1.15 V; 0.53 μA ; 351.0 μA ; 1.51 μV ; 177 ps; 10.60; 0.67 V; 1.25 V; 10.52, 1.1 GHz.

CHAPTER 11

11.1 2.16 V; 0.9%; 1.86; 11.3, 6; 11.11, 0.4 μs ; 0.8 V; 5.7 V; $= 0.1$ V; 21.5 μA ; The source current can be as large as 21.12 A (5% $R_{\text{in}} = 200$ k Ω), but is clearly limited by k_T of G₁ to a much smaller value: 11.13 ($\omega_0 = 29\text{CR}$, by 10 k Ω , 72.1 μF , 11.14, 97.28, 11.15, 1.6 μs , 11.19, 1024, 1024, 4000 pF, 225 pF, 2200 pF); 2.8 μA ; 1.20, 0.3 μA^2 , 0.39 $\mu\text{A} \times 0.78 \mu\text{A}$; 11.21, 60.8, 11.22, 4; 11.23, 11.2, 52.1 MHz; 11.23, 2 pA; 11.30, 1.583 mA/V; 1.32, 0.003 A; 1.33, 1.56 μs ; 11.31, 0.638 mA/V, 0.48 V, 0.21 V; 50%; 7.5 ns; 11.32 (g) 2; (h) 1.46; 11.34, 9; 5.2, 18; 1008 NMOS and 912 PMOS transistors; 11.35, 9, 1024; 11.36, 512, 564, 1.52; 11.36, 263.144; (i) 11.37, 11.38, 1.4/2 ps; 22 ps; 3.8 V; 1.9 μs ; 1.41, 35.3 MHz; high for 19 ps, low for 17 ps; 11.38, 0.329 V/V; 8.94 V/V; 11.39 (a) -1.575 V, -1.265 V; (b) -1.493 V, -1.147 V; 11.41, 21.2; 11.42, 11.51; (h) 7.1, $= 5$ μmA ; 11.52, 6.5 mA; 11.53, 2.32 V; 3.83 μA ; 11.53, 10.2; $\tan \theta_1 = 50\%$; 26.5 k Ω ; 20%; 11.54, 8.22 ps; 50.7 ps; 57.0 ps; 1.56; $(W/L)_{Q_{\text{ext}}} = 19\%$; $(W/L)_{Q_{\text{int}}} = (W/L)_{Q_{\text{ext}}} + (W/L)_{Q_{\text{ext}}}$.

CHAPTER 12

12.1 1 V/V, 0, 0, -40, 0, -43
0.894 V/V, -26.6%, 0.97 dB, 0.97 dB
0.707 V/V, -35.2%, -5.01 dB, 3.01 dB
0.447 V/V, -63.4%, -0.99 dB, 0.99 dB
0.106 V/V, -78.7%, -11.1 dB, 11.1 dB
0.106 V/V, -84.7%, -20.0 dB, 20.0 dB
0.016 V/V, -89.4%, -40.0 dB, 0.0 dB
12.3 ± 0.002 ; ± 0.04 ; 0.010, 12.5, 0.519 ± 0.02 ; 2, ± 0.05 ; 5.00
12.4 $T(\omega) = 10^{10} / [(\omega - 10^4 \omega^2 - 618\omega - 10^6)(\omega^2 - 1618\omega - 10^6)]$, low-pass;
 $T(0) = \omega^2 / (\omega^2 - 10^4 \omega^2 - 6.18\omega - 10^6)$; mid-pass; 12.9 $T(\omega) = 0.2225 \omega^2 / [\omega^2(\omega^2 - 1618\omega - 10^6)]$
12.1 $T(\omega) = 0.5 / (\omega^2 - 1618\omega - 10^6)$; poles at $\omega = 1.1 \sqrt{1618} / 2$, 0.1618 rad/s; $\omega = \pm 12.15, 28.6$ rad/s
12.15 $N = 5$; $f_0 = 10.55$ kHz; $\alpha = -108^\circ, -144^\circ, -180^\circ, -216^\circ, -252^\circ$; $\rho_1 = -20.184 \times 10^3 + j 62.043 \times 10^3$ (rad/s);
 $\rho_2 = -53.628 \times 10^3 - j 83.957 \times 10^3$ (rad/s); $\rho_3 = -66.388 \times 10^3$ rad/s; $\rho_4 = -83.628 \times 10^3 - j 98.963 \times 10^3$ (rad/s);
 $\rho_5 = -20.484 \times 10^3 - j 63.043 \times 10^3$ (rad/s); $T(\omega) = \omega^2 / (\omega^2 - 1614\omega^2 + 10^6) + 0.618\omega / (\omega^2 + 10^6)$
12.16 $R = 10^3$ k Ω ; $R_2 = 100$ k Ω ; $C = 10$ pF; 12.21, $K_1 = 1$ k Ω ; $R_3 = 1$ k Ω ; $C_1 = 0.156 \mu\text{F}$; $C_2 = 1.59 \mu\text{F}$
High-frequency gain: ± 120 V/V; 12.23, $T(\omega) = (1 - RC\omega)/(1 - RC\omega^2)$; 2.68 k Ω , 5.77 k Ω , 10 k Ω ; 17.3 k Ω
27.3 $\times 10^{-3}$; 12.25, $T(\omega) = 10^6 / (\omega^2 + 10^6 \omega + 10^6)$ rad/s; 10 V/V; 12.27, $R = 4.50$ k Ω ; $R = 10.181$
12.28 $T(\omega) = \omega^2 / (\omega^2 + \omega^2 + 1)$; 12.30, $T(\omega) = (\omega^2 + 1.42 \times 10^3) / (\omega^2 + 475.5 + 1.42 \times 10^3)$; 12.33, $\lambda = -0.5$ dB; $\epsilon = 20$ dB
12.35 $V_{\text{out}} / V_{\text{in}} = \omega^2 / (\omega^2 + \omega^2 + 1 / LC)$; 12.37, $S = 0$ into two carts, leaving 2R in its place and adding 2R
from the output to ground; 12.39, $L = L_1 + L_2 - 0.293$; $|T| = 1 - 1.2 / \omega$; For all resistors = 10 k Ω
 C_1 is (a) 0.1 μF ; (b) 0.01 μF ; (c) 1000 μF ; For $R_1 = 100$ k Ω and $R_2 = R_3 = 10$ k Ω , 0.01 μF
(d) 1000 pF, (e) 100 pF; 12.45, $R_1 = R_2 = R_3 = 30.79$ k Ω ; $C_0 = 0.2$ dB; $C_M = 1.6$ nF

12.44 $C_1 = C_2 = 1$ nF; $R_1 = R_2 = R_3 = R_4 = R_5 = 1.59$ k Ω ; 12.48, $|T(\omega)| = 4.51 \times 10^{-3} \omega^2 + 1.70 \times 10^3 / [\omega^2 + 0.729 \times 10^4 \omega + 1.05 \times 10^6]$; (a) For LP section: $C = 10$ pF; $R_1 = R_2 = 9.76$ k Ω ; $R_3 = 3.9$ k Ω ; $C_M = 3.82$ nF
12.49, $C = 10$ nF; $R_1 = R_2 = 10$ k Ω ; $R_3 = 10$ k Ω ; $R_4 = 30$ k Ω ; 39 V/V; 12.51, $-1\omega_c$; 12.53, (a) For only ω_0 change C_1 and ϵ ; or R_1 , or change R_2 and ϵ ; R_3 and R_4 preferred; (b) For only ω_0 , change only ϵ , or only R_1 ; 12.55, $R_1 = 1 + 1/k\omega$; $R_2 = 10.7$ k Ω ; $12.57, T(\omega) = -(1/\omega_0^2 RC) / [\omega^2 + 2\omega_0^2 RC + 10^6 / R^2 C^2]$; $V_{\text{out}} = 0.2 / \omega_0^2 RC$; $Q = 2$; Center-frequency gain = 8 V/V; 12.59, $T(\omega) = \omega^2 / [\omega_0^2 + (C_1 + C_2)\omega / (R_1 C_1 C_2) + 1 / R_2 C_1 C_2]$; High-pass; High-frequency gain = 1 V/V; $R_2 = 141.4$ k Ω ; $R = 30.7$ k Ω ; 12.60, For first-order section: $C = 5.18$ pF; For one S and K section, the grounded and floating capacitors are, respectively, $C_1 = 0.8$ pF and $C_2 = 10.5$ pF; For the other S and K section, corresponding capacitors are $C_1 = 2.57$ pF and $C_2 = 7.97$ pF, respectively.
12.62 Sensitivities of ω_0 is 8, J_1 , C_M is 0, ω_2 is 1, $\frac{1}{2}$, $\frac{1}{2}$ respectively.

CHAPTER 13

13.1 (a) $\omega_0 = \omega_p / \sqrt{K - 1}$; (b) ω_p /down $\omega = \omega_0 / \omega_p$; (c) $A(\omega_0) / A_0 = -\omega_0^2 / 2Q^2 + 1$; (d) To for increasing input, connect LC to ground and R to output, $A = 1 + R_1 / R_2 \geq 1.0$; Use $R_1 = 10$ k Ω ; $R_2 = 100$ Ω (say); $\omega_0 = 1 / \sqrt{LC}$
13.3, $\pm 5\%$; (b) $\pm 1\%$; (c) 0%; 13.5 Minimum gain is 20 dB; phase shift is 180°; 13.6, Use $R_1 = R_2 = 10$ k Ω ; $R_3 = R_4 = 5$ k Ω ; $R_5 = 50$ k Ω ; 13.9, $V_{\text{out}} / V_{\text{in}} = 1 / \omega_0^2 C^2 / [\omega^2 + 3\omega_0^2 RC + 1 / R^2 C^2]$; ω_0 in magnitude zero at $\omega = 0$; $\omega = \omega_0 = 1 / \sqrt{RC}$; $Q = \frac{1}{2}$; Gain at $\omega_0 = \pm \omega$; 13.10, $\omega_0 = 1 / \sqrt{RC}$; 13.12, $R_3 = R_4 = 6.5$ k Ω ; $\omega_0 = 2.08$ V/ μsec -peak
13.13, $L(j\omega) = (1 + R_2 / R_1)^2 / (R^2 C^2 + \omega^2 R^2 C^2)$; $L(j\omega) = (1 + R_2 / R_1)^2 / (3 + 1 / \omega_0^2 RC + \omega^2 RC)$; $\omega = 1 / \sqrt{RC}$; for oscillation, $R_2 / R_1 = 2$; 13.15, 20.3 V; 13.16, $A(\omega) = -(R_1 / R_2) / [1 + 6 / R C + 5 / R^2 C^2 \omega^2 + 1 / R^2 C^2 \omega^2]$; $R_2 = 29.8$, $j_0 = 0.0565 / RC$; 13.21, For circuit (a), (b), characteristic eqn. is: $C_1 C_2 L / R_1^2 + (C_2 C_1 L / R_1 R_2)^2 + (C_1 C_2 L / R_2 + g_s) - 0$; $g_s = [(C_1 + C_2) / C_1 C_2] / R_1^2$; $g_s R_1 = C_2 / C_1$; For circuit (b), $LC / C_2^2 + (C_1 L / R_1)^2$; $(C_1 + C_2) L / R_1 + g_s = 0$; $g_s = [C_1 C_2 - C_2 C_1 L / R_1^2] / g_s R_1 = C_1 / C_2$; 13.23, From 2.01612 MHz, $\omega = 2.01612$ MHz; 13.24, 724 MHz; 13.25 (a) $R_{\text{in}} = R_2 (1 + R_1 / R_2) - j_0 R_1 / R_2$; $V_{\text{in}} = U_{\text{in}} - V_{\text{out}}$; (b) $R_1 = 200$ k Ω , $V_{\text{in}} = 0.0476$ V; 13.28 (a) Either -12 V or +2 V; (b) Symmetrical square wave of frequency ω and amplitude 1.2 V, and 1/2 the input by 65.1%. Maximum shift of average is 0.1 V; 13.29, $V_2 = 6.8$ V; $R_1 = R_2 = 17.5$ k Ω ; $R = 4.1$ k Ω
13.31, $F_2 = 5.6$ V; $R_1 = 6.67$ k Ω ; $R = 50$ k Ω ; $R_2 = 27$ k Ω ; 13.33, $V_2 = 6.8$ V; $R_1 = R_2 = R = R_3 = R_4 = 100$ k Ω ; $R_5 = 5.0$ k Ω ; On μm^{-2} , symmetrical triangle with half period of 50 ns and ± 7.5 V peaks.
13.35, 9%; 13.36, $R_1 = R_2 = 100$ k Ω ; $R_3 = 154.1$ k Ω ; $R_4 = 120$ k Ω ; 6.5 V; 61.4 ps; 13.38 (a) 9.1 k Ω ; (b) 13.5 V; 13.39, $R_4 = 21.3$ k Ω ; $R_5 = 10.7$ k Ω ; 13.41, $V = 1.0996$ V; $R = 40$ k Ω ; Table notes, for $\omega_0 = 9.07$ rad/s, unity ω_0 :
0.70 V, 10%; 0.700 V, 0%; 0.69 V, 55.0%; 0.697 V, 0.627 V, 0.7%; 0.69 V, 52.4%; 0.69 V, 0.2%; 0.65 V, 10.1%; 0.65 V, 0.1%; 0.55 V, 11.3%; 0.462 V, 4.3%; 0.40 V, 42.8%; 0.170 V, 5.6%; 0.31 V, 24.6%; 0.29 V, 5.1%; 0.20 V, 16.4%; 0.197 V, 1.5%; 0.10 V, 8.2%; 0.100 V, 0%; 0.00 V, 0%; 0.00 V, 0%; 0.00 V, 0%; 13.42, ± 2.2 V; 13.43, Table notes: circuit ω_0 / V_{in} , circuit $\omega_0 / V_{\text{out}}$, ideal ω_0 / V_{in} , and error as $\pm \%$ of ideal are:
0.250, 0.451, 0.25%, $\pm 3.6\%$
0.500, 0.905, 0.517, $\pm 3.4\%$
1.001, 1.442, 1.030, $\pm 2.9\%$
1.500, 2.086, 1.537, $\pm 2.5\%$
2.000, 2.497, 2.065, $\pm 1.7\%$
2.400, 2.892, 2.412, $\pm 0.6\%$
2.420, 3.539, 2.420, $\pm 0.0\%$

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