# How to Implement a Digital System Using Verilog?

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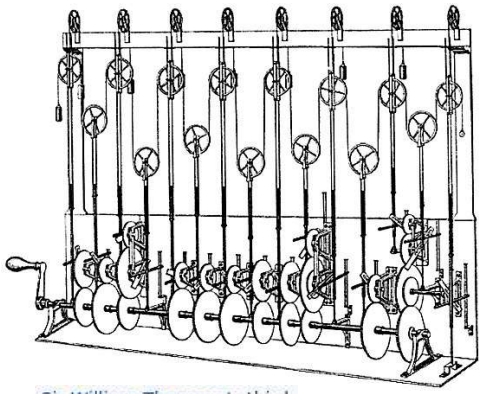
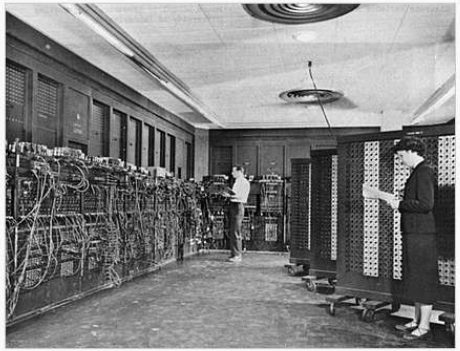
# Digital Systems

- Digital systems originated from computers, first computers were like Abacus, then more complicated mechanical computers came to be. However, nowadays computers use transistors.



Sir William Thomson's third tide-predicting machine design, 1879–81

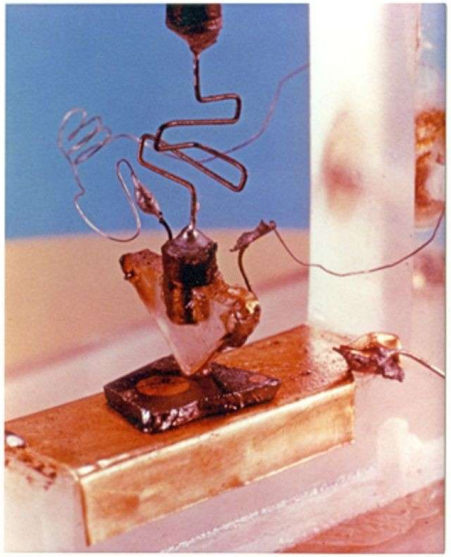


ENIAC was the first electronic, Turing-complete device, and performed ballistics trajectory calculations for the United States Army. 1945

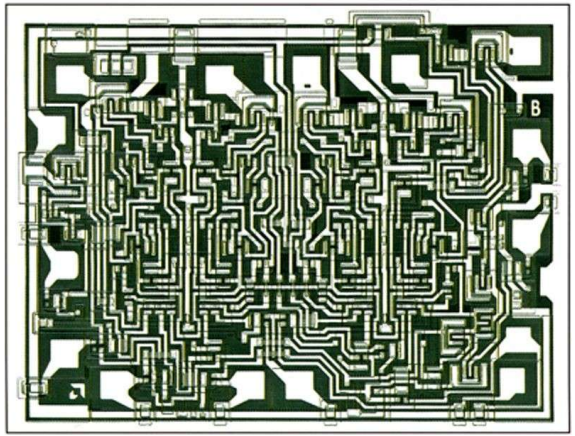
Modern Computers

# Transistors

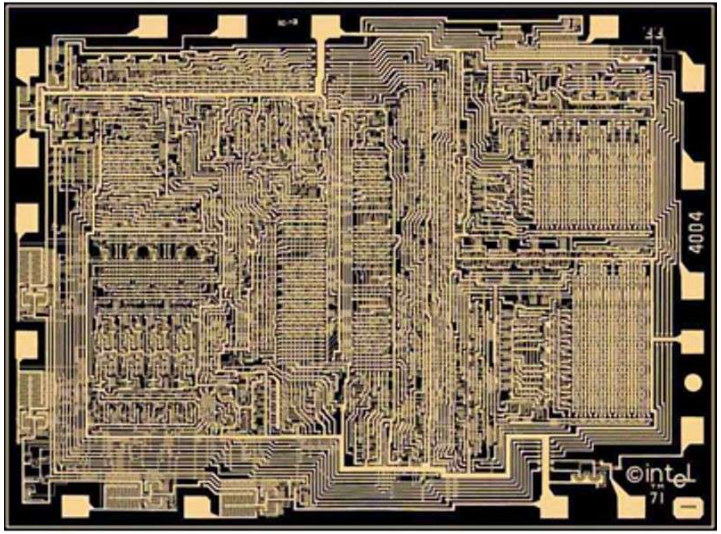
- With the invention of transistors, implementing computers had never been easier.



1947: Invention of the Point-Contact Transistor (John Bardeen & Walter Brattain)



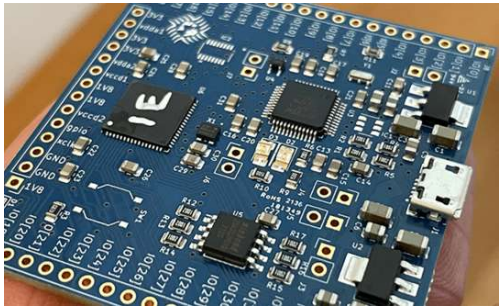
AMD Am9300 TTL MSI universal shift register. 1963

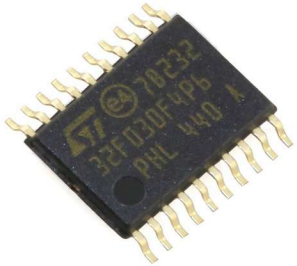



Intel 4004 4-bit Microprocessor 1971

# How can we implement digital systems?

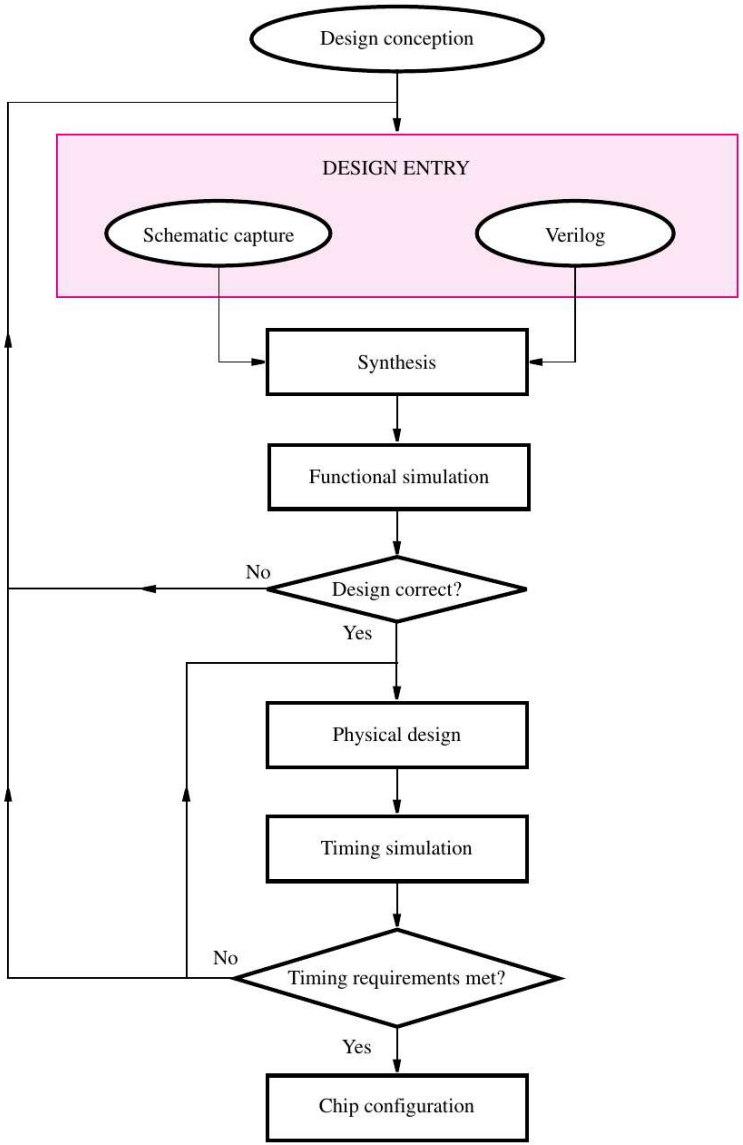
- ASIC (Application-specific integrated circuit): Peripheral controllers
- ASSP (Application-specific standard parts): CPU GPU
- FPGA (Field-programmable gate arrays): Low yield custom systems
- TTL (Transistor–transistor logic): 7400-series integrated circuits





| | |
|---|---|
| Series: | STM32F030F4 |
| Mounting Style: | SMD/SMT |
| Package/Case: | TSSOP-20 |
| Core: | ARM Cortex M0 |
| Program Memory Size: | 16 kB |
| Data Bus Width: | 32 bit |
| ADC Resolution: | 12 bit |
| Maximum Clock Frequency: | 48 MHz |
| Number of I/Os: | 15 I/O |
| Data RAM Size: | 4 kB |
| Operating Supply Voltage: | 2.4 V to 3.6 V |


# How to design complex systems using CAD tools



# HDL (Hardware description language)

- Design, Simulation, Verification
- Gate Level, Data flow (Register Transfer Level (RTL)), Behavioral Descriptions
- VHDL, Verilog, SystemVerilog

```
always_comb begin
    tmp = b * b - 4 * a * c;
    no_root = (tmp < 0);
end
```

```
reg q;
always @(posedge clk or posedge reset)
  if(reset)
    q <= 0;
  else
    q <= d;
```

```
entity COUNTER is
  generic (
    WIDTH : in natural := 32);
  port (
    RST   : in std_logic;
    CLK   : in std_logic;
    LOAD  : in std_logic;
    DATA  : in std_logic_vector(WIDTH-1 downto 0);
    Q     : out std_logic_vector(WIDTH-1 downto 0));
end entity COUNTER;
```