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Multilevel Inverter Topologies with Reduced Device Count: A Review

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***Abstract*— Multilevel inverters have created a new wave of interest in industry and research. While the classical topologies have proved to be a viable alternative in a wide range of high-power medium-voltage applications, there has been an active interest in the evolution of newer topologies. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced topologies. In this paper, some of the recently proposed multilevel inverter topologies with reduced power switch count are reviewed and analysed. The paper will serve as an introduction and an update to these topologies, both in terms of the qualitative and quantitative parameters. Also, it takes into account the challenges which arise when an attempt is made to reduce the device count. Based on a detailed comparison of these topologies as presented in this paper, appropriate multilevel solution can be arrived at for a given application.**

***Index Terms*— Multilevel inverters, reduced device count, even power distribution, fundamental switching frequency operation, source configuration.**

I. Introduction

DC to AC power conversion is a key technology in the modern set-up of generation, transmission, distribution and utilization of electric power. DC to AC power converters (‘inverters’) play a crucial role in variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, static var compensators, active filters, flexible AC transmission systems and DC power source utilization (such as electricity obtained from batteries, solar panels or fuel cells) [1,2]. With the advent of recent power electronics devices, digital controllers and sensors, the role of power inverters is also envisaged and acknowledged in frontiers such as futuristic smart grids and greater penetration of renewable energy sources based power generation [3].

Based on the nature of the output waveform, inverters can be classified as: square wave inverters, quasi-square wave inverters, two-level PWM inverters and multilevel inverters [4]. These waveforms are illustrated in Fig.1. The multilevel inverter (MLI) structure has been introduced as an alternative in high power and medium voltage situations. The elementary concept of an MLI to achieve higher power is to use power semiconductor switches along with several lower voltage DC levels to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple input DC levels. Power switches are controlled so as to aggregate these multiple input DC levels to achieve high voltage at the output, while the rated voltage of the power semiconductor switches depends on the rating of the DC voltage sources to which they are connected. Thus, in general, the voltage stress on a power switch is much lower than the operating voltage.

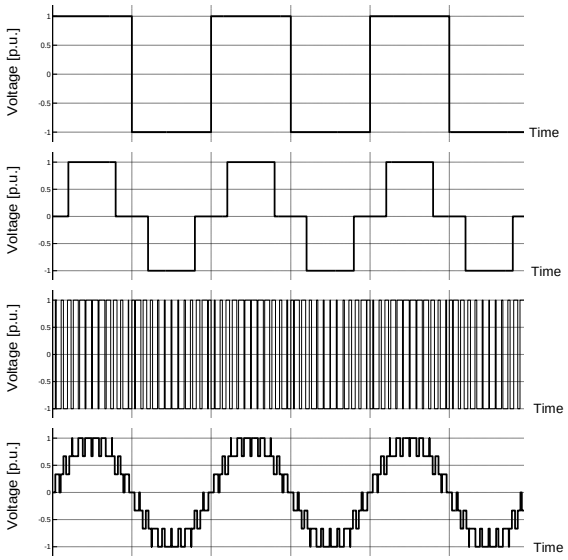

Fig.1.Typical inverter waveforms: (a) Square wave; (b) Quasi-square wave; (c) Two-level PWM waveform; and (d) Multilevel PWM waveform

A. Multilevel DC to AC Conversion and Classical Topologies

The multilevel approach for DC to AC conversion offers many advantages such as [5-10]:

i. The staircase waveform not only exhibits a better harmonic profile but also reduces the d*v*/d*t* stresses. Thus, the filter

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requirements can be greatly brought down (or even eliminated), while electromagnetic compatibility problems can be reduced.

ii. The voltage stresses on the semiconductor devices are much lesser as compared to the overall operating voltage. Thus, a high voltage waveform can be obtained with comparatively low voltage rated switches.

iii. MLIs produce much smaller common mode voltage and thus the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

iv. Many multilevel topologies offer the possibility to obtain a given voltage level with multiple switching combinations. These redundant states can be utilized to program a fault tolerant operation.

v. MLIs can draw input current with low distortion.

vi. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system and can be controlled for equal load sharing amongst the input sources.

Over the past few decades, MLIs have attracted wide interest both in the research community and in the industry, as they are becoming a viable technology for many applications. In the mid-1970s, the first patent describing a converter topology capable of producing multilevel voltage from various DC voltage sources was published by Baker and Bannister [11]. The topology consists of single-phase inverters connected in series as depicted in Fig.2 and it is known as series-connected H-bridge inverter (SCHBI), or cascaded H-bridge (CHB) inverter.

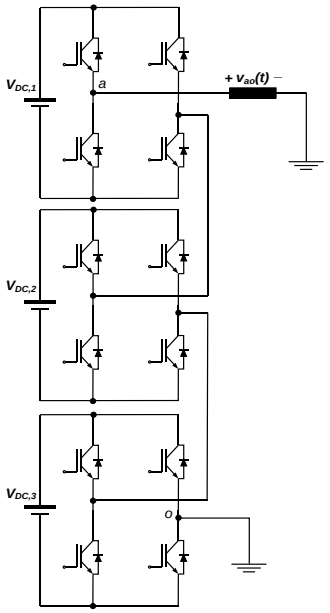

Fig. 2 Cascaded H-bridge structure for multilevel inverters

In another patent by Baker [12] in 1980, a modified multilevel topology was introduced, for which three-level and five-level versions are illustrated in Fig. 3(a) and (b) respectively. In contrast to the CHB inverters, this converter can produce multilevel voltage from a single DC source with extra diodes connected to the neutral point. This topology is now widely referred to as the neutral point clamped (NPC) inverter and/or diode clamped topology. In 1980, Nabae *et al.* [13] demonstrated the implementation of NPC inverter using a pulse width modulation scheme. In the 1980s much of the research was focused only on three-level inverters. The so-called flying capacitor (FC) was introduced in the 1990s by Meynard and Foch [14] and Lavieville *et al*. [15]. The topology of the FC inverter is depicted in Fig.4(a) for three-level and in Fig.4(b) for five-level applications. Much of the literature published in past few decades have shown intense focus in studying the diode clamped, flying capacitors and cascaded H-bridge topologies with regards to their respective pros and cons [5,16-34] and these topologies are now widely referred to as the 'classical topologies'.

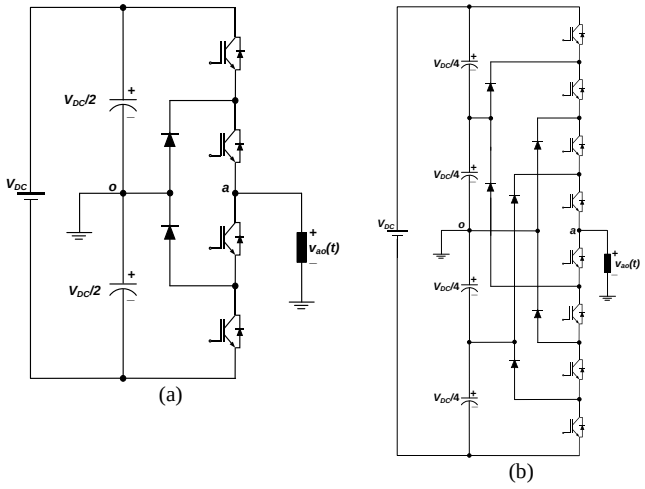

Fig.3. One leg of Neutral-point / Diode-clamped structure; (a) three-level; and (b) five-level

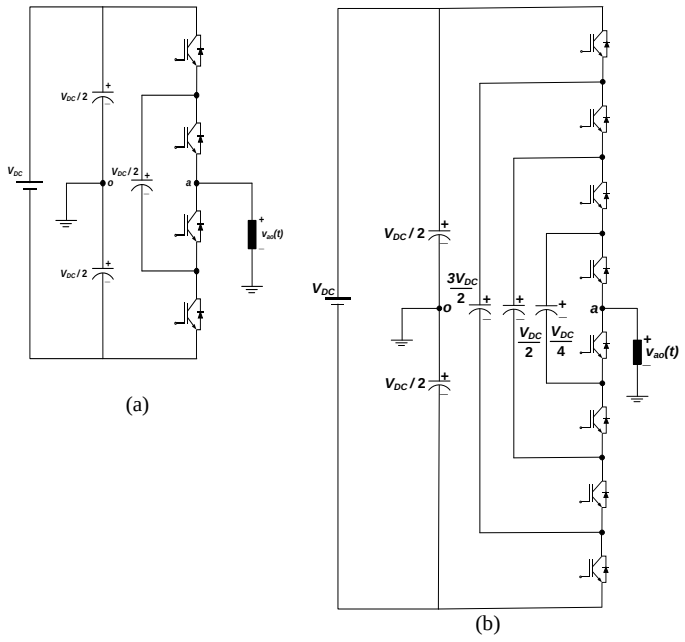

Fig.4. One leg of flying structure; (a) three-level; and (b) five-level capacitor

B. Advent of New Topologies with Application Oriented Approach

The so-called 'classical topologies' have attracted maximum attention both from the academia and industry. Still,

no specific topology seems to be absolutely advantageous as multilevel solutions are heavily influenced by application and cost considerations. Because of its intrinsic characteristics, a given topology can be very well adapted in some cases and totally unsuitable in some others. Therefore, the optimal solution is often recommended on case-to-case basis. Hence, along with the exploration of classical topologies, researchers continued (and still continue) to evolve newer topologies with an application oriented approach. In this sub-section, some of such contributions are discussed.

Agelidis *et al.* [35] presented a multilevel PWM single-phase voltage-source inverter topology for photovoltaic applications, which utilizes a combination of unidirectional and bidirectional switches of different ratings along with the use of phase-opposition carrier disposition multicarrier PWM switching technique. Manjrekar and Lipo [36] have presented a hybrid inverter based on the cascaded H-bridge topology for a 500 HP, 4.5 kV induction motor drive with investigations on design optimization, capacitor voltage balancing and harmonic profile of the output waveform. In [37], Xioming and Barbi presented a modified diode-clamped structure with a view to solve the problem of series-connected diodes in the conventional diode clamped inverter. In this structure, apart from the clamping of the main switches with clamping diodes, there is mutual clamping amongst the clamping diodes themselves.

Cheng and Crow [38] have proposed to employ an additional circuitry, integrated with the diode clamped inverter for implementing a static compensator with battery energy storage system (STATCOM/BESS) using a diode clamped structure, so as to achieve effective balancing of the DC link capacitors. To reduce the number of DC-DC converters supplying the cells of reversible multilevel converters, a topology is proposed by Mariethoz and Rufer [39] combining in series a 3-phase 6-switch voltage source inverter with single phase H-bridges, resulting in advantages in terms of voltage resolution and energetic efficiency. An innovative topological structure using a three-phase three-level integrated gate-commutated thyristor inverter (main inverter), with a two-level IGBT H-bridge (sub-inverter) in series with each phase has been proposed by Veenstra and Rufer [40] along with asymmetric source configuration to obtain a nine-level waveform for implementation of a medium voltage drives application. To obtain uncompromised multilevel voltage waveform in the event of partial failure(s) in the power circuit, a fault tolerant topology was proposed by Chen *et al.* [41] which maintains the output voltage waveform utilizing control signal modification along with redundancy offered by multi switching states.

For photovoltaic medium and high power range with grid connection of two isolated photovoltaic generators, a topology was proposed by Grandi *et al.* [42] utilizing dual two-level voltage source inverter so as to obtain a multilevel waveform thereby reducing grid current harmonics and mitigating output voltage derivatives. Lezana *et al.* [43] have proposed a modification in the classical cascaded H – bridge topology with an active front end with the objectives of problem-free regenerative mode of operation for loads (such as laminators and downhill conveyors) demanding regeneration capability on the converter and effective control of the input current and output voltage waveforms. A solution for standalone applications requiring few kilowatts of power with single battery storage was presented by Daher *et al.* [44] with a multilevel inverter topology utilizing multi-winding transformer with appropriate turn-ratios and an array of bi-directional power switches.

Du *et al.* [45] have shown implementation of a cascaded multilevel boost inverter for electric vehicle and hybrid electric vehicle applications without the use of inductors and multiple power supplies and utilizing a fundamental switching frequency modulation scheme. Ewanchuk *et al.* [46] have proposed an introduction of coupled reactors in each leg of the NPC topology, for low-voltage high-speed motor applications, offering an increased number of output PWM voltage levels, higher frequency PWM output waveforms, reduced dead-time effects, and a significant reduction in harmonic content. Another important contribution in the evolution of MLI topologies is the introduction of 'modular multilevel converter (MMC)' [10]. MMC has become an attractive topology for medium/high power applications, specifically the Voltage-Source Converter High-Voltage Direct Current (VSC-HVDC) transmission systems. This topology is simpler than CHB inverter and has several advantages such as modularity and redundancy.

Thus, apart from the exclusive and extensive studies into various aspects of the 'classical topologies', researchers continue to contribute towards evolution of newer multilevel structures for different applications. Moreover, due to the advantages offered by MLIs, efforts also being made to impart technological and economical feasibility to MLIs for low power applications [47-49].

C. Topologies with Reduced Device Count and Scope of the Paper

In view of their many advantages, MLIs are receiving much more and wider attention both in terms of topologies and control schemes. Multilevel inverters, however, exhibit an important limitation- for an increased number of output levels, they require a large number of power semiconductor switches, thereby increasing the cost, volume and control complexity. Although low-voltage-rated switches can be utilized in an MLI, each switch requires a related gate driver unit, protection circuit and heat sink. This may cause the overall system to be more expensive, bulky and complex. Consequently, for past few years, efforts are being directed to reduce the power switch count in MLIs and a large number of topologies have appeared in the literature [50-68]. These topologies have their own merits and demerits from the point of view of application requirements. As of now, no literature is available which comprehensively reviews the aforementioned topologies, thereby stipulating their comparative advantages and limitations. This paper aims at presenting a review of MLI topologies proposed with the exclusive objective of reducing the power switch count. Analysis of these topologies has been specifically carried out in terms of: count of power semiconductor components, total voltage blocking capability requirement, possibility of even power distribution amongst the input DC sources, possibility of optimal distribution of switching frequency amongst the power switches and possibility of employing asymmetric sources. In addition, this

paper provides a list of appropriate references in relation to MLI topologies and their control. Although the development of topologies has been accompanied with advancement in modulation schemes [5-7], this paper focuses only on the topological features and their consequences.

Rest of the paper is organized as follows. In Section II, a brief description of terminologies used in this paper is given. Some of recent reduced-switch-count topologies of MLIs are discussed in Section III and comments are made on them based on qualitative and quantitative parameters. A discussion is presented in Section IV. Concluding remarks are made in Section V.

II. Terminology, Assessment Parameters and Classification of Topologies

Prior to a comparative analysis of topologies, some terms pertaining to the assessment criteria are defined. Thereafter, various criteria to assess reduced device count topologies are discussed and a classification of the topologies is presented so that a broad outline can be drawn.

A. Terminology

(a) Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies: Topologies which are proposed / presented with an exclusive claim of reducing the number of controlled switching power semiconductor devices for a given number of phase voltage levels are referred to as RDC-MLI topologies. In this paper nine such topologies [50-68] are reviewed.

(b) Total Voltage Blocking Capability: For a topology, the total sum of the voltage blocking capability requirement for all its power switches is referred to as the 'total voltage blocking capability' [65]. For example, if a structure consists of four switches rated at V_{DC} and six switches rated at $2V_{DC}$, the total voltage blocking capability requirement would be: [(4 X V_{DC}) + (6 X $2V_{DC}$) = $16V_{DC}$].

(c) Symmetric and Asymmetric Source Configuration: When the voltages of the input DC levels to an MLI are all equal, the source configuration is known as 'symmetric', otherwise 'asymmetric' [59]. Two popular asymmetric source configurations are: binary and trinary. In binary configuration, values of voltage levels are in geometric progression (GP) with a factor of '2' (i.e. V_{DC}, $2V_{DC}$, $4V_{DC,}$ $8V_{DC}$...), while in trinary configuration the GP factor is '3' (i.e. V_{DC}, $3V_{DC}$, $9V_{DC,}$ $27V_{DC}$...). There are many other asymmetric source configurations proposed by various researchers [44]. An asymmetric source configuration is employed to synthesize more number of output levels with the same count of power switches.

(d) Even Power Distribution: When the multilevel DC to AC conversion is carried out in such a way that each input source contributes equal power to the load, the 'power distribution' amongst the sources is said to be 'even'. Some authors also refer to it as 'charge balance control' or 'equal load sharing' [49]. 'Even power distribution' is a feature of control aspect, only when the topology permits so. When the source configuration is symmetric, the control algorithm is designed such that the average current drawn from each source is equal, thereby making average powers equal. For a given topology, even power distribution is possible if each input source contributes towards all the output levels in one or more output cycles. For example, if a topology has three symmetric input DC sources $V_{DC,1}$, $V_{DC,2}$ and $V_{DC,3}$ ($V_{DC,1}$ = $V_{DC,2}$ = $V_{DC,3}$ = V_{DC}), then even power distribution is possible if all the combinations shown in Table I are permitted by the topology.

TABLE I
EXAMPLE OF POSSIBILITY OF 'EVEN POWER DISTRIBUTION' WHEN THREE INPUT SOURCES $V_{DC,1} = V_{DC,2} = V_{DC,2} = V_{DC}$ ARE AVAILABLE

Output voltage level	Required combination of input DC levels
$\pm V_{DC}$	$\pm\ V_{DC,1}$
$\pm V_{DC}$	$\pm\ V_{DC,2}$
$\pm V_{DC}$	$\pm\ V_{DC,3}$
$\pm 2V_{DC}$	$\pm\ (V_{DC,1} + V_{DC,2})$
$\pm 2V_{DC}$	$\pm(V_{DC,2} + V_{DC,3})$
$\pm 2V_{DC}$	$\pm(V_{DC,1} + V_{DC,3})$
$\pm 3V_{DC}$	$\pm(V_{DC,1} + V_{DC,2} + V_{DC,3})$

(e) Level-Generation and Polarity-Generation: An MLI synthesizes a stepped waveform consisting of the input DC levels and their additive and/or subtractive combinations. Thus, the voltage waveform consists of multiple 'levels' with both 'positive' and 'negative' polarities (in positive and negative half cycles respectively). Many a times, an MLI circuit is such that a part of it synthesizes the multiple levels with only one polarity and an H-bridge is used to convert this single polarity waveform to a bipolar one for the AC load. These parts are respectively referred to as 'level-generation part' and 'polarity-generation part' [66]. It is important to mention here that the power switches for the polarity generation part need to have a minimum voltage rating equal to the operating voltage of the MLI.

(f) Fundamental Frequency Switching: The switching losses in a converter are proportional to the current, blocking voltage and switching frequency [68]. To minimize the switching losses, it is preferred to operate higher voltage-rated power switches at a low frequency and if possible, at the power frequency (or fundamental frequency), without compromising the quality of output waveform. A power switch in a topology can operate at fundamental switching frequency if it remains ON for one complete half cycle (either positive or negative) and remains OFF for the next complete half cycle, while the desired multilevel waveform is synthesized at the load terminals. Thus, fundamental frequency switching frequency is a control feature of modulation scheme, provided the topology permits so. In addition, when a topology consists of power switches with different voltage ratings, in order to properly distribute the switching losses, the higher voltage rated switches should be operated at comparatively lower switching frequencies while those with lower voltage rating should be operated with comparatively higher switching frequencies. Thus, the switching frequency should be calculatedly 'distributed' if the topology offers such a possibility. Also, if the level generation part of a topology can synthesize the zero level, then switches of polarity generation can be operated at the line frequency.

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B. Assessment Parameters

Merit of any given topology can be primarily judged based on the application for which it has to be employed. Still, in the context of this paper, the general criteria for an overall assessment of the merit of an RDC-MLI and its comparison with the other topologies can be:

i. The number of power switches used.
ii. The total blocking voltage of the converter.
iii. The optimal controllability of the topology, in terms of the possibilities of charge-balance control (or 'even power distribution' amongst the input sources) and appropriate distribution of switching frequencies amongst the differently voltage-rated switches.
iv. Possibility of employing asymmetric sources/capacitor voltage ratios in the topology.

While parameters (i) and (ii) affect reliability of the inverter, efficiency is influenced by parameters (i), (ii) and (iii) and application, performance and control complexity are governed by parameter (iii). Number of redundant states and consequently, programmability of fault tolerant operation, is directly influenced by (i) and (iv). In addition, apart from (i) and (ii), the cost of a converter also depends on the dispersion of power switching ratings (e.g. using one 400V switch and one 800V switch would be, in principle, more expensive than using two 600V switches).

C. Categorization of RDC-MLI Topologies

In this paper, nine different RDC-MLI topologies, as proposed in [50-68], are evaluated. These topologies are enlisted below:

i. Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter [50,51]
ii. T-type Inverter [52-54]
iii. Switched Series/Parallel Sources (SSPS) based MLI [55,56]
iv. Series Connected Switched Sources (SCSS) based MLI [57,58]
v. Cascaded 'Bipolar Switched Cells' (CBSC) based MLI [59]
vi. Packed-U Cell (PUC) Topology [60-64]
vii. Multilevel Module (MLM) based MLI [65]
viii. Reversing Voltage (RV) Topology [66,67]
ix. Two-Switch Enabled Level-Generation (2SELG) based MLI [68]

While a detailed analysis of these topologies is presented in Section III, it is important to appreciate that there are several similarities between the different RDC-MLI topologies which can be clearly seen if they are drawn with a similar structure, without taking into account the actual power switch configurations. For example, as shown in Fig.5 (a) and (b), it can be observed that the PUC topology is equivalent to the flying capacitor structure without DC sources. As indicated in Fig.5 (c) and (d), the T-type inverter [52-54] and CBSC based MLI [59] have similar units. The 2SELG based MLI [68] consists of repeated connection of the units used in MLM based MLI [65] as shown in Fig. 5(e) and (f). Similarly, the topologies proposed in [50, 55, 57, 66] consist of similar arrays of sources and switches connected in various fashions, as depicted in Fig.5 (g),(h),(i) and (j). With the help of Fig.5, it can be observed that the RDC-MLI topologies can be classified as those with H-bridge and those without H-bridge. In addition, these topologies may need isolated input DC levels or non-isolated input DC levels. Thus, a broad categorization of RDC-MLI topologies is presented in Fig.6.

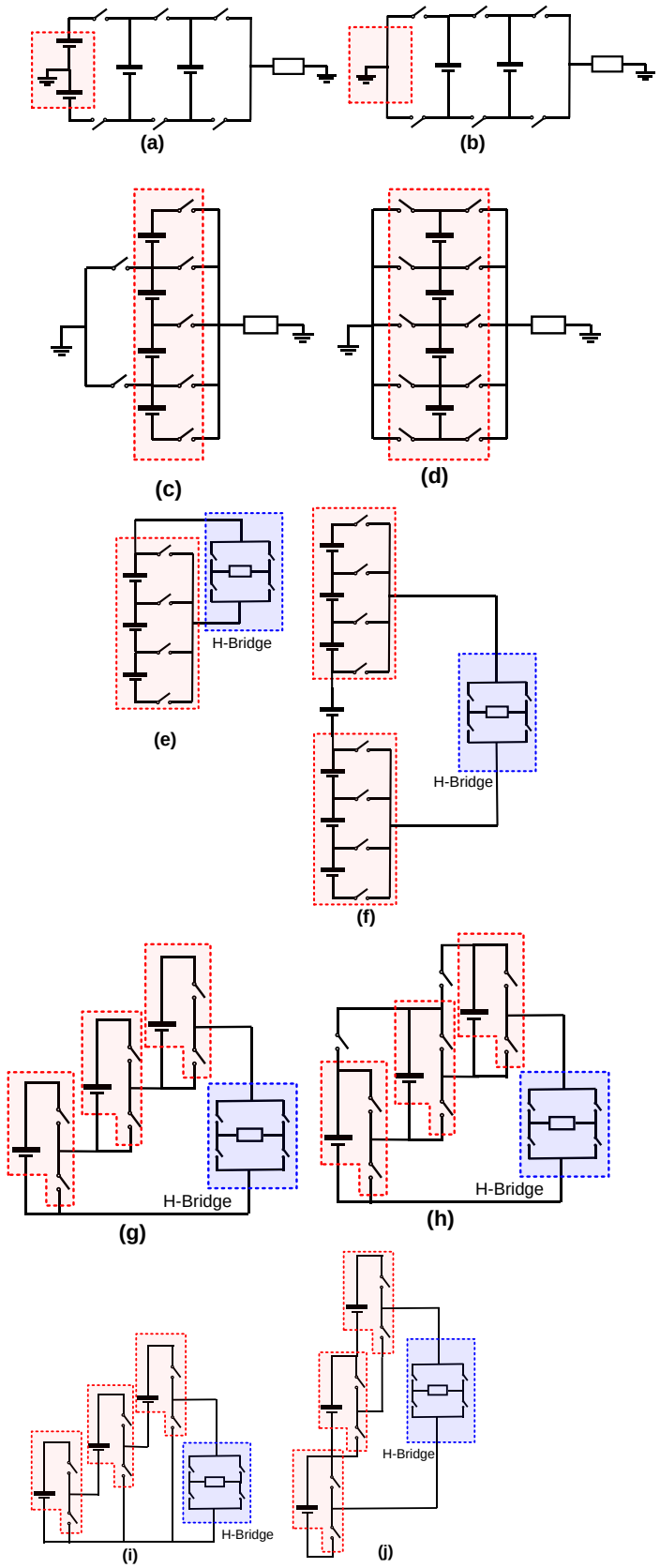

Fig.5. Similarities in the structures of various topologies

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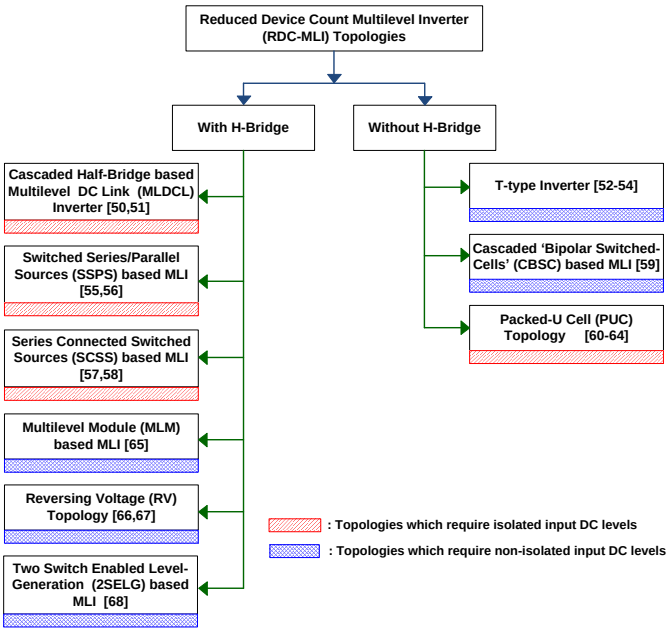

Fig.6 Categorization of reduced device count multilevel inverter (RDC-MLI) topologies

III. Review of Multilevel Inverter Topologies with Reduced Device Count

In this section, nine RDC-MLIs are reviewed and based on the parameters mentioned in section II B, topologies with reduced device count are discussed in this section. The topologies are presented in their single-phase form for the sake of simplicity. Their overall comparison, however, is carried out in terms of three-phase implementation, because MLIs are mostly administered in three-phase configurations. In addition, the illustrations for these topologies are indicated with four input sources and various valid switching states are tabulated. For the TCS-MLDCL inverter, however, seven sources are shown so that its general structure can be comprehended.

A. Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter

Gui Jia Su [50, 51] has presented a new multilevel inverter named as 'Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter'. An MLDCL inverter with four input DC levels is shown in Fig.7. It comprises of cascaded half-bridge cells, with each cell having its own DC source. It has separate 'level-generation' and 'polarity-generation' parts. The level-generation part comprises of the sources $V_{DC,j}$ { j = 1,2,3,4} and the power switches S_j { j = 1 to 8}. This part synthesizes a multilevel DC voltage, $v_{bus}(t)$, fed to the 'polarity-generation' part, comprising of switches Q_j{j = 1 to 4},which in turn alternates the polarity to produce a multilevel AC waveform.

Compared with the cascaded H-bridge topology, the MLDCL inverter can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases [50]. With reference to Fig.7, various valid switching combinations that can be used to obtain the multilevel DC link voltage $v_{bus}(t)$ are summarized in Table II.

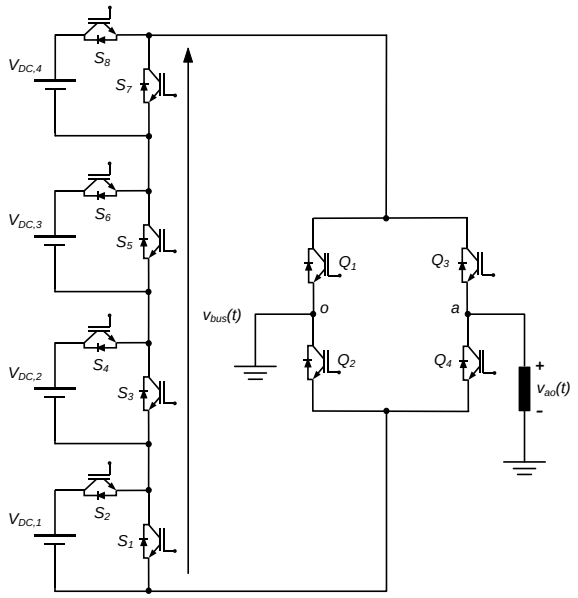

Fig. 7 Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter as proposed in [50, 51]

TABLE II
VALID SWITCHING STATES FOR THE 'MLDCL TOPOLOGY' SHOWN IN FIG.7

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_2 , S_3 , S_5 , S_7
2	$V_{DC,2}$	S_1 , S_4 , S_5 , S_7
3	$V_{DC,3}$	S_1 , S_3 , S_6 , S_7
4	$V_{DC,4}$	S_1 , S_3 , S_5 , S_8
5	$V_{DC,1}$ + $V_{DC,2}$	S_2 , S_4 , S_5 , S_7
6	$V_{DC,1}$+ $V_{DC,3}$	S_2 , S_3 , S_6 , S_7
7	$V_{DC,1}$ + $V_{DC,4}$	S_2 , S_3 , S_5 , S_8
8	$V_{DC,2}$ + $V_{DC,3}$	S_1 , S_4 , S_6 , S_7
9	$V_{DC,2}$ + $V_{DC,4}$	S_1 , S_4 , S_5 , S_8
10	$V_{DC,3}$ + $V_{DC,4}$	S_1 , S_3 , S_6 , S_8
11	$V_{DC,1}$ + $V_{DC,2}$+ $V_{DC,3}$	S_2 , S_4 , S_6 , S_7
12	$V_{DC,2}$ + $V_{DC,3}$+ $V_{DC,4}$	S_1 , S_4 , S_6 , S_8
13	$V_{DC,1}$ + $V_{DC,3}$+ $V_{DC,4}$	S_2 , S_3 , S_6 , S_8
14	$V_{DC,1}$ + $V_{DC,2}$+ $V_{DC,4}$	S_2 , S_4 , S_5 , S_8
15	$V_{DC,1}$ + $V_{DC,2}$+ $V_{DC,3}$+ $V_{DC,4}$	S_2 , S_4 , S_6 , S_8
16	0	S_1 , S_3 , S_5 , S_7

It can be observed from table II that to obtain a given level, four switches conduct simultaneously for the level-generation part and two switches conduct for the polarity-generation part (switches Q_1 and Q_4 for the positive half cycle, Q_2 and Q_3 for the negative half cycle and Q_1, Q_3 / Q_2 , Q_4 for the zero level). It can be observed from the topology that each power switch of polarity-generation part must possess a minimum voltage blocking capability equal to the sum of the input voltage values. Thus these switches are rated higher as compared to the switches in the level-generation part. However, since the zero level can be synthesized using switches of the polarity-generation part, the higher rated switches Q_j { j = 1 to 4} can be operated at fundamental switching frequency.

For a symmetric source configuration with $V_{DC,1}$ = $V_{DC,2}$ = $V_{DC,3}$ = $V_{DC,4}$ = V_{DC} , it can be observed that the switches S_j { j = 1 to 8} need to block a voltage of V_{DC} and need to conduct a current equal to the load current while the switches Q_j {j = 1 to 4} need to block a voltage equal to $4V_{DC}$ and conduct a current equal to the load current. Moreover, it can be observed from Table II that since voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$ and

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$4V_{DC}$ can be synthesized combining all the input sources in groups of one, two and three respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing, in case capacitors are used.

Regarding asymmetric source configurations in the MLDCL topology, no comments are offered in [50, 51]. Since subtractive combinations of the input DC levels cannot be synthesized, the trinary source configuration cannot be employed for this topology. As it can be observed from Table II, a binary source configuration with $V_{DC,1} = V_{DC}$, $V_{DC,2} = 2V_{DC}$, $V_{DC,3} = 4V_{DC}$ and $V_{DC,4} = 8V_{DC}$ is possible since the voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$ .... $15V_{DC}$ can be synthesized by utilizing the states presented in Table II.

As suggested by the author in [50,51], one application area in the low-power range (< 100 kW) for the MLDCL inverters is in the permanent-magnet (PM) motor drives employing a PM motor of very low inductance. The level-generation part can utilize the fast-switching low-cost low-voltage MOSFETs and the polarity-generation part can use IGBTs so as to dramatically reduce the current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. The MLDCL inverter can also be applied in distributed power generation involving fuel cells and photovoltaic cells.

B. T-type Inverter

Gerardo Ceglia *et. al.* [52-54] reported a new multilevel inverter topology, herewith referred to as the 'T-type inverter'. The primary introduction to the topology is described in [52] with the help of a five-level single-phase inverter which results in a significant reduction in the number of power devices as compared to the conventional topologies. A single-phase structure of the topology with four input voltage sources is shown in Fig.8. It comprises of three switches S_j {j = 1,2,3} which are bidirectional-blocking-bidirectional-conducting while four switches Q_j{j= 1 to 4} are unidirectional-blocking-bidirectional-conducting.

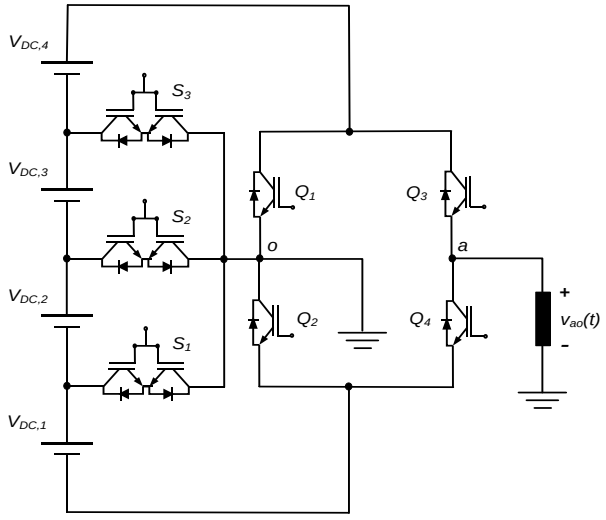

Fig. 8 T-type Inverter as proposed in [52-54]

Thus, this topology inadvertently requires a mix of unidirectional and bidirectional power switches. Valid switching states for the inverter are summarized in Table III and it can be seen that the input DC values are required to be symmetric i.e. $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$. This is so because not all the additive/subtractive combinations of the input voltage levels can be synthesized at the load terminals and many times either a positive or negative combination can be synthesized but not both. For example, while a voltage level $-V_{DC,4}$ can be synthesized at the load terminals, the level $+V_{DC,4}$ cannot be synthesized. Thus, it is imperative that the input sources are symmetric. Also, lack of sufficient redundancies goes against an effective voltage balancing. It can also be observed from Table III that equal load sharing amongst the input voltage sources is not possible as the number of valid states is very limited. For a given state, only two switches conduct simultaneously. The bidirectional switches are voltage-rated at different values. While S_2 should be minimally rated at $2V_{DC}$, S_1 and S_3 should be rated at $3V_{DC}$ each. Switches Q_j {j = 1 to 4} must have minimum blocking capability of $4V_{DC}$ each. These higher-voltage rated switches, however, can be operated at the fundamental switching frequency. A three-phase inverter based on this topology can be implemented with a single DC link. In addition, available literature indicates that it can be effectively used for drives and renewable energy based applications.

TABLE III
VALID SWITCHING STATES FOR THE 'T-TYPE INVERTER' SHOWN IN FIG.8

State	Output voltage [$v_{ao}(t)$]	Switches in ON state
1	$-V_{DC,1}$	S_1 , Q_4
2	$V_{DC,4}$	S_3 , Q_3
3	$-(V_{DC,1}+V_{DC,2})$	S_2 , Q_4
4	$V_{DC,3}+V_{DC,4}$	S_2 , Q_3
5	$-(V_{DC,1}+V_{DC,2}+V_{DC,3})$	S_3 , Q_4
6	$V_{DC,2}+V_{DC,3}+V_{DC,4}$	S_1, Q_3
7	$-(V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4})$	Q_1 , Q_4
8	$V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4}$	Q_2 , Q_3
9	0	Q_1 , Q_3
10	0	Q_2 , Q_4

C. Switched Series/Parallel Sources (SSPS) based MLI

Hinago and Koizumi [55, 56] proposed a single-phase multilevel inverter consisting of an H-bridge and DC sources which can be switched in series and in parallel. The topology is herewith referred to as 'switched series/parallel sources (SSPS) based MLI. The topology requires the same of number of voltage sources as required by a cascaded H-bridge topology but it synthesizes same number of output levels with lesser number of power switches. An important application suggested is for electric vehicular applications where a single battery composed of a number of series-connected battery cells is available, which can be rearranged using the switched sources topology, hence reducing the requirement of switching devices. More importantly, possibility of combining two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive system.

The aforesaid topology with four input DC sources is shown in Fig.9, consisting of two parts: level-generation part which consists of the switched sources and synthesizes a bus voltage v_{bus} (t) and the polarity-generation part which synthesizes positive and negative cycles of voltage v_{bus} (t) to feed an AC load. Four sources $V_{DC,j}$ {j = 1 to 4} and power switches S_j {j = 1 to 9} constitute the level-generation part

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while power switches Q_j {j = 1 to 4} constitute the polarity-generation part. The voltage levels which can be synthesized by the switched sources part are summarized in Table IV.

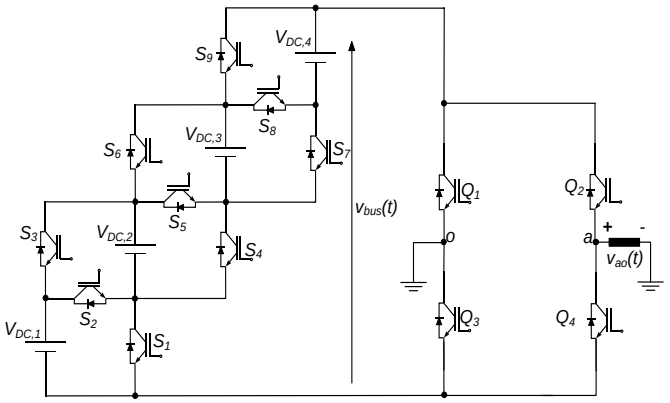

Fig. 9 Switched Series/Parallel Sources (SSPS) based MLI as proposed in [55, 56]

TABLE IV
VALID SWITCHING STATES FOR THE 'SPSS- MLI' SHOWN IN FIG.9

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_3 , S_6 , S_9
2	$V_{DC,2}$	S_1 , S_6 , S_9
3	$V_{DC,3}$	S_1 , S_4 , S_9
4	$V_{DC,4}$	S_1 , S_4 , S_7
5	$V_{DC,1}$ + $V_{DC,2}$	S_2 , S_6 , S_9
6	$V_{DC,1}$ + $V_{DC,3}$	S_3 , S_5 , S_9
7	$V_{DC,1}$ + $V_{DC,4}$	S_3 , S_6 , S_8
8	$V_{DC,2}$ + $V_{DC,3}$	S_1 , S_5 , S_9
9	$V_{DC,2}$ + $V_{DC,4}$	S_1 , S_5 , S_7
10	$V_{DC,3}$ + $V_{DC,4}$	S_1 , S_4 , S_8
11	$V_{DC,1}$ + $V_{DC,2}$ + $V_{DC,3}$	S_2 , S_5 , S_9
12	$V_{DC,1}$ + $V_{DC,2}$ + $V_{DC,4}$	S_2 , S_6 , S_8
13	$V_{DC,2}$ + $V_{DC,3}$ + $V_{DC,4}$	S_1 , S_5 , S_8
14	$V_{DC,1}$ + $V_{DC,3}$ + $V_{DC,4}$	S_3 , S_5 , S_9
15	$V_{DC,1}$ + $V_{DC,2}$+ $V_{DC,3}$+ $V_{DC,4}$	S_2 , S_5 , S_8

For a symmetric source configuration i.e. $V_{DC,1}$ = $V_{DC,2}$ = $V_{DC,3}$ = $V_{DC,4}$ = V_{DC}, it can be observed from Table IV that the voltage levels V_{DC} and $2V_{DC}$ can be synthesized with three states each while one state is available for voltage level $3V_{DC}$. Moreover, the voltage stress experienced by the switches S_j { j = 1 to 9 } in this case would be equal to V_{DC} each. An important limitation of this topology is that the switches Q_j { j = 1 to 4 } need to have a minimum blocking capability equal to summation of voltages of all voltage sources. Thus, for the symmetric source configuration with four sources, the switches of polarity-generation part should possess voltage blocking capability of $4V_{DC}$. Another important limitation is that these switches with higher blocking capability cannot be operated at fundamental switching frequency because the zero voltage level is not synthesized by the switched sources part, as can be observed from Table IV. It can also be inferred from the table that, with input sources of equal voltages, equal load sharing amongst them is possible as the sources can be combined in all additive configurations.

Authors of literature [55, 56] do not comment on the possibilities of asymmetric source configuration in this topology. Although the topology enables the synthesis of all additive combinations of the input sources, subtractive combinations are not possible. Hence, trinary source configuration cannot be employed this topology. Binary source configuration, however, is possible so as to maximize the number of levels in the output waveform. For example, in Fig.9, for $V_{DC,1}$ = V_{DC}, $V_{DC,2}$ =$2V_{DC}$, $V_{DC,3}$ = $4V_{DC}$ and $V_{DC,4}$ = $8V_{DC}$, it can be observed using Table IV that all the voltage levels from V_{DC} to $15V_{DC}$, in steps of V_{DC}, can be obtained as $v_{bus}(t)$ (with the respective use of states 1 to 15) so that the load voltage waveform has fifteen levels.

D. Series Connected Switched Sources (SCSS) based MLI

A topology with sources connected in series through power switches is described in literature [57, 58]. The topology with four input DC sources $V_{DC,j}$ { j = 1 to 4} is shown in Fig.10. The low potential terminals of the sources are all connected through power switches while being also connected to the higher potential terminal of the preceding source through power switches, as illustrated in Fig.10 with S_j { j = 1 to 8}. This interconnection is capable of synthesizing a multilevel rectified waveform $v_{bus}(t)$ (the level-generation part), which is imparted positive and negative polarities using the H-bridge comprising of switches Q_j{ j = 1 to 4} (the polarity-generation part).

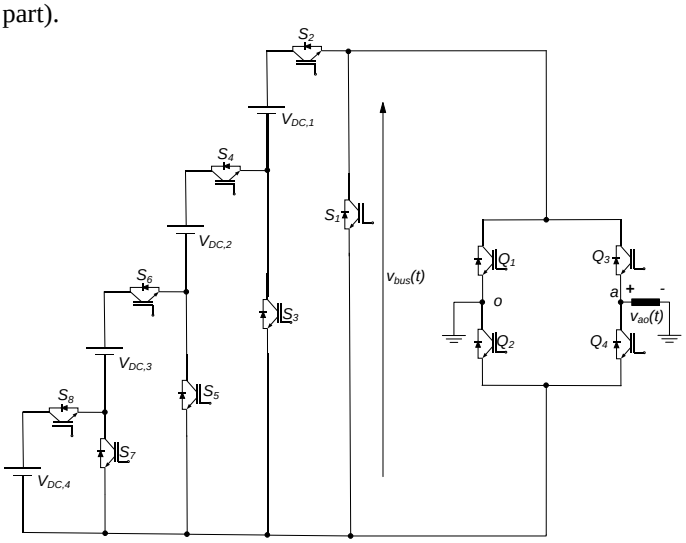

Fig. 10 Series Connected Switched Sources (SCSS) based MLI as proposed in [57, 58]

TABLE V
VALID SWITCHING COMBINATIONS FOR THE 'SCSS- MLI' SHOWN IN FIG.10

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_2,S_3
2	$V_{DC,1}$ + $V_{DC,2}$	S_2 , S_4, S_5
3	$V_{DC,1}$ + $V_{DC,2}$ + $V_{DC,3}$	S_2 , S_4, S_6, S_7
4	$V_{DC,1}$ + $V_{DC,2}$ +$V_{DC,3}$ + $V_{DC,4}$	S_2, S_4, S_6, S_8
5	0	S_1

The possibilities of synthesizing various combinations of input DC levels are summarized in Table V. It can be seen that the structure, though simple, allows very restricted possibilities of synthesis of various levels at the bus end. In fact, not even the individual levels offered by the sources can all be obtained as $v_{bus}(t)$, except that of $V_{DC,1}$. Thus, this topology does not offer any possibility of employing asymmetric source configurations for further reducing the switch count. The source configuration mandatorily needs to be symmetric i.e. $V_{DC,1}$ = $V_{DC,2}$ = $V_{DC,3}$ = $V_{DC,4}$ = V_{DC}. With such configuration, various switches would be differently voltage rated, that is to say, switches Q_j{ j = 1 to 4} should be

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minimally rated at $4V_{DC}$, S_1 should be rated minimally at $4V_{DC}$, while S_3, S_5 and S_7 should be minimally rated at $3V_{DC}$, $2V_{DC}$ and V_{DC} respectively. Moreover, as it can be observed from Table V, for symmetric input sources, equal load sharing is not possible as there are many combinations of input DC levels which are not feasible. Also, since the zero level can be obtained as $v_{bus}(t)$, the higher rated switches Q_j { j = 1 to 4} can be operated at the fundamental switching frequency.

E. Cascaded 'Bipolar Switched Cells' (CBSC) based MLI

Babaei *et al.* in [59] introduced a new class of MLI topology, here referred to as 'cascaded bipolar switched cells (CBSC) based MLI'. Fig. 11 shows the single-phase structure of the topology with four input voltage sources. The topology requires all the switches to be bidirectional-blocking-bidirectional-conducting in order to synthesize the required voltage levels at the output. The structure is such that each 'cell' consisting of a source and power switches can synthesize voltage levels with both its polarities at the load terminals. Although each bidirectional switch requires two IGBTs, the total number of gate drive circuits is equal to the number of bidirectional switches. This results in reducing the cost and overall complexity of the converter.

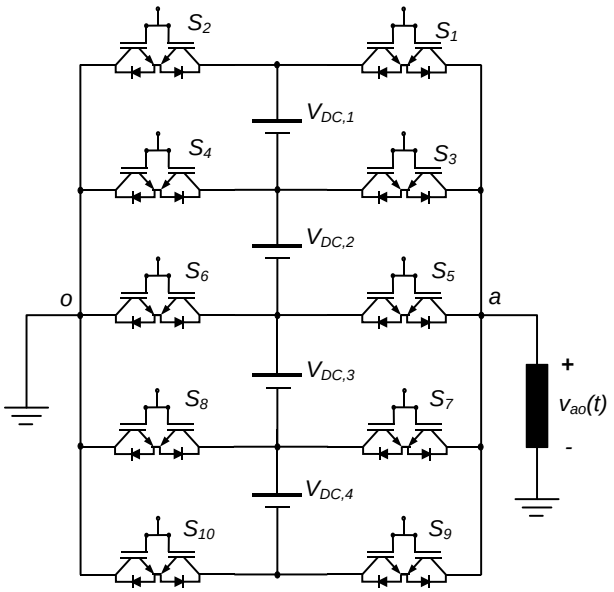

Fig. 11 Cascaded 'Bipolar Switched Cells' (CBSC) based MLI as proposed in [59]

The valid switching states for all possible combination of input voltage sources are given in Table VI. It should also be noted that the topology can only work with a symmetric source configuration. Asymmetric source configurations (binary or trinary) are not possible, since many subtractive and additive combinations of the input DC levels cannot be synthesized. Considering a symmetric source configuration with all input sources equal to V_{DC}, it can be observed that while synthesizing $2V_{DC}$ and $-2V_{DC}$, not all possible combinations of input voltage sources are utilized. Similar is the case for synthesis of voltage levels $3V_{DC}$ and $-3V_{DC}$. As a result, equal utilization of the input voltage sources is not possible in this topology. Moreover, outermost bidirectional switches S_1, S_2, S_9 and S_{10} need to have minimum voltage blocking capability of $4V_{DC}$ each. On the other hand, the inner switches S_3, S_4, S_7 and S_8 need to have minimum voltage blocking capability of $3V_{DC}$. Similarly, switches S_5 and S_6 need to bear a voltage stress of $2V_{DC}$. One can also observe that for synthesizing each voltage level, only two switches need to conduct simultaneously. This may result in equal conduction and switching losses. In addition, the topology requires non-isolated DC sources.

TABLE VI
VALID SWITCHING COMBINATIONS FOR THE CBSC-MLI SHOWN IN FIG.11

State	Output voltage [$v_{ao}(t)$]	Switches in ON state
1	$V_{DC,1}$	S_1, S_4
2	$V_{DC,2}$	S_3, S_6
3	$V_{DC,3}$	S_5, S_8
4	$V_{DC,4}$	S_7, S_{10}
5	$V_{DC,1}+V_{DC,2}$	S_1, S_6
6	$V_{DC,2}+V_{DC,3}$	S_3, S_8
7	$V_{DC,3}+V_{DC,4}$	S_5, S_{10}
8	$V_{DC,1}+V_{DC,2}+V_{DC,3}$	S_1, S_8
9	$V_{DC,2}+V_{DC,3}+V_{DC,4}$	S_3, S_{10}
10	$V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4}$	S_1, S_{10}
11	$-V_{DC,1}$	S_2, S_3
12	$-V_{DC,2}$	S_4, S_5
13	$-V_{DC,3}$	S_6, S_7
14	$-V_{DC,4}$	S_8, S_9
15	$-(V_{DC,1}+V_{DC,2})$	S_2, S_5
16	$-(V_{DC,2}+V_{DC,3})$	S_4, S_7
17	$-(V_{DC,3}+V_{DC,4})$	S_6, S_9
18	$-(V_{DC,1}+V_{DC,2}+V_{DC,3})$	S_2, S_7
19	$-(V_{DC,2}+V_{DC,3}+V_{DC,4})$	S_4, S_9
20	$-(V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4})$	S_2, S_9
21	0	S_9, S_{10}
22	0	S_1, S_2

F. Packed U-Cell (PUC) Topology

In [60-64], Youssef Ounejjar *et al.* proposed a new power multilevel converter topology that is very competitive compared to the classical topologies. The topology is named as the 'packed U-cell (PUC)' topology. It consists of the so-called 'packed U-cells'. Each U-cell consists of an arrangement of two power switches and one DC input level (obtained with a voltage source or a floating capacitor). Authors claim that the topology offers high energy conversion quality using a small number of active and passive devices and consequently, has very low production cost. A single-phase structure of the packed U-cell topology with four input DC levels, $V_{DC,j}$ {j = 1 to 4}, and ten switches S_j {j = 1 to 10}, is shown in Fig.12.

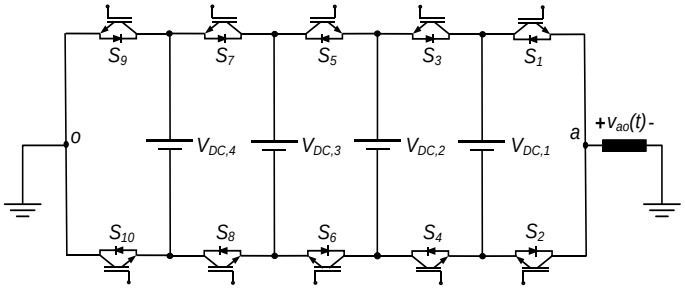

Fig.12 Packed U-cell MLI topology as proposed in [60-64]

The PUC topology is very simple in terms of interconnection of components. The minimal voltage blocking capability required for the switches are : $V_{DC,1}$ for S_1 and S_2,

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($V_{DC,1} - V_{DC,2}$) for S_3 and S_4, ($V_{DC,2} - V_{DC,3}$) for S_5 and S_6, ($V_{DC,3} - V_{DC,4}$) for S_7 and S_8 and $V_{DC,4}$ for S_9 and S_{10}. All the switches, when conducting, should be able to carry the load current. Various valid states for the structure are shown in Table VII. Thus, with four input levels, only five switches conduct simultaneously to obtain a desired voltage level. It is important to observe from Table VII that to derive desired benefit from the topology, symmetric source configuration cannot be used.

TABLE VII
VALID SWITCHING STATES FOR THE PUC TOPOLOGY SHOWN IN FIG.12

State	Output voltage $v_{ao}(t)$	Switches in ON state
1	0	S_1, S_3, S_5, S_7, S_9
2	0	$S_2, S_4, S_6, S_8, S_{10}$
3	$V_{DC,1}$	$S_1, S_4, S_6, S_8, S_{10}$
4	$-V_{DC,1}$	S_2, S_3, S_5, S_7, S_9
5	$V_{DC,2}$	S_1, S_3, S_4, S_6, S_8
6	$-V_{DC,2}$	S_2, S_4, S_5, S_7, S_9
7	$V_{DC,3}$	$S_1, S_3, S_5, S_8, S_{10}$
8	$-V_{DC,3}$	S_2, S_4, S_6, S_7, S_9
9	$V_{DC,4}$	$S_1, S_3, S_5, S_7, S_{10}$
10	$-V_{DC,4}$	S_2, S_4, S_6, S_8, S_9
11	$V_{DC,4}-V_{DC,3}$	$S_2, S_4, S_6, S_7, S_{10}$
12	$-(V_{DC,4}-V_{DC,3})$	S_1, S_3, S_5, S_8, S_9
13	$V_{DC,3}-V_{DC,2}$	$S_2, S_4, S_5, S_8, S_{10}$
14	$-(V_{DC,3}-V_{DC,2})$	S_1, S_3, S_6, S_7, S_9
15	$V_{DC,4}-V_{DC,3}+V_{DC,2}$	S_2, S_4, S_5, S_8, S_9
16	$-(V_{DC,4}-V_{DC,3}+V_{DC,2})$	$S_1, S_3, S_6, S_7, S_{10}$
17	$V_{DC,4}-V_{DC,2}$	$S_2, S_4, S_5, S_7, S_{10}$
18	$-(V_{DC,4}-V_{DC,2})$	S_1, S_3, S_6, S_8, S_9
19	$V_{DC,2}-V_{DC,1}$	$S_2, S_3, S_6, S_8, S_{10}$
20	$-(V_{DC,2}-V_{DC,1})$	S_1, S_4, S_5, S_7, S_9
21	$V_{DC,4}-V_{DC,2}+V_{DC,1}$	S_2, S_3, S_6, S_8, S_9
22	$-(V_{DC,4}-V_{DC,2}+V_{DC,1})$	$S_1, S_4, S_5, S_7, S_{10}$
23	$V_{DC,1}-V_{DC,2}+V_{DC,3}-V_{DC,4}$	$S_2, S_3, S_6, S_7, S_{10}$
24	$-(V_{DC,1}-V_{DC,2}+V_{DC,3}-V_{DC,4})$	S_1, S_4, S_5, S_8, S_9
25	$V_{DC,1}-V_{DC,2}+V_{DC,3}$	S_2, S_3, S_6, S_7, S_9
26	$-(V_{DC,1}-V_{DC,2}+V_{DC,3})$	$S_1, S_4, S_5, S_8, S_{10}$
27	$V_{DC,1}-V_{DC,3}$	$S_2, S_3, S_5, S_8, S_{10}$
28	$-(V_{DC,1}-V_{DC,3})$	S_1, S_4, S_6, S_7, S_9
29	$V_{DC,1}-V_{DC,3}+V_{DC,4}$	S_2, S_3, S_5, S_8, S_9
30	$-(V_{DC,1}-V_{DC,3}+V_{DC,4})$	$S_1, S_4, S_6, S_7, S_{10}$
31	$V_{DC,1}-V_{DC,4}$	$S_2, S_3, S_5, S_7, S_{10}$
32	$-(V_{DC,1}-V_{DC,4})$	S_1, S_4, S_6, S_8, S_9

In fact, in [64], the authors have proposed an elaborate methodology to calculate the asymmetric voltage levels. For a structure with two input sources, switching of middle two switches can be performed at fundamental frequency as demonstrated in [64]. This feature, however, is not feasible for the PUC topology with more than two number of input DC levels. In [64], the authors have described the PUC topology with two input sources. One source is taken as a floating capacitor in which the voltage is maintained at one-third of the voltage level of the other source (obtained with the rectification of input AC). The control scheme, though, is fairly complex in nature.

G. Multilevel Module (MLM) based MLI

Babaei [65] presented another multilevel converter topology, known as 'multilevel module (MLM)' based MLI. The topology consists of separate 'level-generation' and 'polarity-generation' parts. The level-generation part consists of input DC sources and bidirectional-blocking-bidirectional-conducting switches. The voltage stress on these switches is not distributed uniformly. The switches in the polarity-generation part are unidirectional-blocking-bidirectional-conducting and have to withstand the maximum voltage generated by the level generation part. However, these switches can be operated at line frequency as the level generation part is able to generate the zero level. Thus, these switches are high-voltage low-frequency switches.

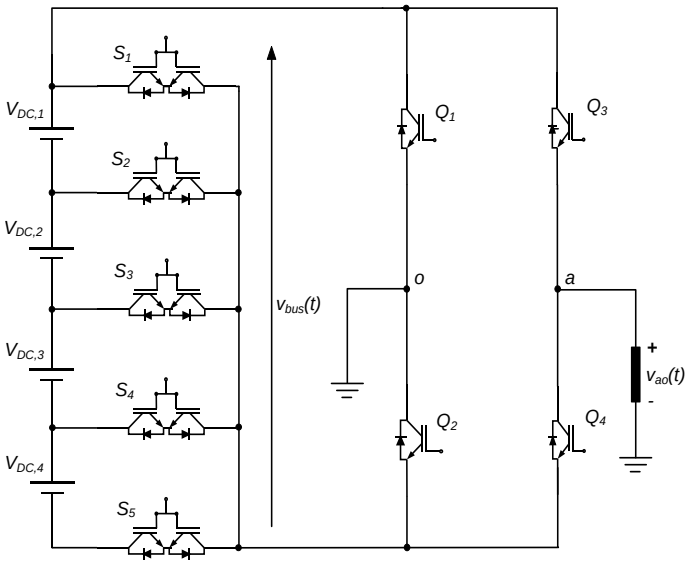

Fig.13 Multilevel Module (MLM) based MLI as proposed in [65]

TABLE VIII
VALID SWITCHING COMBINATIONS FOR THE 'MLM-MLI' SHOWN IN FIG.13

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_2
2	$V_{DC,1} + V_{DC,2}$	S_3
3	$V_{DC,3} + V_{DC,4}$	S_1, S_3, S_5
4	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_4
5	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_5
6	*0*	S_1

A single-phase MLM-MLI with four input sources is shown in Fig.13. All the valid operating states are listed in Table VIII. The proposed topology does not facilitate asymmetrical source configuration (binary or trinary) because it is not possible to synthesize all subtractive and additive combination of the input voltage levels. For $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, it is evident that all the possible combinations of the input voltage levels are not utilized. Thus in this topology, equal load sharing amongst the input sources is not possible. Also, the switches in the polarity-generation part are subjected to the voltage stress of $4V_{DC}$ each. For the level-generation part, switches S_1 and S_5 need to have minimum voltage blocking capability of $4V_{DC}$ whereas switches S_2 and S_4 should be selected to bear the voltage stress of $3V_{DC}$. Switch S_3 needs to bear voltage stress of $2V_{DC}$. However, only one switch in the level-generation part and two switches in the polarity-generation part need to conduct simultaneously to synthesize the required voltage level at the output.

H. Reversing Voltage (RV) Topology

In [66, 67] Najafi *et al.* have proposed a so-called 'reversing voltage' MLI (RV-MLI) topology which separates the output voltage into two parts: 'level-generation' and 'polarity-

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generation'. A single-phase RV-MLI with four input DC sources, $V_{DC,j}$ {j = 1 to 4}, is shown in Fig.14. The level-generation part comprising of the input DC sources and switches S_j {j = 1 to 8}. The polarity-generation part consists of switches Q_j {j = 1 to 8}, operating at the line frequency. In this way, the components are utilized effectively. The switches in the polarity-generation part need to withstand the total additive voltage of the level generation part. The topology exhibits modularity for the level generation part.

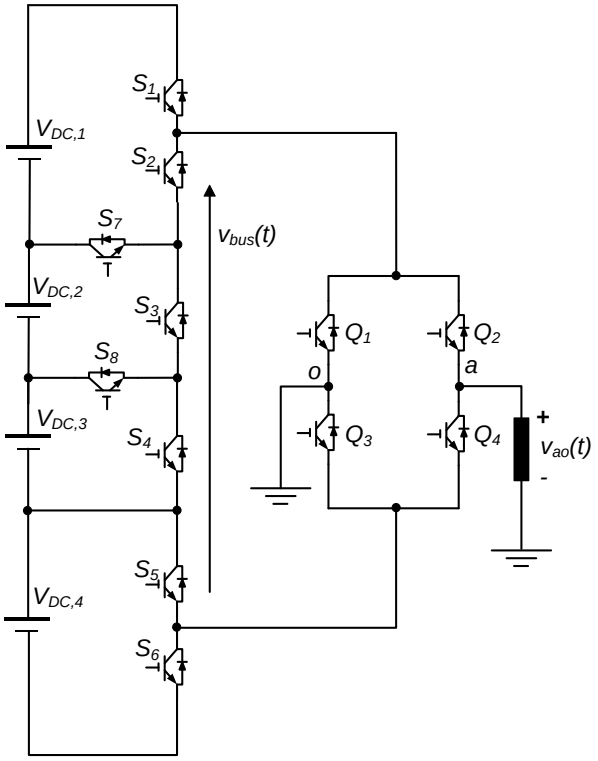

Fig.14 Reversing Voltage (RV) Topology as proposed in [66, 67]

To overcome the issue of voltage balancing, authors in [66, 67] have proposed use of separate DC sources. It is, however, true for several topologies that separate sources can solve the voltage unbalance problem. If separate sources are not used, balancing will have to be achieved by proper utilization of redundant states**.** Various valid states for possible combinations of input sources so as to obtain different levels at the level generation part, $v_{bus}(t)$, are summarized in Table IX. It can be noted that the switches with high blocking voltages, Q_j{j = 1 to 4}, can be operated at fundamental switching frequency as the zero level voltage can be synthesized at the level generation part itself. If symmetric sources are used such that $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, then all switches of the level generation part experience a voltage stress of V_{DC} , while the four switches of the polarity generation part are required to have minimum voltage blocking capability of $4V_{DC}$ each. It can also be inferred from Table IX that for a symmetric source configuration, equal load sharing amongst them is not possible as all source combinations cannot be employed for various cycles of output voltage. For a DC link created with connected capacitors, this limitation will affect voltage balancing in the capacitors. It can also be observed from Table IX that the number of switches conducting simultaneously to synthesize various voltage levels is not same for all the states and thus, conduction losses and switching losses for the switches may not be same. Moreover, since the topology does not facilitate the synthesis of all additive and subtractive combinations of input voltage sources, trinary source combination cannot be implemented with this topology.

TABLE IX
VALID SWITCHING COMBINATIONS FOR THE 'RV TOPOLOGY' SHOWN IN FIG.14

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_1, S_3, S_4,S_5,S_7
2	$V_{DC,3}$	S_2, S_3,S_5,S_8
3	$V_{DC,4}$	S_2, S_3,S_4,S_6
4	$V_{DC,1} + V_{DC,2}$	S_1,S_4,S_5, S_8
5	$V_{DC,2} + V_{DC,3}$	S_2,S_5, S_7
6	$V_{DC,3} + V_{DC,4}$	S_2,S_3,S_6, S_8
7	$V_{DC,1} + V_{DC,4}$	S_1,S_3,S_4, S_6,S_7
8	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_1, S_5
9	$V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_2,S_6, S_7
10	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_1, S_6
11	0	S_2, S_3, S_4,S_5

Employing other asymmetric combinations to maximize the number of output levels is seriously hampered by the absence of some states with a single voltage source. However, one important advantage of the topology is that it uses a single DC link for three-phase implementation, thereby offering savings in the number of input voltage sources.

I. Two-Switch Enabled Level Generation (2SELG) based MLI

The topology presented by Babaei in [68] has separate 'level-generation' and 'polarity-generation' parts. The specialty of this topology is that the level-generation part requires only two conducting switches to synthesize any valid voltage level, irrespective of the number of input sources. Therefore, this topology is referred to as 'two-switch enabled level generation (2SELG) based MLI'. A single-phase configuration of 2SELG-MLI with seven input levels, $V_{DC,j}$ {j = 1 to 7}, is shown in Fig.15.

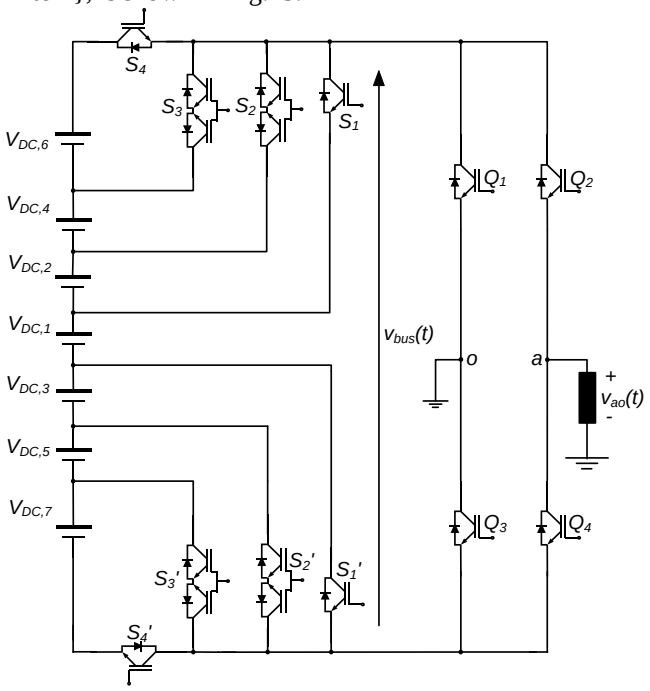

Fig. 15 Two-Switch Enabled Level-Generation (2SELG) based MLI as proposed in [68]

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The topology requires a mix of unidirectional and bidirectional switches. The valid switching states are shown in Table X. It can be seen that the level-generation part is unable to realize the zero level by itself. The switches of the polarity-generation part, therefore, cannot operate with a fundamental switching frequency.

TABLE X
VALID SWITCHING STATES FOR THE '2SELG-MLI' SHOWN IN FIG.15

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_1, S_1'
2	$V_{DC,1} + V_{DC,2}$	S_2, S_1'
3	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_2'
4	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_3, S_2'
5	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5}$	S_3, S_3'
6	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5} + V_{DC,6}$	S_4, S_3'
7	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5} + V_{DC,6} + V_{DC,7}$	S_4, S_4'

For a symmetrical source configuration, $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC,5} = V_{DC,6} = V_{DC,7} = V_{DC}$, it is not possible to apply the concept of 'even power distribution' in this topology, as all the sources do not contribute equally for each level in the $v_{bus}(t)$. Also, the switches in the polarity-generation part need to have minimum voltage blocking capability of $7V_{DC}$. Switches S_1, S_4, S_1' and S_4 need to have minimum voltage blocking capability of $3V_{DC}$. Rest of the switches need to have minimum voltage blocking capability of $2V_{DC}$ .It is also observed that this topology does not support asymmetrical source configuration (binary or trinary) as it is not possible to synthesize all subtractive and additive combinations of the input voltage levels. However, one advantage offered by 2SELG-MLI is that a total of four power electronic switches need to be conducting in all the switching states, thus resulting in lower conduction losses.

IV. DISCUSSIONS

Based on the analysis of RDC-MLI topologies presented in the previous section, comments can be made on them based on qualitative and quantitative parameters. Based on the qualitative features of these topologies, a summary is presented in Table XI. MLDCL-MLI is a highly modular structure whereas the PUC topology can be appreciated for its sheer simplicity in terms of its structure. Both the topologies, however, require isolated DC sources. SSPS-MLI presents novelty in terms of enabling series and parallel combinations of all the input DC levels. Structures such as T-type inverter, CBSC-MLI, MLM-MLI and RV topology require non-isolated input DC levels. Also, three-phase configurations with the T-type inverter and RV topology can be implemented with a single DC link. An important feature of 2SELG-MLI is that only four switches need to conduct to obtain a given voltage level across the load terminals. It can be said that when attempts are made to reduce the power switch count, the number of states are reduced and following features may be hampered: even power distribution amongst the symmetric input sources and possibility of employing binary/trinary source configuration(s). The topologies with isolated input DC sources can be used for applications such renewable energy and battery operated vehicles whereas topologies with a single DC link can be appropriate for AC-DC-AC based applications. Topologies with separate level-generation and polarity-generation parts, however, may find restrictions for high voltage applications because the power switches in the polarity-generation part need to block the total input voltage. Table XI can be helpful for identifying suitable topology/topologies for the mandated application when design restrictions (availability/non-availability of isolated DC sources) and performance characteristics (e.g. requirement of even power distribution) are given.

Quantitative features of RDC-MLI topologies are summarized in Table XII in terms of the count of power switches for three-phase applications and total blocking voltage requirements. In Table XII, the 'classical topologies' are also included. All the topologies are considered with symmetric input sources. Consequently, the Packed U-cell topology does not appear in Table XII since it mandatorily requires asymmetric sources. It can be observed from Table XII that some topologies require a mix of unidirectional and bidirectional power switches. Some topologies require power switches with a variety of voltage ratings. Both these factors present difficulty in the converter design. In addition, a general trend that can be observed is that as an attempt is made to reduce the power switch count, the voltage ratings of converter switches increase. Table XII along with Table XI can be used to choose an appropriate topology with the calculations of total number of power switches with their respective voltage ratings. Thus, an estimation of overall cost consideration can be arrived at.

V. CONCLUSION

As multilevel inverters continue to gain increasing importance for both high power and low power applications, many researchers have proposed specific topological solutions for intended applications. Also, newer multilevel topologies have been proposed, offering high output resolution with a reduced number of power switches. In this paper, a review of nine reduced device count multilevel topologies is presented. Based on the review, it can be concluded that in the process of reducing the power switch count, various compromises are involved such as:

i. Increased voltage rating of semiconductor switches.
ii. Requirement of bidirectional switches
iii. Increased number of sources and/or requirement of asymmetric input DC levels.
iv. Loss of modularity.
v. Reduced number of redundant states.
vi. Complex modulation / control schemes.
vii. Difficulty in possibility of charge balance control.

In this paper, qualitative and quantitative features of RDC-MLI topologies have been discussed and a comparison has been made so as to facilitate a well-informed selection of topology for a given application. In addition, the paradigm presented in the paper will also help to evaluate the RDC-MLI topologies that will be proposed in future.

TABLE XI
ADVANTAGES AND LIMITATIONS OF REDUCED DEVICE COUNT MULTILEVEL INVERTER (RDC-MLI) TOPOLOGIES

Topology	Literature	Advantages	Limitations
MLDCL-MLI	Proposed in [50,51]	• Highly modular and simple • Requires only unidirectional switches • Equal load sharing is possible amongst symmetric input sources • Highest voltage rated switches can be operated at fundamental switching frequency.	• Requires isolated input DC levels • Trinary source configuration cannot be employed.
T-type MLI	Proposed in [52-54]	• Simple structure • Requires non-isolated input DC levels	• Requires a mix of unidirectional and bidirectional switches, • Equal load sharing is not possible, asymmetric source configuration is not possible • Highest voltage rated switches cannot be operated at fundamental switching frequency
SSPS-MLI	Proposed in [55,56]	• Input DC sources can be combined in both series and parallel • Equal load sharing is possible amongst input DC sources • Binary source configuration can be employed	• Highest voltage rated switches cannot be operated at fundamental switching frequency • Trinary source configuration cannot be employed
SCSS-MLI	Proposed in [57,58]	• Simple structure • Highest voltage rated switches can be operated at fundamental switching frequency	• Symmetric source configuration is mandatory • Power switches are differently voltage-rated • Equal load sharing is not possible
CBSC-MLI	Proposed in [59]	• Non-isolated input DC levels are required • All switches are bidirectional • Only two switches conduct simultaneously to synthesize a given voltage level	• Equal load sharing is not possible • Asymmetry is not possible, • Switches are differently voltage rated
PUC Topology	Proposed in [60-64]	• Simple structure • Low losses	• Sources need to be mandatorily asymmetric • Complex control • Isolated input DC levels are required
MLM-MLI	Proposed in [65]	• Requires non-isolated DC sources • Simple structure • Highest voltage rated switches can be operated at fundamental frequency	• Requires a mix of unidirectional and bidirectional switches • Equal load sharing is not possible • Asymmetric source configuration not possible
RV Topology	Proposed in [66,67]	• Requires non-isolated DC sources • Single DC link feeds all the three phases • Highest voltage rated switches can be operated at fundamental switching frequency	• Equal load sharing is not possible • Asymmetric source configuration is not possible
2SELG-MLI	Proposed in [68]	• Requires non-isolated input DC levels • Low conduction losses	• Equal load sharing is not possible • asymmetric sources cannot be employed • Highest voltage rated switches cannot be operated at fundamental frequency

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TABLE XII
COMPARISON OF THREE-PHASE MULTILEVEL INVERTERS ('CLASSICAL TOPOLOGIES' AND 'REDUCED DEVICE COUNT' TOPOLOGIES)
(n_{levels} = NUMBER OF LEVELS IN PHASE VOLTAGE)

Topology	Literature	Number of Unidirectional Switches*	Number of Bidirectional Switches**	Total Blocking Voltage Requirement [p.u.]
NPC-MLI	Proposed in [22]	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
FC-MLI	Proposed in [23, 24]	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
CHB-MLI	Proposed in [20]	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
MLDCL-MLI	Proposed in [50,51]	$3(n_{levels}+3)$	0	$9[(n_{levels}-1)]$
T-Type Inverter	Proposed in [52-54]	12	$3(n_{levels}-1)$	$3\,[2(n_{levels}-1)+\sum_{k=1}^{(n_{levels}-3)/4}(n_{levels}-(2k+1))]$, when number of sources is odd. $3\,[\frac{9(n_{levels}-1)}{4}+\sum_{k=1}^{(n_{levels}-5)/4}(n_{levels}-(2k+1))]$, when number of sources is even.
SSPS-MLI	Proposed in [55,56]	$\frac{3\,(3n_{levels}-1)}{2}$	0	$\frac{3[(7n_{levels}-13)]}{2}$
SCSS-MLI	Proposed in [57,58]	$3(n_{levels}+3)$	0	$3[(3n_{levels}-2)+\sum_{k=2}^{(n_{levels}-3)/2}k\ ]$
CBSC-MLI	Proposed in [59]	0	$3(n_{levels}+1)$	$3[\frac{(n_{levels}+1)(3n_{levels}-1)}{8}]$, when number of sources is odd. $3[\frac{(n_{levels}-1)(3n_{levels}+5)}{8}]$, When number of sources is even.
MLM-MLI	Proposed in [65]	12	$\frac{3\,(n_{levels}+1)}{2}$	$3[3(n_{levels}-1)+\sum_{k=1}^{(n_{levels}-3)/4}\{n_{levels}-(2k+1)\}]$, when number of sources is odd. $3[\frac{13(n_{levels}-1)}{4}+\sum_{k=1}^{(n_{levels}-5)/4}\{n_{levels}-(2k+1)\}]$, when number of sources is even.
RV Topology	Proposed in [66,67]	$3(n_{levels}+3)$	0	$9(n_{levels}-1)$
2SELG-MLI	Proposed in [68]	24	$\frac{3\,(n_{levels}-7)}{2}$	V_o+4n ; $n=\frac{(n_{levels}-1)}{2}$, where, $V_o=\begin{cases}\frac{3n^2+8n+5}{5}\ when\ n\ is\ odd\ and\ \frac{n-1}{2}\ is\ even\\ \frac{3n^2+8n+5}{5}\ when\ n\ is\ odd\ and\ \frac{n-1}{2}\ is\ odd\\ \frac{3n^2+8n+1}{5}\ when\ n\ is\ even\ and\ \frac{n}{2}\ is\ odd\\ \frac{3n^2+8n}{5}\ when\ n\ is\ even\ and\ \frac{n}{2}\ is\ even\end{cases}$

*Bidirectional-conducting-unidirectional-blocking **Bidirectional-conducting-bidirectional-blocking

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