Instrumentation Lab, Physics 111A
Lab 10, ADC and DAC

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Signature Card

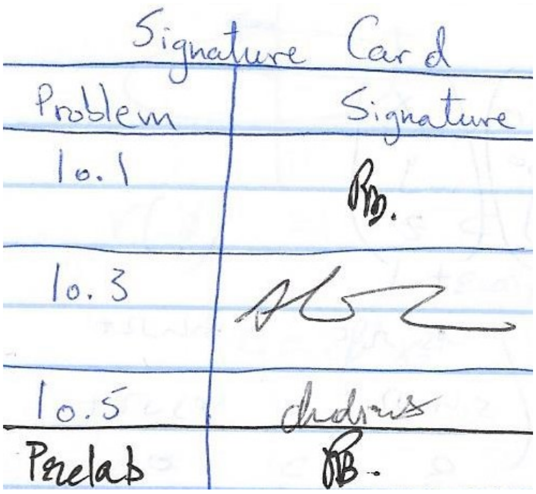


Figure 1: Pre-lab and Problems 10.1, 10.3, 10.5

Problems

Problem 10.1 - Aliasing and Sample Rate

Refer to signature card, figure 1.

Problem 10.2 - Digital to Analog Conversion

We built the scaled resistor DAC with 32 kΩ, 16 kΩ, 8 kΩ, 4 kΩ and 2 kΩ resistors that were matched to within $\frac{1}{32}$.

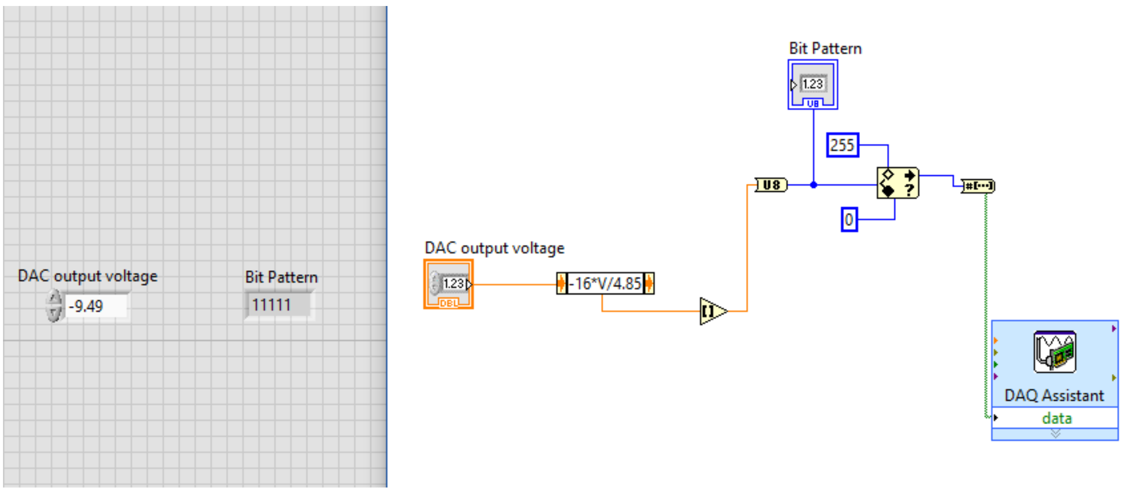


Figure 2: DAC.vi

We built the program shown above that gave us the max output at 9.49 V. The program takes an input and multiplies this voltage by a scaling factor, then rounds to the nearest integer. Which is then converted to an 8 bit digit and the limits of that digit are set by the *In Range and Coerce* operator.

Problem 10.3

Refer to signature card, figure 1.

Problem 10.4 - Analog to Digital Conversion

For the *CompareTrial.vi* we built a program that takes in a trial voltage, adds a 10 millisecond delay and then the output is compared to the ADC input which sets the state of the comparator. The figures below show the true and false states of the *CompareTrial.vi*.

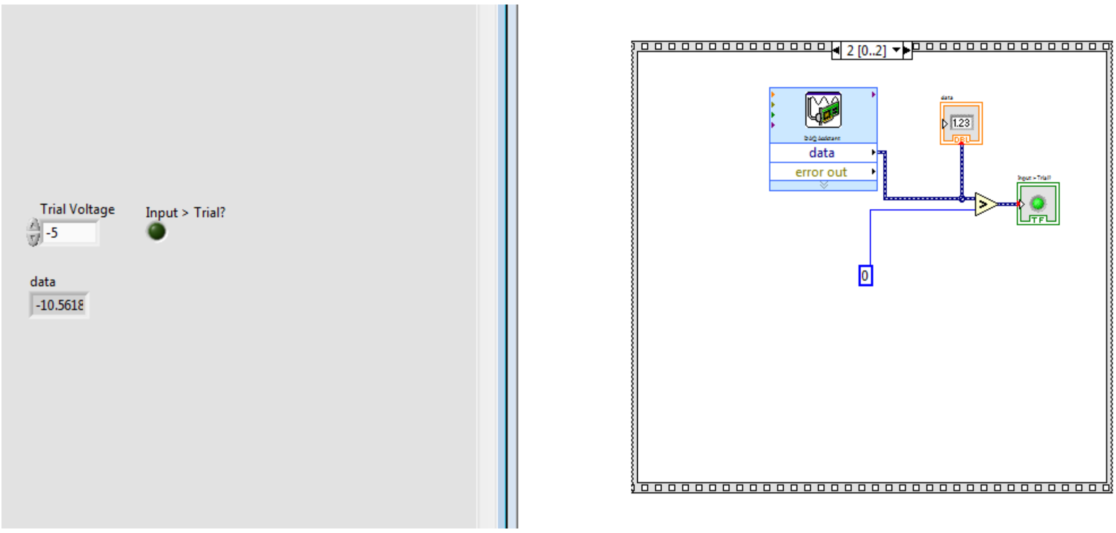


Figure 3: ADC In less than Trial Voltage.vi

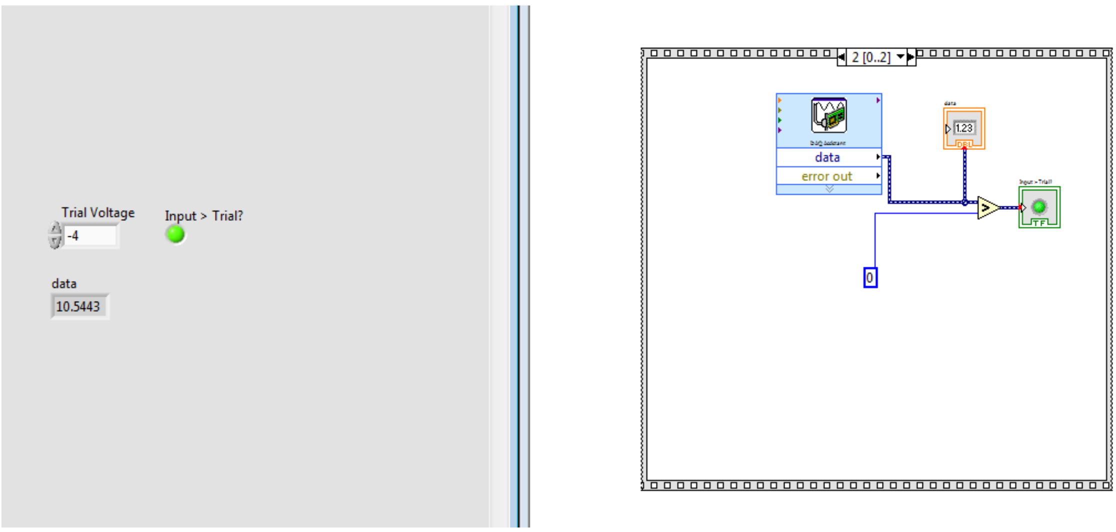


Figure 4: ADC In greater than Trial Voltage.vi

The *CompareTrial.vi* is then used in *ADC.vi* which uses the comparator which, depending on whether the value is true or false, sequentially adds smaller values using shift registers. The guess should converge to the ADC input. We set the constant going into the analogue input and the guess converges to that. As we can see below this works well.

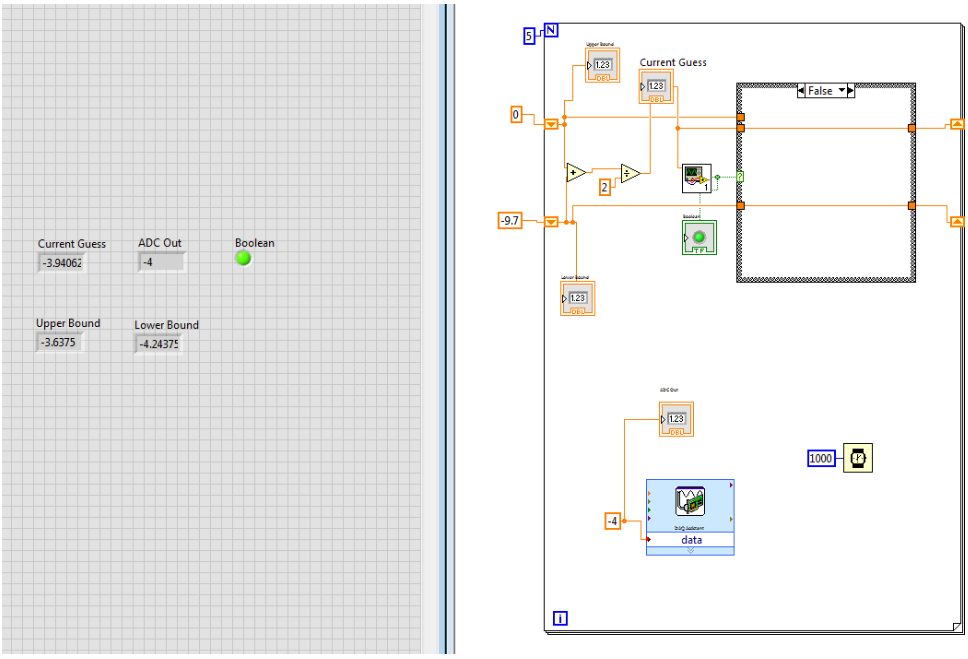


Figure 5: ADC.vi for Trial Voltage -4 V

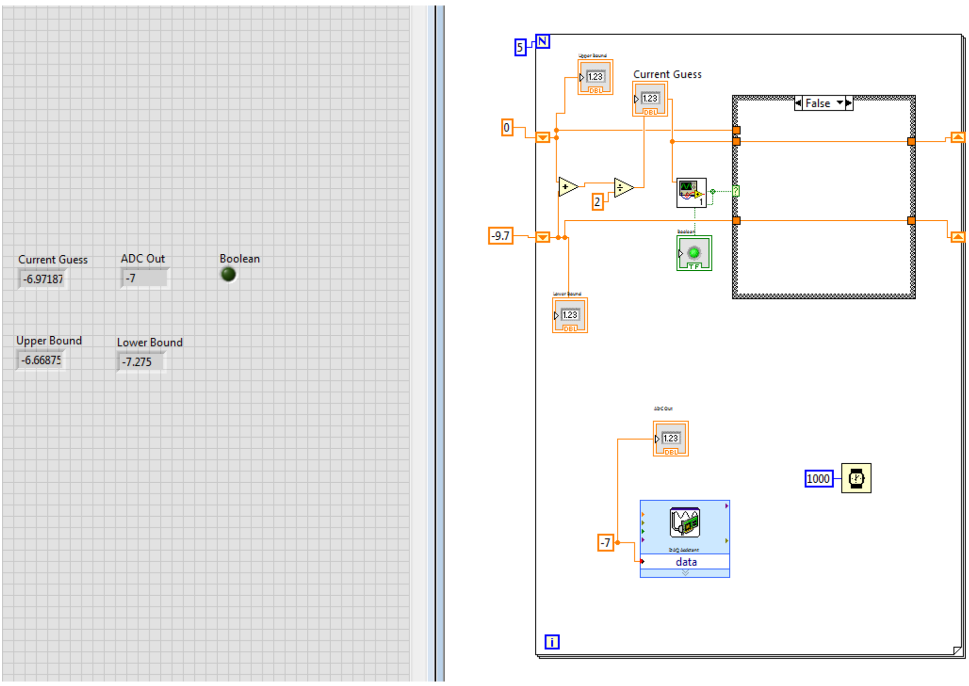


Figure 6: ADC.vi for Trial Voltage -7 V

Problem 10.5

Refer to signature card, figure 1.

Problem 10.6

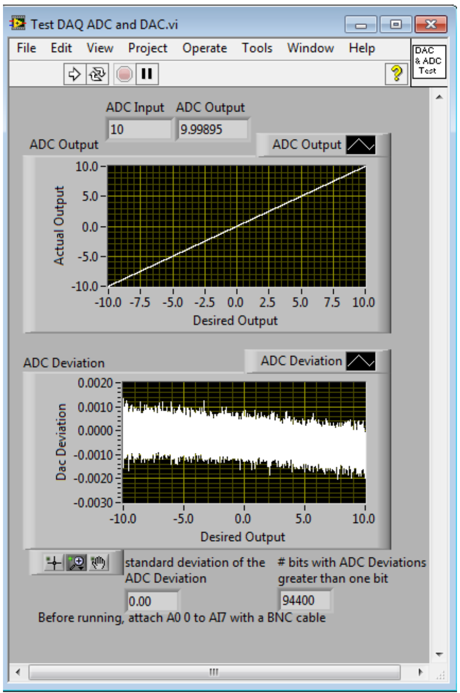


Figure 7: Test DAQ ADC and DAC.vi

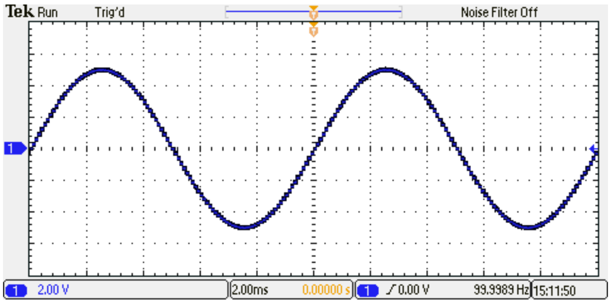
The resolution of the ADC is given by the 1 bit error. This is calculated by dividing the range of the ADC by the number of levels the bits can represent.

$$error_{1\ bit} = \frac{20}{2^{12}}\ \mathrm{V}$$
$$error_{1\ bit} = 0.00488\ \mathrm{V}$$

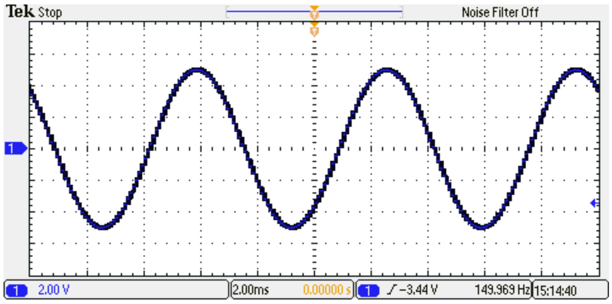
As seen in the image above, none of the errors exceed 0.001 V.

Problem 10.7 - Filtering

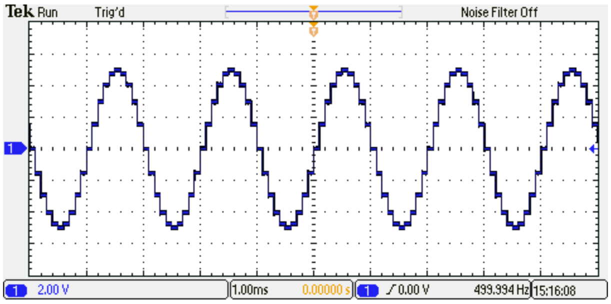
The signal starts to have noticeable steps at 150 Hz and it becomes unrecognizable as a sine wave at 1 kHz. The images below show scope traces for the range of frequencies that we tested.



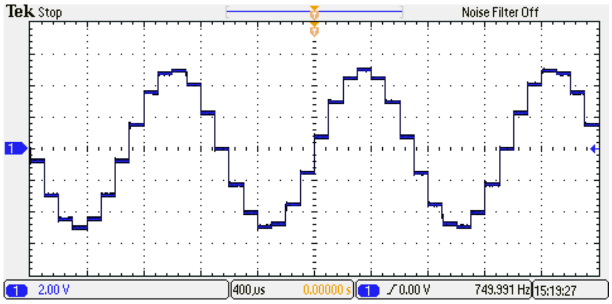
(a) DAQ Drive 100 Hz



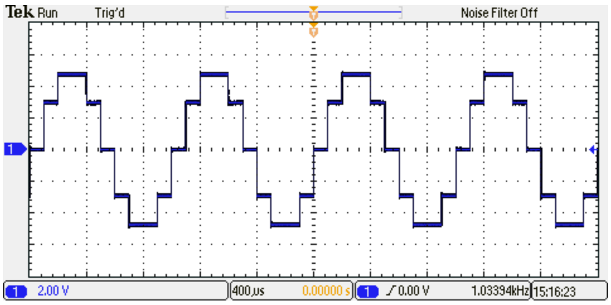
(b) DAQ Drive 150 Hz



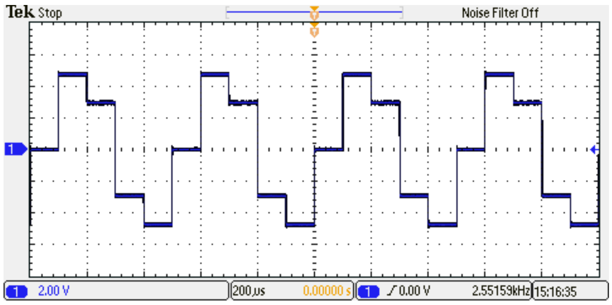
(a) DAQ Drive 500 Hz



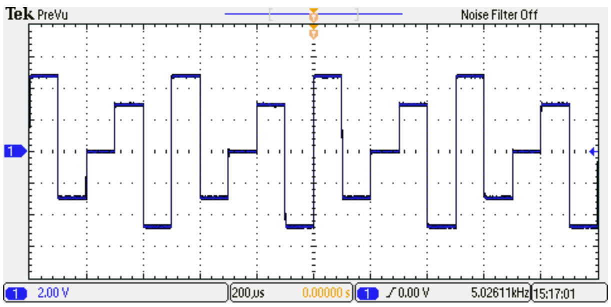
(b) DAQ Drive 750 Hz



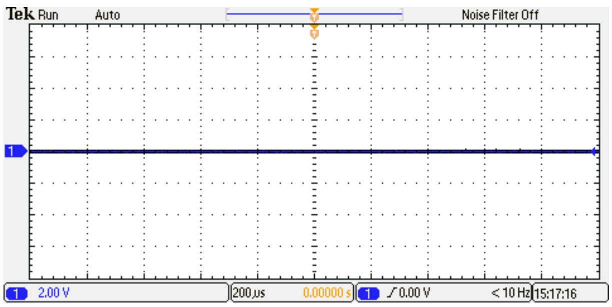
(a) DAQ Drive 1000 Hz



(b) DAQ Drive 2500 Hz

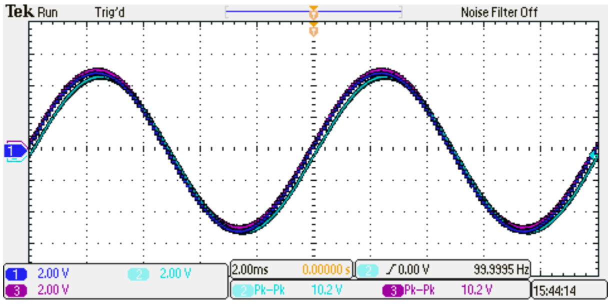


(a) DAQ Drive 4000 Hz

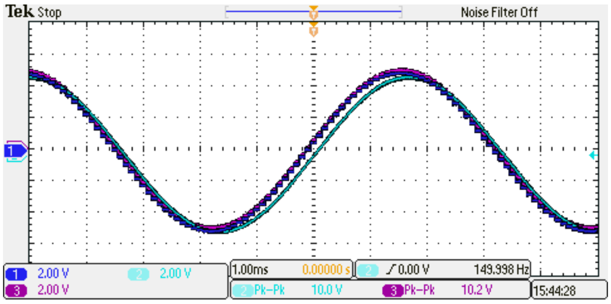


(b) DAQ Drive 5000 Hz

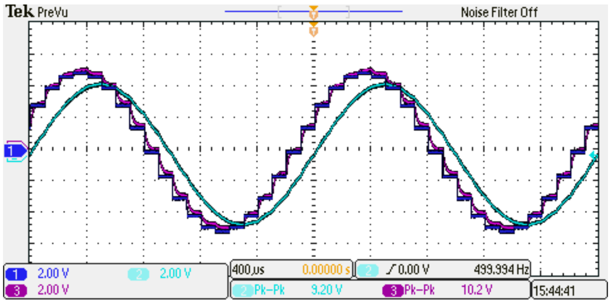
We then built two low pass filters with cut off frequencies at 9929 Hz and 1056 Hz. The traces below show these outputs with the AO-0 output on Channel 1, the 1 kHz filter on channel 2 and the 10 kHz filter on channel 3. The 1 kHz gives a good representation of a sine wave up to 2 kHz however the amplitude drops because of the filtering and the trace is 90 ° out of phase because the filter has a cut-off at about 1 kHz. The 10 kHz filter output has no phase shift and doesn't have lower amplitude but it filters out some of the sampled frequencies.



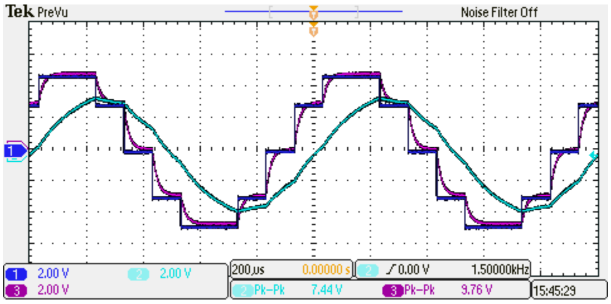
(a) DAQ Drive with filtering 100 Hz



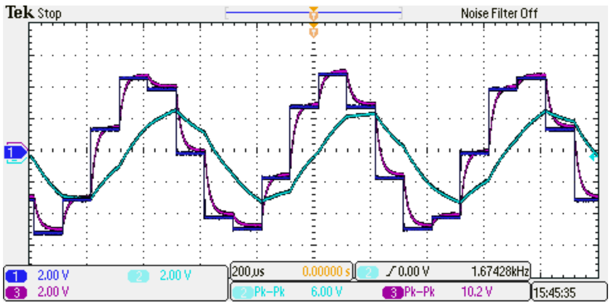
(b) DAQ Drive with filtering 150 Hz



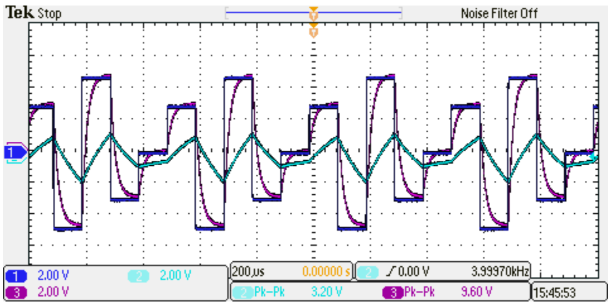
(a) DAQ Drive with filtering 500 Hz



(b) DAQ Drive with filtering 1500 Hz



(a) DAQ Drive with filtering 2000 Hz



(b) DAQ Drive with filtering 4000 Hz