Instrumentation Lab, Physics 111A

Lab 5, JFET Circuits II

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Signature Card

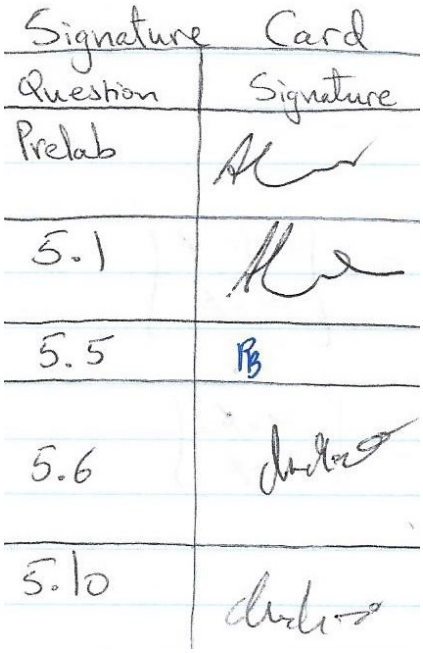


Figure 1: Pre-lab and Problems 5.1, 5.5, 5.6, 5.10

Problem 5.1 - Common Source JFET Amplifier

Refer to signature card, figure 1.

Problem 5.2 - Increased Gain Common Source JFET Amplifier-Large Drain Resistor

Replacing the 1.8 kΩ resistor with an 18.02 kΩ in the circuit from Problem 5.1, our source resistor was 335.8 Ω, we find as expected that the gain drops significantly. We tried a range of voltages at a fixed frequency of 100 kHz, battery voltage of 26.32 V and found the same result.

V_{in}/ V	V_{out}/ V	V_{DS}/ V	Gain
0.0968	0.00152	0.0649	0.0537
1.50V	0.0592	0.0673	0.0394
2.02V	0.0888	0.0692	0.0439

Table 1: V_{in}, V_{out} and V_{DS} for JFET Amplifier, large R_s

Since the 18 kΩ resistor has a large voltage drop across it, the JFET Drain Source voltage is small as is shown in the table above. This means the current source is no longer stiff and we are in the linear regime of the JFET which gives us a Gain close to 0.

Problem 5.3 - Increased Gain Common Source JFET Amplifier-Small Source Resistor

For the circuit we used a 99.0 pF capacitor, $R_s = 165\ \Omega$, $R_d = 1.77\ \text{k}\Omega$ with a driving frequency of 100 kHz.

V_{in}/ V	V_{out}/ V	Gain
0.4	2.48	6.20
0.602	3.76	6.24
0.806	4.96	6.15
1	6.24	6.24
1.21	7.36	6.08
1.51	8.88	5.88

Table 2: V_{in}, V_{out} for JFET Amplifier, small R_s

The gain we found in Problem 5.1 was closer to 4 so we have an increased gain with this circuit.
We found that the signal started distorting around 1.55 V; the figure below shows the distortion for an input signal of 2 V.

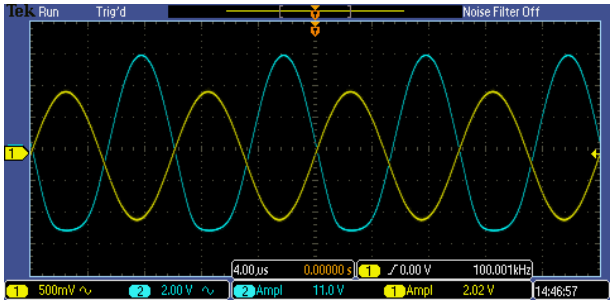


Figure 2: Distorted signal

After we spray the JFET with the circuit cooler we get the following values;

V_{in}/ V	V_{out}/ V	Gain
0.392	2.72	6.94
0.602	4.08	6.78
0.8	5.2	6.50
1	6.44	6.44
1.21	7.44	6.15
1.51	8.88	5.88

Table 3: V_{in}, V_{out} for JFET Amplifier, small R_s, cooled

Cooling the JFET makes the gain change by about 17%.
We found for the four different JFETs;

JFET	V_{in}/ V	V_{out}/ V	Gain
1	0.784	5.12	6.5
2	0.8	5.12	6.4
3	0.8	5.04	6.3
4	0.8	5.36	6.7

Table 4: Measured gain for varied JFETs

The gain for this circuit is larger than the previous circuit because we used a lower source resistor and for simplicity Gain can be approximated as $\frac{R_D}{R_S}$ thus a smaller source resistor gives a larger gain.

Problem 5.4 - Increased Gain Common Source JFET Amplifier-Source Resistor Bypass

We used a 0.97 µF capacitor, and a 1.5 V driving amplitude.

Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain	Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain
5	0.864	3.44	3.98	75	1.5	6.08	4.05
10	1.21	4.96	4.10	100	1.5	6.08	4.05
15	1.35	5.44	4.03	500	1.5	9.4	6.27
20	1.42	5.6	3.94	750	1.5	10.2	6.80
25	1.45	5.76	3.97	1k	1.5	12.2	8.13
30	1.46	5.84	4	2k	1.5	17.3	11.53
35	1.48	5.92	4	5k	1.5	20.6	13.73
40	1.49	5.92	3.97	8k	1.5	21	14
50	1.49	5.92	3.97	10k	1.5	21.4	14.27

Table 5: Measured gain for varied JFETs

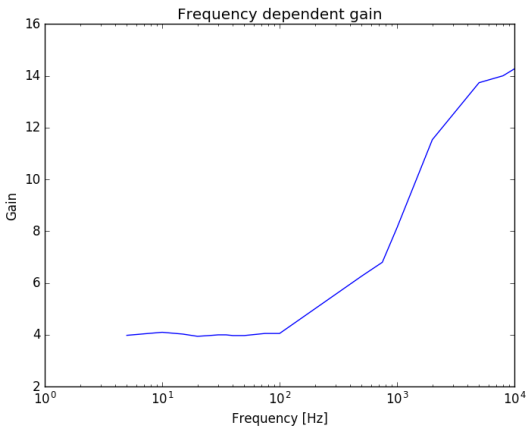


Figure 3: Gain vs Frequency for JFET amplified, source resistance bypass

The capacitor increased the gain because it changes the source resistance which determines the gain; when the frequency increases, the denominator increases which causes the impedance to decrease. Eventually the denominator becomes much bigger than the numerator and the impedance becomes essentially 0 giving high gain as we observed.

$$\frac{1}{Z_{Tot}} = \frac{1}{330\ \Omega} + j\omega C$$
$$Z_{Tot} = \frac{330\ \Omega}{1 + 330\ \Omega j\omega C}$$

For higher frequency gain, we can use equation 1 in the lab write-up, using the high frequency impedance to be about 0 and the fact that most JFETs have an internal resistance of about 200 Ω*;

$$G = \frac{R_D}{R_S + r_s}$$
$$G = \frac{R_D}{r_s}$$
$$r_s = 200\ \Omega$$
$$G = \frac{1800\ \Omega}{200\ \Omega}$$
$$G = 9.0$$

Which is close to what we get from our measurements.
*For lab 4, we had to switch our JFETs in the last problem because our JFET was faulty and we could not find a good match. Therefore the r_s data we found for our JFET in Lab 4 is not applicable here.

Problem 5.5 - Differential Amplifier

Refer to signature card, figure 1.

Problem 5.6 - Improved Differential Amplifier

Refer to signature card, figure 1.

Problem 5.7 - JFET Attenuator

We varied the resistance with the potentiometer to see no attenuation, maximum attenuation and a point which gave an output half as large as the input.
The circuit gave a good output of triangle waves which tells us that it is a good linear circuit.

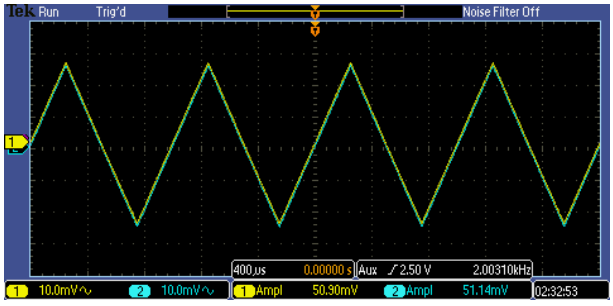


Figure 4: No attenuation

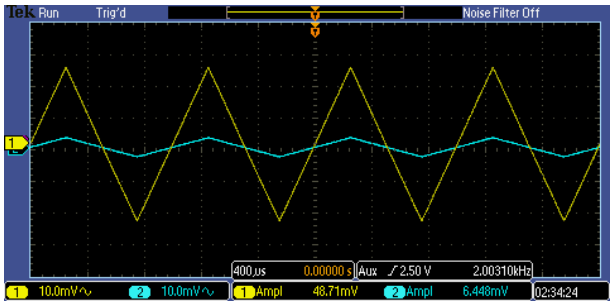


Figure 5: Maximum attenuation

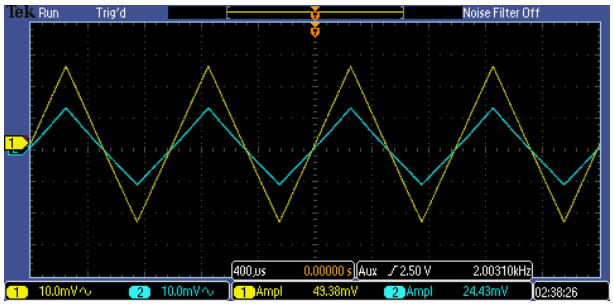


Figure 6: Output signal half as large as the input signal

The output started distorting around $V_{in} = 230$ mV which gave $V_{out} = 118$ mV around where the circuit stopped being linear.

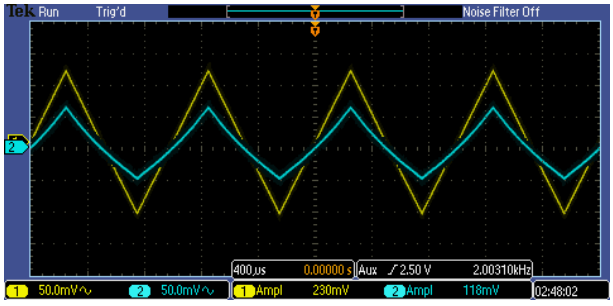


Figure 7: Distortion of output signal from attenuator

Problem 5.8 Linearized JFET Attenuator

We found that the maximum undistorted input to be about 420 mV. This amplitude is about twice the maximum undistorted signal amplitude from Problem 5.7.

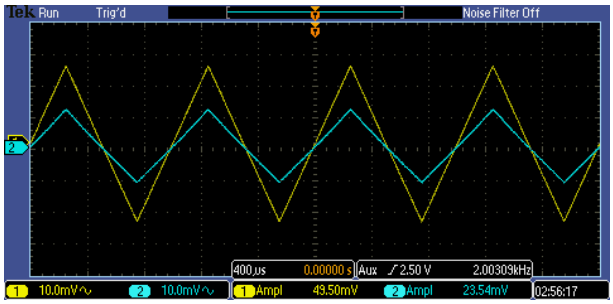


Figure 8: Output signal half as large as the input signal

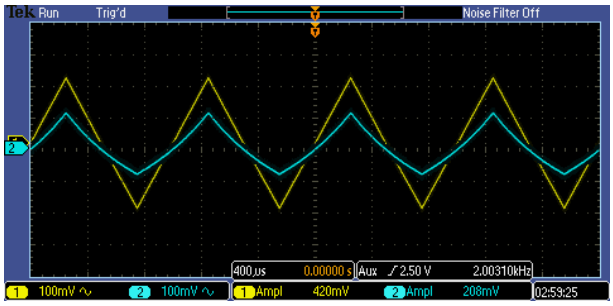


Figure 9: Distortion of output signal from attenuator

The maximum possible attenuation we got was G=0.039 from V_{in} = 96.2 mV and V_{out} = 3.72 mV. Thus to find R_{DS} we can use the voltage divider equation;

$$\frac{V_{out}}{V_{in}} = \frac{R_{DS}}{1\ \text{k}\Omega + R_{DS}}$$

$$R_{DS} = 40.22\ \Omega$$

Problem 5.9 - JFET Modulator

The scope traces for the modulated waves we found are shown in the figures below;

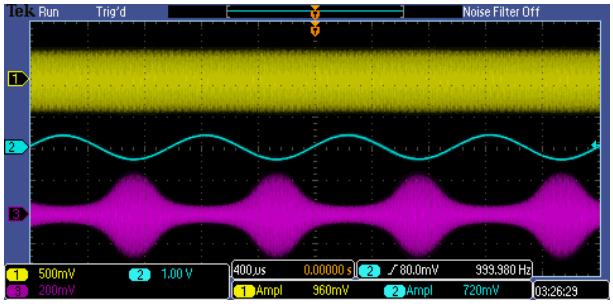


Figure 10: 1 MHz Modulated carrier wave

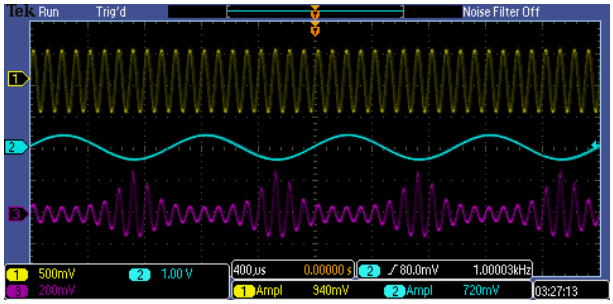


Figure 11: 10 kHz modulated carrier wave

Problem 5.10 - JFET AM Transmitter

Refer to signature card, figure 1.

Problem 5.11 - Surprise Circuit

This circuit is called a Relaxation Oscillator (Professor Fajans told us). We say the following traces at V_{out}, the gate of the left JFET and the gate of the right JFET;

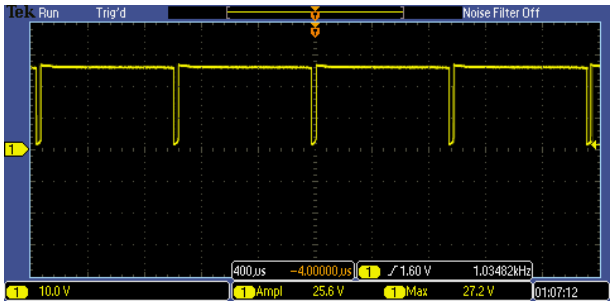


Figure 12: V_{out}

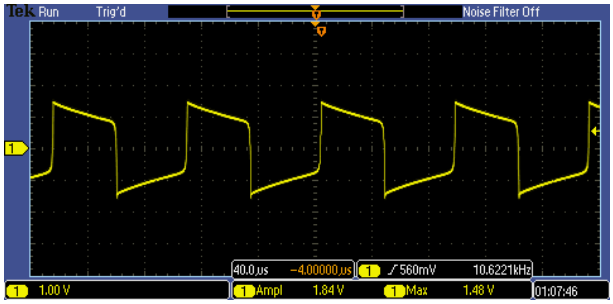


Figure 13: Left JFET gate voltage

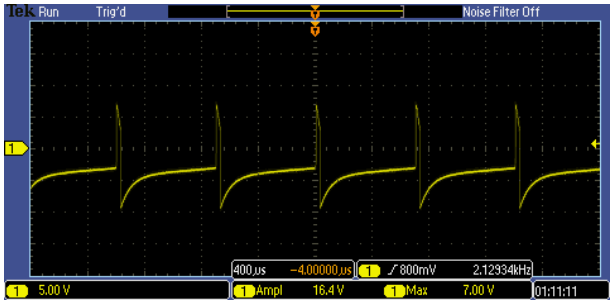


Figure 14: Right JFET gate voltage

We considered the circuit from left to right starting at t=0 and making some simplifications to understand the functioning of the circuit;
Some positive voltage causes current to flow through the JFETs and causes the capacitors to charge, the 5 pF capacitor charges quicker than 0.001 µF capacitor. When the 5 pF is fully charged, there's a potential drop across it, where we have some V+ on the right side and a V- on the left side. This makes the left side JFET to become negatively biased and it cuts off the current below about −3 V, the JFET shuts down and the 0.001 µF capacitor starts to discharge and V_{gate} increases again, current flows and the process continues.
We see pulses on V_{out} because of the difference in the charging time of the capacitors. Calculate the time constant using R and C from the circuit

Problem 5.12 - Phase Splitter

We designed the modified follower circuit below and got the expected 180 ° phase shift with the voltage split in two equal parts. We found that having the resistors at equal value made the output amplitudes be equal, so we used two 4.7 kΩ resistors. The maximum undistorted amplitude was around 4.5 V.

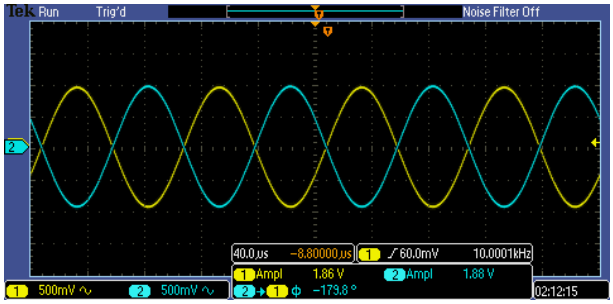


Figure 15: Scope trace for phase splitter

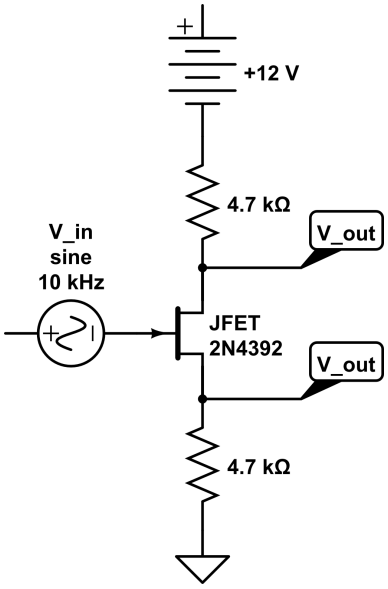


Figure 16: Phase splitter circuit

Problem 5.13 - High Gain Amplifier

We built the high gain amplifier using $R_2 = 335\ \Omega$ to match the $R = 330\ \Omega$ resistor in the upper part of the circuit.
The table below shows our measured values for the gain spanning 100 Hz and 1 MHz. These are plotted in figure 17.
The approximate maximum gain frequency was 5 kHz. We found the 90% range to be between 1.6 kHz and 12 kHz.

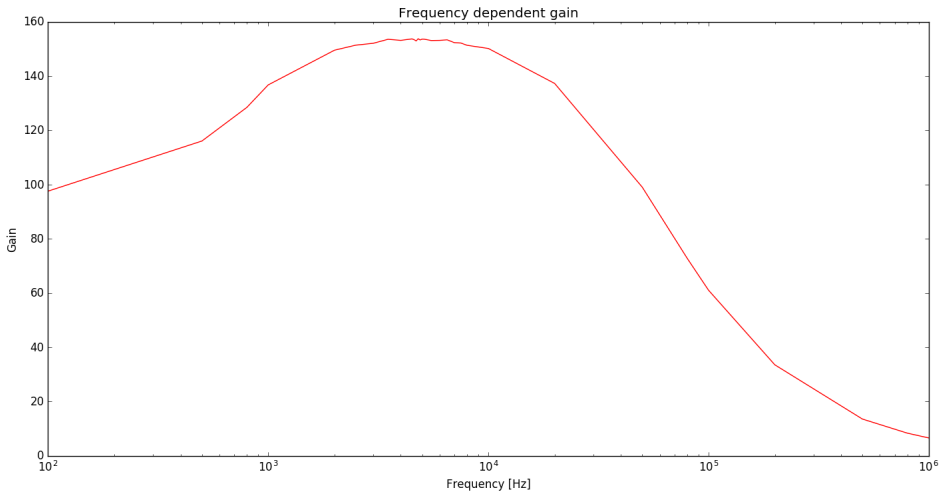


Figure 17: Frequency vs Gain for High gain amp, no R_1

Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain	Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain
100	0.0204	1.99	97.55	5.5k	0.0204	3.123	153.1
500	0.0204	2.367	116.0	6k	0.0204	3.124	153.1
800	0.0204	2.62	128.4	6.5k	0.0204	3.128	153.3
1k	0.0204	2.789	136.7	7k	0.0204	3.107	152.3
2k	0.0204	3.05	149.5	7.5k	0.0204	3.104	152.2
2.5k	0.0204	3.088	151.4	8k	0.0204	3.087	151.3
3k	0.0204	3.102	152.1	10k	0.0204	3.063	150.1
3.5k	0.0204	3.132	153.5	20k	0.0204	2.8	137.3
4k	0.0204	3.124	153.1	50k	0.0204	2.02	99.02
4.5k	0.0204	3.135	153.7	80k	0.0204	1.485	72.79
4.6k	0.0204	3.129	153.4	100k	0.0204	1.245	61.03
4.7k	0.0204	3.12	152.9	200k	0.0204	0.684	33.53
4.8k	0.0204	3.136	153.7	500k	0.0204	0.276	13.53
4.9k	0.0204	3.127	153.3	800k	0.0204	0.17	8.333
5k	0.0204	3.135	153.6	1M	0.0204	0.134	6.569
5.1k	0.0204	3.133	153.5				

Table 6: Measured gain for high gain JFET Amplifier

We then set the frequency to be 5 kHz where we get the maximum gain and switched out the lower JFET with random JFETs getting the following results that tell us that the gain seems to be dependent of the JFET we use;

JFET	V_{in}/ V	V_{out}/ V	Gain
1	0.0204	3.772	184.9
2	0.0204	3.024	148.2
3	0.0204	2.768	135.75
4	0.0204	2.8	137.3
5	0.0204	3.285	161.0
6	0.0204	3.372	165.3

Table 7: Measured gain for varied JFETs

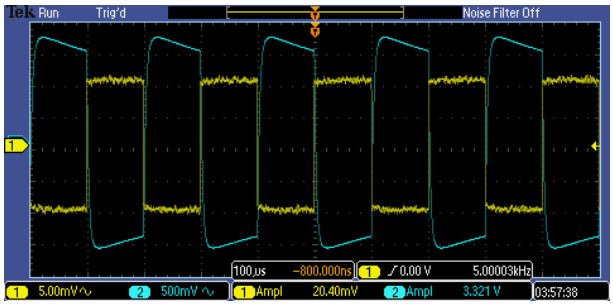


Figure 18: Scope trace for square wave amplifier

The square wave output was a rather poor representation of a square wave. The gain before cooling was measured to be 153.3 with $V_{out} = 3.128$ V and the gain after cooling was 166.1 with $V_{out} = 3.390$ V. We noted an 8% increase in the gain.
In order to find R_1, we noted that, in order to get a gain of about 20, we would want R_1 to be 20 times as large as the 1 kΩ resistor connected to the voltage input. We tried a few resistors in this range and found that 27 kΩ gave the best results. The values for gain and the frequency gain plot are shown below.
We found the 90% frequency range to be between 650 Hz and 150 kHz.

Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain	Frequency/ Hz	V_{in}/ V	V_{out}/ V	Gain
100	0.0196	0.3202	16.34	6.5k	0.0196	0.42	21.43
500	0.0196	0.362	18.47	7k	0.0196	0.42	21.43
800	0.0196	0.388	19.8	7.5k	0.0196	0.42	21.43
1k	0.0196	0.396	20.2	8k	0.0196	0.42	21.43
2k	0.0196	0.416	21.22	10k	0.0196	0.418	21.33
2.5k	0.0196	0.42	21.43	20k	0.0196	0.412	21.02
3k	0.0196	0.42	21.43	50k	0.0196	0.406	20.71
3.5k	0.0196	0.42	21.43	80k	0.0196	0.4	20.41
4k	0.0196	0.42	21.43	100k	0.0196	0.392	20.00
4.5k	0.0196	0.42	21.43	200k	0.0196	0.352	17.96
5k	0.0196	0.422	21.53	500k	0.0196	0.224	11.43
5.5k	0.0196	0.42	21.43	800k	0.0196	0.152	7.755
6k	0.0196	0.42	21.43	1M	0.0196	0.122	6.224

Table 8: Measured gain for high gain JFET Amplifier

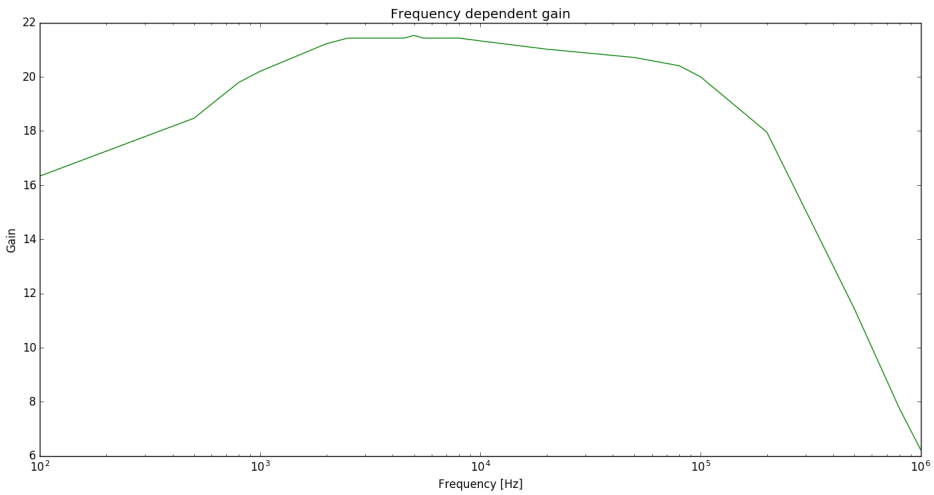


Figure 19: Frequency vs Gain for High gain amp, R_1 included

Switching out the JFETs in the circuit with R_1 included we got a much lower variation in the gain, the variation is within 10%.

JFET	V_{in}/ V	V_{out}/ V	Gain
1	19.6	431	21.99
2	19.6	432	22.04
3	19.6	424	21.63
4	19.6	426	21.73
5	19.6	421	21.48
6	19.6	433	22.093

Table 9: Measured gain for varied JFETs

The square wave output representation with R_1 included is a much better representation than the one without R_1 included.

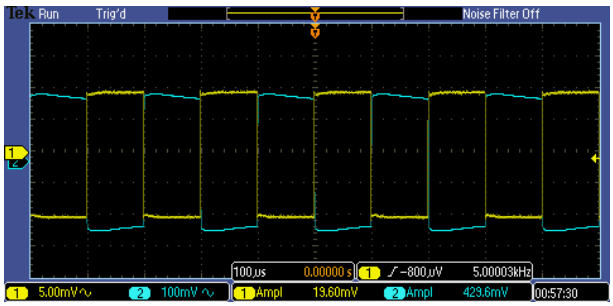


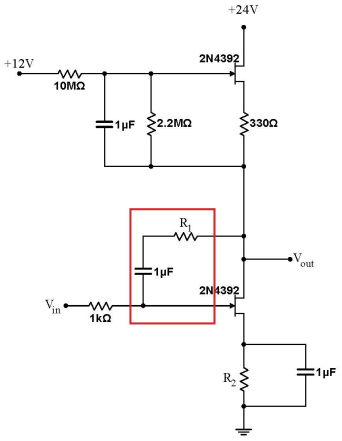
Figure 20: Square wave input and output

Finally, upon cooling we found a gain of 22.07 with V_{out} = 432.5 mV; before cooling we had a gain of 21.45 with V_{out} = 420.5 mV. The difference in gain is only about 3%. From all these results, we know that with the feedback loop, the circuit is much less dependent on temperature and circuit components.

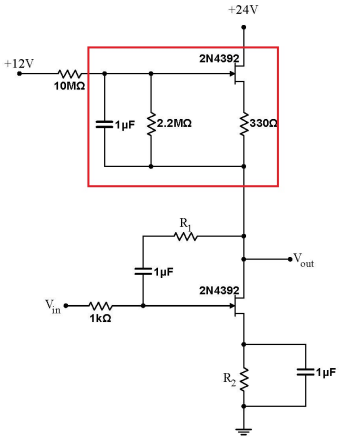
Problem 5.14 - High Gain Amplifier Explanation

1) The loop with R_1 and the 1 µF capacitor form the feedback loop to set the gain. Changing V_{in} causes the gate voltage to change, this in turn changes the current in the lower JFET thus changing V_{out} where the ratio of V_{out} and V_{in} gives us the gain.

2) The upper loop of the circuit with the 1 µF capacitor, the top JFET, the 2.2 MΩ resistor and the 330 Ω resistor acts as a current source for the lower JFET because this acts like a stiff current source that we've seen before in the lab.



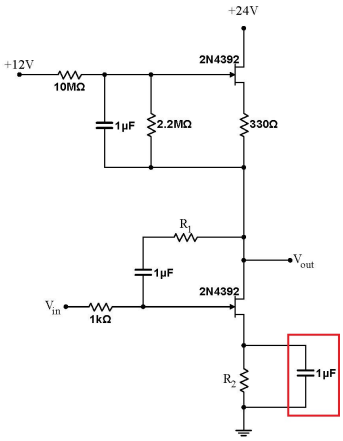
(a) 5.14.1, Sets the gain through feedback



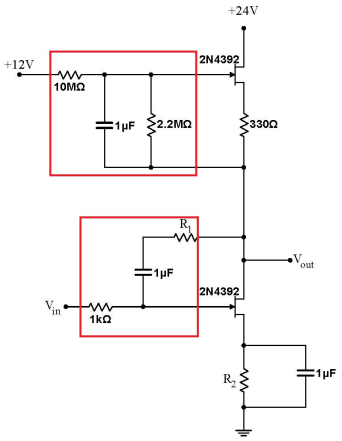
(b) 5.14.2, Acts as a current source

3) The 1 µF capacitor next to the source resistor, R_2, increases the open-loop gain by bypassing the source resistor. This happens because capacitor has low impedance at high frequencies which allows the current to bypass.

4) The combination of resistors and capacitors around each JFET set the respective current through each JFET. They change V_{GS} and changing that controls the current through the JFET.



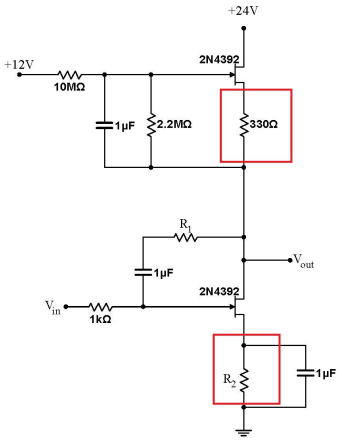
(a) 5.14.3, Increases open loop gain



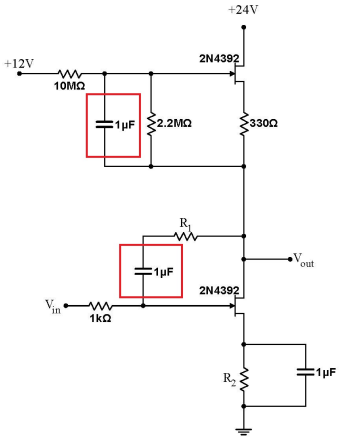
(b) 5.14.4, Sets the current through the JFETs

5) The 330 Ω resistor and R_2 also chosen to be 330 Ω are source resistors, they maintain V_{DS} at 12 V. They have feeback loops to the JFETs and operate at the equilibrium points of the respective JFETs.

6) The 1 µF capacitors connected in series with R_1 and in the loop by the 10 MΩ resistor, provide a bypass for AC signals. A capacitor's impedance is inversely proportional to the frequency of the signal, so the AC signals go through the capacitor rather than through the resistors thus creating a bypass.



(a) 5.14.5, Assures V_{DS} is roughly 12 V



(b) 5.14.6, Increases the stiffness of the current source

Problem 5.15 - Improved Differential Amplifier Gain

Using the circuit values in Problem 5.6 and assuming $r_s = 200\ \Omega$ (explained in problem, we can find the differential gain and common gain but first we need to find an approximate stiffness. I used the values from Lab 4 which gave a stiffness, $Z_{out} = 236\ \text{k}\Omega$ from Problem 4.11. As mentioned before, we had to switch our JFETs so this stiffness will not be true for the JFET we used in Lab 5. However the method of calculating common mode gain remains the same.

$$Gain_{diff} = \frac{R_D}{R_s + r_s} \qquad Gain_{com} = \frac{R_D}{2Z_{out} + R_S + r_s}$$

$$Gain_{diff} = \frac{3.3\ \text{k}\Omega}{100\ \Omega + 200\ \Omega} \qquad Gain_{com} = \frac{3.3\ \text{k}\Omega}{2(236\ \text{k}\Omega) + 100\ \Omega + 200\ \Omega}$$

$$Gain_{diff} = 11 \qquad Gain_{com} = 0.0069$$

Our measured values from Problem 5.6 were as follows, as expected the common mode gain has a much greater error in the measured and calculated values. The large error in differential gain could be attributed to the error in measuring small signals.

$$Gain_{diff} = 5.92 \qquad Gain_{com} = 0.012$$

$$error = 46\% \qquad error = 74\%$$