TEXAS INSTRUMENTS

**SN74LVC2G08**

SCES198N – APRIL 1999 – REVISED DECEMBER 2015

## SN74LVC2G08 Dual 2-Input Positive-AND Gate

### 1 Features

- Available in the Texas Instruments NanoStar™ and NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 4.7 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Maximum of 5.5 V Down to the $V_{CC}$ Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- IP Phones: Wired and Wireless
- Optical Networking: EPON and Video Over Fiber
- Point-to-Point Microwave Backhaul
- Power: Telecom DC/DC Module: Analog
- Power: Telecom DC/DC Module: Digital
- Private Branch Exchange (PBX)
- Telecom Shelter: Power Distribution Unit (PDU)
- Vector Signal Analyzers and Generators
- Wireless Communications Testers
- Wireless Repeaters
- xDSL Modem/DSLAM

### 3 Description

This dual 2-input positive-AND gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC2G08 device performs the Boolean function $Y = A \times B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

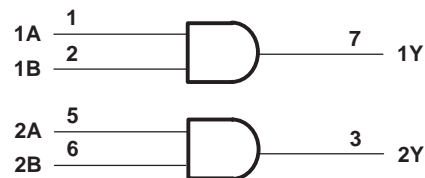NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC2G08DCT | SM8 (8) | 2.95 mm × 2.80 mm |
| SN74LVC2G08DCU | VSSOP (8) | 2.30 mm × 2.00 mm |
| SN74LVC2G08YZP | DSBGA (8) | 1.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)

# Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

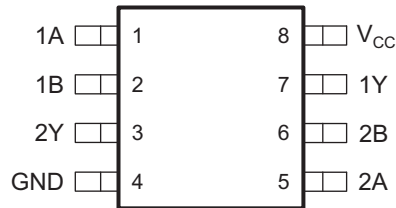**Changes from Revision M (April 2014) to Revision N**                                                                 **Page**

• Added *Pin Configuration and Functions* section, *ESD Ratings* and *Thermal Information* tables, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ................................................................................................................................... 1

Product Folder Links: *SN74LVC2G08*

# 5 Pin Configuration and Functions

**DCT Package**
**8-Pin SM8**
**Top View**

```
        ┌──────────┐
1A  ──┤ 1      8 ├── V_CC
1B  ──┤ 2      7 ├── 1Y
2Y  ──┤ 3      6 ├── 2B
GND ──┤ 4      5 ├── 2A
        └──────────┘
```

**DCU Package**
**8-Pin VSSOP**
**Top View**

```
        ┌──────────┐
1A  ──┤ 1      8 ├── V_CC
1B  ──┤ 2      7 ├── 1Y
2Y  ──┤ 3      6 ├── 2B
GND ──┤ 4      5 ├── 2A
        └──────────┘
```
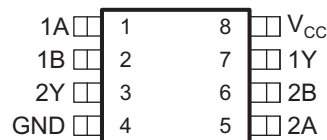
**YZP Package**
**8-Pin DSBGA**
**Bottom View**

```
GND   ○4  5○   2A
2Y    ○3  6○   2B
1B    ○2  7○   1Y
1A    ○1  8○   V_CC
```

## Pin Functions[1]

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | I | Channel 1 logic input |
| 1B | 2 | I | Channel 1 logic input |
| 1Y | 7 | O | Logic level output |
| 2A | 5 | I | Channel 2 logic input |
| 2B | 6 | I | Channel 2 logic input |
| 2Y | 3 | O | Logic level output |
| GND | 4 | — | Ground |
| V_CC | 8 | — | Power Supply |

(1)  See *Mechanical, Packaging, and Orderable Information* for dimensions.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 6.5 | V |
| $V_I$ | Input voltage[2] | | −0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state[2] | | −0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high or low state[2][3] | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | −50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | −50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_j$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *SN74LVC2G08*

## 6.3 Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7 \times V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $0.3 \times V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | | −8 | |
| | | $V_{CC}$ = 3 V | | −16 | |
| | | | | −24 | |
| | | $V_{CC}$ = 4.5 V | | −32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | SN74LVC2G08DCU | −40 | 125 | °C |
| | | SN74LVC2G08DCT | −40 | 125 | |
| | | SN74LVC2G08YZP | −40 | 85 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.4 Thermal Information

| | | SN74LVC2G08 | | | |
|---|---|---|---|---|---|
| **THERMAL METRIC[1]** | | **DCT (SM8)** | **DCU (VSSOP)** | **YZP (DSBGA)** | **UNIT** |
| | | **8 PINS** | **8 PINS** | **8 PINS** | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 220 | 227 | 128 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 108 | 84 | 14 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

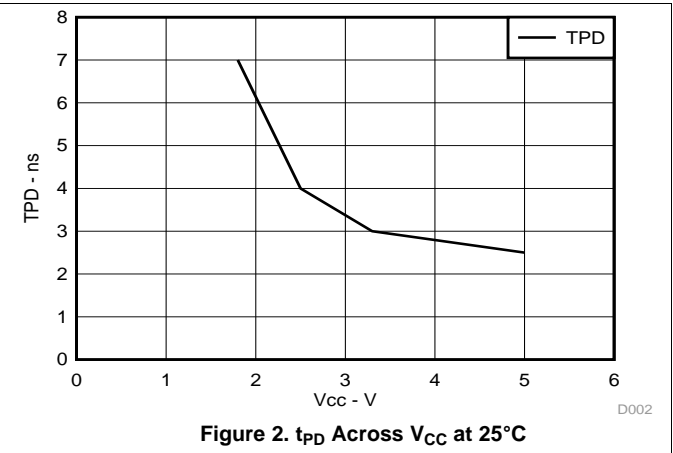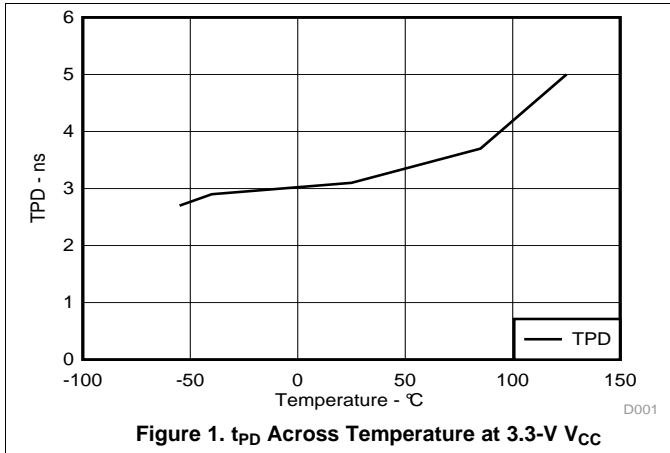over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = −100 µA | 1.65 V to 5.5 V | $V_{CC}$ − 0.1 | | | V |
| | | $I_{OH}$ = −4 mA | 1.65 V | | 1.2 | | |
| | | $I_{OH}$ = −8 mA | 2.3 V | | 1.9 | | |
| | | $I_{OH}$ = −16 mA | 3 V | | 2.4 | | |
| | | $I_{OH}$ = −24 mA | | | 2.3 | | |
| | | $I_{OH}$ = −32 mA | 4.5 V | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | 1.65 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | 2.3 V | | | 0.3 | |
| | | $I_{OL}$ = 16 mA | 3 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | | | 0.55 | |
| | | $I_{OL}$ = 32 mA | 4.5 V | | | 0.55 | |
| $I_I$ | A or B inputs | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | 0 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = 5.5 V or GND, $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | µA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND, $T_A$ = −40°C to 85°C | 3 V to 5.5 V | | | 500 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND, $T_A$ = −40°C to 85°C | 3.3 V | | 5 | | pF |
| $C_{pd}$ | | f = 10 MHz, $T_A$ = −40°C to 85°C | 1.8 V to 3.3V | | 17 | | |
| | | | 5 V | | 20 | | |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | Y | −40°C to 85°C | $V_{CC}$ = 1.8 V ± 0.15 V | 2.6 | 9 | ns |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 5.1 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 4.7 | |
| | | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.8 | |
| | | | −40°C to 125°C | $V_{CC}$ = 1.8 V ± 0.15 V | 2.6 | 9.8 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 5.8 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.3 | |
| | | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4.8 | |

Product Folder Links: *SN74LVC2G08*

## 6.7   Typical Characteristics



**Figure 1. t_PD Across Temperature at 3.3-V V_CC**



**Figure 2. t_PD Across V_CC at 25°C**

# 7 Parameter Measurement Information



**LOAD CIRCUIT**

| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|----------|--------|------|-------|-----------|-------|-------|-----------|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**
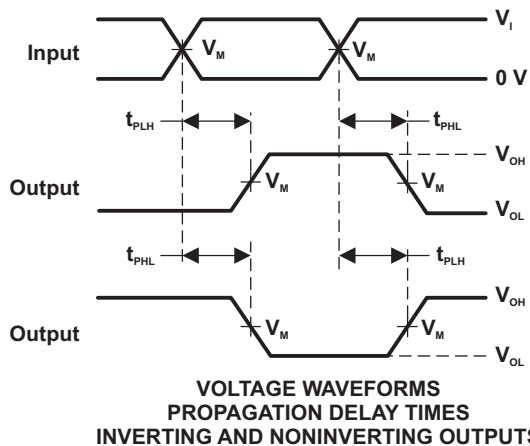
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

Product Folder Links: *SN74LVC2G08*

# 8 Detailed Description

## 8.1 Overview

The SN74LVC1G06 device contains two positive-AND gates with a maximum sink current of 24 mA. A very low tpd of 4.7ns at 3.3V makes the device ideal for high speed applications. Additionally, 5.5V tolerant inputs allow the device to be used as a down translator if needed.

## 8.2 Functional Block Diagram
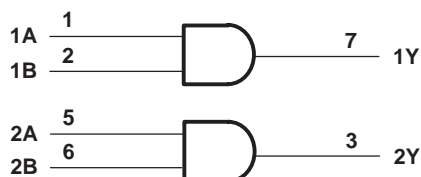


## 8.3 Feature Description

### 8.3.1 Down Voltage Translation

SN74LVC2G08 allows for logic input and output signals up to 5.5 V. While operating at $V_{CC}$ of 3.3 V, the device will still recognize 5.5 V as a valid high input, however, the resulting output will be 3.3 V. This is the same for other voltage levels in the device effectively down translating any input logic level higher than $V_{CC}$ but lower or equal to 5.5 V.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G08.

**Table 1. Function Table**

| INPUTS | | OUTPUT |
| --- | --- | --- |
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

# 9 Application and Implementation

### NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC2G08 is a high-drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application.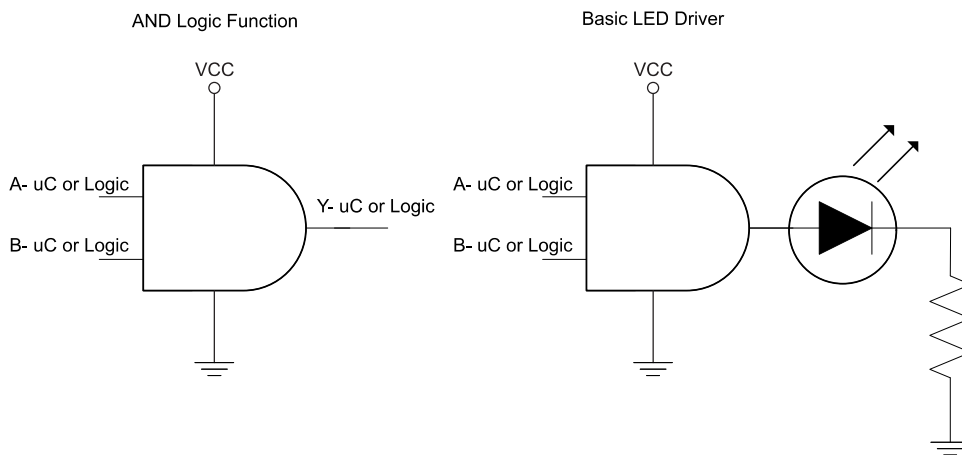 It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to $V_{CC}$.

## 9.2 Typical Application



**Figure 4. Typical Application**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Tak care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ maximum) in the *Recommended Operating Conditions* table at any valid $V_{CC}$.
2. Recommended Output Conditions
   – Load currents must not exceed ($I_O$ maximum) per output and must not exceed total current (continuous current through $V_{CC}$ or GND) for the part. These limits are located in the *Recommended Operating Conditions* table.
   – Outputs must not be pulled above $V_{CC}$ in normal operating conditions.

Product Folder Links: *SN74LVC2G08*

## Typical Application  (continued)

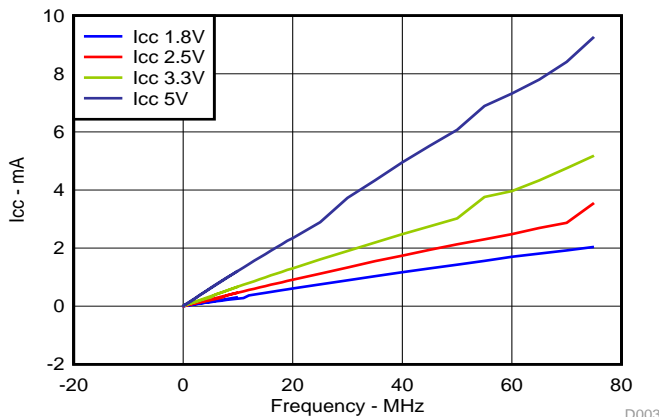### 9.2.3  Application Curves



**Figure 5. I<sub>CC</sub> vs Frequency**

## 10  Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple $V_{CC}$ pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results

## 11  Layout

### 11.1  Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient.
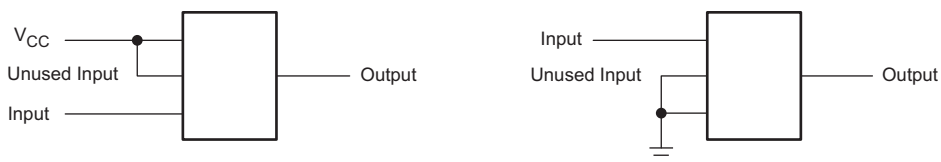
### 11.2  Layout Example



**Figure 6.  Layout Example**

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC2G08DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08 (R ~ Z) | Samples |
| SN74LVC2G08DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08 (R ~ Z) | Samples |
| SN74LVC2G08DCTRG4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08 (R ~ Z) | Samples |
| SN74LVC2G08DCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (08 ~ C08Q ~ C08R) (CR ~ CZ) | Samples |
| SN74LVC2G08DCURE4 | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08R | Samples |
| SN74LVC2G08DCURG4 | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08R | Samples |
| SN74LVC2G08DCUT | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (C08Q ~ C08R) CR | Samples |
| SN74LVC2G08DCUTG4 | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08R | Samples |
| SN74LVC2G08YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (CE7 ~ CEN) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC2G08 :**

● Automotive: SN74LVC2G08-Q1

● Enhanced Product: SN74LVC2G08-EP

NOTE: Qualified Version Definitions:

   ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

   ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC2G08DCTR | SM8 | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 9.0 | 2.05 | 3.3 | 1.0 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCURG4 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCUT | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08DCUTG4 | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G08YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC2G08DCTR | SM8 | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08DCURG4 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08DCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08DCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08DCUTG4 | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G08YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

**DCT (R-PDSO-G8)**                    **PLASTIC SMALL-OUTLINE PACKAGE**



4188781/C 09/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)                                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C,E)

Example Stencil Design
(Note D)

6x0,65

3,40

8x0,25

8x1,55

6x0,65

3,40

Non Solder Mask Defined Pad

0,30

1,60

0,07
All Around

Example
Pad Geometry
(Note C)

Example
Non-solder Mask Opening
(Note E)

4212201/A  10/11

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Publication IPC-7351 is recommended for alternate designs.
        D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers
            should contact their board assembly site for stencil design recommendations.  Refer to IPC-7525.
        E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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B |← E →| A

BALL A1
CORNER

D

0.5 MAX

0.19
0.15

SEATING PLANE

C

⌒ 0.05 C

BALL TYP

0.5 TYP

D

C

SYMM
℄

1.5
TYP

B

0.5
TYP

D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

A

8X ∅ 0.25
        0.21

1          2

⊕ | 0.015Ⓜ | C | A | B

SYMM
℄

4223082/A  07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

8X (∅ 0.23)

(0.5) TYP

(0.5) TYP

1        2

A

B

SYMM
₵

C

D

SYMM
₵

LAND PATTERN EXAMPLE
SCALE:40X

SOLDER MASK
OPENING

0.05 MAX

(∅ 0.23)
METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

(∅ 0.23)
SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A   07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

## YZP0008

(0.5) TYP

8X (☐ 0.25)

(R0.05) TYP

1    2

A

(0.5) TYP

B

SYMM ₵

METAL TYP

C

D

SYMM ₵

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A   07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU (R−PDSO−G8)          PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)

0,50

0,25
0,17

⊕ |0,08 Ⓜ|

8

5

2,40
2,20

3,20
3,00

PIN 1
INDEX AREA

1

4

2,10
1,90

0,13 NOM

Gage Plane

0°−6°

0,12

0,35
0,20

0,90
0,60

0,10
0,00

Seating Plane

⌒ |0,10|

4200503/F 07/05

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−187 variation CA.

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DCU (S−PDSO−G8)          PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout
(Note C,E)

Example Stencil Design
(Note D)

6x 0,5

8x 0,25          6x 0,5

8x 0,75

3,1

3,1

0,3

Example
Solder Mask Opening

0,8

Pad Geometry

0,05

All Around

4210064/C 04/12

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Publication IPC−7351 is recommended for alternate designs.
D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations.  Refer to IPC−7525 for other stencil recommendations.
E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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# IMPORTANT NOTICE