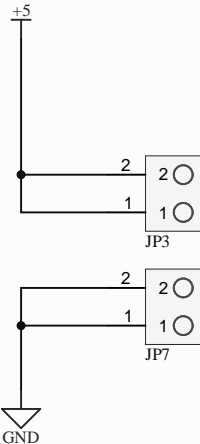
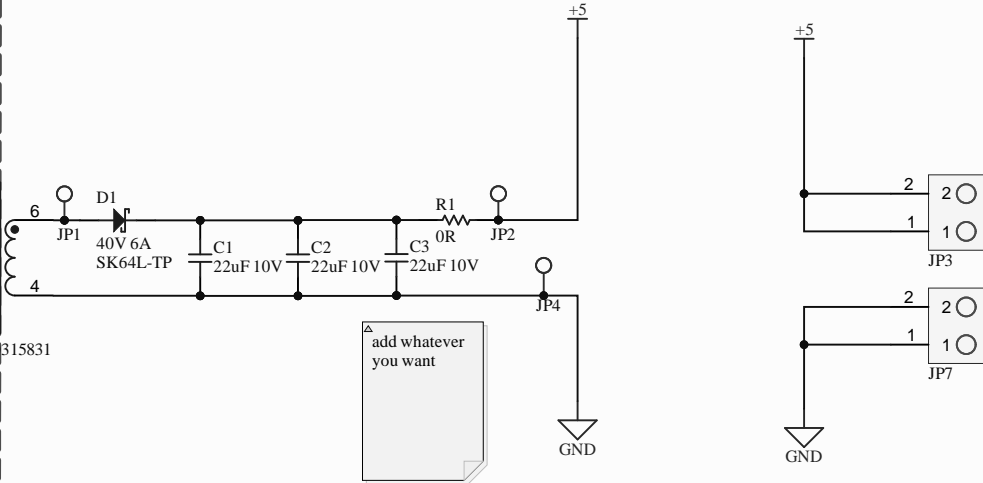
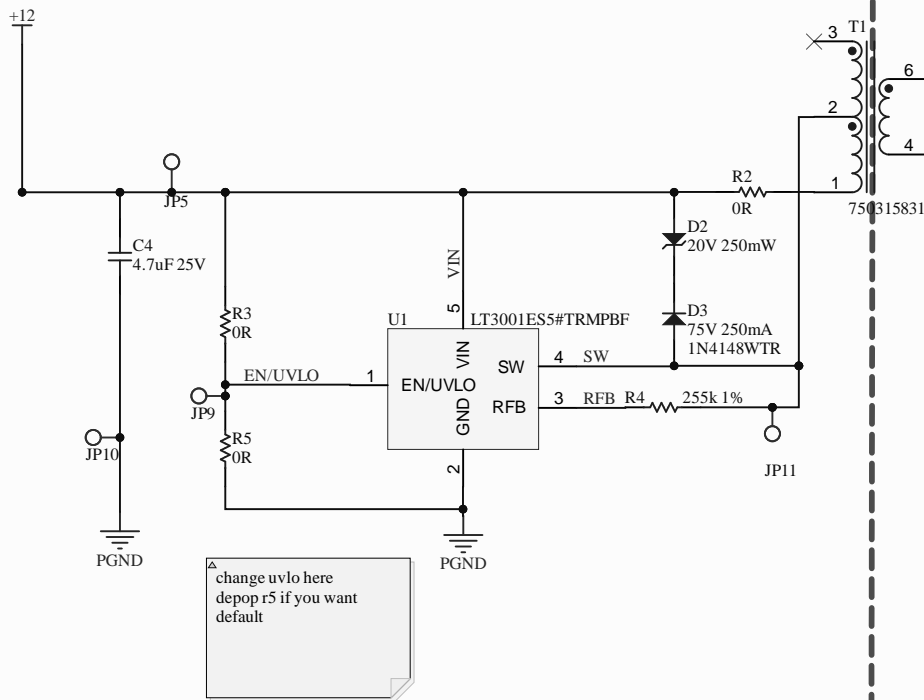
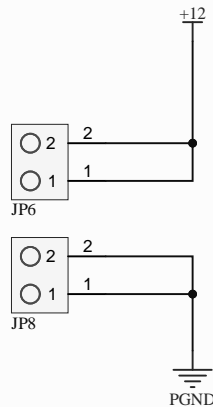


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# LT3001 Eval Board - root



|                     |  |      |  |                   |  |                    |  |                          |  |
|---------------------|--|------|--|-------------------|--|--------------------|--|--------------------------|--|
| APPROVALS           |  | DATE |  | PROJECT           |  | EV_LT3001          |  | Altium                   |  |
| ENG: Justin         |  |      |  | PROJECT REVISION: |  | DOCUMENT REVISION: |  | DESIGN ITEM:             |  |
| DSN: *              |  |      |  | CHK: *            |  | TITLE              |  | LT3001 Eval Board - root |  |
| REFERENCE DOCUMENTS |  |      |  | BOM:              |  | SIZE               |  | CAGE CODE                |  |
| ASSY DWG:           |  |      |  | FAB DWG:          |  | SCALE:             |  | FILE NAME                |  |
| PCB DWG:            |  |      |  |                   |  |                    |  | root.SchDoc              |  |
|                     |  |      |  |                   |  |                    |  | SHEET 1 OF 1             |  |