Design Rules Verification Report

Filename : C:\Users\jtsang451\Documents\TeamPhantom\PowerDistribution\HV_Board_Rev3\

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (IsStitchingVia and InNet('HV_GND')),((IsVia and (Not IsStitchingVia)) Or IsPad)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5.118mil) (Max=1000mil) (Preferred=6mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil) (Conductor Width=10mil) (Air Gap=5mil) (Entries=4)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=9.842mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Height Constraint (Min=0mil) (Max=71497.938mil) (Prefered=500mil) (All)	0
Total	0