Lab 3: Combinational Logic Circuit

Methodology

This lab's objective is to construct the logic circuit using integrated circuits that we implemented in the prior lab. In order to carry out this experiment, we first chose a real-world issue and attempted to generalize it by constructing a truth table.

To determine whether or not I should attend lectures based on the lecture schedule, I am coding a simple circuit in my lab. I then set three input variables to match the lectures. These 3 inputs are denoted by the letters A, B and C.

I. If there is a MATH-241 lesson that day, A is 1. Else, A is 0.
II. If there is an EE-102 lesson that day, B is 1. Else, B is 0.
III. If there is an EE-211 lesson that day, C is 1. Else, C is 0.

The output of the truth table, which I then constructed in Table 1, is based on whether the courses are 1 or 0. For the results (outputs) I symbolized it with the letter R.

A-Q1	B-Q2	C-Q3	R-LED
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 1 – Truth table of circuit

Because it is easier to represent this circuit using minterm, I prefer to use the sum of product (SOP) method. Then, I represented R as,

$$R \equiv m_3 + m_6 + m_7$$

For the simplification I used my EE-102 Lab 2 calculations. (Turnitin results may be high because of this)*

which equal to,

$$R \equiv (A'.B.C) + (A.B.C') + (A.B.C)$$

applied the distributive law,

$$R \equiv (B.C).(A+A') + (A.B.C')$$

applied the complement law because A+ A'=1,

$$R \equiv (B.C).(1) + (A.B.C')$$

and again applied the distributive law,

$$R \equiv (B).(C + A.C')$$

applied the absorption law because C+A.C' = A+C,

$$R \equiv (B).(A+C) \equiv B.A + B.C \quad \text{(Eq.1)}$$

and finally the most simple version is function is obtained as $R \equiv B.A + B.C \equiv (B).(A+C)$.

The schematic design of combinational logic circuit given at Eq.1 is shown at Figure 1.

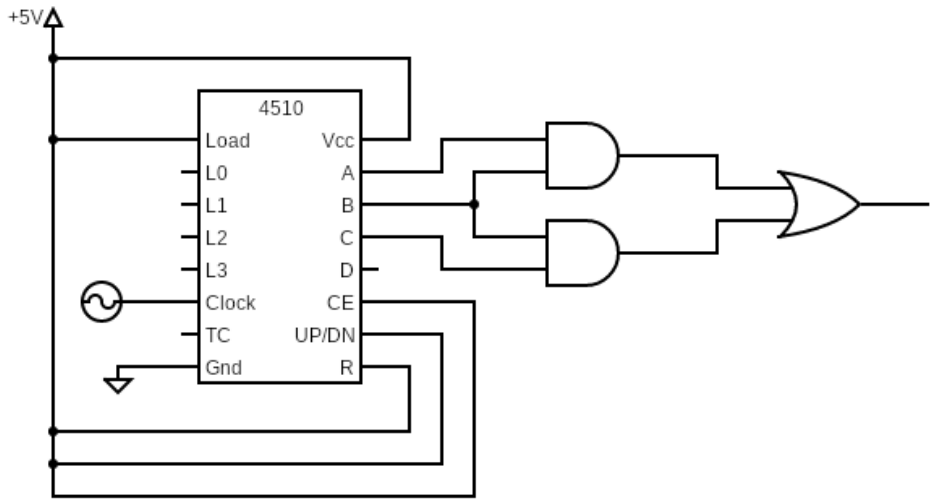

Figure 1

To create the combinational logic circuit, three different integrated circuit component is used. To change the binary bits, 74HC163 4-bit counter is used. To obtained AND-gates, SN74HC08N 4 x AND-gates is used. To obtained OR-gates, SN74HC32N 4 x OR-gates is used.

74HC163 4 Bit Counter

74HC163 4 bit counter allows us to give inputs that change constantly depending on the frequency of the AC current it takes into operation. The $Q0$, $Q1$, $Q2$ and Q3 outputs gives changing signals according to increasing binary numbers. The CP input is connected to the alternating current source. GND is connected to ground. MR, CEP, PE, CET and V_{cc} is directly connected to +5V DC. A circuit diagram of 74HC163 is shown at Figure 2.

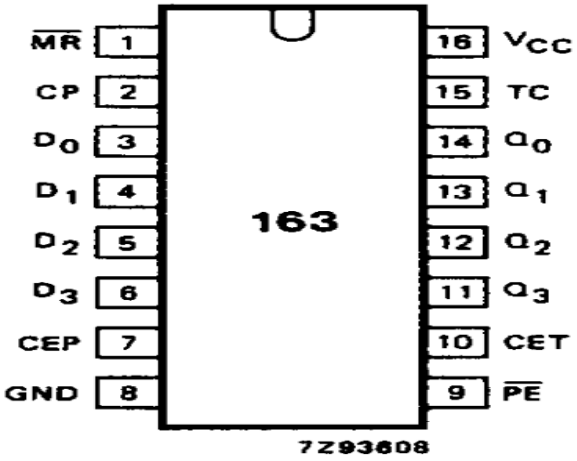

Figure 2

SN74HC08N 4 x AND-gates

SN74HC08N 4 x AND-gates allows to connect the inputs to an AND gate. It consist 4 AND gates. 12 pins of it directly connect to AND gates. It also has V_{cc} and GND pins. A circuit diagram of SN74HC08N is shown at Figure 3.

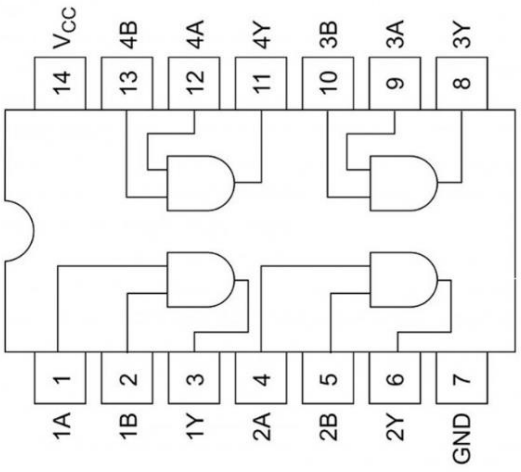

Figure 3

SN74HC32N 4 x OR-gates

SN74HC32N 4 x OR-gates allows to connect the inputs to an OR gate. It consist 4 OR gates. 12 pins of it directly connect to OR gates. It also has V_{cc} and GND pins. A circuit diagram of SN74HC32N is shown at Figure 4.

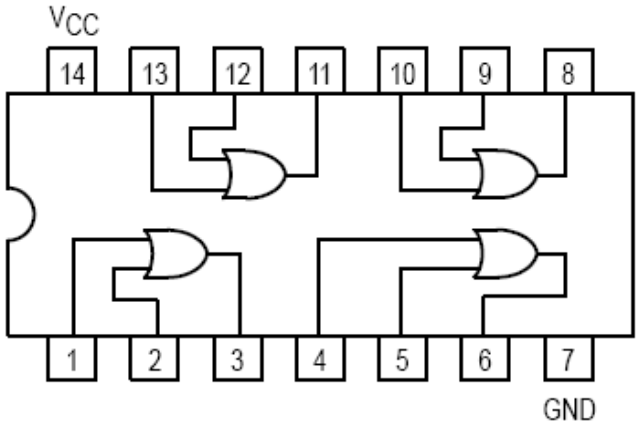

Figure 4

In the continuation of the lab, using these components, the logic circuit that we built on the FPGA board in the EE-102 lab in the second week was established. First of all, it was connected an uninterrupted 5 volt to breadboard from the power supply in order to receive changing signals from the counter. A connection was made between the pins mentioned above in the description of the 74HC163 and 5 volts. Then, a changing current with a peak to peak value of 5 volts and offset value of 2.5 V_{pp} was connected to the clock pin of the counter. It was observed that the counter was working by grounding it. In the observation made with the probe, results close to the varying values at Figure 5 were obtained.

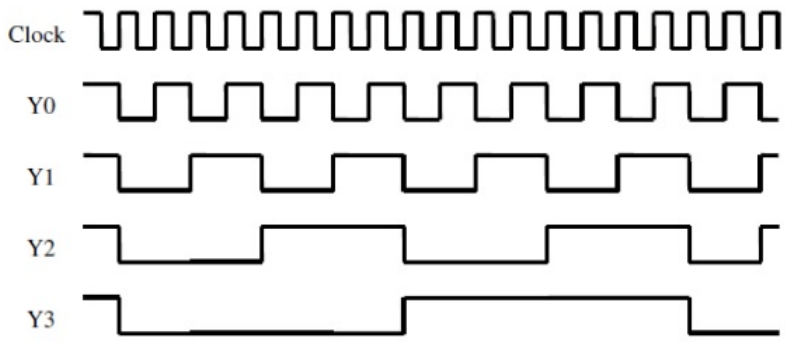

Figure 5

In later stages, SN74HC32N and SN74HC08N are connected to the breadboard. Signals are transmitted from the Q pins of the counter to other components with jumper cables. The required logic circuit is set up at this stage. It has been observed whether the output of the logic circuit at the end is correct with the help of an LED light.

Results

At the end of the lab, the entire circuit was established. Required voltage values are provided and blinking of LED is observed. As expected from the circuit, the results are compatible with the truthtable. The flashing sequence of the LED was in accordance with minterm of $m_3 + m_6 + m_7$. Photos of results are at the below.

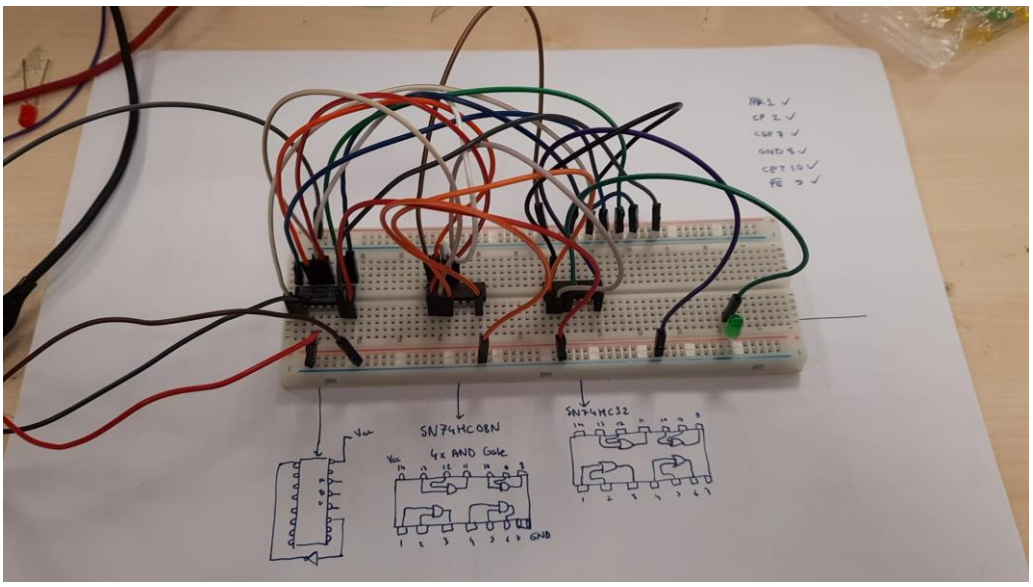

Figure 6 - R ≡ 0 (LED is off), A ≡ 0, B ≡ 0, C ≡ 0

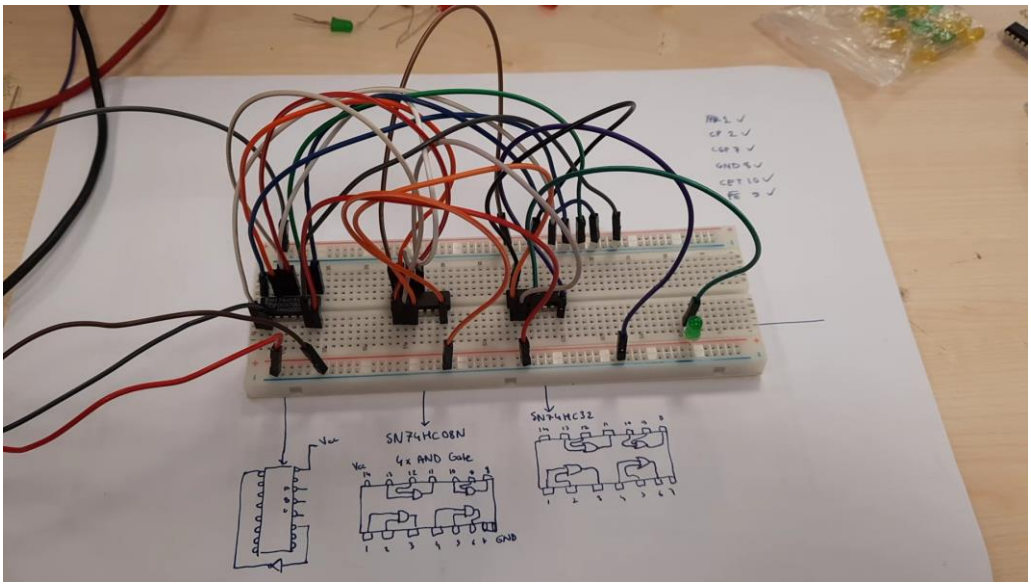

Figure 7 - R ≡ 0 (LED is off), A ≡ 0, B ≡ 0, C ≡ 1

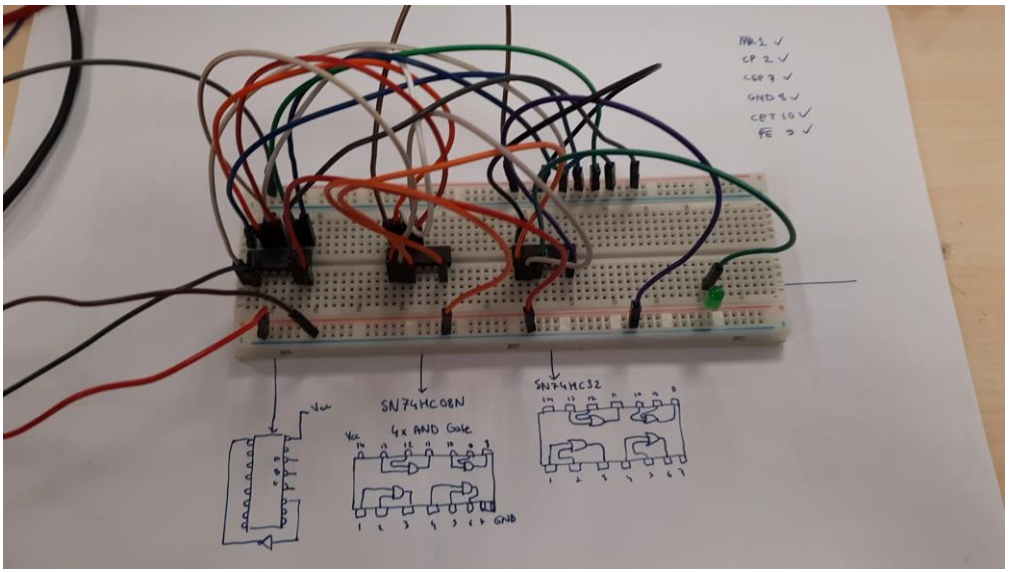

Figure 8 - R ≡ 0 (LED is off), A ≡ 0, B ≡ 1, C ≡ 0

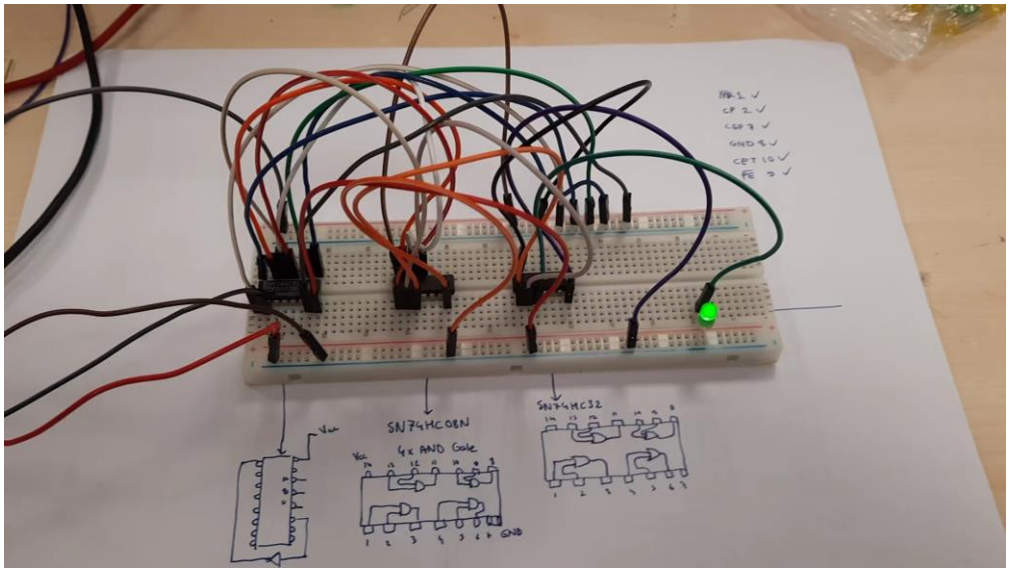

Figure 9 - R ≡ 1 (LED is on), A ≡ 0, B ≡ 1, C ≡ 1

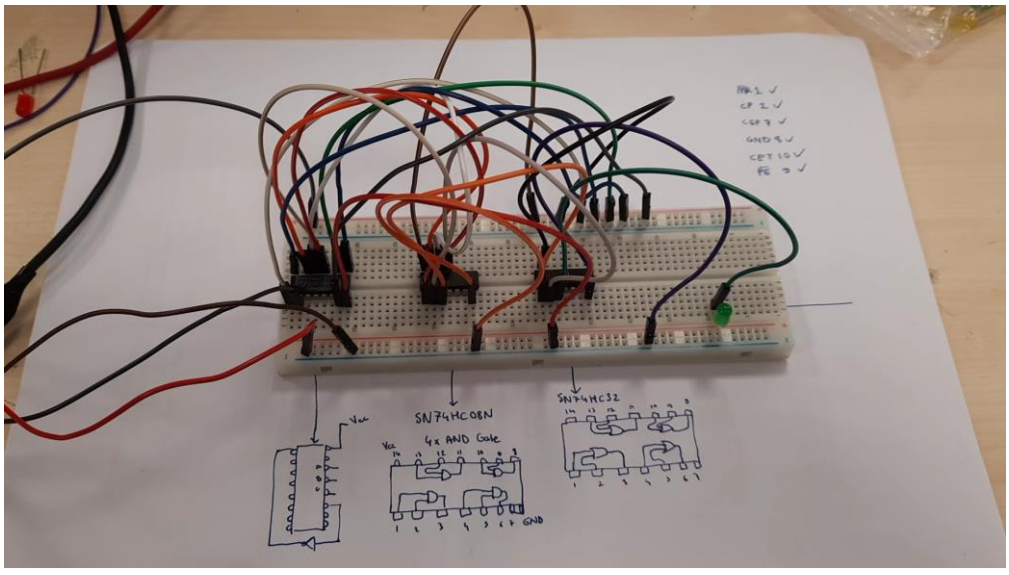

Figure 10 - R ≡ 0 (LED is off), A ≡ 1, B ≡ 0, C ≡ 0

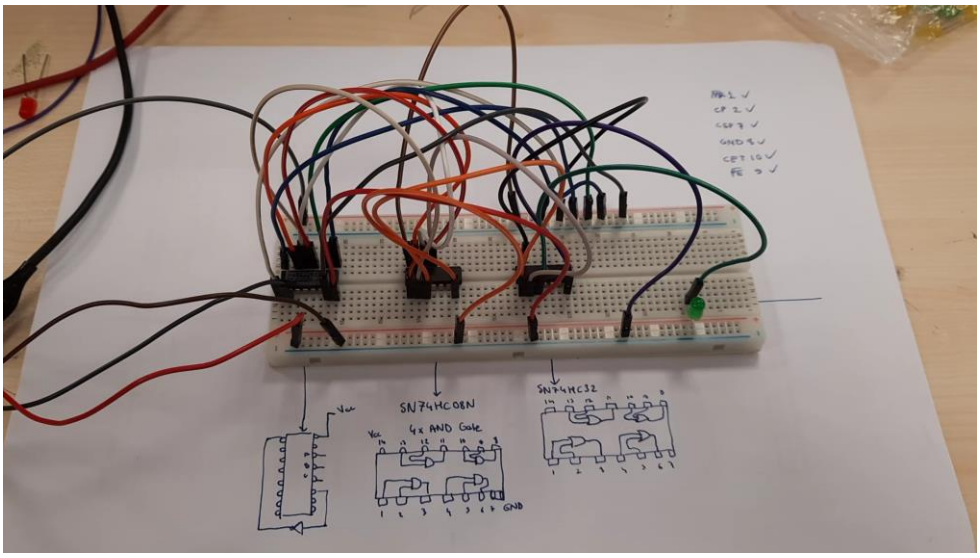

Figure 11 - R ≡ 0 (LED is off), A ≡ 1, B ≡ 0, C ≡ 1

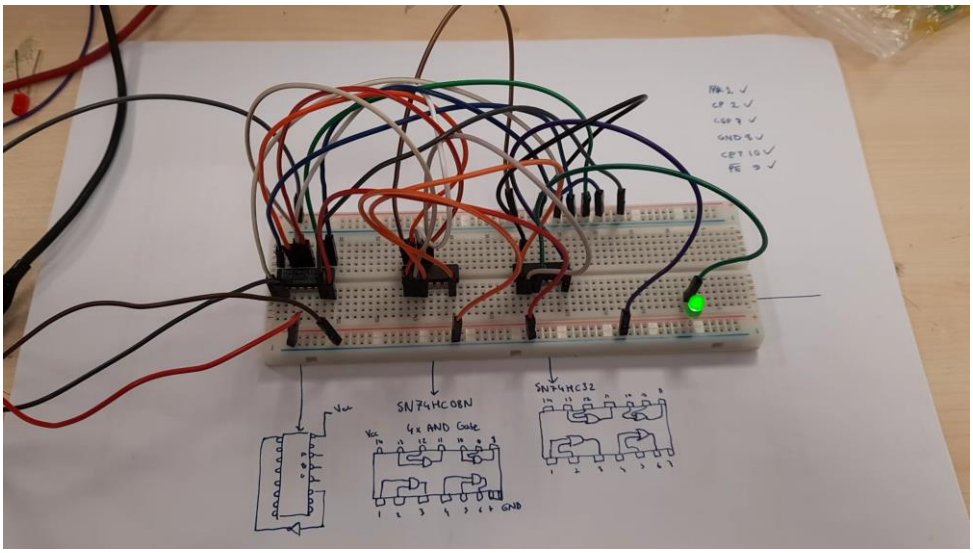

Figure 12 - R ≡ 1 (LED is on), A ≡ 1, B ≡ 1, C ≡ 0

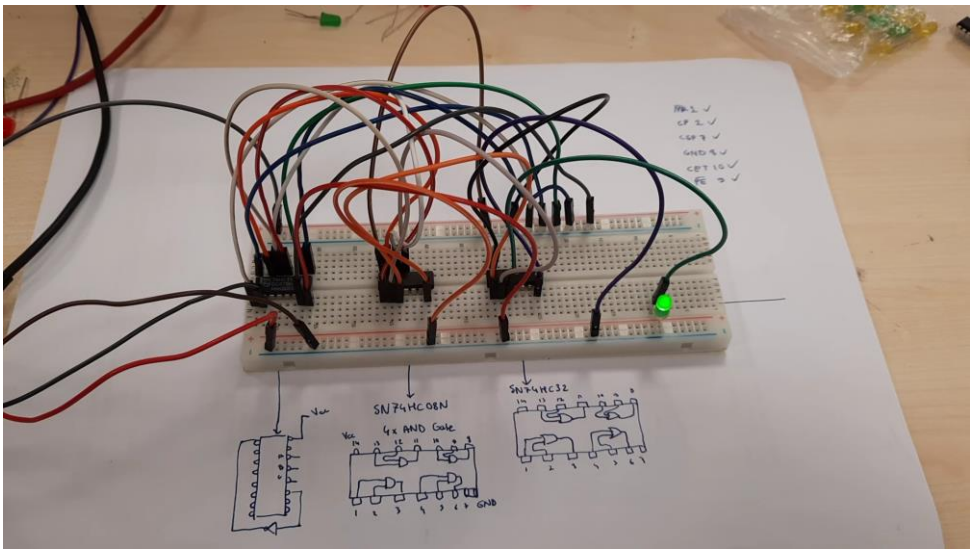

Figure 13 - R ≡ 1 (LED is on), A ≡ 1, B ≡ 1, C ≡ 1

In order to see the incoming signals on the oscilloscope, a probe was connected to the two pins of the led. The signals generated on the oscilloscope are shown in Figure 14 and Figure 15.

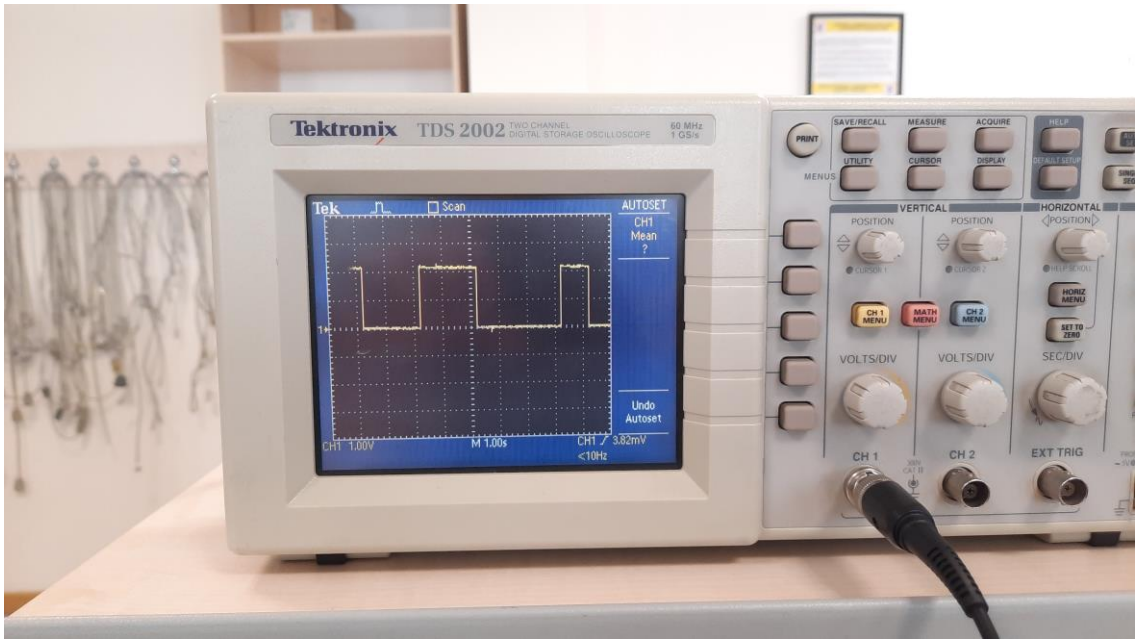

Figure 14

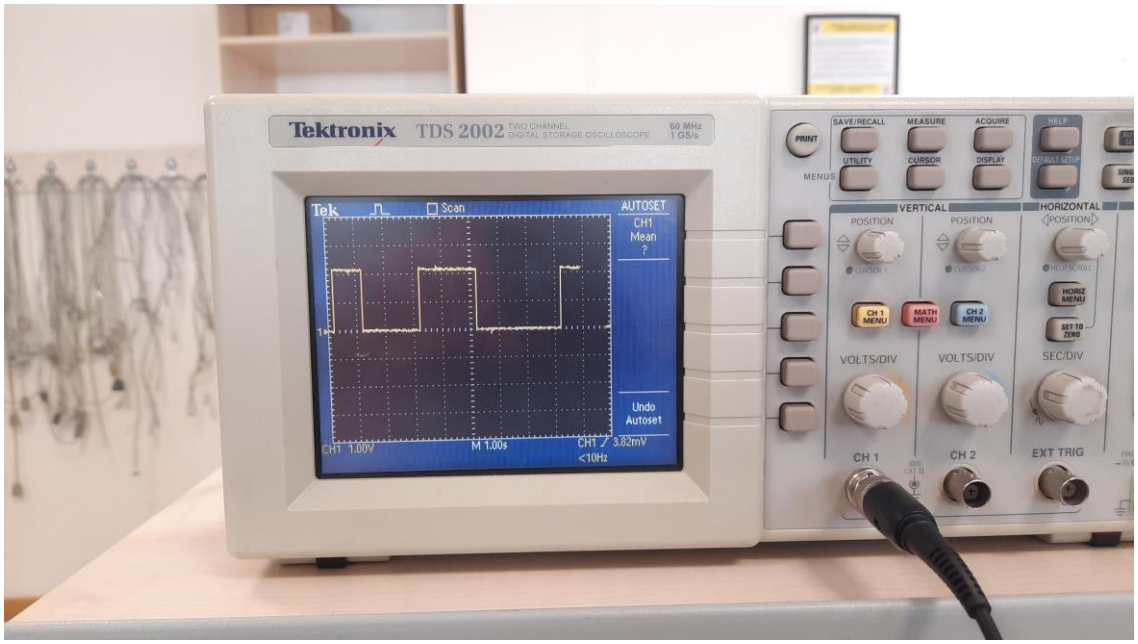

Figure 15

As seen on the oscilloscope, the times when 5 volts reach the LED are compatible with the truth table. With the frequency of the signal generator equal to 1 Hertz, it takes 8 seconds for the clock to

repeat 3 bits. Since the measuring range of the oscilloscope is 1 second, a repeating image is obtained on the screen every 8 seconds.

Conclusion

The main purpose of this lab was to implement logic circuits using integrated circuits. In this lab, I learned how to create logic circuits using an integrated circuit. In addition, I understood how I can transmit 4 bits as input with the counter circuit. While implementing the circuit, I gained experience on how to read data sheets and how to make connections. I also learned lessons from some mistakes made during the lab. For example, I will pay more attention to checking the offset settings of the signal generator. Also some errors were recorded in this lab. Although it is very difficult to observe and record, the voltage change in the circuit cannot instantly affect the LED due to the propagation delay in the integrated circuits. I could not calculate this amount of error, but the necessary information is given in the datasheet.