Chapter

3

Pulse-Width Modulation (PWM)

Electronic control of the basic power converter circuits discussed in Chap. 2 is achieved by modulating the duty factor d of the controlled switch S1, where the duty factor now consists of a variable term $\hat{d}$ in addition to the steady-state term D, which we have been using for steady-state analyses. For topologies with multiple-controlled switches that can be derived from the basic power converter circuits, d represents the total effective duty factor. Typically, the intent is to keep the output voltage constant, as determined by a dc reference signal, in the presence of time-varying sources and loads. However, there are applications where the reference signal may also be time-varying. As we shall see in Chap. 4, the amplitudes of these variations, relative to their respective steady-state values, help determine the analytical approach that may be taken to describe the total switching regulator behavior. In particular, for small enough amplitudes and low enough frequencies, relative to the switching frequency, it is possible to approximate the switching regulator as a linear system when, in fact, it is not even continuous.

Since the duty factor of S1 is defined as the ratio of its ON time to the switching period $1/f_s$ according to the equation

$$d = t_{ON} f_s = \frac{t_{ON}}{t_{ON} + t_{OFF}} \tag{3.1}$$

we see that d can be modulated by modulating either t_{ON} or t_{OFF}, or both. The technique of modulating the duration (or width) of the ON and/or OFF pulses that are applied from the control circuit to the control input of S1 is called "pulse-width modulation" (PWM).

Switching regulators can be classified as either variable-frequency or fixed-frequency. This is a useful distinction when considering electromagnetic interference (EMI) and compatibility (EMC). In principle, variable-frequency regulators can have (1) fixed t_{ON} and variable t_{OFF}, (2) fixed t_{OFF} and variable t_{ON}, or (3) variable t_{ON} and variable t_{OFF}. Naturally, PWM-controlled fixed-frequency regulators must have both variable t_{ON} and variable t_{OFF}.

Fixed ON time controllers are occasionally used in low-power boost and buck-boost regulators, where L is designed to be less than L_c, to provide a simple means of limiting peak switching current. Fixed OFF time control is sometimes used to ensure proper resetting of the transformer in single-ended configurations. Variable-frequency controllers with variable ON and OFF times are discussed in Sec. 3.1. Fixed-frequency controllers are discussed in Sec. 3.2.

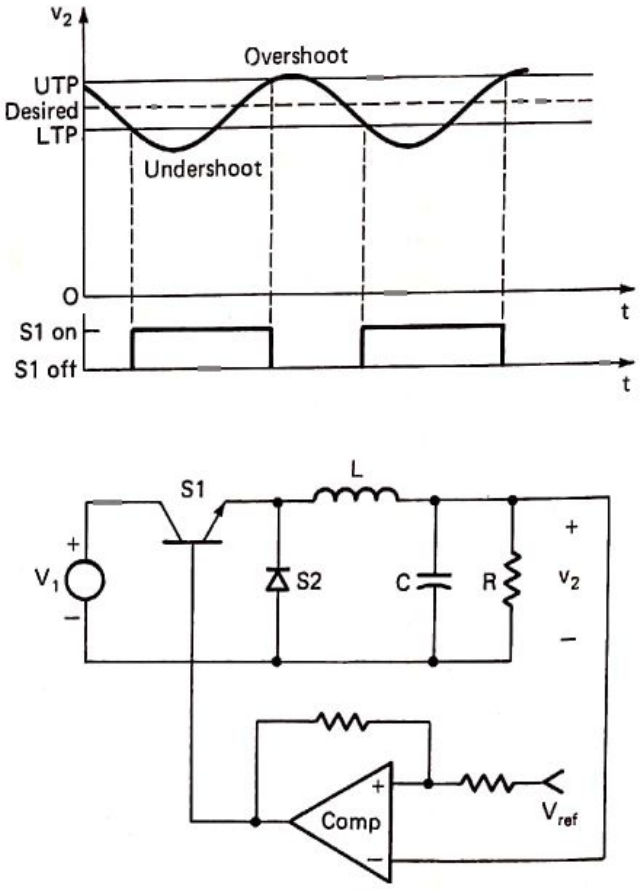


Figure 3.1 Simplified hysteretic-controlled switching regulator.

3.1 Hysteretic Controllers

Prior to the introduction of fixed-frequency integrated-circuit PWM controllers, perhaps the most common PWM control technique consisted simply of comparing the actual output, or an analog thereof, to a reference signal corresponding to the desired output (Fig. 3.1). With this technique, when the actual output becomes too low, S1 is turned on; when the output becomes too high, S1 is turned off. Neither t_{ON} nor t_{OFF} is fixed, and the variable frequency of operation is a function of R, L, C, and the hysteresis h, where h is the difference between the upper and lower trip points of the Schmitt-trigger comparator.* These regulators are variously described as hysteretic, free-running, asynchronous, or simply as bang-bang regulators. Hysteretic-controlled regulators are simple to implement and respond rapidly to sudden load changes, but they have an unpredictable noise spectrum, making EMI control more difficult.

3.2 Fixed-Frequency Controllers

Fixed-frequency PWM control is, by far, the switching regulator control technique that is most widely used today. Two reasons for this are (1) the ready availability of low-cost highly sophisticated fixed-frequency PWM integrated-circuit (IC) controllers and (2) the growing need to minimize the spurious emissions of switching regulators in increasingly sensitive computational and communicative environments. As we shall see in the next section, the switching regulator is a prolific noise generator. The task of containing this noise is made easier by fixed-frequency operation. With proper filtering, grounding, bonding, and shielding, switching regulators can be successfully used in EMI-sensitive applications.

There are many ways that fixed-frequency PWM control can be implemented, including the use of microprocessors and digital signal processing circuits with appropriate analog-to-digital converters. Nevertheless, the basic ingredients of almost all existing PWM IC controllers that are used for simple voltage control are (1) an adjustable clock for setting the switching frequency, (2) an output voltage error amplifier, (3) a sawtooth generator for providing a sawtooth signal that is synchronized to the clock, and (4) a comparator that compares the output error signal with the sawtooth signal. The output of the comparator is the signal from which the drive to the controlled switches is derived.

---

* In practice, the value of capacitor ESR may dominate over the value of C.

Figure 3.2 shows a simple PWM controller with a fixed-frequency fixed-amplitude sawtooth signal applied to the basic buck converter. The width of the PWM ON pulse is the time between the reset of the sawtooth generator and the intersection of the error voltage with the positive-going sawtooth signal, or ramp. If v_e is the error voltage amplitude, which is assumed to change slowly with respect to the switching frequency, and V_p is the sawtooth voltage amplitude, then the duty factor can be approximated by the continuous expression

$$d = \frac{v_e}{V_p} \tag{3.2}$$

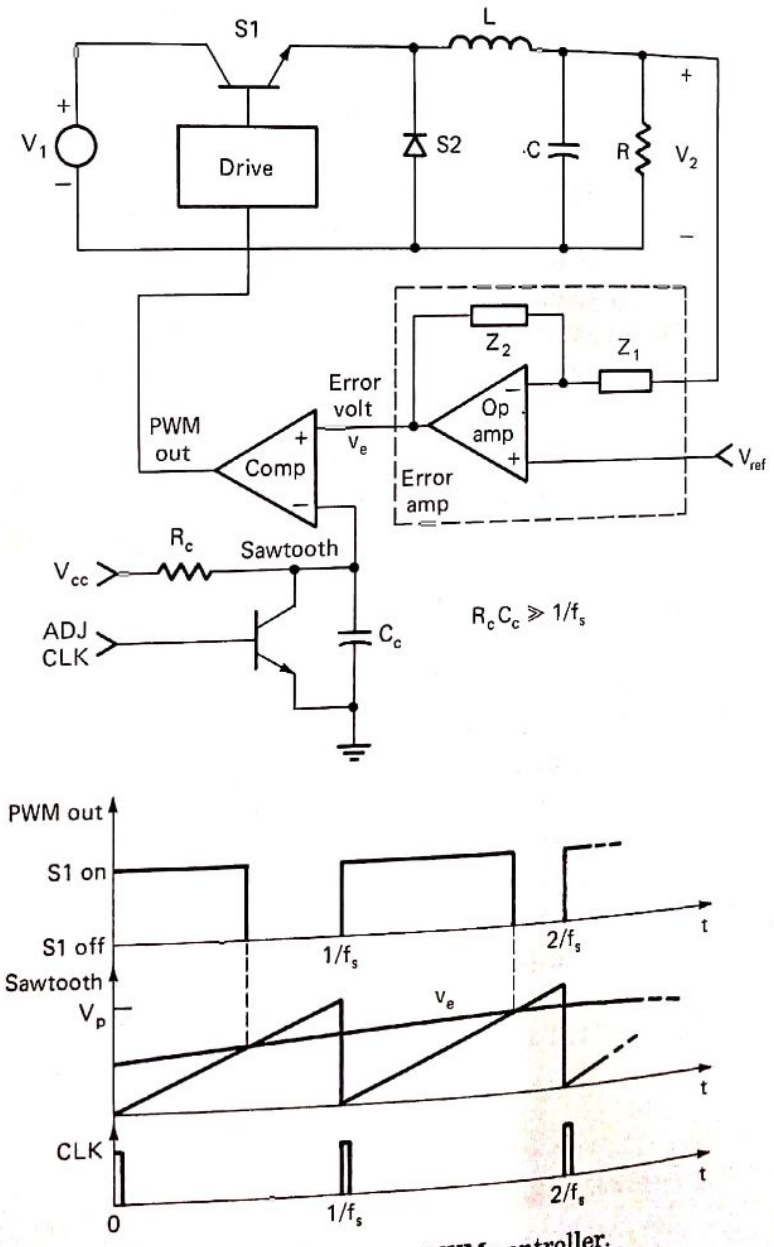


Figure 3.2 Simple fixed-frequency PWM controller.

A lower than desired output voltage produces a high error voltage and, thus, a longer ON pulse which, in turn, results in an increased output voltage. The operational amplifier's feedback network, consisting of Z_1 and Z_2, helps determine the stability and response of the switching regulator. If K is the dc gain of the error amplifier and V_2' is the open-loop input voltage to the error amplifier, then the dc open-loop gain G_0H_0 is

$$G_0H_0 = \frac{V_2}{V_2'} = \frac{V_1D}{V_2'} = \frac{V_1V_e}{V_2'V_p} = \frac{V_1KV_2'}{V_2'V_p} = \frac{V_1K}{V_p} \tag{3.3}$$

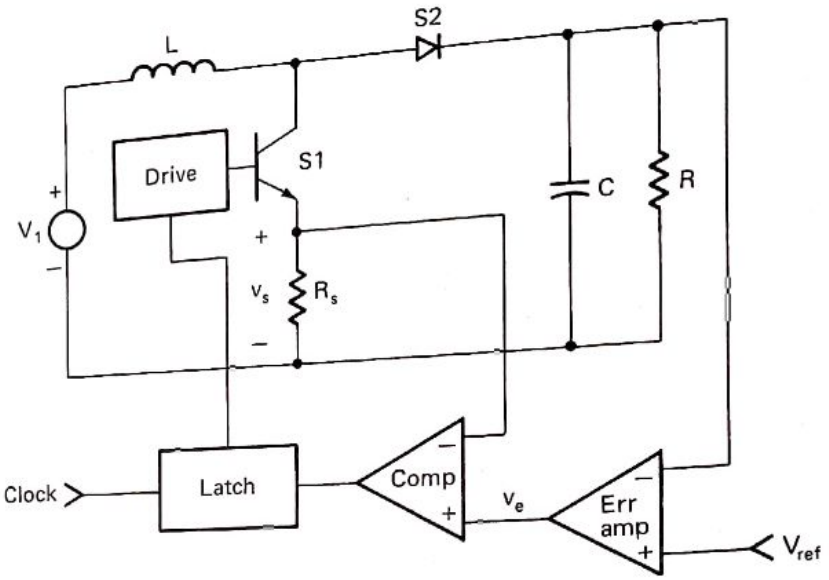
If the output voltage is divided down to the reference voltage prior to being fed to the error amplifier, then G_0H_0 is correspondingly reduced. Note that the value of dc gain in Eq. (3.3) depends directly upon the value of input voltage V_1. For applications with wide input voltage ranges, there may be a problem in maintaining enough gain at $V_{1(\min)}$ to meet performance requirements without risking instability at $V_{1(\max)}$.

This problem can be overcome by using so-called feed-forward control in which the sawtooth supply voltage V_{cc} is derived from the input supply voltage V_1. In this case, the peak sawtooth voltage V_p is directly proportional to V_1. As can be seen from Eq. (3.3), the dc open-loop gain G_0H_0 is then constant over the full range of values of V_1. Furthermore, for a fixed value of v_e, V_2 is constant over variations in V_1. This means that, ideally, line regulation can be maintained using only feed-forward control, allowing the feedback control loop to be optimized for load regulation. This feed-forward PWM control technique as described is limited to buck-derived regulators. Unfortunately, the sawtooth generators of most present-day IC controllers operate from an internally derived V_{cc}, so feed-forward control is not possible. On the other hand, these IC controllers have many built-in protection and monitoring features that designers did not always include in their older discrete-component PWM control circuit designs.

PWM controllers that are modeled after Fig. 3.2, whether they use a fixed sawtooth amplitude or not, are often called "voltage-mode" controllers since only voltage information is used. It will be shown in Chap. 6 that current information, in addition to voltage information, can be used to significant advantage, particularly for boost- and buck-boost-derived switching regulators. One way of adding current information is to use an analog of the switching current waveform in place of the sawtooth generator; after all, the ac component of the inductor current waveform is a sawtooth also. A voltage analog of the switching current waveform can be provided with a small current-sense resistor that is otherwise negligible. In practice, a resettable current transformer for isolation and scaling might also be used. Since only the

positive-going portion of the sawtooth waveform is required, the current-sense means can be placed in series with the controlled switches. This control technique is variously called "current-mode" control, to distinguish it from voltage-mode control, or "current-injected" control. The author's preference is current-injected control, since this term more accurately conveys the notion that voltage information is being augmented by, not replaced by, current information. Figure 3.3 shows, in simplified form, the basic boost converter implemented with current-injected control.

For a given cycle of operation, turn-on is coincident with the clock pulse and turnoff is coincident with the time that the analog voltage of the controlled switch current intercepts the error voltage v_e. In ad-



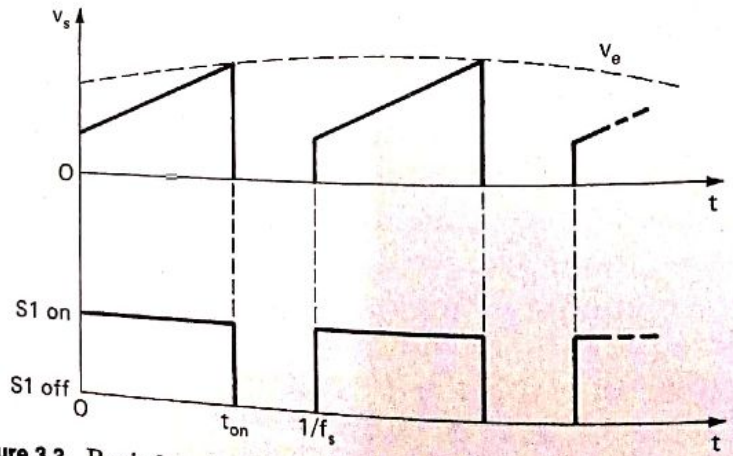


Figure 3.3 Basic boost converter with simplified current-injected control.

dition to any performance advantages, current-injected control provides inherent peak current limiting, thus enhancing the reliability of the controlled switches. Peak current limiting is a desirable feature that must be separately provided in the basic voltage-mode controller. However, as we shall see, there are applications where voltage-mode control may still be preferred. Also, as practical matters, current-injected control is somewhat more difficult to implement and there are fewer available PWM IC current-injected controllers today.

3.3 PWM Waveform Spectral Analysis

Regardless of which of the above control techniques is used, the PWM output waveform can be represented by the normalized pulse train $m(t)$ shown in Fig. 3.4. The pulse width of the nth cycle d_n/f_s is the duty factor of the nth cycle divided by the switching frequency. It consists of (1) a fixed component D/f_s that is determined by the steady-state values of source, load, and reference, and (2) a modulating component $\hat{d}_n/f_s$ that is determined by the time variations in source, load, and reference. As shown, turn-on always occurs at the beginning of the cycle, whereas the relative turnoff times are variable. Consequently, this particular method of PWM control is sometimes described as "trailing-edge" modulation. Conceptually, one could just as well have "leading-edge" modulation or a combination of both trailing-edge and leading-edge modulation. However, the practical differences are small[1] and only trailing-edge modulation will be considered further, particularly since nearly all PWM IC controllers use this method.

The pulse train of Fig. 3.4 is representative of the input switching current in buck-derived converters, the output switching current in boost-derived converters, and both input and output switching currents in buck-boost-derived converters. It also represents the voltage waveform applied to the output filter of buck-derived converters. Furthermore, for any of the PWM switching regulators, it is representative of

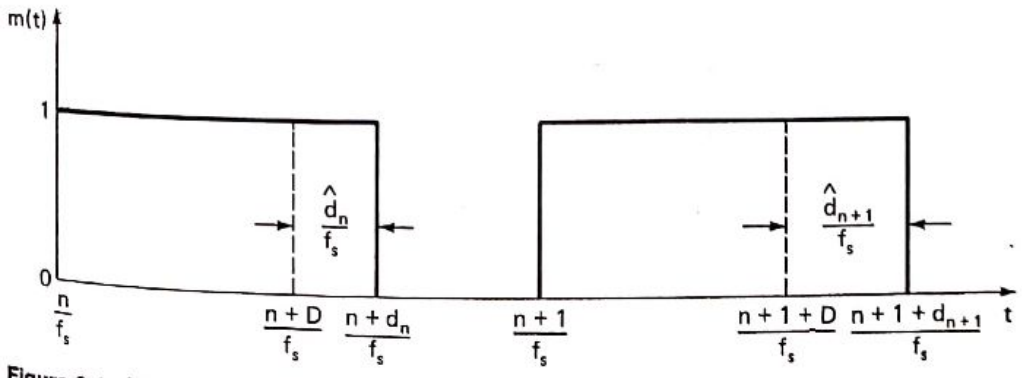


Figure 3.4 Normalized PWM output waveform.

the source of radiated electric and magnetic fields. Thus, an analysis of the frequency spectrum of the PWM output waveform would provide useful information for predicting system noise and for designing associated filters.

In performing this analysis, we consider the situation where the error voltage v_e consists of a dc component V_e and a time-varying component $V_{e1} \sin 2\pi f_m t$, where f_m is the modulation frequency of a variation in source, load, or reference signal. The modulation in error voltage gives rise to a corresponding modulation in duty factor. The duty factor for any given cycle is determined by the exact time at which the positive-going sawtooth intercepts the modulating error signal in accordance with the transcendental equation

$$d_n = D + D_1 \sin \frac{2\pi f_m (n + d_n)}{f_s} \tag{3.4}$$

where D_1 is the peak variation in duty factor. Such a system is sometimes referred to as a "real-time" sampling system, since the pulse widths are not determined prior to the completion of the pulses. In an explicit sample-and-hold PWM system, the pulse widths are predetermined at the beginnings of the pulses, coincident with the clock pulses, according to the equation

$$d_n = D + D_1 \sin \frac{2\pi f_m n}{f_s} \tag{3.5}$$

For the sample-and-hold case, there is an associated transport lag of $2\pi f_m D/f_s$ radians (rad). For high enough modulation frequencies with respect to the switching frequency, the transport lag can be significant and must be included in any loop stability analysis. Real-time sampling systems exhibit no transport lag.[2,3]

The PWM output waveform $m(t)$, as shown in Fig. 3.4, can be expressed as a Fourier series according to the equation

$$m(t) = \sum_{k=1}^{\infty} a_k \sin 2\pi k f_m t + \sum_{k=1}^{\infty} b_k \cos 2\pi k f_m t + D \tag{3.6}$$

where

$$a_k = 2f_m \int_0^{1/f_m} m(t) \sin 2\pi k f_m t \, dt = 2f_m \sum_{n=1}^{r} \int_{n/f_s}^{(n+d_n)/f_s} \sin 2\pi k f_m t \, dt \tag{3.7a}$$

and

$$b_k = 2f_m \int_0^{1/f_m} m(t) \cos 2\pi k f_m t \, dt = 2f_m \sum_{n=1}^{r} \int_{n/f_s}^{(n+d_n)/f_s} \cos 2\pi k f_m t \, dt \tag{3.7b}$$

where r is the ratio of switching frequency to modulation frequency f_s/f_m. Solving Eqs. (3.7a) and (3.7b) results in

$$a_k = \frac{1}{\pi k} \sum_{n=1}^{r} \left[\cos \frac{2\pi k n}{r} - \cos \frac{2\pi k (n + d_n)}{r} \right] \tag{3.8a}$$

and

$$b_k = \frac{1}{\pi k} \sum_{n=1}^{r} \left[\sin \frac{2\pi k (n + d_n)}{r} - \sin \frac{2\pi k n}{r} \right] \tag{3.8b}$$

or

$$a_k = \frac{1}{\pi k} \sum_{n=1}^{r} \left(\cos \frac{2\pi k n}{r} - \cos \frac{2\pi k n}{r} \cos \frac{2\pi k d_n}{r} + \sin \frac{2\pi k n}{r} \sin \frac{2\pi k d_n}{r} \right) \tag{3.9a}$$

and

$$b_k = \frac{1}{\pi k} \sum_{n=1}^{r} \left(\sin \frac{2\pi k n}{r} \cos \frac{2\pi k d_n}{r} + \sin \frac{2\pi k d_n}{r} \cos \frac{2\pi k n}{r} - \sin \frac{2\pi k n}{r} \right) \tag{3.9b}$$

Since Eq. (3.4) is transcendental, there is no sense in using it for d_n in Eq. (3.9) at this point; we would only get d_n back again. Therefore, some sort of reasonable approximation must be made in order to carry this analysis forward in closed form. We recognize from Eq. (3.4) that

$$\hat{d}_n = D_1 \sin \frac{2\pi (n + d_n)}{r} \tag{3.10}$$

Trigonometrically expanding Eq. (3.10), substituting $d_n = D + \hat{d}_n$, and expanding again results in

$$\hat{d}_n = D_1 \sin \frac{2\pi n}{r} \left(\cos \frac{2\pi D}{r} \cos \frac{2\pi \hat{d}_n}{r} - \sin \frac{2\pi D}{r} \sin \frac{2\pi \hat{d}_n}{r} \right) + D_1 \cos \frac{2\pi n}{r} \left(\sin \frac{2\pi D}{r} \cos \frac{2\pi \hat{d}_n}{r} + \sin \frac{2\pi \hat{d}_n}{r} \cos \frac{2\pi D}{r} \right) \tag{3.11}$$

It will now be assumed that the peak duty factor variation D_1 is small enough and the ratio of switching frequency to modulation frequency r is large enough so that the following approximations are valid:

$$\cos \frac{2\pi \hat{d}_n}{r} \approx 1 \tag{3.12a}$$

and

$$\sin \frac{2\pi \hat{d}_n}{r} \approx \frac{2\pi \hat{d}_n}{r} \tag{3.12b}$$

Combining Eqs. (3.11) and (3.12) results in

$$\hat{d}_n = \frac{D_1 \sin [2\pi(n + D)/r]}{1 - (2\pi D_1/r) \cos [2\pi(n + D)/r]} \tag{3.13}$$

or

$$d_n = D + \frac{D_1 \sin [2\pi(n + D)/r]}{1 - (2\pi D_1/r) \cos [2\pi(n + D)/r]} \tag{3.14}$$

Equation (3.14) can now be substituted into Eq. (3.9) to solve explicitly for a_k and b_k, given r, D_1, and D.

Computer design aids can be used to good advantage in predicting the spectrum of a PWM waveform. For example, a personal computer

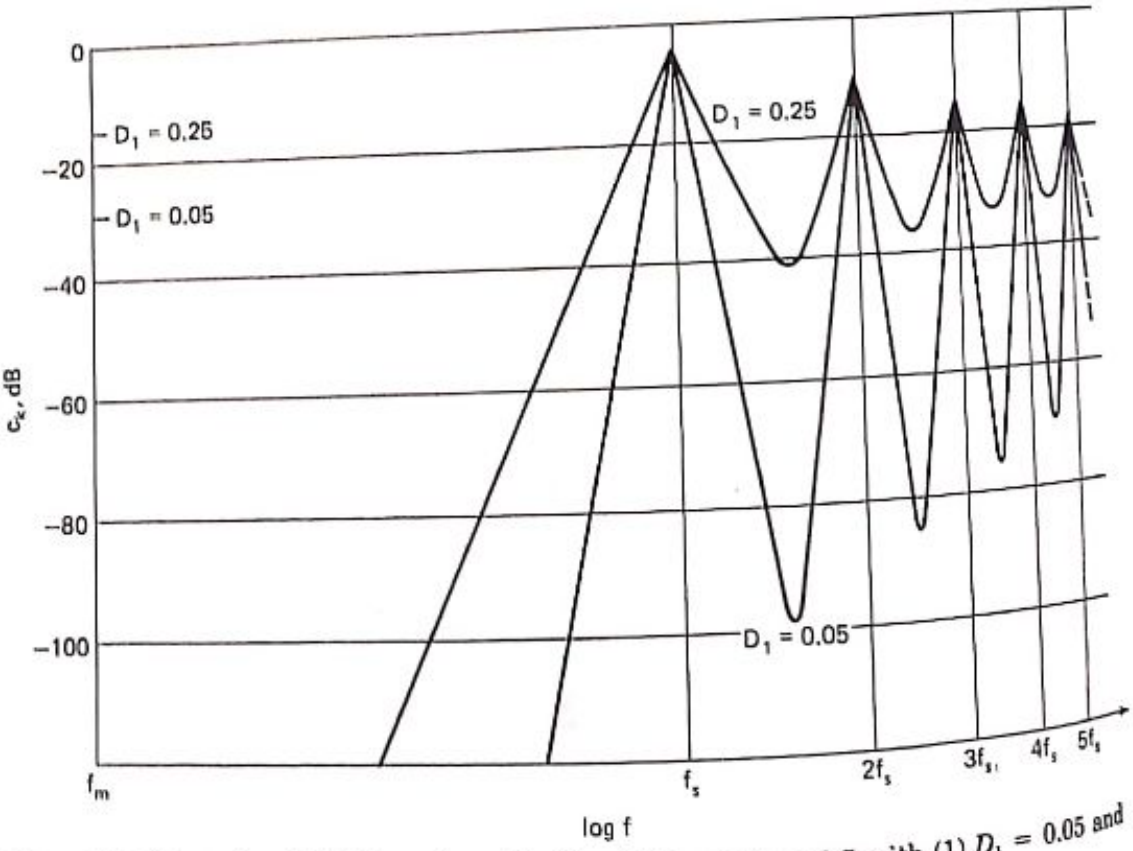


Figure 3.5 Normalized PWM spectrum for $f_s = 10f_m$ and $D = 0.5$ with (1) $D_1 = 0.05$ and (2) $D_1 = 0.25$.

program[4] has been written that, for user-entered values of r, D, and D_1, calculates $c_k = \sqrt{a_k^2 + b_k^2}$ for $k = 1$ (i.e., the modulation frequency), for $k = r$, $r \pm 1$, $r \pm 2$, $r \pm 3$, $r \pm 4$ and $r \pm 5$ (i.e., the switching frequency and the first five modulation frequency increments about either side), and for the corresponding points about the first four harmonics of the switching frequency. Figure 3.5 shows these spectral points for $r = 10$, $D = 0.5$, and $D_1 = 0.05$, and also for $D_1 = 0.25$. A factor of 5 corresponds to 14 decibels (dB); however, several points were increased by more than 14 dB in going from $D_1 = 0.05$ to $D_1 = 0.25$, showing the nonlinear operation of a pulse-width modulator.

In addition to providing a quantitative means for predicting noise external to the switching regulator, programs such as this can be used to predict the behavior of the switching regulator itself in the presence of its own noise. In particular, it is possible for harmonics of the modulation frequency to mix with the switching frequency in such a way that the harmonics are reinforced, according to the equation

$$f_s - kf_m = kf_m \tag{3.15a}$$

or

$$f_m = \frac{f_s}{2k} \tag{3.15b}$$

Switching regulators have been observed that sustain so-called subharmonic oscillations at one-half and sometimes even one-fourth of the switching frequency. Particularly susceptible are push-pull and bridge converters, where a significant $f_s/2$ component may inherently exist because of power circuit imbalances. In general, the higher the unity-gain cross-over frequency of the open-loop gain, the greater the susceptibility to subharmonic oscillations. With computer design aids, this risk can be quantitatively assessed.

3.4 Illustrative Problems

3.1 A 100 kHz half-bridge converter [Fig. 2.15(d)] operates from a three-phase full-wave-rectified 400-Hz aircraft bus and produces 50 V dc at 20 A dc for a solid-state power amplifier with a nominal effective duty factor of 0.5. The wideband feedback control circuitry is designed to maintain good dynamic output voltage regulation for load modulation frequencies up to 20 kHz, where the ac duty factor variation can be as much as ±10 percent. To save the development effort of a second power supply, a low-power 24-V dc output was included whose regulation depends upon the 50-V dc control loop. The 24-V dc output has an LC filter with $L > L_c$ and 40-dB rejection at 200 kHz.

It now turns out that although the 24-V dc load is nearly constant and is tolerant to absolute voltage variations, it is extremely sensitive to any 160-kHz signals greater than 1 mV rms. The original power supply designer says

that there is no problem since there can only be the 200-kHz effective frequency component and harmonics thereof. What do you say?

SOLUTION: Consider the situation at $f_m = 20$ kHz.

$$r = \frac{f_s}{f_m} = \frac{200 \text{ kHz}}{20 \text{ kHz}} = 10$$

$$k = \frac{160 \text{ kHz}}{20 \text{ kHz}} = 8 = r - 2$$

$$D_1 = 0.1(D) = 0.01$$

From Fig. 3.5, the spectral content of the normalized PWM waveform at 160 kHz is -50 dB. For $D = 0.5$, the pulse amplitude must be 48 V dc for a 24-V dc output. Thus, the peak 160-kHz component into the output filter is

$$-50 \text{ dB} + 20 \log 48 = -16.4 \text{ dB}$$

The filter rejection at 160 kHz is

$$-40 \text{ dB} + 20 \log \left(\frac{200}{160}\right)^2 = -36.1 \text{ dB}$$

Thus, the peak 160-kHz component out of the filter is

$$-16.4 \text{ dB} - 36.1 \text{ dB} = -52.5 \text{ dB}$$

$$-52.5 \text{ dB} \rightarrow 2.5 \text{ mV pk} = 1.78 \text{ mV root mean square (rms)}$$

$$1.78 \text{ mV rms} > 1 \text{ mV rms}$$

Therefore, trouble is possible, even without considering the imbalancing effects of the half-bridge converter, which can produce a 100-kHz output that is subject to modulation as well, and without considering possible source modulations.

3.2 In Sec. 3.3, it was stated that real-time sampling systems exhibit no transport lag. What is the effect of a time delay t_d between the "real time" that the sawtooth intercepts the error signal and the time that S1 actually turns off?

SOLUTION: The duty factor of the nth cycle d_n, instead of being $D + \hat{d}_n$, is now determined by the equation

$$d_n = D + \hat{d}_n + t_d f_s$$

The control loop still maintains nearly constant dc output voltage, so the new value of D is smaller by the amount $t_d f_s$, corresponding to a lower value of dc error voltage v_e. From Eq. (3.6), it is clear that any phase shift at the modulation frequency between the PWM output signal $m(t)$ and the time-varying error

voltage component $v_{e1} \sin 2\pi f_m t$ can be expressed as

$$\phi_1 = \tan^{-1} \frac{b_1}{a_1}$$

Substituting the new expression for d_n into Eq. (3.8a) for $k = 1$ results in

$$a_1 = \frac{1}{\pi} \sum_{n=1}^{r} -\cos \frac{2\pi}{r}(n + D + \hat{d}_n + t_d f_s)$$

where it is recognized that

$$\sum_{n=1}^{r} \cos \frac{2\pi n}{r} = 0 \qquad r > 1$$

Trigonometrically expanding, we have

$$a_1 = \frac{1}{\pi} \sum_{n=1}^{r} \left[\sin \frac{2\pi}{r}(n + D) \sin \frac{2\pi}{r}(\hat{d}_n + t_d f_s) \right.$$
$$\left. - \cos \frac{2\pi}{r}(n + D) \cos \frac{2\pi}{r}(\hat{d}_n + t_d f_s) \right] \qquad r > 1$$

Using Eq. (3.12) and expanding again gives us

$$a_1 = \frac{1}{\pi} \sum_{n=1}^{r} \left[\sin \frac{2\pi}{r}(n + D) \sin \frac{2\pi t_d f_s}{r} \right.$$
$$+ \frac{2\pi \hat{d}_n}{r} \cos \frac{2\pi t_d f_s}{r} \sin \frac{2\pi}{r}(n + D)$$
$$- \cos \frac{2\pi}{r}(n + D) \cos \frac{2\pi t_d f_s}{r}$$
$$\left. + \frac{2\pi \hat{d}_n}{r} \sin \frac{2\pi t_d f_s}{r} \cos \frac{2\pi}{r}(n + D) \right] \qquad r > 1$$

Substituting Eq. (3.13), where it is assumed that $2\pi D_1/r \ll 1$, for $\hat{d}_n$ above and recognizing that

$$\sum_{n=1}^{r} \sin \frac{2\pi}{r}(n + D) = \sum_{n=1}^{r} \cos \frac{2\pi}{r}(n + D) = 0 \qquad r > 1$$

results in

$$a_1 = \frac{1}{\pi} \sum_{n=1}^{r} \left[\frac{2\pi D_1}{r} \cos \frac{2\pi t_d f_s}{r} \sin^2 \frac{2\pi}{r}(n + D) \right.$$
$$\left. + \frac{2\pi D_1}{r} \sin \frac{2\pi t_d f_s}{r} \sin \frac{2\pi}{r}(n + D) \cos \frac{2\pi}{r}(n + D) \right] \qquad r > 1$$

Substituting the trigonometric identities

$$\sin^2\alpha = \tfrac{1}{2}(1 - \cos 2\alpha)$$

and

$$\sin\alpha\cos\alpha = \tfrac{1}{2}\sin 2\alpha$$

into the equation above yields

$$a_1 = \frac{D_1}{r}\sum_{n=1}^{r}\left\{\cos\frac{2\pi t_d f_s}{r}\left[1 - \cos\frac{4\pi}{r}(n + D)\right] + \sin\frac{2\pi t_d f_s}{r}\sin\frac{4\pi}{r}(n + D)\right\} \qquad r > 1$$

Since

$$\sum_{n=1}^{r}\cos\frac{4\pi}{r}(n + D) = \sum_{n=1}^{r}\sin\frac{4\pi}{r}(n + D) = 0 \qquad r > 2$$

and

$$\sum_{n=1}^{r} 1 = r$$

we arrive at

$$a_1 = D_1\cos\frac{2\pi t_d f_s}{r}$$

Similarly,

$$b_1 = -D_1\sin\frac{2\pi t_d f_s}{r}$$

Thus,

$$\phi_1 = -\tan^{-1}\left(\tan\frac{2\pi t_d f_s}{r}\right) = -\frac{2\pi t_d f_s}{r} = -2\pi t_d f_m$$

This is, for example, the phase shift due to a switching transistor with a storage time t_d, even in a so-called real-time sampling system. If the storage times of the transistors in a push-pull converter operating at 300 kHz are 1 microsecond (μs), then the modulator phase shift at one-tenth the effective switching frequency is

$$\phi_1 = -2\pi \times 10^{-6} \times 60 \times 10^3 = -0.377 \text{ rad} = -21.6^\circ$$

This may not be a trivial consideration in a wideband lead-compensated*

* This is discussed further in Chap. 5.

system. The result of $\phi_1 = -2\pi t_d f_m$ is also sufficient to prove the statement that transport lag of a sample-and-hold pulse-width modulator is $\phi_1 = -2\pi f_m D/f_s$, where D/f_s is interpreted here as the total delay for the case where the pulse width is determined at the beginning of the switching period.

References

1. W. R. Kolk, "A Study of Pulse Width Modulation in Feedback Control Systems," Ph.D. dissertation, Univ. of Conn., 1972.
2. D. M. Mitchell, "Pulsewidth Modulator Phase Shift," *IEEE Transactions on Aerospace and Electronic Systems,* vol. AES-16, no. 3, May 1980, pp. 272–278.
3. R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," *Proceedings of Powercon 8,* Power Concepts, Inc., Ventura, CA, April 1981.
4. D. M. Mitchell, "Spectral Analysis of Pulse-Width Modulated (PWM) Waveforms," Rockwell International Working Paper WP84-2023, July 1984.