

Collaboration Meeting: TDAQ Update

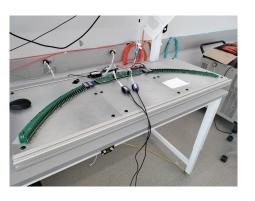
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Working area



- 3 test stands (TS0,1,2) IERC;
- Optical fibers connect them to the DTC installed in the DAQ computer mu2edaq09;
- Each teststand has 96 channels;
- A pulser implemented in the DRACs is sending pulses to the preamps (CAL side) at 50 kHz;
- Pulses are digitized at 40 MHz;
- Only 12 channels pulsed per RUN (one pulse every 8 channels);
- We are using 1 or 2 ROCs at the same time.

Data Quality Monitoring

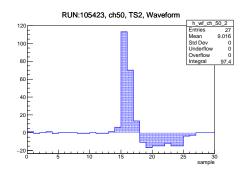
Description of the teststand setup

A timing diagram of a single channel readout is shown in Fig. 5. Pulses, separated by Tgen = 1/fgen, where fgen is the generator frequency are represented by gray triangles. The event window, with the width of TEW, that represents the distance between the proton pulses, was varied from 700 ns to $50\mu s$. The ROC firmware has an internal hit buffer which stores up to 255 hits. Depending on Tgen and TEW, the data taking can proceed in two different scenarios: The event window is large enough, so the total number of generated hits is greater than 255. In this case the ROC hit buffer always gets filled up, and only the first 255 hits are read out; The total number of hits within the event window is less than 255. In this case the ROC hit buffer doesnât get filled up and the total number of hits may vary from one event to another. Each digi FPGA has its own pulse generator and the pulse sequences from the two generators are offset with respect to each other by a time interval Δt . The offset is constant for as long as the DRAC board is powered up and varies randomly between 0 and Tgen when DRAC is powercycled. The timing of the readout is uncorrelated with the generator timing seguinces

Waveforms

We can plot:

- Number of hits vs channel;
- Waveform shape;
- First Sample ($Wf_{thr} > 5$);
- Charge;
- Pulse Height;



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