Commissioning of the Mu2e Data AcQuisition system and the Vertical Slice Test of the straw tracker

11. Mu2e ROC simulation

version 1.0 October 23, 2023

Abstract

This note presents an analysis of data coming from the teststand of the motherboard and the comparison with ROC simulation.

Contents

1 Notes for the authors

1.1 Revision history

- v1.01: initial version

2 Introduction to the analysis

In this note, we present an analysis of the data derived from the readout teststands of the motherboard. This analysis was performed with the aim of characterizing the functionality of the Data Acquisition (DAQ) system. A signal generator was employed to send pulses and we tried to understand the output and non-output of the DTC. Our study centered on testing the performance of ROCs and DTCs, actually we were reading 1 ROC (96 channels), which is the equivalent of one panel or 2 ROCs. The analysis was executed employing a single DTC. During the analysis, we had the capability to change different generator's features. We varied the event window duration between successive pulses and modulated the generator's operating frequency. Specifically, we could operate with two distinct frequencies: 31.29 MHz/(2^7+1), resulting in approximately 250 kHz, and 31.29 MHz/(2^9+1), 60 kHz.

The selection of the event window duration and the frequency played an important role in determining the number of hits per event, considering that the ROC buffer possessed a storage capacity for up to 255 hits. The relationship between the generator and readout counts can be summarized as follows:

- $N_{gen} < 255$: $N_{readout} = N_{gen}$;

- $N_{gen} \geq 255$: $N_{readout} = 255$.

3 Full buffer mode: RUN281

3.1 Time distribution

The analysis started analyzing the data time distribution of each channel. After a preliminary observation of the distributions, we saw a different pattern for channels in the first FPGA and in the second FPGA, as illustrated in Fig. 1: the initial though was the occurrence of a cessation in data acquisition for specific channels at a certain time.
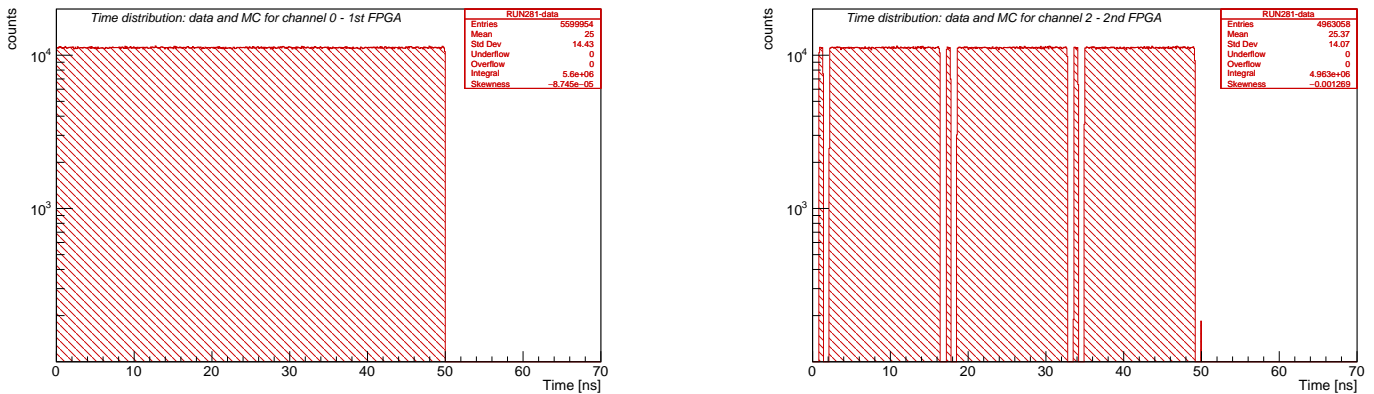

Figure 1: right: First FPGA's channel time distribution, right: Second FPGA's channel time distribution.

We thought it was necessary to characterize the apparatus with a Monte Carlo simulation for our Data Acquisition (DAQ) system, in order to understand the interruptions, so we redirect to section **??** for further information.

3.2   nh vs ch

At this point we have plotted the number of hits versus the channel number in the order that we expected, as we can see in Fig. **??**.

3.3   nhits

4   buffer not full

4.1   Time distribution

4.2   nh vs ch

4.3   nhits

5   Monte Carlo simulation

6   rate

7 Summary

Upper bounds on the direct beam-related backgrounds are as follows:

- background from beam electrons scattered in the stopping target $< 1 \times 10^{-3}$

- background from muon decay in flights $< 1 \times 10^{-3}$

- background from beam muons scattered in the stopping target $< 1 \times 10^{-5}$