ECE/CS 250 Exam: Answer Key (Numbered)

SectionECE/CS 250 Exam Answer Key with Slide References

Section1: Fundamentals & Digital Logic

1. A flip-flop stores a single bit of state, updating only on a clock edge.[See 5-logic-sequential.pdf, slides 69]

2. A D flip-flop diagram includes D (input), Q (output), clock input, and optional enable. On rising edge, D is latched to Q.[5-logic-sequential.pdf, slide 6]

3. Combinational: output = f(inputs); Sequential: output = f(inputs, previous state).[5-logic-sequential.pdf, slide 3]

4. FSMs are circuits that remember past inputs using state. They consist of states and transitions.[5-logic-sequential.pdf, slides 2427]

5. Moore: outputs depend only on state. Mealy: outputs depend on state and inputs.[5-logic-sequential.pdf, slide 26]

6. A decoder converts binary input to one-hot output for selecting registers.[5-logic-sequential.pdf, slides 1315]

Section2: From C to Binary & Data Representation

7. -18 = 11101110 (8-bit 2's complement)[2b-from-C-to-binary.pdf, slide 13]

8. Two's complement enables easy negation, only one zero, simple hardware.[2b-from-C-to-binary.pdf, slide 1314]

9. IEEE 754 uses sign, exponent, and mantissa. 32 bits: 1|8|23 format.[2b-from-C-to-binary.pdf, slide 9]

10. Binary: 1001001, Hex: 0x49[2b-from-C-to-binary.pdf, slide 56]

11. Steps: C assembly binary (compiler + assembler).[2a-cprogramming.pdf, slide 67]

12. C allows direct memory access and pointer arithmetic.[2a-cprogramming.pdf, slide 22]

Section3: MIPS Assembly Language

13. add $11, $11, $10[3-assembly.pdf, slide 17]

14. Op=000000, rs=00010, rt=00011, rd=00001[3-assembly.pdf, slide 23]

15. j sets PC to specified label address.[3-assembly.pdf, slide 18]

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16. Displacement mode: adds base register and offset.[3-assembly.pdf, slide 25]

17. Use loop with addi, bne, add.[General synthesis of slides 1217]

18. slt sets dest to 1 if rs < rt. Used before conditional branch.[3-assembly.pdf, slide 37]

19. Op=100011, base=00110, rt=00101, offset=0000 0000 0001 0000[3-assembly.pdf, slide 28]

20. R-type: 3 registers, I-type: 2 registers + immediate.[3-assembly.pdf, slide 22]

21. All ALU operations require registers; memory accessed only via loads/stores.[3-assembly.pdf, slide 32]

22. Big endian: high-order byte at low address; little endian: low-order byte at low address.[3-assembly.pdf, slide 29]

Section4: CPU & Datapath Design

23. PC Insn Mem Reg File ALU Data Mem Writeback[6-cpu.pdf, slides 2025]

24. Fetch, Decode, Execute[6-cpu.pdf, slide 17]

25. Control generates signals for muxes, writes, ALU ops.[6-cpu.pdf, slide 31]

26. R-type: destination is rd; I-type: destination is rt.[6-cpu.pdf, slide 2223]

27. Each instruction is 4 bytes. PC increments by 4 to point to next.[3-assembly.pdf, slide 9]

28. Sign extension ensures 16-bit immediates become 32-bit values.[6-cpu.pdf, slide 23]

Section5: Cache & Memory Hierarchy

29. Hit rate = hits/accesses, etc.[7-caches.pdf, slide 17]

30. Temporal: reuse of same data. Spatial: accessing nearby data.[7-caches.pdf, slides 1415]

31. tavg = 1 + 0.05 * 100 = 6 ns[7-caches.pdf, slide 17]

32. Direct-mapped: simple, fast, but more conflict misses. Fully-associative: flexible, slower lookup.[7-caches.pdf, slides 29, 32]

33. 64KB = 2^16 bytes; block = 32B = 2^5 2^11 sets.[7-caches.pdf, slide 13]

34. On miss: load block from lower level, replace an existing one.[7-caches.pdf, slide 43]

35. Write-back defers write to memory until block eviction. Write-through writes immediately.[General knowledge, see 7-caches.pdf discussions of block replacement]

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36. Larger blocks fewer compulsory misses, but higher miss penalty.[7-caches.pdf, slide 12]

37. Compulsory, Capacity, Conflict misses.[7-caches.pdf, slide 14]

38. Stores recently evicted blocks to avoid miss penalties.[7-caches.pdf, not explicit, implied in design enhancements]

39. TLBs translate VA to PA for indexing physical caches.[8-vmem.pdf, slide 40]

40. Index with bits unaffected by address translation; tag is physical.[8-vmem.pdf, slide 41]

Section6: Virtual Memory

41. It gives processes the illusion of large contiguous memory.[8-vmem.pdf, slide 24]

42. VPN = upper bits of VA; PPN = upper bits of PA.[8-vmem.pdf, slide 33]

43. Page table maps VPN PPN or indicates not present.[8-vmem.pdf, slide 36]

44. TLB caches recent translations to reduce access latency.[8-vmem.pdf, slide 38]

45. Page fault: OS loads page from disk, updates PT.[8-vmem.pdf, slide 36]

46. Multi-level PTs reduce memory usage by sharing levels.[8-vmem.pdf, slide 37]

47. Cache uses PA; translation must happen before access.[8-vmem.pdf, slide 40]

48. Set index bits must be invariant under translation for VIPT caches.[8-vmem.pdf, slide 41]

Section7: Multicore, Pipelining, and I/O

49. Challenges: race conditions, synchronization, load balancing.[11-multicore.pdf, slide 6]

50. Deeper pipelines increase branch penalty and may not improve throughput due to hazards.[10-pipelining.pdf, slides 4, 1819]