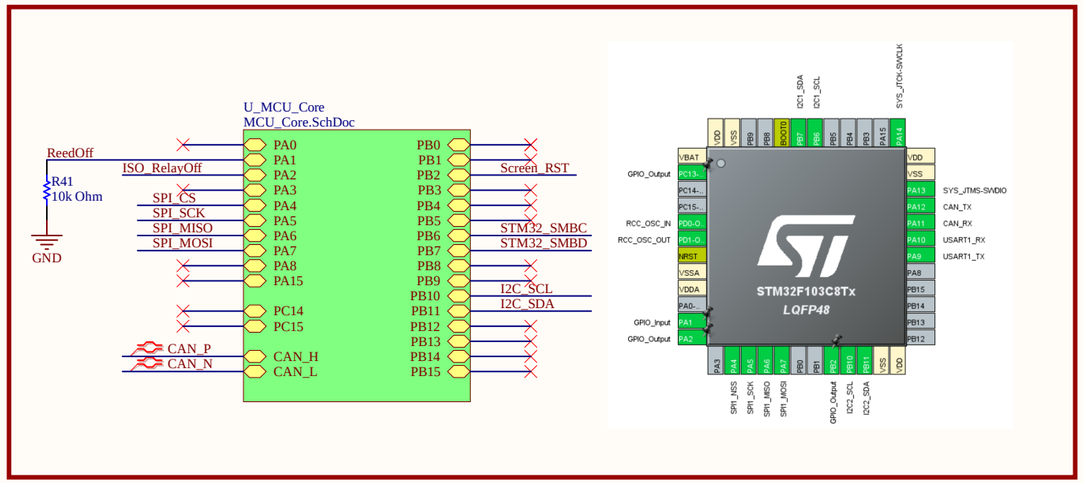
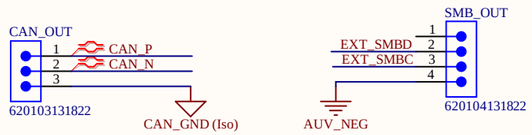
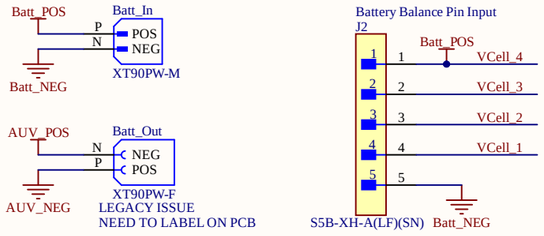
# MCU



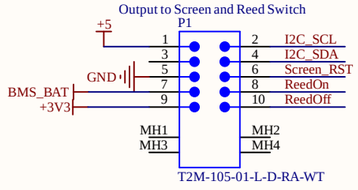

# External Comms Connector



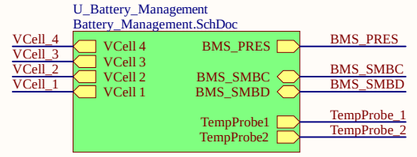

# Power In/Out and Balance Pins




# Screen and Reed Switches



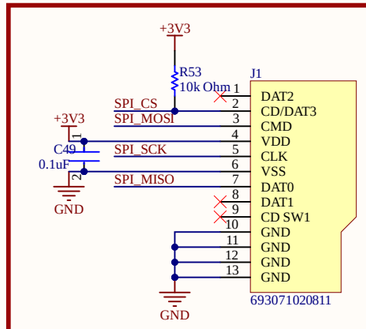

While old PMB has GND connected to Pin 3, Pin 5 was actually used as MCU_GND was shorted to Pin 5



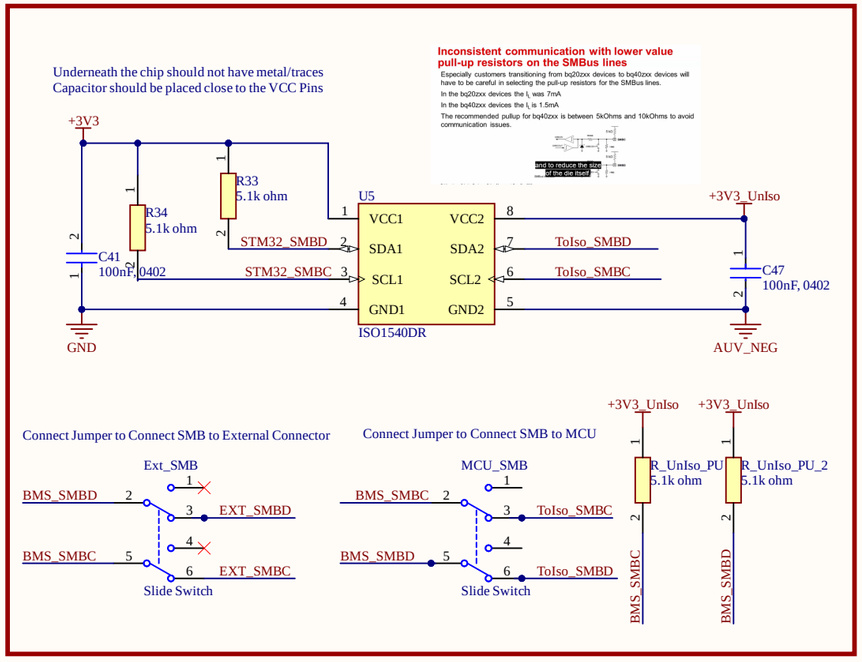


Power Ports
Batt_POS, Bat_NEG -> Input from Battery
AUV_POS, AUV_NEG -> Output after BQ40Z50
+3V3 -> Isolated 3V3 from Isolated 5V
+5V -> Isolated 5V from AUV_POS
+3V3_UnIso -> Unisolated 3V3 from AUV_POS
CAN_GND (Iso) -> Isolated CAN GND

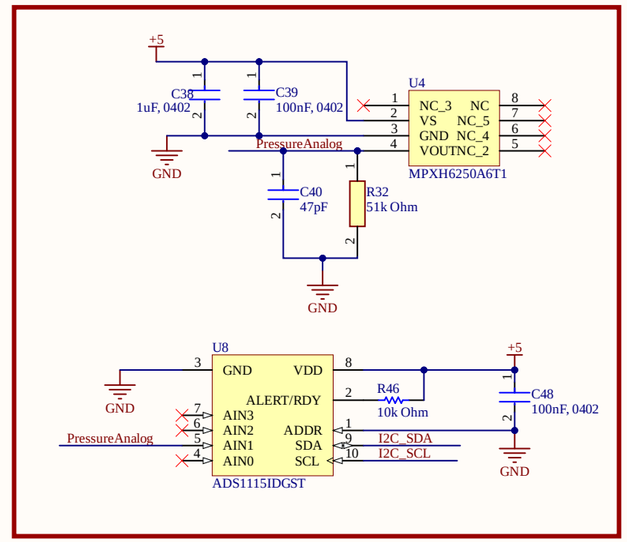
# SDCard Reader



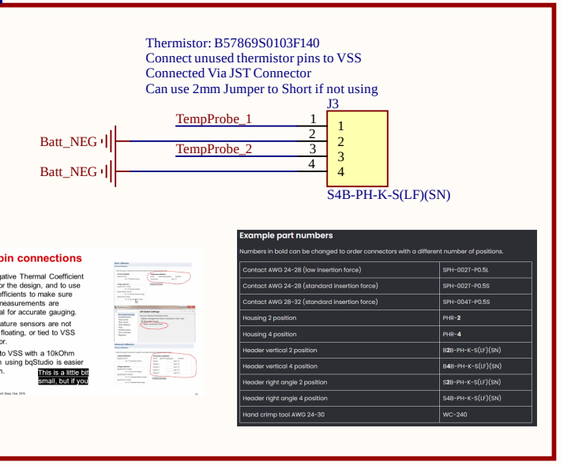

# SMBus




# Pressure Sensor




# Temp Probe Connector

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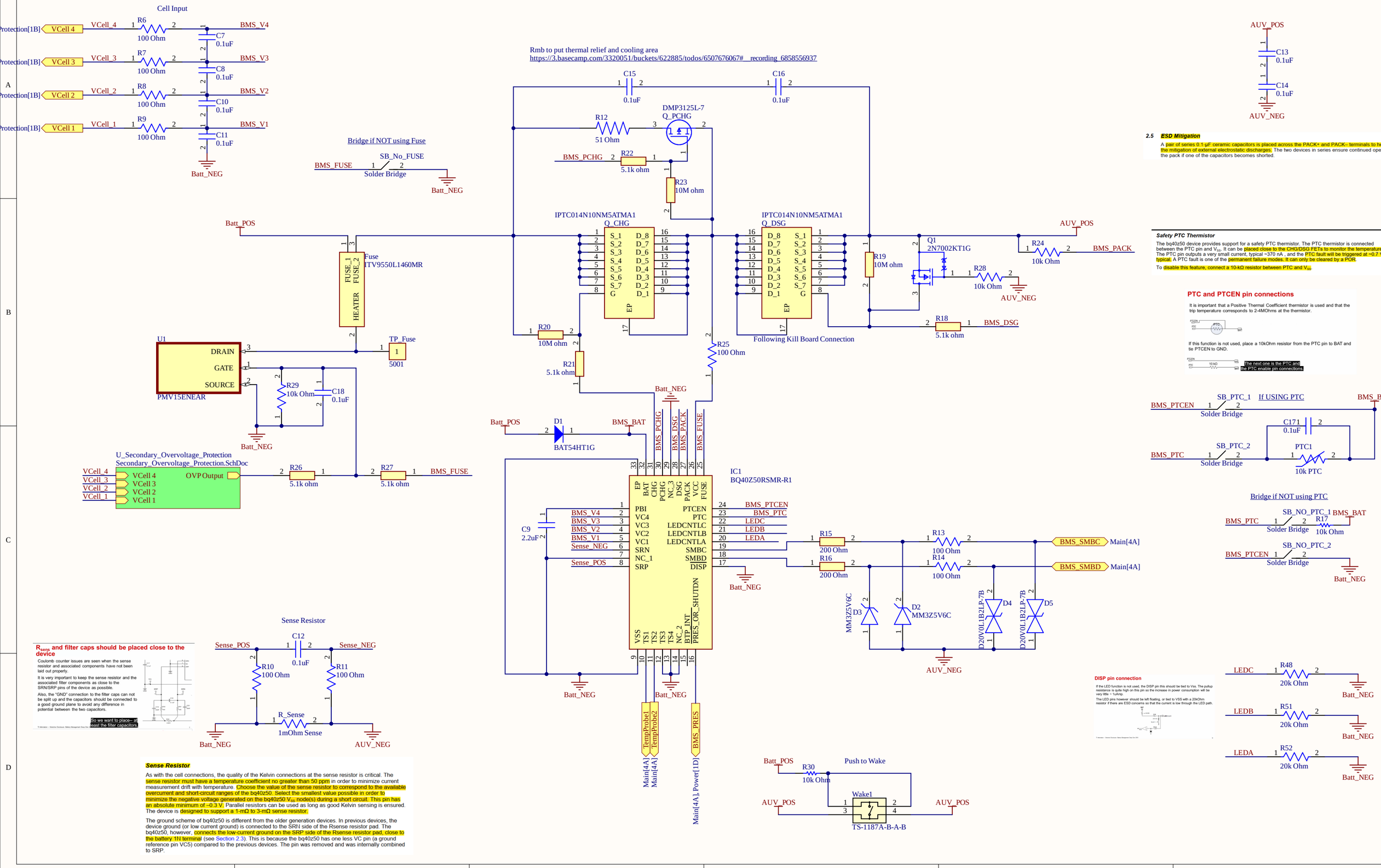
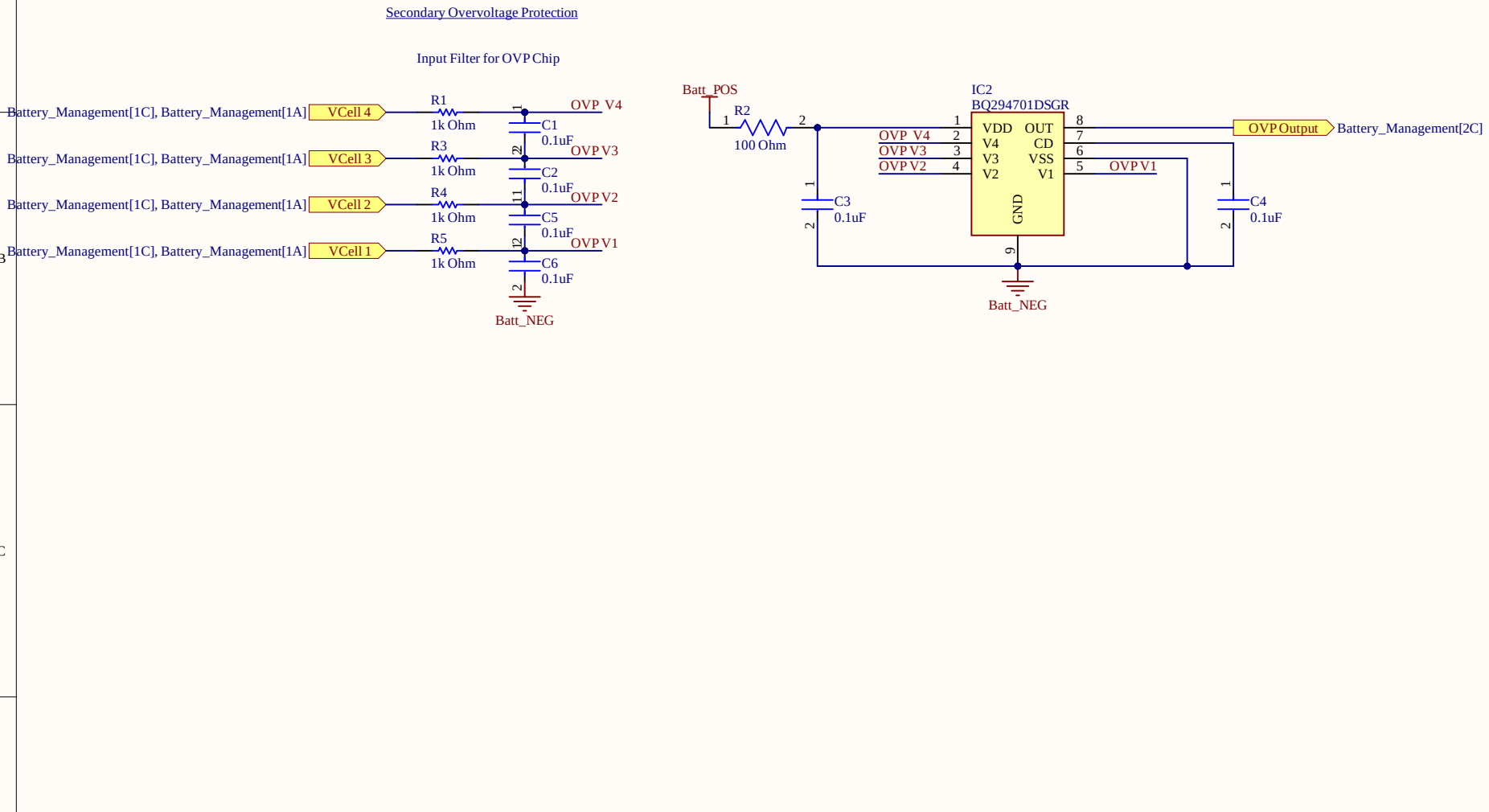

Cell Input
VCell_4
VCell_3
VCell_2
VCell_1
R6
R7
R8
R9
100 Ohm
C7
C8
C10
C11
0.1uF
BMS_V4
BMS_V3
BMS_V2
BMS_V1
Batt_NEG
Rmb to put thermal relief and cooling area
https://3.basecamp.com/3320051/buckets/622885/todos/6507676067#__recording_6858556937
C15
C16
DMP3125L-7
Q_PCHG
R12
51 Ohm
BMS_PCHG
R22
5.1k ohm
R23
10M ohm
Bridge if NOT using Fuse
SB_No_FUSE
BMS_FUSE
Solder Bridge
IPTC014N10NM5ATMA1
Q_CHG
Q_DSG
Batt_POS
Fuse
ITV9550L1460MR
FUSE_1
FUSE_2
HEATER
TP_Fuse
5001
U1
DRAIN
GATE
SOURCE
PMV15ENEAR
R29
10k Ohm
C18
0.1uF
R20
10M ohm
R21
5.1k ohm
R25
100 Ohm
R19
10M ohm
Following Kill Board Connection
Q1
2N7002KT1G
R28
10k Ohm
R18
5.1k ohm
BMS_DSG
AUV_POS
R24
10k Ohm
BMS_PACK
AUV_NEG
U_Secondary_Overvoltage_Protection
Secondary_Overvoltage_Protection.SchDoc
VCell 4
VCell 3
VCell 2
VCell 1
OVP Output
R26
5.1k ohm
R27
5.1k ohm
BMS_FUSE
D1
BAT54HT1G
IC1
BQ40Z50RSMR-R1
BMS_PCHG
BMS_DSG
BMS_PACK
BMS_FUSE
TempProbe1
TempProbe2
BMS_PRES
C9
2.2uF
BMS_PTCEN
BMS_PTC
LEDC
LEDB
LEDA
R15
200 Ohm
R16
200 Ohm
R13
100 Ohm
R14
100 Ohm
BMS_SMBC
BMS_SMBD
Main[4A]
D3
MM3Z5V6C
D2
MM3Z5V6C
D4
D20V0L1B2LP-7B
D5
D20V0L1B2LP-7B
Sense Resistor
C12
0.1uF
Sense_POS
Sense_NEG
R10
100 Ohm
R11
100 Ohm
R_Sense
1mOhm Sense
Push to Wake
R30
10k Ohm
Wake1
TS-1187A-B-A-B
AUV_POS
AUV_NEG
C13
C14
0.1uF
2.5 ESD Mitigation
A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.
Safety PTC Thermistor
The bq40z50 device provides support for a safety PTC thermistor. The PTC thermistor is connected between the PTC pin and V_SS. It can be placed close to the CHG/DSG FETs to monitor the temperature. The PTC pin outputs a very small current, typical ~370 nA , and the PTC fault will be triggered at ~0.7 V typical. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.
To disable this feature, connect a 10-kΩ resistor between PTC and V_SS.
PTC and PTCEN pin connections
It is important that a Positive Thermal Coefficient thermistor is used and that the trip temperature corresponds to 2-4MOhms at the thermistor.
If this function is not used, place a 10kOhm resistor from the PTC pin to BAT and tie PTCEN to GND.
The next one is the PTC and the PTC enable pin connections
BMS_BAT
SB_PTC_1
If USING PTC
C17
0.1uF
SB_PTC_2
PTC1
10k PTC
Bridge if NOT using PTC
SB_NO_PTC_1
SB_NO_PTC_2
R17
10k Ohm
DISP pin connection
If the LED function is not used, the DISP pin this should be tied to Vss. The pullup resistance is quite high on this pin so the increase in power consumption will be very little ~ 1uAmp.
The LED pins however should be left floating, or tied to VSS with a 20kOhm resistor if there are ESD concerns so that the current is low through the LED path.
R48
R51
R52
20k Ohm
R_sense and filter caps should be placed close to the device
Coulomb counter issues are seen when the sense resistor and associated components have not been laid out properly.
It is very important to keep the sense resistor and the associated filter components as close to the SRN/SRP pins of the device as possible.
Also, the "GND" connection to the filter caps can not be split up and the capacitors should be connected to a good ground plane to avoid any difference in potential between the two capacitors.
So we want to place– at least the filter capacitors
Sense Resistor
As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq40z50. Select the smallest value possible in order to minimize the negative voltage generated on the bq40z50 V_SS node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.
The ground scheme of bq40z50 is different from the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the Rsense resistor pad. The bq40z50, however, connects the low-current ground on the SRP side of the Rsense resistor pad, close to the battery TN terminal (see Section 2.3). This is because the bq40z50 has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

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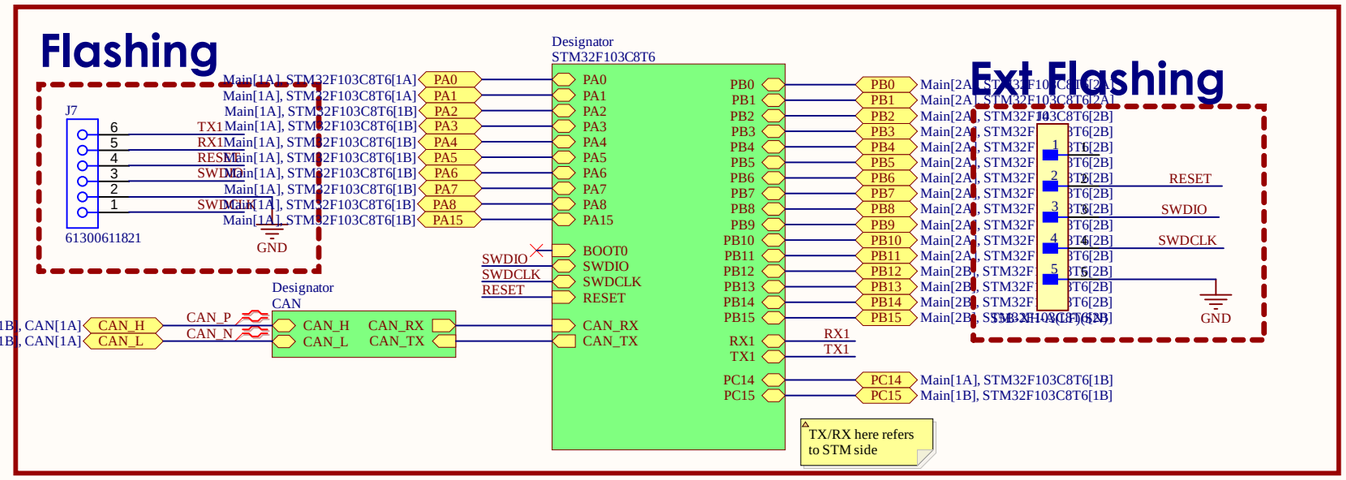
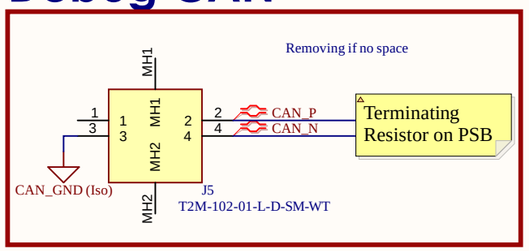
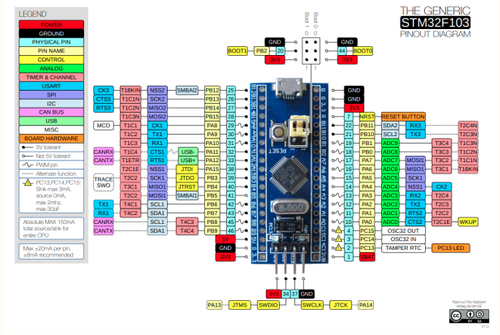
# STM32 / CAN

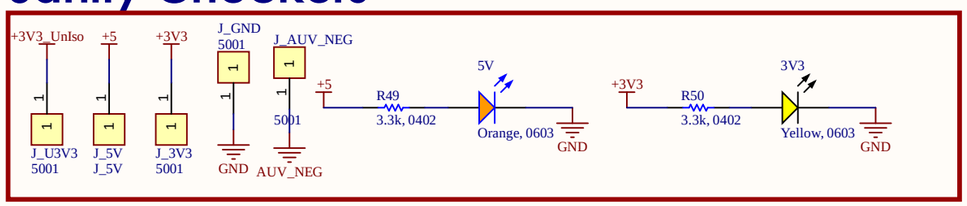



# Debug CAN




# Sanity Checkers

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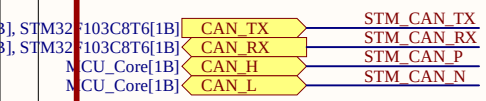
MCU_Core.SchDoc

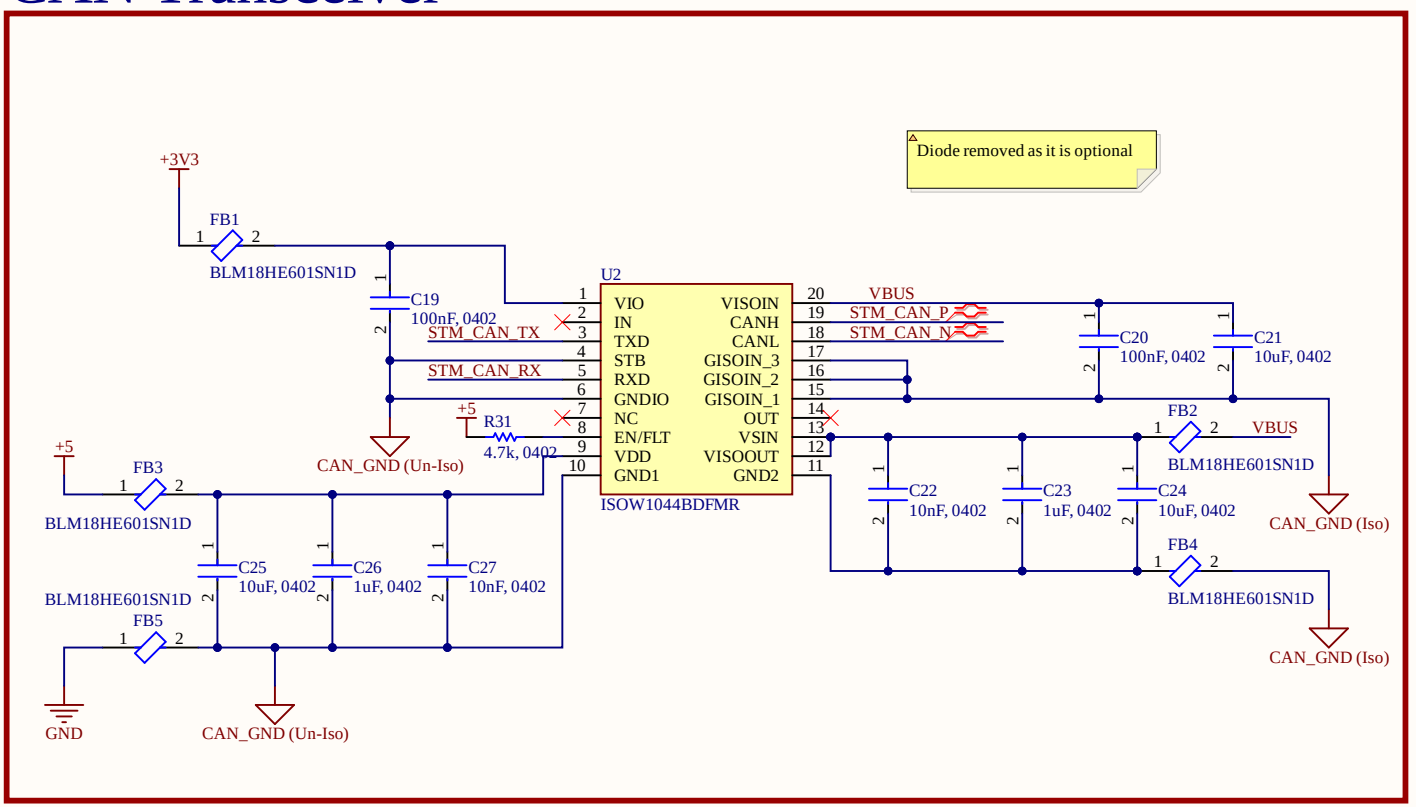
# Ports



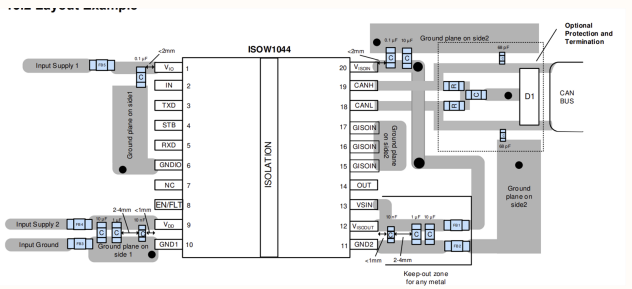

# Termination

Terminating Resistor on ESC Backplane

# CAN Transceiver




# Please follow the layout




**13 Layout**

**13.1 Layout Guidelines**

Figure 11-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to achieve low emissions design:

1. High frequency bypass capacitors 10 nF must be placed close to $V_{DD}$ and $V_{ISOOUT}$ pins, within 1 mm distance away from device pins. This is very essential for optimised radiated emissions performance. Ensure that these capacitors are 0402 size so that they offer least inductance (ESL).
2. Bulk capacitors of atleast 10 μF must be placed on power converter input ($V_{DD}$) and output ($V_{ISOOUT}$) supply pins after the 10 nF capacitor with a distance of 2 - 4 mm, as shown in Layout Example.
3. Traces on $V_{DD}$ and GND1 must be symmetric till bypass capacitors. Similarly traces on $V_{ISOOUT}$ and GND2 must be symmetric.
4. Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on power supply pins, one between $V_{ISOOUT}$ and $V_{ISOIN}$ and the other between GND2 (pin 11) and GND2(pin 15), as shown in example PCB layout, so that any high frequency noise from power converter output sees a high impedance before it goes to other components on PCB.
5. Do not have any metal traces or ground pour within 4 mm of power converter output terminals $V_{ISOOUT}$ (pin12) and GND2 (pin11).
6. Place the CAN BUS protection and filtering circuitry close to the bus connector to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows two optional 68pF bus filter capacitors
7. Common mode choke or ferrite beads on bus terminals (CANH/CANL) can minimise any high frequency noise that can couple of CAN bus cable which can act as antenna and amplify that noise. This will improve Radiated emissions performance on a system level.
8. Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design. EVM Link is available in Related Documentation.

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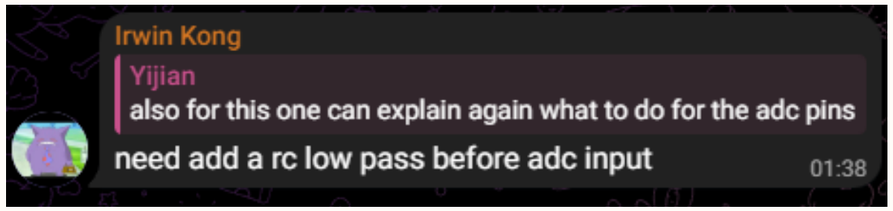
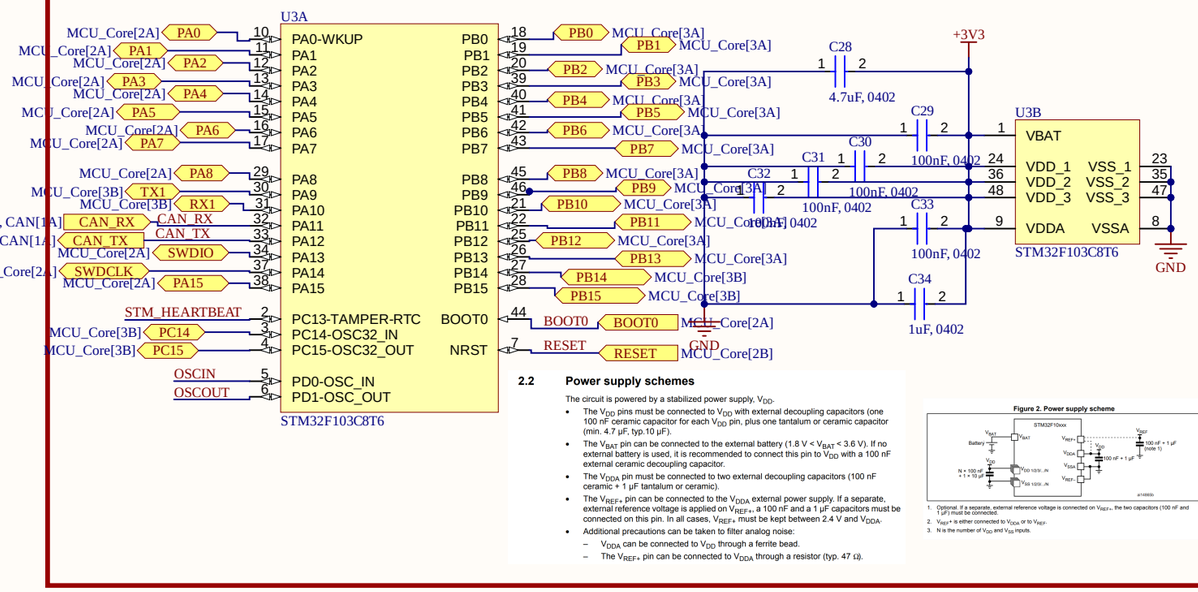
# MCU




### 2.2 Power supply schemes

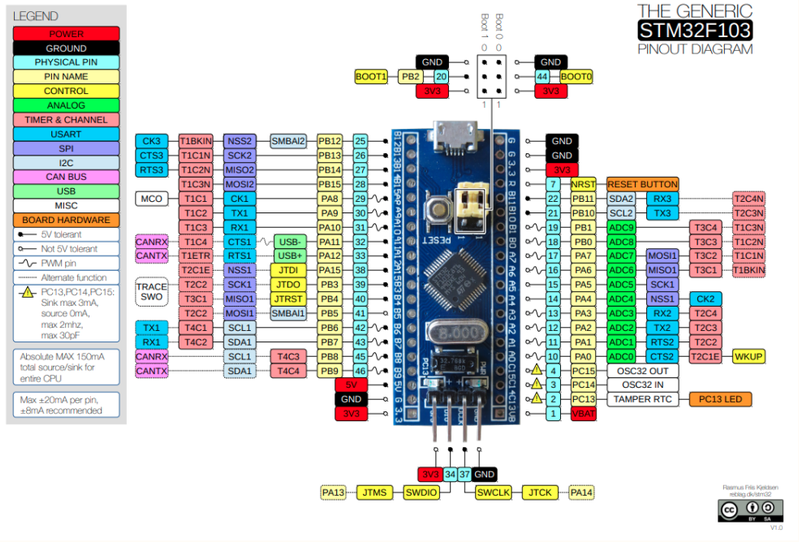
The circuit is powered by a stabilized power supply, $V_{DD}$.

- The $V_{DD}$ pins must be connected to $V_{DD}$ with external decoupling capacitors (one 100 nF ceramic capacitor for each $V_{DD}$ pin, plus one tantalum or ceramic capacitor (min. 4.7 µF, typ.10 µF).
- The $V_{BAT}$ pin can be connected to the external battery (1.8 V < $V_{BAT}$ < 3.6 V). If no external battery is used, it is recommended to connect this pin to $V_{DD}$ with a 100 nF external ceramic decoupling capacitor.
- The $V_{DDA}$ pin must be connected to two external decoupling capacitors (100 nF ceramic + 1 µF tantalum or ceramic).
- The $V_{REF+}$ pin can be connected to the $V_{DDA}$ external power supply. If a separate, external reference voltage is applied on $V_{REF+}$, a 100 nF and a 1 µF capacitors must be connected on this pin. In all cases, $V_{REF+}$ must be kept between 2.4 V and $V_{DDA}$.
- Additional precautions can be taken to filter analog noise:
  - $V_{DDA}$ can be connected to $V_{DD}$ through a ferrite bead.
  - The $V_{REF+}$ pin can be connected to $V_{DDA}$ through a resistor (typ. 47 Ω).

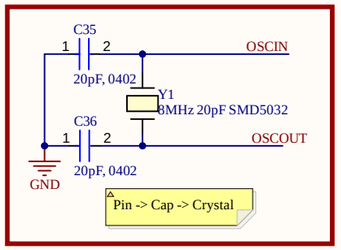
**Figure 2. Power supply scheme**

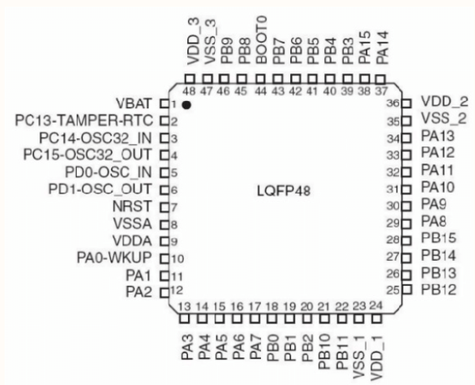


1. Optional. If a separate, external reference voltage is connected on $V_{REF+}$, the two capacitors (100 nF and 1 µF) must be connected.
2. $V_{REF+}$ is either connected to $V_{DDA}$ or to $V_{REF-}$.
3. N is the number of $V_{DD}$ and $V_{SS}$ inputs.

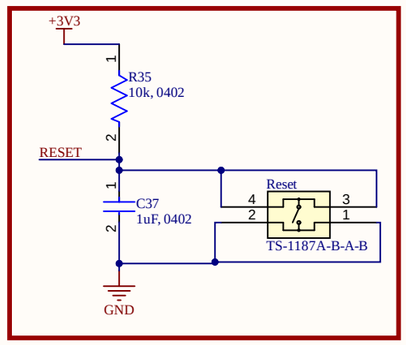



# Crystal

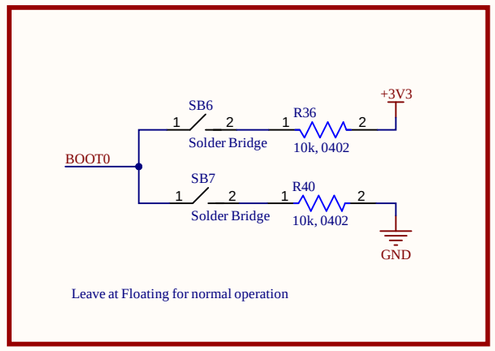


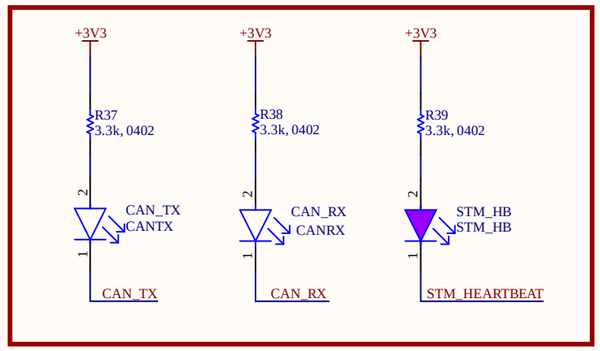

# Reset




# Boot



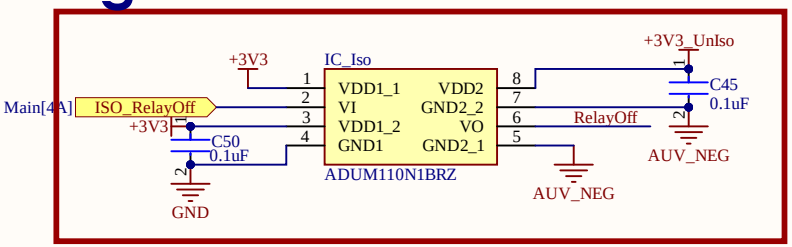

# LED Indicators



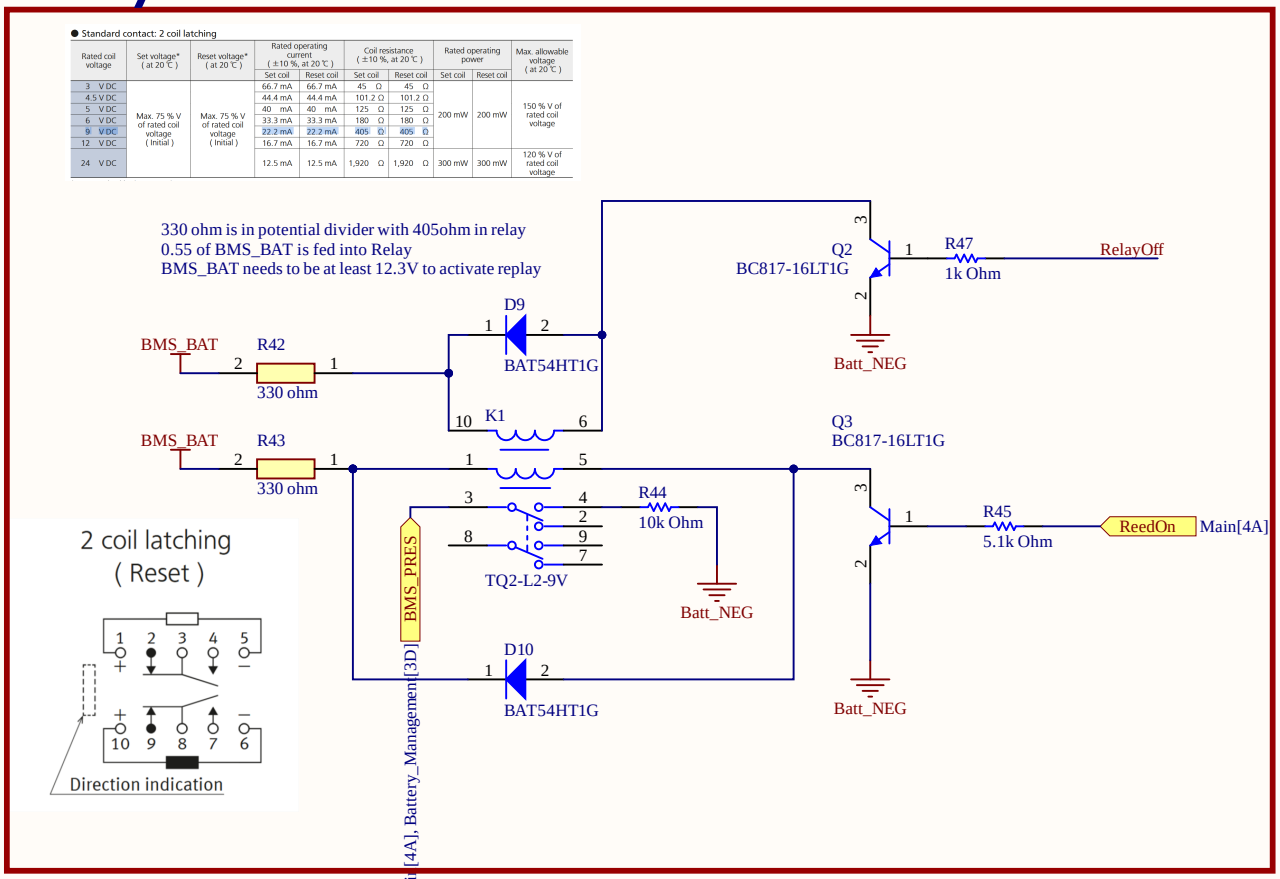

# Blue Pill

The STM32 will receive ReedOff and send out a signal through the isolator to reset the Relay
This allows the STM to stop stuff first before being powered down
E.g.: Closing File on SDCard

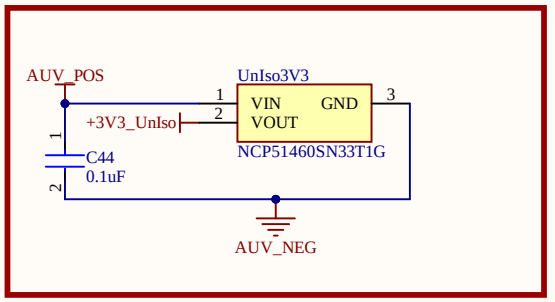
# Signal Isolator



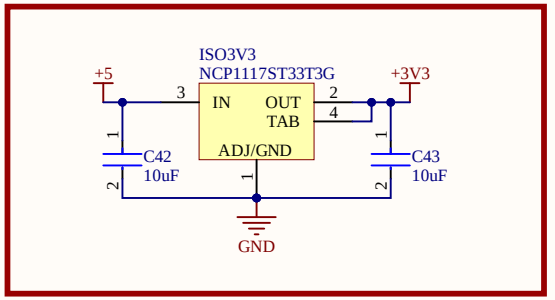

# Relay Circuit



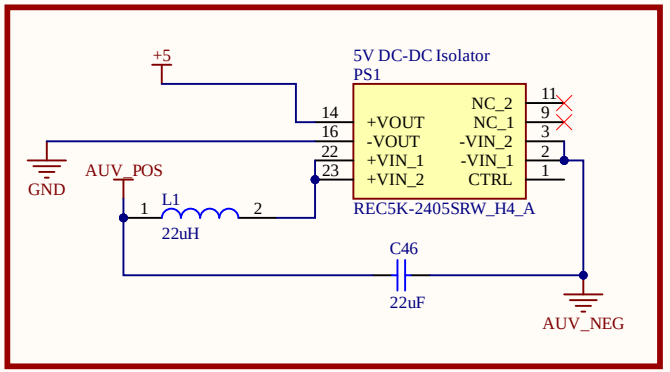

# UnIso 3V3




# Isolated 3V3




# Isolated 5V

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