PROJECT REPORT
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I. INTRODUCTION

This project mainly dealt with integrating a cache hierarchy together with the MIPS pipeline. An instruction cache and data cache is implemented. The instruction cache is a 32KB direct mapped cache with a block size of 32B while the data cache is 32KB two way set associative cache with a block size of 32B. The figure below shows a flowchart describing the cache write/read process implemented in the processor.

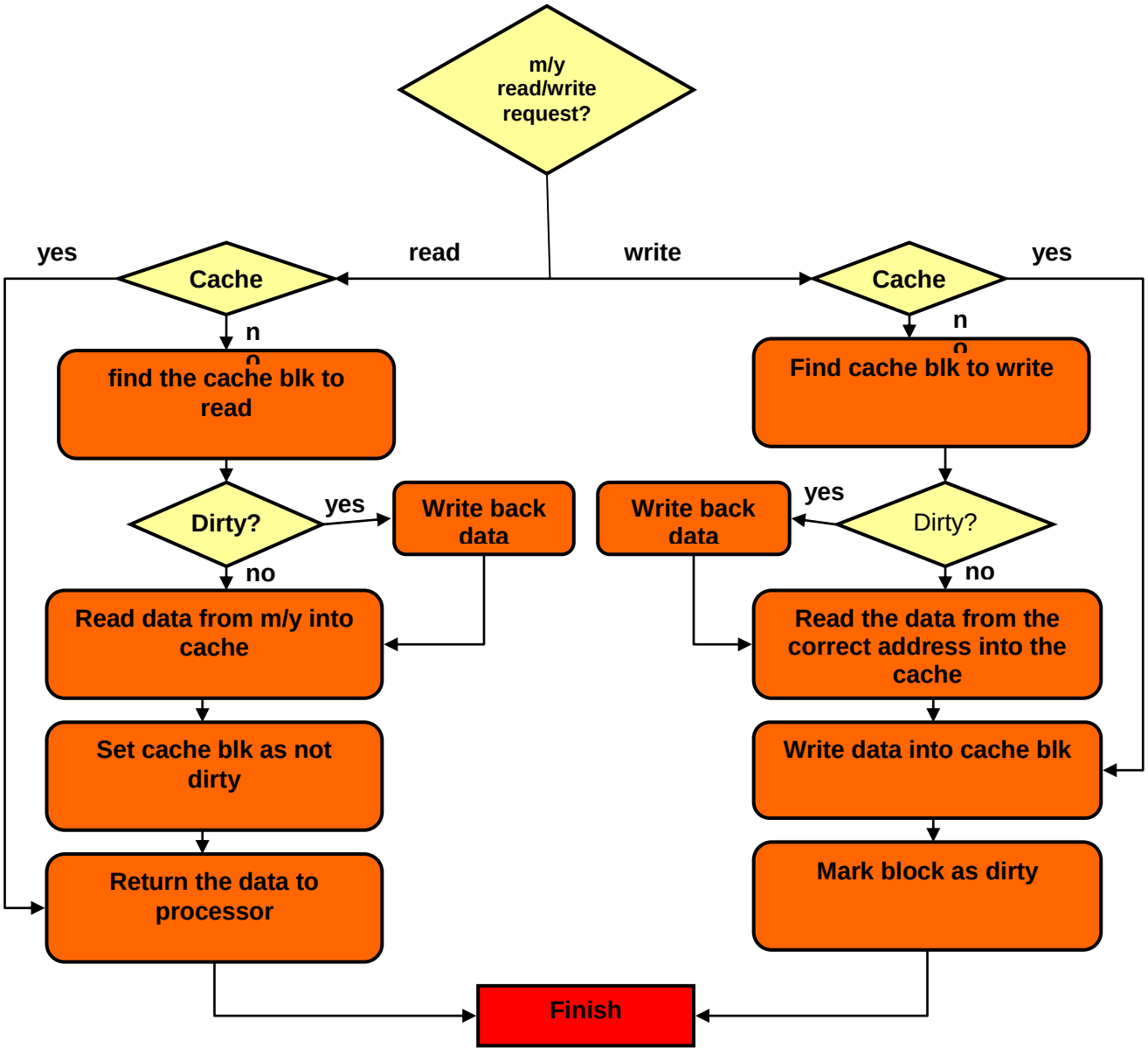

Figure1. Flow chart of cache read/write process

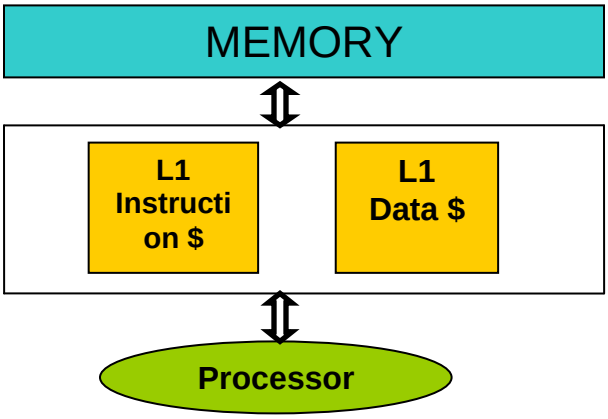

Figure2. Block diagram of the memory hierarchy

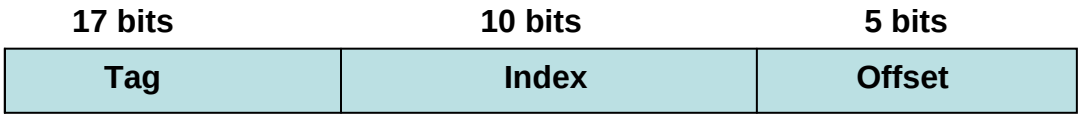

Figure3. Instruction Cache fields

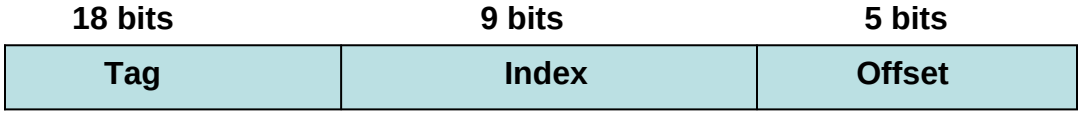

Figure4. Data Cache fields

II. IMPLEMENTATION DETAILS

- As mentioned above, a verilog module CACHE.v is implemented based on the mechanism described in figure1. This module has both the instruction and data caches.
- While implementing the data cache, one of the main problems encountered was during syscalls. The sim_main.cpp file was modified to make the syscalls access memory via the cache and not directly so as to avoid fetching stale data.
- If there is a cache miss, the pipeline is stalled (so in addition to the access time it would have to be stalled for 10 penalty cycles).
- Writing data into the memory and from the memory into the cache is done in the sim_main.cpp file.

III. RESULTS

The simulation results with the L1 data and L1 instruction cache:

a) noio :

Simulation time : 1 sec

Total cycles: 4006
Total instructions: 2116
IPC: 0.528208

b) hello:

WriteToFile at time:112293
Hello World
Exit at time:115321
****
Simulation time : 11 sec
Total cycles: 115321
Total instructions: 97148
IPC: 0.842414

c) fib18

WriteToFile at time:343728
Fibonacci 18 is: 2584
Exit at time:346731
****
Simulation time : 39 sec
Total cycles: 346731
Total instructions: 307191
IPC: 0.885963

d) class

WriteToFile at time:114237
Rectangle(3,4) area is: 12
Exit at time:117253
****
Simulation time : 12 sec
Total cycles: 117253
Total instructions: 98614
IPC: 0.841036

e)fact12

Compute factorial 12:

1

2

6

24

120

720

5040

40320

362880

3628800

39916800

479001600

Munmap at time:133587
Exit at time:133743
****
Simulation time : 13 sec
Total cycles: 133743
Total instructions: 112950
IPC: 0.84453

f)Hanoi

Moving 1 from 1 to 3

Moving 2 from 1 to 2

Moving 1 from 3 to 2

Moving 3 from 1 to 3

Moving 1 from 2 to 1

Moving 2 from 2 to 3

Moving 1 from 1 to 3

Moving 4 from 1 to 2

Moving 1 from 3 to 2

Moving 2 from 3 to 1

Moving 1 from 2 to 1

Moving 3 from 3 to 2

Moving 1 from 1 to 3

Moving 2 from 1 to 2

Moving 1 from 3 to 2

Moving 5 from 1 to 3

Moving 1 from 2 to 1

Moving 2 from 2 to 3

Moving 1 from 1 to 3

Moving 3 from 2 to 1

Moving 1 from 3 to 2

Moving 2 from 3 to 1

Moving 1 from 2 to 1

Moving 4 from 2 to 3

Moving 1 from 1 to 3

Moving 2 from 1 to 2

Moving 1 from 3 to 2

Moving 3 from 1 to 3

Moving 1 from 2 to 1

Moving 2 from 2 to 3

Moving 1 from 1 to 3

Munmap at time:242525

Exit at time:242675
****
Simulation time : 23 sec
Total cycles: 242675
Total instructions: 204294
IPC: 0.841842

g)ical

WriteToFile at time:250172
Result is: 15277824
Exit at time:253186
****
Simulation time : 51 sec
Total cycles: 253186
Total instructions: 217923
IPC: 0.860723

h)matrix

M1=

1 1 1

0 1 1

0 0 1

M2=

2 0 3

0 1 2

1 1 1

M1 + M2 =

3 1 4

0 2 3

1 1 2

M1 * M2 =

3 2 6

1 2 3

1 1 1

Munmap at time:166026
Exit at time:166176
****
Simulation time : 16 sec
Total cycles: 166176
Total instructions: 139647
IPC: 0.840356

i)sort

3 4 7 12 17 23 45 78 90 101

Munmap at time:125462
Munmap at time:127788
Exit at time:127938
****
Simulation time : 13 sec
Total cycles: 127938
Total instructions: 107008
IPC: 0.836405

j)file

Exit at time:116537
****
Simulation time : 11 sec
Total cycles: 116537
Total instructions: 97333
IPC: 0.835211

Created a file out.txt:
##########
ECE201/401
##########