phyCORE-LPC2292/94

Hardware Manual

Edition September 2004

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Preface

This phyCORE-LPC2292/94 Hardware Manual describes the board's design and functions. Precise specifications for the Philips LPC2292/94 microcontroller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-LPC2292/94

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-LPC2292/94 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit as well as selected 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-LPC2292/94 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-LPC2292/94 is a subminiature (60 x 53 mm) insert-ready Single Board Computer populated with the Philips LPC2292/94 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the Philips LPC2292/94. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-LPC2292/94.

The phyCORE-LPC2292/94 offers the following features:

- subminiature Single Board Computer (60 x 53 mm) achieved through modern SMD technology
- populated with the Philips LPC2292/94 microcontroller (TQPF-144 packaging)
- improved interference safety achieved through multi-layer PCB technology and dedicated Ground pins
- controller signals and ports extend to two 100-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- 32-bit, demultiplexed bus mode
- max. 60 MHz clock frequency (ca. 50 ns instruction cycle, extern; ca. 10 ns internal Flash)
- 1.5 Gbyte external address space
- 2 MByte (up to 16 MByte) on-board Flash[1]
- on-board Flash programming, no dedicated Flash programming voltage required through use of 3.3 V Flash devices
- 1 MByte (up to 8 MByte) RAM on-board, max. 2 MByte at 0 wait states[1]
- up to two CAN transceivers (Infineon TLE6250V33)
- RS-232 transceiver for two serial interfaces
- optional SMSC 91C111 Ethernet controller with EEPROM
- 2 kByte (up to 8 kByte) SPI-EEPROM[1]
- I^2C Real-Time Clock with internal quartz (can be battery buffered)
- up to two free microcontroller Chip Select signals (if optional Ethernet controller is not populated)

[1] : Please contact PHYTEC for more information about additional module configurations.

- up to 6 freely programmable Chip Select signals from on-board CPLD device (requires changing the default CPLD code[1])
- one operating voltage for core & peripherals, 3.3 V, typ. < 280 mA (with maximum circuitry installed at 60 MHz CPU frequency)
- controller 1.8 V core voltage generated on-board
- additional 5 V operating voltage for CAN transceivers, typ. <12 mA
- support of LPC2292/2294 single chip mode
- support of ETM debug interface (only on debugCORE version)

[1] : Please contact PHYTEC if you have questions about changing the CPLD code.

1.1 Block Diagram

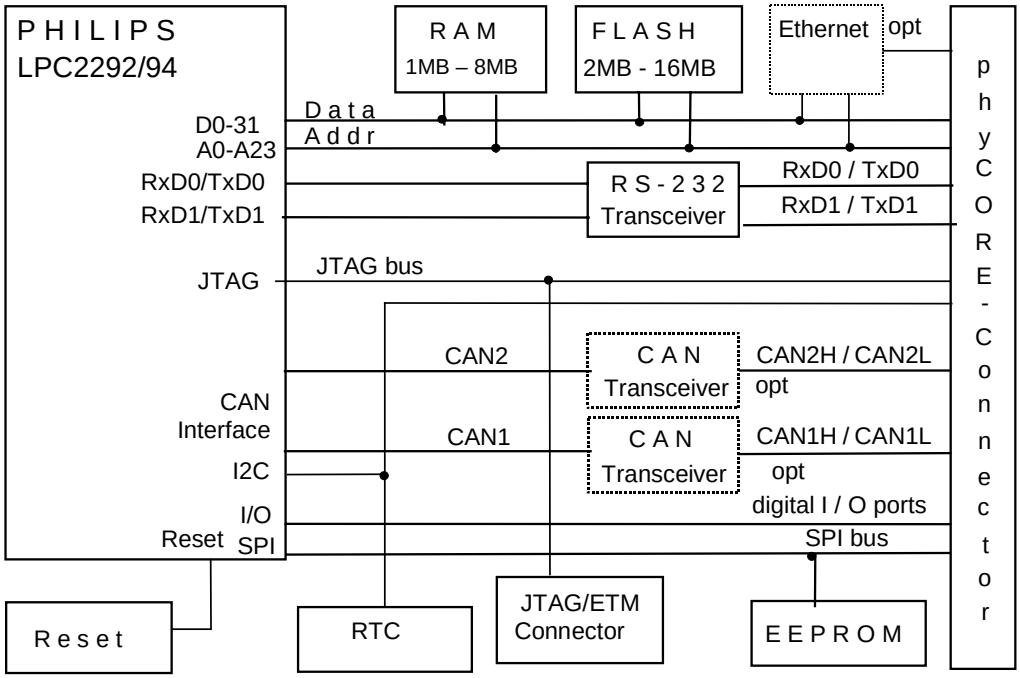


Figure 1: Block Diagram phyCORE-LPC2292/94

1.2 View of the phyCORE-LPC2292/94

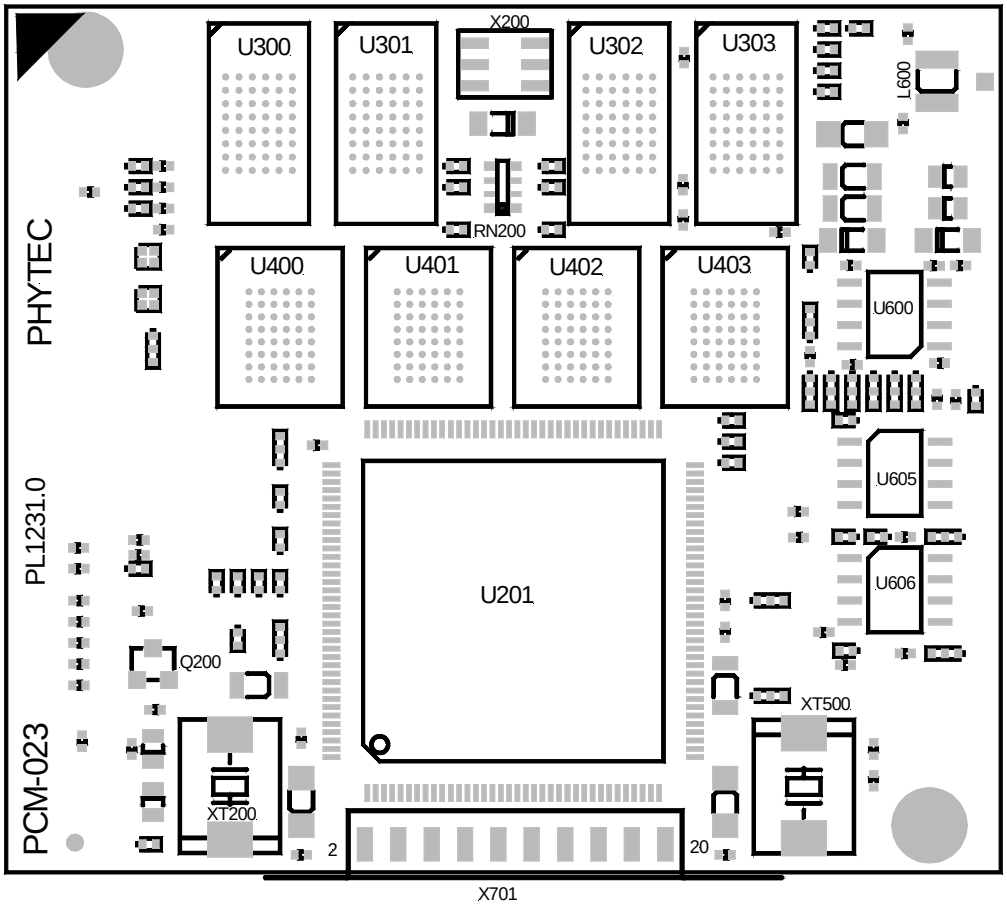


Figure 2: Top View of the phyCORE-LPC2292/94

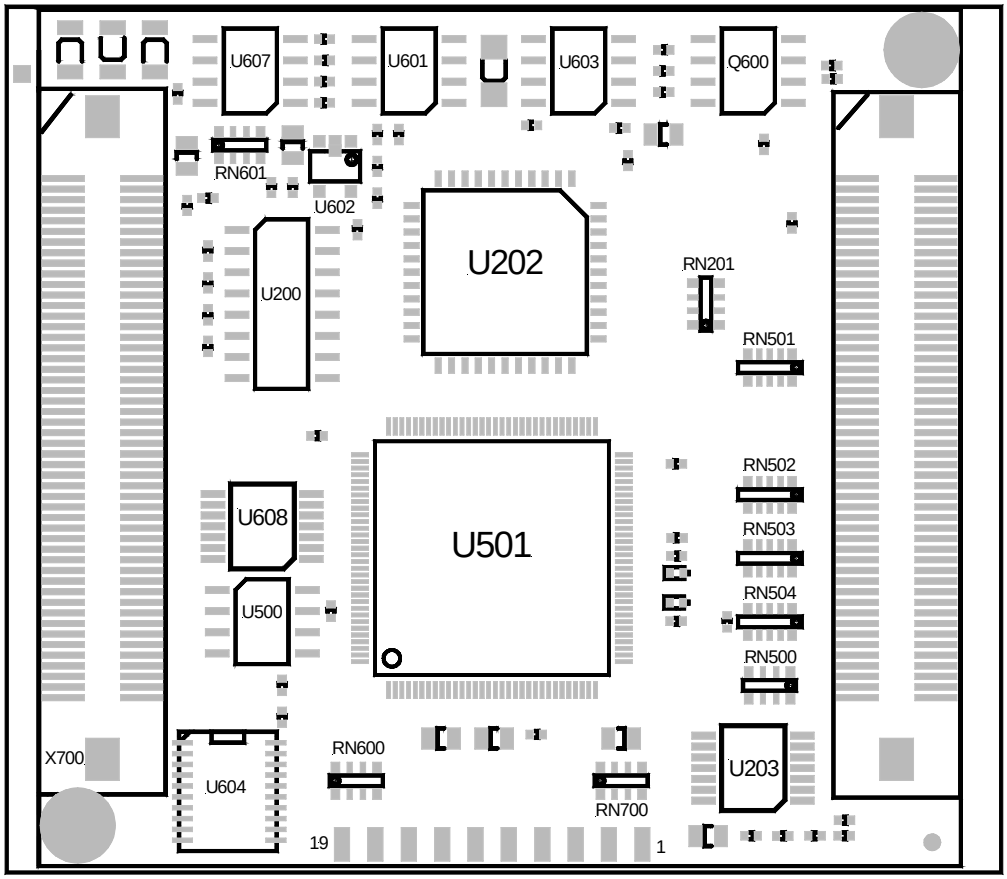


Figure 3: Bottom View of the phyCORE-LPC2292

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-LPC2292/94 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-LPC2292/94 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-LPC2292/94 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-LPC2292/94 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a crossview of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module's PCB.

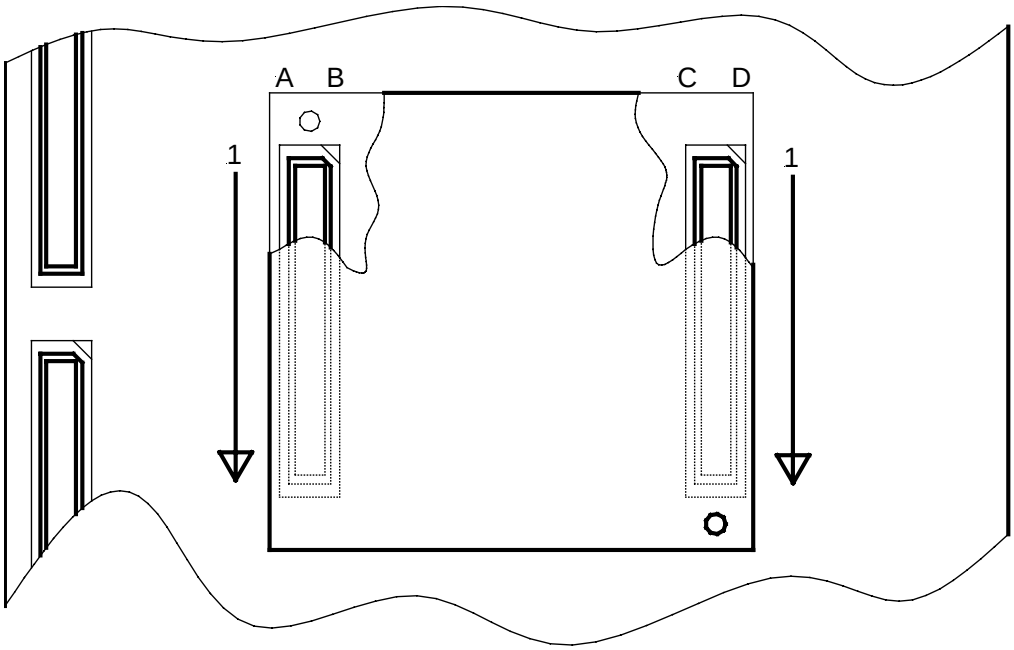


Figure 4: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Many of the controller port pins accessible at the connectors along the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Philips phyCORE-LPC2292/94 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Description
Pin Row X1A			
1A	CLKIN	I	Optional external clock generator (only in if capacitor C210 is populated)
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A	GND	-	Ground 0 V
3A	P014	I/O	Port 014 of the microcontroller *(see data sheet)* (alternative: external interrupt 1 input)
4A	P020	I/O	Port 020 of the microcontroller *(see data sheet)* (alternative: external interrupt 3 input)
5A	/CS0	O	Chip Select #0
6A	/CS2	O	Chip Select #2
8A	/WE	O	/WR signal of the microcontroller
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23	O	Address line of the microcontroller
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A 39A, 40A, 41A, 43A, 44A, 45A, 46A	D1, D2, D4, D7, D9, D10, D12, D15, D17, D19, D20, D22, D25, D27, D28, D30	I/O	Data line of the microcontroller
34A	/BLS0	O	Low active Byte Lane Select signal (Bank0)
35A	FSO	I/O	Freely programmable PLD signal (may be used as additional Chip Select signal)
36A	/BLS2	O	Low active Byte Lane Select signal (Bank2)
48A, 49A, 50A	P03, P05, P06	I/O	Port 0 of the microcontroller (*see corresponding Data Sheet*)
Pin Row X1B			
1B	MCKO	O	CLKOUT system clock output (only available if Jumper J207 is populated)
2B	P016	I/O	Port 016 of the microcontroller *(see data sheet)* (alternative: external interrupt 0 input)
3B	P015	I/O	Port 015 of the microcontroller *(see data sheet)* (alternative: external interrupt 2 input)
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B	GND	-	Ground

Pin Number	Signal	I/O	Description
Pin Row X1B			
5B	/CS1	O	Chip Select #1
6B	/CS3	O	Chip Select #3
7B	/OE	O	Output enable signal of the microcontroller
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22	O	Address line of the microcontroller
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D0, D3, D5, D6, D8, D11, D13, D14, D16, D18, D21, D23, D24, D26, D29, D31	I/O	Data line of the microcontroller
33B	/BLS1	O	Low active Byte Lane Select signal (Bank1)
35B	FS1	I/O	Freely programmable PLD signal (may be used as additional Chip Select signal)
36B	/BLS3	O	Low active Byte Lane Select signal (Bank3)
47B, 48B, 50B	P02, P04, P07	I/O	Port 0 of the microcontroller (*see corresponding Data Sheet*)
Pin Row X1C			
1C, 2C	VCC	-	Voltage input +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C	GND	-	Ground 0 V
4C, 5C	VDD_V5V0	-	Voltage input +5 VDC
6C	VBAT	I	Battery input for back-up of RTC and optional buffering of RAM
8C	N.C.	-	Not connected
9C	BOOT	I	Boot input of the phyCORE module, switches controller into boot mode during reset
10C	/RESET	O	/RESET output of the phyCORE-LPC2292/94
11C	FS2	I/O	Freely programmable PLD signal (may be used as additional Chip Select signal)
13C	P010	I/O	Port P010 of the microcontroller *(see data sheet)*
14C	P012	I/O	Port P012 of the microcontroller *(see data sheet)*
15C	P013	I/O	Port P013 of the microcontroller *(see data sheet)*
16C	P018	I/O	Port P018 of the microcontroller *(see data sheet)*
Pin Row X1C			
18C	CAN_H2	I/O	Differential CANH line of second CAN transceiver (alternative: P024 if J603 populated and U606 not populated)
19C	P019	I/O	Port P019 of the microcontroller *(see data sheet)*
20C	/PWROFF	I	/PWROFF signal, low level on this pin disables the power supply of the module
21C	RxD1_ext	I	Input of the second serial interface of the phyCORE-LPC2292/94, RS-232 level

Pin Number	Signal	I/O	Description
Pin Row X1C			
23C	TxD1_ext	O	Output of the second serial interface of the phyCORE-LPC2292/94, RS-232 level
24C	P021	I/O	Port P021 of the microcontroller *(see data sheet)*
25C	P022	I/O	Port P022 of the microcontroller *(see data sheet)*
26C	/PCS0	I/O	SPI Chip Select 0 (for EEPROM U607)
28C	MOSI0	I/O	Master-Out/Slave-In (for EEPROM U607)
29C	P118	I/O	Port P118 of the microcontroller *(see data sheet)*
30C	P119	I/O	Port P119 of the microcontroller *(see data sheet)*
31C	SCL	I/O	I^2C clock line (for RTC)
33C	/LAN_LED_A	O	LINK LED output for Ethernet interface
34C	/LAN_LED_B	O	LAN LED output for Ethernet interface
35C	LAN_TPI-	I	Negative Rx input of the Ethernet interface
36C	LAN_TPO-	O	Negative Tx output of the Ethernet interface
38C	P128 (TDI)	I/O I	Port P128 of the microcontroller *(see data sheet)* (alternative: data input JTAG interface)
39C	P131 (/TRST)	I/O I	Port P131 of the microcontroller *(see data sheet)* (alternative: reset input JTAG interface)
40C	P129 (TCK)	I/O I	Port P129 of the microcontroller *(see data sheet)* (alternative: clock input JTAG interface)
41C	P122	I/O	Port P122 of the microcontroller, (alternative: PIPESTAT1 of TRACE port)
42C, 47C	AGND	-	Analog Ground of the microcontroller
43C	P125	I/O	Port P125 of the microcontroller, (alternative: EXTIN0 of TRACE port)
44C, 45C	FS4, FS5	I/O	Freely programmable PLD signal (may be used as additional Chip Select signal)
46C	TMS_PLD	I	JTAG Scan Chain TMS Signal from the PLD
48C, 49C, 50C	P030, P028, P027	I/O	Port P0 of the microcontroller, alternative: analog inputs AIN0, AIN1, AIN3
Pin Row X1D			
1D, 2D	VCC	-	Voltage input +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D	GND	--	Ground 0 V
4D, 5D, 7D	NC	-	Not connected. These contacts should remain unconnected on the target hardware side.
6D	VPD	O	Output of back-up voltage supply for buffering of external components
8D	WDI	I	MAX6301 Watchdog input
10D	/RESIN	I	/RESET input of the phyCORE-LPC2292/94
11D	TxD1	O	Output of the second serial interface, TTL level (alternative: port P08 of the microcontroller)
12D	RxD1	I	Input of the second serial interface, TTL level (alternative: port P09 of the microcontroller)
13D	P011	I/O	Port P011 of the microcontroller *(see data sheet)*
15D	P017	I/O	Port P017 of the microcontroller *(see data sheet)*

Pin Number	Signal	I/O	Description
Pin Row X1D			
16D	RxD0	I	Input of the first serial interface, TTL level (alternative: port P0.1 of the microcontroller)
17D	TxD0	O	Output of the first serial interface, TTL level (alternative: port P0.0 of the microcontroller)
18D	CAN_L2	I/O	Differential CANL line of the 2nd CAN transceiver (alternativ P023 if J605 populated and U606 not populated)
20D	CAN_L1	I/O	Differential CANL line of the first CAN transceiver (alternativ P025 if J604 populated and U605 not populated)
21D	CAN_H1	I/O	Differential CANH line of the first CAN transceiver (alternativ TD1 if J602 populated and U605 not populated)
22D	RxD0_ext	I	Input of the first serial interface, RS-232 level
23D	TxD0_ext	O	Output of the first serial interface, RS-232 level
25D	P116	I/O	Port P116 of the microcontroller *(see data sheet)*
26D	P117	I/O	Port P117 of the microcontroller *(see data sheet)*
27D	MISO0	I/O	Master-In/Slave-Out (for EEPROM)
28D	SCLK0	I/O	Clock input SPI interface (for EEPROM)
30D	P120	I/O	Port P120 of the microcontroller *(see data sheet)* (alternative: TRACESYNC of TRACE port)
31D	P121	I/O	Port P121 of the microcontroller *(see data sheet)* (alternative: PIPESTAT0 of TRACE port)
32D	SDA	I/O	I^2C data line (for RTC)
33D	/INT_RTC	O	RTC interrupt output (from RTC)
35D	LAN_TPI+	I	Positive Rx input of the Ethernet interface
36D	LAN_TPO+	O	Positive Tx output of the Ethernet interface
37D	P126 (RTCK)	I/O	Port P126 of the microcontroller *(see data sheet)* (alternative: RTCK of the JTAG interface)
38D	P127 (TDO)	I/O	Port P127 of the microcontroller *(see data sheet)* (alternative: Data output JTAG interface)
40D	P130 (TMS)	I/O	Port P130 of the microcontroller *(see data sheet)* (alternative: JTAG interface select input)
41D	P123	I/O	Port P123 of the microcontroller *(see data sheet)* (alternative: PIPESTAT2 of TRACE port)
42D	P124	I/O	Port P124 of the microcontroller *(see data sheet)* (alternative: TRACECLK of TRACE port)
43D	FS3	I/O	Freely programmable PLD signal (may be used as additional Chip Select signal)
45D	TDI_PLD	I	JTAG Scan Chain TDI signal from the PLD
46D	TCK_PLD	I	JTAG Scan Chain TCK signal from the PLD
47D	TDO_PLD	O	JTAG Scan Chain TDO signal from the PLD
44D, 49D	VAGND	-	Analog Ground
48D	P029	I/O	Port P029 of the microcontroller *(see data sheet)*
50D	ADVREF	I	Reference voltage input for A/D converter

Table 1: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-LPC2292/94 has 50 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and *Figure 7* indicate the location of the jumpers on the board. With the exception of J619 and J620, all other solder jumpers are located at the top side (microcontroller side) of the module.

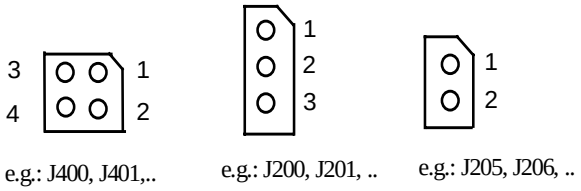


Figure 5: Numbering of the Jumper Pads

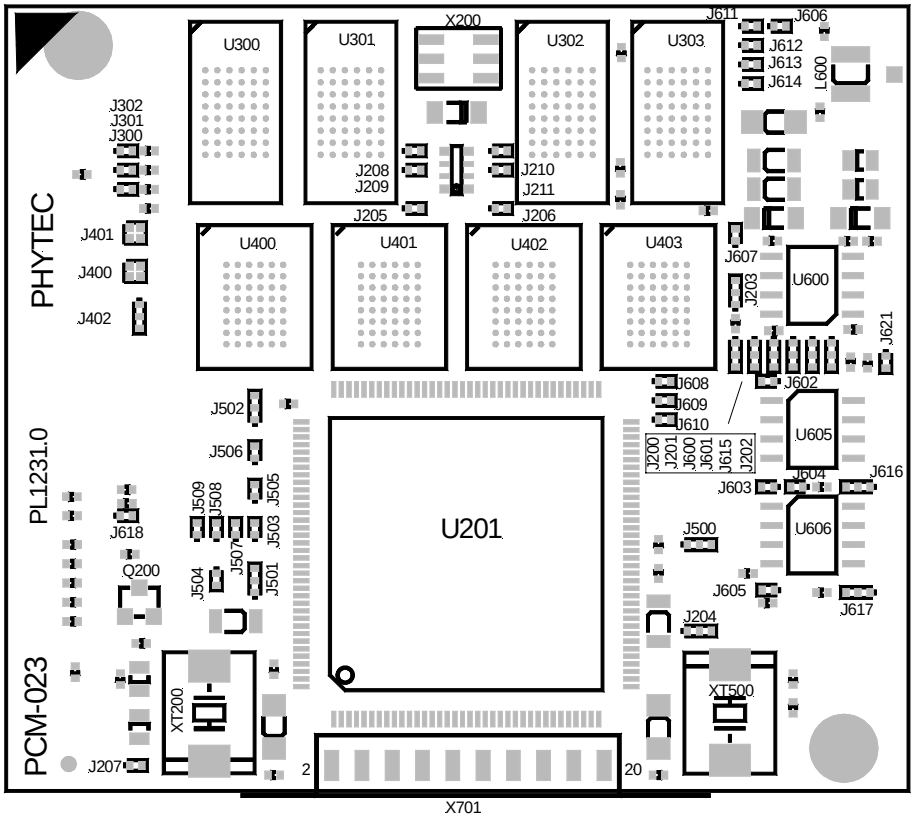


Figure 6: Location of the Jumpers (Top View)

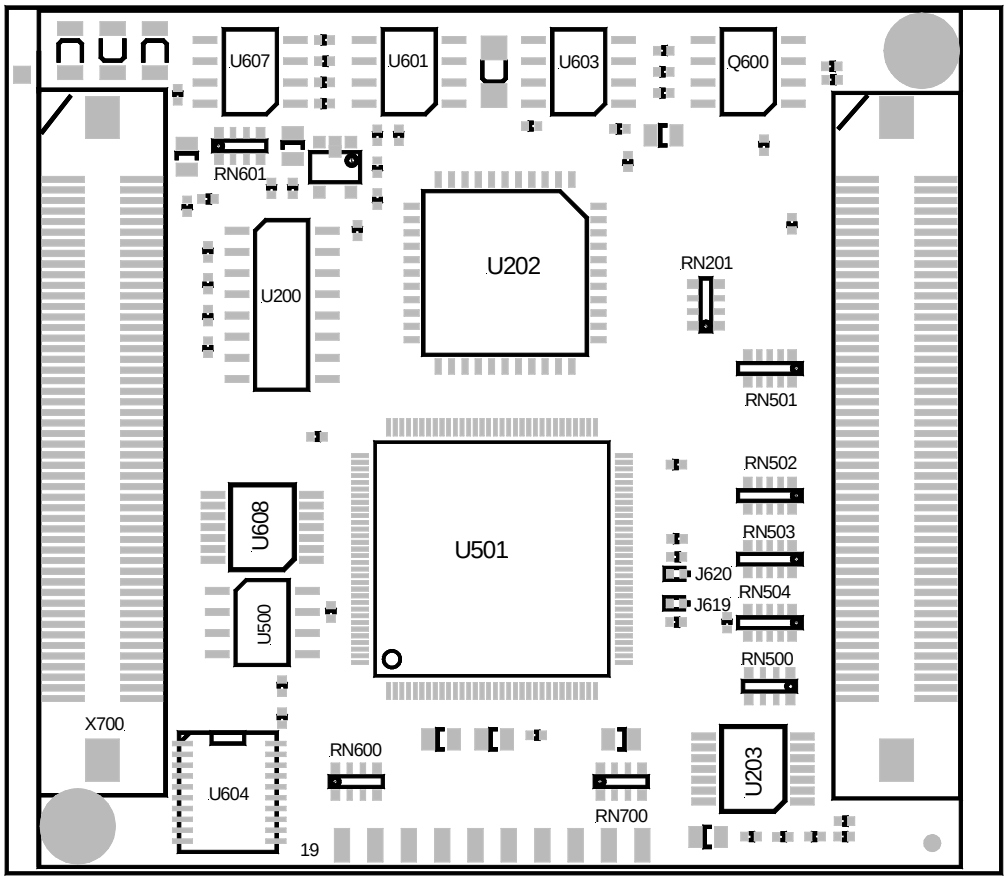


Figure 7: Location of the Jumpers (Bottom View)

The jumpers (J = solder jumper) have the following functions:

	Default Setting[1]		**Alternative Setting**	
J200	1 + 2	P08 as TxD1 with RS-232 level available at X700C23	2 + 3	P08 of the µC available as standard I/O or TxD1 with TTL level at pin X700C23
J201	1 + 2	P00 as TxD0 with RS-232 level available at X700D23	2 + 3	P00 of the µC available as standard I/O or TxD0 with TTL level at pin X700D23
J202	1 + 2	P09 as RxD1 with RS-232 level available at X700C21	2 + 3	P09 of the µC available as standard I/O or RxD1 with TTL level at pin X700C21
J203	1 + 2	P01 as RxD0 with RS-232 level available at X700D22	2 + 3	P01 of the µC available as standard I/O or RxD0 with TTL level at pin X700D22
J204	1 + 2	VDD_V3V3 as reference voltage for CPU internal A/D converter	2 + 3	Reference voltage for internal A/D converter can be supplied via pin X700D50
J205	closed	/CS0 connected with /CSF0 (only if CPLD U202 is not populated)	open[2]	/CS0 of the controller connected with CPLD U202, CPLD generates /CSF0 - /CSF1 signals
J206	closed	/CS1 connected with /CSR0 (only if CPLD U202 is not populated)	open[2]	/CS1 of the controller connected with CPLD U202, CPLD generates /CSR0 - /CSR1 signals
J207	open	MCKO signal not routed to Molex connector pin	closed	MCKO signals routed to Molex pin X700B1
J208	open	Flash configuration input 1 of CPLD U202 connected to VCC via 10k pull-up	closed	Flash configuration input 1 of the CPLD connected to GND
J209	open	Flash configuration input 2 of CPLD U202 connected to VCC via 10k pull-up	closed	Flash configuration input 2 of the CPLD connected to GND
J210	open	RAM configuration input 1 of CPLD U202 connected to VCC via 10k pull-up	closed	RAM configuration input 1 of the CPLD connected to GND
J211	open	RAM configuration input 2 of CPLD U202 connected to VCC via 10k pull-up	closed	RAM configuration input 2 of the CPLD connected to GND

1: Applies to standard modules without optional features, minimal memory configuration.

2 : Default on all other configuration options of the phyCORE-LPC2292.

	Default Setting		**Alternative Setting**	
J300	open	P017 of the µC available as standard I/O at Molex pin X700D15	closed	P017 used to supervise the Ready/Busy outputs of both Flash banks U300/U301 and U302/U303
J301	open	Flash bank U300/U301 not write protected	closed	Flash banks U300/U301 is write protected
J302	open	Flash bank U302/U303 not write protected	closed	Flash banks U302/U303 is write protected
J400	1 + 2 3 + 4	/BLS0 and /BLS1 signals configured for accessing fast SRAM devices	1 + 3 2 + 4	/BLS0 and /BLS1 signals configured for accessing standard SRAM devices
J401	1 + 2 3 + 4	/BLS2 and /BLS3 signals configured for accessing fast SRAM devices.	1 + 3 2 + 4	/BLS2 and /BLS3 signals configured for accessing standard SRAM devices.
J402	1 + 2	VCCRAM connected with VDD_V3V3.	open 2 + 3	No power supply for RAM devices. VCCRAM connected with VBAT, for external supply via battery.
J500	1 + 2	EEPROM (U500) ORG pin connected with VDD_V3V3, internal EEPROM organization configured to *16	2 + 3	EEPROM (U500) ORG pin connected with GND, internal EEPROM organization configured to *8.
J501	1 + 2	High-active interrupt output from SMSC LAN91C111 chip connected to EINT0 (PA016) on the µC. P016 is then no longer available as standard I/O pin at X700B2.	2 + 3 open	High-active interrupt output from SMSC LAN91C111 chip connected to EINT1 (PA014) on the µC. P014 is then no longer available as standard I/O pin at X700A3. Interrupt signals or standard I/O pins freely available at Molex pins X700B2 and X700A3.
J502	1 + 2	/CS2 from the µC connected with Chip Select signal on SMSC LAN91C111 chip. /CS2 is then no longer available at X700A6.	2 + 3 open	/CS3 from the µC connected with Chip Select signal on SMSC LAN91C111 chip. /CS3 is then no longer available at X700B6. /CS2 and /CS3 freely available at Molex pins X700A6 and B6.
J503	open	P018 from the µC freely available at X700C16.	closed	P018 used to supervise the Ready signal on the on SMSC LAN91C111. P018 is then no longer available at Molex pin X700C16.

	Default Setting		**Alternative Setting**	
J504	open	LAN_IRQ signal not connected to an additional 10k pull-up resistor to VDD_V3V3.	closed	LAN_IRQ signal is connected to an additional 10k pull-up resistor to VDD_V3V3
J505	open	IOS0 signal on SMSC LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents.	closed	IOS0 signal on SMSC LAN 91C111 connected to GND. *See LAN91C111 data sheet for more details.*
J506	open	IOS1 signal on SMSC LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents.	closed	IOS01 signal on SMSC LAN 91C111 connected to GND. *See LAN91C111 data sheet for more details.*
J507	open	IOS2 signal on SMSC LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents.	closed	IOS02 signal on SMSC LAN 91C111 connected to GND. *See LAN91C111 data sheet for more details.*
J508	open	ENEEP signal on SMSC LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents.	closed	ENEEP signal on SMSC LAN 91C111 connected to GND. *See LAN91C111 data sheet for more details.*
J509	closed	LAN 91C111 nLNK pin tied to GND, LINK_ON bit in the EPH status register is set to "1"	open	LAN 91C111 nLNK pin not connected, LINK_ON bit in the EPH status register is set to "0"
J600	1 + 2	P020 on the µC freely available as standard I/O at Molex pin X700A4	2 + 3	P020 used for enabling resp. disabling the CAN transceiver U605, connected to INH.
J601	1 + 2	P019 on the µC freely available as standard I/O at Molex pin X700C19	2 + 3	P019 used for enabling resp. disabling the CAN transceiver U606, connected to INH input.
J602	open	CAN_H1 signal generated by CAN transceiver U605 (only if CAN transceiver U605 populates the module).	closed	CAN_H1 signal directly connected with µC port TD1 and available as CAN TTL signal an X700D21, for connection to external CAN transceiver (only in connection with unpopulated U605).

	Default Setting		**Alternative Setting**	
J603	open	CAN_H2 signal generated by CAN transceiver U606 (only if CAN transceiver U606 populates the module).	closed	CAN_H2 signal directly connected with µC port P024 and available as CAN TTL signal an X700C18, for connection to external CAN transceiver (only in connection with unpopulated U606).
J604	open	CAN_L1 signal generated by CAN transceiver U605 (only if CAN transceiver U605 populates the module).	closed	CAN_L1 signal directly connected with µC port P025 and available as CAN TTL signal an X700D20, for connection to external CAN transceiver (only in connection with unpopulated U605).
J605	open	CAN_L2 signal generated by CAN transceiver U606 (only if CAN transceiver U606 populates the module).	closed	CAN_L2 signal directly connected with µC port P023 and available as CAN TTL signal an X700D18, for connection to external CAN transceiver (only in connection with unpopulated U606).
J606	open	SPI EEPROM not wrote protected.	closed	SPI EEPROM write protected, /WP input tied to GND.
J607	open	MAX6301 configured for extended mode (*see IC data sheet for details*), WDS pin via pull-up resistor to VCC, if WDI is floating the processor independend WDT is disabled	closed	MAX6301 is disabled if the /BOOT or /DEBUG signals are active. Otherwise the WDT is active following a RESET. (*Please refer to the MAX6301 datasheet for further information.)*
J608	closed	/INT_RTC output from RTC (U604) connected to port P015 of the µC. P015 is then no longer available as standard I/O pin at X700B3.	open	RTC interrupt not connected to the µC. P015 is available as standard I/O pin at X700B3.
J609	closed	RTC (U604) SDA signal connected to port P03 of the µC. P03 is then no longer available as standard I/O pin at X700A48.	open	RTC SDA signal not connected to the µC on the module, external connection required (at pin X700D32). P03 is available as standard I/O pin at X700A48.

	Default Setting		**Alternative Setting**	
J610	closed	RTC (U604) SCL signal connected to port P02 of the µC. P02 is then no longer available as standard I/O pin at X700A47.	open	RTC SCL signal not connected to the µC on the module, external connection required (at pin X700C31). P02 is available as standard I/O pin at X700A47.
J611	closed	EEPROM (U607) /PCS0 signal connected to port P10 of the µC. P10 is then no longer available as standard I/O pin at X700B50.	open	EEPROM /PCS0 signal not connected to the µC on the module, external connection required (at pin X700C26). P10 is available as standard I/O pin at X700C13.
J612	closed	EEPROM (U607) MISO0 signal connected to port P05 of the µC. P05 is then no longer available as standard I/O pin at X700A49.	open	EEPROM MISO0 signal not connected to the µC on the module, external connection required (at pin X700D27). P05 is available as standard I/O pin at X700A49.
J613	closed	EEPROM (U607) MOSI0 signal connected to port P06 of the µC. P06 is then no longer available as standard I/O pin at X700A50.	open	EEPROM MOSI0 signal not connected to the µC on the module, external connection required (at pin X700C28). P06 is available as standard I/O pin at X700A50.
J614	closed	EEPROM (U607) SCLK0 signal connected to port P04 of the µC. P04 is then no longer available as standard I/O pin at X700B48.	open	EEPROM SCLK0 signal not connected to the µC on the module, external connection required (at pin X700D28). P04 is available as standard I/O pin at X700B48.
J615	1 + 2	Supply voltage for CAN transceivers U605 and U606 (TLE6250V33) from VCC2 (5 V).	2 + 3	Supply voltage for CAN transceivers U605 and U606 connected to VDD_V3V3 (3.3 V).
J616	closed	Pin 5 on CAN transceivers U605 connected to 3.3V supply voltage (use only with TLE6250V33 devices).	open	Pin 5 on CAN transceivers U605 not connected to 3.3V supply voltage (use only with other CAN transceivers devices).
J617	closed	Pin 5 on CAN transceivers U606 connected to 3.3V supply voltage (use only with TLE6250V33 devices)	open	Pin 5 on CAN transceivers U606 not connected to 3.3V supply voltage (use only with other CAN transceivers).
J618	open	VDD_V3V3 supply voltage is switched via FET Q600A.	closed	VDD_V3V3 supply voltage directly derived from VCC.

	Default Setting		Alternative Setting	
J619	open	SPI0 is operated in master mode.	closed	SPI0 is operated in slave mode.
J620	open	SPI1 is operated in master mode.	closed	SPI1 is operated in slave mode.
J621	open	P021 is available as standard I/O pin at X700C24	closed	WDI signal is generated via port P021.
Additional jumper settings, only applicable when using the debugCORE-LPC2292/2294				
J800	open	Pin 1 on ETM/OCDS connector (/RESET) not connected.	closed	Pin 1 on ETM/OCDS connector carries module's /RESET signal.
J801	1 + 2	Vsupply and VTREF on the ETM/OCDS connector are supplied via VDD_V3V3. (Configuration depends on Emulator requirements, *refer to applicable data sheets*)	2 + 3	Vsupply and VTREF are connected to GND. (Configuration depends on Emulator requirements, *refer to applicable data sheets)*

Table 2: Jumper Settings

3.1 J200, J202 Second Serial Interface

Jumpers J200 and J202 are used to route the signals of the second synchronous/asynchronous serial interface via the RS-232 transceiver to the phyCORE connector pins X700C21 (RxD1) and X700C23 (TxD1). If the jumpers are closed in position 2+3, then the applicable controller pins P08 and P09 can be used with their alternative functions or the serial interface signals are available with their TTL level at phyCORE-connector pins X700C21 and X700C23.

If the jumpers are closed at position 1+2 we recommend **not** to use the interface signals with their TTL level as this will cause damage to the on-board components.

The following configurations are possible:

Signal Configuration	J200	J202
TxD1 and RxD1 with RS-232 levels	1 + 2*	1 + 2*
P08 and P09 as I/O pin or TxD1 and RxD1 as interface signals with TTL level	2 + 3	2 + 3

* = Default setting

Table 3: J200, J202 Second Serial Interface Configuration

3.2 J201, J203 First Serial Interface

Jumper J201 and J203 connect the signals of the first synchronous/ asynchronous serial interface to the on-board RS-232 transceiver. The interface signals are then available with RS-232 level at the phyCORE-connector pins X1D22 (RxD0) and X1D23 (TxD0). If the jumpers are opened, the applicable controller pins P00 and P01 can be used with their alternative functions or the serial interface signals are available with their TTL level at phyCORE-connector pins X1D17 and X1D16.

If the jumpers are closed we recommend **not** to use the interface signals with their TTL level as this will cause damage to the on-board components.

The following configurations are possible:

Signal Configuration	J201	J203
TxD0 and RxD0 with RS-232 level at X700D22 and X700D23	1 + 2*	1 + 2*
TxD0 and RxD0 with TTL level or as I/O pin at X700D22 and X700D23	2 + 3	2 + 3
P00 and P01 as I/O pin or TxD0 and RxD0 interface signals with TTL level at X700D16 and X700D17	open	open

* = Default setting

Table 4: J201, J203 First Serial Interface Configuration

3.3 J204 A/D Converter

The integrated analog/digital converter on the phyCORE-LPC2292/94 requires an upper and lower reference voltage (V_{ADREF}) connected at pin 14 of the microcontroller. The reference voltage source can be selected using Jumper J204.

The following configurations are possible:

Reference Voltage Configuration	J204
V_{ADVREF} derived from main supply voltage VDD_V3V3	1 + 2*
external A/D reference voltage source (V_{ADVREF} at X700D50)	2 + 3

* = Default setting

Table 5: J204 A/D Converter Reference Voltage

3.4 J205, J206 Chip Select Configuration

If the phyCORE-LPC2292/94 is delivered with the minimum memory configuration, then the CPLD device is not required. In this case Jumper J205 and J206 must be closed in order to connect the Chip Select signals for Flash and SRAM with the corresponding controller signals. These jumpers remain open on all other memory configuration varaints of the phyCORE-LPC2292/94 since the required Chip Select signals for Flash and SRAM must be decodede by the CPLD at U202 in order to ensure correct memory addressing.

The following configurations are possible:

Chip Select for Flash and RAM	J205	J206
Chip Selects for Flash and RAM decoded by the CPLD	open	open
Chip Selects for Flash and RAM directly connected to µC (/CS0 and /CS1)[1]	closed*	closed*

*** Note:**
If minimum configuration of the phyCORE-LPC2292/94 is used these jumpers must be closed

Table 6: J205, J206 Chip Select Configuration

3.5 J207 MCKO Signal

This jumper can be used to connect the master clock output signal (MCKO) to Molex pin X700B1 for use in external application circuitry.

The following configurations are possible:

Flash Memory Size	J207
MCKO signal not routed to Molex connector pin	open*
MCKO signals routed to Molex pin X700B1	closed

* = Default setting

Table 7: J207 MCKO Signal Configuration

1: Only possible if minimum configuration of the phyCORE-LPC2292 is used, CPLD not populated.

3.6 J208, J209 Flash Size Configuration

The phyCORE-LPC2292/94 can be populated with three different Flash memory sizes per shape (U300 thru U303). The size of the device must be configured to ensure linear addressing of the entire Flash bank. Jumpers J208 and J209 are used to select the size of the memory device. The on-board CPLD reads the signal level on the applicable input pins and configures the individual Chip Select signals for the Flash devices accordingly.

Note:
Jumpers J208 and J209 are configured at time of delivery of the phyCORE-LPC2292/94 according to the choosen memory configuration. Therefor these jumpers must **not** be altered by the user!

The following configurations are possible:

Flash Memory Size	J208	J209
1 MByte (per shape)	open*	open*
2 MByte (per shape)	closed	open
4 MByte (per shape)	open	closed
Not permitted	closed	closed

* = Default setting

Table 8: J208, J209 Flash Memory Size Configuration

3.7 J210, J211 RAM Size Configuration

The phyCORE-LPC2292/94 can be populated with three different RAM memory sizes per shape (U400 thru U403). The size of the device must be configured to ensure linear addressing of the entire RAM bank. Jumpers J210 and J211 are used to select the size of the memory device. The on-board CPLD reads the signal level on the applicable input pins and configures the individual Chip Select signals for the RAM devices accordingly.

Note:
Jumpers J210 and J211 are configured at time of delivery of the phyCORE-LPC2292/94 according to the choosen memory configuration. Therefor these jumpers must **not** be altered by the user!

The following configurations are possible:

RAM Memory Size	J210	J211
512 kByte (per shape)	open*	open*
1 MByte (per shape)	closed	open
2 MByte (per shape)	open	closed
Not permitted	closed	closed

* = Default setting

Table 9: J210, J211 RAM Memory Size Configuration

3.8 J300 Flash Ready/Busy Configuration

The state of the Flash device can be queried during a programming cycle by using the Flash's Ready/Busy signal. To accomplish this, the Ready/Busy signal from the populated Flash devices can be connected with port P017 on the LPC2292/94 controller using Jumper J300. *Refer to the applicable Flash device Data Sheet/User's Manual for more information about this feature.*

The following configurations are possible:

Flash Ready/Busy Configuration	J300
Ready/Busy outputs of both Flash banks U300/U301 and U302/U303 disconnected from P017 of the µC, P017 available as standard I/O at Molex pin X700D15	open*
P017 used to supervise the Ready/Busy outputs of both Flash banks U300/U301 and U302/U303, P017 not available as standard I/O at Molex pin X700D15	closed

* = Default setting

Table 10: J300 Flash Ready/Busy Configuration

3.9 J301, J302 Flash Write Protection Configuration

Jumpers J301 and J302 are used to protect the contents of Flash banks U300/U301 and U302/U303 from unauthorized or unintentional erasure. By closing jumpers J301 and J302, the hardware mechanism is activated for write protection of the individual Flash banks.

This feature is not supported by all the Flash devices that could be populated on the module. *For more detailed information about the write protection function, refer to the Data Sheet/User's Manual of the Flash device in question.*

The following configurations are possible:

Flash Write Protection	J301	J302
Flash bank U300/U301 without hardware write protection	open*	don't care
Flash bank U300/U301 with hardware write protection	closed	don't care
Flash bank U302/U303 without hardware write protection	don't care	open*
Flash bank U302/U303 with hardware write protection	don't care	closed

* = Default setting

Table 11: J301, J302 Flash Write Protection Configuration

3.10 J400, J401 SRAM Configuration

Jumpers J400 and J401 are required for configuring the SRAM signals /BLS0 through /BLS3. This configures the controller access to the various SRAM types that can be populated on the phyCORE-LPC2292/94, since these can have various data bus configurations.

The following configurations are possible:

Signal Configuration	J400	J401
/BLS0 and /BLS1 signals configured for accessing fast SRAMs, /BLS2 and /BLS3 signals configured for accessing fast SRAMs (i.e. 10 ns)	1 + 2* 3 + 4*	1 + 2* 3 + 4*
/BLS0 and /BLS1 signals configured for accessing standard SRAMs /BLS2 and /BLS3 signals configured for accessing standard SRAMs (i.e. 55 ns)	1 + 3 2 + 4	1 + 3 2 + 4

* = Default setting

Table 12: J400, J401 SRAM Access Configuration

3.11 J402 SRAM Supply Voltage

The SRAMs (U400-U403) can operate with or without a battery buffer. Jumper J402 is used to set the supply voltage for the SRAM.

The following configurations are possible:

SRAM U400-U403 Supply Voltage	J402
VCCRAM derived from VDD_V3V3	1 + 2*
VCCRAM derived from VBAT	2 + 3

* = Default setting

Table 13 J402 SRAM Supply Voltage Configuration

3.12 J500 through J509 Ethernet Controller SMSC LAN91C111Configuration

As an option, a LAN91C111 Ethernet controller from SMSC can populate the phyCORE-LPC2292/94 at U501.

If the Ethernet controller populates the phyCORE module, one of two possible Chip Select signals for controlling access to the LAN91C111 can be selected using Jumper J502. Jumper J501 selects, which of the microcontroller interrupts connects with the interrupt output (LAN_IRQ) of the Ethernet controller. The LAN_IRQ signal can be connected to a 10k pull-up resistor with the help of Jumper J504. Connection of the LAN91C111 controller's Ready (LAN_RDY) signal to port pin P018 is established by closing Jumper J503.

The following configurations are possible:

/CS Signal Configuration	**J502**
/CS2 from the µC selects Ethernet controller	1 + 2*
/CS3 from the µC selects Ethernet controller	2 + 3

* = Default setting

Table 14: J503 Ethernet Chip Select Signal Configuration

Interrupt of the Ethernet Controller...	**J501**
... connects to EINT0 (P016) of the microcontroller	1 + 2*
... connects to EINT1 (P014) of the microcontroller	2 + 3
… not connected to the microcontroller	open

* = Default setting

Table 15: J501 Ethernet Interrupt Signal Configuration

Ethernet Controller Ready Signal...	J503
… not connected to the LPC2292/94. P018 available as standard I/O pin.	open*
... connects to P018 of the microcontroller.	closed

* = Default setting

Table 16: J503 Ethernet Ready Signal Configuration

LAN_IRQ Pull-up Configuration	J504
LAN_IRQ signal not connected to an additional 10k pull-up resistor to VDD_V3V3	open*
LAN_IRQ signal is connected to an additional 10k pull-up resistor to VDD_V3V3	closed

* = Default setting

Table 17: J504 Ethernet LAN_IRQ Pull-up Configuration

The LAN91C111 Ethernet controller provides 4 configuration inputs, IOS0-IOS2 and ENEEP, to enable access to the serial EEPROM and use predefined EEPROM configurations. The corresponding Jumpers J505-J507 and J508 connect these inputs to GND level when closed.

LAN91C111 Configuration	J505 IOS0	J506 IOS1	J507 IOS2
IOSx signal on LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents	open*	open*	open*
IOSx signal on LAN 91C111 connected to GND (*see data sheet for details*)	closed	closed	closed

* = Default setting

Table 18: J505, J506, J507 Ethernet EEPROM Configuration

Ethernet EEPROM Enable Configuration	J508
ENEEP signal on LAN 91C111 connected with internal pull-up to VDD_V3V3, configuration via predefined EEPROM contents	open*
ENEEP signal on LAN 91C111 connected to GND (*see data sheet for details*)	closed

* = Default setting

Table 19: J508 Ethernet EEPROM Enable Configuration

Jumper J509 configures the general purpose input port of the LAN91C111 Ethernet controller that is used to convey the LINK status (EPHSR bit 14). This LINK_ON bit is typically used for link test. *See the LAN91C111 data sheet for details*.

Ethernet EEPROM Enable Configuration	J509
LAN 91C111 nLNK pin tied to GND, LINK_ON bit in the EPH status register is set to "1"	closed*
LAN 91C111 nLNK pin not connected, LINK_ON bit in the EPH status register is set to "0"	open

* = Default setting

Table 20: J509 Ethernet nLNK Pin Configuration

3.13 J600, J601, J616 CAN Transceiver Configuration

The three Jumpers J600, J601 and J616 are used to configure both CAN transceivers U605 and U606. If the Jumpers J600 and J601 are placed in the corresponding position, the CAN transceivers can be switched into power-down mode via controller port pins P019 and P020.

The following configurations are possible:

CAN Transceiver Activation	J600	J601
CAN transceiver U605 always active	1 + 2*	don't care
CAN transceiver U605 mode is controlled via port P020 on the LPC2292/94 microcontroller	2 + 3	don't care
CAN transceiver U606 always active	don't care	1 + 2*
CAN transceiver U605 mode is controlled via port P019 on the LPC2292/94 microcontroller	don't care	2 + 3

* = Default setting

Table 21: J600, J601 CAN Transceiver Activation

Jumper J616 is used to supply power to the CAN transceivers U605 and U606. Routing the VDD_V3V3 supply voltage to pin 5 of the relevant CAN transceiver is only required if the TLE 6250V3V3 populates the phyCORE module. If the Philips 82C251 CAN transceiver is populated, the jumper must be open.

The following configurations are possible:

CAN Transceiver Supply Configuration	J616
Pin 5 on CAN transceivers U605 and U606 connected to 3.3V supply voltage VDD_V3V3 (use only with TLE6250V33 devices)	closed*
Pin 5 on CAN transceivers U605 and U606 not connected to 3.3 V supply voltage VDD_V3V3 (use only with 82C251 devices)	open

* = Default setting

Table 22: J616 CAN Transceiver Supply Configuration

3.14 J602, J603, J604, J605 CAN Interfaces

Two CAN interfaces are provided by the phyCORE-LPC2292/94. The CAN signals extend to the two TLE6250V33 CAN transceivers at U605 and U606. The CAN transceivers generate the corresponding CAN_H1, CAN_L1, CAN_H2 and CAN_L2 signals. These signals can be directly connected to a CAN dual-wire bus.

In order to use external (opto-isolated) transceivers, direct access to the CAN1Rx, CAN1Tx, CAN2Rx and CAN2Tx signals is also available at the phyCORE-connector X700. This requires **both** removal of the on-board CAN transceiver devices **and** closing Jumpers J602, J603, J604 and J605.

The following configurations are possible:

First CAN Interface	J602	J604
CAN_H1 at X700D21 CAN_L1 at X700D20	open*[1]	open*[1]
CAN1_Rx at X700D21 CAN1_Tx at X700D20	closed [2]	closed[2]

Second CAN Interface	J603	J604
CAN_H2 at X700C18 CAN_L2 at X700D18	open*[1]	open*[1]
CAN2_Rx at X700C18 CAN2_Tx at X700D18	closed[2]	closed[2]

* = Default setting

Table 23: J602, J603, J604 and J605 CAN Interface Configuration

3.15 J606 Write Protection of SPI EEPROM

Various types of SPI EEPROM devices can populate space U607. Some of these devices provide a write protection function[3]. Closing Jumper J606 connects pin 3 of the serial EEPROM with GND and thus activates write protection.

The following configurations are possible:

Write Protection EEPROM	J606
Write protection of EEPROM deactivated	open*
Write protection of EEPROM activated	closed

* = Default setting

Table 24: J606 EEPROM Write Protection

[1] : Should only be used if CAN transceivers U605 and U606 are populated.

[2] : **Note!** Should only be used if CAN transceivers U605 and U606 are **NOT** populated.

[3]: *Refer to the corresponding EEPROM Data Sheet for more information on the write protection function.*

3.16 J607 Watchdog Configuration

The phyCORE-LPC2292/94 supports a processor-independent MAX6301 watchdog device, which can be configured with the help of Jumper J607. This jumper configures various watchdog operating modes with preconfigured settings or using a controller port pin to change the mode.

The following configurations are possible:

Watchdog	J607
MAX6301 configured for extended mode (*see IC data sheet for details*), WDS pin via pull-up resistor, disables watchdog due to floating WDI signal	open*
The MAX6301 WDT is activated via the /BBOT or /DEBUG signal. Additional logic ICs monitor the level of these signals. If one of the signals has a low level, then the WDT is disabled allowing unlimited use of the phyCORE module. Following RESET (without active low signals /BOOT and /DEBUG) the WDT is always enabled if Jumper J607 is closed.	closed

* = Default setting

Table 25: J607 Watchdog Configuration

3.17 J608, J609, J610 I²C Interface

Jumpers J608, J609 and J610 are provided to connect the controller's I²C interface to the on-board RTC and the phyCORE-connector. The I²C signals SDA and SCL are available at pins X700C31 and X700D32 if Jumpers J609 and J610 are closed. Jumper J608 connects the RTC interrupt output to port P015. If all 3 jumpers remain open the corresponding controller signals are available as standard I/O pins at X700B47, X700A48 and X700B3.

The following configurations are possible:

Signal Configuration	J608	J609	J610
Port pins P02, P03, P015 configured as I²C interface signals	closed*	closed*	closed*
Port pins P02, P03, P015 available as standard I/O pins	open	open	open

* = Default setting

Table 26: J608, J609, J610 I²C Interface Configuration

3.18 J611, J612, J613, J614 SPI0 Interface

Jumpers J611 through J614 connect the SPI0 interface signals of the microcontroller to the on-board SPI bus. The on-board EEPROM (U607) is connected to the SPI bus. If the jumpers remain open, then the applicable controller pins pins P04, P05 P06 and P10, can be used with their alternative functions at phyCORE-connector pins X700B48, X700A49, X700A50 and X700C13. The SPI interface signals are available at X700C26, X700C28, X700D27 and X700D28.

The following configurations are possible:

Function	J611	J612	J613	J614
on-board SPI0 bus connected (SCLK0, /PCS0 MISO0, MOSI0)	closed*	closed*	closed*	closed*
on-board SPI0 bus disconnected	open	open	open	open

* = Default setting

Table 27: J611, J612, J613, J614 SPI Interface Signal Configuration

3.19 J615 CAN Bus Level Configuration

Jumper J615 is used for configuration of the CAN level power supply on the CAN transceivers U605 and U606. In order to ensure proper CAN_High and CAN_Low voltage levels the applicable CAN transceiver must be supplied with the required voltage level at pin #3.

The following configurations are possible:

CAN Transceiver Supply Configuration	J615
Pin 3 on CAN transceivers U605 and U606 connected to 5 V supply voltage VDD_V5V0 *(use only with TLE6250V33 devices)*	1 + 2*
Pin 3 on CAN transceivers U605 and U606 not connected to 3.3 V supply voltage VDD_V3V3 *(use only with other CAN transceivers)*	2 + 3

* = Default setting

Table 28: J615 CAN Level Configuration

3.20 J616, J617 CAN Transceiver VCC, Pin 5

These jumpers are used to connect the 3.3 V main supply voltage to pin #5 on the TLE6250V33 CAN transceivers at U605 (J616) and U606 (J617). If other CAN transceiver devices are used on the phyCORE-LPC2292/94 these jumpers must remain open.

The following configurations are possible:

CAN Transceiver VCC, Pin 5	J616	J617
Pin 5 on CAN transceivers U605 connected to 3.3 V supply voltage (use only with TLE6250V33 devices).	closed*	-
Pin 5 on CAN transceivers U605 not connected to 3.3 V supply voltage (use only with other CAN transceivers devices).	open	-
Pin 5 on CAN transceivers U606 connected to 3.3 V supply voltage (use only with TLE6250V33 devices).	-	closed*
Pin 5 on CAN transceivers U606 not connected to 3.3 V supply voltage (use only with other CAN transceivers devices).	-	open

* = Default setting

Table 29: J616, J617 CAN Transceiver VCC at Pin #5

3.21 J618 VDD_V3V3 Supply Control

Jumper J618 can be used to directly connect the VDD_3V3V on-board main supply voltage with the external VCC voltage. In normal operation the FET switch Q600A controls the VDD_3V3V connection to VCC. Jumper J618 should remain open.

The following configurations are possible:

VDD_V3V3 Supply Control	J618
VDD_V3V3 supply voltage is switched via FET Q600A	open*
VDD_V3V3 supply voltage directly derived from VCC	closed

* = Default setting

Table 30: J618 VDD_V3V3 Supply Control

3.22 J619, J620 SPI Master/Slave Selection

Jumpers J619 and J620 are used to configure the SPI interface mode. If both jumpers remain open, then both SPI interfaces operate in Master mode. The SPI interfaces will operate in Slave mode if the corresponding jumpers are closed.

The following configurations are possible:

SPI Master/Slave Mode Selection	J619	J620
SPI0 operates in Master mode after RESET.	open*	-
SPI0 operates in Slave mode after RESET.	closed	-
SPI1 operates in Master mode after RESET.	-	open*
SPI1 operates in Slave mode after RESET.	-	closed

* = Default setting

Table 31: J619, J620 SPI Master/Slave Selection

3.23 J621 WDI Signal Source

Jumper J621 configures the source of the signal connected to the WDI input on the external Watchdog timer (WDT). Jumper J621 connects microcontroller port P021 to the WDI input signal which allows software controlled WDT activation.

The following configurations are possible:

WDI Signal Source	J621
WDI signal on WDT MAX6301 is not controlled by the microcontroller, if the WDT is used then the WDI signal needs to be controlled via Molex pin X700D8	open*
Microcontroller port P021 controls the WDI input signal. Additional peripheral components can be controlled by the WDI/P021 signal at Molex pin X700D8	closed

* = Default setting

Table 32: J621 WDI Signal Source

3.24 J800, J801 ETM/OCDS Connector Configuration (only with debugCORE-LPC2292/94)

Jumper J800 and J801 are used to route certain signals to the ETM/OCDS connector at X800. This connector is only available on the debugCORE-LPC2292/94. Configuration of these jumpers greatly depends on the characteristics of the emulator that connects to the debugCORE module, *refer to the emulator User's Manual for details*.

The following configurations are possible:

ETM/OCDS Connector Configuration	J800	J801
Pin 1 on ETM/OCDS connector (/RESET) not connected, depends on emulator	open*	-
Pin 1 on ETM/OCDS connector carries module's /RESET signal	closed	-
Vsupply and VTREF on the ETM/OCDS connector are supplied via VDD_V3V3	-	1 + 2*
Vsupply and VTREF are connected to GND	-	2 + 3

* = Default setting

Table 33: J616, J617 CAN Transceiver VCC at Pin #5

3.25 C210 CLKIN Configuration

Capacitor C210 is used to input an external clock signal. In default settings the on-board quartz oscillator is used for generating the microcontroller's clock speed (C210 not populated). As an alternative an external clock signal can be connected to the controller pin XIN via phyCORE connector pin X1A1. This requires removal of the on-board quartz oscillator and populating C210 with a 100p/50V capacitor.

Note:
Because of the oscillator properties, C210 should not be closed when using the on-board quartz oscillator. This can have a negative effect on the stability of the quartz oscillation!
If an external clock input via X1A1 is required, the on-board quartz oscillator must be removed.

The following configurations are possible:

CLKIN Configuration	C210
Using the on-board crystal XT1	open*
Supply via external clock signal at phyCORE connector pin X1A1	100p/50V capacitor mounted

* = Default setting

Table 34: C210 CLKIN Configuration

4 System Configuration

Although most features of the Philips LPC2292/94 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

4.1 System Startup Configuration

Following a hardware reset, certain port pins are latched by the controller to configure chip-level features. The desired port pins can be connected to a weak pull-down resistor (resulting in logical 0), or by leaving the connections open (resulting in logical 1). Internal pull-up resistors ensure a high level if the pin is left unconnected. 4.7 kΩ pull-down resistors are recommended, although the resistor value is also dependent upon the external circuitry connected to the port pins in question.

Table 35 and *Table 36* show the individual port pins used for system startup configuration, the corresponding pull-down resistor and the location of the signals on the phyCORE connector:

Boot Device Selection		
Configuration	**D26/BOOT0 via R203 (X700B43)**	**D27/BOOT1 via R204 (X700A44)**
/CS0 configured for 32-bit memory	populated BOOT0 = 0	unpopulated BOOT1 = 1
/CS0 configured for 16-bit memory	unpopulated BOOT0 = 1	populated BOOT1 = o
/CS0 configured for 8-bit memory	populated BOOT0 = 0	populated BOOT1 = 0
Internal Flash access	unpopulated BOOT0 = 1	unpopulated BOOT1 = 1

Table 35: System Startup Configuration – Boot Device Selection

Default system startup configuration on the phyCORE-LPC2292/94

Debug/Trace Port Configuration		
Configuration	**R205 for P120 (X700D30)**	**R206 for P126 (X700D37)**
P1.16 through P1.25 function as TRACE port	populated	don't care
P1.16 through P1.25 function as port pins	unpopulated	don't care
P1.26 through P1.31 function as Debug port	don't care	populated
P1.26 through P1.31 function as port	don't care	unpopulated

Table 36: System Startup Configuration – Debug/Trace Port

Default system startup configuration on the phyCORE-LPC2292/94
Default system startup configuration with debugCORE-LPC2292/94

4.2 Starting the LPC2292/94 ISP Mode

In order to start the ISP command handler on the LPC2292/94, port P0.14 of the microcontroller must be connected to a low signal level at the time the reset signal changes from its active to the inactive state. This is achieved by applying a high-level signal at pin X1C9 (BOOT) of the phyCORE-LPC2292/94. A transistor circuitry connects P0.14 to GND as long as the BOOT pin is high. An on-board pull-up resistor (R213) ensures a high level at P0.14 if the BOOT signal is not active. This BOOT signal can be generated by a push button (temporary signal) or jumper setting (permanent signal) on the phyCORE Developent Board HD200 *(refer to section 15.3.2 for more details)*.

5 Memory Models

The Philips LPC2292/94 controller provides up to four Chip Select signals for easy selection of external peripherals or memory banks. Depending on the number of memory devices installed on the phyCORE-LPC2292/94, as well as the availability of the optional Ethernet controller, up to three Chip Select signals are used internally. /CS0 selects the two Flash banks installed on U300 – U303 with either 1 MByte, 2 MByte or 4 MByte devices in CBGA-48 packaging per shape. The total amount of Flash memory is 2 MByte in the minimum configuration of the module and 16 MByte if the maximum configuration is used.

The external data memory consists of the two RAM banks at U400 – U403. These spaces can house memory devices of 512 kByte, 1 MByte or 2 MByte in an TBGA-48 package. /CS1 selects the RAM banks on U400 – U403.

Access to the optional Ethernet controller at U501 can be established via /CS2 or /CS3 configurable with Jumper J502. The default configuration allows access via /CS2 (J502 closed at 1+2).

Configuration of the LPC2292/94 controller's Chip Select signals is only possible in a restricted matter. This is due to hardware defined address ranges for the individual /CS signals. Only bus access time and access type can be coinfigured with the bus configuration registers BCFG0 to BCFG3.

The following table shows the predefined address ranges for the individual /CS signals (banks) and the corresponding bus configuration registers.

Bank	Address Range	Configuration Register
0	8000 0000 – 80FF FFFF	BCFG0
1	8100 0000 – 81FF FFFF	BCFG1
2	8200 0000 - 82FF FFFF	BCFG2
3	8300 0000 - 83FF FFFF	BCFG3

Table 37: /CS Signal (Bank) Address Ranges and Configuration Registers

The following image depicts the default memory model on the Philips LPC2292/94 microcontroller showing internal and external address spaces of the controller. This memory model also applies to the phyCORE-LPC2292/94 module.

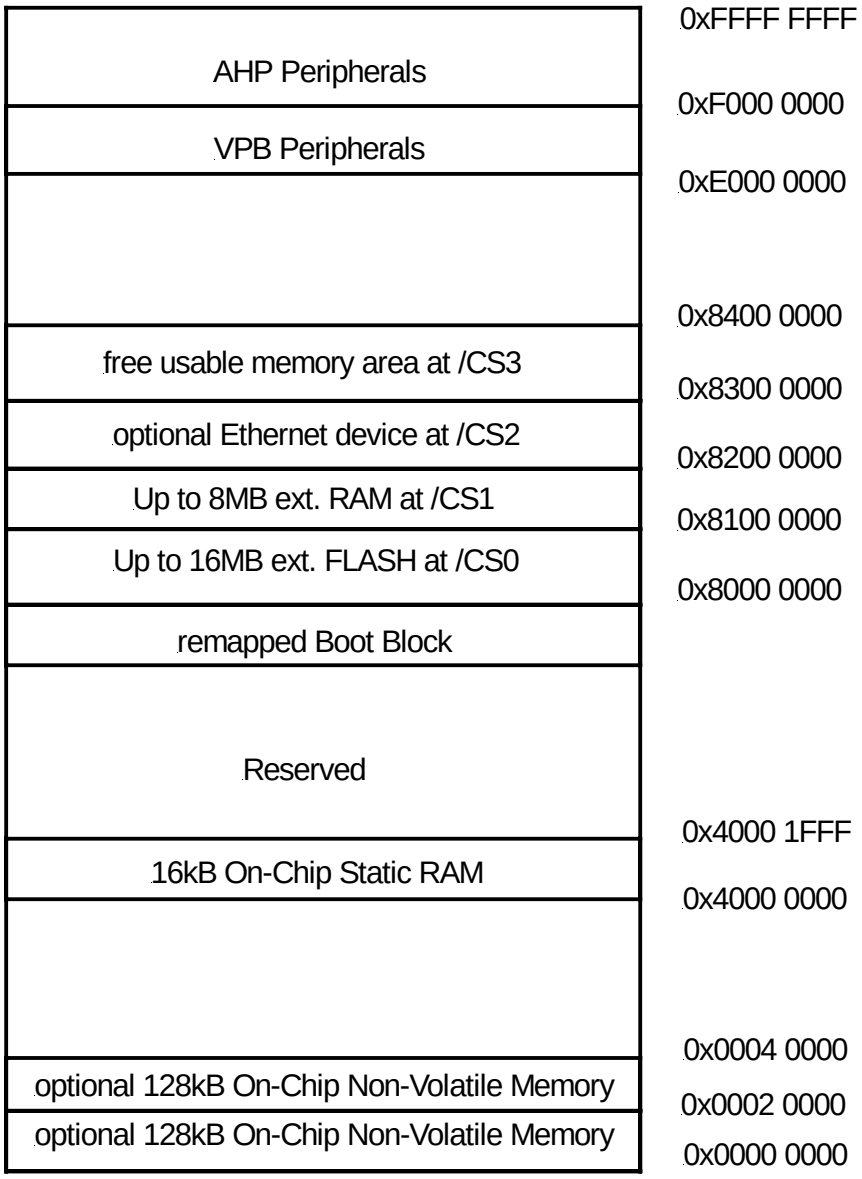


Figure 8: phyCORE-LPC2292/94 Memory Model

The following section contains two examples of the controller's configuration registers. These examples match the needs of most standard applications for the phyCORE-LPC2292/94.

Example a)

Module Configuration:

- Flash access time = 90 ns
- SRAM access time = 10 ns

BCFG0 Register Configuration Value: 0x02000 0060

IDCY	:	0	->	1 idle cycle
WST1	:	3	->	6 CCLK cycles
RBLE	:	0	->	0 non byte partitioned device
WST2	:	0	->	only for read access
BUSERR	:	0	->	not relevant
WPERR	:	0	->	no write protection error
WP	:	0	->	bank not write protected
BM	:	0	->	no burst ROM bank
MW	:	2	->	32-bit wide bus
AT	:	0	->	always write 0 to this field

BCFG1 Register Configuration Value: 0x02000 0400

IDCY	:	0	->	1 idle cycle
WST1	:	0	->	3 CCLK cycles
RBLE	:	1	->	byte partitioned device
WST2	:	0	->	only for read access
BUSERR	:	0	->	not relevant
WPERR	:	0	->	no write protection error
WP	:	0	->	bank not write protected
BM	:	0	->	no burst rom bank
MW	:	2	->	32-bit wide bus
AT	:	0	->	always write 0 to this field

Example b)

Module Configuration:

- Flash access time = 90 ns
- SRAM access time = 70 ns
- Ethernet access time = 25 ns

BCFG0 Register Configuration Value: 0x02000 0060

IDCY	:	0	->	1 idle cycle
WST1	:	3	->	6 CCLK cycles
RBLE	:	0	->	0 non byte partitioned device
WST2	:	0	->	only for read access
BUSERR	:	0	->	not relevant
WPERR	:	0	->	no write protection error
WP	:	0	->	bank not write protected
BM	:	0	->	no burst ROM bank
MW	:	2	->	32-bit wide bus
AT	:	0	->	always write 0 to this field

BCFG1 Register Configuration Value: 0x02000 1440

IDCY	:	0	->	1 idle cycle
WST1	:	2	->	5 CCLK cycles
RBLE	:	1	->	byte partitioned device
WST2	:	2	->	5 CCLK cycles
BUSERR	:	0	->	not relevant
WPERR	:	0	->	no write protection error
WP	:	0	->	bank not write protected
BM	:	0	->	no burst ROM bank
MW	:	2	->	32-bit wide bus
AT	:	0	->	always write 0 to this field

BCFG1 Register Configuration Value: 0x02000 0400

IDCY	:	0	->	1 idle cycle
WST1	:	0	->	3 CCLK cycles
RBLE	:	1	->	byte partitioned device
WST2	:	0	->	3 CCLK cycles
BUSERR	:	0	->	not relevant
WPERR	:	0	->	no write protection error
WP	:	0	->	bank not write protected
BM	:	0	->	no burst ROM bank
MW	:	2	->	32-bit wide bus
AT	:	0	->	always write 0 to this field

6 Serial Interfaces

6.1 RS-232 Interfaces

One RS-232 transceiver is populating the phyCORE-LPC2292/94 at U200. This device converts the signal levels for:

- P01/RxD0 and P00/TxD0 (frist serial interface)
- P09/RxD1 and P08/TxD1 (second serial interface)

The ports listed above can also be used alternatively as standard I/Os, as interface signals with TTL-level or in their alternative function on the phyCORE-connector X700. For this Jumpers J201 and J203 as well as J200 and J202 must be closed at position 2 + 3.

All RS-232 interfaces enable connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-LPC2292/94 circuitry needs to be connected to the applicable Ground pin on the COM port as well.

One of the microcontroller's on-chip UARTs (UART0) does not support handshake signal communication. However, depending on user needs, handshake communication can be software emulated using port pins on the microcontroller. The controllers second UART (UART1) supports standard modem signals. However, these signals are not converted to RS-232 signal level on the phyCORE-LPC2292/94. All modem signals are routed to the phyCORE-connector at X700. In order to support handshake communication with RS-232 signal level an external RS-232 transceiver is required. The applicable circuirty needs to be added by the user.

6.2 CAN Interface

The phyCORE-LPC2292/94 is designed to house two CAN transceivers at U605 and U606 (either PCA82C251 or TLE6250V33). The CAN bus transceiver devices support signal conversion of the CAN transmit (CANTx) and receive (CANRx)lines. The CAN transceiver supports up to 110 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). In order to ensure proper message transmission via the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus.

For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-LPC2292/94. This requires removal of the on-board CAN transceivers and routing the CANTx and CANRx lines to the phyCORE connector X700 by closing Jumpers J602, J603, J604 and J605. For connection of the CANTx and CANRx lines to an external transceiver we recommend using a Hewlett Packard HCPL06xx or a Toshiba TLP113 HCPL06xx fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1]: CiA: CAN in Automation. Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

7 Serial EEPROM (U607)

The phyCORE-LPC2292/94 is populated with a non-volatile memory with a serial interface (SPI interface) to store configuration data. According to the memory configuration of the module an EEPROM (1 to 8 kByte) can be mounted at U607. *A description of the SPI protocol can be found in the applicable EEPROM Data Sheet.*

Table 38 gives an overview of the memory components that can be used at U607 at the time of printing of this manual.

Device Type	Size	Component	Manufacturer
EEPROM	1 kByte (1024*8)	AT25080	Atmel
EEPROM	2 kByte (2048*8)	AT25160	Atmel
EEPROM	4 kByte (4096*8)	AT25320	Atmel
EEPROM	8 kByte (8192*8)	AT25640	Atmel

Table 38: Memory Device Options for U607

Various available EEPROM types provide a write protection function[1]. Jumper J606 is used to activate this function. If this jumper is closed, then pin 3 of the serial EEPROM is connected to GND. *Refer to section 3.15* for details on jumper settings for J606.

1: *Refer to the corresponding EEPROM Data Sheet for more information on the write protection function.*

8 On-Board Flash Memory (U300-U303)

Use of Flash as non-volatile memory on the phyCORE-LPC2292/94 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-LPC2292/94:

- 29LV800B with 1*16 kByte, 2*8 kByte, 1*32 kByte, 15*64 kByte
- 29LV160B with 1*16 kByte, 2*8 kByte, 1*32 kByte, 31*64 kByte
- 29LV320B with 8*8 kByte, 63*64 kByte

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

Use of a Flash device as the only code memory results in no or only a limited usability of the Flash memory as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash-internal programming process, the reading of data from Flash is not possible. Hence, for Flash programming, program execution must be transferred out of Flash (such as into von Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

If the phyCORE-LPC2292/94 is populated with multiple Flash devices on the available Flash banks it is possible to store application data in a Flash area which is physically seperated from the Flash area that contains program code.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

9 LAN91C111 Ethernet Controller (U501)

Connection of the phyCORE-LPC2292 to the world wide web or a local network is possible with the on-board SMSC LAN91C111 10/100 Mbps Ethernet controller populating the module at U501. This Ethernet controller features an integrated PHY layer. Thus the external components required to connect the phyCORE-LPC2292 to a LAN are limited to the transformer, the RJ45 socket and a few discrete components. The Ethernet chip is supported by a wide range of operating systems, such as Linux etc.

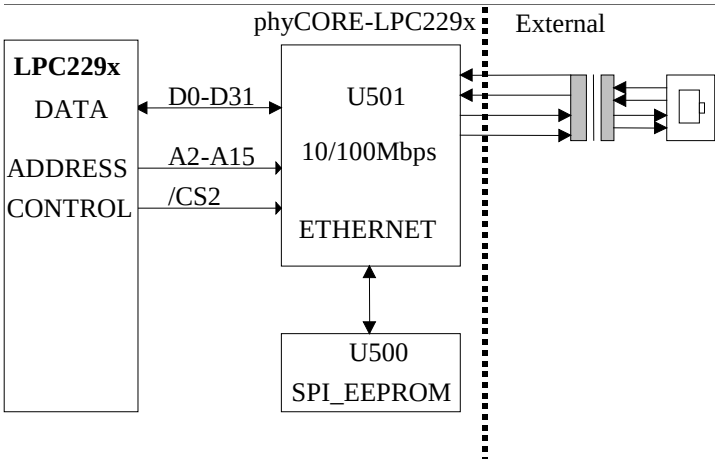


Figure 9: Ethernet Connection to LPC2292/94 Controller

The Ethernet controller is connected to the data bus with a 32-bit width and can be configured via Jumpers J501, J502 and J503. Jumper J501 is used to connect the interrupt signal of the LAN91C111 with a corresponding input on the LPC2292/94 processor. The interrupt is being used as active high edge triggered. The /CS signal for the LAN91C111 Ethernet controller at U501 can be connected to the LPC2292 processor's /CS2 or /CS3 signal using Jumper J502. The Ethernet controller's offset of 0x300 has to be noted when accessing the chip.

The Ethernet controller provides a READY output that can be connected to the P018 input of the controller using Jumper J503. It is also possible to combine various signal sources externally if multiple components need to use the processor's P018 input for READY indication. *Refer to section 3.12 for more details on applicable jumper settings and configuration options.*

The physical memory area for the Ethernet chip is defined in the following table. An offset of 0x300 has to be added to the address of /CS2 if Jumper J502 is closed at position 1+2 for accessing the LAN91C111.

Ethernet	**Start Address**
/CS2 + OFFSET	0x8200 0000 + 0x0000 0300 = 0x8200 0300

Table 39: Memory Area Ethernet Controller

9.1 MAC Address

The MAC (Media Access Control) address is a **unique** identification code of computer hardware operating within a LAN (Local Area Network). When connecting the hardware to the Internet the assigned IP number is mapped to the MAC address via a conversion table.

The MAC addresses are administered in a central location in order to ensure the uniqueness of these numbers. PHYTEC has purchased a pool of such MAC addresses and each one of our Ethernet-based Single Board Computers gets one of these addresses. The MAC address of your phyCORE-LPC2292/94 is printed on a barcode sticker attached to the module. The MAC address is provided as a 12-digit hexadecimal value. In addition, the MAC address is also programmed into the Ethernet controller EEPROM (U500) at the time of delivery. This allows immediate start-up of the module and its Ethernet hardware. Following a hardware-reset the MAC address is automatically loaded from the EEPROM into the Ethernet controller (*refer to section 9.2*).

9.2 Ethernet EEPROM (U500)

The EEPROM connected to the Ethernet controller can be used to store specific confguration data that are automatically loaded into the LAN91C111 following a hardware-reset. The EEPROM can be programmed on-board via the Ethernet controller. *Please refer to the SMSC LAN91C111 Ethernet controller datasheet for details.*

The MAC address is pre-programmed into the EEPROM (U500) at time of delivery (*refer to section 9.1*).

9.3 10/100Base-T Interface

The phyCORE-LPC2292/94 has been designed exclusively for operation in 10/100Base-T networks. The 10/100Base-T interface with its signals LAN_LEDA and LAN_LEDB extends to phyCORE-connector X1. The MII interface of the LAN91C111 is not available on the phyCORE-connector. However, these signals are routed to an optional connector X500 that populates the debugCORE-LPC2292 variant.

Additional external circuitry is required to connect the module to an existing 10/100Base-T network. It should be noted that the 3.3 V version of the LAN91C111 controller is used on the phyCORE-LPC2292/94. *Please refer to the SMSC Ethernet controller datasheet for details on the external circuitry design*. This circuitry is also available from PHYTEC on an Ethernet adapter module, order code EAD-003 (*refer to section 16*).

10 Battery Buffer

The connection of a battery buffer is not essential to the functioning of the phyCORE-LPC2292/94. However, this battery buffer embodies an economical and practical means of storing data in the SRAM devices. It is necessary to preserve data from the I^2C Real-Time Clock of the phyCORE-LPC2292/94 in case of a power failure.

The VBAT input at pin X700C6 of the board is provided for connecting the external battery. The negative polarity pin on the battery must be connected to GND on the phyCORE-LPC2292/94. As of the printing of this manual, a lithium battery is recommended as it offers relatively high capacity at low discharge. In the event of a power failure at VCC, the RTC will be buffered by a connected battery via VBAT. The RTC is generally supplied via VPD in order to preserve data by means of the battery back-up in the absence of a power supply via VCC.

The battery supply for the SRAM devices is configured with Jumper J402 *(refer to section 3.11)*. If the SRAM battery supply is enabled the user must ensure that the battery is capable of supplying both SRAM and RTC at runtime of the module.

Power consumption depends on the installed components and memory size (*see section 13, "Technical Specifications"*).

11 Debug Interface X701

The phyCORE-LPC2292/94 is equipped with a JTAG interface for downloading program code into the external Flash or for debugging programs in the external SRAM. The JTAG interface extends out to 2 mm pitch pin header rows X701 on the controller side of the module. *Figure 10* and *Figure 11* show the position of the debug interface (JTAG connector X701) on the phyCORE module.

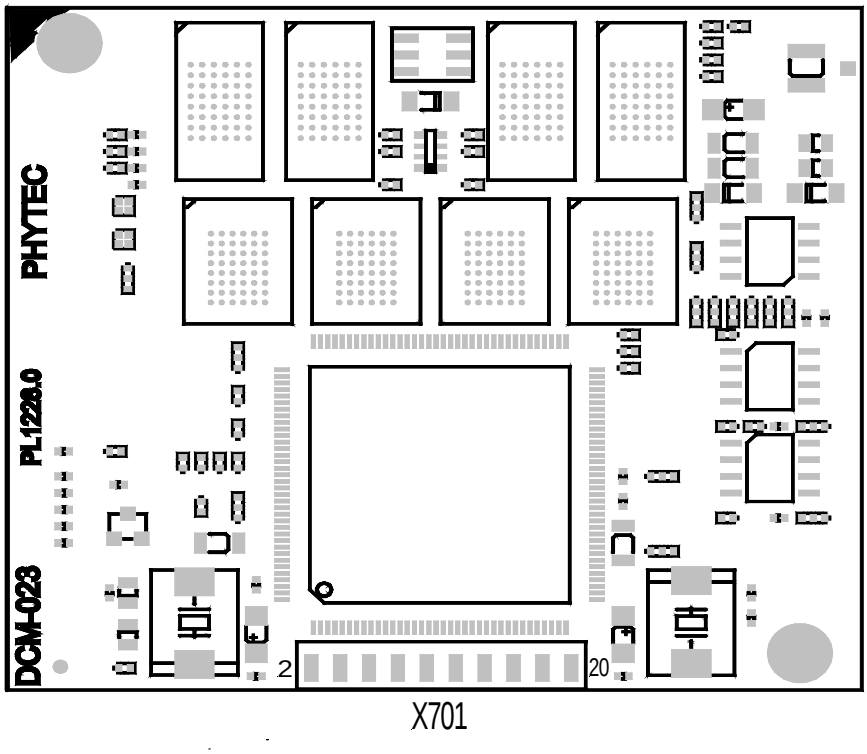


Figure 10: JTAG Interface (Top View)

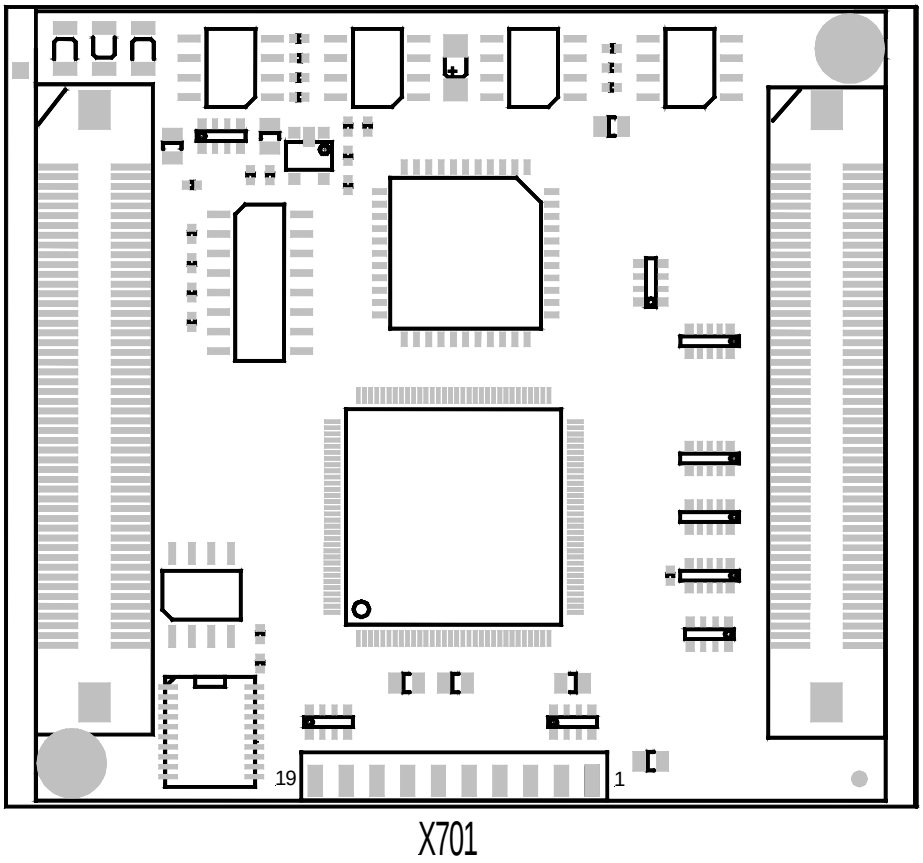


Figure 11: JTAG Interface (Bottom View)

Pin 1 of the JTAG concector X701 is marked by a black pad on the connector side of the PCB.

The JTAG interface of the phyCORE-LPC2292/94 can operate in various modes. On-board configuration resistors select if the corresponding port pins function as JTAG interface or as standard I/O port.

In addition to the standard JTAG port the phyCORE-LPC2292/94 also features a TRACE port which is also configured via on-board resistors. *Refer to section* ***Error! Reference source not found.*** *for details.*

The following configuration options are available:

R205	R206	JTAG/ETM Interface Function
unpopulated	populated	Port pins P1.26-P1.31 function as JTAG ICE interface
populated	unpopulated	Port pins P1.16-P1.25 function as ETM TRACE port
unpolulated	unpopulated	Port pins P1.16-P1.31 available as standard I/O port
populated	populated	Port pins P1.16-P1.31 function as JTAG and ETM TRACE port

Table 40: JTAG and TRACE Modes

Note:
The JTAG connector X701 only populates phyCORE-LPC2292/94 modules with order code PCM-023-D. This version of the phyCORE module is included in all Rapid Development Kits (order code KPCM-023). JTAG connector X701 is not populated on phyCORE modules with order code PCM-014 that are intended for OEM implementation. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See Table 71 for details on the JTAG signal pin assignment.*

PHYTEC offes a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-LPC2292/94 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X701 to standard Emulator connectors.

12 debugCORE-LPC2292/94

The debugCORE-LPC2292/94 is a special debugging version of the phyCORE-LPC2292/94 module. The debugCORE differs from its phyCORE counterpart, in that an additional debug interface and corresponding circuitry has been added. On the debugCORE-LPC2292/94 there is also the possibility of connecting the MII interface of the LAN91C111 Ethernet controller. The following images depict the debugCORE-LPC2292/94 with the debugCORE-specific expansion.

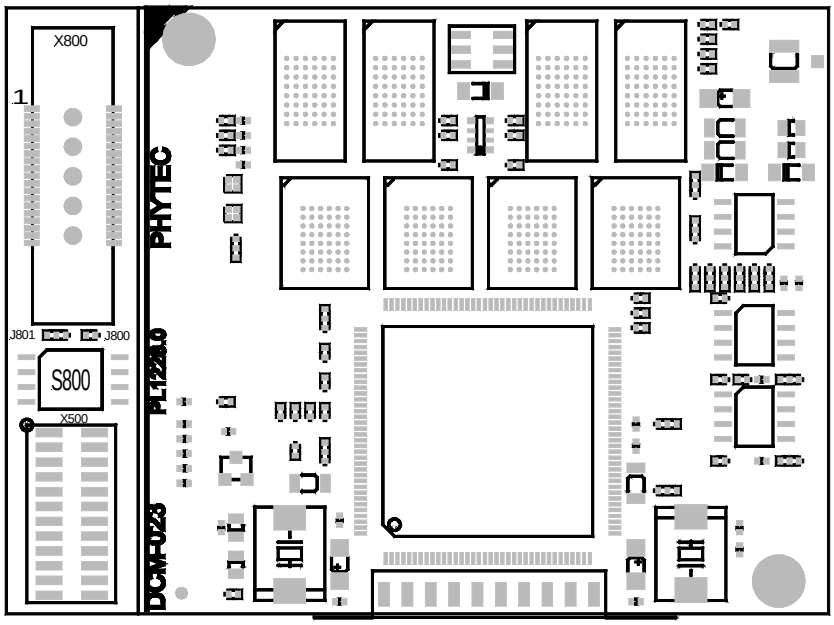


Figure 12: debugCORE-LPC2292/94 (Top View)

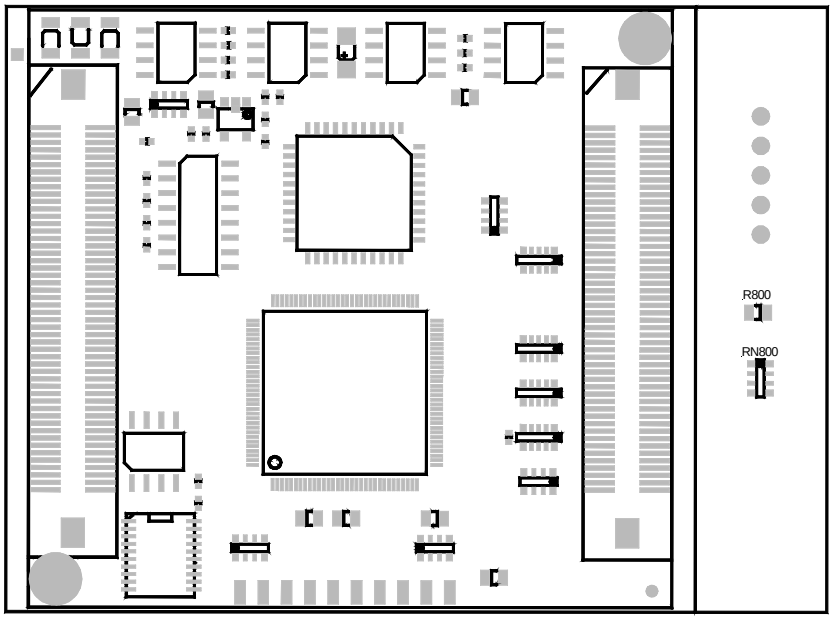


Figure 13: debugCORE-LPC2292/94 (Bottom View)

A DIP switch has been added to the configuration resistors already present on the phyCORE module to enable easier configuration of the controller's debug interface. When using the DIP switch for configuration, resistors R205 and R206 must be removed.

DIP switch S800 on the debugCORE-LPC2292/94 has the following configuration options:

DIP Switch	Open/OFF	Closed/ON
#1	Normal operation of the LPC2292/94	Boot mode always enabled
#2	Port pins P116-P125 function as standard I/O port	Port pins P116-P125 function as Trace port
#3	Port pins P126-P131 function as standard I/O port	Port pins P126-P131 function as debug interface
#4	reserved	reseverd

Table 41: debugCORE-LPC2292/94 DIP Switch S800

The pinout of the 38-pin (0.64 mm pitch) Embedded Trace Macrocell (ETM) and OCDS MICTOR connector at X800 is described below:

Pin Number	Signal	Description
1	/RESET	Low-active reset signal. Can be disconnected by opening Jumper J800.
2, 3, 4	N.C.	Not connected
5	GND	Ground
6	TRACECLK	Clock signal for trace port.
7, 8	N.C.	Not connected
9	/RESET	Low-active reset signal.
10	EXTIN0	External trigger input.
11	TDO	JTAG signal test data out.
12	VTREF	Can be connected to VCC (3.3V) or GND via Jumper J801.
13	RTCK	JTAG signal returned test clock output.
14	Vsupply	Can be connected to VCC (3.3V) or GND via Jumper J801.
15	TCK	JTAG signal test clock.
16, 18, 20, 22	GND	Ground
17	TMS	JTAG signal test mode select.
19	TDI	JTAG signal test data in.
21	/TRST	JTAG signal test reset.
23, 25, 27, 29, 31, 33, 35, 37	N.C.	Not connected
24	TRACEPKT3	Trace packet signal 3.
26	TRACEPKT2	Trace packet signal 2.
28	TRACEPKT1	Trace packet signal 1.
30	TRACEPKT0	Trace packet signal 0.
32	TRACESYNC	Trace synchronization signal.
34	PIPESTAT2	Pipe Line status signal 2.
36	PIPESTAT1	Pipe Line status signal 1.
38	PIPESTAT0	Pipe Line status signal 0.

Table 42: ETM/OCDS Connector at X800

The pinout of the 24-pin MII (0.64 mm pitch) connector at X500 is described below:

Pin Number	Signal	Description
1, 20, 21	VCC	3.3V supply voltage
2	LAN_MDI	MII management data input
3	LAN_MDO	MII management data output
4	LAN_MCLK	MII management clock
5	LAN_RXD3	Received data nibble from MII PHY, input
6	LAN_RXD2	Received data nibble from MII PHY, input
7	LAN_RXD1	Received data nibble from MII PHY, input
8	LAN_RXD0	Received data nibble from MII PHY, input
9	LAN_RX_DV	Envelope of data valid reception, MII PHY input
10	LAN_RX_ER	Code error detection by PHY input
11	LAN_RX25	Receive clock input from MII PHY
12	LAN_TX25	Transmit clock input from MII PHY
13	LAN_TXEN	Output to MII PHY
14	LAN_TXD0	Transmit data nibble to MII PHY, output
15	LAN_TXD1	Transmit data nibble to MII PHY, output
16	LAN_TXD2	Transmit data nibble to MII PHY, output
17	LAN_TXD3	Transmit data nibble to MII PHY, output
18	LAN_COL	Collision detect input from MII PHY.
19	LAN_CRS	Envelope of packet reception from MII PHY.
22, 23, 24	GND	Ground

Table 43: LAN MII Connector at X500

13 Technical Specifications

The physical dimensions of the phyCORE-LPC2292/94 are represented in *Figure 14*. The module's profile is ca. 7.2 mm thick, with a maximum component height of 2.6 mm on the bottom (connector) side of the PCB and approximately 3.0 mm on the top (microcontroller) side. The board itself is approximately 1.6 mm thick.

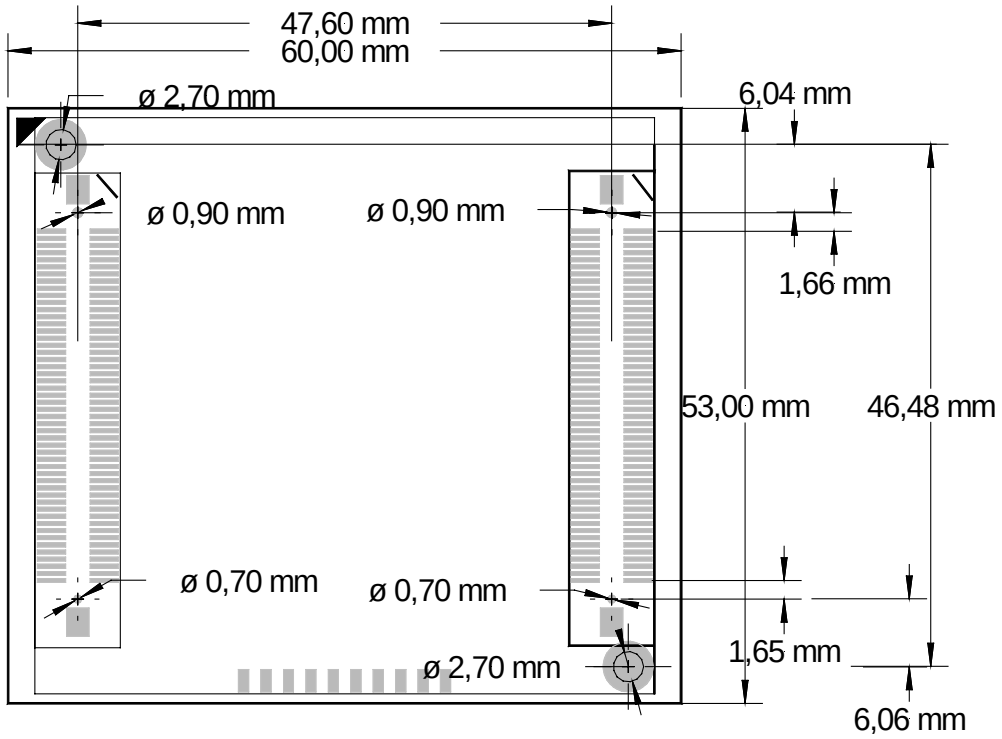


Figure 14: Physical Dimensions

Additional specifications:

• Dimensions:	60 mm x 53 mm
• Weight:	approximately 25 g with all optional components mounted on the circuit board
• Storage temperature:	-40°C to +90°C
• Operating temperature:	standard: 0°C to +70°C extended: -40°C to +85°C
• Humidity:	95 % r.F. not condensed
• Operating voltage:	VCC 3.3 V 5 %, VCC2 5 V 5 %, VBAT 3 V 20 %
• Power consumption: VCC1 3.3V/300mA typical VCC2 5.0V/12mA typical	Conditions: **VCC = 3.3 V, VBAT = 0 V**, 2 MByte fast SRAM, 4 MByte Flash, 10 MHz quartz, 60 Mhz CPU frequency at 20°C

These specifications describe the standard configuration of the phyCORE-LPC2292/94 as of the printing of this manual.

Please note that the module storage temperature is only 0°C to +70°C if a battery buffer is used for the RAM devices.

14 Hints for Handling the phyCORE-LPC2292/94

The address and data bus on the module is not buffered. To connect external components to the data/address bus, as well as the control lines (/RD, /WR), an external buffer (i.e. 74AHCT245) between the modul and the peripheral components should be installed.

The data bus D0…31 (Port 0) should be connected with a 100 kΩ pull-up resistor against VCC.

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

15 The phyCORE-LPC2292/94 on the phyCORE Development Board HD200

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in labratory environments prior to their use in customer designed applications.

15.1 Concept of the phyCORE Development Board HD200

The phyCORE Development Board HD200 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-LPC2292/94 Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in *Figure 15* and includes the following components:

- The actual **Development Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors (depending on the module, up to two RS-232 interfaces and up to two RS-485 or CAN interfaces).
- All of the signals from the SBC module mounted on the Development Board extend to two mating receptacle connectors. A strict 1:1 signal assignment is consequently maintained from the phyCORE-connectors on the module to these expansion connectors. Accordingly, the pin assignment of the **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Development Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Development Boards, we are able to offer various **expansion boards** (5) that attach to the Development Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Development Board.
- All controller and on-board signals provided by the SBC module mounted on the Development Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Development Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 15 illustrates the modular development platform concept:

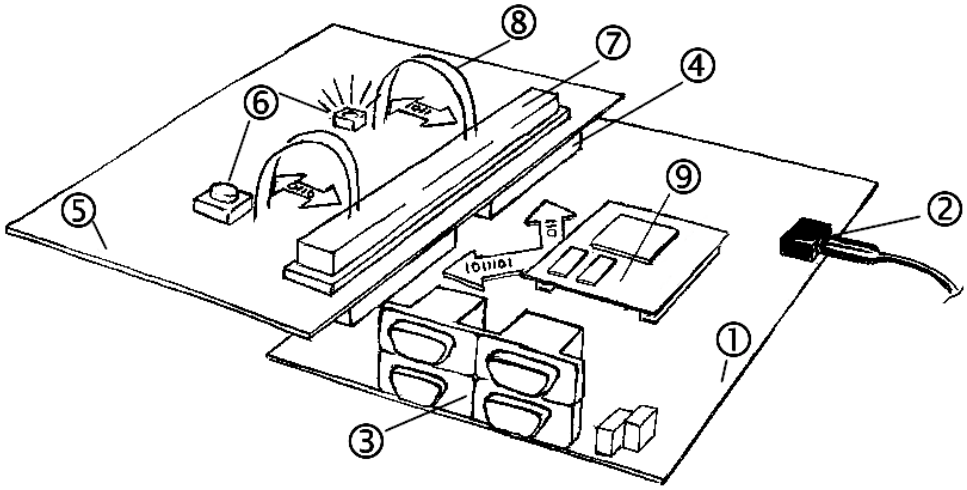


Figure 15: Modular Development and Expansion Board Concept with the phyCORE-LPC2292/94

The following sections contain specific information relevant to the operation of the phyCORE-LPC2292/94 mounted on the phyCORE Development Board HD200. For a general description of the Development Board, please refer to the corresponding Development Board Hardware Manual.

15.2 Development Board HD200 Connectors and Jumpers

15.2.1 Connectors

As shown in *Figure 16*, the following connectors are available on the phyCORE Development Board HD200:

X1- low-voltage socket for power supply connectivity
X2- mating receptacle for expansion board connectivity
P1- dual DB-9 sockets for serial RS-232 interface connectivity
P2- dual DB-9 connectors for CAN or RS-485 interface connectivity
X4- voltage supply for external devices and subassemblies
X5- GND connector (for connection of GND signal of measuring devices such as an oscilliscope)
X6- phyCORE-connector enabling mounting of applicable phyCORE modules
X7- interface for Ethernet transformer module EAD-003
U9/U10- space for an optional silicon serial number chip
BAT1- receptacle for an optional battery

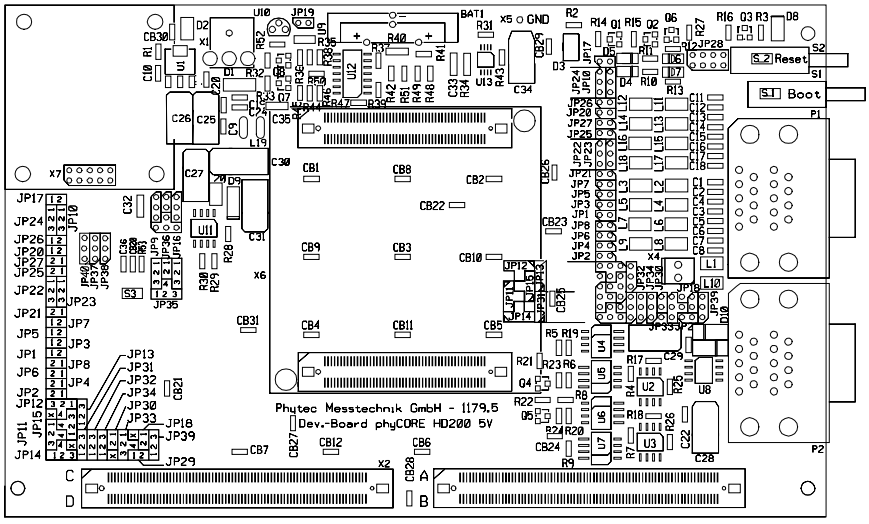


Figure 16: Location of Connectors on the phyCORE Development Board HD200

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

15.2.2 Jumpers on the phyCORE Development Board HD200

Peripheral components of the phyCORE Development Board HD200 can be connected to the signals of the phyCORE-LPC2292/94 by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-LPC2292/94 by means of insertable jumpers. If no jumpers are set, no signals connect to the DB-9 connectors, the control and display units and the CAN transceivers. The Reset input on the phyCORE-LPC2292/94 directly connects to the Reset button (S2). *Figure 17* illustrates the numbering of the jumper pads, while *Figure 18* indicates the location of the jumpers on the Development Board.

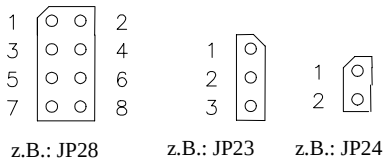


Figure 17: Numbering of Jumper Pads

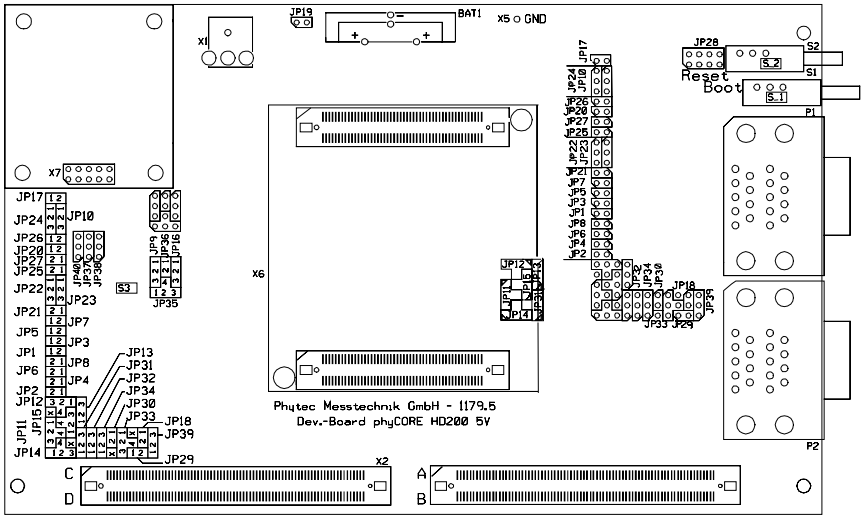


Figure 18: Location of the Jumpers (View of the Component Side)

Figure 19 shows the factory default jumper settings for operation of the phyCORE Development Board HD200 with the standard phyCORE-LPC2292/94 (standard = LPC2292 controller, use of first and second RS-232 and CAN interfaces and LED D3 on the Development Board). Jumper settings for other functional configurations of the phyCORE-LPC2292/94 module mounted on the Development Board are described in *section 15.3*.

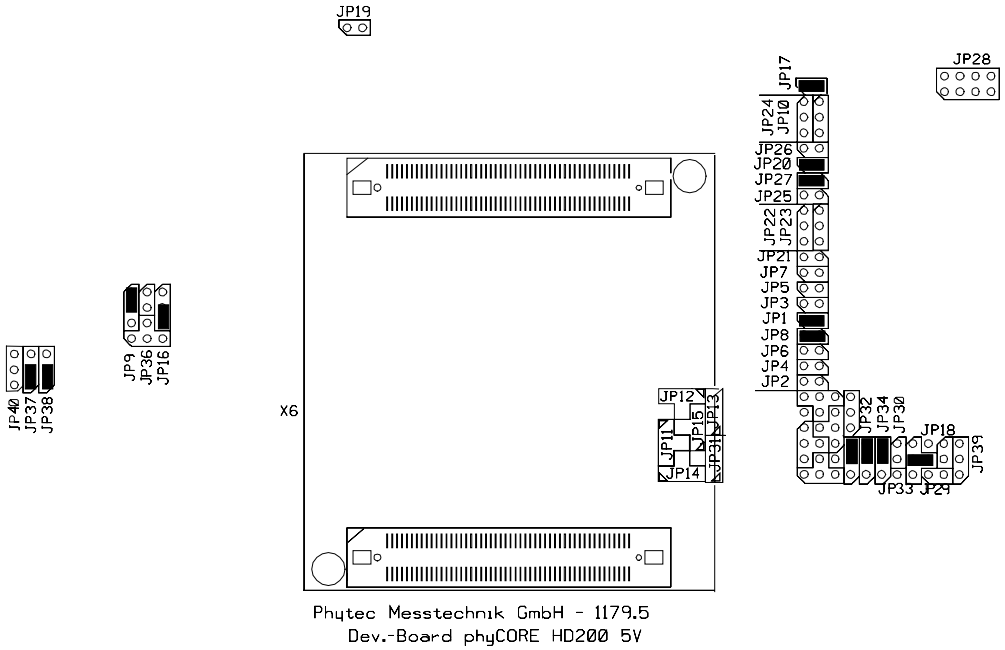


Figure 19: Default Jumper Settings of the phyCORE Development Board HD200 with phyCORE-LPC2292/94

15.2.3 Unsupported Features and Improper Jumper Settings

The following table contains improper jumper settings for operation of the phyCORE-LPC2292/94 on a phyCORE Development Board HD200. Functions configured by these settings are not supported by the phyCORE module.

No RS-485 interface:

DB-9 plug P2B on the Development Board can be configured as RS-485 interface as an alternative to the second CAN interface. The phyCORE-LPC2292/94 does not support an RS-485 interface. For this reason the corresponding jumper settings should never be used.

Jumper	Setting	Description
JP30	closed	TxD signal for second serial interface routed to pin 8 on the DB-9 plug P2B
JP33	1 + 2	RxD signal for second serial interface routed to pin 2 on the DB-9 plug P2B

Table 44: Improper Jumper Setting for JP30/33 on the Development Board

Reference Voltage Source for A/D Converter

Pins X1C42, X1C47, X1D44 and X1D49 (VAGND) of the phyCORE-LPC2292/94 are solely connected with the phyCORE Development Board HD200 GND potential. This makes a separate supply with an alternative VAGND potential impossible. Free definition of the VAGND potential is however available in a customer application board.

15.3 Functional Components on the phyCORE Development Board HD200

This section describes the functional components of the phyCORE Development Board HD200 supported by the phyCORE-LPC2292/94 and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-LPC2292/94 module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 19* and enable alternative or additional functions on the phyCORE Development Board HD200 depending on user needs.

15.3.1 Power Supply at X1

Caution:
Do not use a laboratory adapter to supply power to the Development Board! Power spikes during power-on could destroy the phyCORE module mounted on the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +/-5 VDC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-LPC2292/94 mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 500 mA is recommended.

Jumper	Setting	Description
JP9	1 + 2	3.3 V primary main supply voltage to the phyCORE-LPC2292/94
JP16	2 + 3	5 V as secondary main supply voltage to the phyCORE-LPC2292/94

Table 45: JP9, JP16 Configuration of the Main Supply Voltages VCC / VCC2

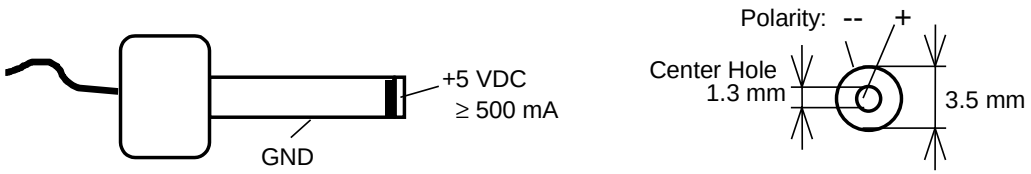


Figure 20: Connecting the Supply Voltage at X1

Caution:
When using this function, the following jumper settings are not allowed:

Jumper	Setting	Description
JP9	2 + 3	5 V as primary main supply voltage for the phyCORE-LPC2292/94
	open	phyCORE-LPC2292/94 not connected to primary main supply voltage
JP16	1 + 2	3.3 V as secondary main supply voltage for the phyCORE-LPC2292/94
	open	phyCORE-LPC2292/94 not connected to secondary main supply voltage **NOTE: This setting is correct if the module in its minimum configuration without on-board CAN transceivers is used.**

Table 46: JP9, JP16 Improper Jumper Settings for the Main Supply Voltages

Setting Jumper JP9 to position 2+3 configures a primary main power supply to the phyCORE-LPC2292/94 of 5 V which could destroy the module. Setting Jumper JP16 to position 1 + 2 configures a secondary main power supply to the phyCORE-LPC2292/94 of 3.3 V which also can damage the module. If Jumper JP9 and JP16 remain open, no primary and secondary main power supply is connected to the phyCORE-LPC2292/94. These jumper settings should therefore not be used.

15.3.2 Starting the ISP Command Handler

The Philips LPC229x microcontroller family contains an on-chip boot loader that provides both In-System (ISP) and In-Application programming (IAP) interfaces. The loader can execute an ISP command handler or the user application. The combination of this ISP handler and the corresponding LPC2000 Flash Utility software installed on the PC allows for on-chip Flash programming with application code via an RS-232 interface.

In order to start the ISP command handler on the phyCORE-LPC2292/94, port P0.14 of the microcontroller must be connected to a low signal level at the time the Reset signal changes from its active to the inactive state. This is achieved by applying a high-level signal at pin X1C9 (BOOT) of the phyCORE-LPC2292/94. A transistor circuitry connects P0.14 to GND as long as the BOOT pin is high. An on-board pull-up resistor (R213) ensures a high level at P0.14 if the BOOT signal is not active. *Refer to the Philips LPC229x User Manual, section 20 for more details.*

The phyCORE Development Board HD200 provides two different options to activate the ISP mode:

1. The Boot button (S_1) can be connected to VCC via Jumper JP28 which is located next to the Boot and Reset buttons at S_1 and S_2. This configuration enables start-up of the ISP command handler if the Boot button is pressed during a hardware reset or power-on.

Jumper	Setting	Description
JP28	6 + 8 and 3 + 4	Boot button (in conjunction with Reset button or connection of the power supply) starts the ISP mode on the LPC2292/94

Table 47: JP28 Configuration of the Boot Button

2. The Boot input of the phyCORE-LPC2292/94 can also be permanently connected to VCC via a pull-up resistor. This pulls port pin P0.14 to low level via on-board circuitry which then starts the ISP mode. This spares pushing the Boot button during a hardware reset or power-on.

Caution:
In this configuration a regular reset, hence normal start of your application, is not possible. The microcontroller will always enter ISP mode after reset.

Jumper	Setting	Description
JP28	4 + 6	Boot input connected permanently with VCC via pull-up resistor. The ISP command handler is always started with reset or with connection of the power supply

Table 48: JP28 Configuration of a Permanent ISP Mode Start

15.3.3 First Serial Interface at Socket P1A

Socket P1A is the lower socket of the double DB-9 connector at P1. P1A is connected via jumpers to the first serial interface of the phyCORE-LPC2292/94.

Jumper	Setting	Description
JP20	closed	Pin 2 of DB-9 socket P1A connected with RS-232 signal TxD0 of the phyCORE-LPC2292/94
JP21	open	Pin 9 of DB-9 socket P1A not connected
JP22	open	Pin 7 of DB-9 socket P1A not connected
JP23	open	Pin 4 of DB-9 socket P1A not connected
JP24	open	Pin 6 of DB-9 socket P1A not connected
JP25	open	Pin 8 of DB-9 socket P1A not connected
JP26	open	Pin 1 of DB-9 socket P1A not connected
JP27	closed	Pin 3 of DB-9 socket P1A connected with RS-232 signal RxD0 from the phyCORE-LPC2292/94

Table 49: Jumper Configuration for the First RS-232 Interface

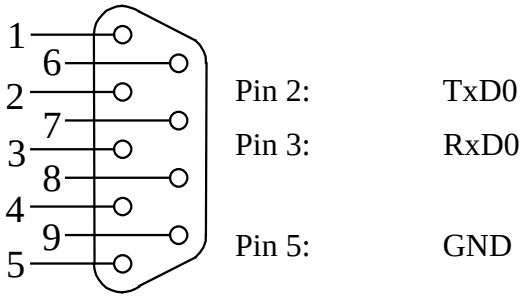


Figure 21: Pin Assignment of the DB-9 Socket P1A as First RS-232 (Front View)

Caution:
When using the DB-9 socket P1A as RS-232 interface on the phyCORE-LPC2292/94 the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP20	open	Pin 2 of DB-9 socket P1A not connected, no connection to TxD0 signal from phyCORE-LPC2292/94
JP21	closed	Pin 9 of DB-9 socket P1A connected with port P1.20 from phyCORE-LPC2292/94
JP22	1 + 2	Pin 7 of DB-9 socket P1A connected with port P1.17 from phyCORE-LPC2292/94
JP23	1 + 2	Pin 4 of DB-9 socket P1A connected with MISO0 signal from phyCORE-LPC2292/94
JP24	1 + 2	Pin 6 of DB-9 socket P1A connected with SCLK0 signal from phyCORE-LPC2292/94
	2 + 3	Pin 6 of DB-9 socket P1A connected with VOUT from Development Board HD200
JP25	Closed	Pin 8 of DB-9 socket P1A connected with port P1.16 from phyCORE-LPC2292/94
JP26	closed	Pin 1 of DB-9 socket P1A connected with port P1.21 from phyCORE-LPC2292/94
JP27	open	Pin 3 of DB-9 socket P1A not connected, no connection to RxD0 signal from phyCORE-LPC2292/94

Table 50: Improper Jumper Settings for DB-9 Socket P1A as First RS-232

If an RS-232 cable is connected to P1A, the voltage level on the RS-232 lines could destroy the phyCORE-LPC2292/94.

15.3.4 Power Supply to External Devices via Socket P1A

The phyCORE Development Board HD200 can be populated by additional components that provide a supply voltage of 5 V at pin 6 of DB-9 socket P1A. This allows for easy and secure supply of external devices connected to P1A. This power supply option especially supports connectivity to analog and digital modems. Such modem devices enable global communication of the phyCORE-LPC2292/94 over the Internet or a direct dial connection.

The following figure shows the location of these components on the Development Board:

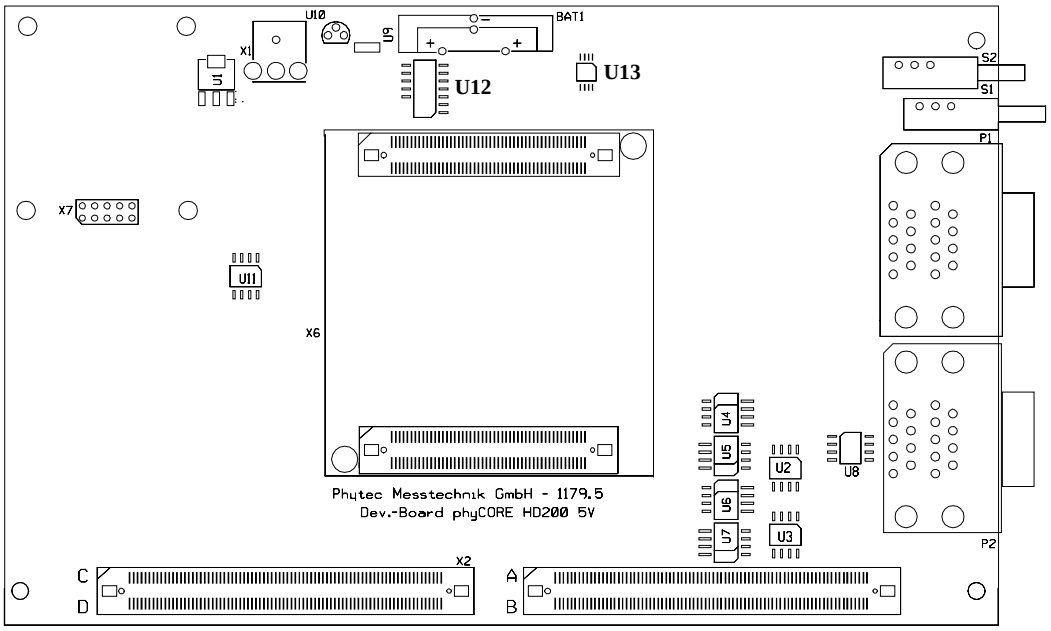


Figure 22: Location of Components at U12 and U13 for Power Supply to External Subassemblies

The components at U12 and U13 guarantee electronic protection against overvoltage and excessive current draw at pin 6 of P1A; in particular:

- Load detection and controlled voltage supply switch-on:

  In order to ensure clear detection of the switch-on condition, the connected device should cause a current draw of at least 10 mA at pin 6. The controlled voltage supply switch-on prevents voltage drop off on the phyCORE Development Board HD200.

- Overvoltage Protection:

  If the voltage at pin 6 exceeds the limiting value that can be provided by the phyCORE Development Board HD200, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 as well as connected modules and expansion boards.

- Overload Protection:

  If the current draw at pin 6 exceeds the limiting value of approximately 150 mA, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 and its power adapter caused by current overload.

This configuration option provides the following possibility:

Jumper	Setting	Description
JP24	2 + 3	Electronically protected 5 V at pin 6 for supply of external devices connected to P1A

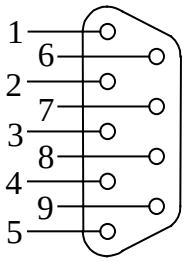
Table 51: JP24 Power Supply to External Devices Connected to P1A on the Development Board

15.3.5 Optional Second Serial Interface at Socket P1B[1]

Socket P1B is the upper socket of the double DB-9 connector at P1[1]. P1B is connected via jumpers to the second serial interface of the phyCORE-LPC2292/94. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the second serial interface (*refer to section 3.1*).

Jumper	Setting	Description
JP1	closed	Pin 2 of DB-9 socket P1B connected with RS-232 signal TxD1_RS232[2] of the phyCORE-LPC2292/94
JP2	open	Pin 9 of DB-9 socket P1B not connected
JP3	open	Pin 7 of DB-9 socket P1B not connected
JP4	open	Pin 4 of DB-9 socket P1B not connected
JP5	open	Pin 6 of DB-9 socket P1B not connected
JP6	open	Pin 8 of DB-9 socket P1B not connected
JP7	open	Pin 1 of DB-9 socket P1B not connected
JP8	closed	Pin 3 of DB-9 socket P1B connected with RS-232 signal RxD1_RS232[3] of the phyCORE-LPC2292/94

Table 52: Jumper Configuration of the DB-9 Socket P1B (Second RS-232)



Pin 2: TxD1
Pin 3: RxD1
Pin 5: GND

Figure 23: Pin Assignment of the DB-9 Socket P1B as Second RS-232 (Front View)

[1]: This second CAN DB-9 socket is NOT available on the standard Rapid Development Kit version KPCM-023-xxx since these Development Boards only offer single DB-9 connectors.

[2]: Check configuration of Jumper J200 on the phyCORE-LPC2292, *refer to section 3.1*.

[3]: Check configuration of Jumper J202 on the phyCORE-LPC2292, *refer to section 3.1*.

Caution:
When using the DB-9 socket P1B with the configuration of the phyCORE-LPC2292/94 as described above the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP1	open	Pin 2 of DB-9 socket P1B not connected, no connection to TxD1 signal from phyCORE-LPC2292/94
JP2	closed	Pin 9 of DB-9 socket P1B connected with port P1.18 from phyCORE-LPC2292/94
JP3	closed	Pin 7 of DB-9 socket P1B connected with port P0.22 from phyCORE-LPC2292/94
JP4	closed	Pin 4 of DB-9 socket P1B connected with port /PCS0 from phyCORE-LPC2292/94
JP5	closed	Pin 6 of DB-9 socket P1B connected with MOSI0 signal from phyCORE-LPC2292/94
JP6	closed	Pin 8 of DB-9 socket P1B connected with port P0.21 from phyCORE-LPC2292/94
JP7	closed	Pin 1 of DB-9 socket P1B connected with port P1.19 from phyCORE-LPC2292/94
JP8	open	Pin 3 of DB-9 socket P1B not connected, no connection to RxD1_ext. signal from phyCORE-LPC2292/94

Table 53: Improper Jumper Settings for DB-9 Socket P1B (Second RS-232)

If an RS-232 cable is connected to P1B by mistake, the voltage level on the RS-232 lines could destroy the phyCORE-LPC2292/94.

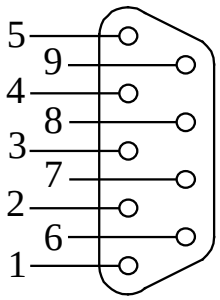
15.3.6 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (CAN1) of the phyCORE-LPC2292/94 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-LPC2292/94 is populated and the CAN signals from the module extend directly to plug P2A.

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of the DB-9 plug P2A is connected to CAN_L1 from on-board transceiver on the phyCORE module
JP32	2 + 3	Pin 7 of the DB-9 plug P2A is connected to CAN_H1 from on-board transceiver on the phyCORE module
JP11	open	Input at opto-coupler U4 on the phyCORE Development Board HD200 open
JP12	open	Output at opto-coupler U5 on the phyCORE Development Board HD200 open
JP13	open	No supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP18	open	No GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 54: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the phyCORE-LPC2292/94



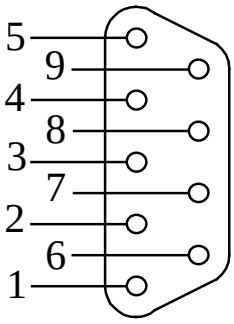
Pin 3: GND (Development Board Ground)
Pin 7: CAN_H1 (not galvanically separated)
Pin 2: CAN_L1 (not galvanically separated)
Pin 6: GND (Development Board Ground)

Figure 24: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on phyCORE-LPC2292/94, Front View)

2. No CAN transceiver is populating the phyCORE-LPC2292/94 and Jumpers J602 and J604 are closed; CAN signals generated by the CAN transceiver (U2) on the Development Board extending to connector P2A **without galvanic seperation:**

Jumper	Setting	Description
JP31	1 + 2[1]	Pin 2 of the DB-9 plug P2A is connected to CAN_L1 from transceiver on the Development Board HD200
JP32	1 + 2[1]	Pin 7 of the DB-9 plug P2A is connected to CAN_H1 from transceiver on the Development Board HD200
JP11	2 + 4	Input at opto-coupler U4 on the phyCORE Development Board HD200 connected with CAN_H1/TD1 of the phyCORE-LPC2292/94
JP12	2 + 4	Output at opto-coupler U5 on the phyCORE Development Board HD200 connected with CAN_L1/RD1 of the phyCORE-LPC2292/94
JP13	2 + 3	Supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP18	1 + 2	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 55: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN_H1 (not galvanically separated)
Pin 2: CAN_L1 (not galvanically separated)
Pin 6: GND (Development Board Ground

Figure 25: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-LPC2292/94 is not populated and Jumpers J602 and J604 are closed (*refer to section 3.14 for details*).

Caution:
When using the DB-9 connector P2A as CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with RD1 of the phyCORE-LPC2292/94
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with TD1 of the phyCORE-LPC2292/94
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SCLK0 of the phyCORE-LPC2292/94
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to A22 of the phyCORE-LPC2292/94
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to MISO0 of the phyCORE-LPC2292/94
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to A21 of the phyCORE-LPC2292/94
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	*see Table 58*	CAN bus supply voltage reduction for CAN circuitry

Table 56: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on the Development Board)

3. The CAN transceiver is not populated on the phyCORE-LPC2292/94 and Jumpers J602 and J604 are closed; CAN signals generated by the CAN transceiver (U2) on the Development Board extend to connector P2A **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP31	1 + 2	Pin 2 of DB-9 plug P2A connected with CAN_L1 from CAN transceiver U2 on the Development Board
JP32	1 + 2	Pin 7 of DB-9 plug P2A connected with CAN_H1 from CAN transceiver U2 on the Development Board
JP11	2 + 4[1]	Input at opto-coupler U4 on the Development Board connected to CAN_H1/TD1 of the phyCORE-LPC2292/94
JP12	2 + 4[1]	Output at opto-coupler U5 on the Development Board connected to CAN_L1/RD1 of the phyCORE-LPC2292/94
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	*see Table 58*	CAN bus supply voltage reduction for CAN circuitry

Table 57: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board with Galvanic Separation

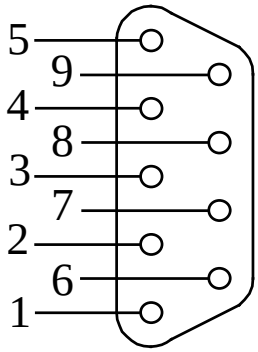
1: Please make sure the CAN transceiver on the phyCORE-LPC2292/94 is not populated and Jumpers J602 and J604 are closed (*refer to section 3.14 for details*).

CAN Bus Voltage Supply Reduction via JP39:

Depending on the voltage level that is supplied over the CAN bus at P2A or P2B (VCAN_IN1+) JP39 must be configured in order to routed the applicable voltage to the CAN voltage regulator at U8 on the Development Board:

VCAN_IN+	**JP39**
7 V..18 V	1 + 2
18 V..23 V	2 + 3
23 V..28 V	open

Table 58: JP39 CAN Bus Voltage Supply Reduction



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN_H1 (galvanically separated)
Pin 2: CAN_L1 (galvanically separated)
Pin 6: VCAN-

Figure 26: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

Caution:
When using the DB-9 plug P2A as CAN interface, and the CAN transceiver on the Development Board with galvanic separation, the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with RD1 of the phyCORE-LPC2292/94
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with TD1 of the phyCORE-LPC2292/94
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SCLK0 of the phyCORE-LPC2292/94
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to A22 of the phyCORE-LPC2292/94
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to MISO0 of the phyCORE-LPC2292/94
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to A21 of the phyCORE-LPC2292/94
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	see *Table 58*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 59: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

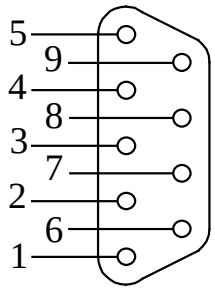
15.3.7 Optional Second CAN Interface at Plug P2B[1]

Plug P2B is the upper plug of the double DB-9 connector at P2[1]. P2B is connected to the second CAN interface (CAN2) of the phyCORE-LPC2292/94 via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-LPC2292/94 and the CAN signals from the module extend directly to plug P2B.

Jumper	Setting	Description
JP33	2 + 4	Pin 2 of the DB-9 plug P2B is connected to CAN_L2 from on-board transceiver on the phyCORE module
JP34	2 + 3	Pin 7 of the DB-9 plug P2B is connected to CAN_H2 from on-board transceiver on the phyCORE module
JP14	open	Input at opto-coupler U6 on the phyCORE Development Board HD200 open
JP15	open	Output at opto-coupler U7 on the phyCORE Development Board HD200 open
JP13	open	CAN transceiver and opto-coupler on the Development Board disconnected from supply voltage
JP18	open	No GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 60: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the phyCORE-LPC2292/94



Pin 3: GND (Development Board Ground)
Pin 7: CAN_H2 (not galvanically separated)
Pin 2: CAN_L2 (not galvanically separated)
Pin 6: GND (Development Board Ground)

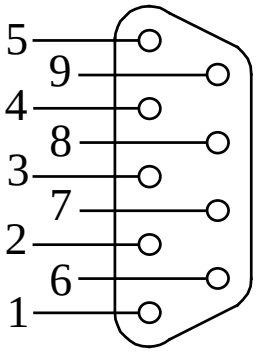
Figure 27: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on phyCORE-LPC2292/94, Front View)

[1]: This second CAN DB-9 plug is NOT available on the standard Rapid Development Kit version KPCM-023-xxx since these Development Boards only offer single DB-9 connectors.

2. No CAN transceiver is populating the phyCORE-LPC2292/94 and Jumpers J603 and J605 are closed; CAN signals generated by the CAN transceiver (U3) on the Development Board extending to connector P2B **without galvanic seperation:**

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of the DB-9 plug P2B is connected to CAN_L2 of CAN transceiver U3 of the Development Board HD200
JP34	1 + 2	Pin 7 of the DB-9 plug P2B is connected to CAN_H2 of CAN transceiver U3 of the Development Board HD200
JP14	2 + 4[1]	Input at opto-coupler U6 on the Development Board connected to CAN_H2/TD2 of the phyCORE-LPC2292/94
JP15	2 + 4[1]	Output at opto-coupler U7 on the Development Board connected to CAN_L2/RD2 of the phyCORE-LPC2292/94
JP13	closed	CAN transceiver and opto-coupler on the Development Board connected with 5 V supply voltage
JP18	closed	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 61: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN_H2 (not galvanically separated)
Pin 2: CAN_L2 (not galvanically separated)
Pin 6: GND (Development Board Ground

Figure 28: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-LPC2292/94 is not populated and Jumpers J603 and J605 are closed (*refer to section 3.14 for details*).

Caution:
When using the DB-9 connector P2B as second CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TxD1_ext from the phyCORE-LPC2292/94
JP33	1 + 2	Pin 2 at P2B is connected with RxD1_ext from the phyCORE-LPC2292/94
	2 + 4	Pin 2 at P2B is connected with CAN_L2/RD2 from the on-board CAN transceiver on the phyCORE-LPC2292/94
JP34	2 + 3	Pin 7 at P2B is connected with CAN_H2/TD2 from the on-board CAN transceiver on the phyCORE-LPC2292/94
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to P1.21 of the phyCORE-LPC2292/94
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to A23 of the phyCORE-LPC2292/94
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to P1.20 of the phyCORE-LPC2292/94
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to A20 of the phyCORE-LPC2292/94
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	see *Table 58*	CAN bus supply voltage reduction for CAN circuitry

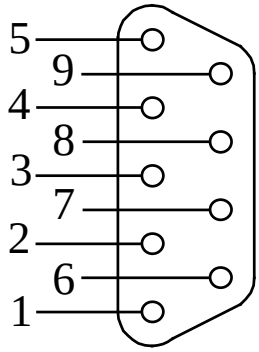
Table 62: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on the Development Board)

3. The CAN transceiver is not populating the phyCORE-LPC2292/94 and Jumpers J603 and J605 are closed; CAN signals generated by the CAN transceiver (U3) on the Development Board extend to connector P2B **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of DB-9 plug P2B connected with CAN_L2 from CAN transceiver U3 on the Development Board
JP34	1 + 2	Pin 7 of DB-9 plug P2B connected with CAN_H2 from CAN transceiver U3 on the Development Board
JP14	2 + 4[1]	Input at opto-coupler U6 on the Development Board connected to CAN_H2/TD2 of the phyCORE-LPC2292/94
JP15	2 + 4[1]	Output at opto-coupler U7 on the Development Board connected to CAN_L2/RD2 of the phyCORE-LPC2292/94
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	*see Table 58*	CAN bus supply voltage reduction for CAN circuitry

Table 63: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board with Galvanic Separation

1: Please make sure the CAN transceiver on the phyCORE-LPC2292/94 is not populated and Jumpers J603 and J605 are closed (*refer to section 3.14 for details*).



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H1 (galvanically separated)
Pin 2: CAN-L1 (galvanically separated)
Pin 6: VCAN-

Figure 29: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

Caution:
When using the DB-9 plug P2B as second CAN interface, and the CAN transceiver on the Development Board with galvanic separation, the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TxD1_ext from the phyCORE-LPC2292/94
JP33	1 + 2	Pin 2 at P2B is connected with RxD1_ext from the phyCORE-LPC2292/94
	2 + 4	Pin 2 at P2B is connected with CAN_L2/RD2 from the phyCORE-LPC2292/94
JP34	2 + 3	Pin 7 at P2B is connected with CAN_H2/TD2 from the phyCORE-LPC2292/94
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to P1.21 of the phyCORE-LPC2292/94
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to A23 of the phyCORE-LPC2292/94
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to P1.20 of the phyCORE-LPC2292/94
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to A20 of the phyCORE-LPC2292/94
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	*see Table 58*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 64: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

15.3.8 Programmable LED D3

The phyCORE Development Board HD200 offers a programmable LED at D3 for user implementations. This LED can be connected to port pin P0.8 (TxD1) of the phyCORE-LPC2292/94 which is available via signal GPIO0 (JP17 = closed). A low-level at port pin P0.8 causes the LED to illuminate, LED D3 remains off when writing a high-level to P0.8.

Jumper	Setting	Description
JP17	closed	Port pin P0.8 (GPIO0) of the LPC2292/94 controls LED D3 on the Development Board

Table 65: JP17 Configuration of the Programmable LED D3

15.3.9 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 15.1*, all signals from the phyCORE-LPC2292/94 extend in a strict 1:1 assignment to the Expansion Bus connector X2 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X2.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X2 on the Development Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

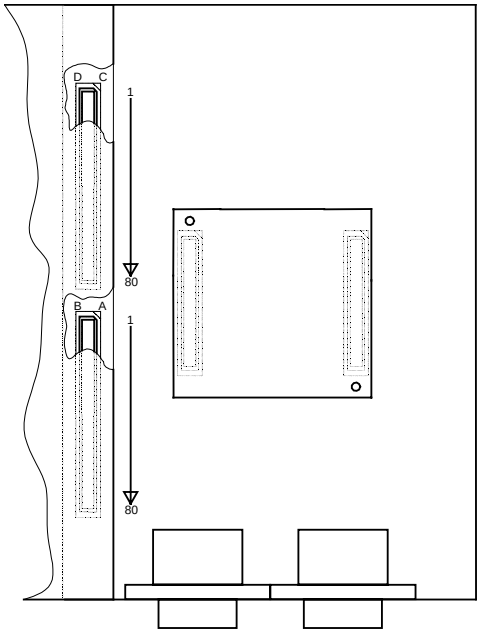


Figure 30: Pin Assignment Scheme of the Expansion Bus

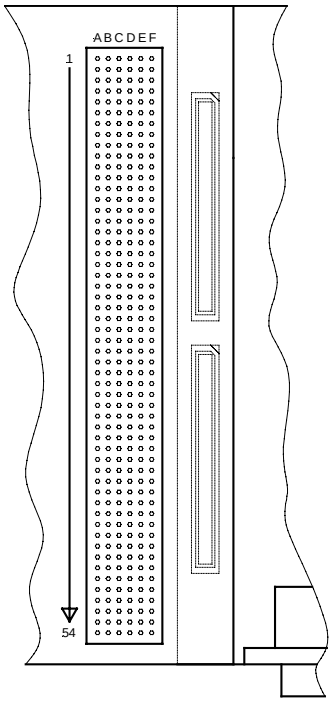


Figure 31: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-LPC2292/94, in conjunction with the Expansion Bus (X2) on the Development Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
D0	18B	18B	33F
D1	19A	19A	34A
D2	20A	20A	34E
D3	20B	20B	34B
D4	21A	21A	34D
D5	21B	21B	34F
D6	22B	22B	35A
D7	23A	23A	35E
D8	28B	28B	37C
D9	29A	29A	37E
D10	30A	30A	37B
D11	30B	30B	37F
D12	31A	31A	38A
D13	31B	31B	38C
D14	32B	32B	38E
D15	33A	33A	38B
D16	37B	37B	40A
D17	38A	38A	40E
D18	38B	38B	40B
D19	39A	39A	40D
D20	40A	40A	40F
D21	40B	40B	41A
D22	41A	41A	41E
D23	41B	41B	41B
D24	42B	42B	41F
D25	43A	43A	42A
D26	43B	43B	42C
D27	44A	44A	42E
D28	45A	45A	42B
D29	45B	45B	42F
D30	46A	46A	43A
D31	46B	46B	43C

Table 66: Pin Assignment Data Bus for the phyCORE-LPC2292/94 / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
A0	8B	8B	30B
A1	9A	9A	30D
A2	10A	10A	30F
A3	10B	10B	31A
A4	11A	11A	31E
A5	11B	11B	31B
A6	12B	12B	31F
A7	13A	13A	32A
A8	13B	13B	32C
A9	14A	14A	32E
A10	15A	15A	32B
A11	15B	15B	32F
A12	16A	16A	33A
A13	16B	16B	33C
A14	17B	17B	33E
A15	18A	18A	33B
A16	23B	23B	35B
A17	24A	24A	35D
A18	25A	25A	35F
A19	25B	25B	36A
A20	26A	26A	36E
A21	26B	26B	36B
A22	27B	27B	36F
A23	28A	28A	37A

Table 67: Pin Assignment Address Bus for the phyCORE-LPC2292/94 / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/CS0	5A	5A	29E
/CS1	5B	5B	29B
/CS2	6A	6A	29D
/CS3	6B	6B	29F
FS0	35A	35A	39E
FS1	35B	35B	39B
FS2	11C	11C	4E
FS3	43D	43D	15A
FS4	44C	44C	15C
FS5	45C	45C	15E
FS9	47D	47D	16C
/BLS0	34A	34A	39A
/BLS2	36A	36A	39D
/BLS3	36B	36B	39F
/OE	7B	7B	30A
/WE	8A	8A	30E
/RESIN	10D	10D	3F
/RESET	10C	10C	3D
BOOT	9C	9C	3B
/PWROFF	20C	20C	7A
/INT_RTC	33D	33D	11B

Table 68: Pin Assignment Address/Control Bus and Analog Port for the phyCORE-LPC2292/94 / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
P00 (TxD0)	17D	17D	6C
P01 (RxD0)	16D	16D	6A
P02	47B	47B	43E
P03	48A	48A	43B
P04	48B	48B	43F
P05	49A	49A	44A
P06	50A	50A	44E
P07	50B	50B	44B
P08 (TxD1)	11D[1]	11D	4A
P09 (RxD1)	12D[2]	12D	4B
P010	13C	13C	4F
P011	13D	13D	5A
P012	14C	14C	5C
P013	15C	15C	5E
P014 (IRQ1)	3A	3A	28B
P015 (IRQ2)	3B	3B	28F
P016 (IRQ0)	2B	2B	28E
P017	15D	15D	5B
P018	16C	16C	5F
P019	19C	19C	6F
P020	4A	4A	29A
P021	24C	24C	8B
P022	25C	25C	8D
P027 (AIN0)	50C	50C	17A
P028 (AIN1)	49C	49C	16F
P029 (AIN2)	48D	48D	16B
P030 (AIN3)	48C	48C	16E

Table 69: Pin Assignment Port P0 for the phyCORE-LPC2292/94 / Development Board / Expansion Board

[1] : Check configuration of Jumper J200 on the phyCORE-LPC2292/94, *refer to section 3.1*.

[2] : Check configuration of Jumper J202 on the phyCORE-LPC2292/94, *refer to section 3.1*.

Signal	phyCORE Module	Expansion Bus	Patch Field
P1.16 (TRACEPKT0)	25D	25D	8F
P1.17 (TRACEPKT1)	26D	26D	9E
P1.18 (TRACEPKT2)	29C	29C	10C
P1.19 (TRACEPKT3)	30C	30C	10E
P1.20 (TRACESYNC)	30D	30D	10B
P1.21 (PIPESTAT0)	31D	31D	11A
P1.22 (PIPESTAT1)	41C	41C	14A
P1.23 (PIPESTAT2)	41D	41D	14E
P1.24 (TRACECLK)	42D	42D	14B
P1.25 (EXTIN0)	43C	43C	14F
P1.26 (RTCK)	37D	37D	12F
P1.27 (TDO)	38D	38D	12E
P1.28 (TDI)	38C	38C	13A
P1.29 (TCK)	40C	40C	13D
P1.30 (TMS)	40D	40D	13F
P1.31 (/TRST)	39C	39C	13B

Table 70: Pin Assignment Port P1 for the phyCORE-LPC2292/94 / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
CAN_H1	21D	21D	7D
CAN_L1	20D	20D	7E
CAN_H2	18C	18C	6E
CAN_L2	18D	18D	6B
TxD0 (P0.0)	17D	17D	6C
RxD0 (P0.1)	16D	16D	6A
TxD1 (P0.8)	23C[1]	23C[1]	8A
RxD1 (P0.9)	21C[2]	21C[1]	7B
RxD0_ext	22D	22D	7F
TxD0_ext	23D	23D	8E
RxD1_ext	21C	21C	7B
TxD1_ext	23C	23C	8A
SCL	31C	31C	10F
SDA	32D	32D	11C
SCLK0	28D	28D	10A
MISO0	27D	27D	9B
MOSI0	28C	28C	9F
/PCS0	26C	26C	9A
LAN_LED_A	33C	33C	11E
LAN_LED_B	34C	34C	11F
LAN_TPI-	35C	35C	12A
LAN_TPI+	35D	35D	12E
LAN_TPO-	36C	36C	12B
LAN_TPO+	36D	36D	12D
RTCK (P126)	37D	37D	12F
TDO (P127)	38D	38D	12E
TDI (P128)	38C	38C	13A
TCK (P129)	40C	40C	13D
TMS (P130)	40D	40D	13F
/TRST (P131)	39C	39C	13B
WDI	8D	8D	3A
TMS_PLD	46C	46C	15F
TDI_PLD	45D	45D	15B
TCK_PLD	46D	46D	16A
TDO_PLD	47D	47D	16C

Table 71: Pin Assignment Interface Signals for the phyCORE-LPC2292/94 / Development Board / Expansion Board

[1] : Check configuration of Jumper J200 on the phyCORE-LPC2292/94, *refer to section 3.1*.

[2] : Check configuration of Jumper J202 on the phyCORE-LPC2292/94, *refer to section 3.1*.

Signal	phyCORE Module	Expansion Bus	Patch Field
VCC	1C, 2C, 1D, 2D	1C, 2C, 1D, 2D	1A, 1C
VCC2	4C, 5C	4C, 5C	2A, 1B
CLKIN	1A	1A	28A
MCKO	1B	1B	28C
VPD	6D	6D	2D
VBAT	6C	6C	2B
ADVREF	50D	50D	17E
VAGND	42C, 47C, 44D, 49D	42C, 47C, 44D, 49D	connected to GND
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 42D, 47D, 52D, 57D, 62D, 67D, 72D, 77D	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C, 41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 9D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E, 1F

Table 72: Pin Assignment Power Supply for the phyCORE-LPC2292/94 / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
NC	8C, 4D, 5D, 7D	50A, 51A, 53A, 54A, 55A, 56A, 58A, 59A, 60A, 61A, 63A, 64A, 65A, 66A, 68A, 69A, 70A, 71A, 73A, 74A, 75A, 76A, 78A, 79A, 80A 51B, 53B, 54B, 55B, 56B, 58B, 59B, 60B, 61B, 63B, 64B, 65B, 66B, 68B, 69B, 70B, 71B, 73B, 74B, 75B, 76B, 78B, 79B, 80B 51C, 53C, 54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C, 73C, 74C, 75C, 76C, 78C, 79C, 80C 4D, 5D, 7D, 8D, 51D, 53D, 54D, 55D, 56D, 58D, 59D, 60D, 61D, 63D, 64D, 65D, 66D, 68D, 69D, 70D, 71D, 73D, 74D, 75D, 76D, 78D, 79D, 80D	18A, 19A, 20A, 21A, 22A, 23A 24A, 25A, 26A, 27A, 45A, 46A, 47A, 48A, 49A, 50A, 51A, 52A, 53A, 54A 17B, 18B, 19B, 20B, 21B, 22B, 23B, 24B, 25B, 26B, 27B, 45B, 46B, 47B, 48B, 49B, 50B, 51B, 52B, 53B, 54B 20C, 21C, 25C, 26C, 47C, 48C, 52C, 53C 17D, 18D, 22D, 23D, 27D, 44D 45D, 49D, 50D, 54D 18E, 19E, 20E, 21E, 22E, 23E, 24E, 25E, 26E, 27E, 45E, 46E, 47E, 48E, 49E, 50E, 51E, 52E, 53E, 54E 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F

Table 73: Unused Pins on the phyCORE-LPC2292/94 / Development Board / Expansion Board

15.3.10 Battery Connector BAT1

The mounting space BAT1 (*see PCB stencil*) is provided for connection of a battery that buffers the RTC on the phyCORE-LPC2292/94. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected battery. There is also the option of buffering the SRAMs with an external battery. This optional setting is configured with Jumper J25 (*see section 3.11*). In most cases an SRAM buffer is not recommended since the SRAM devices draw their operating current from VBAT during runtime of the module and therefore cause rapid battery discharge. It is the user's responsibility to ensure sufficient SRAM power supply during runtime. The optional battery required for the RTC buffering (*refer to section 10*) is available through PHYTEC (order code BL-011).

15.3.11 DS2401 Silicon Serial Number

Communication to a DS2401 Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS2401 can be soldered on space U10 or U9 on the Development Board, depending on the type of device packaging being used.

The Silicon Serial Number Chip mounted on the phyCORE Development Board HD200 can be connected to port pin P0.9 of the LPC2292/94 available at GPIO1 (JP19 = closed).

Jumper	Setting	Description
JP19	closed	Port pin P0.9 (GPIO1) of the LPC2292/94 is used to access the Silicon Serial Number

Table 74: JP19 Jumper Configuration for Silicon Serial Number Chip

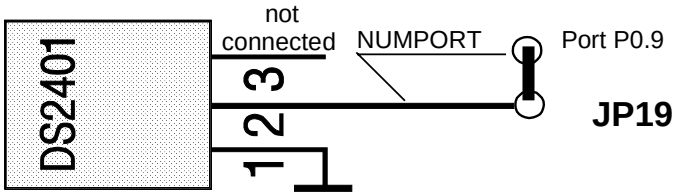


Figure 32: Connecting the DS2401 Silicon Serial Number

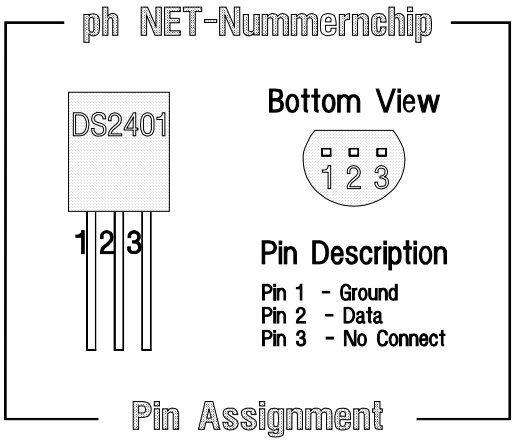


Figure 33: Pin Assignment of the DS2401 Silicon Serial Number

15.3.12 Pin Header Connector X4

The pin header X4 on the Development Board enables connection of an optional modem power supply. Connector X4 supplies 5 V = at pin 1 and provides the phyCORE Development Board HD200 GND potential at pin 2. The maximum current draw depends on the power adapter used. We recommend the use of modems with less than 250 mA current draw.

16 Ethernet Port

The phyCORE Development Board HD200 provides a 10-pin header connector at X7 for mounting the PHYTEC Ethernet transformer module. The optional add-on module is available through PHYTEC (order code EAD-003). This allows for direct connection of the phyCORE-LPC2292/94 with populated Ethernet controller mounted on a Development Board HD200 to a 10/100Base-T network.

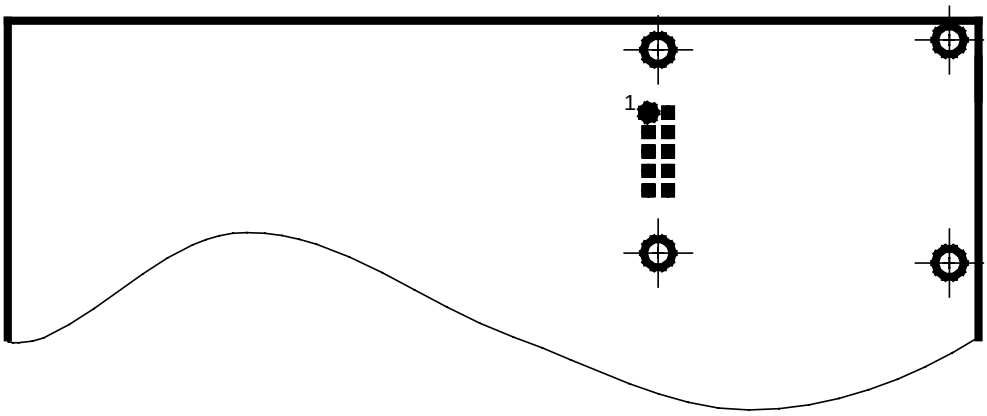


Figure 34: Ethernet Transformer Module Connector

The pinout for the Ethernet transformer connector is shown below:

Pin#	Function	Note
1	ETH_LanLED	Make sure JP37 on the Development Board is closed at position 1+2.
2	ETH_LinkLED	Make sure JP38 on the Development Board is closed at position 1+2.
3	VCC	
4	ETH_TxD+	
5	ETH_TxD-	
6	GND	
7	ETH_RxD+	
8	ETH_RxD-	
9	GND	
10	VCC	

Table 75: Ethernet Transformer Connector Pinout

17 Revision History

Date	Version numbers	Changes in this manual
24-Mar-2004	Manual L-658e_0 PCM/DCM-023 PCB# 1228.0 PCM-997-V2 PCB# 1179.5	First draft, Preliminary documentation. Describes the debugCORE-LPC2292/94 only
17-Jun-2004	Manual L-658e_1 PCM/DCM-023 PCB# 1231.0 PCB# 1228.0 PCM-997-V2 PCB# 1179.5	Description and module images changed to match the phyCORE-LPC2292/94. Pinout changes, PLD JTAG signals routed to Molex connector, *see section 2, Pin Description.* Jumpers J619, J620 and J621 added. J607 changed to 2-pad jumper. Paragraphs added to *section 5, Memory Models.*
13-Sep-2004	Manual L-658e_2 PCM/DCM-023 PCB# 1231.0 PCB# 1228.0 PCM-997-V2 PCB# 1179.5	Section 4.2, Starting the LPC2292/94 ISP Mode added. In section 12, debugCORE-LPC2292/94, Table 42, ETM/OCDS Connector at X800 and Table 43, LAN MII Connector at X500 pinout added. Section 15.3.2, Starting the ISP Command Handler added. Section 18, Component Placement Diagram added.

18 Component Placement Diagram

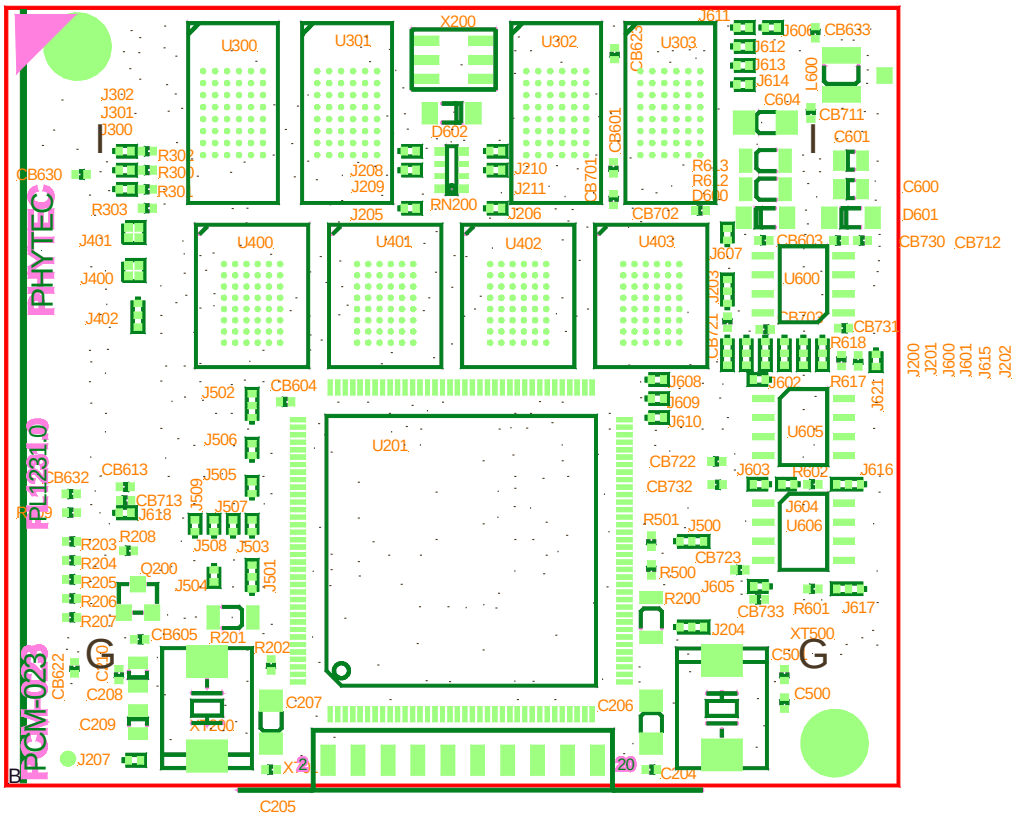


Figure 35: phyCORE-LPC2292/94 Component Placement, Top View

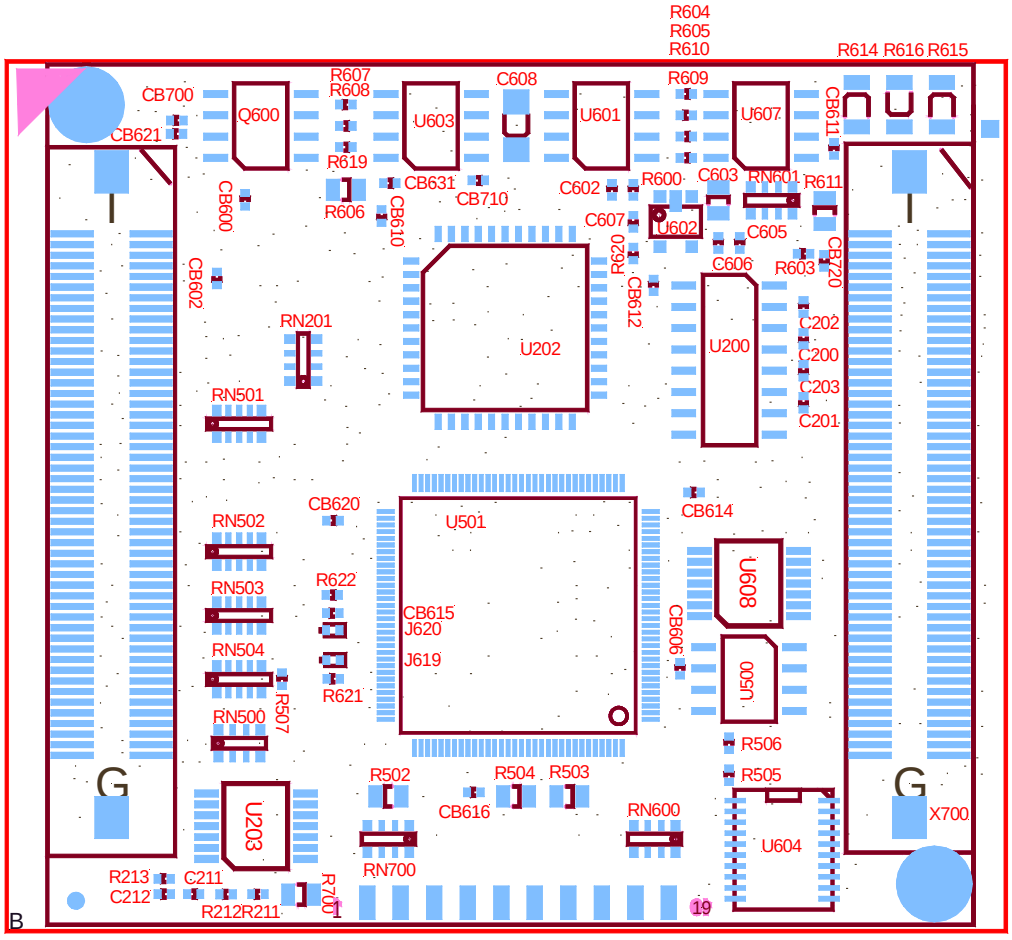


Figure 36: phyCORE-LPC2292/94 Component Placement, Bottom View

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Document number: **L-658e_2, September 2004**

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