

# Ripple: Asynchronous Programming for Spatial Dataflow Architectures

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Spatial dataflow architectures (SDAs) are a promising and versatile accelerator platform. They are software-programmable and achieve near-ASIC performance and energy efficiency, beating CPUs by orders of magnitude. Unfortunately, many SDAs struggle to efficiently implement irregular computations because they suffer from an *abstraction inversion*: they fail to capture coarse-grain dataflow semantics in the application — namely asynchronous communication, pipelining, and queueing — that are naturally supported by the dataflow execution model and existing SDA hardware.

*RIPPLE* is a language and architecture that corrects the abstraction inversion by preserving dataflow semantics down the stack. *RIPPLE* provides *asynchronous iterators*, shared-memory atomics, and a familiar task-parallel interface to concisely express the asynchronous pipeline parallelism enabled by an SDA. *RIPPLE* efficiently implements deadlock-free, asynchronous task communication by exposing hardware token queues in its ISA. Across nine important workloads, compared to a recent ordered-dataflow SDA, *RIPPLE* shrinks programs by 1.9×, improves performance by 3×, increases IPC by 58%, and reduces dynamic instructions by 44%.

CCS Concepts: • Software and its engineering → Data flow architectures; • Computer systems organization → Parallel architectures.

Additional Key Words and Phrases: spatial dataflow architectures, asynchronous programming

## ACM Reference Format:

Souradip Ghosh, Yufei Shi, Brandon Lucia, and Nathan Beckmann. 2025. Ripple: Asynchronous Programming for Spatial Dataflow Architectures. *Proc. ACM Program. Lang.* 9, PLDI, Article 157 (June 2025), 29 pages. <https://doi.org/10.1145/3729256>

## 1 Introduction

Over the last decade, computing has turned to specialized architectures to scale performance and efficiency, from low-power sensing [33] to datacenter-scale machine learning [40, 65]. Fixed-function accelerators are fast and efficient, but workload diversity and non-recurring engineering costs precludes using a custom ASIC for every application [44].

Spatial dataflow architectures (SDAs) are a flexible, efficient alternative to specialized hardware accelerators [5, 24, 33–36, 42, 54, 55, 58–60, 62, 66, 68, 70–72, 76, 81, 83–85, 87, 90]. An SDA and its compiler represents a program as a *dataflow graph* (DFG). The DFG’s nodes are instructions, and its directed edges explicitly encode communication between instructions. There is no global instruction order (i.e., program counter) in the dataflow execution model. Instead, the *dataflow firing rule* governs execution: an instruction fires whenever its inputs are ready [28]. Upon firing,

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ACM 2475-1421/2025/6-ART157

<https://doi.org/10.1145/3729256>

an instruction typically generates a data *token* for dependent instructions that is sent through a *token queue*. The compiler maps the DFG onto the SDA’s array of processing elements (PEs), or *fabric*, by placing instructions onto PEs and routing communication over a network on-chip (NoC). Token queues are routinely implemented in hardware as self-managing FIFOs, which buffer data tokens at PEs. Fig. 1 shows an SDA fabric and a small slice of the core SDA components: a single PE, the NoC, and hardware queues for input tokens.

Spatial distribution of compute and communication is key to an SDA’s performance and efficiency. Spatial distribution exposes ample instruction-level parallelism (ILP), while dramatically reducing the switching activity of an SDA’s PEs vs. a CPU [33, 76]. However, spatial distribution makes SDAs highly sensitive to *program size* because a DFG must fit onto an SDA to realize these advantages. A larger program requires more PEs and bigger NoC, which increases area and power. A larger program also often executes more instructions, wasting energy.

Moreover, depending on fabric size, placing and routing a large program can take hours [7, 34, 61].

Prior work has mainly focused on regular, affine loops, where dataflow compilers easily extract feed-forward DFGs from simple code regions (e.g., a dot product). These DFGs contain plentiful ILP and pipeline parallelism for SDAs to exploit [33, 42, 59, 66, 77, 84]; however, this approach neglects irregular code [24, 55, 68, 83]. Irregularity increases DFG size and reduces parallelism due to extra instructions for memory ordering and data-dependent control [34, 38, 63, 76].

**Why do SDAs struggle on irregular applications?** Many irregular programs feature regions of computation that execute and communicate data to other regions asynchronously. An SDA executes programs similarly: PEs fire asynchronously and hardware queues convey values from producers to consumers. These irregular algorithms and an SDA’s execution model both express *task-level* or *coarse-grain dataflow parallelism*. SDAs should be well-suited to accelerate these workloads.

Unfortunately, existing SDAs commonly extract DFGs from sequential [8, 14, 24, 34–36, 42, 54, 55, 59, 70, 76, 81, 82, 87] or data-parallel [45, 72, 77, 84, 85] code that lack explicit primitives for dataflow parallelism. Instead, the programmer must express coarse-grain communication explicitly in code. The resulting DFG implements asynchronous communication via several control and memory instructions. Whereas, if only dataflow behavior had survived compilation, communication could map directly onto hardware token queues. The mismatch between high-level dataflow semantics and the low-level compiled code is an **abstraction inversion** that (i) *increases program size* and (ii) *requires conservative serialization* of memory operations.

**Programming languages targeting SDAs should explicitly expose asynchrony and queueing, enabling the compiler to map dataflow operations directly to their corresponding hardware primitives.** We introduce **RIPPLE**, a language and spatial dataflow architecture, which combines an asynchronous dataflow programming model with simple ISA extensions to eliminate the abstraction inversion. *RIPPLE* programs are composed of asynchronously communicating tasks written using *asynchronous iterators* that define queueing and pipelining semantics for tasks and their inputs. *RIPPLE* allows arbitrary structure, from feed-forward pipelines to feedback loops of

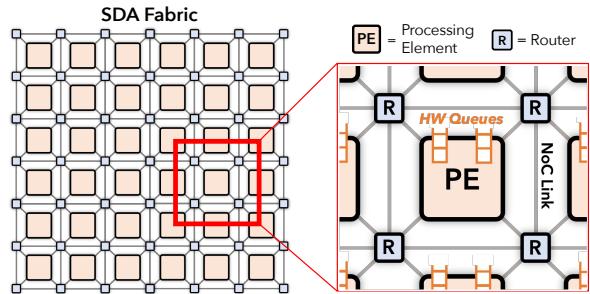


Fig. 1. Typical SDA fabric. Spatially distributed PEs execute instructions and communicate tokens over the NoC (via links and routers). Tokens are buffered at *hardware queues*.

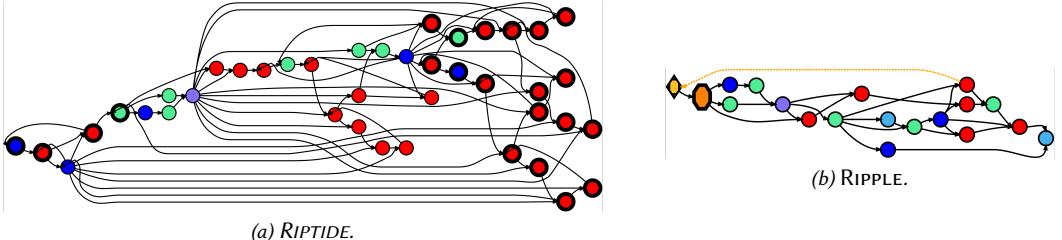


Fig. 2. DFGs of breadth-first search (bfs) for RIPTIDE and RIPPLE. (a) RIPTIDE compiles C, requiring heavy control flow (red) to implement dataflow semantics. The DFG serializes execution. (b) RIPPLE directly supports token queues (golden/orange) and atomics (light blue), shrinking the DFG while exposing parallelism.

tasks that generate dynamic amounts of work. RIPPLE’s ISA abstracts SDA token queues, allowing the compiler to map asynchronous task communication nearly one-to-one onto SDA hardware.

By exposing dataflow semantics, RIPPLE decreases program size, increases parallelism, and saves energy. Fig. 2 demonstrates RIPPLE’s benefits; it shows the DFGs of breadth-first search (bfs) compiled for RIPTIDE [34], a recent general-purpose dataflow architecture (left) and for RIPPLE (right). bfs traverses the graph using a FIFO queue, but its C implementation fails to express high-level queue semantics. Instead, the code implements a software queue using loads, stores, and data-dependent control flow. RIPTIDE’s compiler produces a large DFG that serializes execution to order the queue’s loads and stores. Fig. 2a has a sea of control flow (red nodes) with few memory (green) and arithmetic (blue) instructions. On a real-world input, 83% of all dynamic instructions were control flow.

The RIPPLE DFG (Fig. 2b) has fewer than half as many instructions. Traversal logic is implemented with an asynchronous code region, or `async`, that provides iterator semantics and a built-in work queue. bfs’s queue semantics lowers directly to a single `spill` instruction (orange node), eliminating almost all control flow in the DFG. `spill` implements vertex queueing – including concurrent enqueue and dequeue operations – using existing hardware token queues; it automatically spills tokens to memory if the hardware queue is full. Moreover, RIPPLE supports atomics to synchronize concurrent memory accesses in asynchronous tasks, allowing concurrent updates in bfs. RIPPLE efficiently implements atomics via its `acquire` and `release` instructions (light blue nodes). atomics eliminate memory orderings imposed by C, further shrinking programs while increasing parallelism.

**Contributions.** This paper solves an abstraction inversion problem that hinders SDAs:

- *Language.* RIPPLE implements the asynchronous dataflow programming model to efficiently program SDAs. RIPPLE’s few primitives for explicit asynchronous communication, queueing, and pipelining are designed to map nearly one-to-one to SDA hardware (e.g., token queues).
- *Spatial Dataflow ISA.* RIPPLE introduces queue and spill instructions that expose token queues for safe, efficient task communication, and RIPPLE provides acquire/release instructions for efficient and composable shared-memory synchronization on SDAs.
- *Evaluation.* We implement a full RIPPLE software stack and architectural simulator. Across nine important workloads, RIPPLE achieves a gmean 3× speedup, gmean 58% gain in IPC, and nearly 2× reduction in program size and dynamic instruction count vs. RIPTIDE, a recent SDA.

## 2 The Dataflow Execution Model

This section motivates RIPPLE’s contributions using a running example, bfs. Sec. 2.1 demonstrates how SDAs achieve high ILP through the dataflow execution model. Sec. 2.2 presents the abstraction inversion problem, which prevents SDAs and their compilers from extracting the ample dataflow parallelism present in many programs. RIPPLE solves the abstraction inversion problem by encoding dataflow semantics from the language down to the architecture (Sec. 3–Sec. 6).

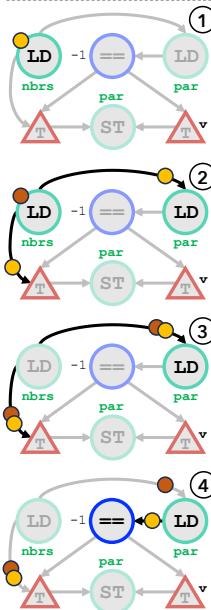
## 2.1 A Primer on Dataflow Execution

The dataflow model is the source of SDA performance. Dataflow execution achieves high ILP through three key properties: asynchronous instruction execution, fine-grained pipeline parallelism, and token queueing. We detail these properties by walking through a code section of bfs (Fig. 3). The program builds a search tree (parents) of a sparse graph using a software queue (`queue`).

**How does dataflow execution work?** Fig. 4 plots a DFG of L10-12, which performs neighbor updates in bfs. The DFG is implemented with the RIPTIDE ISA, a recent general-purpose SDA [34]. For concreteness, we focus on RIPTIDE’s ISA, but the lessons generalize to other SDAs. Fig. 4 uses common instructions like loads, stores, and comparators (`LD`, `ST`, `==`). The DFG uses steering control ( $\phi^{-1}$  [22, 28]), routing values from producers to consumers using steers ( $\triangle$ ) instead of branches.  $\triangle$  takes a data value and a conditional; if the conditional is true, it emits the data. Otherwise, it emits nothing. The top three nodes of the DFG perform the conditional in L10-11 to check for an unvisited neighbor: they load a neighbor,  $nb = nbrs[i]$ , then load  $parents[nb]$ , and compare it to  $-1$ . The bottom three nodes set  $parents[nb]$  to the current vertex,  $v$ . The DFG conditionally routes  $nb$  and  $v$  through  $\triangle$ s to the `ST`.

Fig. 5 shows an execution trace that highlights asynchronous instruction execution, pipeline parallelism, token queueing, and high ILP. This trace shows two iterations of the for loop (L9): the first (denoted by  $\bullet$  tokens) processes an unvisited neighbor, but the second ( $\circ$  tokens) does not. In this example, instructions fire and finish in one step, unless otherwise stated.

Tokens:  $\bullet$  Iter#1 |  $\circ$  Iter#2  
 $\bullet$  = Token queues on  $\textcircled{N}$   
 $\circ$  = Idle |  $\circ$  = Firing



```

1. void bfs (u32 *ofs, u32 *nbrs,
2. i32 *parents, u32 source):
3. u32 *queue, head = 0, tail = 0
4. void push(v): queue[tail++] = v
5. u32 pop(): return queue[head++]
6. bool empty(): return head == tail
7. while (!empty()):
8. u32 v = pop()
9. for (i = ofs[v]..ofs[v+1]):
10. u32 nb = nbrs[i]
11. if (parents[nb] == -1):
12. parents[nb] = v
13. push(nb)

```

Fig. 3. bfs in C-like code.

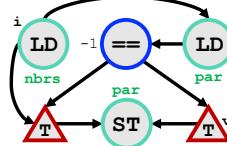


Fig. 4. DFG of L10-12 of Fig. 3. parents is abbreviated to par.

Step ①. A  $\bullet$  token that represents  $i$  is present and  $\text{LD}_{nbrs}$  fires because it has all of its inputs. The  $\text{LD}$  takes a single step to finish. It produces output tokens that arrive at consumers on the next step.

Step ②. Output  $\bullet$ s from ① (sent along the darkened arcs) arrive and *queue* at both of  $\text{LD}_{nbrs}$ ’s consumers. One consumer, a  $\triangle$ , does not yet have a complete set of tokens, so it does not fire. The other consumer,  $\text{LD}_{par}$ , has all of its inputs (i.e., just the result of  $\text{LD}_{nbrs}$ ) and fires. However, load latency can vary, and this  $\text{LD}$  arbitrarily takes longer; it will continue past step ② and finish in ③. Meanwhile, a  $\bullet$  from the second iteration arrives at the  $\text{LD}$  of  $nbrs$ , enabling it to fire again and *pipeline* work over consecutive loop iterations. The second iteration’s  $\text{LD}_{nbrs}$  finishes in a single step and sends output  $\bullet$ s for the next step.

Step ③. The  $\bullet$ s from ② arrive and queue at both consumers. A  $\bullet$  queues behind the  $\bullet$  at  $\text{LD}_{par}$  while the  $\text{LD}$  finishes up from step ②, and a  $\bullet$  also queues at the  $\triangle$  while it awaits its other input. Neither consumer fires using  $\bullet$ s in ③. Once  $\text{LD}_{par}$  completes, it outputs a  $\bullet$  that arrives in ④.

Step ④.  $\text{LD}_{par}$ ’s result arrives at  $\text{==}$ , allowing it to fire. Concurrently,  $\text{LD}_{par}$  fires again by dequeuing the  $\bullet$  and finishes in one step. Thus,  $\text{LD}_{par}$  also pipelines tokens from consecutive iterations, just like  $\text{LD}_{nbrs}$  in ①-②.

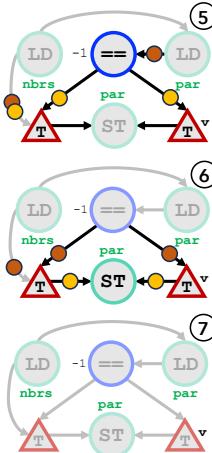


Fig. 5. Running Fig. 4 across two for loop iterations (L9, Fig. 3).

several times, even if its consumers are not ready (e.g.,  $\text{LD}_{\text{nbrs}}$  and its consumer  $\Delta$  in ①-③). This decoupling allows both loop iterations to pipeline through the DFG (e.g., in ④-⑦).

An SDA exploits this high ILP by spatially distributing a DFG on its fabric, allowing natural asynchronous instruction execution, pipelining, and queueing behavior inherent in the dataflow model. As shown in the example of an arbitrary SDA in Fig. 6, dataflow programs are commonly mapped onto an SDA fabric exactly as they appear as a DFG [34, 36, 54, 72]. All six instructions are distributed across PEs, and DFG edges are routed through the NoC. Token queues are implemented directly in hardware at each PE.

## 2.2 The Dataflow Abstraction Inversion Problem

Recent SDAs focus on extracting DFGs from sequential code [8, 14, 24, 34–36, 42, 54, 55, 59, 70, 76, 81, 82, 87] (often C), which lacks abstractions for asynchrony and queueing. Even when queueing is essential to the algorithm (as in bfs), programmers have no way to directly refer to queueing primitives that express asynchronous communication or token queues in hardware. Instead, the programmer writes a software queue with the same behavior as a hardware queue, but using many control-flow operations and memory accesses. *The queue abstraction is inverted*, leading to a serious performance problem. In contrast to Sec. 2.1, where the SDA achieves high ILP and IPC on a simple DFG of fine-grain data dependencies, *coarse-grained*, queue-based communication that spans the entire loop nest in bfs (Fig. 3) does not compile to a simple DFG. The extra instructions to support the software queue amounts to half of bfs’s DFG (bold-bordered nodes in Fig. 2a).

**Our observation: ignoring coarse-grain dataflow semantics leads to significant serialization.** A compiler sees the implementation of `queue` as many unstructured memory dependences, rather than a dataflow dependence. If multiple accesses potentially alias and race, an SDA compiler enforces *memory ordering*: accesses are conservatively serialized at compile-time to follow program order, at the expense of performance. In bfs, memory ordering serializes `push` and `pop` (L8, L13, Fig. 3). Fig. 7

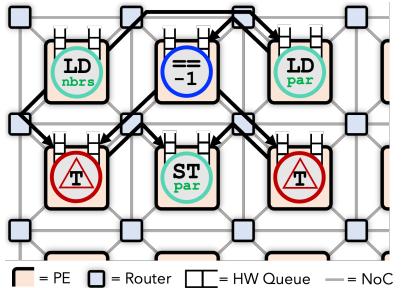


Fig. 6. An SDA implementing Fig. 5a. Instructions map to PEs and send tokens that buffer at hardware queues.

zooms into the (simplified) subgraph to show how **push** and **pop** are serialized. loads and stores take an optional ordering input (red arcs). The for node abstracts loop iteration: every iteration, it emits i and a control token, last. last is true on the last iteration and false otherwise.

From the left, **pop** (i.e., the **LD**) produces v, the current vertex, and triggers the inner for loop to emit i and a neighbor (nb, L8-10, Fig. 3). If nb is unvisited (L11), it will **push** back to **queue** (L13). A steer  $\Delta$  (top) routes nb to the store **ST** for **push**. Due to memory ordering, all **pushes** in the inner loop must complete before the next **pop** can execute. Every execution of the **ST** emits an ordering token (outgoing red edge) that the bottom steer  $\Delta$  gates. Only when last is true does the bottom  $\Delta$  allow the latest ordering token from **ST** to pass through to **LD**. In practice, several control-flow instructions implement each red edge and route tokens into and out of nested control structures. The effect compounds when multiple sets of aliasing reads and writes exist across the program.

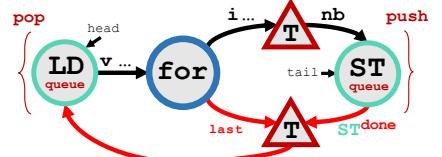


Fig. 7. Memory ordering of **pop** → **push** in Fig. 2a. Red edges indicate ordering.

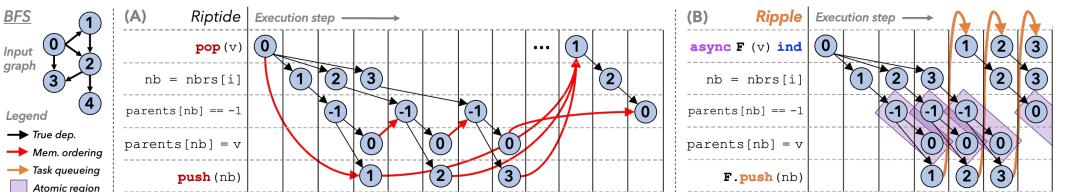


Fig. 8. A high-level pipeline diagram of bfs referencing C (Fig. 3) and *RIPPLE* code (Fig. 9). parents are initialized to  $\perp$ . (a) RIPTIDE is marred with serialization of the software queue. (b) *RIPPLE* eliminates ordering with pipelined tasks and atomics for better IPC and speedup.

**Memory ordering prevents asynchronous parallel execution.** Fig. 8a shows a significant loss of parallelism from ordering using a pipeline diagram of bfs running on RIPTIDE. The diagram illustrates the ordering (red edges) in Fig. 7: all unvisited vertices **push** before another is  **popped**. Read-modify-writes (RMWs) to parents (L12) are also ordered. The ordering prevents the idealized, pipelined loop iterations shown in Fig. 5 and results in serialization (third-fourth rows of Fig. 8a). *This loss in parallelism stems from the lack of language-level abstractions that match dataflow execution.*

Efficiently ensuring memory correctness is a long-standing problem for all SDAs. Prior architectures and systems impose ordering in a variety of ways, but the net result is the same: serialization and performance degradation. Strict ordering models [76] and RIPTIDE-style token-based ordering [15, 54] degrade parallelism, even when applied to code blocks to amortize costs [90]. Id's I- and M-structures [4, 9, 57] stand out as a mechanism to ensure memory correctness while retaining parallelism, but they require intrusive software changes. No existing solution ensures memory correctness without degrading performance due to serialization or making programming harder.

### 3 RIPPLE to the Rescue!

*RIPPLE* corrects the dataflow abstraction inversion by implementing the *asynchronous dataflow programming model*, in which programs are decomposed into asynchronous code regions that explicitly communicate data across regions. These abstractions enable the compiler to lower coarse-grain dataflow behavior to dataflow primitives implemented in SDA hardware. *RIPPLE* reduces DFG size and boosts parallelism by eliminating the inefficiency of software queues.

*RIPPLE*'s prototype language provides *asynchronous iterators* or *asyncs*, each of which represents a task-parallel region of code. An *async* can contain arbitrary code written in an imperative language.

asyncs execute asynchronously from one another. Communication between asyncs is explicit and happens via queues that match the dataflow execution model. With *just a few changes to the code* to encode asynchronous dataflow and queueing, the resulting implementation in *RIPPLE* eliminates the memory ordering dependences that degraded performance.

[Fig. 9](#) shows bfs implemented using *RIPPLE*. It has two asyncs, each of which has an implicit, dedicated task queue for its inputs. At runtime, `Init` (L2) kicks off the traversal with a *task*, or dynamic instance of an *async*, which pushes source to *async F*'s input queue. As *F* (L3-9) asynchronously receives inputs (e.g., *source*) to its task queue, it simultaneously dispatches tasks that run in *pipeline-parallel* fashion. We mark *F* with *ind*, expressing that its tasks are *independent*, with no memory ordering or data dependencies between any two tasks. As a result, *F*'s independent tasks use *atomics* to synchronize updates to parents (L6-9), avoiding memory ordering that would force a complete RMW to finish before another one starts. In *RIPPLE*, *atomics* pipeline, allowing many RMWs to launch before the first finishes. Finally, *RIPPLE* allows arbitrary, unrestricted task creation. Here, any task of *F* can push new inputs (i.e., unvisited vertices) back to create a future task of *F* (L11). *RIPPLE*'s execution enables high throughput processing over vertex neighbors.

```

1. def bfs (u32 *ofs, u32 *nbrs,
   i32 *parents, u32 source):
2.   async Init() : F.push(source)
3.   async F (u32 v) ind:
4.     for (i = ofs[v]...ofs[v+1]):
5.       u32 nb = nbrs[i]
6.       atomic <i32*>(&parents[nb]):
7.         if (parents[nb] == -1):
8.           F.push(nb)
9.           parents[nb] = v

```

Fig. 9. bfs in *RIPPLE*.

[Fig. 2b](#) shows that bfs gets much smaller, with a single backedge (orange) to a spill instruction using existing token queues. [Fig. 8b](#) shows how *RIPPLE* aggressively pipelines and concurrently processes vertices. Nodes ①-③ queue, dispatch, and pipeline using *async* (first row) and **push** (last row) while ④ finishes processing. Rows 3-4 of [Fig. 8b](#) show perfect pipelining because *atomics* execute in parallel. *RIPPLE achieves better performance with fewer resources*.

By embracing bfs's inherent dataflow behavior – i.e., queueing and asynchrony – *RIPPLE* removes bottlenecks that limit prior SDAs. First, *async* and **push** directly program token queues, obviating software queues. Second, explicit asynchrony removes serialization needed for sequential code. For bfs, *RIPPLE* need not sequentialize tasks, like the *while* loop in C demands. Vertices queue and drain safely and asynchronously. Third, *RIPPLE*'s architecture eliminates nearly all overheads for task queueing and dispatch. Queue and spill primitives are handled by hardware queues that efficiently self-manage a buffer of tokens and dynamically route tokens to and from memory when needed. Queueing and dispatch thus appear automatic in the language. *RIPPLE need no extra runtime support for asyncs and few changes to monolithic code to reap benefits.*<sup>1</sup>

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## 4 Programming with *RIPPLE*

The *RIPPLE* language implements the asynchronous dataflow programming model, which explicitly expresses dataflow semantics. *RIPPLE* provides a small set of language features designed around the dataflow execution model and existing SDA hardware. This section explores those features in the context of our *RIPPLE* prototype implementation. [Sec. 3](#) showed an example *RIPPLE* program.

### 4.1 Asynchronous Programming in *RIPPLE*

An asynchronous iterator or *async* defines a code region that accepts inputs through an implicit *queue*. *async* automatically iterates over inputs and dispatches work as a *task* (a dynamic instance of the *async*). [Fig. 10a](#) shows the syntax of an *async*. An *async* has a name, an arbitrary number of input arguments that forms a task input tuple (L1-2), and a body (scoped between L2 and L4) containing arbitrary code (C code in our prototype).

<sup>1</sup>See Appendix for more examples of C code vs. *RIPPLE* code.

A *RIPPLE* task executes with sequential semantics. Tasks of different `async`s run in parallel, and tasks of the same `async` pipeline in dataflow fashion. An `async` dispatches tasks following dataflow queueing semantics: they drain and launch in the FIFO order of the `async`'s input queue. Tasks do not need to finish in-order, e.g., if tasks take diverging control paths. An `async` with an empty input tuple (e.g., `Init` in Fig. 9) runs immediately.

```
1  async Name ([type _],      1  async P (u32 x) ind { 1  async Q (u32 y) ind {
2    ... ) [ind] {          2    atomic<u32*> (&A[x]) { 2    atomic<u32*> (&A[y]) {
3      // body           3      A[x]++;        3      A[y] = y - 1;
4    } } } } } } }
```

(a) *async* syntax.

(b) Shared-memory updates with atomics.

Fig. 10. atomics synchronize racing shared-memory updates.

**Independent work.** By default, *RIPPLE* orders any dependencies across tasks of the same `async` in dispatch order (e.g., serializing updates to the same `static` variable). A programmer can, instead, mark an `async` as *independent* or `ind`, indicating the absence of dependences between tasks of that `async`. The absence of dependences exposes more pipeline parallelism. `ind`, however, does not prevent data races between pipelined tasks of the same `async`. Instead, the programmer must synchronize accesses to shared memory using `atomics`, which Sec. 4.2 describes. Applying `ind` to an `async` essentially converts it from DOACROSS parallelism to pipelined DOALL parallelism [43]. Fig. 9 implements bfs with `ind` to aggressively pipeline unvisited neighbor updates.

`push` is *RIPPLE*'s only inter-task communication primitive. `push` creates and sends a tuple of task inputs to a named `async`, automatically queueing those inputs at that `async` (L2 and L8 of Fig. 9). *RIPPLE* allows feed-forward and cyclic communication among `async`s using `push`. *RIPPLE*'s architecture supports sending an unrestricted amount of data from one `async` to another, allowing the user to avoid thinking about communication bottlenecks or deadlocks related to queue capacity (Sec. 5).

`push` is also *RIPPLE*'s main task coordination primitive, with fence-like behavior that enforces dataflow ordering. A `push` does not execute until the completion of all reads, writes, and pushes that precede that `push` on its dynamic control-flow path from the entry point of the `async`.

## 4.2 Shared Memory Synchronization in *RIPPLE*

Tasks synchronize their accesses to shared memory using `atomics`, designed after atomic sections or blocks [17, 18, 32]. Fig. 10b shows the syntax of an `atomic`. `atomic` is parameterized, taking an arbitrary-sized, typed list of input memory addresses, which the user reads from or writes to in the `atomic`'s body. `atomics` have acquire-release semantics similar to two-phase locking [10, 31]. The body of an `atomic` executes only after acquiring exclusive access rights for all input addresses. The `atomic` releases its access rights when its body finishes executing. *RIPPLE* `atomics` allow multiple inputs that may alias, and instances of an `atomic` with disjoint sets of input addresses pipeline. *RIPPLE* implements these semantics in its ISA (Sec. 5), keeping the programming model simple.

**RIPPLE's memory model** is a data-race-free (DRF) memory consistency model [1], which gives undefined semantics to a program execution with a data race. `atomics` order concurrent accesses to the same memory location(s), eliminating data races. `atomics` have “all-or-nothing” atomicity semantics, and all accesses in an `atomic` appear to other `atomics` to happen simultaneously. A valid execution of a *RIPPLE* program corresponds to a partial order over memory operations. Operations in the partial order are unordered, except for (i) the serialization of operations with direct dataflow dependences (including explicit ordering dependences) and (ii) the serialization of memory operations in `atomics` that have overlapping input address sets.

### 4.3 Why is *RIPPLE* designed this way?

Each *RIPPLE* language primitive is designed to integrate with existing SDA hardware primitives without overly complicating the programming interface or the architecture. While *RIPPLE* is not the first to introduce asynchronous tasks (see Sec. 9), its implementation of the asynchronous dataflow programming model yields a concise language-to-hardware mapping.

**Explicit dataflow semantics.** Capturing dataflow behavior in code means expressing *asynchronous queue-based communication* and *coarse-grain pipeline parallelism* (Sec. 2). *RIPPLE*'s asynchronous iterators and communication primitives abstract exactly these properties: (i) `async` defines queueing semantics for task inputs and pipelining semantics for task execution; (ii) `push` enables arbitrary asynchronous task communication. Combined with its ISA, *RIPPLE* solves the abstraction inversion problem by preserving application-level dataflow semantics through compilation.

**async and push precisely capture an SDA hardware token queue's functionality.** In the dataflow model, a DFG edge represents an instruction dependence, and an SDA implements the dependence with a hardware token queue. A hardware queue is self-managing: it asynchronously receives input tokens and automatically drains whenever its associated PE is ready to fire another instruction (using the universal dataflow firing rule). `async` and `push` are designed to express dataflow dependencies just as an SDA does; they capture hardware queueing behavior in a number of ways. First, `push` defines an explicit dataflow dependence between `async`s in a program. Just as DFG dependencies are implemented by SDA token queues, a dependence defined by `push` is captured with `async`'s input queueing semantics. `async` defines an *implicit*, opaque work queue for its inputs that is only modified by `push`, rather than exposing queues to the user (e.g. via a special type). Limiting user control (e.g., by eliminating random access or preventing arbitrary queue instantiation [17, 29]) streamlines the API without losing the abstraction of token queues. Second, `async` defines iterator semantics to invoke automatic task dispatch rather offering user control over task launch. This design precisely expresses the automatic nature of draining a hardware queue. Any explicit “pop” or “receive” primitive that complements `push` would be a mismatch. Third, `push` is synchronization-free in software and automatically sends task inputs; it precludes the need for any runtime system. Instead, *RIPPLE* exposes hardware queues and arbitration in its ISA (Sec. 5), allowing the architecture to efficiently handle all task creation and routing.

**RIPPLE's atomic simplifies both the language and architecture.** `atomic` alone can express arbitrary shared-memory synchronization, eliminating the need for a library of common, low-level primitives (e.g., compare-and-swap or atomic-increment). This design also reduces the need for complex architectural support; *RIPPLE*'s ISA adds only two instructions to directly implement `atomic` (`acquire` and `release`, Sec. 5.4). Common low-level atomics are implemented by composing `acquire` and `release` rather than introducing a specialized instruction for each one.

**Eliminating ordering bottlenecks.** *RIPPLE* is designed to make it easy to expose coarse-grained pipeline parallelism. An *independent* (`ind`) `async` frees the compiler to optimize without adding memory ordering across tasks. Additionally, `atomics` synchronize shared-memory accesses with high performance; they pipeline and eliminate conservative memory ordering to reduce DFG size.

**Simplicity.** Motivated by the observations from Sec. 2.1–Sec. 2.2, *RIPPLE* extends a mainstream language, namely C in our implementation, rather than proposing an entirely new language. This strategy avoids a complete rewrite of programs, unlike other dataflow languages (Sec. 9). Rather, *RIPPLE* provides a small set of primitives that directly express the coarse-grained dataflow parallelism missed by mainstream SDA compilers. The *RIPPLE* version of `bfs` in Fig. 3 highlights the simplicity: an `async` and an `atomic` replaces the serialized `while` loop and the rest remains the same.

## 5 The *RIPPLE* Architecture

*RIPPLE* introduces simple dataflow ISA extensions that implements the queueing and synchronization primitives in *RIPPLE*'s asynchronous dataflow programming model.

### 5.1 Baseline Architecture

*RIPPLE* builds on the RIPTIDE ISA, which is a general-purpose ISA that supports full program execution in the *ordered dataflow* execution model. Sec. 2.1 demonstrated the ordered dataflow model, in which a PE fires its instruction after all of its inputs arrive via FIFO token queues (TQs). The ISA supports standard arithmetic and memory instructions and converts memory ordering into direct data dependencies. *RIPPLE* uses token steering to implement conditional control-flow (as shown in Sec. 2.1); the left side of Fig. 11 shows *RIPPLE*'s main control-flow instructions.

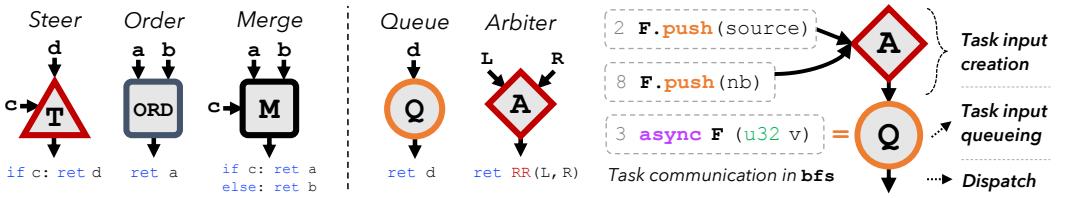


Fig. 11. Key instructions in *RIPPLE*. It borrows steer, order, and merge from [34] (left). It adds queue and arbiter (right).

Fig. 12. arb (A) and queue (Q) (shown for bfs) perform task creation, queueing, and dispatch.

### 5.2 *RIPPLE* Architecture Extensions

Two simple ISA primitives implement TQs and arbitration for multiple pushes to a TQ. The right side of Fig. 11 shows these extensions.

**queue** instructions expose hardware TQs to the compiler. queues have a single data input and output, passing its input token unmodified to its output. A queue can be marked to **spill**, which indicates the need to back the queue's input with memory (i.e., dynamic capacity). A spill is architecturally identical to a queue, but its unlimited capacity to buffer tokens prevents deadlocks stemming from overflow of a TQ in hardware (Sec. 5.3 describes this problem in more detail).

**arbiter** (arb) collects inputs pushed from different locations and fairly merges them into a TQ. arb takes two data inputs (L and R) and produces one output by selecting round-robin from inputs. If a single input is present, arb still fires, passing it as output.

**signal-arbiter** (sarb) is identical to arb but outputs the side chosen (not data): 0 for L, 1 for R.

**queue and arbiter directly implement language-level asynchronous communication.** An arb-queue pair is allocated for each async input. An arb selects tokens from pushes to an async, where each push is a separate arb input. We demonstrate using bfs (Fig. 9) and the DFG of async F's input queue in Fig. 12. The DFG shows a single arb-queue pair for F's input, v. In Fig. 12, there are two pushes to F, requiring a single arb. Note the simplicity in Fig. 12 over the same program compiled from C (Fig. 2a); only two *RIPPLE* instructions are needed to support the same dataflow queueing semantics that Fig. 2a implements with a sea of control flow (red, dark-bordered nodes). By abstracting token queues, *RIPPLE* language primitives can directly program existing SDA hardware.

**RIPPLE supports any number of async inputs and pushes by composing arbitration instructions.** Multi-input asyncs require more care than single-input ones (e.g., F in bfs). Fig. 13a shows multiple pushes to async F, which has two inputs. Fig. 13b shows the resulting arb-queue pairs for each input. The risk is that distributing input tuples without synchronization can erroneously

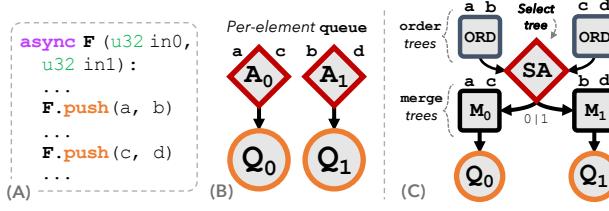


Fig. 13. General task input synchronization. (a) A multi-input `async`,  $F$ , and 2 pushes to it. (b) arb-queue pairs per element. (c) order-, select-, and merge-trees ensure tuples are ready, picks one, and emits per-element tokens to queue.

interleave tokens that arrive at different times. *RIPPLE* requires logic to choose only a complete input tuple. The logic has three parts: (i) tuple synchronization, (ii) tuple arbitration, and (iii) element-wise token selection. Fig. 13c illustrates an *order-tree*; it waits until an entire tuple is ready (e.g., both  $a$  and  $b$  in  $\langle a, b \rangle$ ). Once a tuple is ready for arbitration, its *order-tree* emits a token that feeds a *select-tree* of sarbs. The *select-tree* emits boolean signals that encode which tuple it picked. Fig. 13c shows a *select-tree*, comprising a single sarb since there are only two tuples ( $\langle a, b \rangle$  and  $\langle c, d \rangle$ ). Finally, the signals guide the chosen tuple, routing tuple-element-wise to their respective queues. *merge-trees* perform element-wise selection; each *merge* outputs a token based on a condition. In Fig. 13c, a *merge-tree* per tuple element takes the *select-tree* as its condition input (e.g.,  $SA \rightarrow M_0$ ). arbs in Fig. 13b lower to *merge-trees* in Fig. 13c to perform element-wise selection. *order-, select- and merge-trees* grow logarithmically with the number of pushes.

### 5.3 Preventing Deadlock in *RIPPLE* Tasks

While *RIPPLE*'s ISA abstracts hardware queues and implements arbitrary communication between `async`s, the resulting DFGs can produce *deadlock* when those queues do not have enough capacity. *RIPPLE* identifies deadlock in DFGs and avoids deadlock using the `spill` instruction.

**How might *RIPPLE* programs deadlock?** bfs (Fig. 9 and Fig. 14) illustrates the risk for deadlock. `async F` (L3-8) pipelines tasks without memory ordering between them. The *asynchrony* of both task creation and dispatch allows for rapid, unrestricted queueing of inputs.

The dynamic rate of task creation in `async F` is higher than the rate of dispatch because each task may push many neighbors while processing a single vertex. With a finite-size queue implementation,  $F$  exhausts its resources, blocking more inputs from being pushed. This blocking cascades through the DFG, eventually forming a cycle and deadlocking the program when nothing can fire.

*RIPPLE* captures this notion using a *task dependence graph* (TDG) [26, 79] that attaches relative rates of communication to dependent tasks. Fig. 14 shows the TDG for bfs lined up with code snippets. Nodes are `async`s ( $\textcircled{F}$ ) and ( $\textcircled{I}$ ) and arcs are task creation points (i.e., pushes). Importantly, when  $F$  dispatches, it pushes at most  $i$  inputs back to  $F$  (L8);  $i > 1$  if a vertex has many unvisited neighbors. The TDG encodes the cycle and the relative rate of task creation to dispatch on each arc.  $\textcircled{F} \xrightarrow{i}$  is then labeled with a variable rate:  $>1$ . *Variable rates along a cycle indicate a possible deadlock.*

**The key observation: task inputs must have space to queue to guarantee forward progress in *RIPPLE*.** Cyclic task communication is a property of a *RIPPLE* program. For instance, bfs *must* complete the `for` loop (lines 4-8 in Fig. 14) to finish one of  $F$ 's tasks, so it *must* have space to queue the new inputs for  $F$ . Common deadlock avoidance schemes fail to support cyclic, dynamic routes; they suggest eliminating cycles [26] or adding minimal, finite buffering [67] unsuitable for dynamic token queueing. Imposing extra control flow to throttle progress yields a DFG similar to one extracted from C, bloating it and eliminating any asynchrony or parallelism.

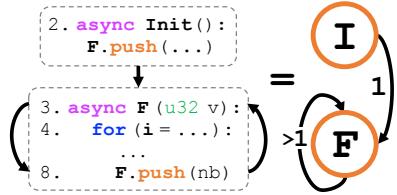


Fig. 14. Task dependence graph (TDG) of bfs.

**Only dynamically sized, on-demand buffering avoids deadlock in Ripple programs.** Once a queue runs out of buffering, Ripple automatically spills task inputs to a *backing queue* (BQ) in memory. Ripple accomplishes spilling with the specialized spill instruction. spill is functionally equivalent to queue, but it automatically reroutes tokens to the BQ whenever TQ storage runs out using an internal state machine (see Sec. 6.2 for its microarchitecture). A single instruction to manage both TQ and BQ (i) retains the asynchrony of task input creation and dispatch and (ii) avoids extensive resource consumption of distributing logic across many added instructions. Ripple prevents deadlock by analyzing the TDG and marking queues as spills in the compiler.

#### 5.4 Architecture for Ripple atomics

Ripple introduces acquire (acq) and release (rel) instructions to directly implement atomic's acquire-release semantics. acq and rel make requests (req) to the SDA memory system to acquire rights to an address and release it. acq and rel can compose to handle multi-input atomics and aliasing input addresses, while maintaining high performance.

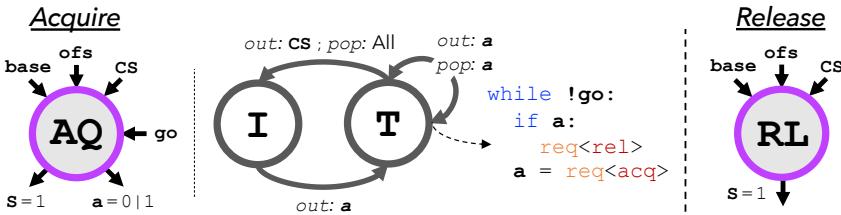


Fig. 15. acq/rel implement Ripple atomics and acquire/release addresses. acq has a state machine (middle).

#### Synchronizing memory accesses using acq and rel.

acq and rel are outlined in Fig. 15 and put in action in a read-modify-write atomic (Fig. 16). Each address requires an acq-rel pair that envelopes loads and stores in the DFG (i.e., two pairs in the example). To guarantee atomicity, all acqs must acquire before proceeding with dependencies. acqs acquire in parallel and synchronize with a reduction tree that controls if they proceed. Otherwise, all acqs must release, if necessary, and try again. The DFG shows a single-node tree ( $\textcircled{A}$ ) that reduces and routes to both acqs.

acq takes 4 inputs: a base and offset (ofs) to form an address, an optional control signal (CS) if ordered with other atomics, and a signal, “go”, that decides if it should retry. acq has two outputs: a, a status returned from an address acquire request ( $\text{req} < \text{acq} >$ ), and S, a final success status.

Each acq starts at state Init (I) once it receives  $\langle \text{base}, \text{offset}, [\text{CS}] \rangle$  and sends out  $\text{req} < \text{acq} >$ . It then switches to Try (T) and runs the loop in Fig. 15. Until go=1, the acq passes the return value from  $\text{req} < \text{acq} >$  as output a to the reduction tree and waits for a new go input. Importantly, an acq must release (i.e.,  $\text{req} < \text{rel} >$ ) an acquired address and retry if other acqs failed (i.e.,  $\langle a=1, go=0 \rangle$ ). Once go=0, acqs revert to I and send S, shown as solid DFG arcs from acqs to dependent memory instructions (e.g.,  $\text{AQ}_{\&A} \rightarrow \text{LD}_{\&A}$ ). They then consume inputs and wait for a new address.

rel takes base, ofs, and CS. It invokes a release request ( $\text{req} < \text{rel} >$ ) once it receives CS from completed memory operations upstream (e.g.,  $\text{ST}_{\&A} \rightarrow \text{RL}_{\&A}$ ). Like acq, rel emits S, an ordering token. rels do not need to synchronize. A concurrent atomic with the same input set cannot

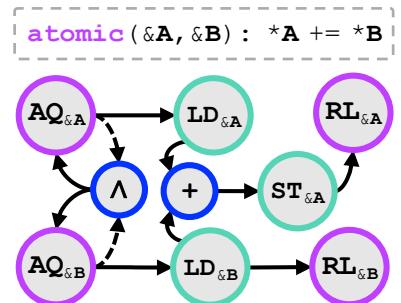


Fig. 16. DFG of an atomic. acq-rel pairs sandwich loads/stores for atomicity. acqs synchronize first (dashed arcs).

start unless *all* addresses are acquired, allowing even a single unreleased address to block another atomic. This feature maintains atomicity and enables `rels` to remain *disjoint* (as seen in Fig. 16).

### 5.5 Preventing Deadlock in *RIPPLE* atomics

atomics must have enough token buffering from `acqs` → `rels` in the DFG so acquired addresses are not held perpetually. atomics that produce a live-out (e.g., an atomic load) consumed by another atomic can cause deadlock if both share aliasing inputs. Consider a consumer atomic that waits on an address that a producer atomic has acquired but has not released. A “backpressure” or blocking cascade (similar to Sec. 5.3) can stall instructions in the producer, preventing it from executing its `rels`. The data dependence in the DFG that causes backpressure *and* the dynamic memory dependence between atomics creates an implicit deadlock-inducing cycle.

*RIPPLE* prevents deadlocks between atomics by reapplying spill. spills are inserted at any live-outs that yield data dependencies between atomics to provide abundant buffering. On-demand buffering enables forward progress so atomics can eventually release all acquired addresses.

## 6 *RIPPLE*’s Implementation

We implement a full *RIPPLE* system: a language prototype, compiler, and spatial dataflow architecture.

### 6.1 *RIPPLE*’s language prototype and compiler

We built the *RIPPLE* language prototype on top of C, using its types and scoping. *RIPPLE*’s async mimics C function signatures (e.g., Fig. 9), simplifying frontend compilation without adding new conventions. *RIPPLE* generates optimized DFGs, lowering *RIPPLE* code to LLVM-IR and expanding prior work [34] to insert control flow, enforce memory ordering, and prevent deadlock.

*RIPPLE*’s frontend generates a single, well-formed control flow graph (CFG) in LLVM-IR for each program (see Fig. 17 for an example). Frontend passes convert push, async iteration, and ind to intrinsic functions (see `%a = @A.iterator()` in block `A.body`). Each atomic is similarly translated; a pair of `_acq/_rel` intrinsics surrounds its scope. `async` and `atomics` are converted to basic blocks via clang (e.g. `async A` is `A.body`, `if`, and `else`). To convert several `asyncs` to one CFG, the frontend adds glue code (gray blocks) and transforms `async` subgraphs to loops. A well-formed CFG importantly avoids irreducibility [2] and maintains assumptions made by LLVM (e.g., in dominance analysis). Glue code is not lowered further; it only streamlines compiler analyses.

**Memory ordering for *RIPPLE*.** Before lowering to the DFG, *RIPPLE*’s compiler performs memory ordering analysis, similar to [34]. *RIPPLE* borrows RIPTIDE’s analysis framework, which (i) leverages alias analysis to build an ordering graph, (ii) optimizes it with a specialized transitive reduction, and (iii) inserts data dependencies to enforce happens-before arcs.

*RIPPLE*’s compiler builds on this by handling atomics. `_acq/_rel` pairs become nodes in the ordering graph. New happens-before arcs are added: (a) `_acq` → paired `_rel`, (b) `_acq` → loads/stores in its atomic, (c) loads/stores in an atomic → its `_rel`, (d) `_rel` → *all reachable and aliasing \_acq*. (a) and (b) enforce that an atomic must acquire its addresses first. (c) compels reads and

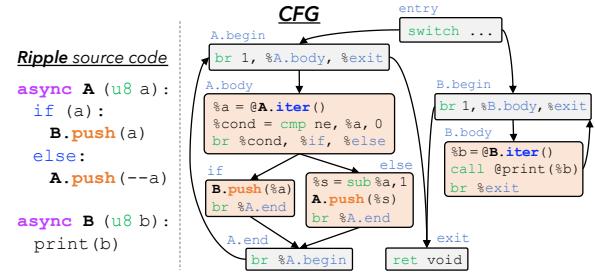


Fig. 17. *RIPPLE*’s frontend produces a well-formed control flow graph (CFG, as abridged LLVM-IR) with glue code (gray blocks) and async code (bright-colored blocks).

writes to finish before releasing. (d) orders atomics with other atomics that have aliasing input addresses (inferred via alias analysis) in the same async. The compiler transitively reduces the ordering graph to prune arcs and enforces remaining edges. Importantly, atomic reads/writes are only ordered with each other and their `_acq/_rel` pair. Different atomics then run concurrently.

**DFG generation.** *RIPPLE* creates a DFG from LLVM-IR. It leverages steer and stream insertion from RIPTIDE for control flow and optimized loop iterators. Next, every async parameter maps to an arb-queue pair in the DFG. push intrinsics are converted to input arcs for arbs and iterators (e.g., `.iter()`) to outgoing arcs from queues. When necessary, order-, select-, and merge-trees are added for multi-input asyncs or >2 pushes to an async. Finally, atomics are lowered by mapping each `_acq/_rel` intrinsic to acq-rel pairs in the DFG per address. A reduction tree of ands are inserted for multi-input atomics. Otherwise, the “go” input is configured to 1 for a single-acq atomic.

**Spill analysis.** The *RIPPLE* compiler prevents deadlock by marking or inserting spills. It first builds a task dependence graph (TDG, Sec. 5.2) from each push in the program. Nodes are asyncs and arcs are pushes. Arcs are conservatively labeled with a variable rate (>1) if the associated push resides in a loop; i.e., each task of the push’s parent async can create many tasks itself. Arcs are labeled with 1 otherwise. Variable-rate arcs along a TDG cycle indicate potential deadlock. *RIPPLE* then picks any queue in the DFG that corresponds to a node along a cycle and marks it as spill.

The compiler also prevents deadlocks for atomics (Sec. 5.5). It first checks for dependent atomics; i.e., if any live-out from an atomic in the DFG reaches another atomic. If dependent atomics access aliasing memory, a spill is inserted after each live-out that reaches the other atomic.

## 6.2 RIPPLE microarchitecture

We describe the microarchitecture of a PE for spill and a directory that manages acquire/release requests for atomics. Both require small hardware changes to integrate with a real SDA system.

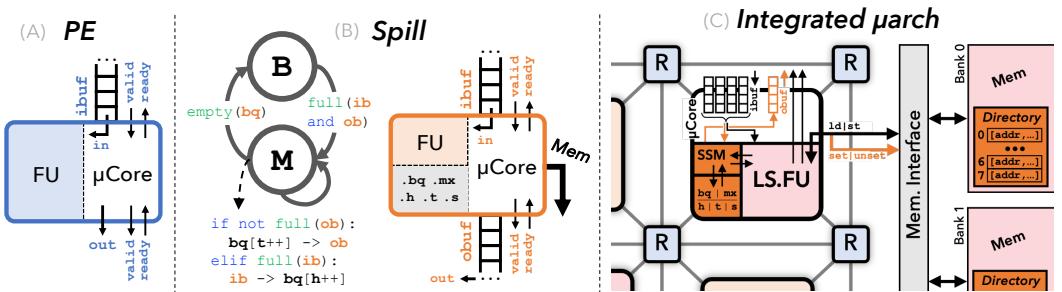


Fig. 18. (a) *RIPPLE* PE microarchitecture ( $\mu$ arch). (b) spill’s  $\mu$ arch has both ibuf and obuf (abv. ib, ob) and redirects or drains tokens with a FSM and internal state (gray portion). (c) *RIPPLE*’s  $\mu$ arch components (orange) added to RIPTIDE’s memory PE (left; e.g., the spill state machine or SSM) and memory subsystem (right).

**Microarchitecture for spilling.** spill prevents deadlock with on-demand buffering. We propose a PE for spill borrowing from RIPTIDE’s PE. A PE (Fig. 18a) has a functional unit (FU) and  $\mu$ core that communicate through the network-on-chip (NoC) using a ready/valid protocol. PEs use dedicated TQs at inputs (i.e., an input buffer or ibuf) for token storage.

The spill PE (Fig. 18b) has an ibuf and obuf (output buffer) to increase TQ space. Once TQs fill up, spill moves tokens to a backing queue (BQ) in memory, treated as a ring buffer. A state machine reroutes or drains tokens (from ibuf or BQ). The spill PE requires registers for a pointer to the BQ (bq), max capacity (mx), head/tail indices (h/t), and a bit, s, to track the state machine.

spill starts in the Buffer (B) state, where tokens transfer ibuf  $\rightarrow$  obuf. If both are full, spill transitions to Memory (M), where tokens route to the BQ and drain from ibuf  $\rightarrow$  BQ  $\rightarrow$  obuf. In

ℳ, the PE has two choices (see code in Fig. 18b). It (i) fills the obuf by loading from the BQ (i.e., prefetching [76]) or (ii) stores to the BQ if its ibuf is full. spill (i.e., blocks instructions upstream) if its ibuf saturates while rerouting tokens. Once the BQ is empty, spill moves back to ℳ.

**Microarchitecture for atomics.** *RIPPLE* uses a directory (dir), a hardware memory structure, to manage acquired addresses and talk with acq and rel using its API: set() and unset(). Fig. 19 shows pseudocode for each; set() implements req<acq> and unset() implements req<rel>. dir stores a tuple of metadata per address: <addr, atmid, ref, iid> to allow aliasing input sets and atomic instances to *pipeline*.

```

1 def set(addr, atmid, iid) -> bool:
2     if addr in dir: # There's an entry ...
3         if dir[addr].atmid != atmid: ret F # No match
4         elif dir[addr].iid != iid: ret F # No match
5         else: dir[addr].ref += 1 ; ret T # Match!
6         # @param addr isn't set, make a new entry
7         dir[addr] = (atmid, iid, ref=0) ; ret T
8
9 def unset(addr, atmid, iid) -> bool:
10    assert {addr, (atmid, iid, ref=Any)} in dir
11    dir[addr].ref -= 1 # Always decrement
12    if dir[addr].ref == 0: del dir[addr] # Released
13    ret T

```

Fig. 19. Pseudocode for the set() and unset() API. This API exposes the dir to acq and rel and also manages its metadata.

The *atomic ID* (atmid) is a static numbering of an atomic based on source code. It enables an atomic to safely acquire the *same* address multiple times if it appears in an input set. set checks for a matching atmid (L3) if a dir entry exists for addr, indicating an acq of the same static atomic reserved addr already. Similarly, dir records a *reference count* (ref) on acquisition (L5-7) so rel can safely release addr multiple times using unset. ref decrements for each unset() (L11), which removes the entry for addr when ref is 0 (L12). The language need not force atomics to use statically differentiable addresses because the directory manages it.

Finally, the directory records an *instance ID* (iid) per entry, that enumerates dynamic instances of an atomic. iid disambiguates instances of the same atomic (i.e., atmid) in case two concurrent instances have identical inputs. Atomicity is violated if multiple instances are allowed to run on shared inputs, so set blocks a new instance from progressing on an iid mismatch (L4). The iid enables the same atomic to safely *pipeline* concurrent instances with high throughput.

**Integrating *RIPPLE* into an existing SDA fabric.** *RIPPLE*'s microarchitectural extensions require few hardware changes. Fig. 18c shows the changes on RIPTIDE's SDA fabric in orange. RIPTIDE features several types of PEs, and *RIPPLE* leverages RIPTIDE's memory PE to implement spill, acq, and rel. The memory PE already supports most of the logic required: spill, acq, and rel reuse the same load-store FU (LS.FU in Fig. 18c) and datapath to access memory or make set/unset requests. With spill's state machine (SSM), registers, and obuf added, the memory PE has similar hardware complexity to other stateful SDA hardware implemented in prior work, including RIPTIDE's stream PE or Softbrain's memory stream engines [59]. Fig. 18c shows *RIPPLE*'s directory integrated into RIPTIDE's banked memory subsystem, where the memory interface directs set/unset requests. Each directory bank holds 8 entries; across RIPTIDE's 8 banks, the directory needs just 1KB total.

## 7 Methodology

**Systems.** We compare *RIPPLE* to RIPTIDE, building a full *RIPPLE* software stack and modeling both systems in a simulator. We also evaluate against a sequential von Neumann (vN) architecture (modeling 1 instruction per cycle or IPC) on performance and program size metrics. The vN system is modeled by directly executing LLVM-IR instructions. We count arithmetic, memory, and branching instructions but exclude all others (e.g.,  $\phi$ -nodes) for a fairer comparison to the SDAs.

**Compiler.** Compilers for all systems use LLVM 14 [49] and apply -Oz to reduce code size.

**Architectural simulator.** We evaluate *RIPPLE* and RIPTIDE using an in-house, event-driven dataflow simulator that directly executes DFGs.

*Modeling RIPTIDE:* The simulator accurately models RIPTIDE’s SDA fabric, including pipelined PE execution, bufferless NoC, and instruction timing. Each PE is assigned one instruction that it executes for the duration of the program; the SDA does not support dynamic time-multiplexing [62]. We assume DFGs successfully map as one unit and hence do not model fabric reconfiguration. In fairness to RIPTIDE, the simulator implements ibufs for instruction inputs at each PE (4 slots per ibuf) — follow-on work to RIPTIDE found that input buffers improved performance with small hardware overheads [72]. Any token transferring between buffers (e.g., from a spill’s obuf to its consumer’s ibuf) incurs a 1-cycle delay. Simulation of RIPTIDE in its original configuration (i.e., with obufs) was within 10% of its RTL execution cycles reported in [34] on two sample programs (bfs and dense matrix-vector multiplication).

*Modeling arithmetic and control-flow instructions:* Arithmetic instructions have 1-cycle latency. We simulate control flow for RIPTIDE with 0-cycle latency and no buffering. This models RIPTIDE’s combinational control-flow-in-NoC (CFIN) technique, wherein bufferless NoC routers perform control flow with no delay for better performance (e.g., over control flow on PEs). We empirically confirmed RIPTIDE’s findings that it performs better with CFIN.

*Modeling RIPPLE:* We run *RIPPLE* programs using the *RIPPLE* microarchitecture that extends the RIPTIDE fabric (Sec. 6.2). Simulation is identical to RIPTIDE apart from control flow. *RIPPLE* executes most control flow on a PE because it prefers buffering for better throughput and pipelining. *RIPPLE* only executes reduction trees (e.g., for atomics or accumulators) combinationally, where latency is more critical than throughput. arb and queue instructions have 1-cycle latency, and spill has 1-cycle latency when it only drains from its hardware queue (i.e., the Buffer state).

*Modeling memory:* loads, stores, and spills talk to a single-level, 8-way banked memory (e.g., like RIPTIDE’s hardware). Each bank queues memory requests and processes one per cycle with 1-cycle latency; bank conflicts can increase latency. *RIPPLE*’s dir is also 8-way banked, with 8 entries per bank (as in Sec. 6.2). dir has two request queues for set and unset. Each dir bank runs one set() and one unset() per cycle with 1-cycle latency each.

**Applications.** We evaluate *RIPPLE* on nine workloads in graph analytics and linear algebra, demonstrating that SDAs can efficiently support irregular code. By contrast, RIPTIDE was evaluated on workloads with simple dependencies (e.g., dense linear algebra). Our irregular workloads highlight the dataflow abstraction inversion problem solved by *RIPPLE*.

*Breadth-first search* (bfs) is Fig. 3 and Fig. 9. *Topological sort* (ts) partially orders nodes of a directed acyclic graph. *K-core decomposition* (kc) produces a maximal induced subgraph,  $S$ , s.t.  $\deg(v) \geq K, \forall v \in |V_S|$  ( $K = 128$ ). *Connected components* (cc) assigns components to vertices via label propagation. *Single-source shortest path* (sssp) finds the shortest path from a source to all vertices. *PageRank-Delta* (prd) [53] ranks vertices, only refining ranks that change  $> \delta$  in each step. *Matrix addition* (ma) performs a weighted sum of sparse matrices (dense output). *Stencil* (st) is a 2D, 5-point stencil using the Jacobi method ( $\text{iters} = 100$ ). Finally, we evaluate *Dense matrix-vector multiplication* (dmv) to cover workloads that SDAs like RIPTIDE already accelerate well.

*RIPPLE* and RIPTIDE (i.e., C) implement the same algorithm for each program. Graph workloads follow data-driven, iterative algorithms with high parallelism and fast convergence properties [27, 37, 47, 52, 88]. We use push-style updates [11]. ma and st are derived from Polybench [89].

**Inputs.** Workloads were evaluated on two synthetic or real-world inputs each (Table 1). Inputs range in size and cover different structures (e.g. uniform v. power-law graphs).

## 8 Evaluation

We evaluate *RIPPLE* and show that it improves performance, IPC, performance-per-area, and shrinks program size over RIPTIDE, a state-of-the-art, general-purpose ordered dataflow architecture.

Table 1. *Inputs*. Real inputs are fetched from SuiteSparse [46] (KR [6]; CA, WG, WS from [75]; DL is the SCC-DAG of [74]). DS is the SCC-DAG of a random Erdős-Rényi graph [20, 30]. S0, S1, D0, and D1 are random, uniform matrices. SM and LG are dense grids produced by Polybench. sssp adds random weights in [1, 128] to inputs.

App(s)	Graph	$ V $	$ E $	$d_{avg}$	$d_{max}$	App	Matrix ( $n \times n$ )	$n$	Structure	
[bfs, kc, cc, sssp]	KR CA	kron_g500-logn17 roadNet-CA	131K 2M	5.1M 2.8M	78 2.8	ma	S0 S1	Random-Sp-0 Random-Sp-1	$2^{14}$ $2^{14}$	Sparse ( $nnz_{avg}: 16$ ) Sparse ( $nnz_{avg}: 512$ )
	WG	web-Google	916K	5.1M	11.1		SM LG	Small-Grid Large-Grid	$2^8$ $2^9$	Dense Dense
	WS	web-Stanford	282K	2.3M	16.4		D0 D1	Random-D-0 Random-D-1	$2^{11}$ $2^{12}$	Dense Dense
prd	DL	DAG:Linux.call	320K	1.1M	7.2	dmv	DS	DAG:Synthetic	1M	80K
	DS	DAG:Synthetic								
ts										

## 8.1 Performance and Resource Utilization

**RIPPLE is fast.** Fig. 20 shows *RIPPLE*'s and RIPTIDE's speedups over the vN baseline. Both *RIPPLE* and RIPTIDE significantly outperform the sequential baseline by leveraging dataflow execution to extract high ILP (gmean 14.2 $\times$  and 4.7 $\times$ , respectively). Crucially, asynchronous tasks allow *RIPPLE* to unlock parallelism that RIPTIDE cannot exploit from C, amounting to gmean 3 $\times$  speedup over RIPTIDE. Queue operations are performance-critical in many irregular programs, and *RIPPLE*'s async iterators and atomics make these fast by eliminating software queues and memory ordering. They pipeline

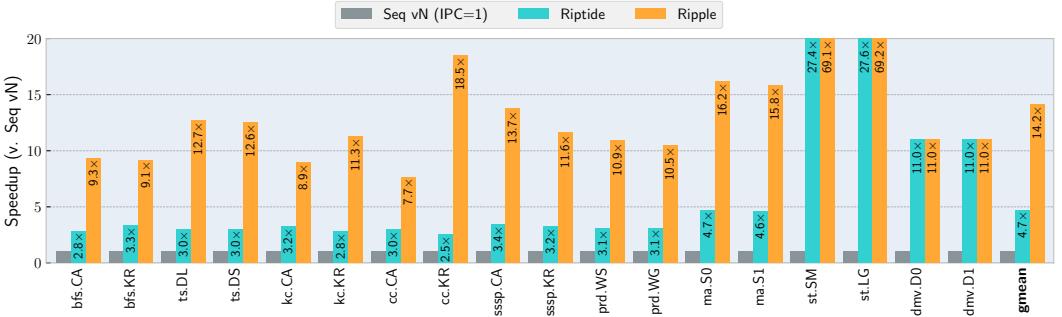


Fig. 20. Speedup of *RIPPLE* and RIPTIDE over a sequential von Neumann (vN) baseline (IPC=1) on all applications. *RIPPLE* is faster than RIPTIDE by gmean 3 $\times$  and the vN baseline by gmean 14.2 $\times$ .

better than RIPTIDE, accounting for most of the speedup. For example, *RIPPLE*'s cc sees a massive 7.3 $\times$  speedup over RIPTIDE on the power-law graph KR because queueing and atomic updates for label propagation are on the critical path. ma shows the benefit of *RIPPLE* avoiding serialization on independent, pipelineable asyncs, while RIPTIDE is forced to conservatively serialize ma's computation (which additionally disrupts pipelining), leading to *RIPPLE*'s 3.5 $\times$  advantage. *RIPPLE* is on-par with RIPTIDE's performance in its best domain: dense linear algebra. RIPTIDE's compiler extracts maximal pipeline parallelism from dmv's simple loop nest to produce a feed-forward DFG with no memory ordering, leading to a 11 $\times$  improvement over the vN baseline. *RIPPLE* performs just as well; however, expressing dmv's computation with asyncs offers little advantage because affine loops already express dmv's parallelism well.

**RIPPLE massively improves resource usage.** While *RIPPLE* programs enjoy fewer total (static) instructions, they execute substantially *more* IPC than RIPTIDE. Fig. 21 plots IPC (split by instruction type), measured as number of PE firings divided by execution time. *RIPPLE* improves IPC by gmean 58% and routinely achieves >10 IPC on *smaller* programs.

*RIPPLE* eliminates parallelism-killing artificial dependences to achieve high IPC. It executes more computational (arithmetic and memory) operations each cycle than the SDA baseline, which instead spends most of its time on control operations. Asynchronous tasks translate to better pipelining and high ILP. arb and spill often execute on every cycle, indicating high task throughput. st helps illustrate the effect of memory ordering instructions. Both RIPTIDE and *RIPPLE* have high IPC, but

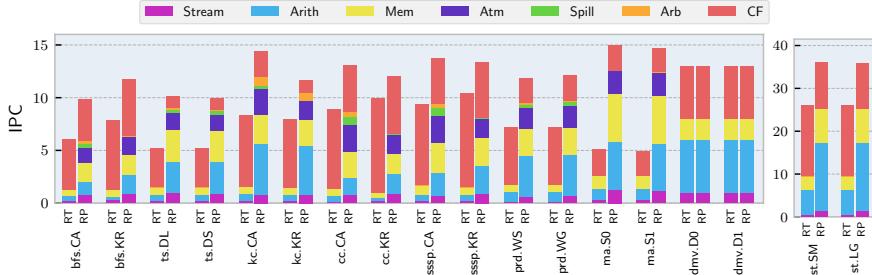


Fig. 21. IPC split by operator type. *RIPPLE* improves IPC on all applications (by gmean 58%) over RIPTIDE.

RIPTIDE wastes cycles on memory ordering. *RIPPLE* updates data rows in parallel (using red-black coloring), leading to its 2× memory IPC. *RIPPLE* implements a coarse-grain pipeline for dmv that compiles to the same DFG as from C, allowing *RIPPLE* and RIPTIDE to achieve the same IPC on dmv.

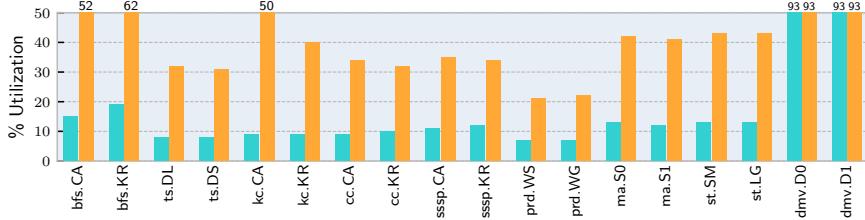


Fig. 22. Utilization of *RIPPLE* (orange) vs. RIPTIDE (teal). *RIPPLE* shows higher utilization by eliminating control-flow bottlenecks while improving concurrency via tasks.

Fig. 22 shows utilization, defined as the IPC divided by program size (i.e. number of DFG nodes). *RIPPLE*'s high utilization on irregular workloads (often 30-40%) showcases its unique ability to improve parallelism while requiring fewer static instructions. prd is an exception; much of its time is spent in a computationally intensive loop for each vertex that updates residuals. Nonetheless, *RIPPLE* almost triples its utilization against the baseline. Reducing control flow is key to utilization gains, as *RIPPLE* requires fewer resources to run a program while still performing with higher IPC. *RIPPLE* and RIPTIDE both perfectly pipeline dmv, allowing near 100% utilization.

**Improved resource usage coupled with small programs translates to high area-normalized performance for RIPPLE.** Fig. 23 shows gains in performance-per-area – execution time divided by program size – for *RIPPLE* over RIPTIDE. We use DFG size as a proxy for physical area consumption. *RIPPLE* improves by gmean 5.8× through reduced resource usage (smaller DFGs) and large speedups (more parallelism).

## 8.2 Characterizing *RIPPLE* Programs

***RIPPLE* produces small programs.** *RIPPLE* reduces program size by gmean 1.9× (and as much as 3×) over RIPTIDE's dataflow programs and by gmean 1.4× over the sequential von Neumann (vN) system, as Fig. 24 shows. RIPTIDE incurs high control flow overhead from excessive memory ordering and software queueing. vN programs need less control flow than RIPTIDE; branching requires fewer instructions than steering, and a program counter enforces all ordering by default. However, vN programs still need many instructions to implement software queueing. *RIPPLE* tackles both sources of static instruction overhead by significantly reducing memory ordering (e.g., with

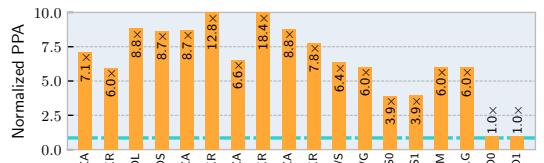


Fig. 23. Performance-per-area gains of *RIPPLE* over RIPTIDE, with a gmean 5.8× improvement.

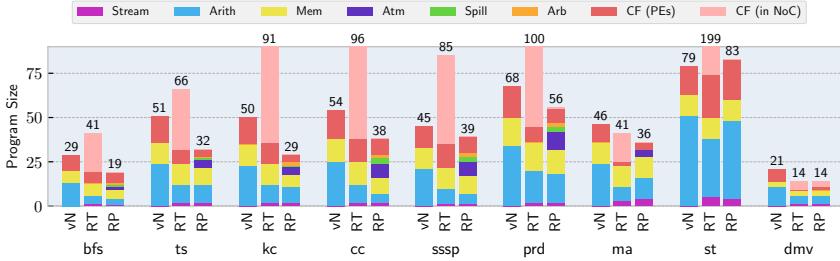


Fig. 24. Program size plotted as the number of DFG nodes or static instructions (split by operator type) for the vN system (vN), RIPTIDE (RT), and Ripple (RP). Control flow for RT and RP is split by PEs (dark red) and control-flow-in-NoC (light red). RP shrinks program size by gmean 1.9× over RT and gmean 1.4× over vN.

atomics) and eliminating software queues (with arb and spill). As a result, Ripple programs have far fewer control flow operations over RIPTIDE. ma shows other code size benefits of asynchronous programming. It does not use a software queue, but Ripple shrinks its DFG by splitting it into independent asyncs that pipeline with atomics. The resulting code has no ordering control flow across its loops, and no spilling, because its task graph is acyclic. Both Ripple and RIPTIDE produce small, nearly identical DFGs for dmv, as affine loops are easy to express and compile.

### 8.3 Estimating Ripple's Energy Costs

Ripple's benefits come without high energy overheads, and with a decrease in key sources of energy consumption. We focus on dynamic instruction count and memory usage as proxies for energy.

**Ripple executes fewer dynamic instructions.** Ripple reduces dynamic instructions by 44% on average (Fig. 25). Ripple eliminates the majority of instructions

that implement software queues, which are especially common in graph applications. Additionally, kc, cc, sssp, and prd implement asynchronous, iterative algorithms that process a vertex many times (e.g. path relaxation in sssp). These algorithms finish faster when they discover high-degree vertices more quickly, which can depend on vertex processing order and timing. Ripple very quickly discovers vertices in a traversal and aggressively pipelines their processing, leading to faster convergence and shorter runtimes. RIPTIDE instead serializes discovery and processing.

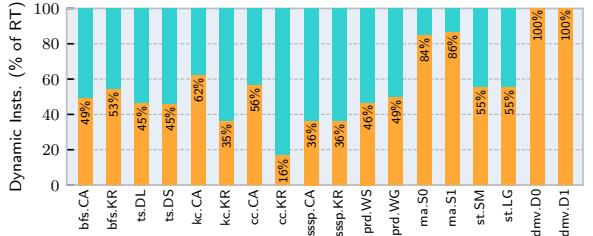


Fig. 25. Ripple (orange) reduces dynamic instructions, shown as a % of RIPTIDE's execution (teal), by 44% on avg.

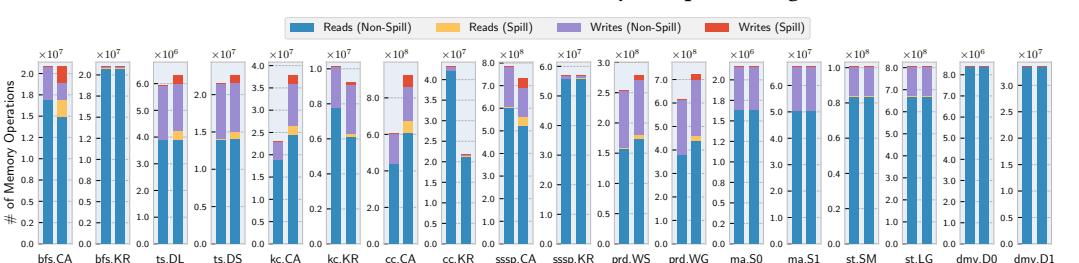


Fig. 26. Memory usage of Ripple vs. RIPTIDE, split into spilling and non-spilling reads and writes.

**Ripple incurs modest spilling overheads.** Fig. 26 shows total memory operations executed for each application, and Ripple's bars account for extra spill-induced reads and writes. Spilling to memory accounts for 7.6% of total memory operations on average in applications that need it. bfs.CA incurs the highest spill percentage at 18.8% of all memory operations. bfs and ts have

the highest per-application spill proportion at 9.9% and 9.7%, respectively. Generally, the graph applications spill more on uniform, high-diameter inputs (e.g. CA). Nevertheless, this tradeoff is a win for high throughput and performance across all applications.

**RIPPLE experiences reasonable but higher memory usage.** Fig. 26 also shows that *RIPPLE* can increase memory usage, often in iterative, work-inefficient programs. kc.CA and cc.CA execute 66% and 53% more memory instructions, respectively, with *RIPPLE*. Suboptimal vertex visiting order (i.e. work scheduling) coupled with aggressive pipelining degrade work efficiency since more vertices are revisited than needed compared to RIPTIDE. kc.KR and cc.KR reduce memory usage similar to their reductions in dynamic instructions with *RIPPLE*: they discover high-degree vertices and propagate updates quickly. *RIPPLE* requires fewer memory instructions for sssp on both inputs, likely because its traversals differ from kc and cc. These results point to a need for better work scheduling, either based on priority, rank, or dynamic information [23].

Other factors contribute to higher memory usage. In ts, spilling and slight implementation differences in bookkeeping of in-degrees come to increase overall memory usage by 6.2%. *RIPPLE* executes 14% more memory operations on prd because it aggressively pipelines tasks, causing it to update residuals of some neighbors that have already converged. prd also reloads data from the graph on occasion to fetch neighbors; it reduces pipeline bubbles but increases memory usage.

When work efficiency is not in play, *RIPPLE* has identical memory usage as RIPTIDE. *RIPPLE*'s bfs has no memory overheads with spilling since the traversal queues each vertex only once. ma, st, and dmv also have no change in memory usage since they compute a fixed number of updates. As with spilling, *RIPPLE* prefers to trade off reasonable memory overheads for much higher performance.

#### 8.4 Common Patterns in *RIPPLE* Code

We identified common patterns and pitfalls from our experience writing applications in *RIPPLE*.

**Expressing different forms of task parallelism.** We found that *RIPPLE* is excellent at expressing worklist parallelism [64]. async's queues naturally track outstanding work. Take prd: only outgoing neighbors of unconverged nodes ( $\text{rank} > \delta$ ) need to be refined and pushed back to the work queue. Users need not iterate through all vertices in each round and poll for convergence.

*RIPPLE* also expresses DAG parallelism well. End-to-end asynchrony and atomics allow the user to discover task dependencies (often a DAG) and process them simultaneously. *RIPPLE*'s ts shows this pattern; it begins sorting as soon as any zero in-degree node is found, improving concurrency over the common strategy of computing a task graph and processing it in separate, disjoint stages [39].

Finally, *RIPPLE* encodes coarse-grain pipelines efficiently. We find that using push as coordination primitive to split computation leads to a natural pipeline structure. st exhibits this well; we use push to stagger and trigger updates at row-level granularity in a red-black colored grid.<sup>2</sup>

**Decoupling reads and writes across asyncs.** Many RMWs or atomics in a single async can hamper performance because of memory ordering. We find that decomposing one async into multiple often naturally decouples and batches reads and writes with no memory ordering imposed across asyncs. Instead, we use push as a fence for correctness. The 5-point stencil update in st is an example; queries are decoupled from updates to the grid.

**Correctly using atomic with ind.** Correct synchronization is difficult in parallel code, and the use of atomic is no different. asyncs marked ind add extra complexity because their tasks aggressively pipeline. Using atomic in the presence of ind is crucial to eliminate races from potentially many in-flight tasks from the same async. The atomic in bfs (Fig. 9) shows this in practice.

---

<sup>2</sup>See Appendix for C and *RIPPLE* source code for ts and st.

## 9 Related Work

*RIPPLE* builds on prior work in asynchronous dataflow, dataflow languages, and dataflow ISAs.

### 9.1 Programming for SDAs

Sec. 2 outlined the pitfalls of SDA compilers that extract DFGs from mainstream, sequential code. Few prior general-purpose languages target SDAs. Prior languages that do require a complete implementation overhaul, often including both software and hardware changes. We divvy these languages and SDAs by their parallel programming paradigm.

**Implicit asynchronous parallelism.** The functional dataflow language Id [3] assumes *all* code is implicitly parallel by default. However, functional languages like Id make common computation idioms difficult to express because they do not support mutable state. Id requires separate hardware support, called I- and M-structures [4, 9], to enable this common feature. Id also requires several instructions to launch parallel work on its target dataflow architecture [21].

*RIPPLE* takes an incremental approach: A few `asyncs` are enough to inform the compiler about high-level dataflow semantics in the program. Fine-grain parallelism can be successfully expressed and extracted by the compiler within an `async`. Moreover, by starting from common SDA hardware with shared memory, *RIPPLE*'s architecture remains simple and efficient.

**Data parallelism.** Recent SDAs like Plasticine [66] and SGMF [84] exploit massive fine-grained data parallelism replicated across onto large fabrics. They are programmed with data-parallel code: SGMF uses CUDA while Plasticine implements parallel patterns from the Spatial language [45]. While highly performant on regular code, users must morph iterative, irregular applications into map-reduce blocks that can underutilize the SDA's feed-forward pipeline stages [66]. Consequently, subsequent work continually adds language features and hardware to support workloads from other application domains [68, 69, 83, 85] (e.g., dMT-CGRA's message passing in CUDA threads).

*RIPPLE*, instead, starts from a point of generality and adds asynchronous communication to the language because it best models dataflow execution and SDA hardware; only few hardware changes are needed to achieve high performance *and* small programs.

**Structured pipeline parallelism.** Many SDA-adjacent systems target code decomposed into coarse-grain pipeline stages; StreamIt [79] and Raw [86] are archetypes of this model. StreamIt efficiently implements streaming programs as coarse-grained pipelines with FIFO communication. Raw supports StreamIt programs on a distributed architecture of many scalar cores. StreamIt and Raw do not support fine-grained dataflow execution like *RIPPLE* and other SDAs (they support message passing between cores). However, they analyze and optimize pipelines using the synchronous dataflow model [50], which restricts the structure of StreamIt pipelines. All pipeline stages, feedback loops, and asynchronous messaging channels [80] must exhibit statically analyzable bounds.

Ultimately, structured pipelines are unable to express arbitrary, asynchronous communication that governs dataflow firing and application-level dataflow behavior seen in irregular code like bfs. *RIPPLE*, instead supports arbitrary, unrestricted communication between `asyncs`, and can easily encode general pipelines *and* feedback loops without deadlock.

### 9.2 Conventional Asynchronous and Task-Parallel Languages

Message passing [19, 73], actor [25, 51], coordination [13], and task-parallel [12, 16, 18, 29, 48, 78] languages provide primitives that share core features of asynchronous dataflow programming and *RIPPLE*. For instance, MPI implements explicit asynchronous communication while Cilk supports asynchronous thread launch. Galois supports iterative execution, go offers first-class FIFO channels, and Habanero-Java (HJ) provides its own `async` and data-driven tasks.

**So, what sets Ripple apart?** A parallel language should enable programmers to express the kind of parallelism efficiently supported by the target architecture. For instance, CUDA forces programmers to write data-parallel programs, which yields high parallelism on GPUs. Likewise, Ripple’s asynchronous iterators express exactly the parallel semantics supported by SDAs. As a result, Ripple programs map efficiently to dataflow hardware by construction. This is the key to Ripple’s benefits: high pipeline parallelism and small programs, and no software runtime. Other languages do not map efficiently because they target conventional multicore or distributed systems, and they consequently express parallelism that does not map one-to-one to SDA hardware.

go and Cilk are languages that may impose too little or too much structure in task communication, respectively. In particular, go lacks structure in channel manipulation to effectively represent SDA queues; channels can be created and destroyed arbitrarily, drained imperatively, and passed by reference. SDA queues always accept and dispatch tokens automatically, which requires only a simple primitive to push data to a queue; the rest of its functionality is automatic in Ripple. On the other hand, Cilk imposes too much structure in task communication, requiring parent-child task joining. In Ripple, tasks can communicate arbitrarily, which maximizes asynchrony.

In addition, Galois and HJ support parallel execution models unfit for SDAs. Galois iterators support speculative, transactional worklist parallelism, where worklist data structures can be programmatically defined. HJ supports data-driven tasks, but at the wrong granularity; the programmer must stitch together all dataflow behavior explicitly with futures and `async-await` statements for each computational step. By contrast, Ripple features pipeline-parallel, asynchronous iterators amenable to dataflow execution on SDAs. Ripple programmers only need to specify coarse-grained asynchronous communication, and Ripple relies on the compiler to extract fine-grained dataflow parallelism, obviating the need for a future for each value.

Finally, due to the mismatch between language and architecture, these languages require complex software runtime systems to effectively extract parallelism. Ripple does not need one because it directly maps asynchronous dataflow parallelism to SDA hardware exposed by Ripple’s ISA.

### 9.3 SDAs for Irregular Workloads

Few SDAs directly optimize for irregular code through hardware changes. UE-CGRA [81] identified underutilization with irregular code on spatial hardware. However, they apply VLSI techniques to accelerate only inner loops. Several SDAs optimize sparse tensor code via specialized tensor iteration [24, 68, 72] or efficient near-data spatial computation [41]. However, these SDAs need extra hardware and data-parallel expression of sparse computation (e.g., `par for`); this diverges from Ripple’s approach and goals (as discussed with data-parallel SDAs in Sec. 9.1). Fifer [55] is a high-performance SDA that targets decoupled irregular code [56] to hide long-latency memory operations through aggressive pipelining. However, Fifer does not support arbitrary cyclic dependencies. Ripple and Fifer also differ in their approaches and goals: Fifer adds massive task queues between pipeline stages that ensures ample work to hide memory latency. By contrast, Ripple solves the abstraction inversion problem to make better use of existing hardware queues, without modification.

## 10 Conclusion

This paper presents Ripple, a language and spatial dataflow architecture that implements the asynchronous dataflow programming model. Ripple explicitly encodes and maps high-level asynchrony, pipelining, and queueing semantics in irregular computation to an efficient dataflow representation. Ripple eliminates control-flow and memory ordering bottlenecks that plague DFGs extracted from sequential code by preserving dataflow semantics down the hardware-software stack. On important irregular workloads, and over a state-of-the-art SDA, Ripple improves performance by gmean 3 $\times$ , reduces DFG size by nearly half, improves IPC, and slashes dynamic instructions.

## A Appendix

**Fig. A1** lists reference C and *RIPPLE* code for two workloads we evaluate, *Topological sort* (ts) and *Stencil* (st), that demonstrate how *RIPPLE* expresses different kinds of parallelism. *RIPPLE*'s implementation of ts exploits dynamic task parallelism, where the DAG task graph is discovered and processed simultaneously (in Init and Sort, respectively). *RIPPLE*'s st implementation constructs a coarse-grained pipeline that exploits red-black coloring of the stencil grid. Rows of red points and black points are computed concurrently, but staggered for correctness using push.

```

1. void topsort(u32 N, u32 *sorted,
   u32 *inOfs, u32 *inNbrs, // incoming
   u32 *outOfs, u32 *outNbrs, // outgoing
   u32 *inDegrees, u32 *queue):
2.   u32 head = 0, tail = 0, sI = 0
3.   void push(v): queue[tail++] = v
4.   u32 pop(): return queue[head++]
5.   bool empty(): return head == tail
6.   for (v = 0..N): // find 0-inDeg nodes
7.     u32 inDeg = inOfs[v+1] - inOfs[v]
8.     if (!inDeg): push(v)
9.     else: inDegrees[v] = inDeg
10.  while (!empty()): // sort
11.    u32 v = pop(), sorted[sI++] = v
12.    for (i = outOfs[v]..outOfs[v+1]):
13.      u32 out = outNbrs[i]
14.      if (!--inDegrees[out]):
15.        push(nb)

1. def topsort(u32 N, u32 *sorted,
   u32 *inOfs, u32 *inNbrs, // incoming
   u32 *outOfs, u32 *outNbrs, // outgoing
   i32 *inDegrees):
2.   async Init(): // find 0-inDeg nodes
3.     for (v = 0..N):
4.       u32 inDeg = inOfs[v+1] - inOfs[v]
5.       // Atomic add to inDegrees allows
6.       // Init to discover work *and* Sort
7.       // to process tasks concurrently.
8.       atomic<i32*>(&inDegrees[v]):
9.         inDegrees[v] += inDeg;
10.        if (!--inDegrees[v]):
11.          Sort.push(v)
12.   async Sort(u32 v) ind:
13.     Record.push(v)
14.     for (i = outOfs[v]..outOfs[v+1]):
15.       u32 out = outNbrs[i]
16.       atomic<i32*>(&inDegrees[out]):
17.         if (!--inDegrees[out]):
18.           Sort.push(out)
19.   async Record(u32 v):
20.     static u32 sI = 0
21.     sorted[sI++] = v

1. void stencil(u32 n, u32 steps
   f32 A[n][n], f32 B[n][n], f32 α):
2.   for (0..steps):
3.     // Memory ordering on A and B
4.     // spans the entire loop nest.
5.     for (i = 1..n-1):
6.       for (j = 1..n-1): // compute B from A
7.         B[i][j] = α * (A[i][j] + A[i-1][j] +
8.                         A[i+1][j] + A[i][j-1] + A[i][i+1])
9.     for (i = 1..n-1):
10.      for (j = 1..n-1): // compute A from B
11.        A[i][j] = α * (B[i][j] + B[i-1][j] +
12.                         B[i+1][j] + B[i][j-1] + B[i][i+1])

1. const DEPTH = 3 // 5-point pattern spans 3 rows
2. def stencil(u32 n, u32 steps, f32 A[n][n], f32 α):
3.   async GenRedRows():
4.     for (0..steps * 2):
5.       for (redRow = 1..n-1):
6.         ProcessRed.push(redRow)
7.   async ProcessRed(u32 i):
8.     // Compute red cells of row i
9.     for (j = ((i % 2)+1)..n-1; j += 2):
10.      f32 sum = α * (A[i][j] + A[i-1][j] +
11.                      A[i+1][j] + A[i][j-1] + A[i][j+1])
12.      WriteRed.push(i, j, sum)
13.   async WriteRed(u32 i, u32 j, f32 sum):
14.     // Writes and reads are decoupled to remove
15.     // unnecessary memory ordering. Instead of
16.     // atomics, push coordinates the pipeline.
17.     A[i][j] = sum;
18.     GenBlackRow.push(i, j)
19.   async GenBlackRow(u32 redRow, u32 col):
20.     // At the start of a red row (col <= 2),
21.     // a black row DEPTH=3 rows behind is ready.
22.     if (col <= 2):
23.       u32 blackRow = (redRow - DEPTH + n) % n
24.       ProcessBlack.push(blackRow)
25.   async ProcessBlack(u32 i):
26.     // Compute black cells of row i
27.     for (j = (! (i % 2)+1)..n-1; j += 2):
28.       f32 sum = α * (A[i][j] + A[i-1][j] +
29.                       A[i+1][j] + A[i][j-1] + A[i][j+1])
30.       WriteBlack.push(i, j, sum)
31.   async WriteBlack(u32 i, u32 j, f32 sum):
32.     A[i][j] = sum;

```

Fig. A1. Abridged reference C and *RIPPLE* code for *Topological sort* (left) and *Stencil* (right).

## Acknowledgments

We thank Nathan Serafin, Nikhil Agarwal, Mitchell Fream, our anonymous reviewers, and our shepherd for their time and feedback. This work was generously funded by NSF grants CCF-2403144 and CCF-1845986. Souradip Ghosh was supported by the U.S. Department of Energy Computational Science Graduate Fellowship (DESC0022158).

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Received 2024-11-15; accepted 2025-03-06