An Integrated Circuit for Galvanostatic Electrodeposition of on-chip Electrochemical Sensors

Minghao Li*†, Atal A. S. Gill†, Anne Vanhoestenberghe‡, Sara S. Ghoreishizadeh†
*Division of surgery and interventional science, †Department of Electronics and Electrical Engineering, University College London, UK
‡School of Biomedical Engineering and Imaging Sciences, King's College London, UK
Email: {minghao.li.19, s.ghoreishizadeh, atal.gill@ucl.ac.uk}@ucl.ac.uk, a.vanhoest@kcl.ac.uk

***Abstract*— This paper presents the design of an integrated circuit (IC) for (i) galvanostatic deposition of sensor layers on the on-chip pads, which serve as the sensor's base layer, and (ii) amperometric readout of electrochemical sensors. The system consists of three main circuit blocks: the electrochemical cell including a 4×4 electrode array, two Beta-multiplier based current generators and one pA-size current generator for galvanostatic electrodeposition, and a switch-capacitor based amperometric readout circuit for sensor current measurement. The circuits are designed and simulated in a 180-nm CMOS process. The three current reference circuits generate a stable current from 7.2 pA to 88 µA with low process, power supply voltage and temperature (PVT) sensitivity. The pA-size current generator has a temperature coefficient of 517.8 ppm/°C on average (across corners) in the range of 0 to 60°C. The line regulation is 4.4 %/V over a supply voltage range of 0.8-3 V. The feasibility of galvanostatic deposition on on-chip pads is validated by applying a fixed current of 300 nA to electrochemically deposit a gold layer on top of electrodes with nickel/zinc as the adhesive layer for gold. Successful deposition of gold was confirmed using optical microscope images of the on-chip electrodes.**

***Index Terms*—current reference, subthreshold region, sensor fabrication, potentiostat, biosensor array, complementary metal–oxide semiconductor (CMOS), electrochemical sensor.**

I. Introduction

Electrochemical biosensors evolved rapidly over the last decades and are suitable for diverse applications, such as environmental monitoring, medical diagnosis and clinical investigation, due to their high sensitivity to target biomolecule, high specificity, inherent capability for miniaturization and low cost of batch manufacturing [1] – [4]. The miniaturization enables the establishment of large-scale sensor arrays and parallel detection of multiple biomolecules [2]. Amperometric electrochemical sensors typically use a three-electrode system to measure the concentration of analyte, which is proportional to the sensor current. Substantial progress with electrochemical biosensors has led to the development of commercial hand-held analyzers, which generally offer an attractive alternative to expensive, bulky and inconvenient instruments for health-care monitoring devices [3]. Electrochemical biosensors have proven a powerful tool for analyzing a variety of biomolecules such as glucose, lactate and oxygen [4].

The recent integration of electrochemical sensors and complementary metal–oxide semiconductor allows low cost, low power, portability and high scalability for parallel sensing [1]. The benefit of signal path reduction to micron size can only be achieved when sensing takes place on the surface of CMOS ICs [5]. The exposed top aluminum layer of on-chip pads can be used as the base on which the sensing element (such as antibody, enzyme, nanomaterial) is deposited to fabricate the sensing platform. The state-of-art techniques used to deposit these sensing elements include photolithography [2], electroless deposition [6] and the electrochemical deposition with external instruments [7]. These techniques require bulky external instruments, manual handling and lack of repeatability, which decreases their commercial potential. Therefore, to produce scalable, low-cost and autonomous sensing devices on CMOS, we propose to implement the electrochemical deposition technique on chip. The galvanostatic technique is one of the commonly used electrodeposition technique, in which the deposition takes place at constant current, while the potential remains uncontrolled. By programming a few parameters on the IC, a fixed current of different values can be generated to fabricate diverse metallic, nanostructure and organic layers when immersed in dedicated electrolytic solutions.

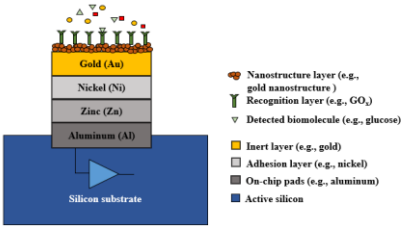

Fig.1. The envisaged cross-sectional view of an on-chip electrode.

The on-chip electrochemical sensors typically include an inert layer, adhesion layer, nanostructure layer and bio-recognition layer, as shown in Fig. 1. The majority of them may be deposited using galvanostatic techniques. To match the diversity of deposition parameters for different sensor layers, fixed currents of different values should be generated by the IC. This paper introduces an integrated system to enable the galvanostatic deposition of the inert metal layers, and the amperometric readout of the sensor current. The galvanostatic deposition procedure for a gold film, via chronopotentiometry, is presented in Section II. The experiment results of the gold electrodeposition and the simulation results of the pA-size current reference are presented in Section III and the conclusion is presented in Section IV.

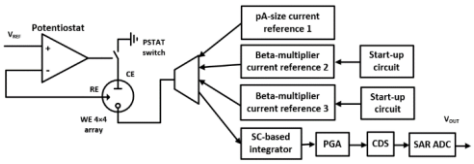

Fig.2. High level block diagram of the integrated system with three current references and an amperometric readout circuit.

TABLE I
ELECTRODEPOSITION PARAMETERS SUMMARY

Ref.	Deposits	Deposition time (s)	Temp. (°C)	Current density (A/cm^2)
[8]	Au	3600	45 - 65	0.003 – 0.006
[9]	Cu	30	N.A.	2
[10]	Ni	3600	25	0.03 - 5
[11]	Ag	15 - 200	27	-2
[12]	Prussian blue	N.A.	N.A.	-40 × 10^{-6}

II. System Design

A. *System specification*

Galvanostatic electrodeposition has been reported in the literature for gold [8], porous copper [9], nickel [10], silver nanostructures [11], platinum black and Prussian blue [12]. Table I summarizes the deposition parameters. The current density of the key layers ranges from 40 µA to 5 A/cm2. With an electrode surface area of 66×66 µm^2, to achieve the range of current densities suggested in Table I, the on-chip current generator must have a range of 7.2 pA to 88 µA. We expect variation from the nominal current amplitude of the current generators due to process variation, temperature dependence, and power supply voltage fluctuation. Work by Choi et al suggests that such tolerable variation can be mitigated by adjusting the electrodeposition time [13]. The amperometric readout circuit includes the switched capacitor transimpedance amplifier and the programmable amplifier prior to a 8-bit SAR ADC.

B. *System architecture*

Fig. 2 shows a high level block diagram of the integrated system for electrodeposition and amperometric readout of on-chip sensors. This design is based on previous work with the addition of two more new current references [1]. The electrochemical cell consists of a common reference electrode (RE), a common counter electrode (CE) and a 4×4 array of working electrodes (WEs). One working electrode is connected to either the electrodeposition circuits or the readout circuit at a single time, though a 16 to 4 multiplexer, while the other WEs are kept floating. The CE and RE are connected to an amplifier in negative feedback, forming a potentiostat.

Eight current amplitudes are selected to satisfy the requirements from Table I. The current reference 1 generates 7.2 pA for ultrasmall electrodes. The Beta-multiplier current reference 2 generates 1.7 nA, 30 nA, and 300 nA, and the current reference 3 with the same topology generates 2.17 µA, 15 µA, 21.7 µA, 44 µA, and 88 µA, using a digitally controlled current mirror, as shown in Fig. 3. The principle of the designed Beta multiplier current reference as well as the amperometric readout circuit were explained in detail in previous work [1].

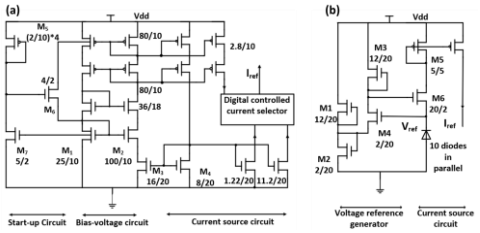

Fig.3. Schematic of (a) the proposed Beta multiplier current reference. (b) The pA-size current reference.

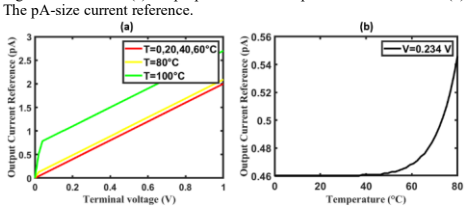

Fig.4.(a) N/PW diode simulated I-V characteristics with different temperature. (b) Simulated temperature dependence of diode current.

The current reference 1 is expected to generate a constant current of 7.2 pA without resistors. Only a few prior-art pA-size current references have been reported. Some of the circuits [14], [15] generate a reference current through applying a voltage across a gate-leakage transistor, however the gate leakage current is only small enough when the gate oxide thickness is less than 20 Å. The typical value of the gate oxide thickness is 40 Å in the 180 nm CMOS process, which makes the utilization of gate leakage transistors impractical. Choi et al [16] use a complementary to absolute temperature (CTAT) voltage reference which takes advantage of native transistors to drive a subthreshold-region transistor, but not all CMOS technologies support native transistors. Camacho-Galeano et al [17] proposes a simple topology with regular transistors but has a high temperature coefficient and line regulation. This challenge is overcome by utilizing a reverse-connected diode to replace resistors to achieve a pA-size current. Based on Shockley's equation, the reverse current of diodes varies with temperature, as the reverse saturation current doubles for every 10°C rise in temperature, and is almost independent with operating voltage [18]. However, the simulated I-V characteristics of the N/+PW diode in Fig.4 shows an opposite results, which nearly follows Ohm's law and the temperature dependence is negligible in the range of 0 - 60°C. The linear I-V characteristics may be caused by the increasing junction leakage current as the substrate is connected to the cathode with higher voltage.

Fig.3.(b) shows the schematic of the current reference where the diodes act as a GΩ-size resistor. The stacked reference voltage generator consists of four transistors, M1-M4 to produce a CTAT voltage around 0.23 V to compensate for the temperature dependence of the resistance in the diodes. M6 is a common drain NMOS, employed as a voltage buffer due to its input and output following characteristics. M5 is utilized to reduce the impact of Vdd on the output current, which is in

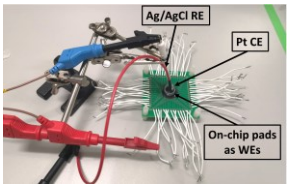

Fig. 5 Experiment setup with an electrode test chip.

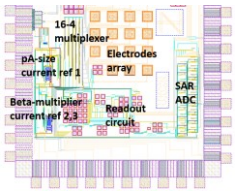

Fig. 6 Layout of the 1.7×1.7 mm CMOS chip.

a cascode configuration. Eq. (2) shows the temperature coefficient of the current reference:

$$I_D = I_S(e^{V_D/V_T} - 1) \tag{1}$$

$$\frac{dI_{ref}}{dT} = \frac{m_2 k}{qR_D} \ln \frac{\mu_1 C_{OX}(m_1 - 1)K_1}{\mu_2 C_{OX}(m_2 - 1)K_2} + \frac{m_1 C_{vth2} - m_2 C_{vth1}}{m_1} \tag{2}$$

where R_D is the equivalent resistance of diodes, m is the subthreshold slope factor, C_{vth} is the temperature coefficient of threshold voltage.

Thus, the optimal aspect ratio of M1 and M2 (as well as M3 and M4) are calculated to obtain a CTAT voltage. The bulk of all transistors are connected to their source node as reported in Fig.3 to reduce the body effect.

C. *Materials and methods for gold deposition*

An electrode test chip was glued to a printed circuit board (PCB) with silver conductive epoxy (MG Chemicals 8331D) and wire-bonded to the PCB. The wire-bonds were covered using epoxy (Masterbond EP41S-5). An autolab potentiostat, PGSTAT204, was used to carry out the electrochemical deposition with a three electrode setup, shown in Fig.5, with a Ag/AgCl electrode as reference, a platinum wire as the counter electrode and the aluminum pad as the working electrode. The electrode test chip consists of an array of on-chip pads with various dimension including 66×66 μm^2 and 128×128 μm^2 which were used in this experiments.

The electrochemical deposition of gold on the aluminum electrodes is carried out in two steps: (i) Electroless deposition of zinc and nickel films, (ii) electrochemical deposition of gold film. All solutions were prepared in deionized (DI) water. Nickel electroless plating solution was prepared by mixing 1 mL solution of nickel sulphate (28 g/L) and 1 mL solution of sodium hypophosphite (27 g/L). Xenolyte Zincate CFA was used as the electroless zinc plating solution and NB Semiplate Au-100 was used as gold electroplating solution.

Step (i) is a slight modification on the electroless deposition method described by Hwang et. al [19]. This involved the initial cleaning of the electrodes with DI water, followed by immersion with sodium hydroxide (10 %) to remove the oxide layer from the aluminium electrodes for 1 min. Then the electrodes are cleaned with DI water, which is followed by de-smutting with 20% nitric acid for 1 min. After obtaining a clean surface and removing the acid remains with DI water, a drop of Xenolyte Zincate CFA solution is put on the electrodes at 45°C for 2 mins. The de-smutting and zinc plating step is repeated twice to achieve a smooth zinc coating for nickel deposition. Nickel deposition was carried out covering the chip by a drop of nickel plating solution at 90°C for 15 mins.

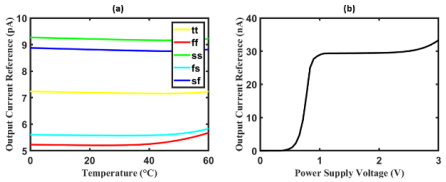

Fig. 7. Simulated output current of pA-size current reference I_{OUT} as a function of (a) temperature from four different corners. (b) supply voltage.

Step (ii), Step (ii), electrochemical deposition: two individual electrode pads were deposited with each of the following current amplitudes, 100 nA, 300 nA, 500 nA, 2 µA and 22 µA, in a 3 electrode setup with 350 µL of NB Semiplate Au-100 as the electrolyte solution. Currents of 300nA, 2 µA and 22 µA can be generated by the designed current references. Although an external setup was used here for validation, these amplitudes are capable of being produced by the circuit described in this paper. For each pad, the current was applied for 600 seconds at room temperature.

Commented [LM1]: The explanation of why I choose these currents is added.

III. RESULTS

A. *Current reference*

The schematic-level circuit was simulated in the 180 nm CMOS process using Cadence V6. The layout of the integrated system is presented in Fig. 6, the circuits occupies a total area of 2.9 mm^2.

Corner simulations were performed to simulate the process variation in the worst scenarios. Fig. 7. (a) shows the simulated output current I_{ref} as a function of temperature within 0-60°C at different process corners. The temperature coefficient is 517 ppm/°C on average, while the temperature coefficient ranges from 185 (tt corner) to 1480 ppm/°C (ff corner). This relatively low temperature coefficient was achieved through optimising the dimensions of M1 and M2 (or M3 and M4) in the stacked voltage generator. The pA-size current reference generates an average current of 7.2 pA with a standard deviation of 0.82 pA (11.4%) when the supply voltage is 1.8 V and consumed an average power of 1.6 nW at room temperature. The results in Fig.7. (b) show line sensitivity of 4.4 %/V at room temperature with the power supply voltage over 1.8 V. The sub-threshold transistors are more sensitive to the process variation which can be minimized by adding a programmable transistor M2 (M4).

Table II summarizes the circuit performances and provides a comparison with other pA-size current references. This design is suitable for a wide range of CMOS technologies as only regular transistors are used.

TABLE II
COMPARISON WITH REPORTED PA-SIZE CURRENT REFERENCES

Specifications	This work*	[14]	[15]	[16]	[17]
Process, CMOS	180 nm	65nm	130nm	180nm	1500nm
V_{DD} (V)	0.8-3	> 0.4	0.7	> 1.2	> 1.1
Temp. (°C)	0 - 60	-20-60	0 - 80	0 - 80	-20 - 80
I_{REF} (pA)	7.2	1.2	3.2	20	410
$T.C._{ave}$ (ppm/°C)	517.8	469	201	780	2500
Power (pW)	1632	3.4	6	23	2000
Line reg. (%/V)	4.4	2.5	0.62	0.58	6
Process var. (%)	11.3	17.5	4	2	N.A.

*This work is based on simulation results.

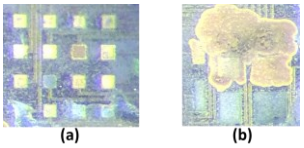

Fig. 8. Optical microscope images of the on-chip pad array (a) Gold plating on the 66×66 μm^2 electrode at nA current. (b) Overflow on the 128×128 μm^2 electrode at µA current.

B. Results and discussion for gold layer deposition

The direct deposition of gold films over aluminum is not recommended due to poor adhesion and gold aluminum inter-diffusion. Therefore, zinc and nickel layers were used as barrier and adhesive layers prior to gold deposition [8]. The deposition of a zinc layer also prevents the re-oxidation of the aluminum surface and provides a base for direct electroless deposition of nickel. This nickel layer eases the gold deposition on top of itself and prevent the inter-diffusion of other metals into the gold film. The selective deposition of gold was obtained as shown in Fig.8(a), taken under an optical microscope. The optical images show that the nA-size currents electrochemical deposit bright and smooth gold film layer on the 66×66 μm^2 electrode array.

The quality of the gold film with galvanostatic deposition depends on three parameters: (i) the amplitude of current applied on the electrode; (ii) the quality of the gold coating solution; (iii) the base of the electrode which was the electroless nickel and zinc films. In this work we achieve a uniformly coated film by; firstly, limiting the current in nA range as it was observed that higher amplitude (µA) currents led to an overflow of gold outside the electrode and formation of 3-D structure as shown in Fig.8(b). Secondly, the gold coating solution was changed after plating two electrodes as a precaution to prevent low gold in the electrolyte due to low quantity (350 µL) of electroplating solution. Thirdly, the base of electrode was well isolated via electroless coated nickel and zinc films. The recommended 300 nA constant current can be generated by the designed current reference. The successful deposition under 100nA and 500nA illustrates the tolerable of current variation.

IV. Conclusion

The circuit includes a set of current references that generate currents from 7.2 pA to 88 µA for galvanostatic electro-deposition of sensor layers on chip. Results of early tests at 300 nA, with an external setup, demonstrate the feasibility of our approach. This is a system designed towards autonomous fabrication of on-chip electrodes. The future work is to design the voltage generation circuit and digital control blocks.

Acknowledgement

The authors thank Dr. Kerim True for designing the electrode test chip and helping with the tape out of this IC.

References

[1] M. Li, A. Vanhoestenberghe and S. S. Ghoreishizadeh, "An integrated circuit to enable electrodeposition and amperometric readout of sensing electrodes, " IEEE Latin America Symp. on Circuits Syst., Mar. 2022.

[2] C. Yang, S. R. Jadhav, R. M. Worden, A. J. Mason, "Amperometric Electrochemical Microsystem for a Miniaturized Protein Biosensor Array," IEEE Trans. Biomed. Circuits Syst., vol. 3, no. 3, June 2009.

[3] A. J. Bandodkar and J. Wang, "Non-invasive wearable electrochemical sensors: review," A Trends Biotechnol., vol. 32, no. 7, pp. 363–371, Jul. 2014.

[4] Ciobanu. M, Taylor. D.E, Wilburn. J.P, Cliffel. D.E, "Glucose and lactate biosensors for scanning electrochemical microscopy imaging of single live cells. " Anal. Chem.,no.80, pp. 2717–2727, Mar. 2008.

[5] L. Li, H. Yin, and A. J. Mason, "Epoxy chip-in-carrier integration and screen-printed metalization for multichannel microfluidic lab-on CMOS microsystems," IEEE Trans. Biomed. Circuits Syst., vol. 12, no. 2, pp. 416–425, Apr. 2018.

[6] X. Zhou, E. Mai, M. Sveiven, C. Pochet, et al. "A 9.7-nT_{rms}, 704-ms Magnetic Biosensor Front-End for Detecting Magneto-Relaxation, " IEEE J. Solid-State Circuits, vol. 56, no. 7, pp. 2171-2181, July 2021.

[7] S. Ghoreishizadeh, I. Taurino, G. D. Micheli, S. Carrara, and P. Georgiou, "A differential electrochemical readout ASIC with heterogeneous integration of bio-nano sensors for amperometric sensing," IEEE Trans. Biomed. Circuits Syst., vol. 11, no. 5, pp. 1148–1159, Oct. 2017.

[8] N. Saeidi, M. Schuettler, A. Demosthenous, N. Donaldson, "Technology for integrated circuit micropackages for neural interfaces, based on gold–silicon wafer bonding," Micromech. Microeng., vol. 23, no. 7, June 2013

[9] H. Zhang, Y. Ye,1, R. Shen, C. Ru, Y. Hu, "Effect of Bubble Behavior on the Morphology of Foamed Porous Copper Prepared via Electrodeposition," J. Electrochem. Soc., vol. 160, no. 10, July 2013.

[10] C.A. Marozzi, A.C. Chialvo, "Development of electrode morphologies of interest in electrocatalysis: Part 2: Hydrogen evolution reaction on macroporous nickel electrodes, " Electrochimica Acta, vol. 46, no. 6, pp. 861–866, 2001.

[11] L. Mattarozzi, S. Cattarin, N. Comisso, P. Guerriero, M. Musiani and E. Verlato, "Preparation of porous nanostructured Ag electrodes for sensitive electrochemical detection of hydrogen peroxide," Electrochimica Acta, vol. 198, pp. 296–303, 2016.

[12] A. Roig, J. Navarro, J.J. Garcia, F. Vicente, "Voltammetric study of the stability of deposited Prussian blue films against succesive potential cycling", Electrochimica Acta, vol. 39, no. 3, pp. 437–442, 1994.

[13] Double-template fabrication of three-dimensional porous nickel electrodes for hydrogen evolution reaction

[14] H. Wang and P. P. Mercier, "A 3.4-pW 0.4-V 469.3 ppm/°C FiveTransistor Current Reference Generator," IEEE Solid-State Circuits Lett., vol. 1, no. 5, pp. 122–125, May 2018.

[15] H. Zhuang, J. Guo, C. Tong, X. Peng, and H. Tang, "A 8.2-pW 2.4-pA current reference operating at 0.5 V with no amplifiers or resistors," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 7, pp. 1204–1208, Jul. 2020.

[16] M. Choi et al., "A 23pW, 780ppm/0C resistor-less current reference using subthreshold MOSFETs," in Eu. Solid-State Circuits Conf., 2014.

[17] E. M. Camacho-Galeano and C. Galup-Montoro, "A 2-nW 1.l-V self-biased current reference in CMOS technology, " IEEE Trans. Circuits Syst. D, Exp. Briefs, vol. 52, no. 2, pp. 61-65, Feb. 2005.

[18] Bogart, F. Theodore Jr. "Electronic Devices and Circuits": Merill Publishing Company, 1986.

[19] Hwang, S., LaFratta, C.N., Agarwal, V., Yu, X., Walt, D.R. and Sonkusale, S., 2009. CMOS microelectrode array for electrochemical lab-on-a-chip applications. IEEE Sensors Journal, 9(6), pp.609-615.

Commented [LM2]: I add the electrode size in Fig.8