Roll No. _____ Name_____ Group_____

Computer Science & Engineering Department
Thapar Institute of Engineering & Technology, Patiala
Computer Architecture and Organization (UCS510/UCS319)
Theory Quiz-2 (Set-A) [November 28, 2023]

Time: 20 min [05:15 PM - 05:35 PM] **Max Marks: 15**

Instructions for students:

- Any cutting or overwriting will be considered as a wrong answer.
- Missing roll number or name will be considered as an absent.
- No Negative marking is there and No extra material is allowed.
- It is mandatory to write your answers at the end of the given table.

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1. Consider a 3-stage pipelined processor having a delay of 5ns (nanoseconds), 10 ns, and 4 ns, for the first, second, and third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also, assume that one instruction is fetched every cycle. What would be the total execution time for executing 100 instructions on this processor?

a. 1000ns
b. 1020ns
c. 2040ns
d. 1030ns

2. The contention for the usage of a hardware device is called _____?

a. Structural hazard
b. Control hazard
c. Data hazard
d. Stall

3. The 5 stages of the processor have the following latencies:

Fetch	Decode	Execute	Memory	Writeback
350ps	300ps	380ps	390ps	340ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages. What is the cycle time in pipelined processor?

a. 390ps
b. 410ps
c. 400ps
d. 360ps

4. Consider a pipeline having 4 phases with duration 20, 30, 40 and 35ns. Given latch delay is 10 ns. What would be the speed up ratio?

a. 2.7
b. 2.8
c. 2.5
d. 2.9

5. Consider the following instructions and identify the type of data hazard between the Instruction I_1& I_2_____ and I_2& I_3_____ respectively.

I_1: ADD R_0, R_2, R_1
I_2: SUB R_4, R_3, R_0
I_3: MUL R_4, R_5, R_6

6. The cache memory of 1K words uses direct mapping with a block size of 4 words. How many blocks can the cache accommodate?

a. 256 words
b. 128 words
c. 512 words
d. 1024 words

7. A page fault occurs when

a. there is an error on a specific page
b. a program accesses a page of main memory
c. a program accesses a page belonging to another program
d. a program accesses a page not currently in main memory

8. Specify the control word of 14 bits that must be applied to the processor to implement the micro-operation:

$R_4 \leftarrow$ shl R_3

R_3 and R_4 is of 3bits and shl is 11000.
Ans:

9. A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2k bytes of RAM, and 4k bytes of ROM. What will be the address range of the ROM if the two highest-order bits of the address bus are assigned 01?

a. $(4000)_H$ to $(4FFF)_H$
b. $(0000)_H$ to $(4FFF)_H$
c. $(4000)_H$ to $(47FF)_H$
d. $(0000)_H$ to $(0FFF)_H$

10. The two numbers given below are multiplied using the Booth's algorithm:
Multiplicand: 0101 1010 1110 1110
Multiplier: 0111 0111 1011 1101
How many additions/Subtractions are required for the multiplication of the above two numbers?

a. 6
b. 8
c. 10
d. 12

11. Consider a 16 bit processor in which the following appears in main memory starting at location 38246:

38246	JMP	Mode
38247	-12	
38248	Next Instruction	

The first byte of the instruction specifies the opcode and type of addressing mode used. Second byte of the instruction is the address field. Determine the effective address of the instruction to transfer the control if the mode field uses the PC-relative addressing mode.

a. 38234
b. 38235
c. 38236
d. 38248

12. The temporal aspects of the locality of reference means

a. The recently executed instruction is temporarily not referenced.
b. All those instructions which are stored nearby to the recently executed instruction have high chances of execution.
c. The recently executed instruction will be executed soon again in near future.
d. The recently executed instruction will not be executed soon again.

13. Which of the following type of address instruction format support PUSH and POP operation?

a. Zero-address Instruction
b. One-address Instruction
c. Two-address Instruction
d. Three-address Instruction

14. Booth algorithm gives a procedure for multiplying binary integers in _____ representation.

a. signed-2's complement
b. signed-magnitude
c. signed-1's complement
d. sign-complement

15. An 8-bit computer has a register R contains the value in hexadecimal A2. Determine the values of status bits:

a. C: _____
b. S: _____
c. Z: _____
d. V: _____

after the execution of Exclusive-OR operation on R with R.

Q. No.	**1.**	**2.**	**3.**	**4.**	**5.**	**6.**	**7.**	**8.**	**9.**	**10.**	**11.**	**12.**	**13.**	**14.**	**15.**
Correct Answer	**B**	**A**	**B**	**C**	**RAW WAW**	**A**	**D**	**011 000 100 11000**	**A**	**B**	**C**	**C**	**A**	**A**	**0 0 1 0**