Estimation of Wirelength Reduction for
λ-Geometry vs. Manhattan Placement and Routing*

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ABSTRACT

λ-geometry routing has recently received much attention due to the potential for reduced interconnect length in comparison to today's prevalent Manhattan routing. An accurate cost-benefit analysis of λ-geometry routing is impossible without good estimation of the wirelength reduction expected when switching from Manhattan to λ-geometry routing. However, in the literature, estimates of wirelength improvements achieved by λ-geometry routing are usually for randomly generated nets, and the effect of λ-geometry-driven placement on the overall wirelength improvement is not properly considered. In this paper, we improve existing estimates for the wirelength reduction of various λ-geometry interconnect architectures. First, we give more accurate estimations of the expected wirelength reduction given by λ-geometry routing on Manhattan placements. We take into account the effect of wirelength-driven Manhattan placement on pin locations for nets with $k = 2$, 3 and 4 pins, and observe smaller expected reductions compared to previous estimates based on nets randomly located in the plane. Second, we estimate the wirelength improvement achieved by λ-geometry placement and routing versus Manhattan placement and routing. Our estimate is based on a simulated annealing placer, driven by λ-geometry metrics. Finally, we discuss and analyze the "virtuous cycle" effect: reduction of overall wirelength results in decreased routing area, which in turn leads to further wirelength reduction.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: INTEGRATED CIRCUITS —*Design Aids*

General Terms

Algorithms, Measurement, Performance

Keywords

Wirelength Reduction Estimation, λ-Geometry Routing, λ-Geometry-Driven Placement

1. INTRODUCTION

Because of its restrictions on routing directions, the Manhattan architecture entails significant added wirelength beyond the Euclidean optimum. Non-Manhattan routing has recently received much attention from both academia and industry ([1, 9, 13, 14, 16]) due to the potential for reduced interconnect length (and hence improved power consumption and timing) in comparison to today's prevalent Manhattan routing. Most attention has been devoted to λ-geometry routing, in which routing is allowed along $\lambda > 2$ orientations forming consecutive angles of π/λ. In particular, $\lambda = 2$, 3, 4 and ∞ correspond to Manhattan architecture, Y-architecture, X-architecture and Euclidean geometry, respectively.

An accurate cost-benefit analysis of λ-geometry routing is impossible without good estimation of the wirelength reduction expected when switching from Manhattan to λ-geometry routing. However, the literature contains only simplistic (and seemingly conflicting) estimates.

- For nets with 10 or more pins, experiments with both exact [12] and heuristic Steiner algorithms [2, 3, 4] suggest an average improvement between Manhattan and octilinear Steiner trees of approximately 10% when the nets are randomly generated, and even smaller improvements when nets are extracted from real VLSI designs.

- For 2-pin nets, the octilinear over Manhattan improvement is estimated to be 17.17% in [9], respectively 14.6% in [14]. [9] and [14] assume different probability distributions over 2-pin nets: in [9] one pin is assumed to be chosen uniformly at random from an Euclidean circle centered at the other pin, while in [14] the Euclidean circle is replaced by a Manhattan circle.

- For full commercial designs placed and routed with octilinear-aware tools, [8] and [14] report wirelength improvements of 20% or more.

The previous estimates do not adequately address k-pin nets ($k > 2$) and the fact that nets are not randomly placed

in the plane, but are rather driven by Steiner Minimal Tree (SMT) cost minimization in the prevailing geometry; the importance of this was previously mentioned in [13, 14]. Also the effect of λ-geometry-driven placement on the overall wirelength improvement needs to be considered. Wirelength reduction achieved by λ-geometry routing is limited without such a λ-geometry-aware placer.

In this paper, we study wirelength reduction for λ-geometry routing applied to both Manhattan and λ-geometry placements. We improve existing estimates for the wirelength reduction of various interconnect architectures by taking into account the effect of wirelength-driven Manhattan or λ-geometry placements on pin locations for nets with $k = 2$, 3 and 4 pins. We observe smaller expected reductions compared to previous estimates based on nets randomly located in the plane. We estimate the wirelength improvement achieved by λ-geometry versus Manhattan placement and routing, using a simulated annealing placer, which is driven by λ-geometry metrics. And finally, we discuss and analyze the "virtuous cycle" effect: reduction of overall wirelength results in decreased routing area, which in turn leads to further wirelength reduction.

The remainder of the paper is organized as follows. Section 2 studies wirelength reduction for λ-geometry routing of nets from Manhattan-driven placement. Section 3 discusses the wirelength improvement achieved by λ-geometry placement and routing versus Manhattan placement and routing. The paper concludes in Section 4.

2. WIRELENGTH IMPROVEMENTS WITH λ-GEOMETRY ROUTING ON MANHATTAN PLACEMENTS

When wirelength reduction achieved by non-Manhattan routing is discussed, nets are often assumed to be randomly placed, and average wirelength reduction is computed using heuristic or exact Steiner tree algorithms. But compared with wirelength improvements for nets extracted from real VLSI designs, the above estimates are usually much larger [2, 3, 12]. One reason for this difference is that in real VLSI designs nets are not randomly placed in the plane, but are rather driven by SMT cost minimization.

In [14], average wirelength improvement for octilinear routing is computed by an integral formula, assuming that Manhattan placers optimize only interconnect wirelength for 2-pin nets: a second point is uniformly distributed on the "rectilinear unit circle" around the first point. In this section, we extend this idea and give more accurate analysis of interconnect length reduction of different interconnect architectures, for nets with $k = 2$, 3 and 4 pins from Manhattan placement. Our results show smaller wirelength improvements obtained by λ-geometry routing, compared to previous estimates based on randomly generated nets. Table 1 summarizes related analysis in the literature.

2.1 2-Pin Nets

We assume a placer driven by λ-geometry metrics optimizes only interconnect wirelength for 2-pin nets. Suppose there is a 2-pin net between two components A and B. Given a location for A and an interconnect length L, B will be placed uniformly on the "λ-geometry circle" centered at A with λ-geometry radius L. For $\lambda = 2$, 3, 4 and ∞ respectively, the λ-geometry circle is a diamond, a hexagon, an

Table 1: Related analyses of wirelength reduction for λ-geometry routing.

reference	placement	routing	k-pin nets
[13]	random	$\lambda = 4$	$k = 2$
[1]	random	$\lambda = 3, 4, \infty$	$k = 2$
[14]	Manhattan	$\lambda = 4$	$k = 2$
This paper	λ-geometry	$\lambda = 3, 4, \infty$	$k = 2, 3, 4$
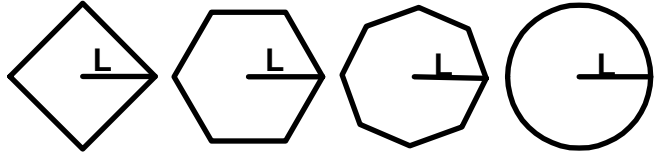
Figure 1: λ-geometry circles with $\lambda = 2$, 3, 4 and ∞.

octagon and a circle, as shown in Figure 1.

Under these assumptions about the placer, the expected wirelength of a 2-pin net routed in λ'-geometry can be computed using integrals. The results for $\lambda, \lambda' \in \{2, 3, 4, \infty\}$ are summarized in Table 2; the detailed analysis is given in the Appendix.

2.2 3-Pin Nets

We may similarly analyze the regime where all placements of a 3-pin net with the same rectilinear SMT length are equally possible. For a 3-pin net with a bounding box BB, there are two possibilities: 1) *canonical case*: one point A is at one corner of the bounding box, and the other two points are on the two edges opposite to A; 2) *degenerated case*: two points are at the two opposite corners of the bounding box, and the other point is in the bounding box.

Given a bounding box BB with half perimeter L and length x, $0 \leq x \leq L$, randomly select u and v such that $0 \leq u \leq x$ and $0 \leq v \leq L - x$. Each combination of u and v specifies a canonical 3-pin net $\{(0, 0), (u, L - x), (x, v)\}$ and a degenerated 3-pin net $\{(0, 0), (u, v), (x, L - x)\}$; both of these 3-pin nets have an SMT length of L. All canonical and degenerated 3-pin nets with bounding box BB can be uniformly sampled in this way. Considering orientations of 3-pin nets, we need to multiply the wirelength of canonical nets by 4, and multiply that of degenerated nets by 2.

To uniformly sample 3-pin nets with different bounding box aspect ratio, the probability of sampling the bounding box with length x should be proportional to $x(L-x)$.[1] Given a uniform sampling of all possible placements for a 3-pin net, the average SMT length with λ-geometry routing can be computed using the Geosteiner algorithm [12].

2.3 4-Pin Nets

For a 4-pin net with a bounding box BB, similar analysis covers three possibilities. Case 1 is the canonical case where all points are on the edges of the bounding box. Case 2 has one point A at a corner, two points on the edges opposite to A, and the fourth point in the bounding box. Case 3 has two points at two opposite corners, and the other two points in the bounding box.

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[1] Given a uniform sampling $t \in [0, 1]$, $x = Q^{-1}(t)$ gives a sampling of x with probability density $p(x)$, where $p(x) \geq 0$, $x \in [0, 1]$, $\int_0^1 p(x)dx = 1$, and $Q(t) = \int_0^t p(x)dx$.

Table 2: Expected wirelength of a 2-pin net routed in λ'-geometry, assuming a λ-geometry-driven placer and λ-geometry length of L_λ.

λ-geometry placement	λ'-geometry routing			
	$\lambda' = 2$	$\lambda' = 3$	$\lambda' = 4$	$\lambda' = \infty$
$\lambda = 2$	L_2	$0.894\ L_2$	$0.854\ L_2$	$0.812\ L_2$
$\lambda = 3$	$1.161\ L_3$	L_3	$1.070\ L_3$	$0.912\ L_3$
$\lambda = 4$	$1.207\ L_4$	$1.047\ L_4$	L_4	$0.950\ L_4$
$\lambda = \infty$	$1.273\ L_\infty$	$1.103\ L_\infty$	$1.055\ L_\infty$	L_∞
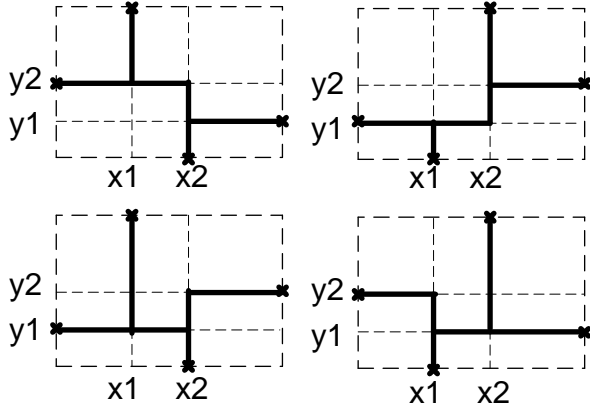
Figure 2: Canonical 4-pin nets.

Figure 3: Degenerated 4-pin nets.

Table 3: Average wirelength reduction for nets from Manhattan placement and random nets (%).

net size	$\lambda = 3$		$\lambda = 4$		$\lambda = \infty$	
	Manh.	Rand.	Manh.	Rand.	Manh.	Rand.
k = 2	10.57	13.52	14.65	17.14	18.84	21.47
k = 3	5.86	7.55	10.75	12.41	14.61	16.21
k = 4	5.45	6.56	9.89	11.26	13.30	14.80
average	8.70	11.05	13.00	15.11	16.97	19.19

Given a bounding box BB with half perimeter L and length x, $0 \leq x \leq L$, we randomly select $x1$, $x2$, $y1$ and $y2$ such that $0 \leq x1 \leq x2 \leq x$ and $0 \leq y1 \leq y2 \leq L - x$. Each combination of $x1$, $x2$, $y1$ and $y2$ specifies four canonical (Case 1) 4-pin nets (Figure 2), four Case-2 nets and two Case-3 nets (see Figure 3 for examples of degenerated 4-pin nets).[2] All 4-pin nets that have a bounding box with the same aspect ratio as BB can be uniformly sampled in this way.
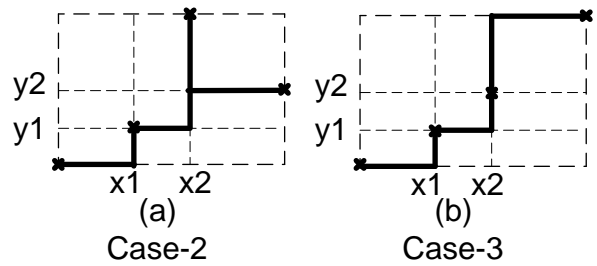
Analogous to the 3-pin analysis, we weight the wirelengths for different cases to account for orientation: the weights for the three cases are 1, 4 and 2 respectively. To uniformly sample 4-pin nets with different bounding box aspect ratio, the probability of sampling the bounding box with length x is proportional to $x^2(L - x)^2$.

Table 3 summarizes average wirelength reductions using λ-geometry routing for nets with $k = 2$, 3 and 4 pins from Manhattan wirelength-driven placement. The results are compared with average wirelength improvements achieved by λ-geometry routing for nets randomly picked from a square. For every λ, we observe smaller wirelength reduction for λ-geometry routing of nets from Manhattan wirelength-driven placement. In the last row of Table 3 we give the wirelength improvement expected for λ-geometry routing of a net, based on the average net degree distribution in [10, 11].

3. WIRELENGTH IMPROVEMENTS WITH λ-GEOMETRY PLACEMENT AND ROUTING

A λ-geometry-aware placer factors λ-geometry wiring dur-

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[2] Some nets have an SMT length greater than L, and need to be scaled down.

ing placement, and results in better distribution of nets when such wiring is used to route the nets. Wirelength improvement with λ-geometry routing ($\lambda > 2$) is impaired if the placer is only optimized for Manhattan wiring, since the placer poorly positions the nets in the IC layout. Previous studies of the routing demand using different traditional placers [5] show that for octilinear routing there is relatively little demand for the two diagonal directions. The placement tools align most circuit elements either vertically or horizontally, leaving few opportunities to exploit diagonal wiring. On the other hand, a λ-geometry-driven placer can place the nets in more locations that cost the same, which in turn opens up more positions for other nets. Therefore, the wirelength can be greatly reduced.

3.1 Estimation with a Simulated Annealing Placer

To estimate the wirelength improvement achieved by λ-geometry placement and routing versus Manhattan placement and routing, we have built a simplified placer, which uses simulated annealing driven by λ-geometry wirelength estimation. The input of the placer is a simplified netlist extracted from MCNC instances, in which, a list of cells is specified for each net. After a random initial placement of cells, two cells are randomly selected, and we decide whether to exchange these two cells based on the current temperature and the new SMT cost with λ-geometry routing, which is computed using Geosteiner. The initial temperature of the simulated annealing algorithm is specified so that it is far larger than the standard deviation of the cost distribution [6]. For each temperature, a repeat time is specified so that the number of new states generated is on the order of 100 times the number of cells [7]. And the new temperature is generated by multiplying the current temperature by $\alpha = 0.95$, which is a relatively large α for simulated annealing [7].

For each instance and each λ-geometry metrics, we run the placer 5 times, and get the best wirelength with λ-geometry placement and routing. The wirelength improvements achieved by λ-geometry placement and routing are

Table 4: Average wirelength improvements for λ-geometry placement and routing vs. Manhattan placement and routing (%).

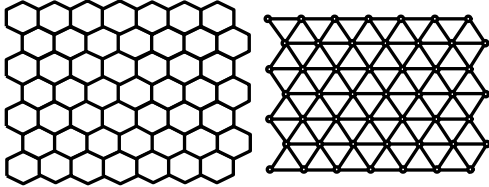| Instance	#nets	$\lambda = 3$	$\lambda = 3$ hex cells	$\lambda = 4$	$\lambda = \infty$
C2	601	3.43	4.81	8.92	11.04
BALU	658	3.96	7.13	9.29	11.07
PRIMARY1	695	5.67	7.32	10.31	13.03
C5	1438	6.24	8.34	11.48	12.73

Figure 4: Layout of hexagonal cells on a rectangular chip and the triangular mesh that connects them.

summarized in Table 4. In Tables 5 and 6 we give total wirelength obtained with different combinations of placement and routing for two of the testcases, C2 and Balu.

From the tables, we can see that square cells are not quite suitable for 3-geometry. When the placer is optimized for Manhattan wiring, the total wirelength with tri-directional routing is usually larger than that with rectilinear routing. And the wirelength improvements with 3-geometry placement and routing are relatively small, compared to the wirelength improvements when $\lambda = 4$ and ∞. Therefore, hexagonal cells [9, 17] are adopted when the placer is driven by 3-geometry wirelength. The cell layout on the chip and the mesh connecting them are shown in Figure 4. The total wirelength with 3-geometry placement and routing is improved significantly by the use of hexagonal cells.

Table 5: Total wirelength of instance "C2" with different combinations of placement and routing.

λ-geometry driven placer	λ-geometry routing			
	$\lambda = 2$	$\lambda = 3$	$\lambda = 4$	$\lambda = \infty$
$\lambda = 2$	1805	1841.8	1719.2	1683.9
$\lambda = 3$	1896	1743.0	1665.9	1621.5
$\lambda = 3$, hex cells	2002	1690.3	1718.3	1640.8
$\lambda = 4$	1908	1799.6	1644.0	1617.4
$\lambda = \infty$	1865	1772.1	1646.9	1605.7

3.2 Analysis of the "Virtuous Cycle" Wirelength Reduction Effect

The above placer puts cells in a chip with fixed area. However, reduction of overall wirelength results in decreased routing area, which in turn leads to further wirelength reduction, and this determines a "virtuous cycle" effect.

Consider a cluster of two-pin nets, which are connected to one pin A. All other pins are uniformly located in a λ-geometry circle by a λ-geometry-aware placer. Based on the "virtuous cycle" effect, the λ-geometry circle will have an area proportional to the total routing area. For Manhattan placement and routing, suppose the pins are placed in a rectilinear circle with radius R. We have the area of

Table 6: Total wirelength of instance "Balu" with different combinations of placement and routing.

λ-geometry driven placer	λ-geometry routing			
	$\lambda = 2$	$\lambda = 3$	$\lambda = 4$	$\lambda = \infty$
$\lambda = 2$	1820	1856.0	1728.4	1694.7
$\lambda = 3$	1878	1748	1660.8	1623.6
$\lambda = 3$, hex cells	2010	1718.2	1744.0	1669.3
$\lambda = 4$	1886	1785.6	1650.9	1621.3
$\lambda = \infty$	1898	1769.8	1654.6	1616.5

Table 7: Total wirelength of instance "C7" with different combinations of placement and routing.

λ-geometry driven placer	λ-geometry routing			
	$\lambda = 2$	$\lambda = 3$	$\lambda = 4$	$\lambda = \infty$
$\lambda = 2$	6802	6859.1	6419.1	6276.9
$\lambda = 3$	6942	6396.2	6104.4	5959.9
$\lambda = 3$, hex cells	7382	6254.0	6342.1	6056.4
$\lambda = 4$	6840	6400.1	5945.9	5848.7
$\lambda = \infty$	6806	6370.8	5971.2	5823.5

the rectilinear circle: $A = 2R^2$, and the total routing area: $A_{\text{routing}} = 4 \int_0^R (x \cdot \frac{x dx}{A} N) = \frac{4}{3} \frac{R^3}{A} N = \frac{2}{3} R N$, where N is the number of two-pin nets and $\frac{x dx}{A} N$ is the number of pins located between unit circles with radius x and $x + dx$. Let $A \sim A_{\text{routing}}$. We have $R \sim N/3$ and $A_{\text{routing}} \sim \frac{2}{9} N^2$. Similar analysis is done for λ-geometry placement and routing with $\lambda = 3$, 4 and ∞, and the results are summarized as follows:

$\lambda = 2$: $A_{\text{routing}} \sim \frac{2}{9} N^2$

$\lambda = 3$: $A_{\text{routing}} \sim \frac{8\sqrt{3}}{81} N^2$, 23.0% less compared to Manhattan placement and routing.

$\lambda = 4$: $A_{\text{routing}} \sim \frac{\sqrt{2}}{9} N^2$, 29.3% less compared to Manhattan placement and routing.

$\lambda = \infty$: $A_{\text{routing}} \sim \frac{4}{9\pi} N^2$, 36.3% less compared to Manhattan placement and routing.

This simple analysis shows that the wirelength reduction caused by the "virtuous cycle" effect is significant, and at least partly explains the large wirelength reductions reported in [8] and [14].

4. CONCLUSION

In this paper, we have studied the wirelength reduction expected from λ-geometry placement and routing. We have improved existing estimates for the wirelength reduction of various interconnect architectures by taking into account the effect of Manhattan-driven placement on pin locations for nets with $k = 2$, 3 and 4 pins. We have estimated the wirelength improvement achieved by λ-geometry placement and routing versus Manhattan placement and routing, using a simulated annealing placer driven by λ-geometry metrics. We have also discussed and analyzed the "virtuous cycle" effect on overall wirelength.

Many questions on the estimation of wirelength improvement achieved by λ-geometry routing remain open. For example, the interaction between nets needs to be modeled to get an accurate estimation of the overall wirelength reduction. Similarly, detailed site maps and detailed routing need

to be considered to determine the actual effect of the "virtuous cycle". Finding efficient optimizers and estimators of λ-geometry wirelength is another interesting open problem.

5. REFERENCES

[1] H. Chen, B. Yao, F. Zhou, and C. K. Cheng. The Y-Architecture: Yet Another On-Chip Interconnect Solution. *Proc. ASPDAC*, 2003, pp. 840-846.

[2] M. Hayase and S. Meki. An Algorithm for Steiner Trees in λ-Geometry. *IPSJ Journal* 38(4).

[3] A. B. Kahng, I. I. Măndoiu, and A. Z. Zelikovsky. Highly Scalable Algorithms for Rectilinear and Octilinear Steiner Trees. *Proc. ASPDAC*, 2003, pp. 827-833.

[4] C. K. Koh and P. H. Madden. Non-Manhattan Routing. *IEEE Transactions Computer-Aided Design*, to appear.

[5] P. H. Madden. Congestion Reduction in Traditional and New Routing Architectures. To appear.

[6] T. Hildebrandt. An Annotated Placement Bibliography. *ACM SIGDA Newsletter*, Dec. 1985, pp. 12-21.

[7] Carl Sechen. Placement and Global Routing of Integrated Circuits Using Simulated Annealing. Ph.D. Dissertation, U. of California, Berkeley, 1987, Chapter 2.

[8] M. Igarashi, T. Mitsuhashi, A. Lee, et al. A Diagonal-Interconnect Architecture and Its Application to RISC Core Design. *Proc. ISSCC*, 2002.

[9] R. Scepanovic et al. Microelectronic Integrated Circuit Structure and Method Using Three Directional Interconnect Routing Based on Hexagonal Geometry. *U.S. Patent*, No. US5578840, Nov. 1996.

[10] D. Stroobandt. A Priori Wire Length Estimates for Digital Design. Kluwer Academic Publishers, 2001, Chapter 3.

[11] D. Stroobandt and F. J. Kurdahi. On the Characterization of Multi-Point Nets in Electronic Designs. *Proc. 8th Great Lakes Symp. on VLSI*, 1998, pp. 344-350.

[12] B. K. Nielsen, P. Winter, and M. Zachariasen. An Exact Algorithm for the Uniformly-Oriented Steiner Tree Problem. *Proc. 10th European Symp. on Algorithms*, Springer LNCS Vol. 2461, 2002, pp. 760-772.

[13] S. Teig, and J. L. Ganley. Method and Apparatus for Considering Diagonal Wiring in Placement. *International Application*, No. WO 02/47165 A2, June 2002.

[14] S. Teig. The X Architecture. *Proc. ACM/IEEE Workshop on System Level Interconnect Prediction*, 2002, pp. 33-37.

[15] http://www.xinitiative.org

[16] M. C. Yildiz and P. H. Madden. Preferred Direction Steiner Trees. *IEEE Transactions Computer-Aided Design*, to appear.

[17] K. Shin. HARTS: A Distributed Real-Time Architecture. *IEEE Computer* 24(5), May 1991.

APPENDIX

A. EXPECTED λ-GEOMETRY LENGTH OF A 2-PIN NET

We assume a placer driven by λ-geometry metrics optimizes only interconnect wirelength for 2-pin nets. Suppose there is a 2-pin net between two components A and B. Given a location for A and a unit interconnect length, B will be placed uniformly on the "λ-geometry unit circle" centered at A.

A.1 Preliminaries

The minimal λ-geometry length from $(0,0)$ to a point (x, y), $x, y \geq 0$, is:

$\lambda = 2$: $x + y$

$\lambda = 3$: $x + \frac{1}{\sqrt{3}}y$ when $y/x \in [0, \sqrt{3}]$ and $\frac{2}{\sqrt{3}}y$ when $y/x \in [\sqrt{3}, \infty]$

$\lambda = 4$: $x + (\sqrt{2} - 1)y$ when $y/x \in [0, 1]$ and $y + (\sqrt{2} - 1)x$ when $y/x \in [1, \infty]$

$\lambda = \infty$: $\sqrt{x^2 + y^2}$

A.2 Manhattan-Driven Placement

B is assumed to be placed uniformly on the rectilinear unit circle centered at A, whose intersection with the first quadrant is given by $y = 1 - x$, $0 \leq x \leq 1$. Then the expected λ-geometry length of the 2-pin net between A and B is:

$\lambda = 2$: 1

$\lambda = 3$: $\int_0^{\frac{1}{1+\frac{1}{\sqrt{3}}}} (1 - y + \frac{y}{\sqrt{3}})dy + \int_{\frac{1}{1+\frac{1}{\sqrt{3}}}}^{1} \frac{2y}{\sqrt{3}}dy = \frac{9+\sqrt{3}}{12} \approx 0.89434$

$\lambda = 4$: $2\int_0^{\frac{1}{2}}(1 - y + (\sqrt{2} - 1)y)dy = \frac{2+\sqrt{2}}{4} \approx 0.85355$

$\lambda = \infty$: $\int_0^1 \sqrt{(1-y)^2 + y^2}dy = \frac{1}{2} - \frac{1}{4}\sqrt{2}\ln\left(\sqrt{2} - 1\right) \approx 0.81161$

A.3 3-Geometry-Driven Placement

B is assumed to be placed uniformly on the hexagonal unit circle centered at A, whose intersection with the first quadrant is given by $y = \sqrt{3}/2$ for $0 \leq x \leq 1/2$ and by $y = -\sqrt{3}(x - 1)$ for $1/2 \leq x \leq 1$ Then the expected λ-geometry length of the 2-pin net between A and B is:

$\lambda = 2$: $\frac{2}{3}2\int_{\frac{1}{2}}^{1}(x - \sqrt{3}(x-1))dx + \frac{1}{3}2\int_0^{\frac{1}{2}}(x + \frac{\sqrt{3}}{2})dx = \frac{7+4\sqrt{3}}{12} \approx 1.1607$

$\lambda = 3$: 1

$\lambda = 4$: $\frac{2}{3}2\int_{\frac{1}{2}}^{\frac{1}{1+\frac{1}{\sqrt{3}}}}(-\sqrt{3}(x-1) - x + \sqrt{3}x)dx + \frac{2}{3}2\int_{\frac{1}{1+\frac{1}{\sqrt{3}}}}^{1}(x - (-\sqrt{3}(x-1)) + \sqrt{3}(-\sqrt{3}(x-1)))dx + \frac{1}{3}2\int_0^{\frac{1}{2}}(\frac{\sqrt{3}}{2} - x + \sqrt{3}x)dx = \frac{23\sqrt{3}-27}{12} \approx 1.0698$

$\lambda = \infty$: $2\int_0^{\frac{1}{2}}\sqrt{x^2 + (\frac{\sqrt{3}}{2})^2}dx = \frac{1}{2} + \frac{3}{8}\ln 3 \approx 0.91198$

A.4   4-Geometry-Driven Placement

B is assumed to be placed uniformly on the octilinear unit circle centered at A, whose intersection with the first quadrant is given by $y = 1 - (\sqrt{2} - 1)x$ for $0 \le x \le \sqrt{2}/2$ and by $x = 1 - (\sqrt{2} - 1)y$ for $\sqrt{2}/2 \le x \le 1$. Then the expected λ-geometry length of the 2-pin net between A and B is:

$\lambda = 2$: $\sqrt{2} \int\limits_{0}^{\frac{\sqrt{2}}{2}} (1 + (2 - \sqrt{2})y)dy = \frac{\sqrt{2}+1}{2} \approx 1.2071$

$\lambda = 3$: $\frac{1}{2}\sqrt{2} \int\limits_{0}^{\frac{1}{\sqrt{2}+\sqrt{3}-1}} \frac{2\sqrt{3}}{3}(1-(\sqrt{2}-1)x)dx + \frac{1}{2}\sqrt{2} \int\limits_{\frac{1}{\sqrt{2}+\sqrt{3}-1}}^{\frac{\sqrt{2}}{2}} (x +$

$\frac{\sqrt{3}}{3}(1-(\sqrt{2}-1)x))dx + \frac{1}{2}\sqrt{2} \int\limits_{0}^{\frac{\sqrt{2}}{2}} (1-(\sqrt{2}-1)y + \frac{\sqrt{3}}{3}y)dy \approx$
1.0471

$\lambda = 4$: 1

$\lambda = \infty$: $\sqrt{2} \int\limits_{0}^{\frac{\sqrt{2}}{2}} \sqrt{x^2 + (1 - (\sqrt{2} - 1)x)^2}\,dx \approx 0.94966$

A.5   Euclidean-Driven Placement

B is assumed to be placed uniformly on the Euclidean unit circle centered at A, whose points are given by $x = \cos\theta$ and $y = \sin\theta$. Then the expected λ-geometry length of the 2-pin net between A and B is:

$\lambda = 2$: $\frac{4}{\pi} \int\limits_{0}^{\frac{\pi}{4}} (\cos\theta + \sin\theta)d\theta = \frac{4}{\pi} \approx 1.2732$

$\lambda = 3$: $\frac{2}{3}\frac{3}{\pi} \int\limits_{0}^{\frac{\pi}{3}} (\cos\theta + \frac{\sqrt{3}}{3}\sin\theta)d\theta + \frac{1}{3}\frac{6}{\pi} \int\limits_{\frac{\pi}{3}}^{\frac{\pi}{2}} \frac{2\sqrt{3}}{3}\sin\theta d\theta = \frac{2}{\pi}\sqrt{3} \approx$
1.1027

$\lambda = 4$: $\frac{4}{\pi} \int\limits_{0}^{\frac{\pi}{4}} (\cos\theta - \sin\theta + \sqrt{2}\sin\theta)d\theta = \frac{8}{\pi}\left(\sqrt{2} - 1\right) \approx 1.0548$

$\lambda = \infty$: 1