Homework 4

CSE 232

May 2021

Design a 6 bit register for *load*, *swap*, *clear* using the control inputs (ld, sw, cl) to swap the 6 bits data inputs I5 I4 I3 I2 I1 I0 and result the data outputs Q5Q4Q3Q2Q1. The load input will load the data to register, the clear input will load 0 to the register and the swap function *swap* the consecutive bits. For example, after running the swap function, the abcdef will become badefe. The bits at location 5 and 6 are swapped, the bits at 4 and 3 are swapped, the bits at 2 and 1 locations are swapped.

(The priority rank is clear, load, swap)

Make your design following the steps below

1- Define MUX size
2- Create MUX table
3- Connect MUX input
4- Map control lines

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Step 1: Defining Mux Size

load + swap + clear + present value
ld sw cl pv

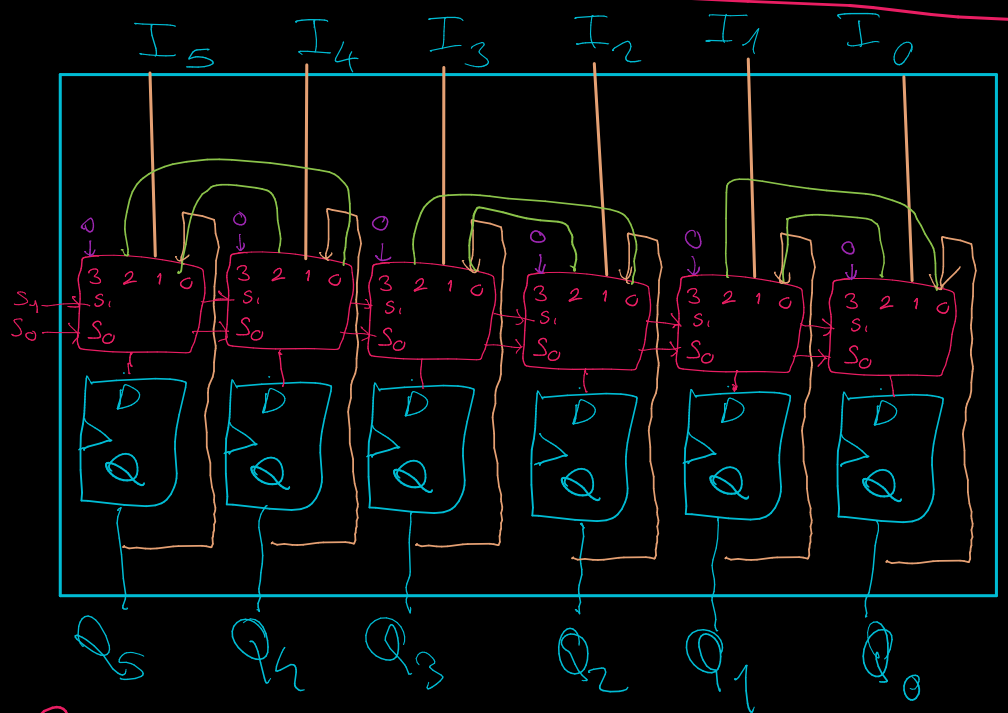
= 4 operations

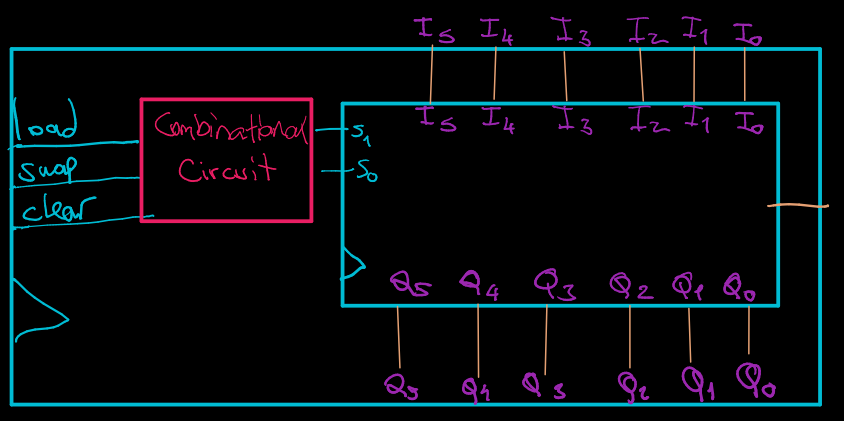
↳ So 4 x 1 Mux

Step 2: Create MUX Operation Table

	S_1	S_0	Operation
0	0	0	Maintain Present Value
1	0	1	Load
2	1	0	Swap
3	1	1	Clear

Step 3: Connect Mux Inputs





Step 4: Map Control Lines

Inputs			Outputs		Operation
cl	ld	sw	S_1	S_0	
0	0	0	0	0	Maintain Present Value
0	0	1	1	0	Swap Values
0	1	X	0	1	Load Values
1	X	X	1	1	Clear All Values

$S_1 = sw(cl)'.(ld)' + cl$

$S_0 = (cl)'.ld + cl$