

Homework 3

CSE 232

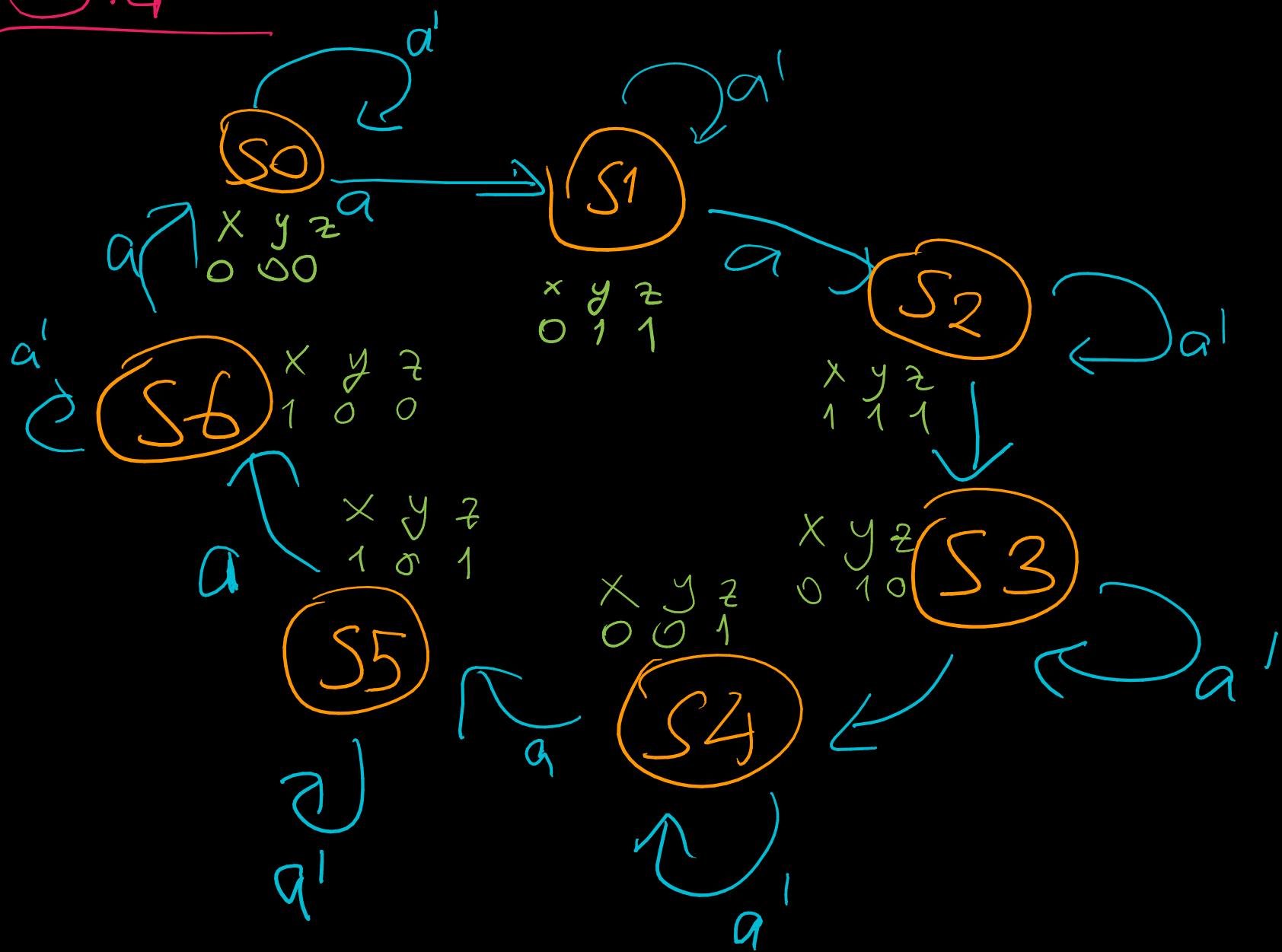
May 2021

Draw a state diagram for an FSM with an input a and three outputs, x, y and z. The xyz outputs generate a sequence in order 000, 011, 111, 010, 001, 101, 100, repeat. The output should change only on a rising clock edge when the input a = 1. Make the initial state 000. Design your solution in five steps

- Step 1: Create FSM
- Step 2: Obtain architecture
- Step 3: Encode states
- Step 4: Generate state table
- Step 5: Obtain Boolean expressions and draw controller

(Hint, at Step 5, you may use K-maps for simplifications)

Step 1



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$S_0 = 000$
$S_1 = 011$
$S_2 = 111$
$S_3 = 010$
$S_4 = 001$
$S_5 = 101$
$S_6 = 110$

Step 2

Total 7 states ($7 < 2^3$)

$S_0 \rightarrow 3 \text{ bits}$

for next state

(n_2, n_1, n_0)

a is input)

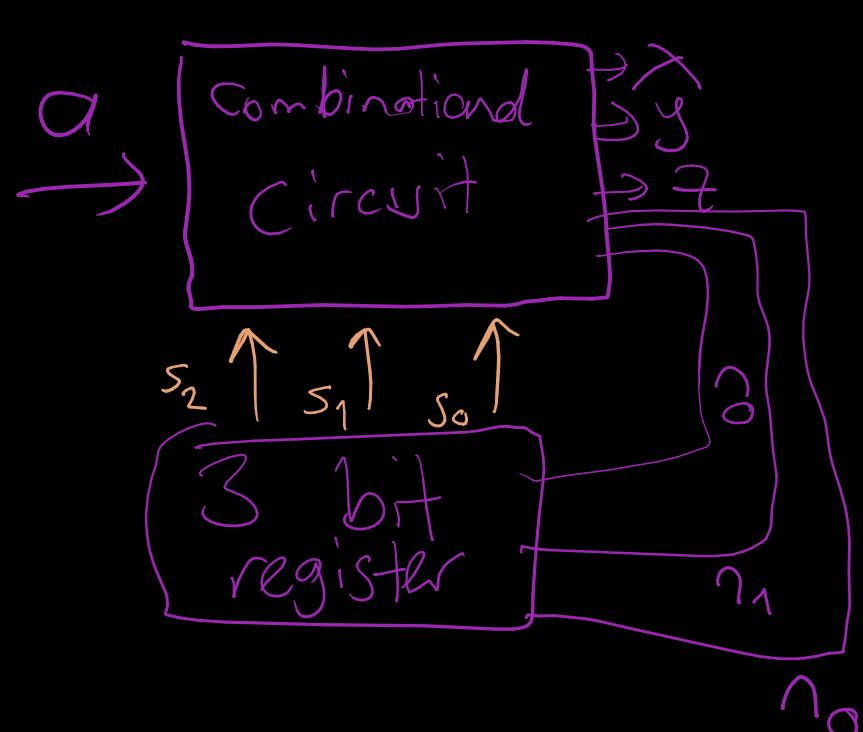
for output
 (x, y, z)

Step 3

Encode States

Wait :

	S_2	S_1	S_0
	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0



Step 4

Create Staff table

Step 5.1

Obtain Boolean Expression

		S0					
		S1					
		S2					
N2	S0,A	.00	10	11	10		
S2,S1		00	0	0	0		
0 0		0	0	0	0		
0 1		0	0	1	0		
1 1		1	0	0	0		
1 0		1	1	1	1		

$$\cap_2 = S_2 S_1' + S_2 S_0' A' + S_2' S_1 S_0 A$$

		S0					
		S1					
		S2					
N1	S0,A	.00	10	11	10		
S2,S1		00	0	1	0		
0 0		0	0	1	0		
0 1		1	1	0	1		
1 1		1	0	0	0		
1 0		0	0	1	0		

$$\cap_1 = S_1' S_0 A + S_2' S_1 S_0' + S_2' S_1 A' + S_1 S_0' A'$$

		S0					
		S1					
		S2					
N0	S0,A	.00	10	11	10		
S2,S1		00	1	0	1		
0 0		0	1	0	1		
0 1		0	1	0	1		
1 1		0	0	0	0		
1 0		0	1	0	1		

$$\cap_0 = S_2' S_0' A + S_1 S_0' A + S_2' S_0 A' + S_1' S_0 A'$$

		S0					
		S1					
		S2					
X	S0,A	.00	10	11	10		
S2,S1		00	0	0	0		
0 0		0	0	1	0		
0 1		1	1	0	0		
1 1		1	1	0	0		
1 0		0	0	1	1		

$$X = S_1 S_0' + S_2 S_1' S_0$$

		S0					
		S1					
		S2					
Y	S0,A	.00	10	11	10		
S2,S1		00	0	1	1		
0 0		0	0	1	1		
0 1		1	1	1	1		
1 1		0	0	0	0		
1 0		0	0	0	0		

$$Y = S_2' S_1 + S_2' S_0$$

		S0					
		S1					
		S2					
Z	S0,A	.00	10	11	10		
S2,S1		00	0	1	1		
0 0		0	0	1	0		
0 1		1	1	0	0		
1 1		0	0	0	0		
1 0		1	1	1	1		

$$Z = S_2 S_1' + S_1' S_0 + S_2' S_1 S_0'$$

Step 5.2

