

CSE 331/503

Computer Organization

Bonus Homework (8%) – Cypher Detector

Due Date 09/01/2023 Monday 23:59

In this assignment you will design cypher detector to be used for security. It will detect a particular number sequence incoming from an input.

Use **Quartus** and **Verilog** HDL. Implement Control Unit and Datapath. Control Unit will be designed as 3 always blocks similar to we did in last lecture.

Your design will get a 16-bit number showing the cypher. For instance if the cypher is 1-2-3-4 then the 16-bit input will be 0100 0011 0010 0001. **cypher'in tersi inputta olacak. Öyle olunca durdur ve toplamı return et**

The second input is 4-bit from where you will read numbers sequentially.

Third input will be the read input, which will be made 1 when the 4-bit input is ready. If read input is 0 you will not read the 4-bit number as it is not ready. Read each 4-bit number only at the positive edge of the read input.

The last inputs are reset and clock signals.

The first output of your design will be 1-bit signal, which becomes 1 only after the right cypher numbers are collected.

The second output will be 8-bits and will show the sum of all numbers until the right cypher is detected.

(See the example at the end)

1. Design your FSM on paper.
2. Design your datapath on paper.
3. Design your datapath on Verilog
4. Design your control unit on Verilog.
5. Write down the Verilog testbench.
6. Simulate and verify your design.

Report:

Your report will include the results of the 6 tasks above. It will be a zip file named with your name and student id like "Ahmet_Caliskan_123456789.zip".

Your TA may request a Demo for the project.

Designs without any FSM will get 0.

Designs not simulating correctly will get 0.

This is a bonus project. There is no partial credit.

An Example Case:

Cypher: 0010 0110 0000 0001 (Cypher is 2-6-0-1)

4-bit inputs: 0000-0001-0011-0000-0011-0100-0001-0000-0010-0001-0001-0000-0110-0010

The first output will become 1 after the last four numbers are observed.

The second output will be 24, i.e. 0001 1000.

“The punishment of desire is the agony of unfulfillment”