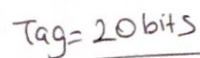


We have a **4-way set associative cache** with **data block size of 128 bytes**. The **physical address width is 34 bits**. For each block there is a **valid** bit and a **dirty** bit. The width of the **index field is 7 bits**.

- Address



c. What is the data size of the cache in KB?

$$\underbrace{2^7}_{\text{index size}} \times \underbrace{4}_{\text{\# of assoc.}} \times \underbrace{2^7}_{\text{block size}} \text{ bytes} = 2^{16} \text{ bytes} = 2^{10} \times 2^6 \text{ bytes} = \underline{64 \text{ KB}}$$

d. What is the total size of the cache in KB?

$$\begin{aligned} (20 + 1 + 1 + 8 \times \underbrace{128}_{\substack{\text{1 byte} \\ \text{= 8 bits}}}) \times \underbrace{4}_{\substack{\text{\# of} \\ \text{assoc.}}} \times 2^7 &= (22 + 1024) \times 2^9 \text{ bits} \\ &= 535552 \text{ bits} / 8 \\ &= 66944 \text{ bytes} / 1024 \\ &= \underline{65.375 \text{ KB}} \end{aligned}$$

e. Compute **average memory access time** considering all costs **including the time required for address translation** by the help of the below table. Show your computations clearly.

Operation	Time required
L1 cache hit time	3ns
L1 cache hit rate	90%
L2 cache hit time	25ns
L2 cache hit rate	80%
Main memory hit time	500ns
Page fault rate	0.2%
Disk access time	30,000ns
TLB hit time	2ns
TLB hit rate	95%
Page table access time	300ns

AMAT

$$\begin{aligned} \text{AMAT} &= 3 + 0.1 \times \left(25 + 0.2 \times (500 + 0.02 \times 30000) \right) + \underbrace{2 + 0.05 \times 300}_{\text{address translation}} \\ &= \underline{\underline{44.5 \text{ ns}}} \end{aligned}$$