ORTEC®

INSTRUCTION MANUAL
MODEL 416
GATE AND DELAY GENERATOR

Serial No. ______________________________

Purchaser ______________________________

Date Issued ______________________________

ORTEC INCORPORATED

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STANDARD WARRANTY FOR ORTEC ELECTRONIC INSTRUMENTS

DAMAGE IN TRANSIT

Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, notify ORTEC of the circumstances so that we may assist in damage claims and in providing replacement equipment when necessary.

WARRANTY

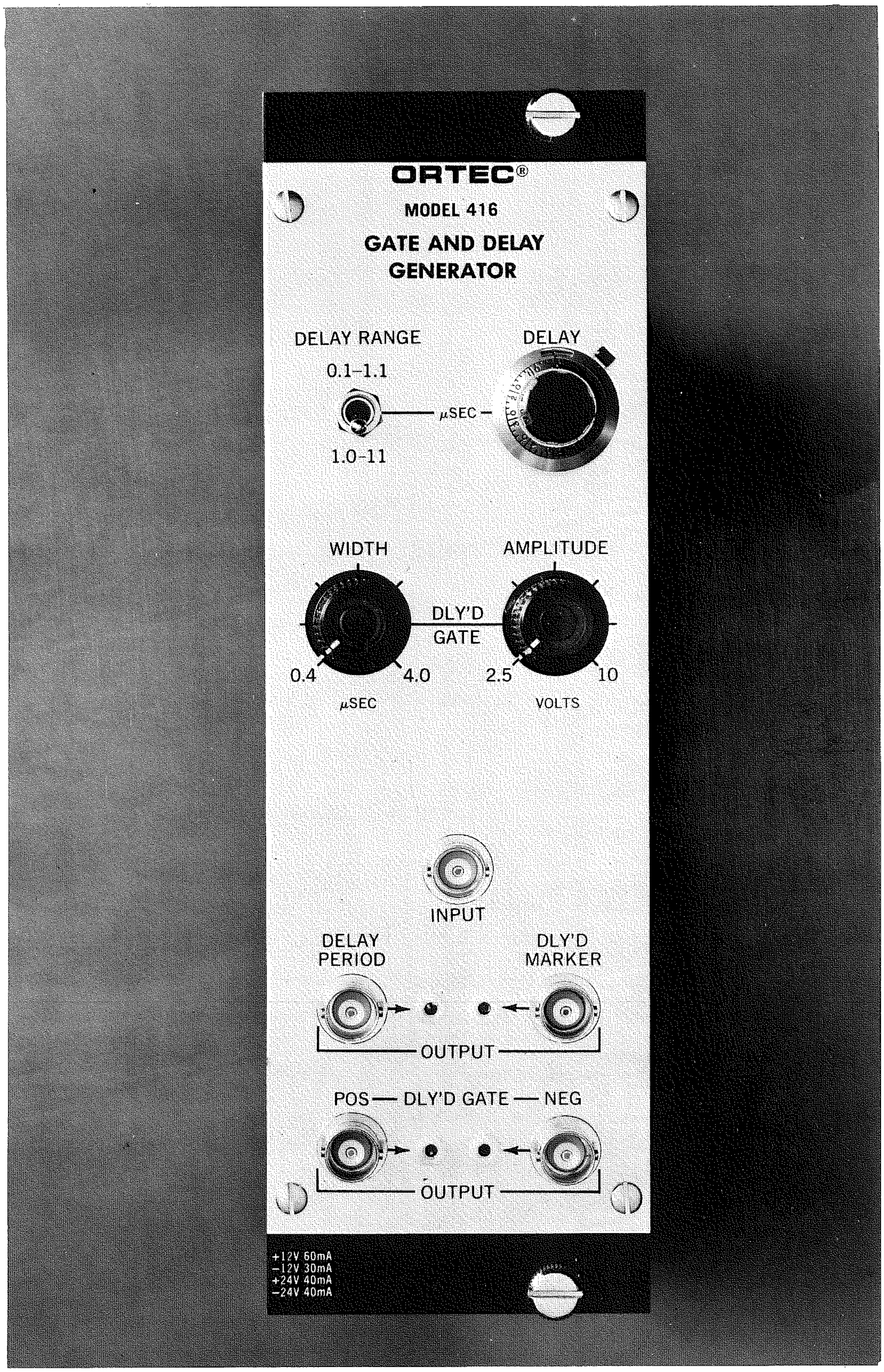
ORTEC warrants its electronic products to be free from defects in workmanship and materials, other than vacuum tubes and semiconductors, for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner and not subjected to abuse. Repairs or replacement, at ORTEC option, will be made without charge at the ORTEC factory. Shipping expense will be to the account of the customer except in cases of defects discovered upon initial operation. Warranties of vacuum tubes and semiconductors, as made by their manufacturers, will be extended to our customers only to the extent of the manufacturers' liability to ORTEC. Specially selected vacuum tubes or semiconductors cannot be warranted. ORTEC reserves the right to modify the design of its products without incurring responsibility for modification of previously manufactured units. Since installation conditions are beyond our control, ORTEC does not assume any risks or liabilities associated with the methods of installation, or installation results.

QUALITY CONTROL

Before being approved for shipment, each ORTEC instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

REPAIR SERVICE

ORTEC instruments not in warranty may be returned to the factory for repairs or checkout at modest expense to the customer. Standard procedure requires that returned instruments pass the same quality control tests as those used for new production instruments. Please contact the factory for instructions before shipping equipment.


ORTEC®
MODEL 416
GATE AND DELAY
GENERATOR
DELAY RANGE
0.1–1.1
μSEC
1.0–11
DELAY
WIDTH
AMPLITUDE
DLY'D
GATE
0.4
4.0
μSEC
2.5
10
VOLTS
INPUT
DELAY
PERIOD
DLY'D
MARKER
OUTPUT
POS — DLY'D GATE — NEG
OUTPUT
+12V 60mA
−12V 30mA
+24V 40mA
−24V 40mA

ORTEC 416

GATE AND DELAY GENERATOR

1. DESCRIPTION

The 416 Gate and Delay Generator is one in a series of modular instruments complying with the AEC Nuclear Instrument Module Standards. This module is designed to provide the interface functions for logic pulses between the logic pulse generation and its end use. These necessary functions are: variable delay, variable pulse amplitude, variable pulse width, and a selection of output polarity. The uses for the unit will include such applications as analyzer gating and coincidence trigger circuits, and others. Due to its unique design, it also provides timing signals which are suitable for driving time to pulse height converters or coincidence circuits in delayed coincidence applications such as pulse shape discrimination, etc.

2. SPECIFICATIONS

Delay Ranges	0.1 μsec to 1.1 μsec 1.0 μsec to 11 μsec
Delay Adjustment	Continuously variable within the selected range by means of a 10-turn potentiometer
Delay Readout	Direct reading via a 10-turn dial
Delay Linearity	±2%
Delay Temperature Stability	≤0.03% of selected range
Delay Generator Dead Time	Delay + 0.1 range
Gate Generator Dead Time	Gate pulse width + 0.2 μsec
Count Rate	1/dead time
Delay Jitter	≤0.02% of range at average dead time <20%
Input	Pos., 2V min., protected to ±100V max., dc-coupled, non-critical to rise time, 25 nsec minimum width
Input Impedance	≥1K ohm
Output Impedance	Less than 10 ohms for all outputs
Delay Period	T_r ≤50 nsec, positive, 4V, width equal to delay time
Delay Marker	T_r ≤10 nsec, negative, 0.6V, width ≤25 nsec
Delayed Gate	Positive and negative simultaneously; amplitude variable 2.5V to 10V, width variable 0.4 μsec to 4 μsec; T_r ≤100 nsec
Power Requirements	+24V at 45 mA, -24V at 35 mA, +12V at 85 mA, and -12V at 50 mA; furnished by 401A/402A

3. INSTALLATION INSTRUCTIONS

3.1 General

The ORTEC 416, used in conjunction with the ORTEC 401A/402A Bin and Power Supply, is intended for rack mounting, and therefore it is necessary to ensure that vacuum tube equipment operating in the same rack has sufficient cooling air circulating to prevent any localized heating of the all-transistor circuitry used throughout the 416. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are taken. The 416 should not be subjected to temperatures in excess of 120°F (50°C).

3.2 Connection to Power — AEC Standard Nuclear Instrument Module, ORTEC 401A/402A

The 416 contains no internal power supply, and therefore must obtain power from a Nuclear Standard Bin and Power Supply such as the 401A/402A. It is recommended that the Bin power supply be turned off when inserting or removing modules. The ORTEC 400 Series is designed so that it is not possible to overload the Bin power supply with a full complement of modules in the Bin; however, this may not be true when the Bin contains modules other than those of ORTEC design. In this case, power supply voltages should be checked after the insertion of modules. The 401A/402A has test points on the power supply control panel to monitor the dc voltages.

4. OPERATING INSTRUCTIONS

The operation of the 416 should be very simple and straightforward. Once it is plugged in and the power turned on, it is necessary only to furnish a trigger pulse of sufficient amplitude to trigger it, select the desired range of delay, then dial in the approximate delay wanted, and connect the desired output to the input of the circuit that it is to drive. For instance, if one wishes to gate an analyzer which requires an 0.8-microsecond delay and a negative 4-volt signal 2 microseconds wide, connect the negative delayed output to the gating input to the analyzer, set the delay range to the 0.1 μsec to 1.0 μsec position, and dial the delay potentiometer to 800 on the 10-turn dial. Set the width potentiometer, R28, at approximately midrange and the amplitude potentiometer, R24, at approximately one-third range. Of course, to set the width and amplitude precisely one must view these with an oscilloscope. Also, the real time delay is not meant to be correlated closely enough with the dial reading to be believed better than ±5 percent; however, the reproducibility of the delay should be very good. Therefore, if one wishes to plot the delay function versus dial reading, he should be able to determine his delay precisely at any time thereafter. In almost all instances, care should be taken to see that the connecting cables used are terminated in their characteristic impedances. In the case of the DELAYED GATE output, this is not quite so critical as it is in the case of the DELAY PERIOD and the DELAYED MARKER; however, if pulse fidelity is a requirement, this precaution should be observed also on the DELAYED GATE outputs.

5. CIRCUIT DESCRIPTION

Diodes D6 and D7 form a current limiting protection circuit to protect against large amplitude signals. Q13, Q14, and Q15 form a dc-coupled Schmitt trigger which has fast rise-time and a width equal to the width of the input signal. The current pulse at the collector of Q14 is differentiated by L2. D1, in turn, clips the negative portion of the differentiated pulse and passes the positive portion to the base of Q1. The positive portion of the pulse triggers the delay multivibrator, which is composed of Q1, Q2, Q3, and Q4. When triggered, this multivibrator sets a voltage step onto a capacitor, either C4 or C5, and then this capacitor is discharged with a constant current which is furnished by way of Q4 and is controlled by the delay potentiometer, R11. Since it is a constant current discharge, the delay will be linear. Diode D2 provides the dc bias necessary to hold Q2 in the conduction state until the multivibrator is triggered, at which time the voltage pulse from the emitter of Q3 is fed over to cut off the diode. It will remain off until the multivibrator recovers. D3 provides a dc restoration for the capacity coupling by C3 of the output pulse from the delay multivibrator. This output pulse is emitter-follower buffered through Q5 and is called the DELAY PERIOD output. The DELAY PERIOD output pulse is differentiated by means of L1, and the differentiated pulse is fed to the base of Q6, which is normally off emitter follower, but the negative portion which occurs at the trailing edge of the DELAY PERIOD pulse will be fed out as a DELAY MARKER pulse. When Q6 conducts, it furnishes the DELAY MARKER pulse at the output and an inversion of the DELAY MARKER pulse at its collector which is ac-coupled to the base of Q7. This pulse triggers the gate pulse generator composed of Q7, Q8, and Q9. When the gate pulse generator is triggered, the constant current that is flowing through Q8 will be switched through Q7, and an output pulse which is the constant current multiplied by the sum of R25 and the amplitude control, R24, will be fed to the base of Q10, and is the generation of the gate pulse. Again, D5 forms a dc restoration for the capacity coupling of C12. Q10 is a phase splitter which forms two pulses of equal amplitude but opposite polarity. The positive pulse is fed to the base of Q11 and the negative to the base of Q12. Q11 and Q12 are an NPN and PNP pair that are both in the cut-off state until the gate pulse arrives, at which time they turn on for the period of the gate pulse and present an output at their respective output connectors. The gate pulse width is controlled by the RC combination composed of C11 and the series resistance, R29 and R28. R28 is the GATE WIDTH control.

6. MAINTENANCE INSTRUCTIONS

6.1 Testing Performance

To test the operation of this unit, first test the operation of the delay multivibrator section. To do this, merely insert an input trigger pulse and check for an output from the DELAY PERIOD output. Monitor the width of the DELAY PERIOD output, vary the delay potentiometer, R11, through its range, and also check the operation of the RANGE SELECTOR switch, S1. Of course, this pulse width should be equal to the desired delay time except for a small propagation delay of about 25 nanoseconds. With the trigger present, if there is no DELAY PERIOD output, the trouble is immediately isolated to the delay multivibrator. Usually the first test to perform is that of measuring dc voltages and comparing them with the voltages given in Table 1. If this does not isolate the trouble, then one must resort to the use of an oscilloscope and waveform checks. Sufficient waveforms for comparison are given on the schematic diagram, drawing number 416-001-S1, in the back of the manual. If the DELAY PERIOD output pulse is present, check for an output from the DELAYED MARKER output BNC. If the DELAYED MARKER output does not exist, then the problem is immediately isolated to the circuit surrounding Q6. If a DELAYED MARKER output exists but there is no gate pulse output, this of course indicates that the gate multivibrator is not being correctly triggered. Again, the best test is a dc voltage measurement test and comparison against the tabulated voltages.

6.2 Calibration Adjustments

There are no calibration adjustments in the Gate and Delay Generator itself; only the adjustments which are available at the front panel are variable.

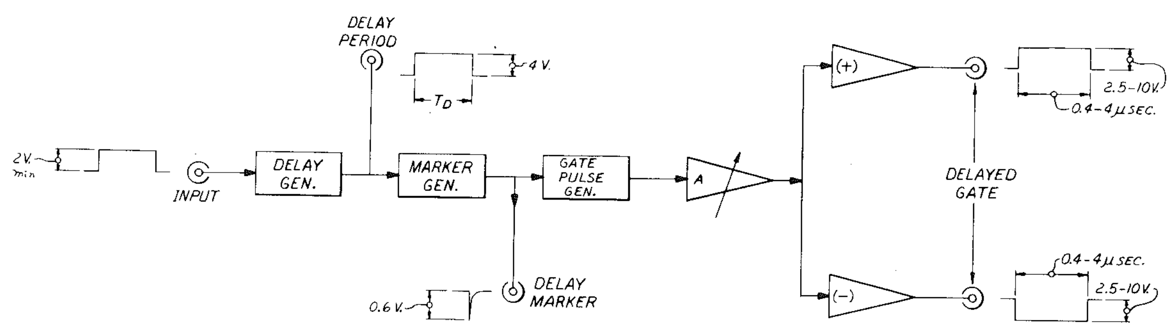


Figure 1. Gate and Delay Generator - Block Diagram

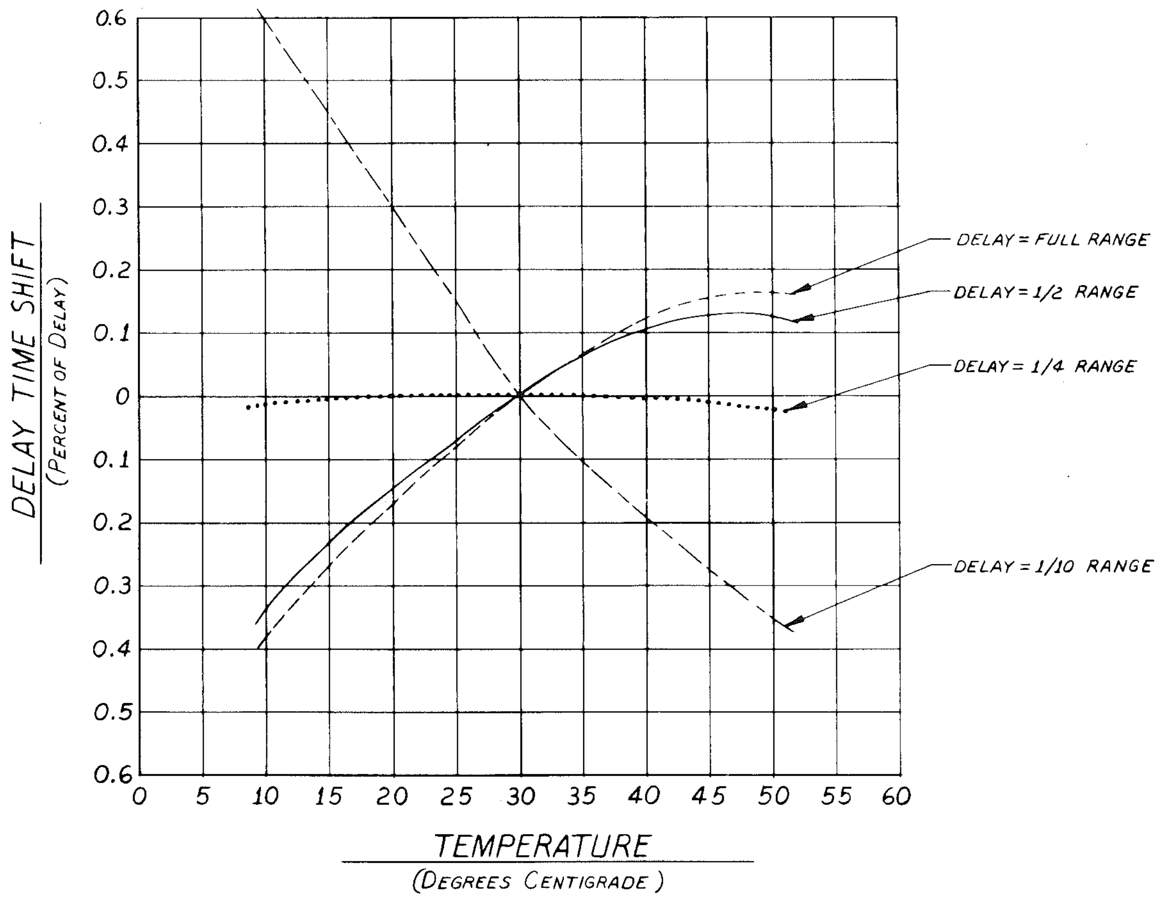


Figure 2. Delay Stability Versus Temperature Curves

Table 1. DC Voltage Measurements

Checkpoint	Average Values
+12 bus	+11.8
+24 bus	+23.8
-24 bus	-23.6
-12 bus	-11.7
Q2-B	+ 0.70
Q2-C	+ 5.0
Q3-B	+11.5
Q4-B	+21.5
Q5-B	- 0.60
Q6-C	-11.8
Q8-B	+ 0.60
Q8-C Amp Pot Min	+ 9.4
Q8-C Amp Pot Max	+ 0.50
Q9-E	+12.4
Q10-B	- 0.25
Q10-E	+ 0.50
*Q10-C	- 0.45
Q11-E	+ 0.1
Q12-E	- 0.1
Q13-B	+ 0.1
Q14-B	+ 1.8
Q15-E	+12.5

* R 33 to be selected, if necessary. Nominal 22 Ω

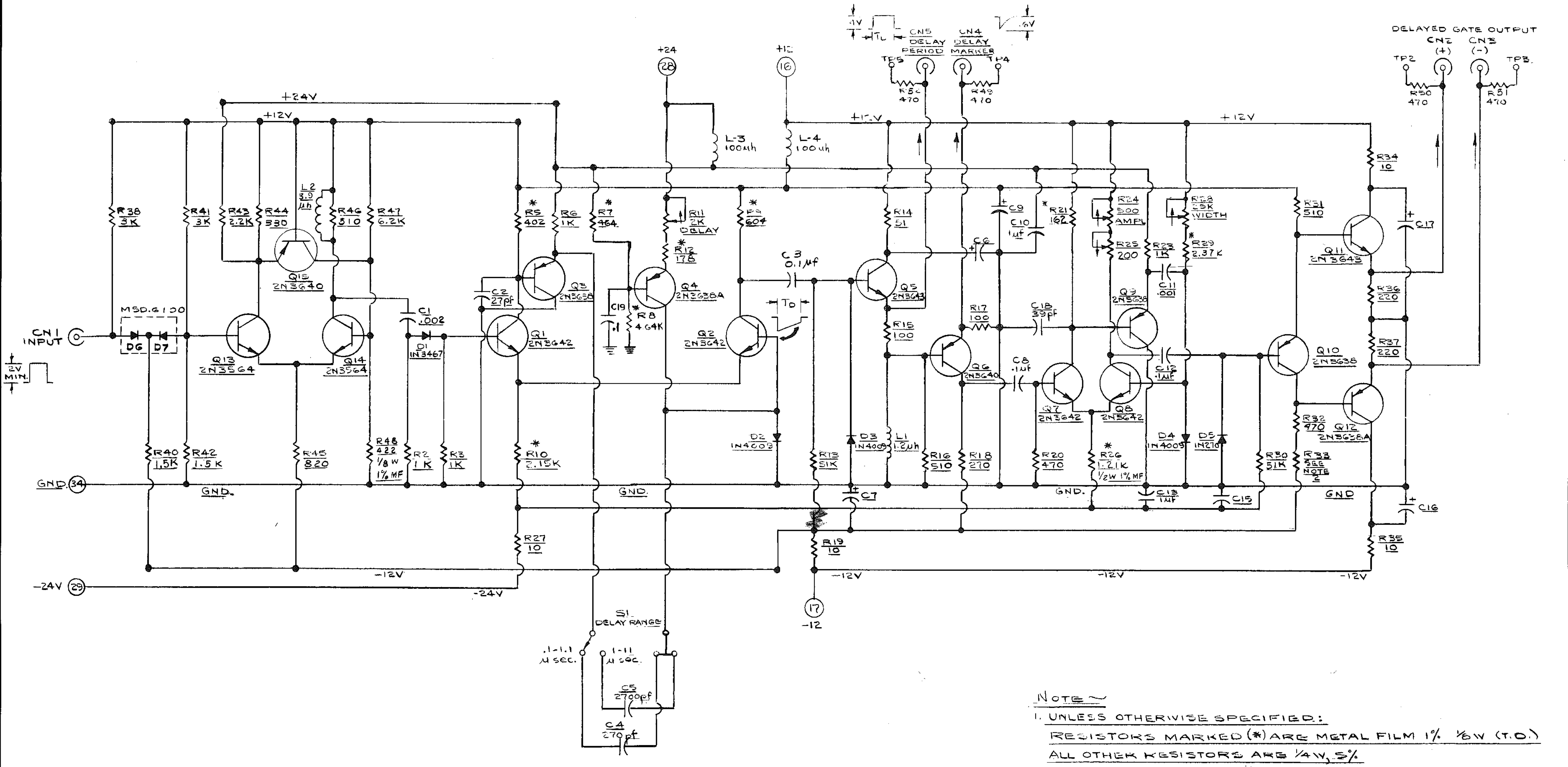
Note: All voltages are read with respect to ground with a vtvm, with no signal input, and with all front panel pots in the zero position.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	−3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	−24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	−6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground.
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	−12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

** These pins are installed and wired in parallel in the ORTEC 401A Modular System Bin.*

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



NOTE ~

1. UNLESS OTHERWISE SPECIFIED:

RESISTORS MARKED (*) ARE METAL FILM 1% 1/8W (T.O.)

ALL OTHER RESISTORS ARE 1/4W, 5%

CAPACITORS ARE 6.8 µf 35V TAN

2. R33 TO BE SELECTED ~ NORMALLY 22Ω.

REV.	ECN. NO.	DATE	BY	APPD.
M	416-16	3-8	JDW	
L	416-15	12-66	JDW	
K	416-13	11-66	JDW	
J	416-11	8-29	RLW	
I	416-10	7-27-66	JDW	
H	416-9	7-20-66	JDW	
G	416-8	7-1-66	JDW	
F	416-7	6-21-66	HW	

REVISIONS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES

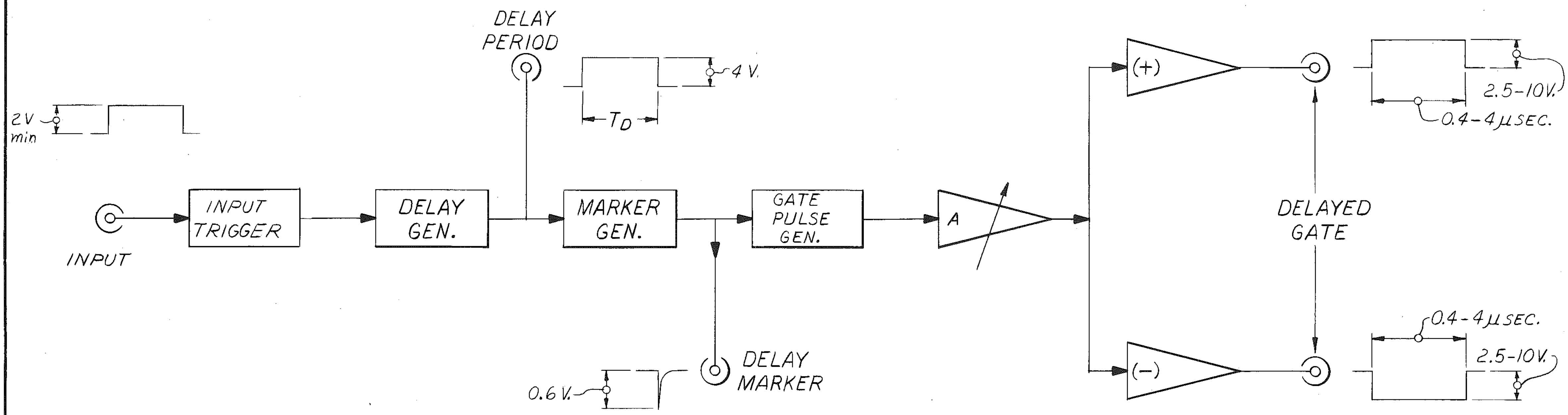
TOLERANCES
FRACTION ± ____
DECIMALS ± ____
ANGLES ± ____
SURFACE FINISH √ RMS
APPLIED PRACTICES

ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE

TITLE
GATE & DELAY GENERATOR

DRAFTSMAN HW DATE 6/22/66
ENG. APPROVAL C.W. Williams
RESP. ENG. C.W. WILLIAMS
CHECKED C.W. DATE 7/5/66
MFG. APPROVAL
DRAWING NO. 416-001-S1
SCALE —
DWG. ISSUED DATE 7-5-66

416-001-81



DATE	NO.	REVISION	BY
7-1-66	A	ECN # 416-7	DOUG

OAK RIDGE TECHNICAL ENTERPRISES CORP.
OAK RIDGE, TENN.

MODEL 416
GATE AND DELAY GENERATOR
BLOCK DIAGRAM

DESIGN	DRAWN	DATE	RESP. ENGR.	APPR.	SCALE	DRAWING NO.
[illegible]	E.C. Keith	7-10-65	[illegible]	[illegible]	~	416-001-81