MODEL 794 QUAD GATE/DELAY UNIT

FEATURES:

- Wide Range - Less than 100 nSec to over 10 Sec
- 'Set - Reset' Flip-Flop Mode
- No Deadtime
- Computer/Remote Programming via a 0 Volt to 10 Volt Input

GENERAL DESCRIPTION

The Quad Gate/Delay Generator, Model 794, complies fully with the NIM specification TID-20893 and is packaged in a single width module. In 'monostable mode', gate/delay periods may be adjusted either locally or remotely from less than 100 nSec to more than 10 seconds. Each channel also operates in a 'set-reset flip-flop' mode. A bright LED indicates an active, logic '1', gate condition. Versatile input and output structures provide compatibility with NIM, ECL, and TTL standards. Further flexibility is afforded by programming jumpers mounted on the printed circuit board. These jumpers allow selected inputs and outputs to be assigned alternate logic functions or polarities.

TIME-BASE DESCRIPTION

The model 794 time-base circuit is non-updating and exhibits essentially no deadtime. Monostable gate/delay periods are selected by a combination of the "RANGE" switch and a time vernier potentiometer or, by jumper option, the "RANGE" switch and an analog programming input. A monitor test point provides a 0 to 1 Volt output which is proportional to the gate/delay period. Setting the gate/delay period with an oscilloscope is easily accomplished by using the "TRIGGER" pushbutton. Depressing this switch for more than 0.5 seconds causes the time-base to retrigger at a 1 KHz rate. In the bistable mode, the gate/delay period is equal to the interval between the arrival of the trigger and reset functions. The "DELAY" output always occurs at the trailing edge of the "GATE" output. The "DELAY" output width may be adjusted by a front panel potentiometer.

INPUT DESCRIPTION

There are three ways to trigger the Model 794: (1) "TRIGGER" input; (2) "OR" input; and (3) "TRIGGER" pushbutton. These functions are enabled in both monostable and bi-stable modes.

The "TRIGGER" input is compatible with both TTL levels and negative NIM logic. This input presents a high impedance to positive signals and 50 ohms to negative signals. The time-base triggers on the leading edge of the input pulse regardless of its polarity. The gate period is independent of the "TRIGGER" pulse width.

"OR" is a negative NIM logic input which is configured with program jumpers. The "OR" input is always logically 'ORed' with the time-base output. Assuming a quiescent time-base, the "GATE" output width is equal to the "OR" input width. A program jumper enables the 'input OR' mode in which the "OR" input also triggers the time-base. 'Input OR' mode produces a "GATE" output equal to the width of the "OR" input or the preset time whichever is greater. An additional jumper allows "OR" to be a high impedance or 50 ohms. Note that the high impedance 'input OR' mode allows multiple channels or multiple modules to be triggered from a single output, i.e., high impedance pick-off.

The "TRIGGER" pushbutton offers two operating modes for manual triggering. 'Single trigger' mode is executed by pushing and releasing the switch in less than 0.5 seconds. This produces a single trigger pulse. 'Retrigger mode' is executed by pushing and holding the switch for more than 0.5 seconds.

INPUT DESCRIPTION (continued)

In the bistable mode the channel is triggered or 'set' and remains in that state until 'reset' by the negative NIM compatible "RESET" input or the "RESET" pushbutton. The "TRIGGER" and "OR" inputs are inhibited from 'setting' the channel when "RESET" is at logic '1'. The "RESET" I/P is enabled only in the bistable mode.

"INHIBIT" is a negative NIM compatible input. All outputs are forced to their quiescent state whenever "INHIBIT" is logic '1'. "GATE" transitions resulting from "INHIBIT" do not generate "DELAY" outputs.

A special feature of the Model 794 is the analog "PROGRAMMING" input. Enabled by program jumpers, each input accepts 0 to +10 Volt levels and produces a 5% to 105% adjustment of the selected range. The analog voltage is received differentially to relieve the noise and common mode offsets associated with long cable runs.

OUTPUT DESCRIPTION

Each channel has five (5) outputs. "GATE", "$\overline{\text{GATE}}$", and "DELAY" are negative NIM current source outputs governed by the trigger rules described above. "TTL" is a TTL compatible output which can be assigned to either the "GATE" or "DELAY" function. A second jumper associated with TTL provides a 'true' or 'complement' feature. "ECL" is a differential ECL output conforming to CERN note EP 79-01 and is jumper programmed to be identical to either "GATE" or "DELAY".

BIN GATE DESCRIPTION

The model 794 is capable of driving the 'bin gate' of the host bin. A switch mounted on the rear panel enables or disables the "BIN GATE" feature. Individual channels are selected to supply this gate signal via program jumpers. More than one channel may be selected resulting in a 'bin gate' which is the logical OR of the selected channels.

MANUAL CONTROL SUMMARY

Range Switch

A ten position rotary switch selects one of eight 'full scale' times for the 'monostable' mode. The remaining two positions are for 'bistable' mode. RANGE positions are: 1 µSec, 10 µSec, 0.1 mSec, 1 mSec, 10 mSec, 0.1 Sec, 10 Sec, FF and FF.

Trigger Pushbutton

Provides a manual 'trigger' function. 'Single trigger' mode is implemented by pressing and releasing in less than 0.5 seconds. 'Retrigger' mode is implemented pressing and holding for more than 0.5 seconds.

Reset Pushbutton

Provides a manual 'reset' function.

Time Vernier Potentiometer

Adjusts the monostable time-base form approximately 5.0% to 105.0% of the selected range in 'local' programming mode. The potentiometer is disable in 'remote' programming and 'bistable' modes.

Delay Width

Adjusts the width of the delay output from 10 nSec to 100 nSec.

Phillips Scientific 305 Island Road • Mahwah, New Jersey 07430 • USA • (201) 934-8015

INPUT CHARACTERISTICS

All input connections are made with LEMO connectors.

Negative NIM Inputs are 50 ohms, logic '0' = +/-1mA, LOGIC '1' = -14 to -18 mA.

"TRIGGER"	:	A high impedance for positive logic levels. Positive logic '0' less than 0.5 V, logic '1' less than 1.5 V. Negative NIM for negative logic levels.
"OR"	:	Negative NIM when jumpered as 50 ohm impedance. For high impedance, logic '0' = +/-50 mV, logic '1' = -0.7 to -0.9 V. "OR" is shipped as high impedance 'input OR'.
"INHIBIT"	:	Negative NIM input.
"RESET	:	Negative NIM input. Enabled only in 'bistable' mode.
"ANALOG PROGRAM"	:	A high impedance, differential, analog input. Maximum input voltage: Differential = 6 to +12 V Common Mode= ±6 V Recommended Input Voltage: Differential = 0 to +10.0 V Common Mode = ±0.5 V

OUTPUT CHARACTERISTICS

ECL is a two pin header, 0.025 in. posts on 0.1 in. centers. All other output connections are made with LEMO connectors.

Negative NIM Outputs are current source type, Logic '0' = 0 mA. typically. Logic '1' equals -16 mA. typically.

"GATE"	:	Negative NIM output.
"$\overline{\text{GATE}}$"	:	Negative NIM output. The complement of "GATE".
"DELAY"	:	Negative NIM output.
"TTL"	:	A TTL compatible output. Logic '1' = 2.7 V, min. @ 45 mA maximum, logic '0' = 0.5 V maximum @ -100 mA maximum. TTL is jumper selected to be "GATE", "DELAY", or their complements. TTL is shipped as "GATE".
"ECL"	:	A differential 100 ohm line driver. Logic '0' = -0.90, typically. Logic '1' = -1.7 V typically. Jumper selected as "GATE" or "DELAY. "ECL" is shipped as "GATE".

PERFORMANCE SUMMARY

Proprogation Delay :

"TRIGGER" to:	"RESET" to:
"GATE" = 11 nSec maximum	"GATE" = 11 nSec maximum
"TTL" = 20 nSec maximum	"TTL" = 20 nSec maximum
"ECL" = 11 nSec maximum	"ECL" = 11 nSec maximum
"OR" to:	**"INHIBIT" to:**
"GATE" = 8 nSec maximum	"GATE" = 6 nSec maximum
"TTL" = 15 nSec maximum	"TTL" = 15 nSec maximum
"ECL" = 8 nSec maximum	"ECL" = 8 nSec maximum

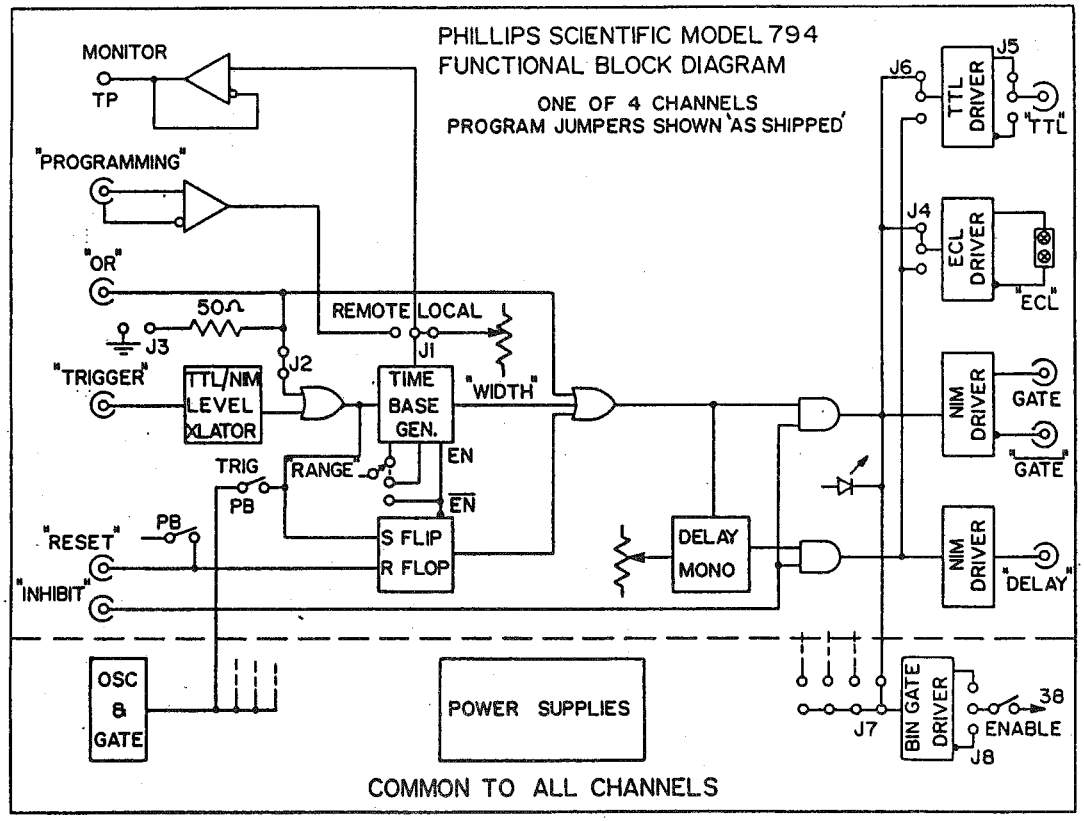
Dead Time : The channel may be triggered immediately upon the completion of the "GATE" logic '1' to logic '0' transition.

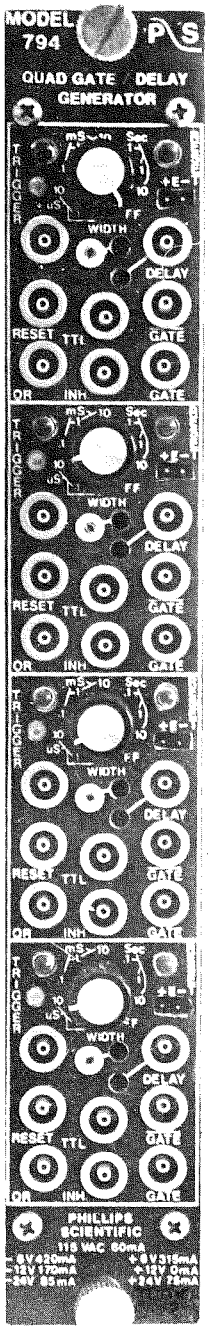
Phillips Scientific 305 Island Road • Mahwah, New Jersey 07430 • USA • (201) 934-8015

MODEL 794

PERFORMANCE SUMMMARY (continued)

Time Jitter	:	Less than 0.03% of range.
Temperature Range	:	0°C to 70°C ambient.
Temperature Stability	:	Less than 400 ppm/°C from 20°C to 50°C
Power Supply Rejection	:	"GATE" width will not change by more than 0.04% of setting for a +/-5% change in any power supply.
Power Supply Requirements	:	-6 V @ 400 mA +6 V @ 325 mA -12 V @ 165 mA +12 V @ 0 mA -24 V @ 85 mA +24 V @ 75 mA





Phillips Scientific 305 Island Road • Mahwah, New Jersey 07430 • USA • (201) 934-8015

MOD. 794 GATE/DELAY UNIT QC CHECK-OFF

DATE: 10-07-88 S/N: 4949

TECH: Nayana ECO: 2002

MODIFICTIONS:

TEST					UNITS
INIT. INSPECT.	✓	✓	✓	✓	
+ 5.3 V.	+5.2				VOLTS
- 5.2 V.	-5.1				VOLTS
+12 A	+12.0				VOLTS
-12 A	-12.1				VOLTS
HIREF.	+7.0				VOLTS
LOREF.	-7.1				VOLTS
HITHR.	+2.4				VOLTS
LOTHR.	-2.6				VOLTS
	CH. A	CH. B	CH. C	CH. D	
RAMP	-2.7	-2.7	-2.7	-2.7	VOLTS
MAX MON. TP	1054	1055	1050	1056	mV.
Tgate > 10 uS	✓	✓	✓	✓	
MIN MON. TP	53	50	47	53	mV.
Tgate < 0.5uS	✓	✓	✓	✓	
Vprog @ 0V.	75	66	68	72	VOLTS
Vprog @ 10V.	1131	1129	1117	1128	VOLTS
Tdel. < 15nS	✓	✓	✓	✓	
Tdel. > 100nS	✓	✓	✓	✓	

MOD. 794 GATE/DELAY UNIT QC CHECK-OFF

DATE: 10-07-88 S/N: 4949

TECH: Nayana ECO: 2002

MODIFICTIONS:

TEST	CH. A	CH. B	CH. C	CH. D	UNITS
DELAY O/P	✓	✓	✓	✓	✓
GATE O/P	✓	✓	✓	✓	✓
/GATE O/P	✓	✓	✓	✓	✓
TTL GATE	✓	✓	✓	✓	✓
/TTL GATE (J5)	✓	✓	✓	✓	✓
TTL DELAY (J6)	✓	✓	✓	✓	✓
/TTL DELAY(J5)	✓	✓	✓	✓	✓
ECL GATE	✓	✓	✓	✓	✓
/ECL GATE	✓	✓	✓	✓	✓
ECL DELAY (J4)	✓	✓	✓	✓	✓
BIN GATE (J7)	✓	✓	✓	✓	✓
/BIN GATE (J8)	✓	✓	✓	✓	✓
FF TRIG. PB	✓	✓	✓	✓	✓
FF RESET PB	✓	✓	✓	✓	✓
FF TRIG I/P	✓	✓	✓	✓	✓
INHIBIT I/P	✓	✓	✓	✓	✓
RESET I/P	✓	✓	✓	✓	✓
O/P "OR"(J2)	✓	✓	✓	✓	✓
INP. "OR"(J2)	✓	✓	✓	✓	✓

MODEL 794 CALIBRATION CHECK-OFF

DATE: 10-07-88

S/N: 4949

TECH: Nayana

ECO: 2002

MODIFICTIONS:

TEST	CH. A	CH. B	CH. C	CH. D	UNITS
CAP. RANGE	med	med	med	med	HI or LO
I source R.	28.7	28.7	28.7	28.7	Kohms
1 uS MAX.	1056	1046	1048	1048	nS.
10 uS. MAX.	10.50	10.49	10.50	10.47	uS.
0.1 mS. MAX.	107.6	107.1	106.2	107.5	uS.
1 mS. MAX.	1067	1062	1074	1053	uS.
10 mS. MAX.	10.69	10.43	10.39	10.59	mS.
0.1 S. MAX	105.5	107.6	105.5	105.6	mS.
1 S. MAX.	1080	1065	1078	1074	mS.
10 S. MAX.	10.82	10.99	10.97	11.08	S.
10 S.MIN.	.470	.471	.448	.458	S.
1 S. MIN.	47.4	46.0	44.6	44.9	mS.
0.1 S. MIN.	4.67	4.72	4.41	4.47	mS.
10 mS. MIN.	474.6	459.2	436.9	452.5	uS.
1 mS. MIN.	48.3	47.3	45.8	45.6	uS.
0.1 mS. MIN.	491	4.82	4.58	4.71	uS.
10 uS. MIN.	497.7	491.8	471.3	478.0	nS.
1 uS. MIN.	60.8	62.5	58.0	60.3	nS.
JITTER @ 10uS.	2.0	2.0	2.0	2.0	nS.

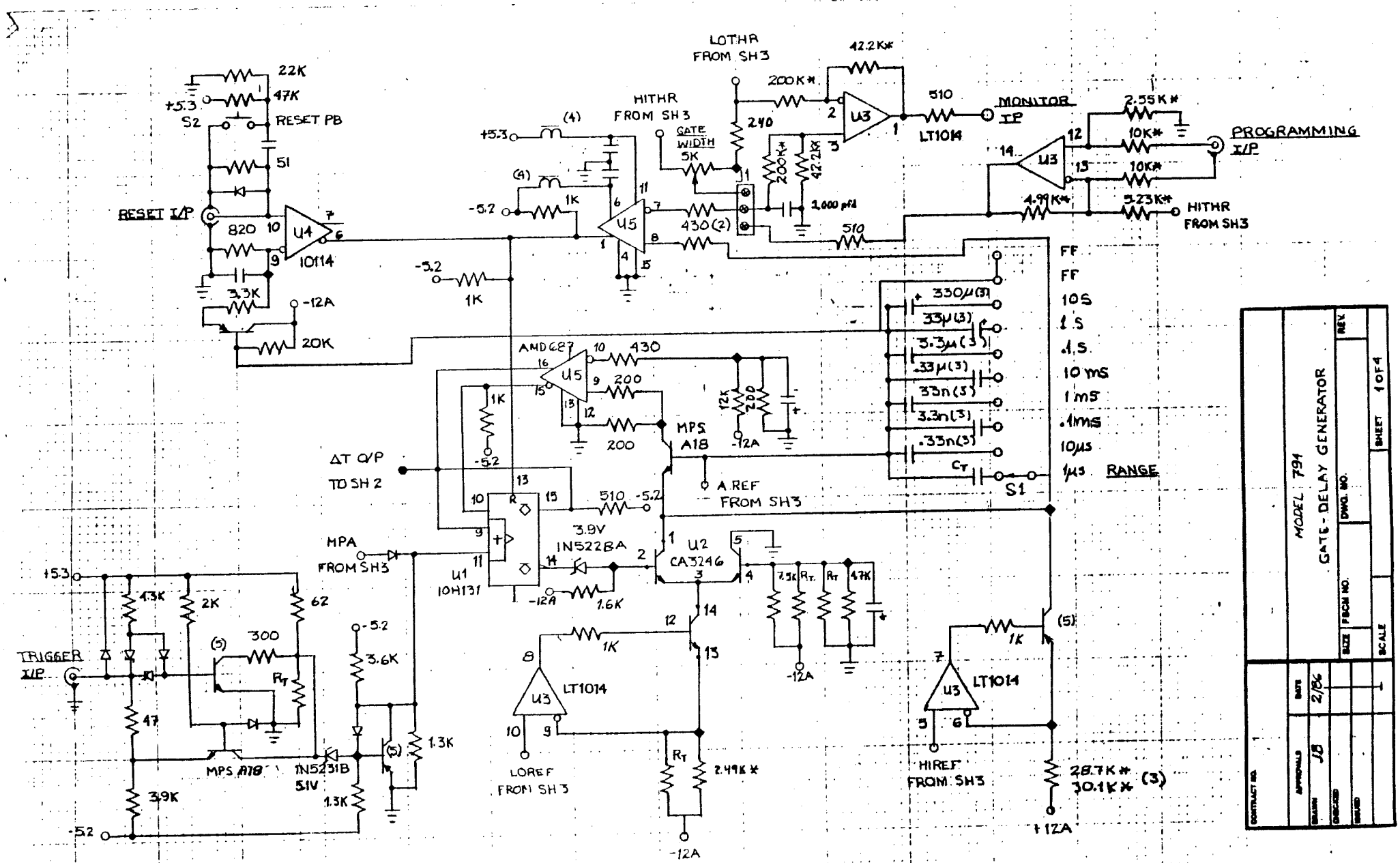
MODEL 794 CALIBRATION CHECK-OFF

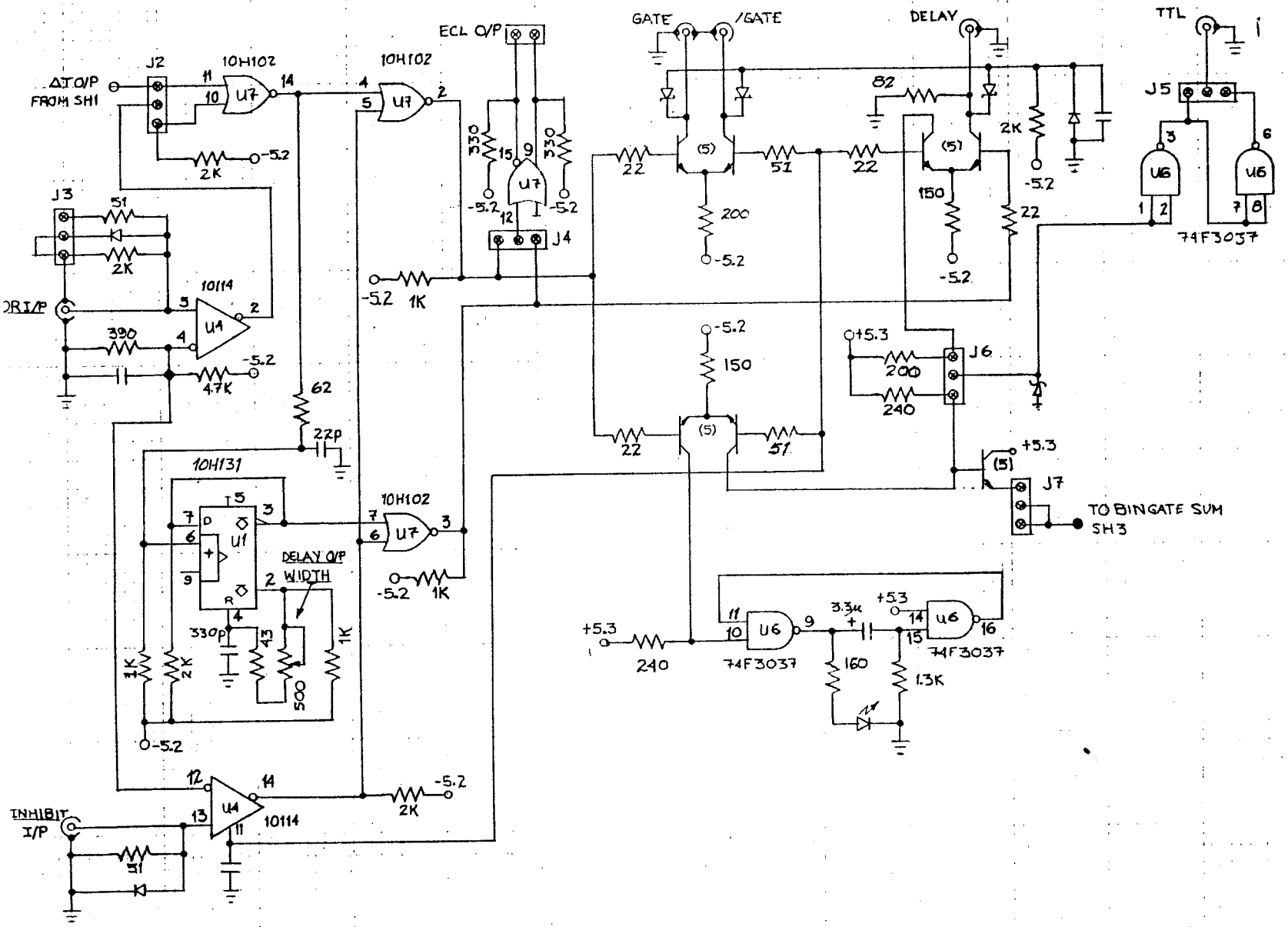
DATE: 10-07-88 S/N: 4949

TECH: Nayana ECO: 2002

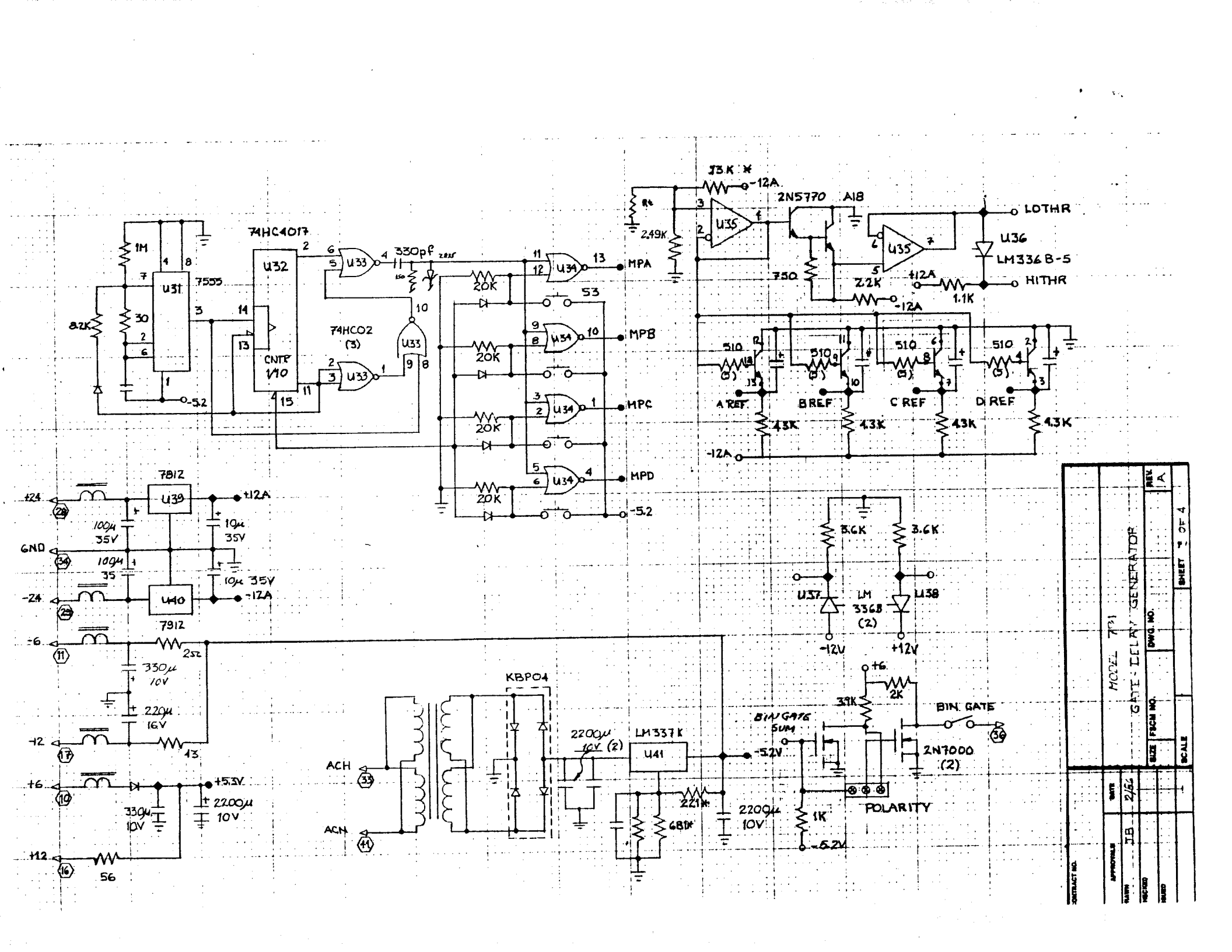
MODIFICTIONS: _____

JUMPER ASS'Y	CH. A	CH. B	CH. C	CH. D	LOCATION
J1 LOC./REMO.	✓	✓	✓	✓	LOC.
J2 I/P O/P OR	✓	✓	✓	✓	INP.
J3 50/2Kohm	✓	✓	✓	✓	2 Kohm
J4 ECL G/DEL	✓	✓	✓	✓	GATE
J5 TTL NOR/COM	✓	✓	✓	✓	NORM.
J6 TTL G/DEL	✓	✓	✓	✓	GATE
J7 BIN E/D	✓	✓	✓	✓	DISABLED
J8 BIN NOR/COM	✓	✓	✓	✓	NORM.


LOTHR FROM SH3
HITHR FROM SH3
GATE WIDTH 5K
MONITOR O/P
PROGRAMMING I/P
RESET I/P
RESET PB
S2
ΔT O/P TO SH 2
A REF FROM SH3
MPA FROM SH3
TRIGGER I/P
LOREF FROM SH3
HIREF FROM SH3
MPS A18
IN5231B 5.1V
IN5228A 3.9V
LT1014
AMD687
CA3246
10H131
S1
FF
FF
10S
1 S
.1 S
10 mS
1 mS
.1mS
10µS
1µS RANGE
MODEL 794
GATE-DELAY GENERATOR
SHEET 1 OF 4



CONTRACT NO.		MODEL 794	REV.		
	APPROVALS	GATE-DELAY GENERATOR	DWG. NO.		SHEET 2 OF 4
	DATE		SIZE	FSCM NO.	SCALE
	DRAWN 2/86				
	CHECKED				
	ISSUED				

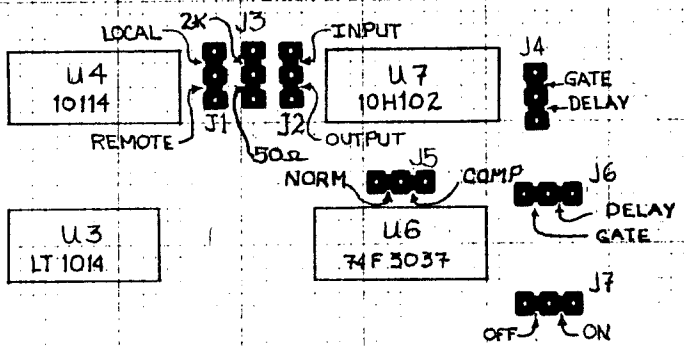

74HC4017
U32
7555
U31
1M
8.2K
30
CNTR 1/10
74HCO2 (3)
330pf
20K
MPA
MPB
MPC
MPD
53
-5.2
33K
-12A
2N5770
A18
U35
2.49K
750
2.2K
1.1K
+12A
LOTHR
HITHR
U36
LM336B-5
510
A REF
B REF
C REF
D REF
4.3K
7812
U39
7912
U40
+24
GND
-24
100µ 35V
10µ 35V
+12A
-12A
+6
+12
+5.3V
330µ 10V
220µ 16V
2200µ 10V
56
43
252
3.6K
U37
U38
LM 336B (2)
-12V
+12V
KBP04
ACH
ACN
2200µ 10V (2)
LM337K
U41
221K
681K
BIN GATE SUM
39K
2K
BIN GATE
2N7000 (2)
1K
POLARITY
-5.2V
MODEL 791
GATE-DELAY GENERATOR
REV. A
SHEET 1 OF 4
DWG. NO.
FSCM NO.
SIZE
SCALE
DATE
2/82
APPROVALS
JB
CONTRACT NO.

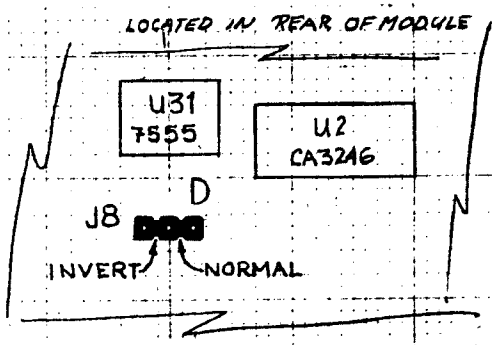
DEVICE	DESIGNATION	+5.2	-5.2	+12R	-12R	GND
10114	U4		8			1,16
10H102	U7		8			1,16
10H131	U1		8			1,16
74F3037	U6	13,12				4,5
74HC02	U33, U33		7			14
74HC4017	U32		8			16
7555	U31		4			8
AM687	U5	11	6			3,14
LF412	U35			8	4	
LT1014	U3			4	11	

NOTES

1) RESISTORS ARE 1/8 W. CF UNLESS OTHERWISE SPECIFIED
2) UNMARKED CAPS ARE 0.1μf MONO
3) INDICATES A SELECTED COMPONENT
4) 3.9μH BEAD W/ 2 TURNS OF #26 WIRE
5) INDICATES SURFACE MOUNT COMPONENT
6) * - INDICATES 1/3 W. CF, 1% RESISTOR
7) ⬡ = NIM BLOCK PIN

PROGRAM JUMPER CONFIGURATION





PROGRAM JUMPER SUMMARY

J1 SELECTS GATE WIDTH CONTROL VIA THE FRONT PANEL POT OR REAR PANEL PROG. INPUT
J2 SELECTS "INPUT OR" MODE OR "OUTPUT OR" MODE
J3 SELECTS 50 OHM OR 'HI Z' 'OR" INPUT
J4 ASSIGNS "ECL" OUTPUT TO GATE OR DELAY
J5 ASSIGNS "TTL" OUTPUT TO NORMAL OR COMPLEMENT
J6 ASSIGNS "TTL" OUTPUT TO GATE OR DELAY
J7 CONNECTS THE CHANNEL TO THE 'BIN GATE' DRIVER
J8 SELECTS 'NORMAL' OR 'INVERTED" BIN GATE

MODEL 794
GATE · DELAY GENERATOR
DWG. NO.
REV.
SHEET 4 OF 4
SIZE
FSCM NO.
SCALE
CONTRACT NO.
APPROVALS
DATE
4/86
DRAWN
JB
CHECKED
ISSUED