DEMULTIPLEXERS [COMPLETE]

Demultiplexers (DEMUX)

A demultiplexer is a combinational logic circuit that takes one input and routes it to one of many output lines,

based on the values of select lines (control inputs).

• Opposite of a multiplexer (MUX).

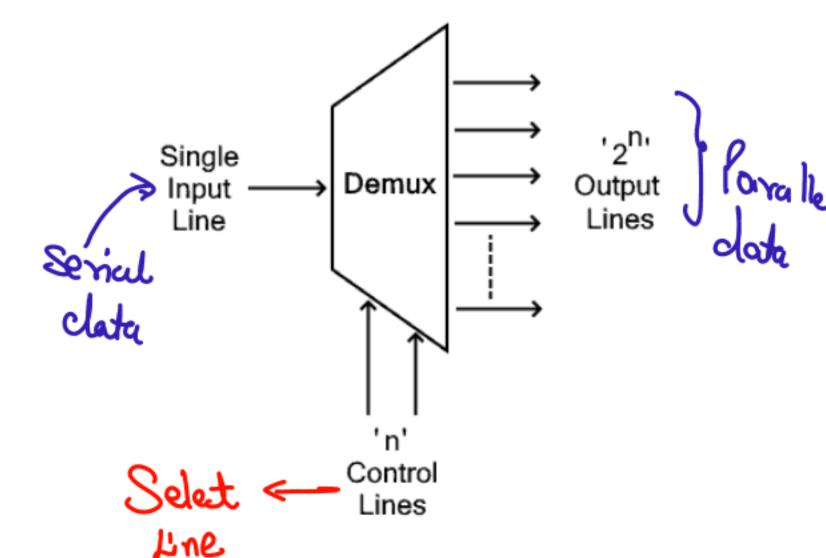
It distributes data from one input line to multiple output lines.

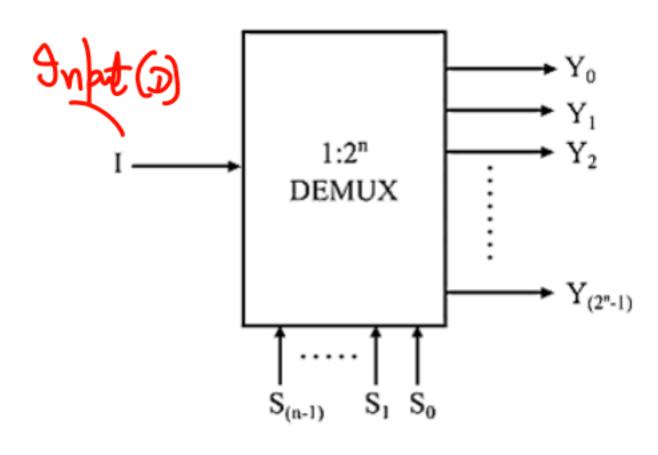
• The output line activated depends on the combination of select inputs.

It convert the serial signals into parallel data output lines.

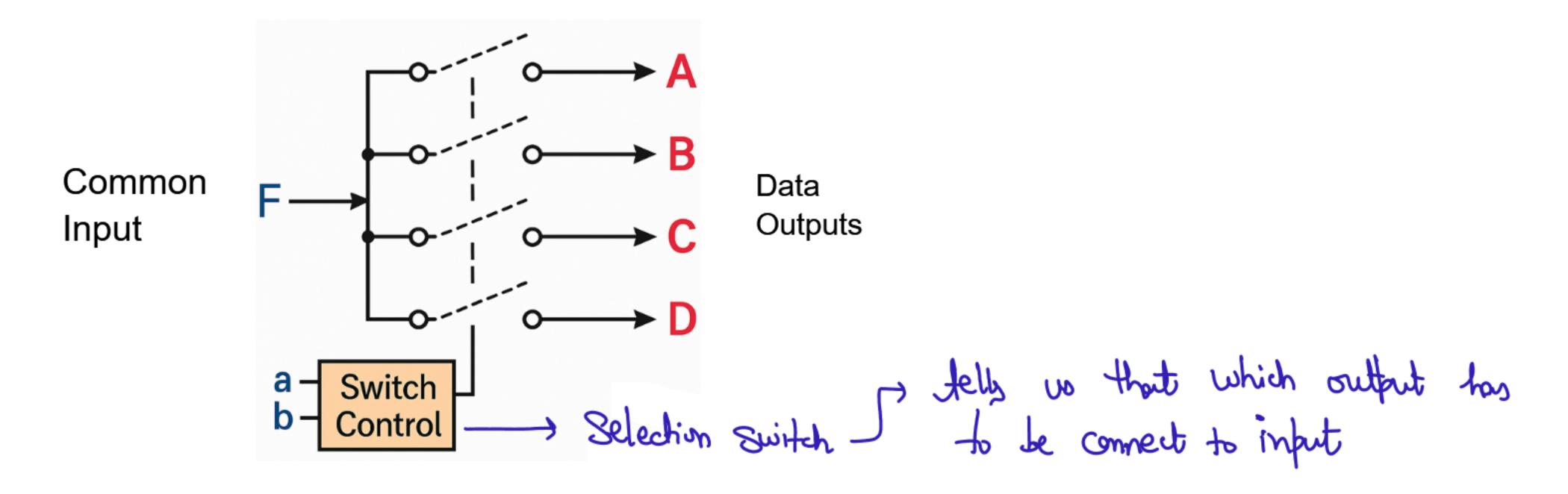
Data on one line Where bits transferred Buccessively. One after one

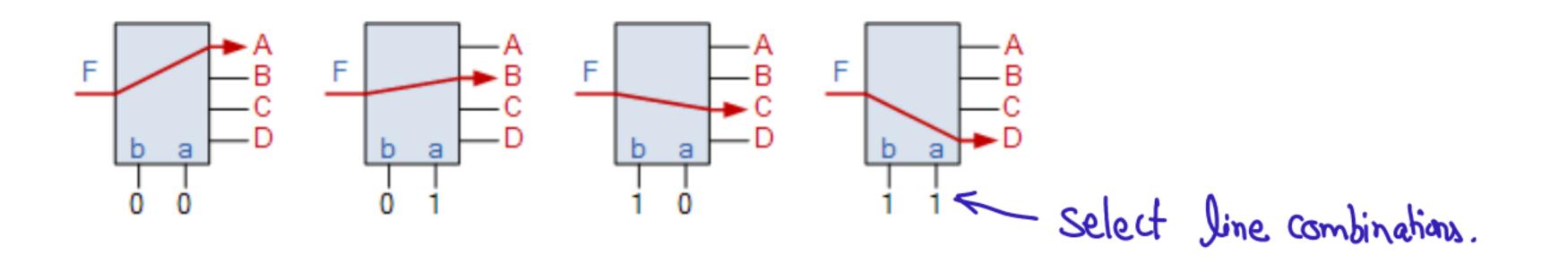
All bits thands in Parallel on separate line



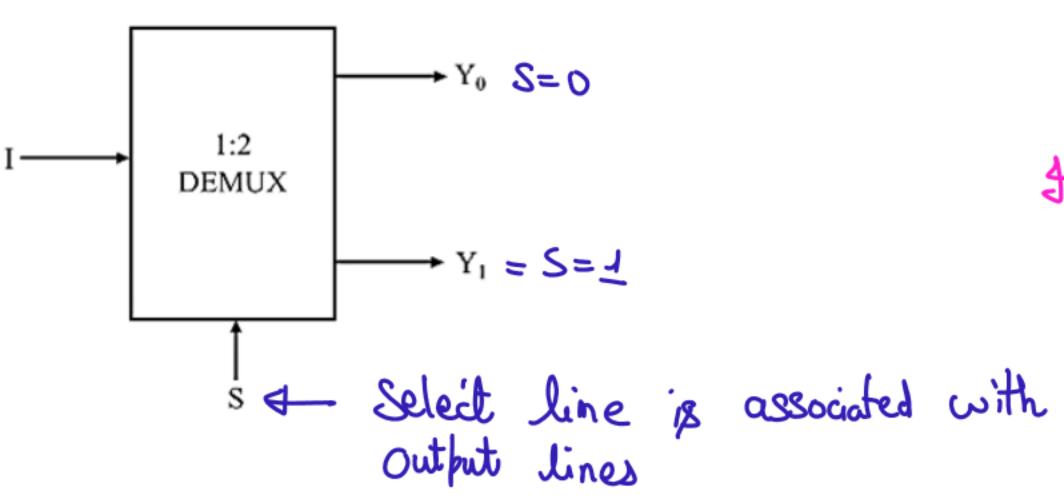


Visual representation of Demultiplexers



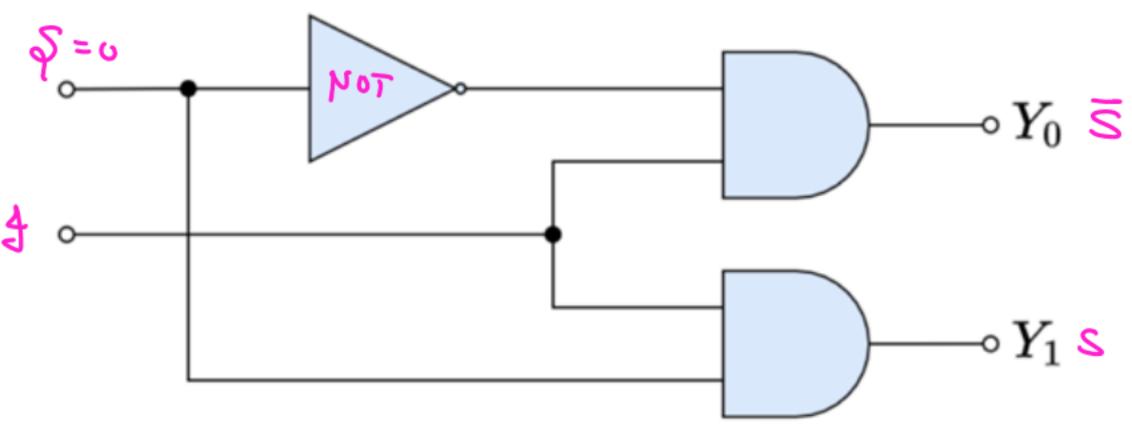


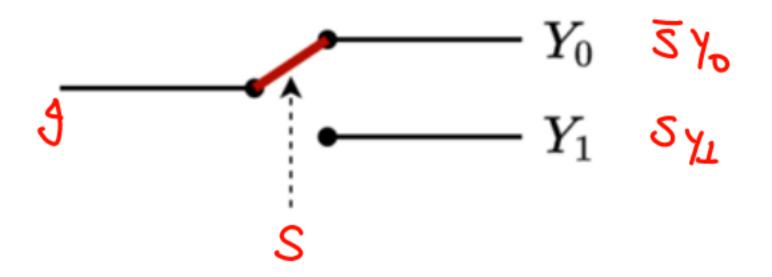
1x2 Demultiplexer



Select Line	Out	outs		
S	Y 1	Yo		
0	0	I	₹ γ _ν ·)
1	I	0	Syı	
			~ 0	parallel
				Parallel orithut

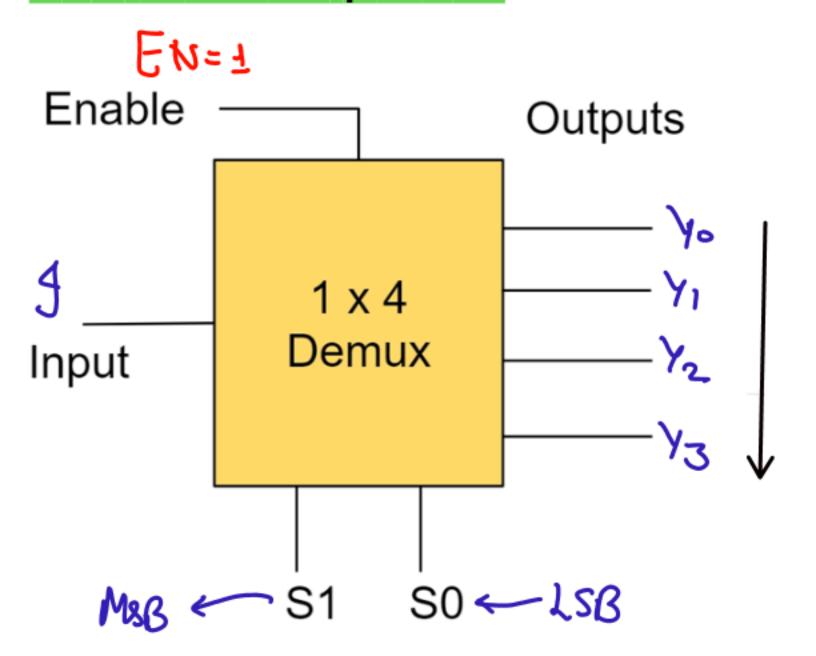
Select	mout	y, out	wh yo	
0	0	×	0	†
O	1	X	4	1
4	0	0	X	> don't Care
4	7	1		L CON O CHAS





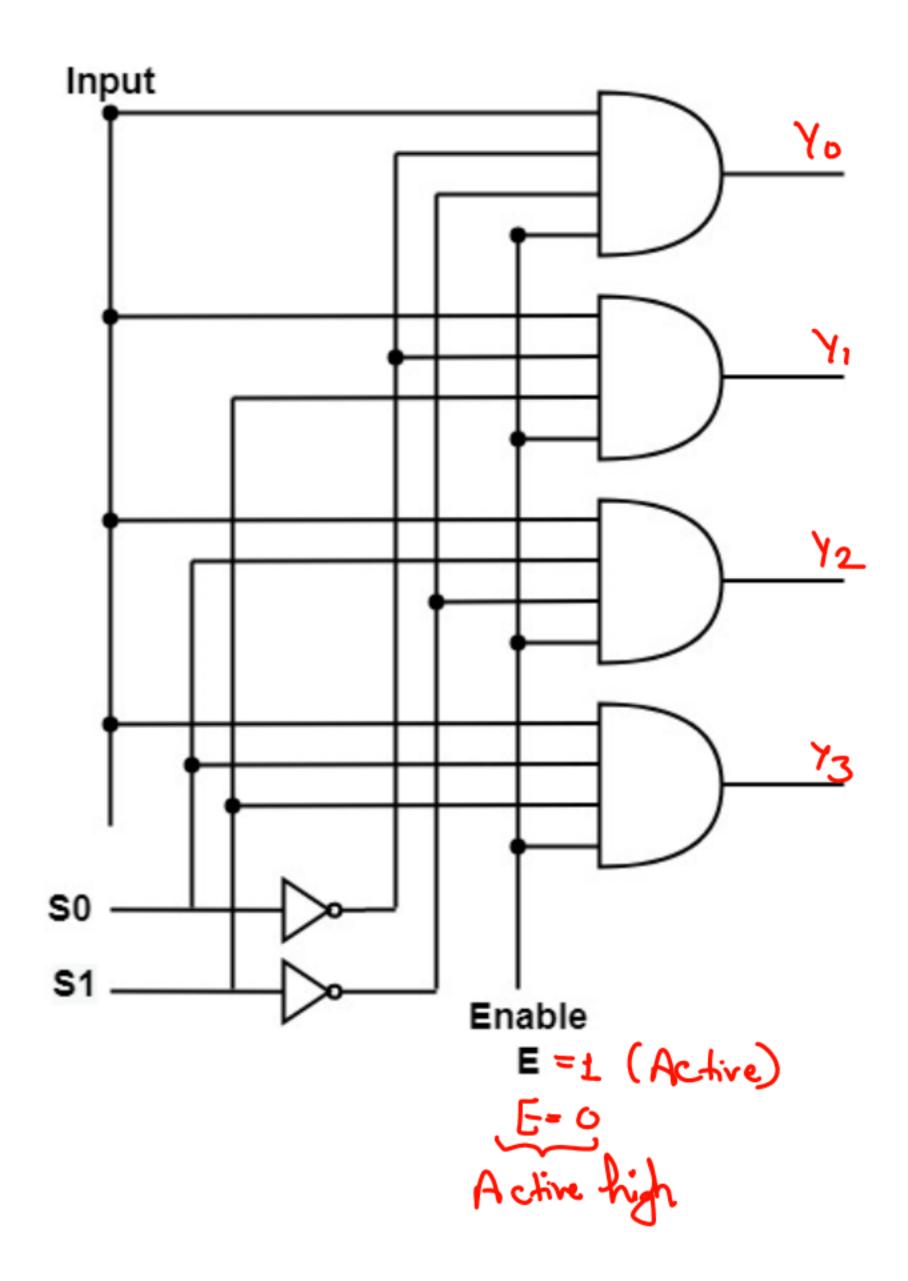
Switch Equivalent

1x4 Demultiplexer



* Each input is a product term hence represented by AND gate.

Select	Line		Outputs			
S 1	S0	Y3	Y2	Y1	Y0	
0	0	0	0	0	(I)	5,5, Yo
0	1	0	0	I	0	5,5072 S15072
1	0	0	Ī	0	0	S1 50 Y2
1	1		0	0	0	S1 S0 Y3



Half adder and Half subtractor using DeMux

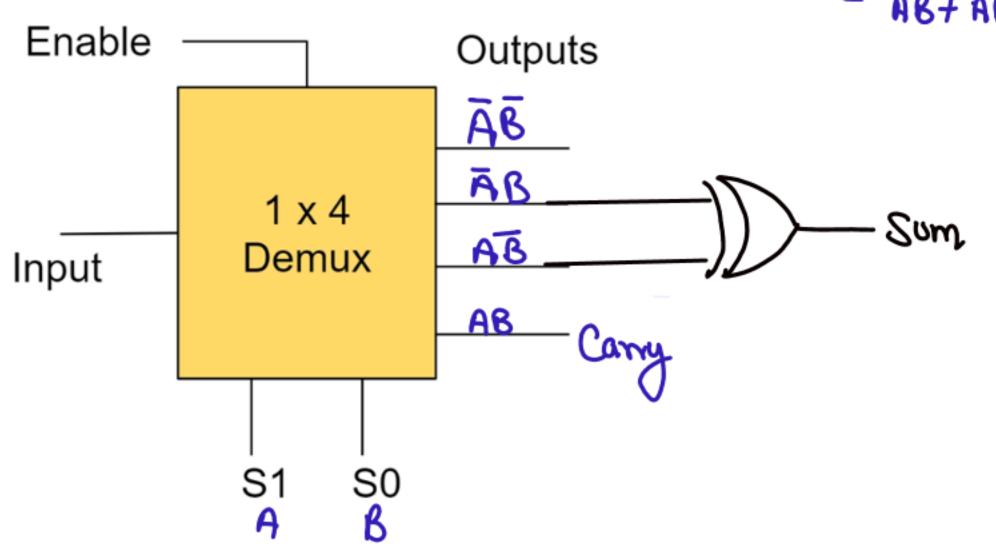
☐ Half Adder

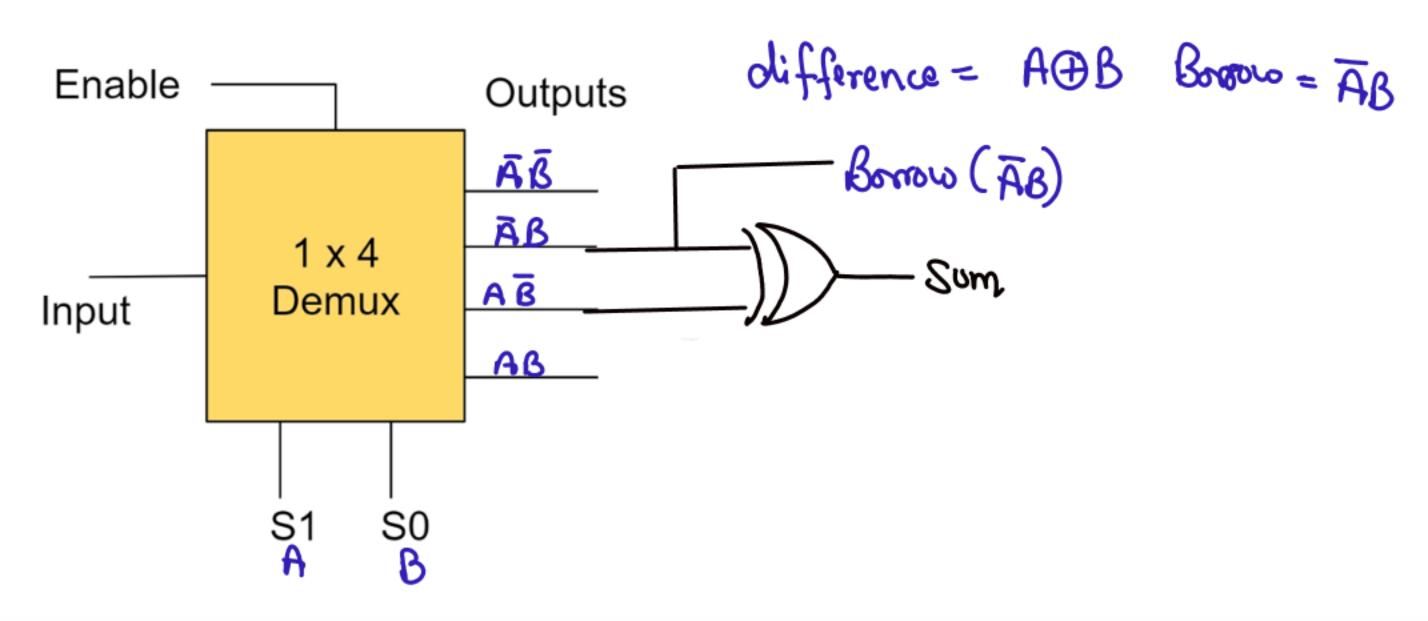
Α	В	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

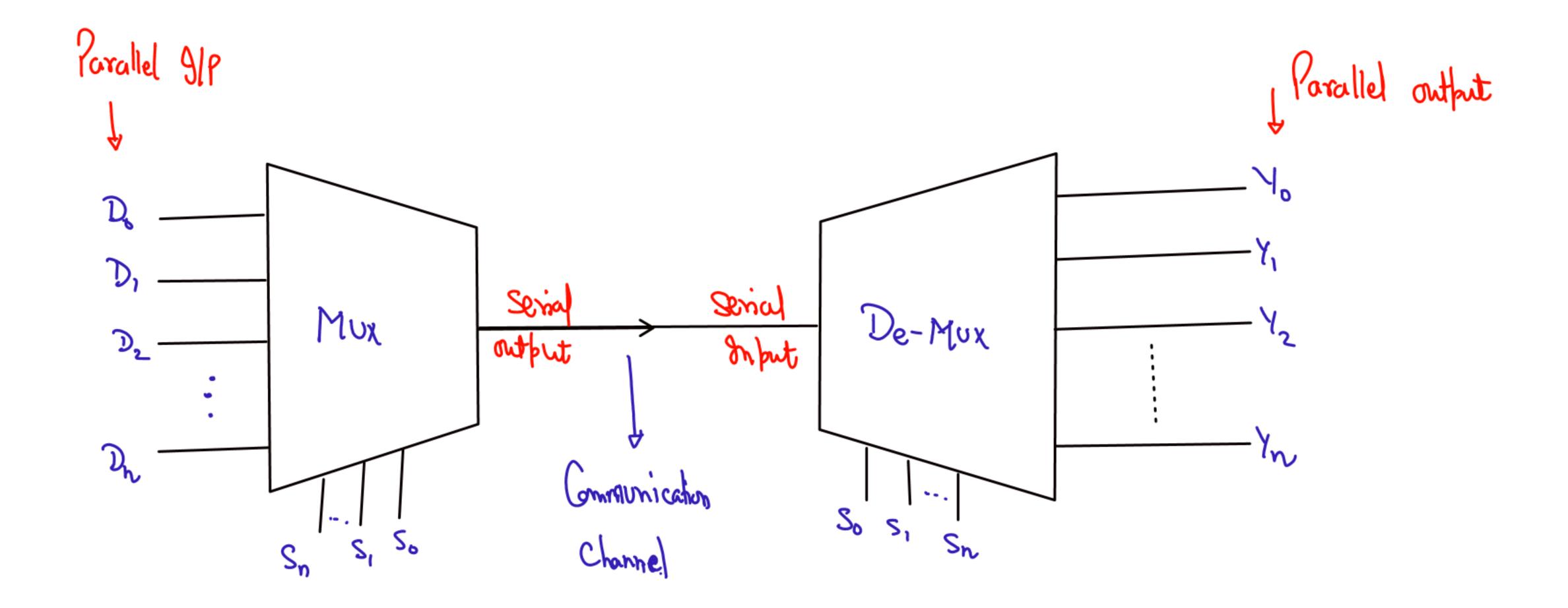
☐ Half Subtractor

Α	В	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0









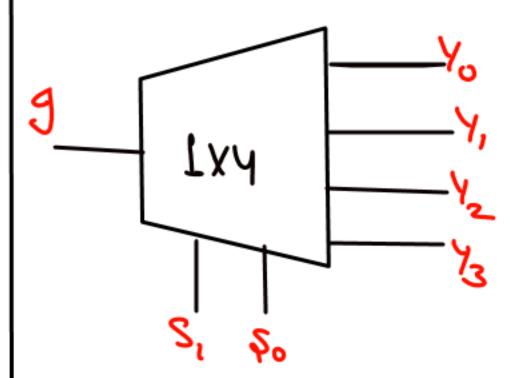
1x8 DeMux using 1x4 DeMux

- ☐ We can build a 1×8 Demultiplexer using two 1×4 Demultiplexers and an extra select line as a control.
- □ we requireTWO 1×4 Demultiplexers in SECOND stage in order to get the final EIGHT outputs.

	Sele	ection In	puts /	_ksg Outputs							
B —	S 2	S 1	S0	Y 7	Y6	Y 5	Y4	Y 3	Y ₂	Y 1	Yo
	0	0	0	0	0	0	0	0	0	0	I
	0	0	1	0	0	0	0	0	0	I	0
	0	1	0	0	0	0	0	0	I	0	0
	0	1	1	0	0	0	0		0	0	0
	1	0	0	0	0	0	I	0	0	0	0
	1	0	1	0	0	I	0	0	0	0	0
	1	1	0	0	I	0	0	0	0	0	0
	1	1	1	ı	0	0	0	0	0	0	0
	∱		7			!	1			!	
	Se on	1:2 De	mux Us	se 5, 4!	S ₀						
	at dir	st stage	11107	at Secon	so Nd Stage						

1x8 DeMux using 1x4 DeMux Y₇ 1 x 4 Y_6 Demultiplexer Y₅ → Y₄ 1 x 2 ← Jower Significance Demultiplexer 1 x 4 → Y₂ Demultiplexer Y_1 → Y₀ MSB

1 X4 Demux



Possible outputs
$$< 0 0 - 10$$

 $1 0 \rightarrow y$

High order DeMux to Low order DeMux: GENERAL FORMULA

o In Mux, MSB is used as select line at last Stage but In DeMux, MSB is used as select line at first stage.

In general, to simplement 1:13 Demox using 1:1 Demox then

 $K_{n-1}/A = K_n = 1$ (first Stage)

* If $K_{n-1}/A = K_n \neq 1$, then implement 1:A Demox at first stage. Q.1 How many 1:4 DeMuxes are required in 2nd stage to implement 1:64 DeMux?

1:B

1: A

Q.2 How many 1:2 DeMuxes are required to implement 1:64 DeMux?

$$\beta/A \rightarrow K$$