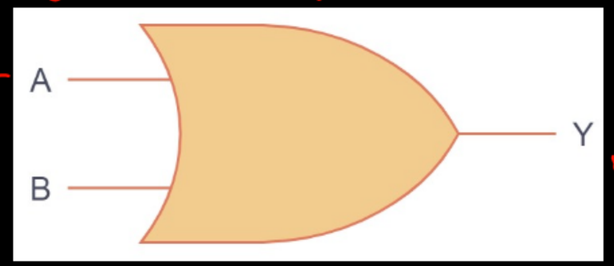
OR Gate :

↳ अथवा, या

→ If any input is true or high then output will be True.

Symbolic Representation :



I/P

OR

A + B

Y = A + B

Truth Table

A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

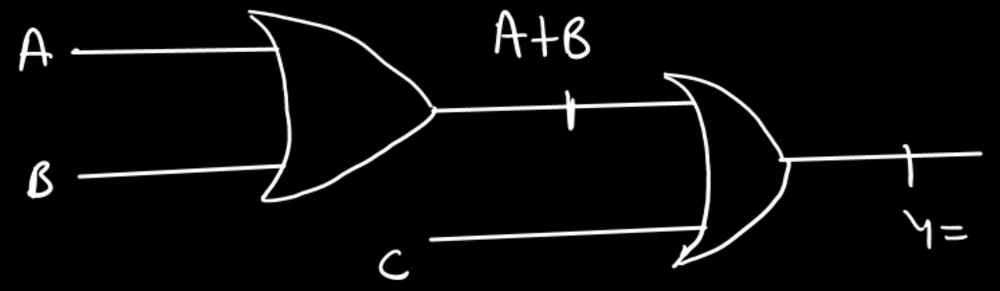
a) Commutative Law : $A + B = B + A$

↳ Possible

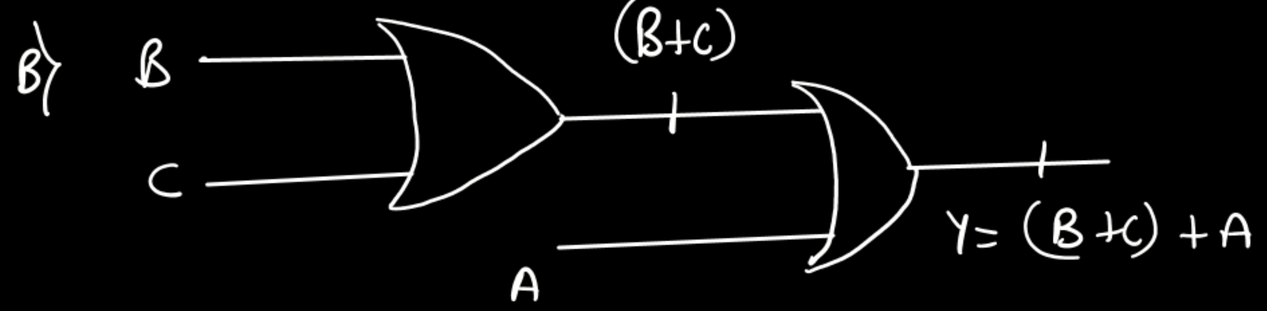
b) Associative Law :

$A + (B + C) = (A + B) + C$ } Possible

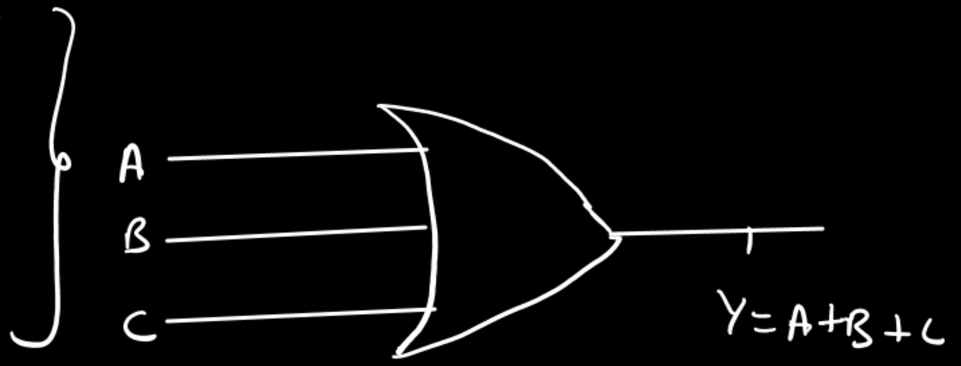
A)



B)



$$Y = A + B + C$$



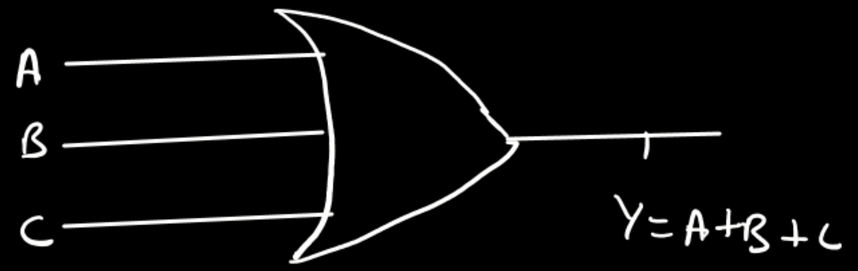
Three Input OR Gate

Truth Table

A	B	C	Y = A+B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

input = 3,

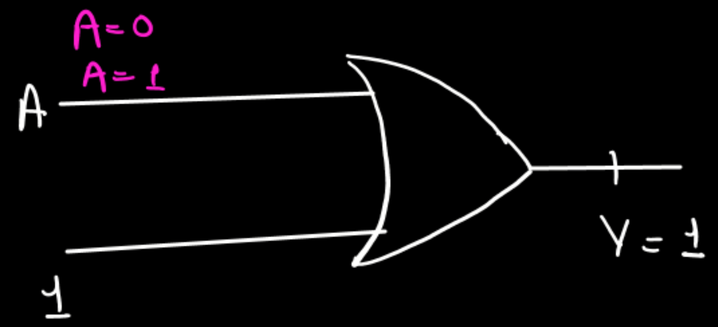
↳ 2^3 = 8 combinations



Three Input OR Gate

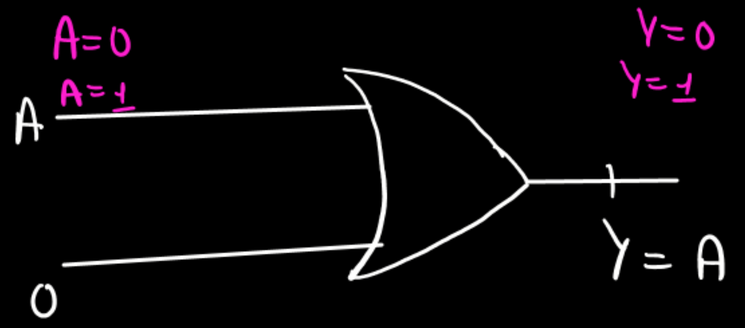
* If any I/P is high then O/P = high

Enable & Disable OR Gate:



→ O/P is not dependent on Input & O/P will stay at 1.

↳ It is Disabled OR Gate

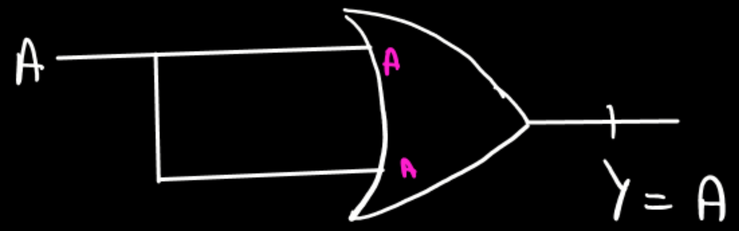


→ O/P is dependent on Input (A)

↳ It is enabled OR gate

↳ Act like a buffer

Floating Input OR Gate



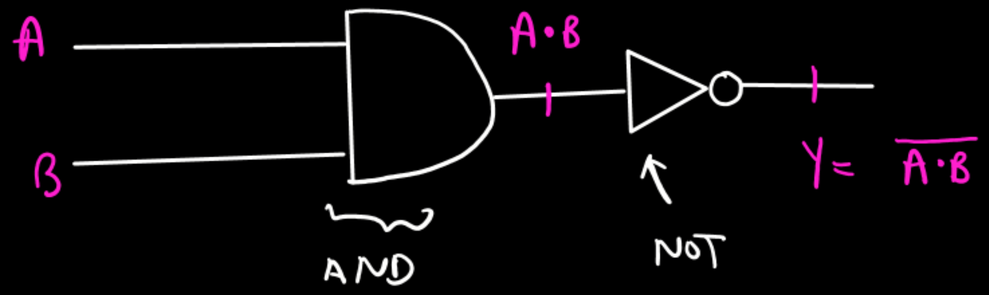
$\{A=0, Y=0\}$

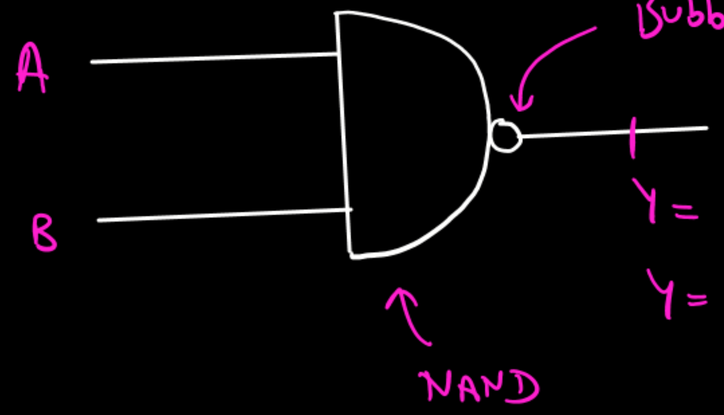
$\{A=1, Y=1\}$

$Y=A$ ← Buffer

NAND Gate

↳ AND gate with Not Gate (AND → NOT)





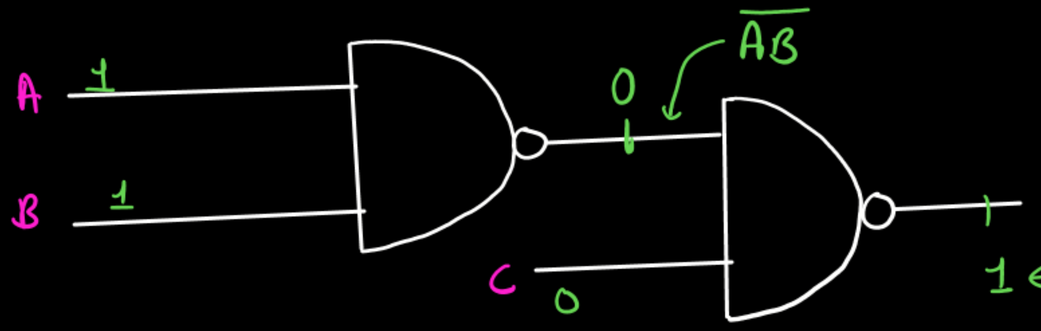
Truth Table

A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

* Commutative law :

$$\overline{A \cdot B} = \overline{B \cdot A}$$

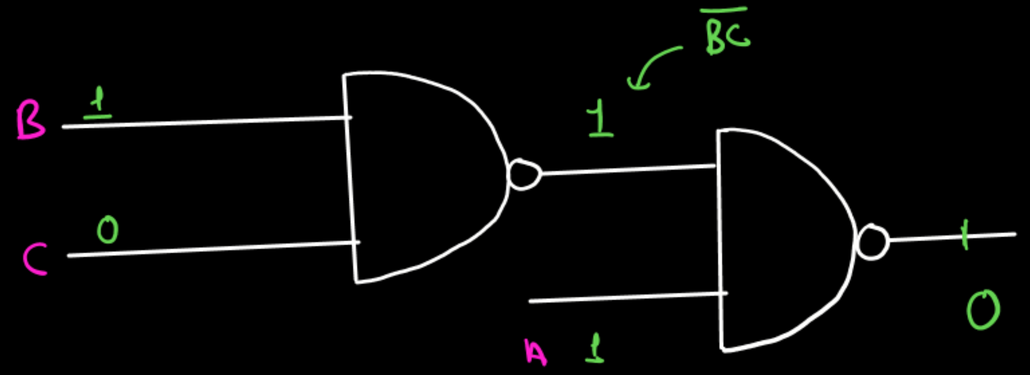
(NAND gate follows Commutative law)



$A = 1, \quad B = 1, \quad C = 0$

$1 \leftarrow \overline{\overline{AB} \cdot C}$

$\hookrightarrow \quad \overline{\overline{AB} \cdot C} = 1$

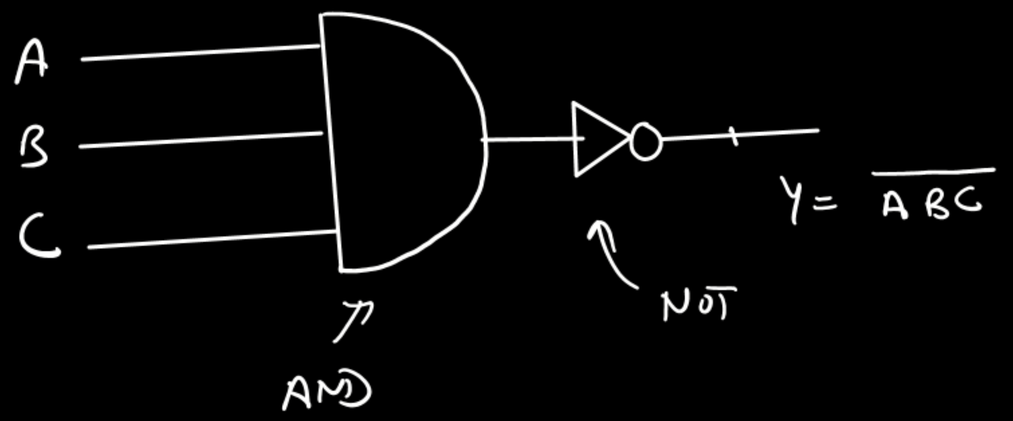


$0 = \overline{\overline{BC} \cdot A} \Rightarrow \overline{\overline{BC} \cdot A} = 0$

$\Rightarrow \overline{\overline{AB} \cdot C} \neq \overline{\overline{BC} \cdot A}$ (It does not follow the law of Associativity)

3 input NAND Gate:

↳ AND gate with 3 inputs + 1 NOT

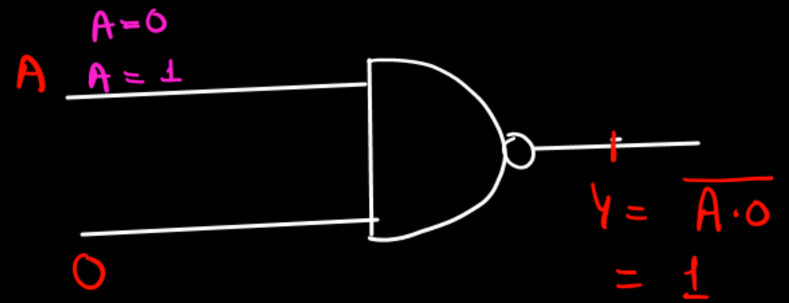


* 3 input AND Gate Can NOT be directly obtained from two input NAND Gate (Cascading).

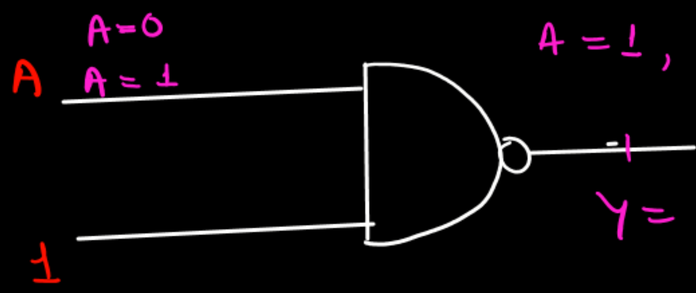
Truth Table

A	B	C	ABC	$\overline{ABC}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Enabled & Disabled NAND Gate :



* O/P remains 1 & does NOT responding by changing in input signal
→ Disabled NAND Gate



A=0, $A \cdot 1 = 0 \cdot 1 = 0$, $\overline{A \cdot 1} = 1$
A=1, $A \cdot 1 = 1 \cdot 1 = 1$, $\overline{A \cdot 1} = \overline{1} = 0$

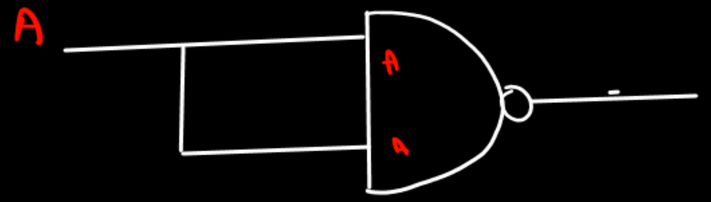
A=0, Y=1
A=1, Y=0

* Output dependent on I/P

A=0, Y=1
A=1, Y=0
} $Y = \overline{A}$ ← Inverter

→ Enabled NAND Gate
↳ Act like an Inverter (NOT)

Floating I/P NAND Gate



A=0, $Y = \overline{A \cdot A} \Rightarrow \overline{0 \cdot 0} = \overline{0} = 1$
A=1, $Y = \overline{A \cdot A} \Rightarrow \overline{1 \cdot 1} = \overline{1} = 0$
} Act like an Inverter