DECODERS AND ENCODERS (PART 01)

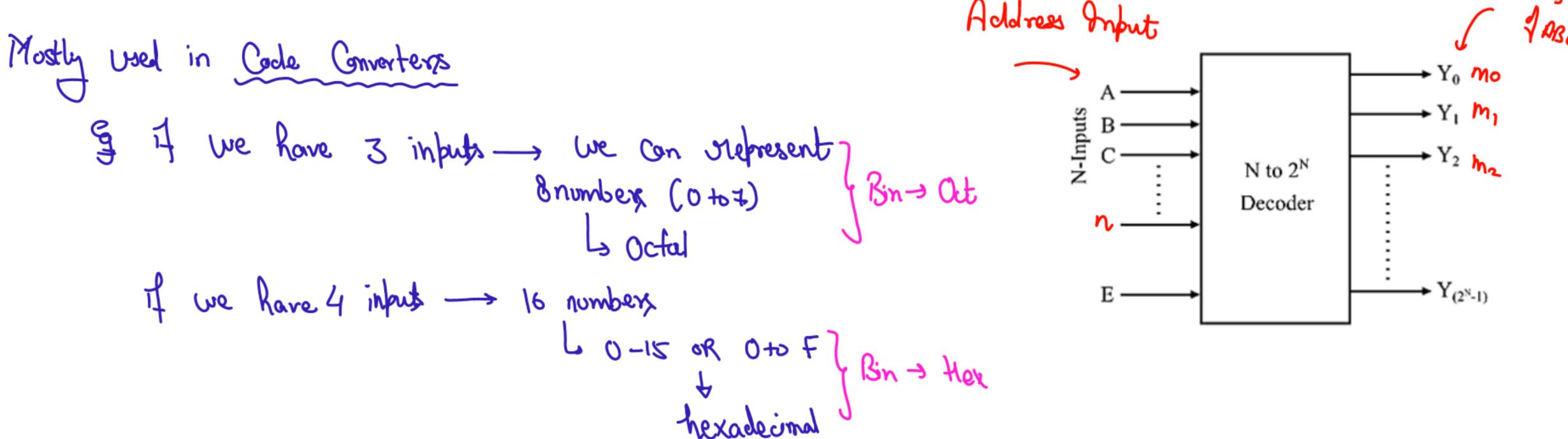
#### WHAT IS DECODER?

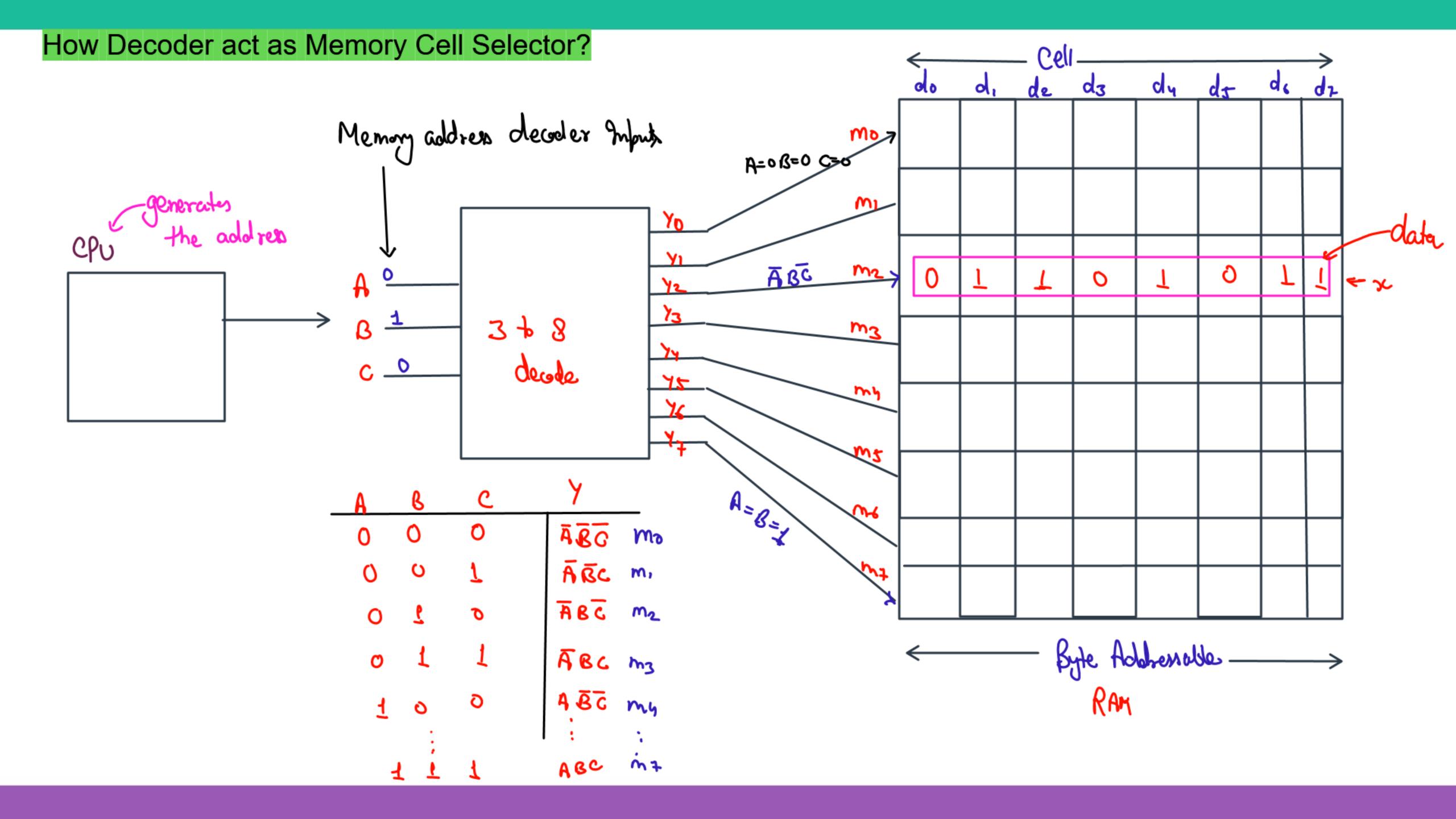
ah

"Decoder is a combinational circuit that has 'n' input lines and maximum of 2<sup>n</sup> output line. Where the outputs of decoder are nothing but the minterms of 'n' input variable lines, when it is Enabled"

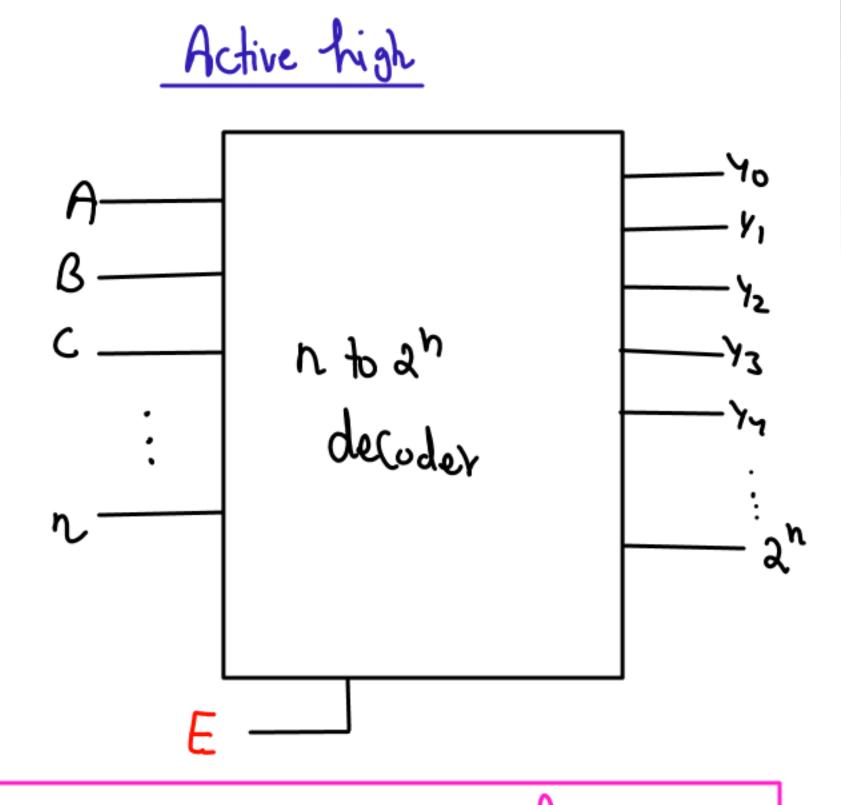
The input combinations of decoder are also termed as Address input, at it act an interface between CPU and Memory (RAM).

The combination of each input will select a cell of memory.



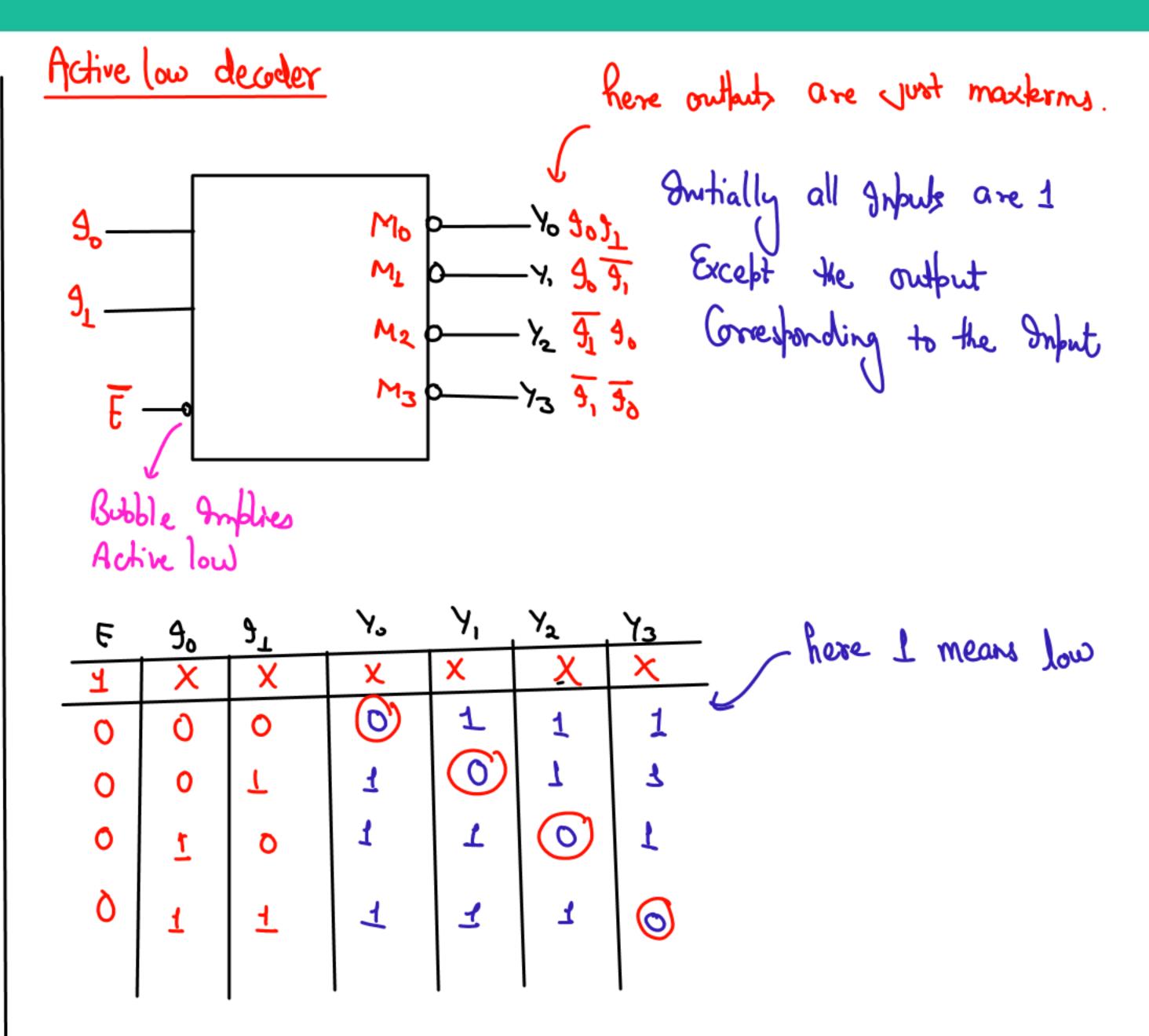


### Active high and Active low Decoder



In Active high deader of Enable (E) is high then decoder is Active otherwise Inactive

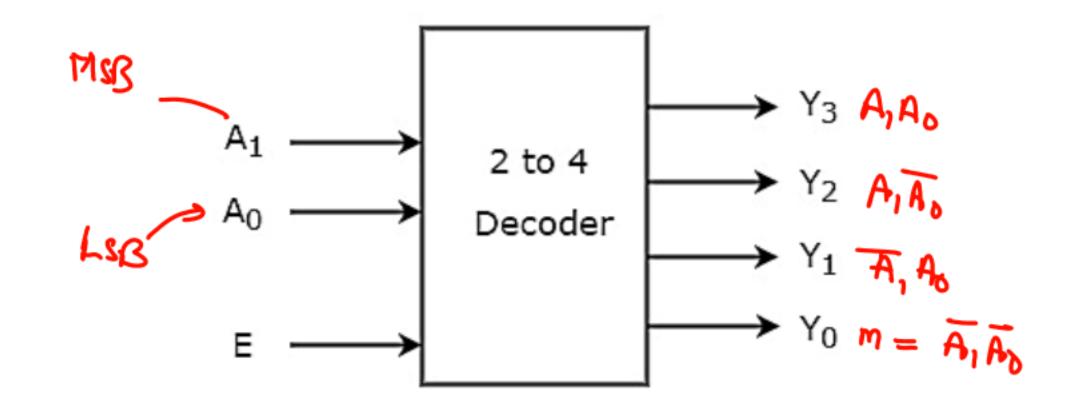
$$En=0 \rightarrow obt$$
  
 $En=\overline{1} \rightarrow on$ 



### 2 to 4 Decoder

2 to 4 Decoder has 2 input lines and 4 output lines.

Enable	Inputs			Out	puts		
	<b>A1</b>	Α0	Y3	Y2	<b>Y1</b>	Y0	
0	X	Х	Х	Х	Х	Х	
1	0	0	0	0	0	1	mo de Active high
1	0	1	0	0	1	0	
1	1	0	0	(1)	0	0	
1	1	1	1	0	0	0	

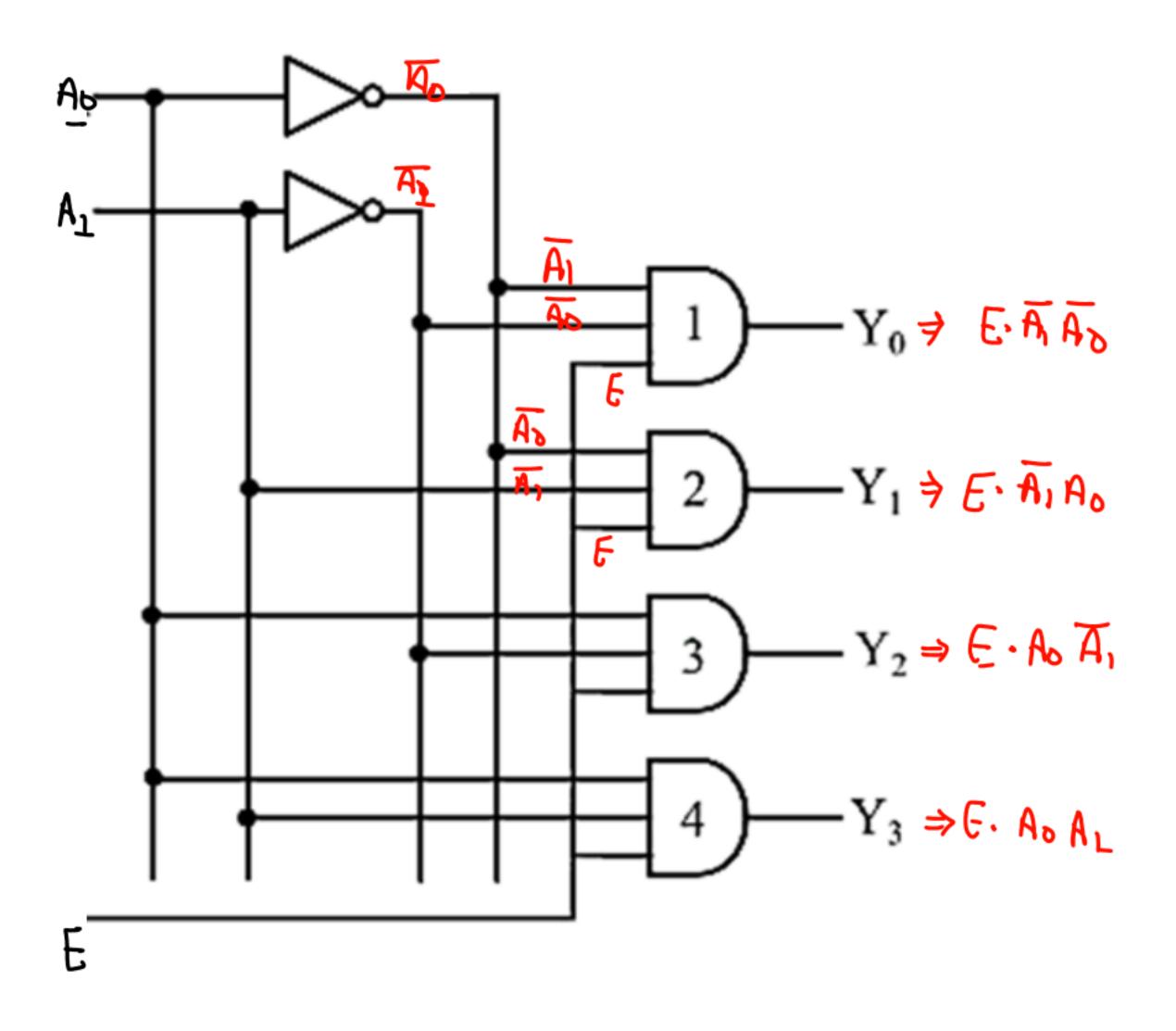


$$Y_3 = E \cdot A_1 A_0$$
 $Y_2 = E \cdot A_1 \overline{A_0}$ 
 $Y_1 = E \cdot \overline{A_1 A_0}$ 
 $Y_0 = E \cdot \overline{A_1 A_0}$ 

\* Each output is one product term
L. AND
total 4 Product terms
L. Hold 4 AND gates

OF If there are 'n' output lines then total 'n' product terms will be there hence It nequired 'n' AND gates

### 2 to 4 Decoder



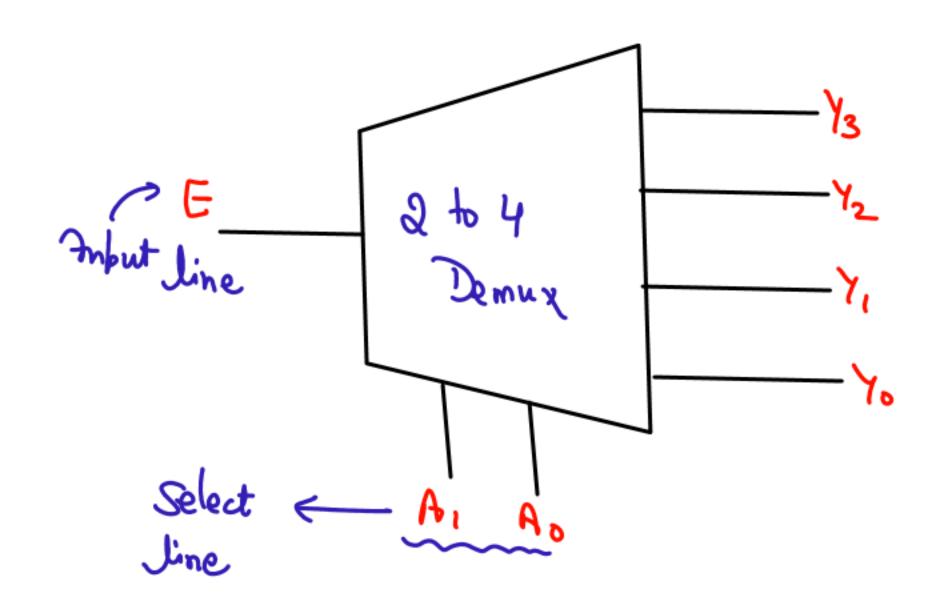
\*A decoder Con works as

Demultiplexer where the input

I Demux = E of decoder and
the Select linex of demux

will work as the input lines of

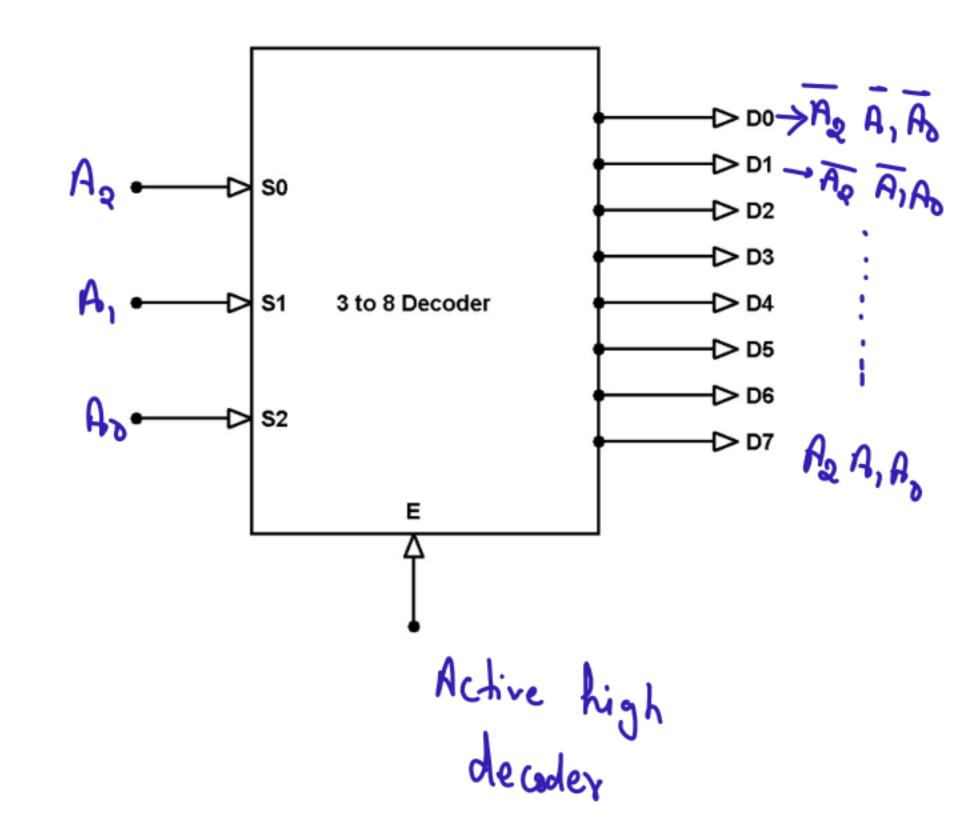
decoder



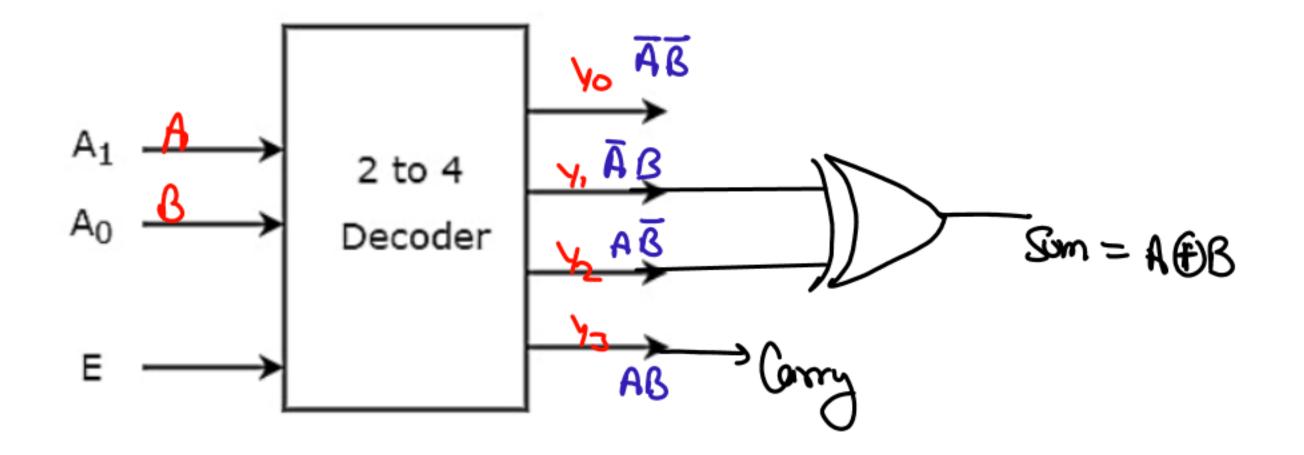
# 3 to 8 Decoder

3 to 8 Decoder has 3 input lines and 8 output lines.

Enable	Inputs			Outputs								
	<b>A2</b>	<b>A1</b>	Α0	Y7	Y6	Y5	Y4	<b>Y3</b>	Y2	Y1	Y0	
0	X	X	Х	X	X	Х	X	X	X	X	X	
1	0	0	0	0	0	0	0	0	0	0	1	
1	0	0	1	0	0	0	0	0	0	1	0	
1	0	1	0	0	0	0	0	0	(1)	0	0	
1	0	1	1	0	0	0	0	1	0	0	0	
1	1	0	0	0	0	0	1	0	0	0	0	
1	1	0	1	0	0	(1)	0	0	0	0	0	
1	1	1	0	0	1	0	0	0	0	0	0	
1	1	1	1	1	0	0	0	0	0	0	0	

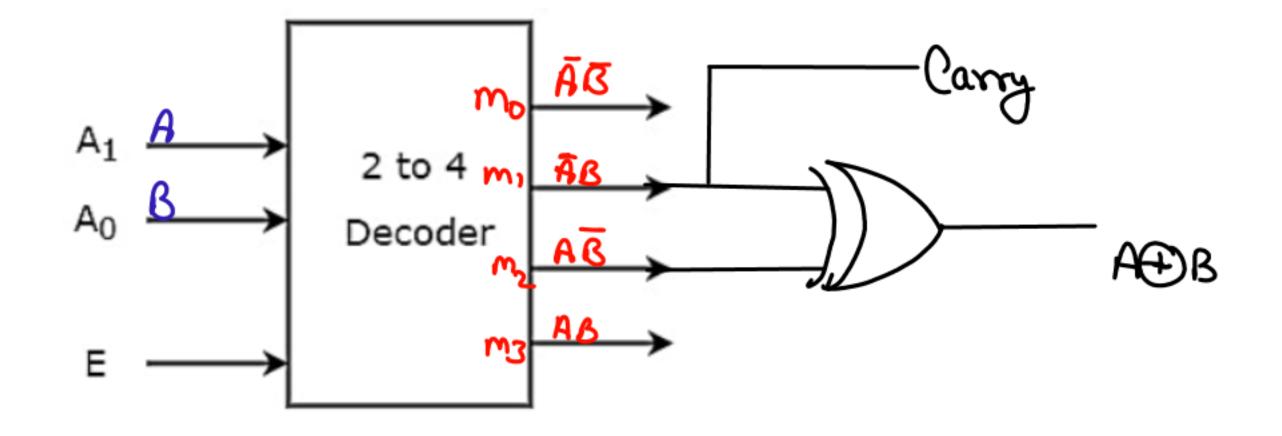


# Half Adder using Decoder



Sum = 
$$A \oplus B = AR + \overline{AB}$$
  
Carry =  $AB$ 

# Half Subtractor using Decoder



difference = 
$$A \oplus B$$
  $\rightarrow$   $A B + \overline{A}B \Rightarrow$   $\sum m(1, 2)$   $\sum m(1, 2)$   $\sum m(1)$ 

full adder -- mintern tourn Subtractor Sop

## Implementing the function using Decoder

To implement a function using decoder following steps we have to follow:

- 1. Connect function variables to the select lines (input variables) Address & hout
- 2. Convert the output into Canonical SOP form
- 3. Connect all the output to the corresponding minterms using OR gates.

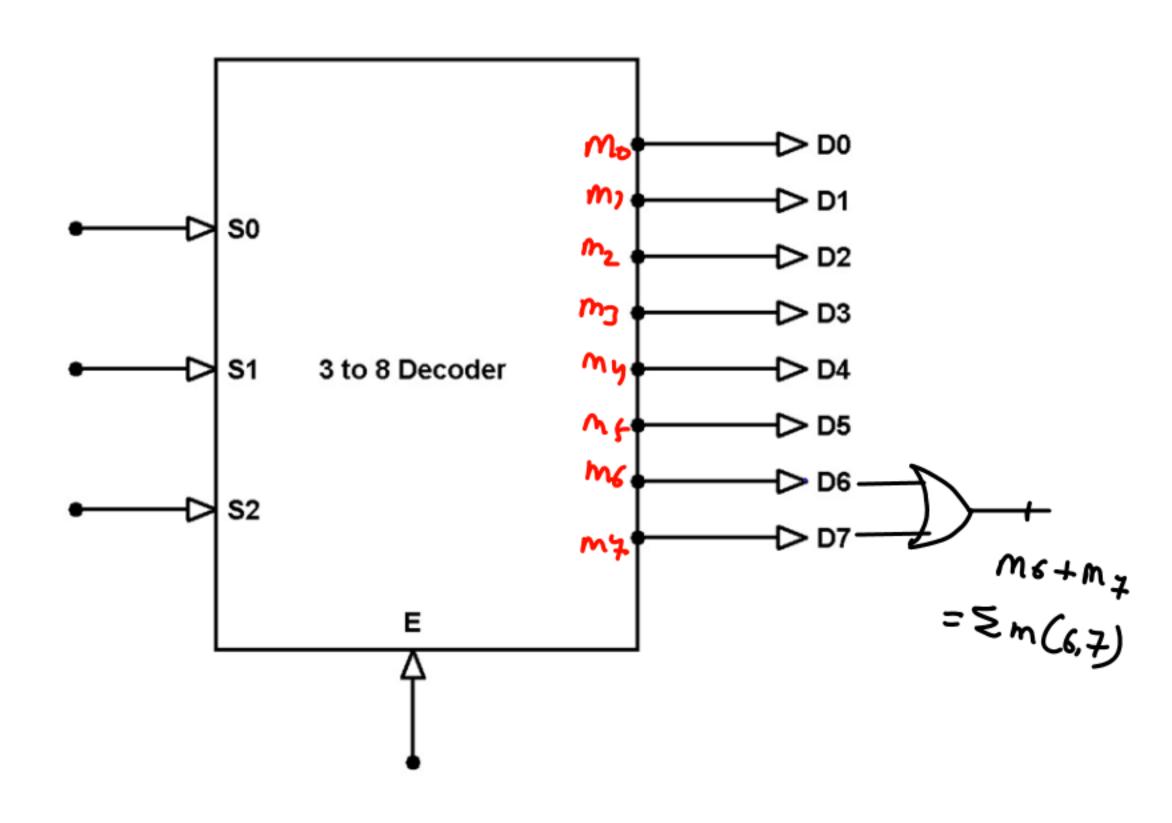
$$f(A,BC) = AB(C+\overline{c})$$

$$= ABC + AB\overline{c}$$

$$J_{111}$$

$$I_{110}$$

$$f(ABC) = \sum_{m} m(6,7)$$



Example: 
$$f(A,B,C) = A+BC$$
 Simplified

A B C BC A

BC (A+A)

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B C

A B

