DPP on Logic Gates

Which of the following Boolean expressions is equivalent to a NOR gate?

A. $\overline{A} + \overline{B}$

B. $\overline{A + B}$

C. $\overline{A} \cdot \overline{B}$

D. $\overline{AB}$

$\overline{A+B} \rightarrow \overline{A} \cdot \overline{B}$

↓

NOR

The simplified Boolean expression for the logic function:

$$F = A\overline{B} + A\overline{B} + \overline{A}B$$

$A \oplus B + AB$

A. $AB + A\overline{B}$

B. $A + B$

C. $A \oplus B + A$

D. $A + B\overline{A}$

$A(B+\overline{B}) + \overline{A}B$

$A + \overline{A}B$ ← RLR

$A + \overline{A}B = A + B$

Q3. Consider the function. The minimum number of 2-input logic gates needed to implement this function using only NAND gates is:

$$F = AB + \overline{A}C$$

2 NAND → AND

1 NAND → NOT

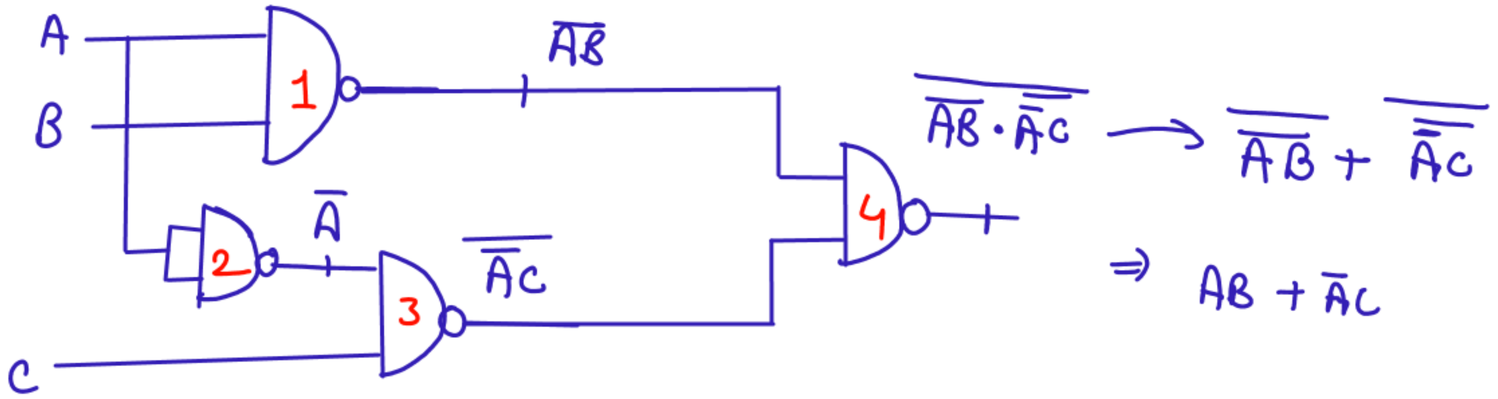
$\overline{A \cdot B} = \overline{A} + \overline{B}$

A. 4

B. 5

C. 6

D. 8

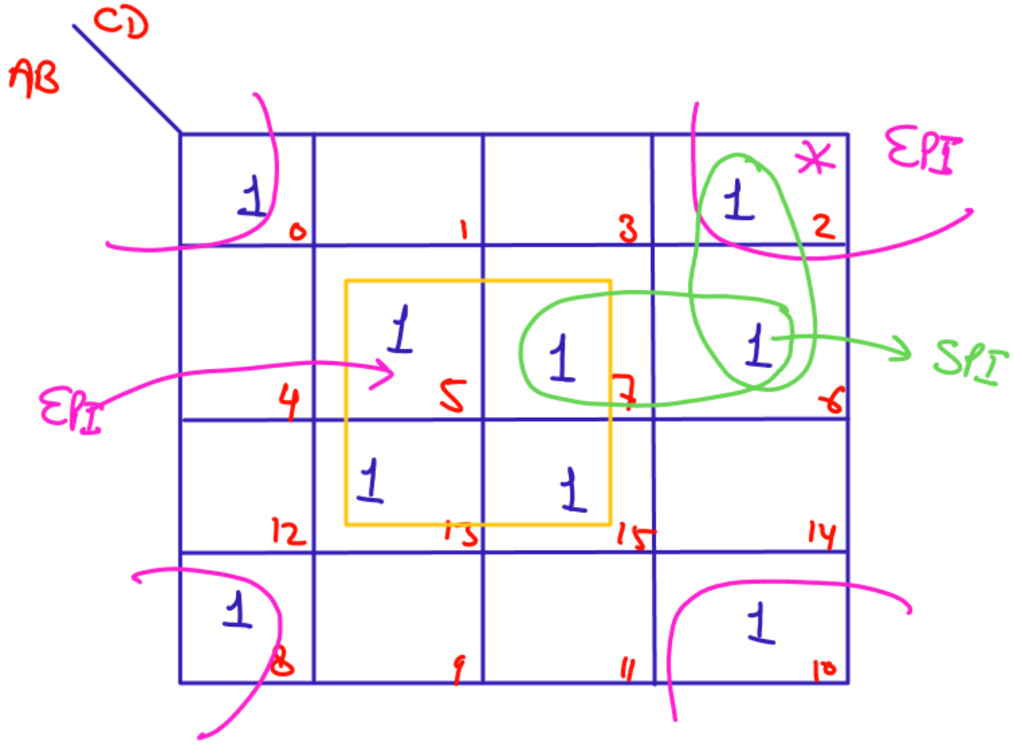


Q4. A function F(A,B,C,D) is given as:

$$F = \sum m(0, 2, 5, 6, 7, 8, 10, 13, 15)$$

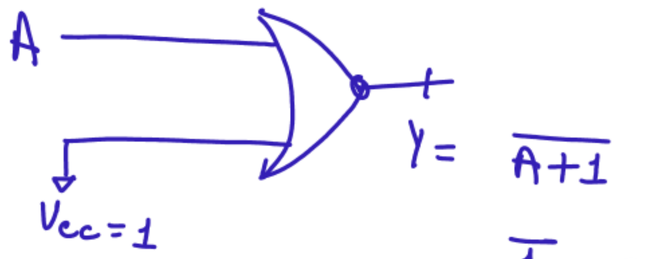
What is the number of essential prime implicants in the minimal SOP?

~~A. 2~~
B. 3
C. 4
D. 5



Q.5. A 2-input NOR gate has one of its inputs permanently stuck at 1. What is the output for any possible input combination?

A. Always 0
B. Output behaves like a NOT gate
C. Output equals the other input
D. Always 1

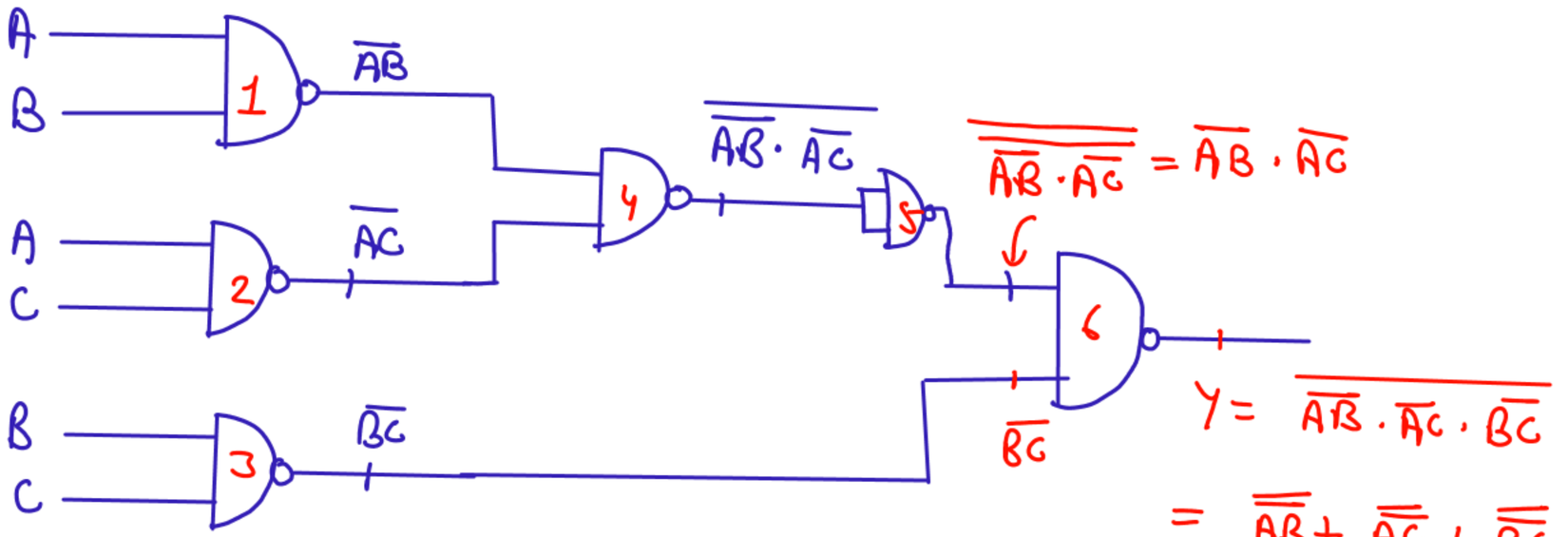


Q6. What is the minimum number of 2-input NAND gates required to implement a 3-input majority function:

↳ NON Associative

$$F(A, B, C) = AB + AC + BC$$

A. 5
~~B. 6~~
C. 7
D. 8

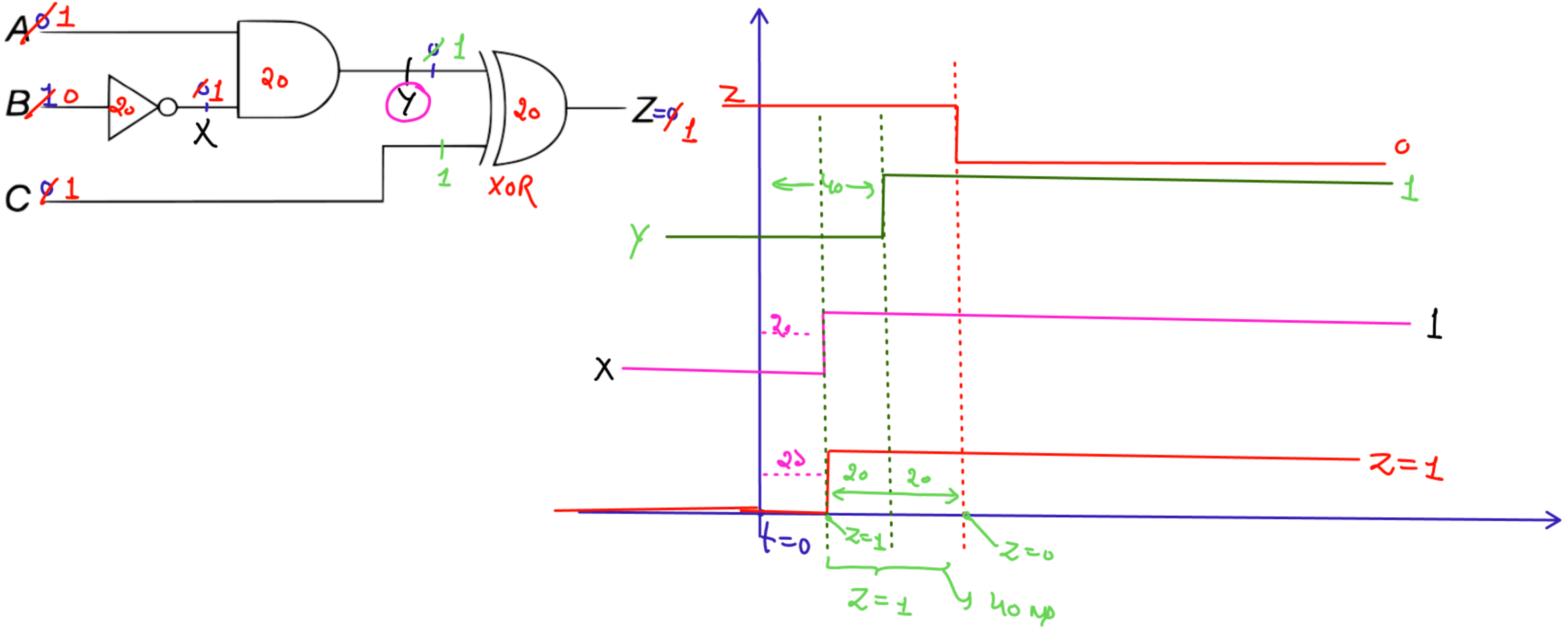


Q.7. Time required by signal to receive after it's been sent is referred to as _____.

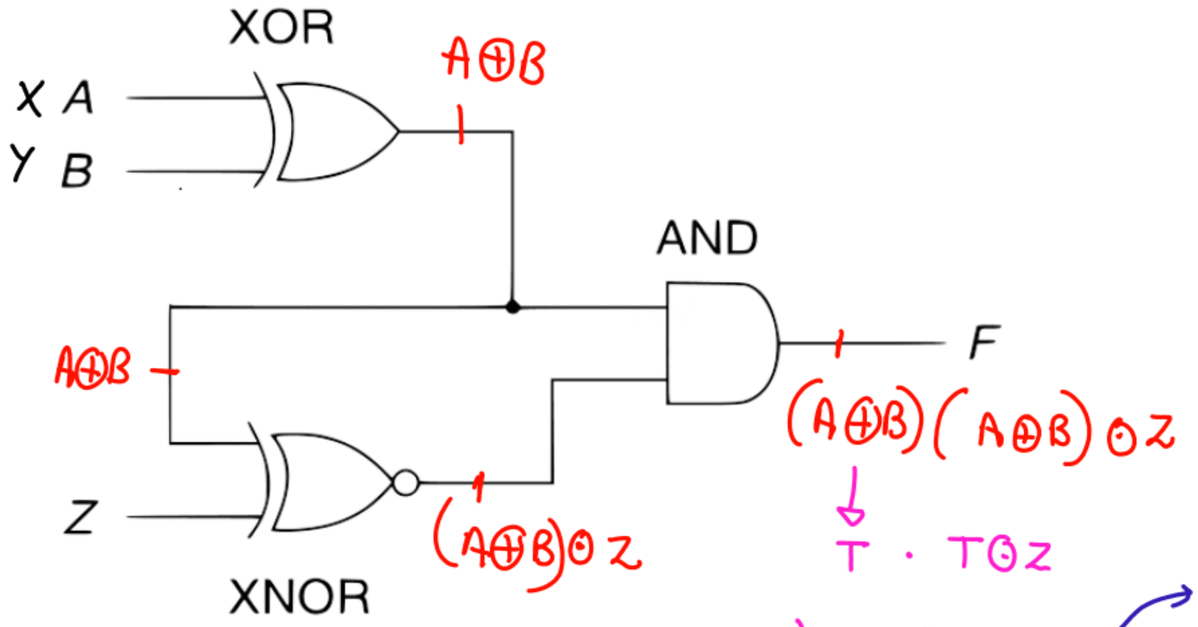
Logic Gate

a) Time Delay
b) Phase Delay
c) Propagation Delay
d) Angular Delay

Q.8. All the logic gates shown in the figure have a propagation delay of 20 ns. Let A = C = 0 and B = 1 until time t = 0. At t = 0, all the inputs flip (i.e., A = C = 1 and B = 0) and remain in that state. For t > 0, output Z = 1 for a duration (in ns) of 40 ns.



Q.11. The output F in the digital logic circuit shown in the figure is:



(A⊕B)(A⊕B)⊙Z

↓

T · T⊙Z

⇒ $T \cdot \overline{T \oplus Z}$

let A⊕B = T

$A \cdot \overline{A \oplus B} = A \cdot B$

= T · Z

Z(A⊕B)

$Z(A\bar{B} + \bar{A}B)$

$= A\bar{B}Z + \bar{A}BZ$

$X\bar{Y}Z + \bar{X}YZ$

A. $F = \overline{X}YZ + X\overline{Y}Z$

B. $F = \overline{X}YZ + X\overline{Y}Z$

C. $F = \overline{X\overline{Y}}Z + XYZ$

D. $F = \overline{\overline{XYZ} + XYZ}$

$$A \cdot \overline{A \oplus B} = AB$$

$\overline{A \oplus B} = \overline{A\bar{B} + \bar{A}B}$

↓ De morgan's law

$\overline{A\bar{B}} \cdot \overline{\bar{A}B}$ De-morgan's law

↓

$= (\bar{A} + B)(A + \bar{B})$

Multiply $\overline{A \oplus B}$ by A

$A \cdot \overline{A \oplus B}$

$A \cdot (\bar{A} + B)(A + \bar{B})$

$\cancel{A\bar{A}} + AB(A + \bar{B})$

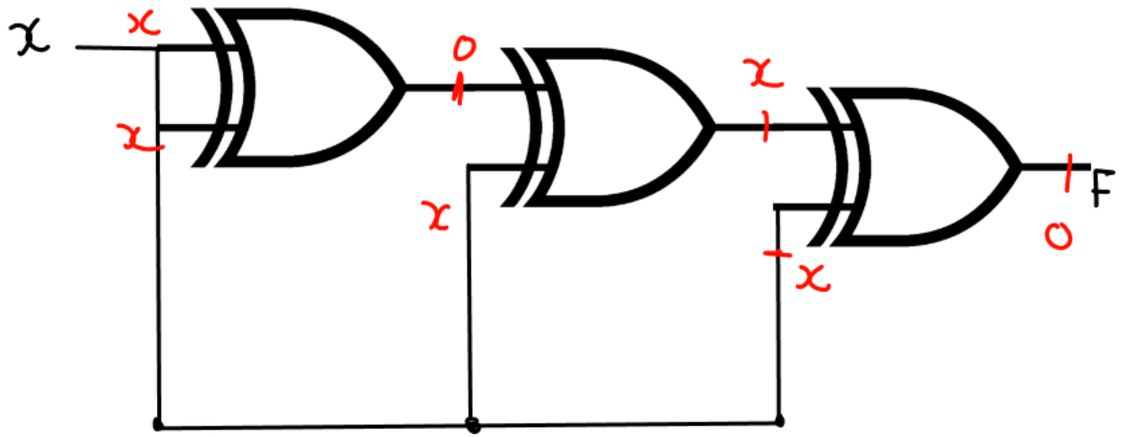
$AB(A + \bar{B})$

$AAB + AB\bar{B}$

$AB + 0$

$= AB$

For the circuit shown below the output F is given by:



$x \oplus x = 0$

$X \oplus 0 = x$

a) F = 1
b) F = 0
c) F = X
d) F = X'

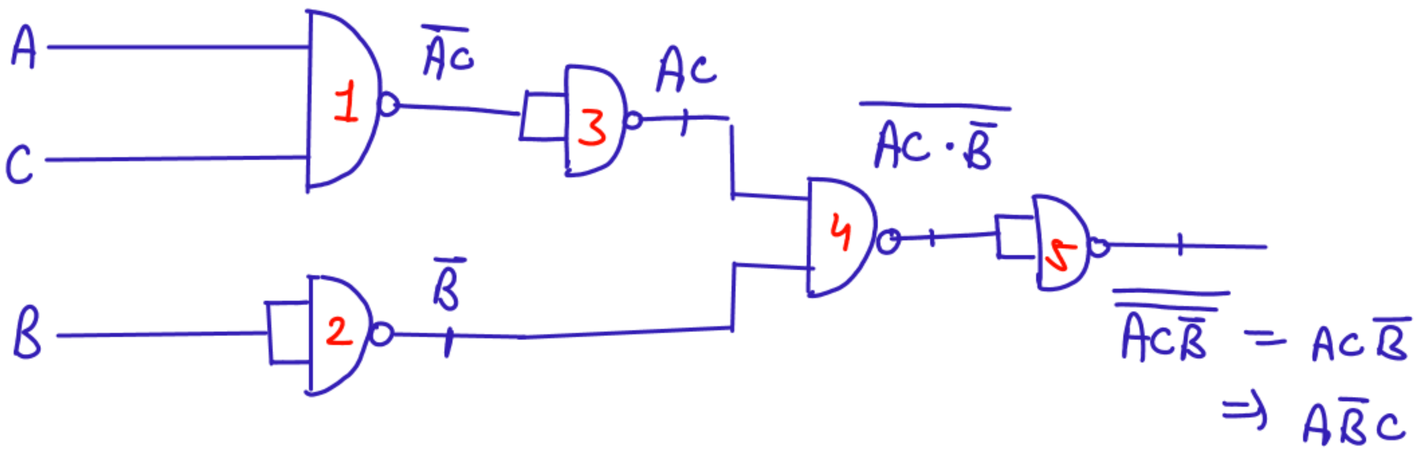
The number of two input NAND gates required to implement the boolean function Z = A B' C assuming that A,B and C are available, is:

A) Two

B) Three

C) Five

D) Six



A ring oscillator of 5 inverters is running at a frequency of 1.0MHz. The propagation delay per gate is _____.

$t = \frac{1}{f}$

time Period = $2n t_{pd}$

$2 \times 5\, t_{pd} = 10 t_{pd}$

$10 t_{pd} = \frac{1}{10^6} \Rightarrow \frac{1}{10 \times 10^6} = \frac{1}{10^7}$ Sec

$\Rightarrow 10^{-7}$ Sec $\Rightarrow$ 0.1 μs

$\frac{1}{10 \times 10^6}$ sec $\Rightarrow 0.1 \times 10^{-6}$ Sec

$= 0.1$ μs

1 KHz = 1000 Hz

1 MHz = 1000 KHz

1 MHz = 10^6 Hz

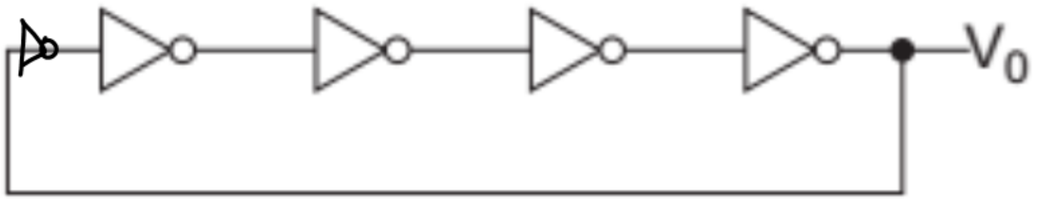
1 GHz = 1000 MHz

1 Sec = 1000 ms

1 ms = 1000 μs

1 Sec = 10^6 μs

For the ring oscillator shown in the figure, the Propagation delay of each inverter is 100 pico second. What is the fundamental frequency of the oscillator output?



No. of Inverters = 5

$T = 2n t_{pd}$

$2 \times (5 \times 100) = 1000$

$f = \frac{1}{t} = 1000 \times 10^{-12}$

$= 10^3 \times 10^{-12} = 10^{-9}$

$= 1\,GHz$

1 sec = 1000 ms

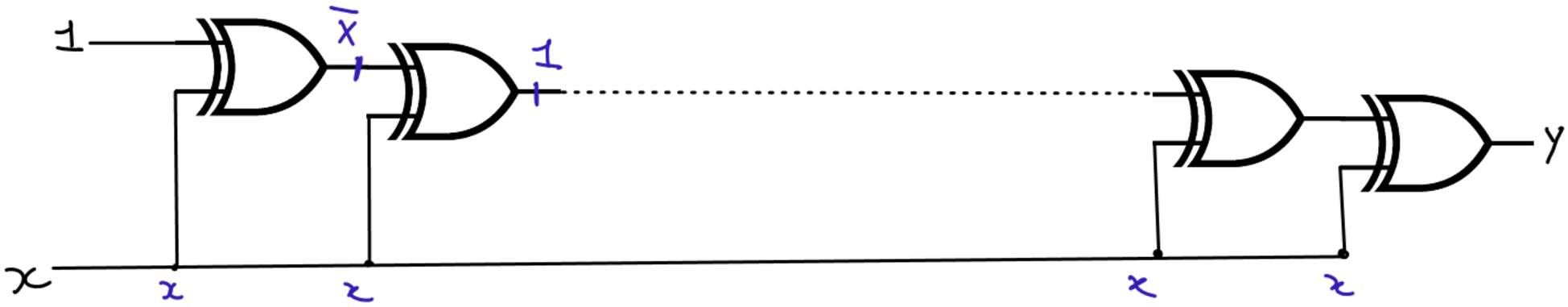
1 ms = 1000 μs

1 μs = 1000 ns

1 ns = 1000 pc

1 sec = 10^{-12} pc

If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is X then the output Y is equal to?



A) 0
B) 1
C) X'
D) X

$x \oplus 1 = \bar{x}$

$x \oplus \bar{x} = 1$

x after 2 logic gates o/p = 1 ↓ Same as input

then after 20 xor gates = 1

A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of sqitching of the bulb resembles.

A) an AND gate
B) an OR gate
C) an XOR gate
D) a NAND gate

G.F
↳ Switch 1 = ON
Switch 1 = off

← Inequality Detector
↓
XOR
=

F.f.
↳ Switch 2 = off — Bulb = ON
Switch 2 = ON → Bulb = ON

⇒ Next Session

↳ Boolean Algebra
- theorems
- K-Maps