- ✓ Unit 01 : Number System
  - Radix
  - Conversion of Radix
- ✓ Unit 02 : Data Representation
  - Types of Code
  - Representation of numbers in different format
    - 1's comp
    - 2's comp
- Unit 03 : Logic Gates
  - शुरुआत से

[foundation]

base 'n'

10 2

Logic Gate :

essential Requirement

'It is a basic building block of a digital Circuit, which is used to make all Logical Decisions'

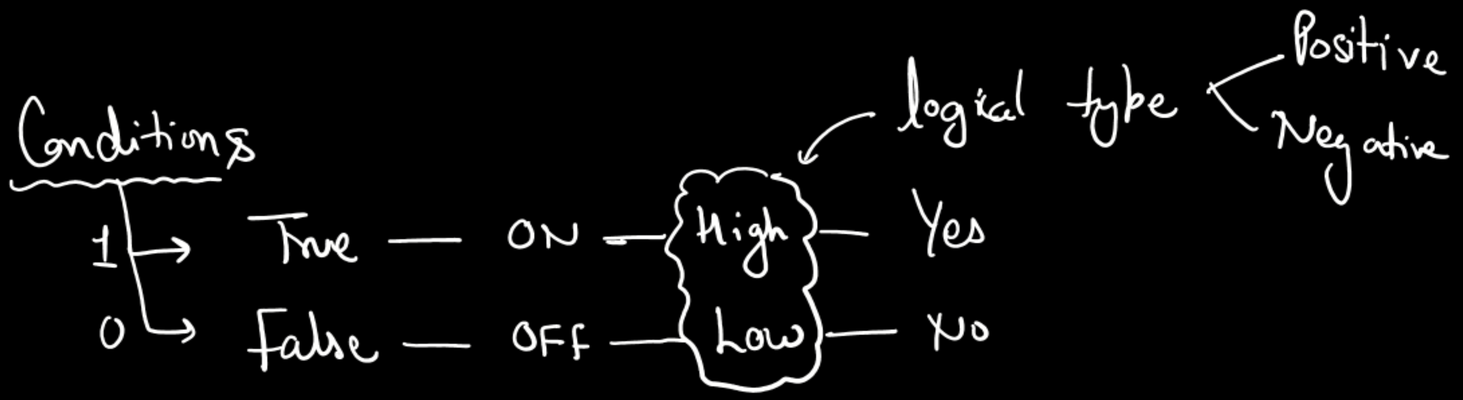
- digital → finite State
  Ex : Switch

following are the logic gates that are used to Create a logical Circuit

i) Buffer
ii) Inverter (NOT)
iii) AND
iv) OR
v) NAND
vi) NOR
vii) XOR
viii) XNOR

Logical Decision :

↳ Depends on Conditions



Positive Logic

True = True

1 = True 0 = false

High = True , Low = false

Logic 1 = 5v (True)

Logic 2 = 0v (False)

Negative Logic

1 = False 0 = True

High = False Low = True

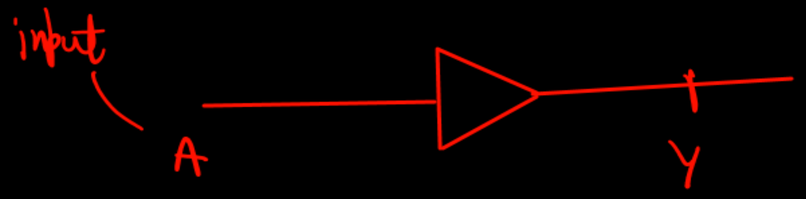
Logic 1 (5v) → False

Logic 2 (0v) → True

Switch = OFF है तो Bulb जलेगा

1) Buffer :

It has same output as input but it increases the signal Strength so that it can travel for longer Distance.



[input = output]

$Y = A$

A	Y
0	0
1	1

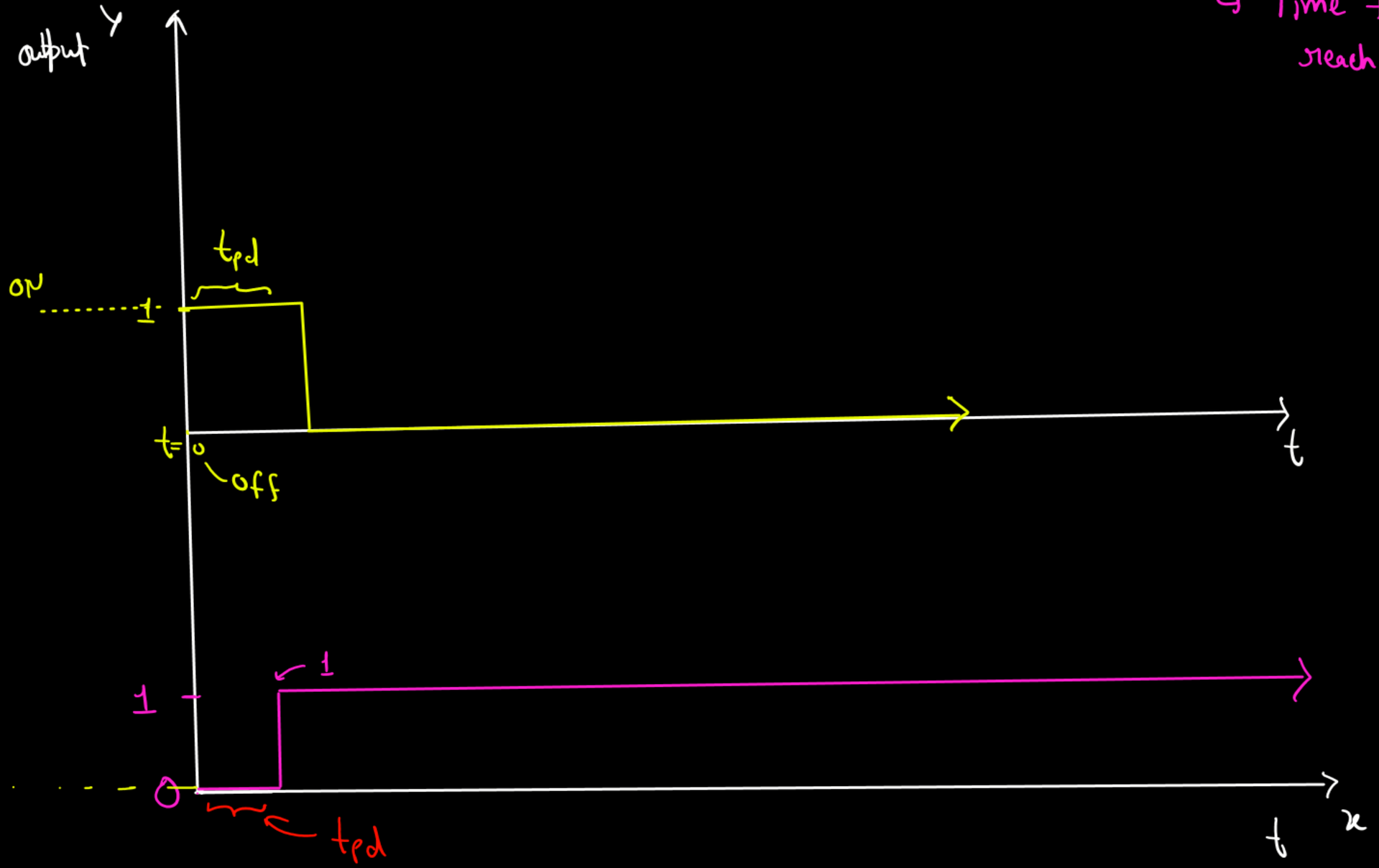
} Truth Table

⇒ **Truth Table** : It is a table that provides the output for each possible Combination of input.

Graph of Buffer Gate

t_{pd} = Propagation Delay

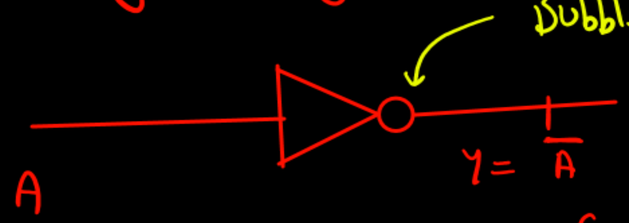
↳ Time taken by Input to reach the output through a gate



2) Inverter (NOT) (उलटा)

↳ It negates the logic [or we can say that it generates the Complement of input signal]

→ Negative Logic



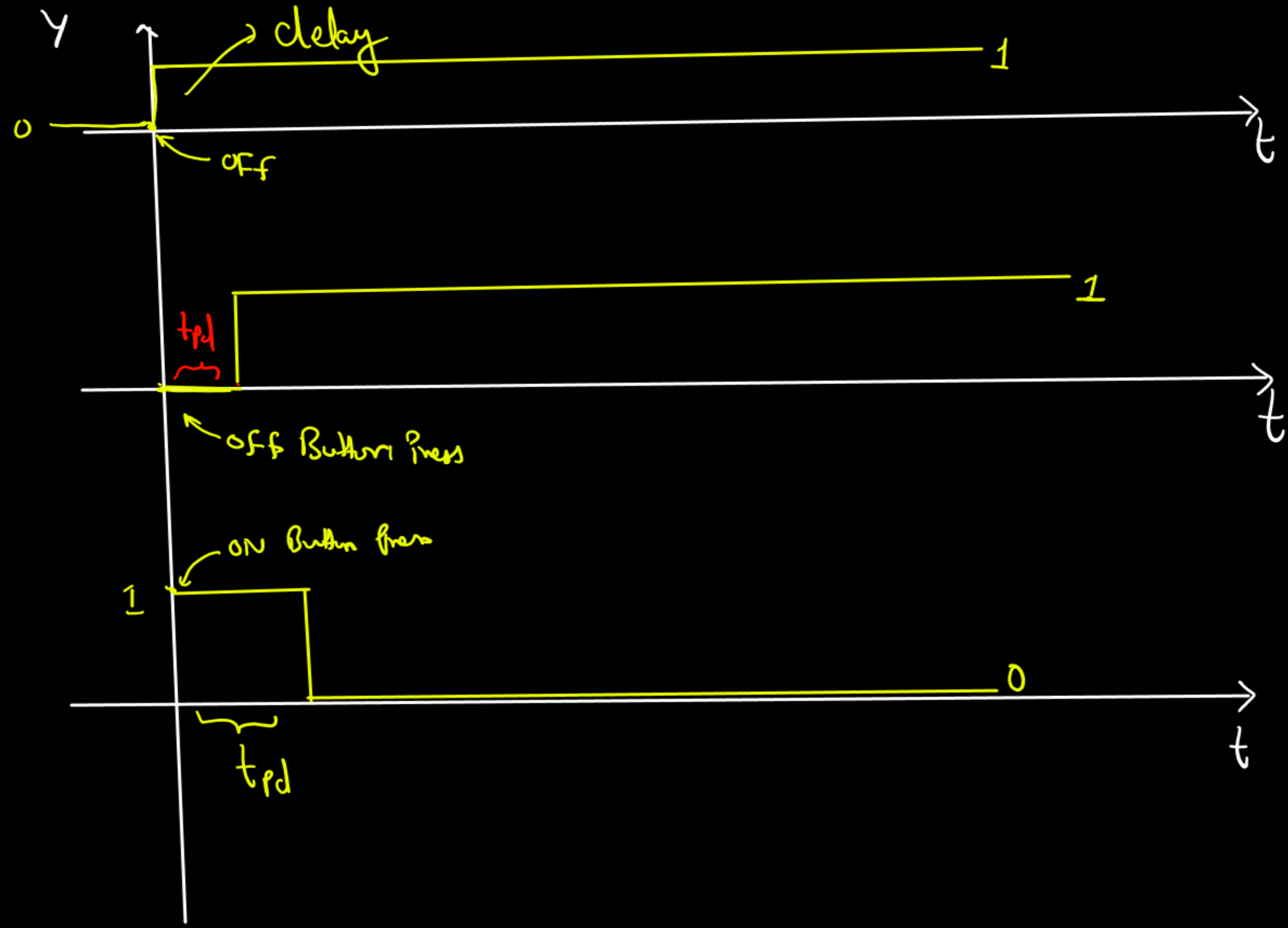
Truth Table

A	Y = $\bar{A}$
0	1
1	0

1 का 0
0 का 1

They are used to Complement the logic

Graph of NOT Gate:



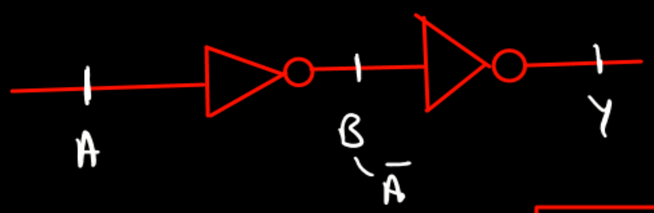
Cascading of Inverter :

जोड़ना (एक के बाद एक)

$B = \overline{A}$

$Y = \overline{B} = \overline{\overline{A}} = A$

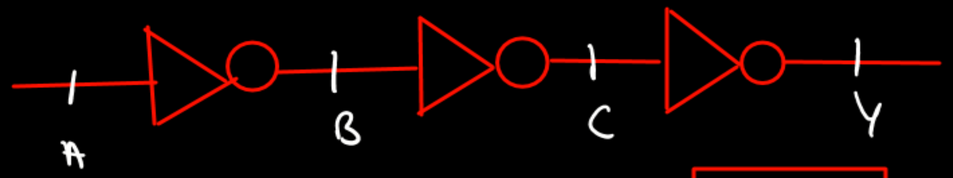
$\boxed{Y = A}$



A = 0	B = 1	Y = 0
A = 1	B = 0	Y = 1

input = output : Buffer gate

* If we Cascade 2 Inverters in a series then it will Act like a Buffer



$B = \overline{A}$
$C = \overline{B}$
$Y = \overline{C}$
$\Big\} \; Y = \overline{A}$

A = 0	B = 1	C = 0	Y = 1
A = 1	B = 0	C = 1	Y = 0

output is Complement of Input ⇒ $\boxed{Y = \overline{A}}$ ← Inverter

* If we Cascade 3 inverters in a series then it will act like an Inverter

Observation :

↳ if even number of NOT gates are Connected in Cascade then it behaves like a buffer.

→ But it generates a delay of $2n$ t_{pd}

↳ if odd number of NOT gates are Connected in Cascade then it behave like an inverter

→ But it generates a delay of $2n+1$ t_{pd}