RUIHONG YIN

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EDUCATION

University of Washington *2021.9-2023.6(expected)*
Master of Science in Electrical & Computer Engineering **Cumulative GPA:3.8**

University of Liverpool *2019.9-2021.6*
Bachelor of Engineering in Electrical and Electronic Engineering **First Class Honours**

Xi'an Jiaotong-Liverpool University *2017.9-2019.6*
Bachelor of Engineering in Electrical and Electronic Engineering

SKILLS SUMMARY

Digital System Design	Verilog/SystemVerilog, RTL design, Simulation and debugging, VCS, DVE
VLSI Design	Virtuoso, HSPICE, Spectre, Calibre, Experiences in TSMC65nm, Standard and custom cell layout, Logical Effort, Timing and Metastability, Power Gating
VLSI automation tool	Synopsys Design Compiler, IC Compiler II, DRC, LVS, STA
Programming and Scripting	linux/bash, C/C++, git, python, TCL, Matlab, Arduino, Raspberry Pi

EXPERIENCE

JTAG Interface with Boundary Scan Register 2022.6-Present
University of Washington Graduate Student Research Assistant

- Part of UW VLSI lab project advised by Prof. Visvesh Sathe
- Wrote **JTAG** interface with Boundary Scan Register with SystemVerilog and verified using **cocotb** python verification framework, then create their assertions
- Did the **post-synthesis** simulation, **post-APR simulation** and functional verification by cocotb.
- Turned DFF in Boundary Scan Register into scan cell and **inserted scan chains** in the design.
- Wrote a technical document for this JTAG interface

RISC-V pipeline processor with Cache 2022.7-Present
University of Chinese Academy of Sciences Developer

- Aimed to design a RISC-V pipeline processor equipped with Cache and support **RV64IM**,and run the real game Legend of Sword and Fairy on the small operating system.
- Designed a single-cycle processor that supports RV64IM and implemented an RV64IM simulator using **C language**.
- Added I/O for single-cycle processors, implemented the UART and RTC peripheral in **emulation environment** and run Super Mario

PROJECTS

ASIC Implementation of Local Feature Detector in ORB SLAM3 2022.4-2022.6

- Employed a **Sliding windows** structure of a patch size 7 × 7 using **FIFO**,and providing access to a moving widow of pixels that iteratively covers every position of the image
- Used **multi-stage pipeline** to compute the pixel differences, compare the threshold, then using ANDs tree to computed corner point's score
- A 3×3 Sliding Window is used to filter the FAST features by achieving **NMS** (Non Maximum Suppression)
- Did the **post-synthesis simulation** and the **placing and routing** using IC Compiler and the performance of this proposed hardware is **250MHz**

Simulation & Synthesis of Ibex CPU Core 2022.2-2022.3

- Simulated and verified the Ibex processor core, tried to achieve 100% **code coverage** using VCS's coverage analysis tool.
- Did **synthesis** of the processor core using Synopsys' DC and confirmed there is no slacks.
- Performed floor-planning, placing and routing using , **IC Compiler II**, to generate a production-quality **GDSII file**.

Full Custom Design of Schematic & Layout of a 16-bit ALU using Sklansky Adder in 65nm CMOS 2021.11-2021.12

- Adjusted logic gate size based on **logical effort** to minimize delay.
- Used gate sharing between the adder and bitwise operations to minimize layout area and optimize power.
- Concluded that maximum delay and energy in post-layout simulations are 470ps and 2.45pJ, respectively, which is the second place in class.