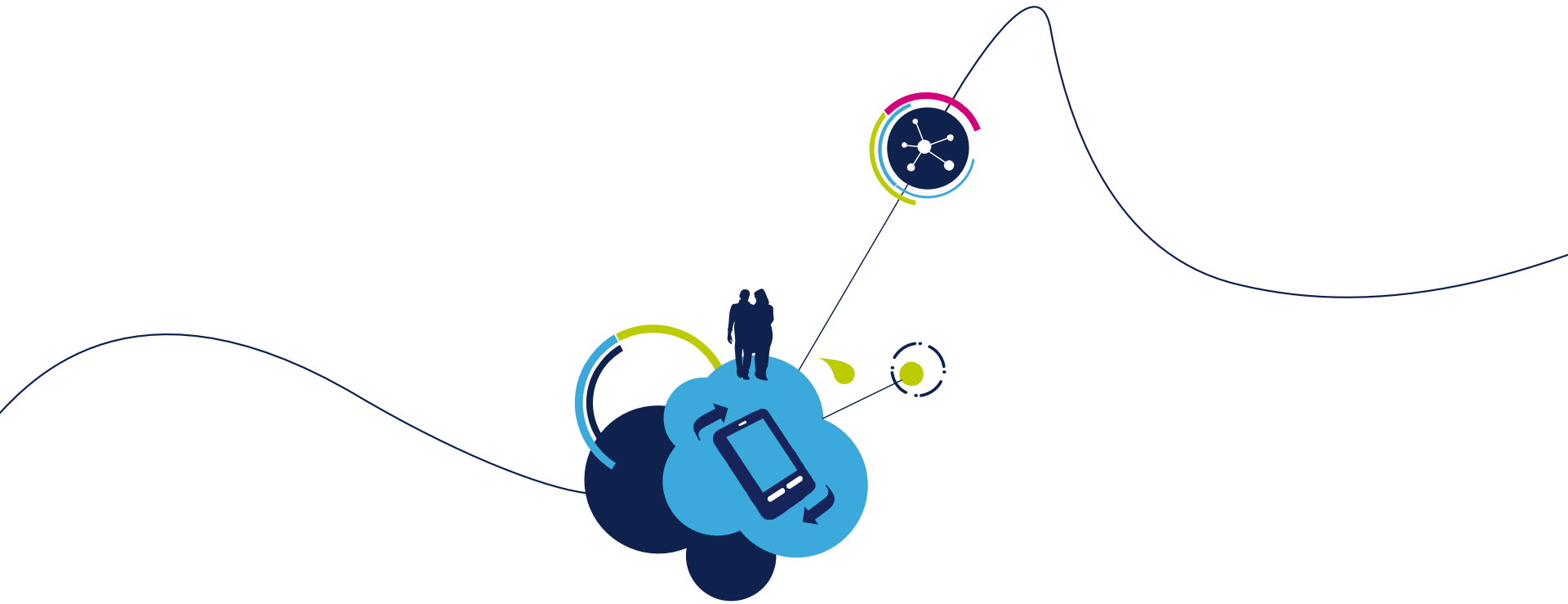




# STLUX385A in primary side controlled LED applications

Using STLUX385A on primary side  
control single 100W LED channel

STEVAL-ILL066V1



# Primary side controlled LED driver

# Target application

3

- Street lighting and Tube replacement
  - Wide-range input
  - Single string output (100V or 200V max.)
  - 100W maximum output power - down to 1W
  - 1 A maximum output current - down to 10mA (500mA on 200V version)
  - DALI interfaces on board - IEC62386-102-207 LED ed. 1.0 (ed. 2.0 in preparation)
  - Insulated 0-10 V interface alternative to DALI.



# Board Characteristics

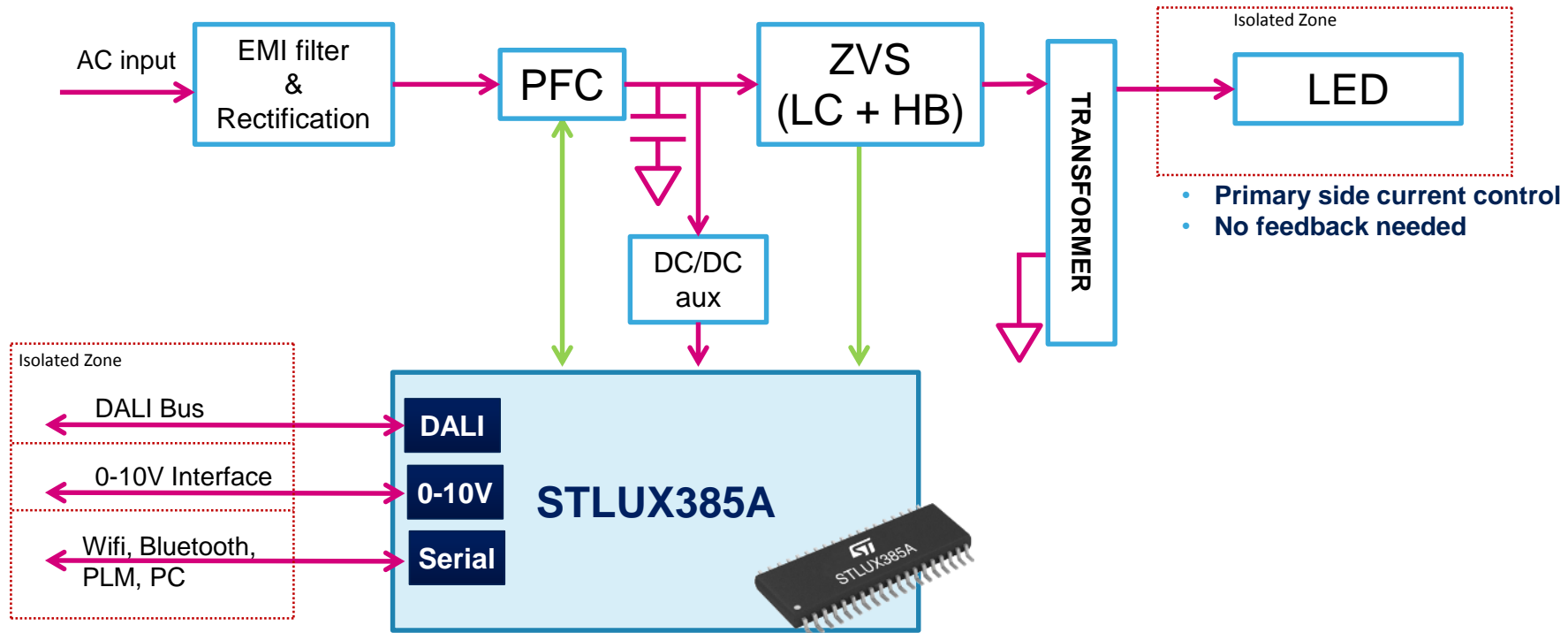
4

- Input: 90~265 Vac
- Output: 100 V - 1 A max [ 200 V – 500mA] (100W)
- Current precision: better than 5% from 50W to 100W output
- Control line: by Serial and DALI bus (Opt: isolated 0-10V)
- Power efficiency: more than 92%
  
- Digitally controlled single chip solution for: PFC+LC+DALI
- Primary side regulation of LED current
- Extremely low power when output LED are turned off by DALI command (lower than 250 mW)
- Operating temperature from -40 to +105°C
  
- Two Layers PCB
- Dimension - 270x50x35 mm (LxWxH)

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# Block schematic

5



## • Key products

- **STLUX385A digital controller**
- STF18N60M2 (PFC stage)
- STD13N60M2 (ZVS stage)
- PM8841/51D (PFC driver)
- VIPer06XS (aux DC/DC)
- L6388ED (ZVS driver)

## • STLUX385A signals:

- Input voltage for  $U_{Vlo}$  & startup
- PFC output voltage for loop regulation
- PFC gate driving signal
- ZVS resonant current for control loop, output voltage for protection
- ZVS HB and relevant dimming control signals
- DALI frame – interpreter, response and execution

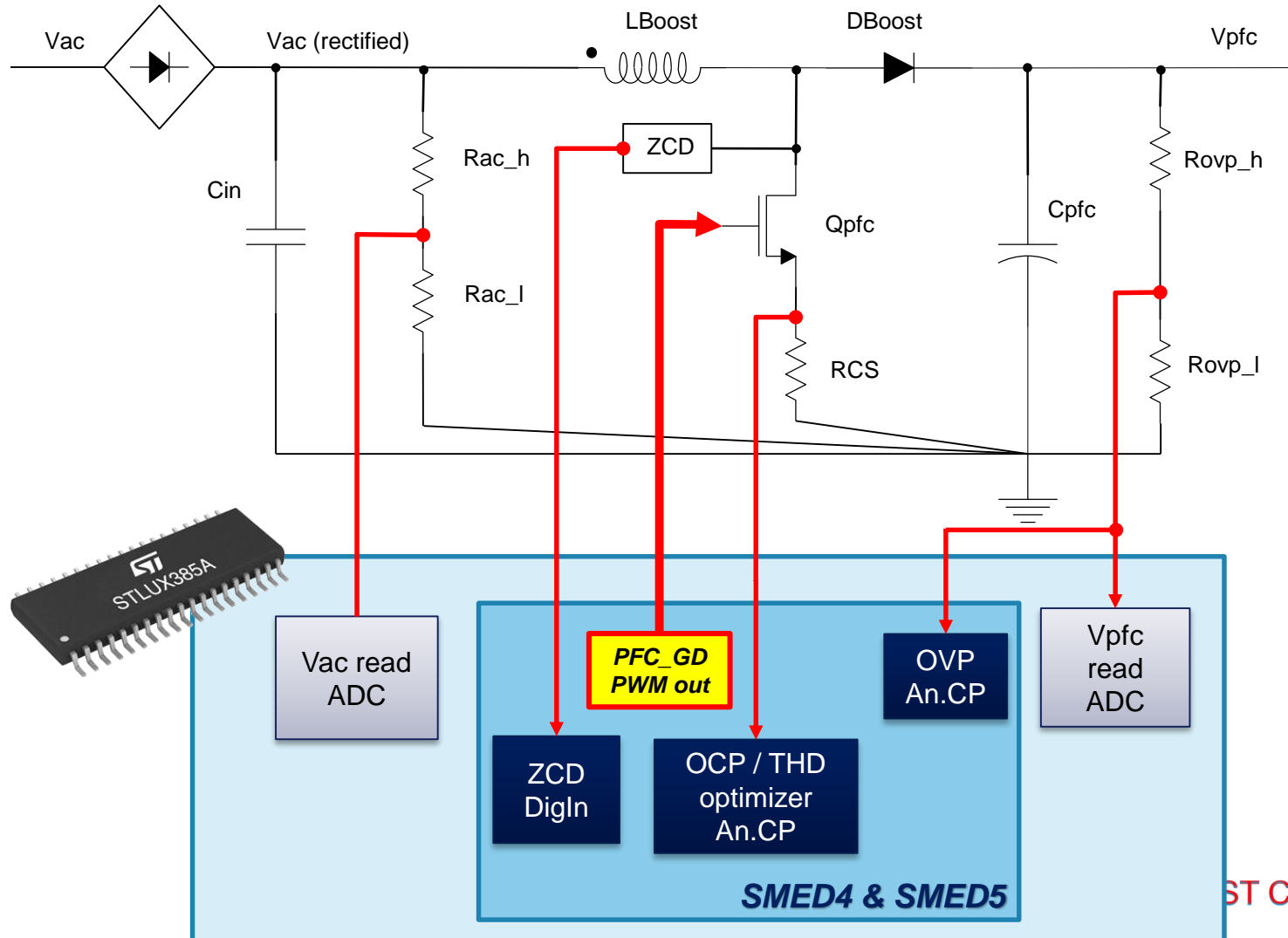
## • Secondary components:

- Rectifier and capacitor (no extra active components)

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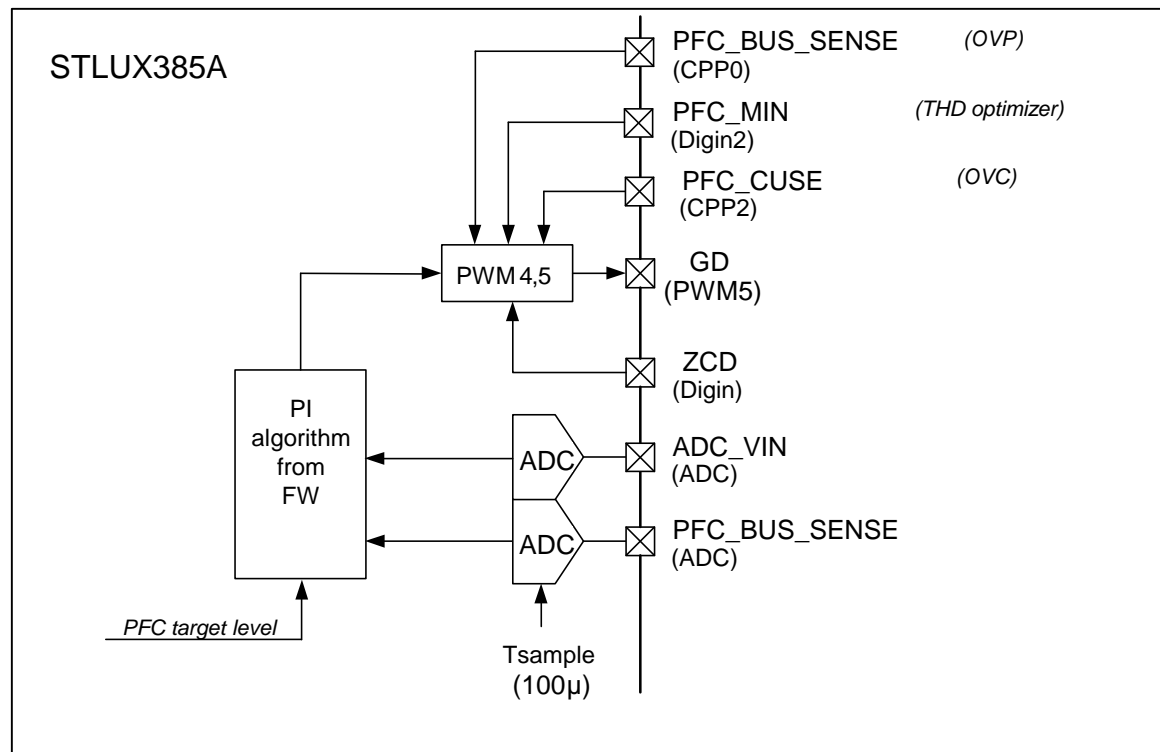
# PFC - Schematic

6



# PFC - Physical connection

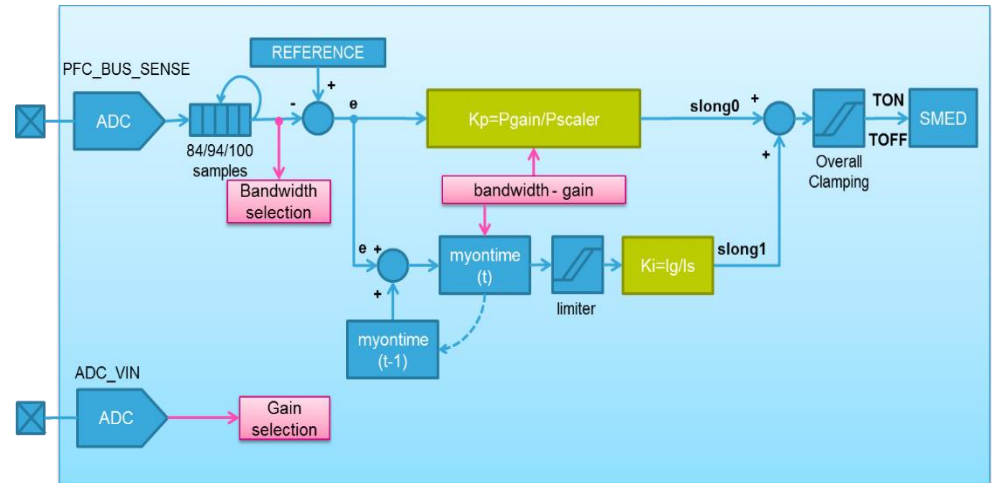
- CPP0 - OVP protection
- DIGIN2 - THD optimizer
- CPP2 - OVC protection
- DIGIN3 - ZCD sensing



# PFC - Implementation

8

- PFC - PI control mode
  - Transition Mode PFC
  - 10KHz PFC error acquisition
  - AC cycle regulation
  - Digital Programmable PI algorithm
  - Adaptable Error Gain
  - Internal compensation algorithm
  - Programmable output voltage

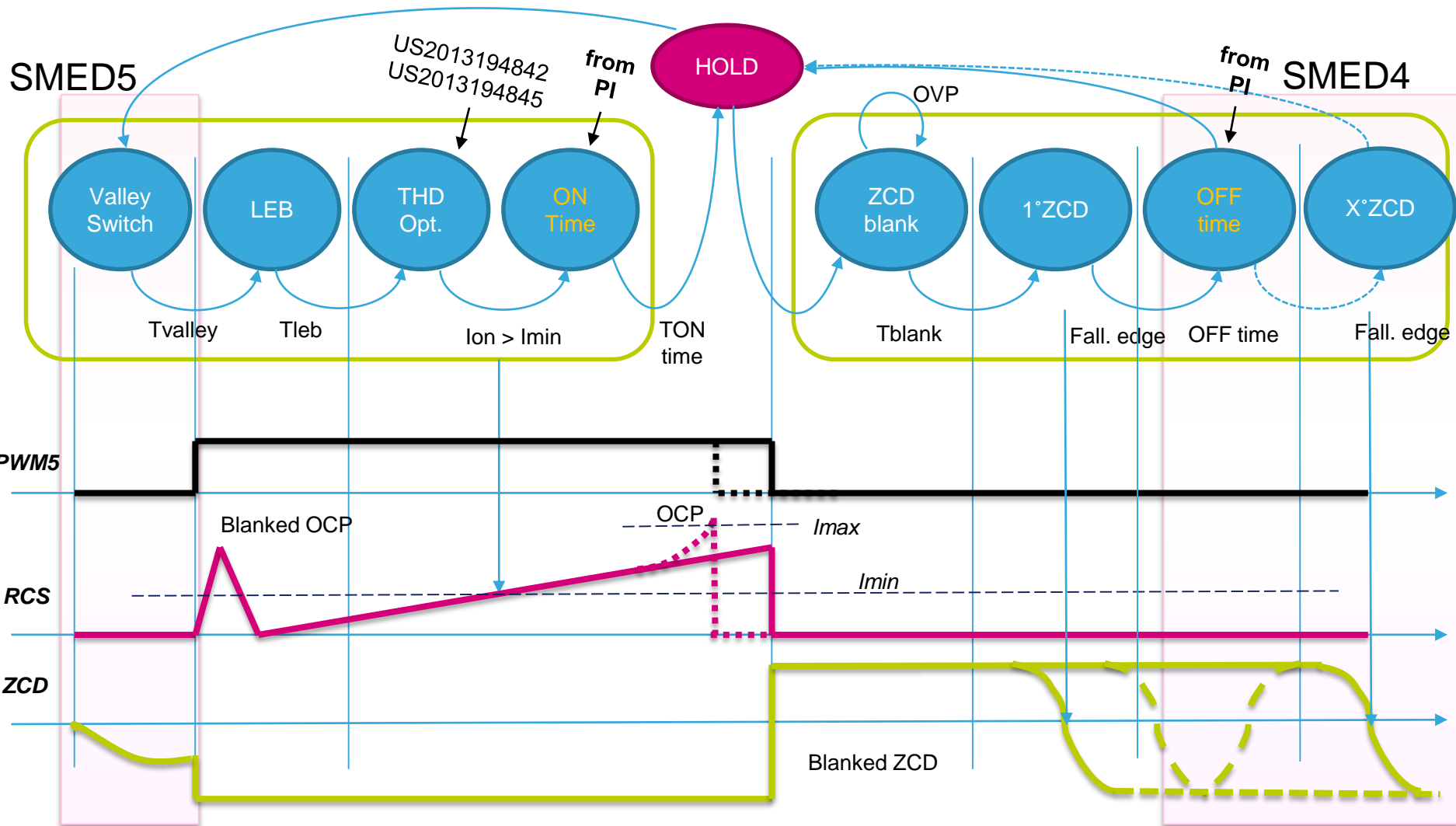


- Fast OVP (no FW intervention using SMED)
- Fast UVLO and Brownout protections (using SMED)
- Fast adaptable OCP protection (better max. output power limiting)
- Controlled start-up ramp



# PFC –implementation - SMED

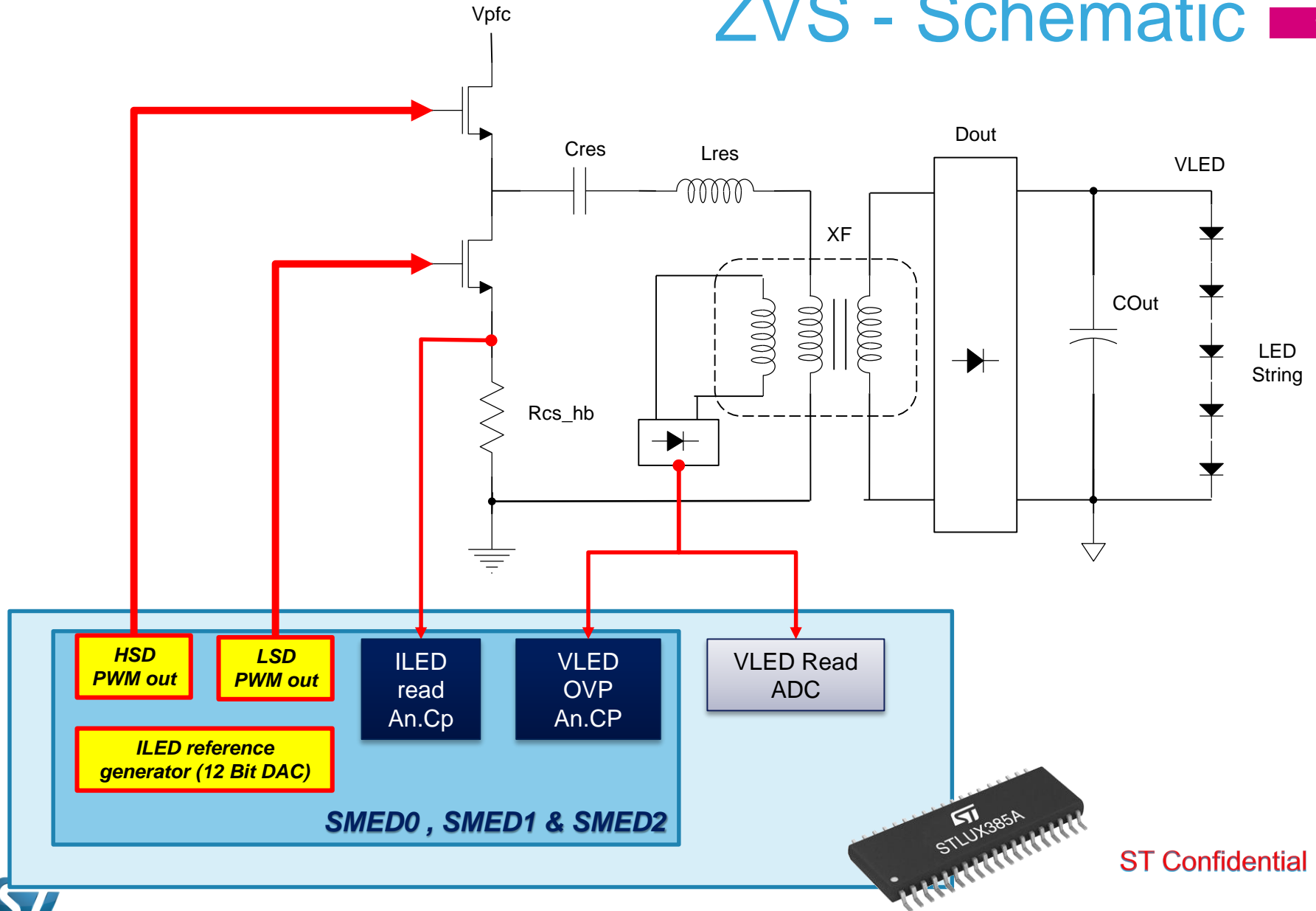
9



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# ZVS - Schematic

10

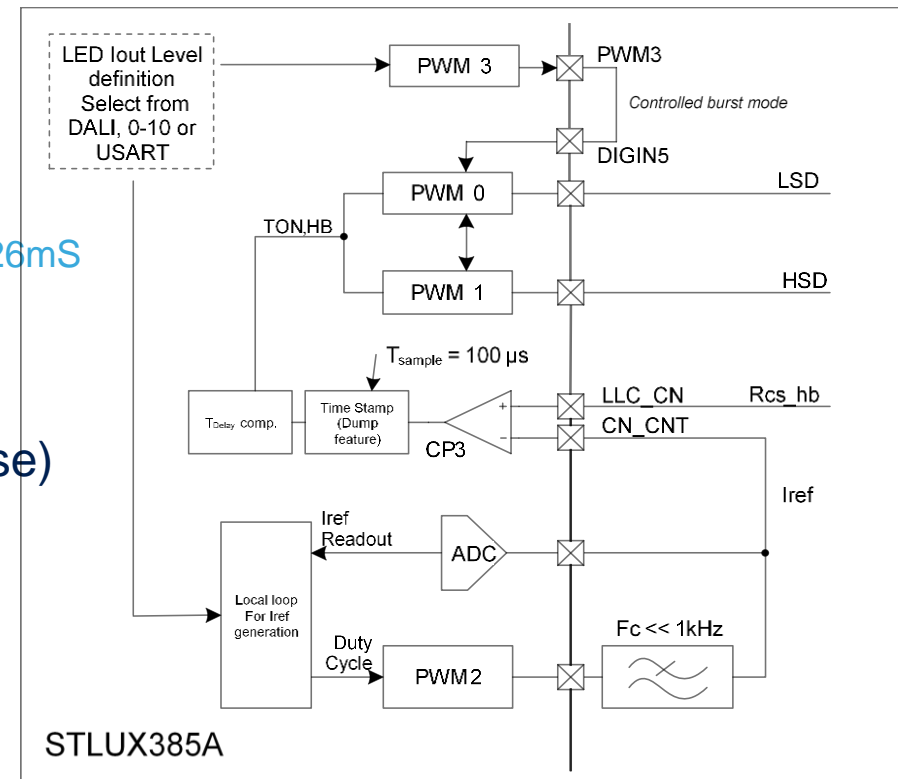


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# ZVS - Implementation

11

- Zero Voltage Switch – resonant LC topology
- Frequency range: from 70KHz to 350KHz
- Output LED current regulated by primary side (1 A to 10mA)
  - Primary current regulated by internal algorithm (12 bit resolving)
  - Loop regulation sampling time: 100uS
  - FW based Soft start
  - DALI 207 Fast Fade Time regulation less than 26mS
  - Innovative Algorithm to reduce the minimum current level
- Automatic ramping time (for DALI purpose)
- Output over-current protection
- Output short circuit protected
- Output no load protection



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# HB – Implementation - SMED

12

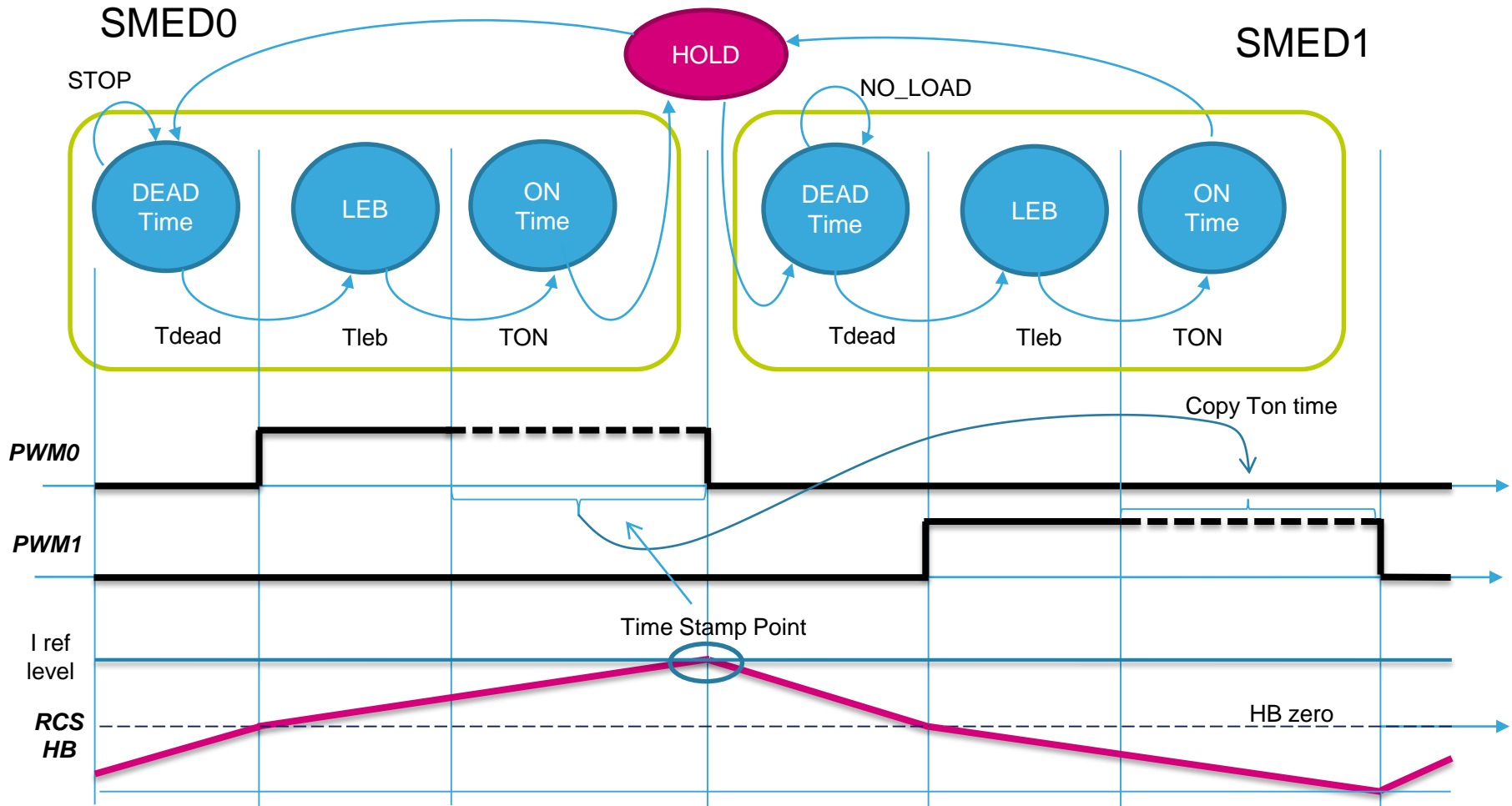


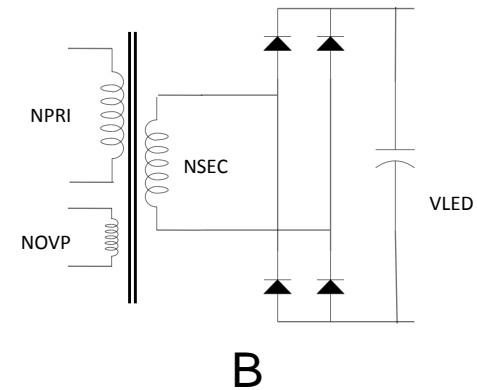
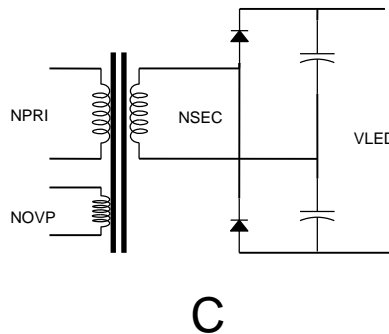
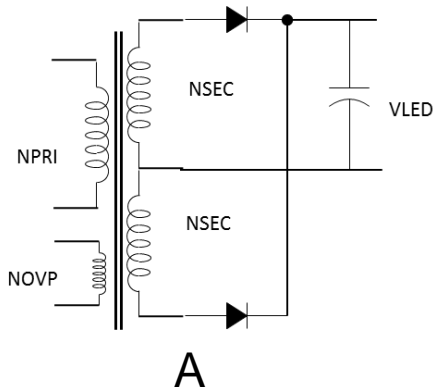
Figure not in scale

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# ZVS – Versions selection

13

- Using one of the two rectification networks the following versions can be selected without further FW / HW modifications:
  - A. 100 V – 1 A
  - B. 200 V – 0.5 A
  - C. 400 V – 0.25 A (not implemented into demo board)

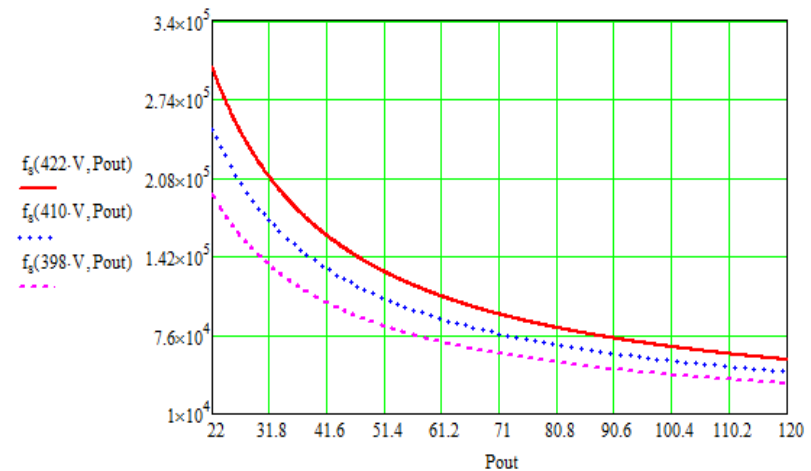


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# Output Power Variability

14

- Variation of output voltage and output current results into frequency variation
- Hyperbolic characteristics limits the minimum output power to roughly 40% of full power.
- Fixed output current / variable output voltage  
Fixed output voltage / variable output current applications are directly addressed.
- Innovative algorithm to address Variable Current and voltage or dimmable solutions is implemented.  
(min power down to <10% already reached)
- Flicker free analog dimming



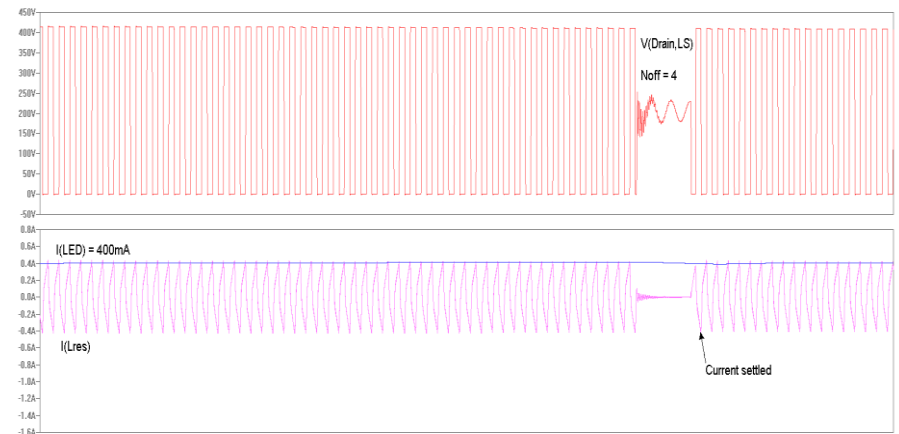
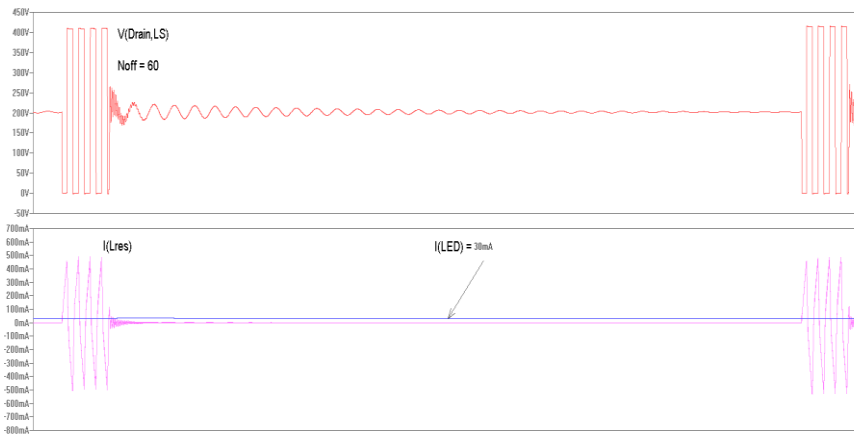
Patent: US 2015/0003117A1

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# Dimming algorithm

15

- Two operating regions are identified
  - **Peak current control area:**
    - To reduce the current starting from max current until a minimum noise-free current level is reached.
    - Resulting into variable frequency with different variation ranges depending on  $V_{out}$ .
  - **Skipping cycle area**
    - A number over a certain amount of HB cycles (currently 112) are skipped to further reduce the output current.
    - This set-up allows to obtain a minimum current lower than 10 mA (100 Vout)



Patent: US 2015/0003117A1

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# DALI - Implementation

16

- Manchester decoder by dedicated HW peripheral
  - Start – Stop – Staffing and de-staffing – Bit validation without FW intervention
  - 16 bit input register (available 24 bit) – 8 bit output register
  - Interfaces failure - 500mS timing by HW
- Dali protocol
  - IEC62386: 102 and 207 implemented (device type 6 – LED)
  - ed. 1.0 available, ed 2.0 under development (90% tests OK)
    - On IEC62386-102&207 ed 2.0 under development the implemented features are: short and open circuit detected, thermal shutdown and light reducing.  
Thermistor simulated by trimmer
    - Fast Fade time implemented (25mS lout start-up)
    - Output power management and control: planned
- Very low power consumption when DALI command “setup output LED off” is received:
  - Smart low power management with input voltage and DALI bus verification during low power mode

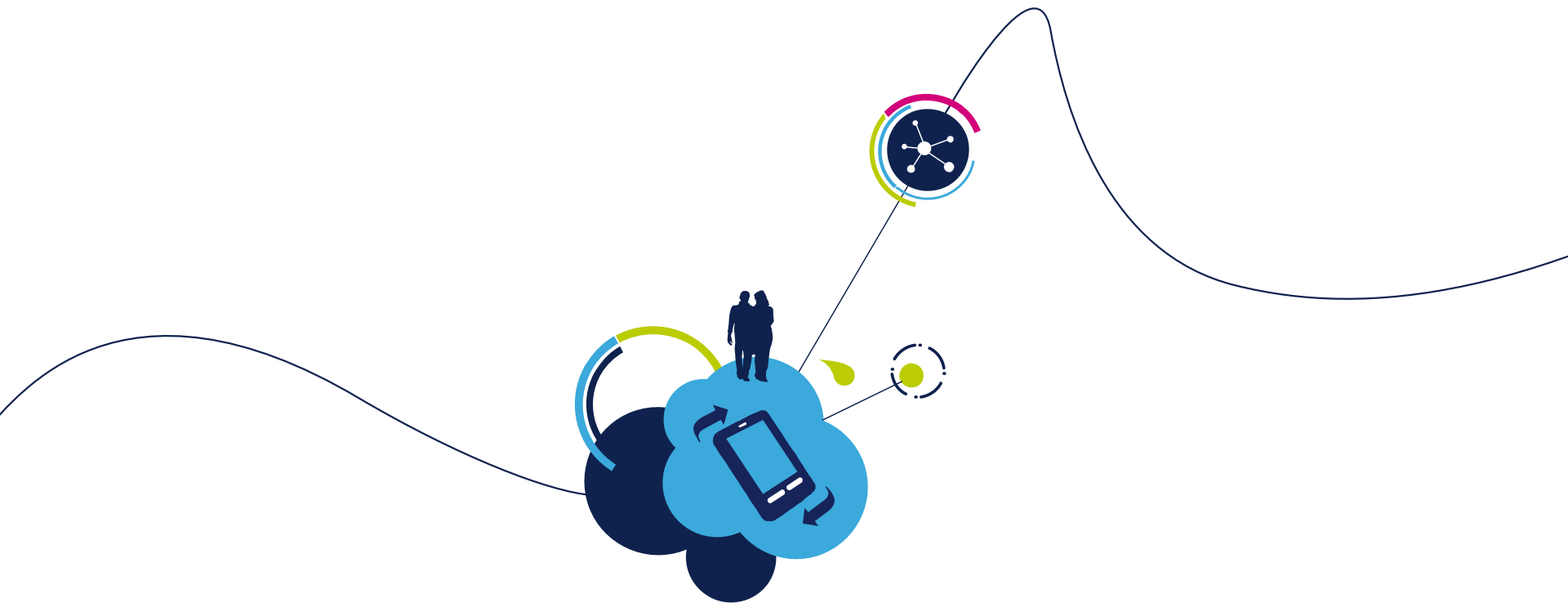
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# Updated features

17

- CLO features - Constant Light Output during board life
  - Maximum time 200K hours : from +0 to +15% of max lout
- lout compensation reading Vout to increase lout precision
  - Remaining on primary side

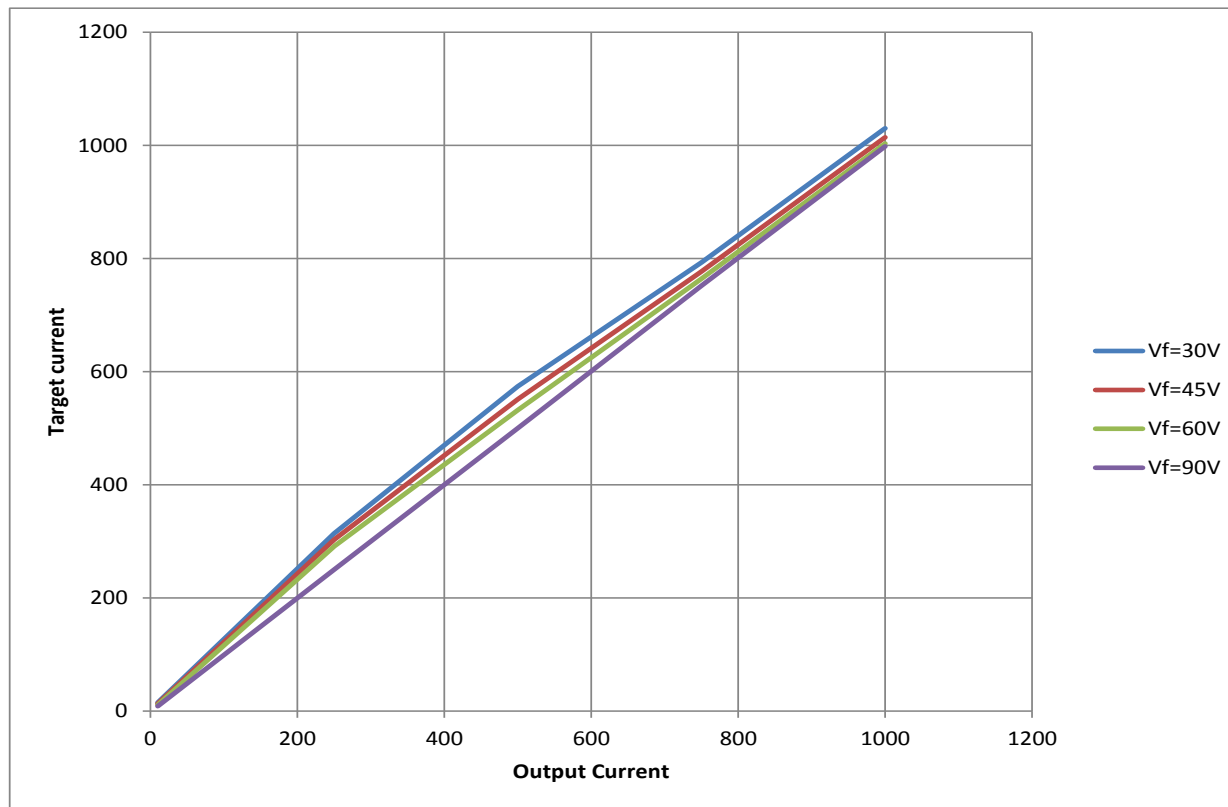


# Results

- Secondary side current precision within 5 %
- Power Factor: higher than 0.98 when output power is above 50W
- THD: below 10% when output power is above 50W
- Higher efficiency: more than 92% at maximum power
- Low input power when in standby: below 250 mW
- **NOTE: using FW revision V3R35**

# Output current regulation summary

21

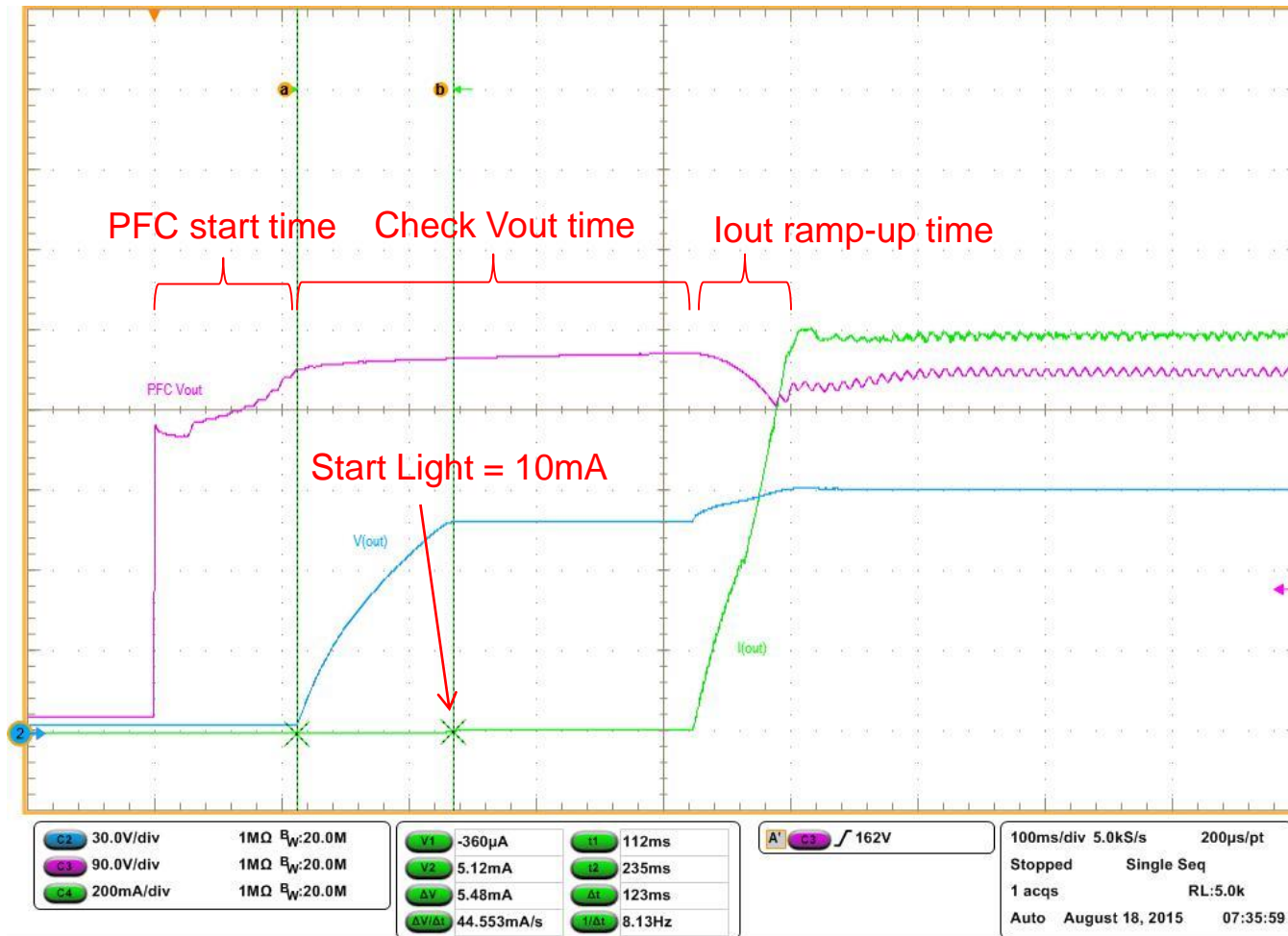


Nominal output current		Vf=30V	Vf=45V	Vf=60V	Vf=75V	Vf=90V
DALI	mA	mA	mA	mA	mA	mA
1%	10	15	13	11	10	8.5
25%	250	314	303	291	273	250
50%	500	574	551	532	516	500
75%	750	793	777	764	754	752
100%	1000	1030	1014	1003	998	998

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# Application start-up

20



PFC Vout

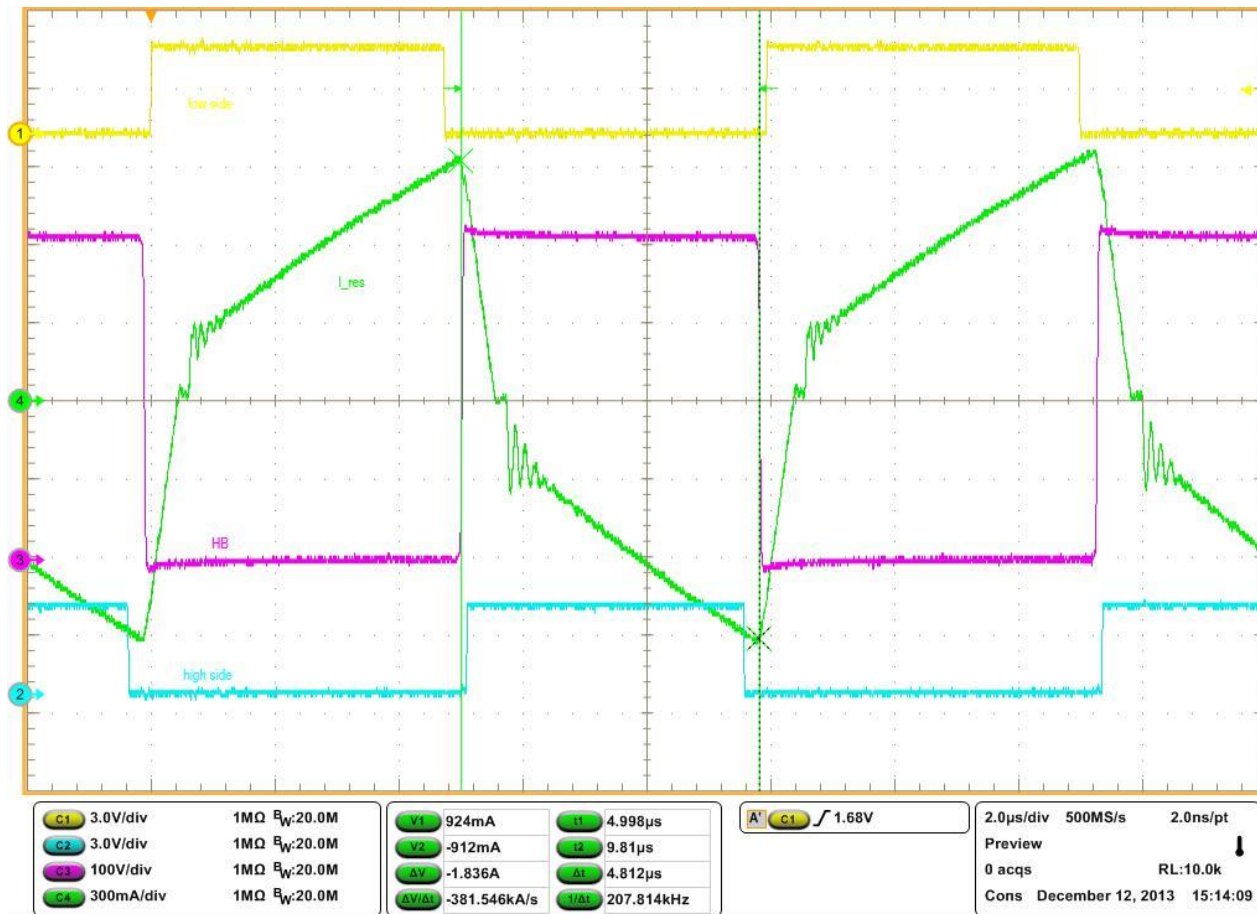
Vout

Iout

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# Output current regulation

24



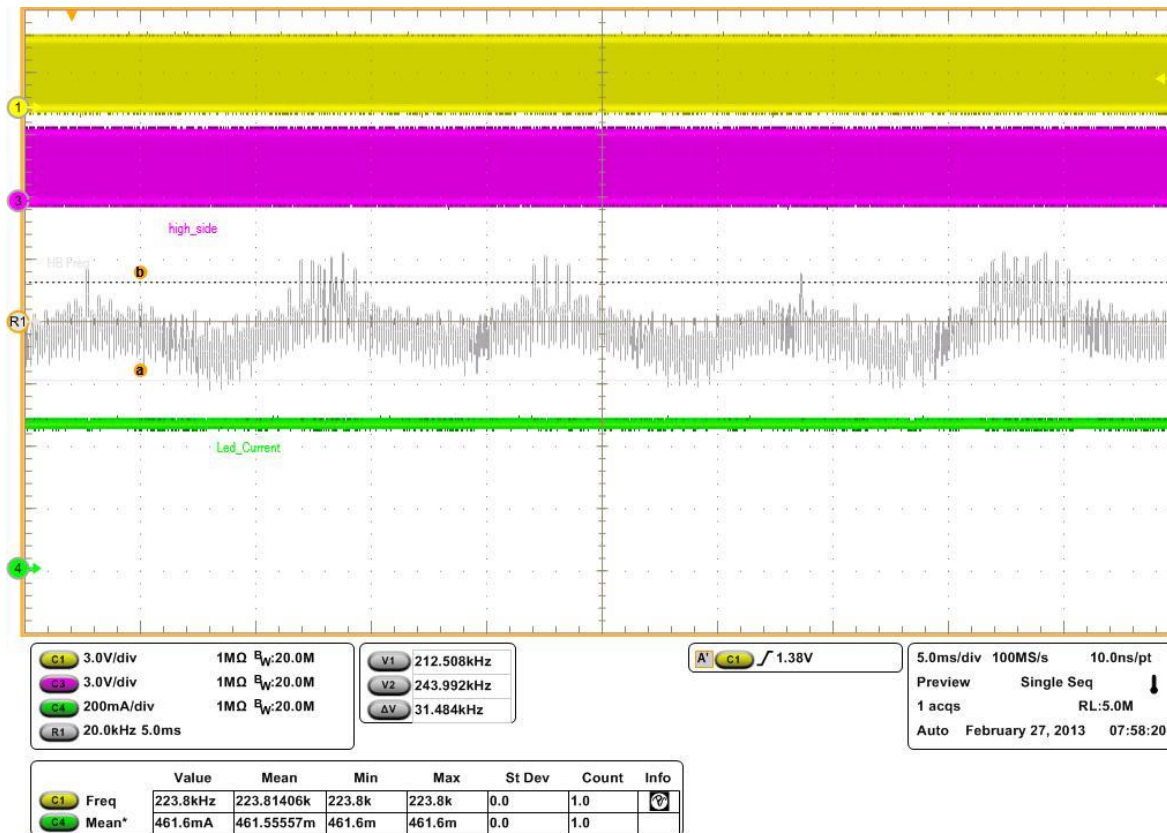
Primary side signals:

- High side (yellow)
- Low side (blue)
- Resonant current (green)
- HB middle point (violet)

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# Output current regulation

22



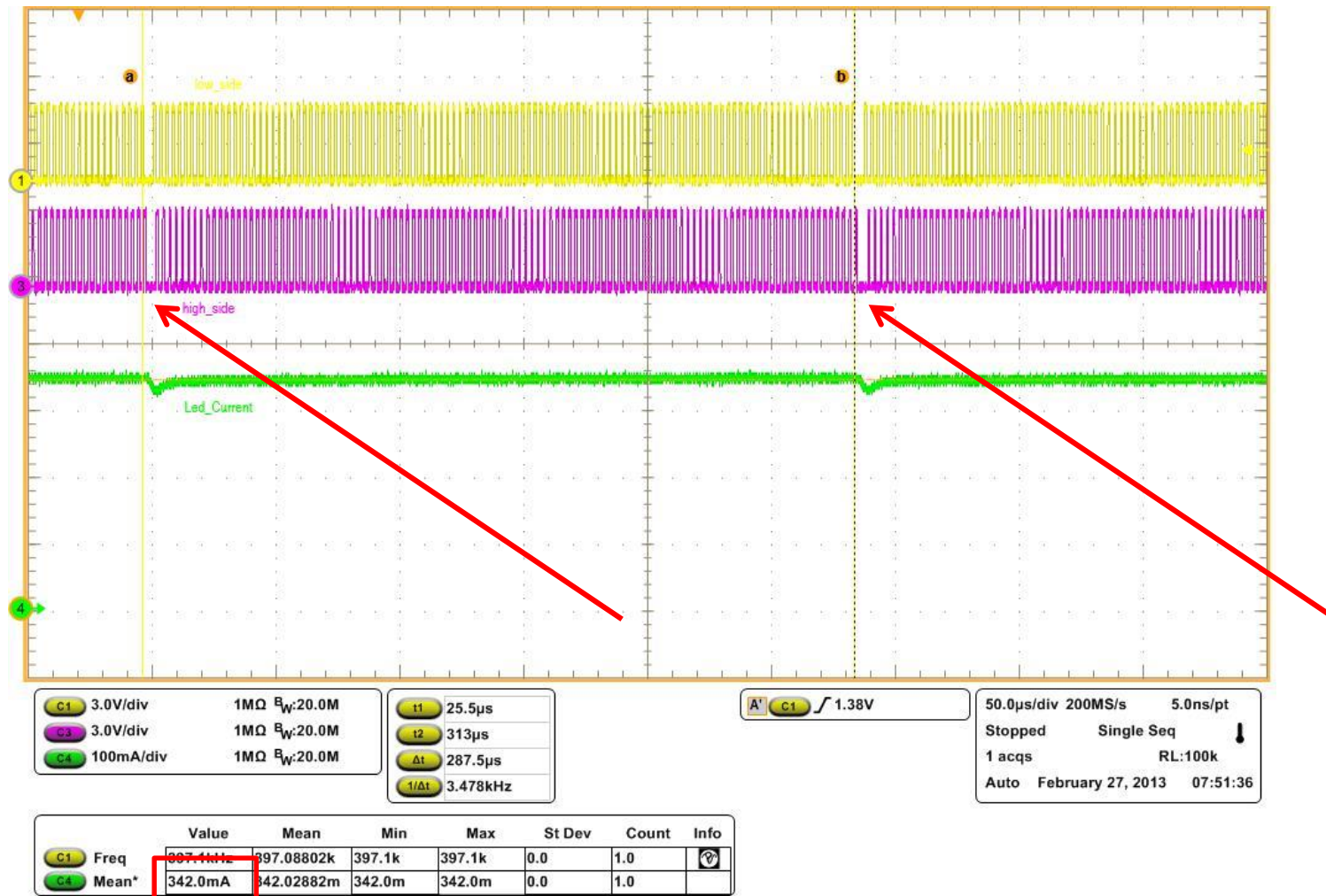
The current is here regulated with peak current mode.

Grey trace depicts the frequency variation having a 100Hz ripple, that is absent into output current (green trace)

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# Skipping cycle – 1 skipped over 112

26

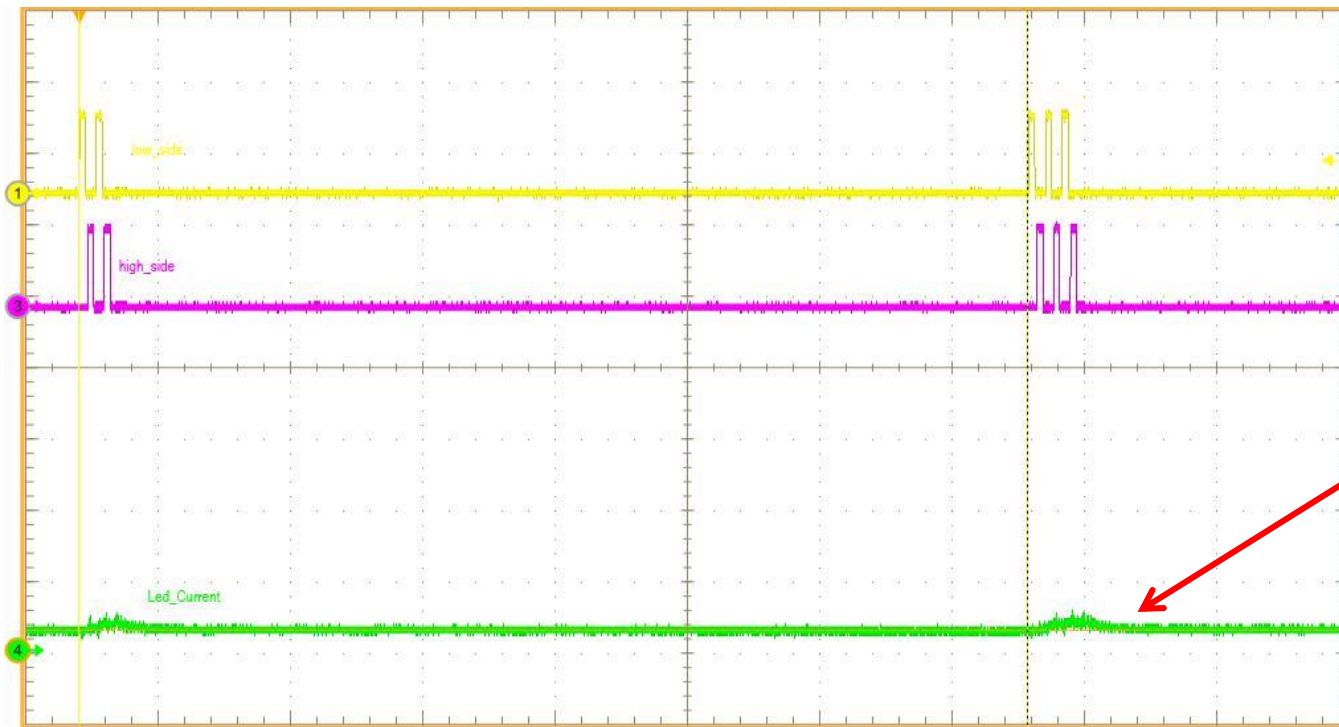


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# Skipping cycle – 107 skipped over 112

27



C1 3.0V/div 1MΩ BW:20.0M  
C3 3.0V/div 1MΩ BW:20.0M  
C4 50.0mA/div 1MΩ BW:20.0M

t1 -200ns  
t2 143.2μs  
Δt 143.4μs  
1/Δt 6.974kHz

A C1 1.38V

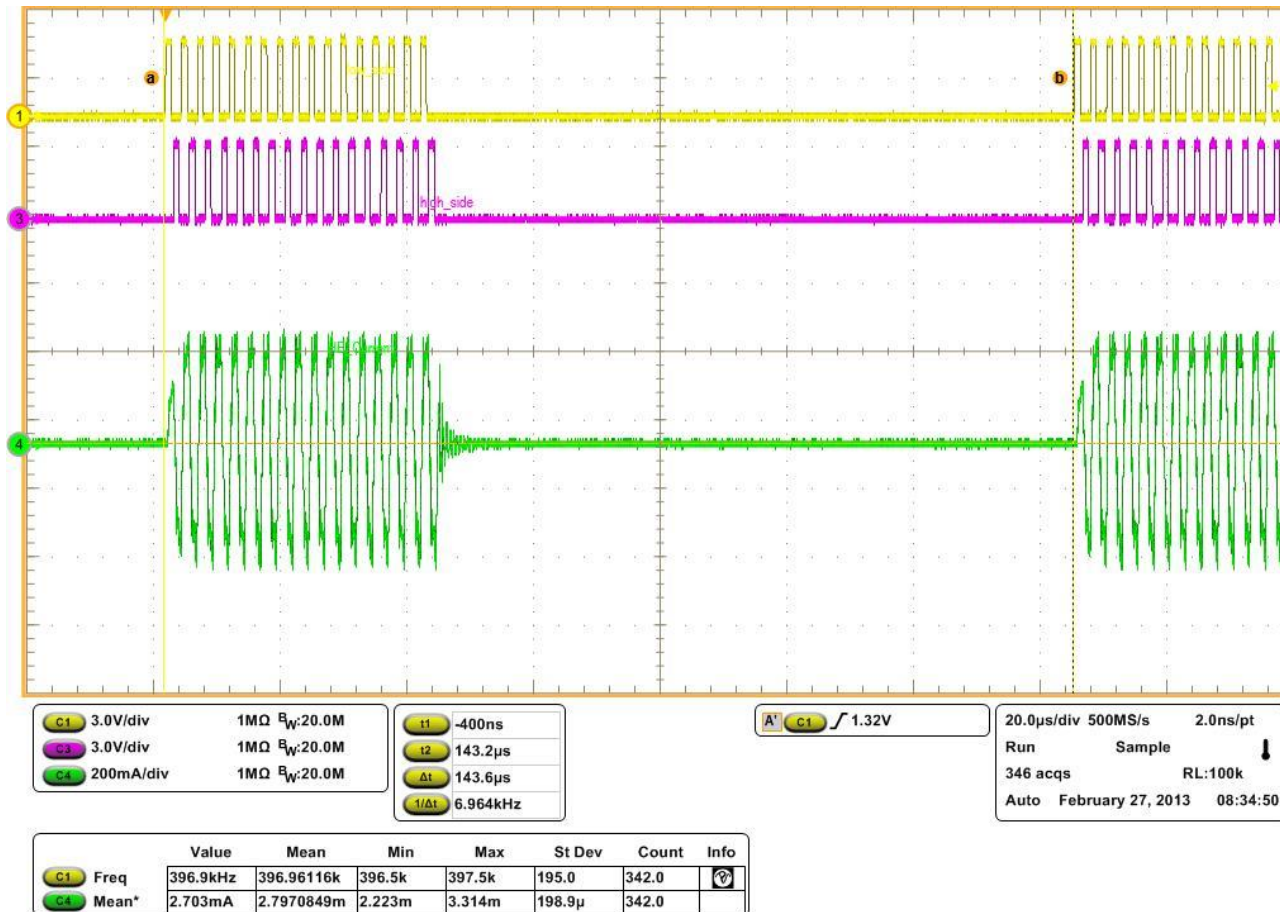
20.0μs/div 500MS/s 2.0ns/pt  
Preview Single Seq  
0 acqs RL:100k  
Auto February 27, 2013 07:48:29

	Value	Mean	Min	Max	St Dev	Count	Info
C1 Freq	207.4kHz	397.08802k	397.1k	397.1k	0.0	1.0	
C4 Mean*	14.12mA	14.124177m	14.12m	14.12m	0.0	1.0	

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# Skipping cycle – 30%

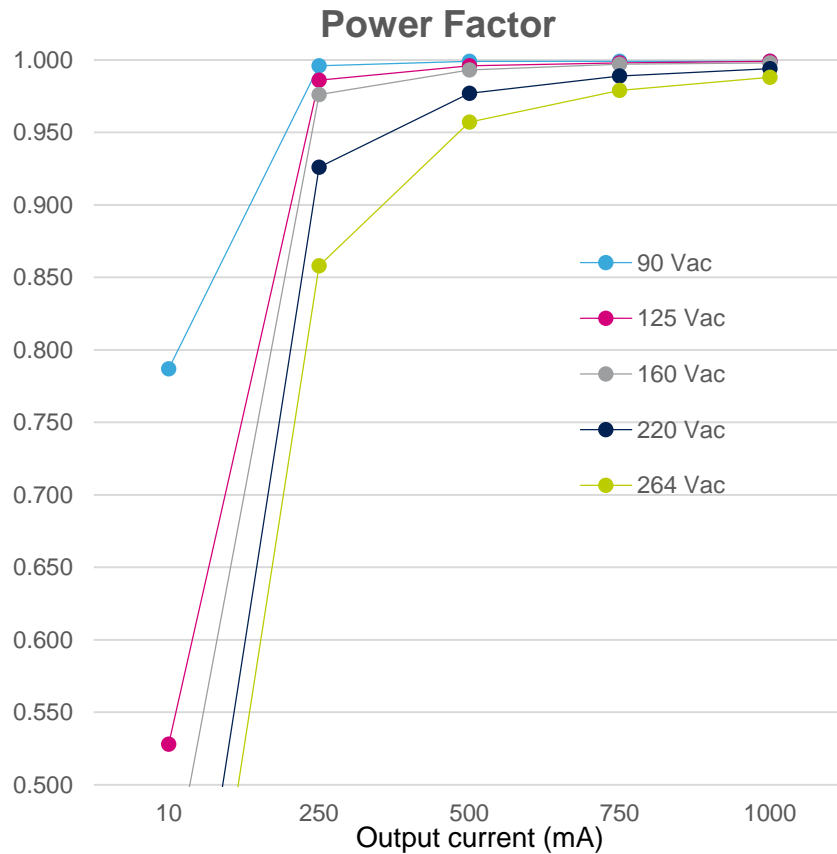
28



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# Power factor and THD summary

29



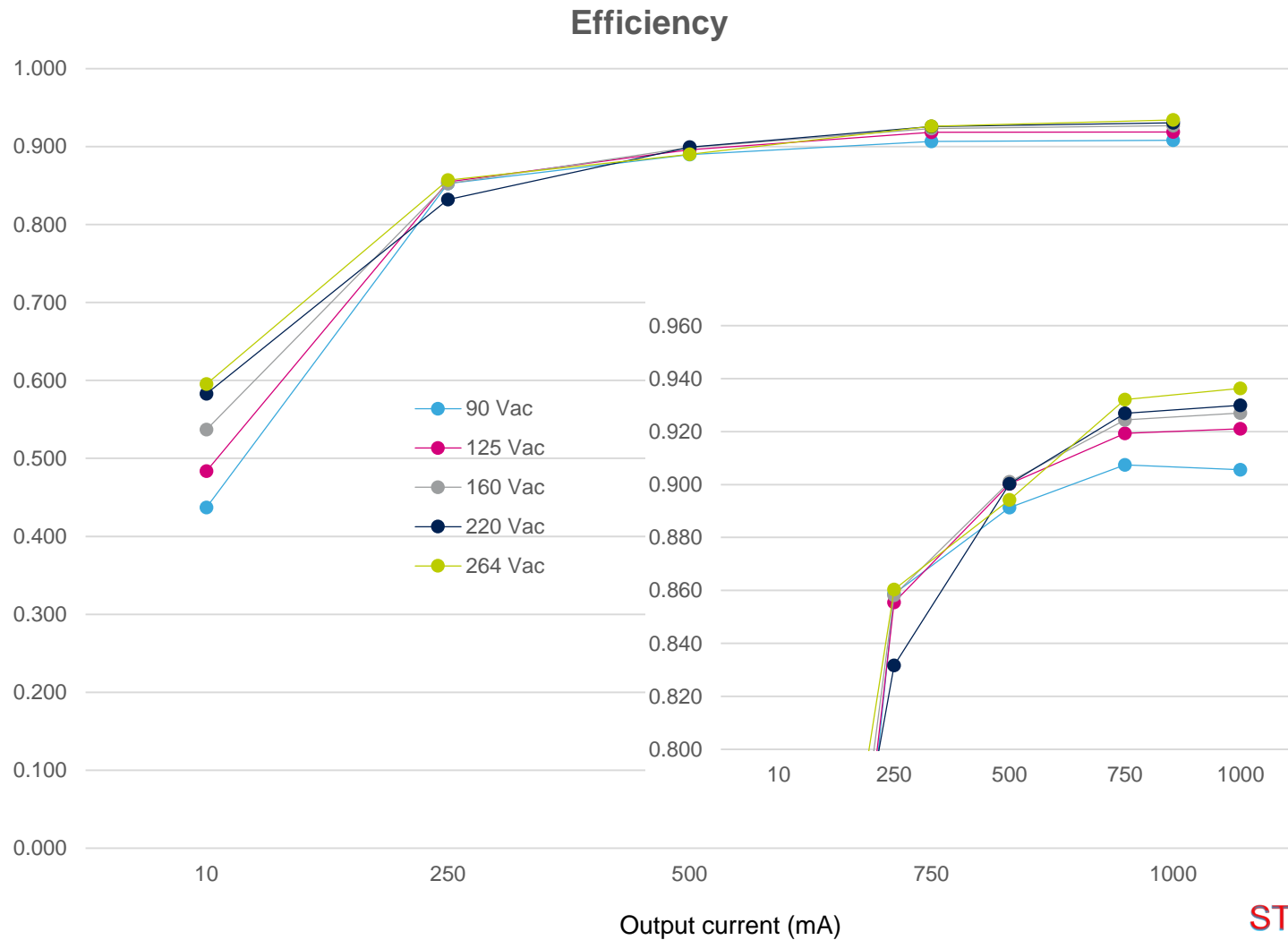
PF and THD values versus output power for different input voltages



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# Overall Efficiency summary

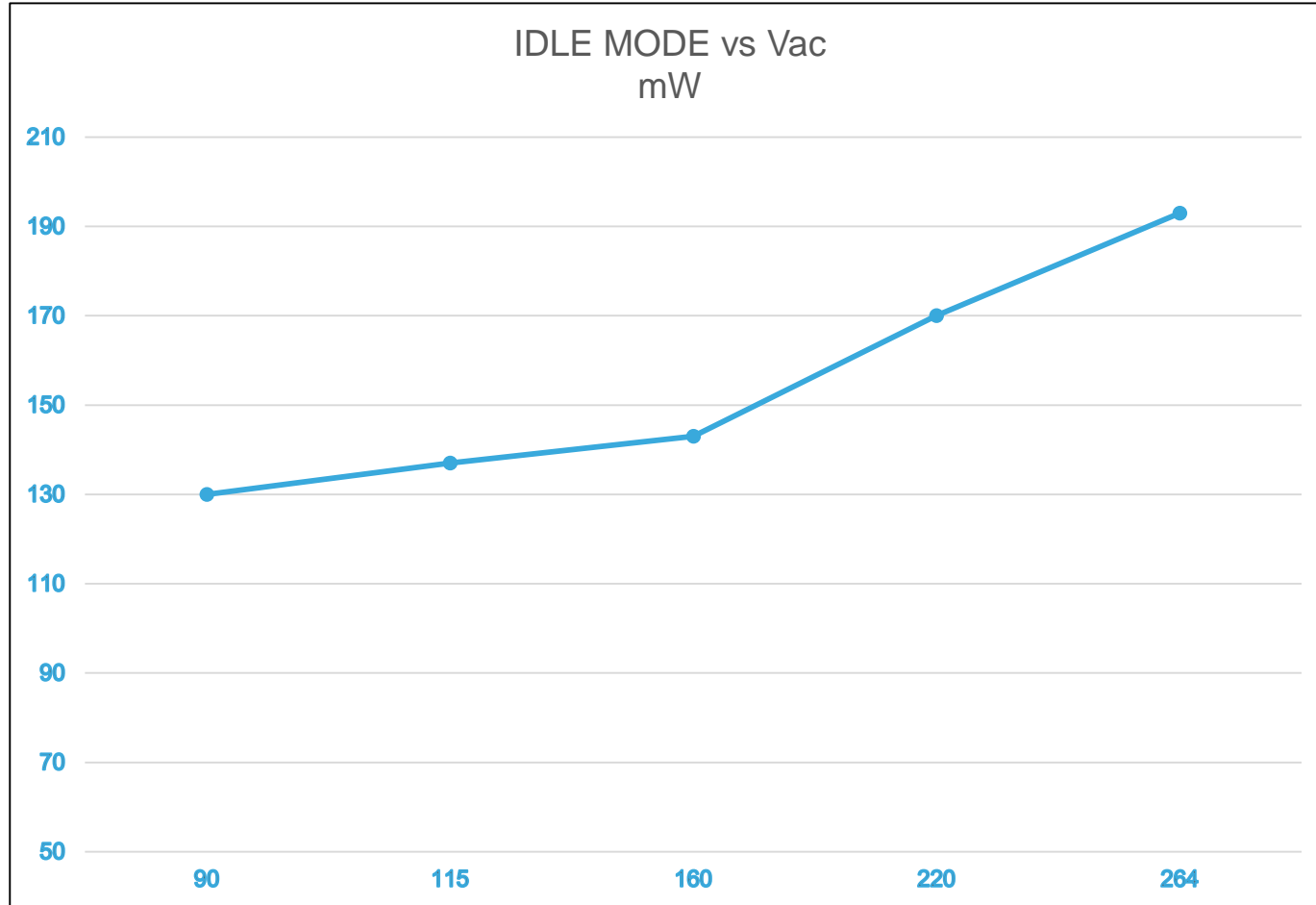
30



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# Standby Power summary

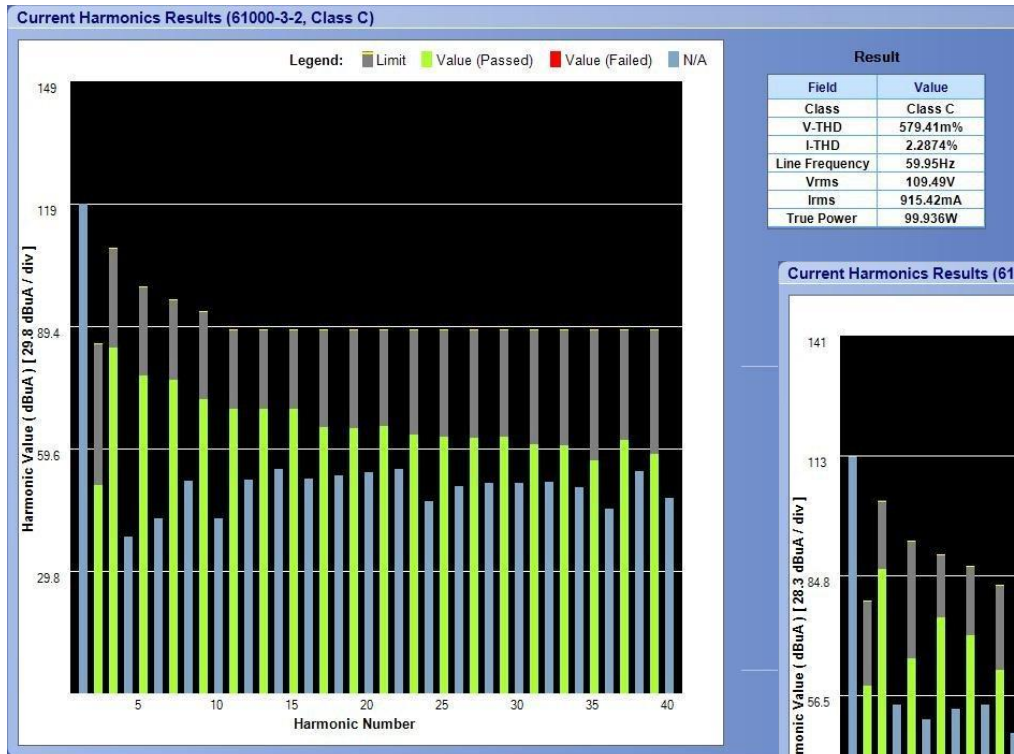
31



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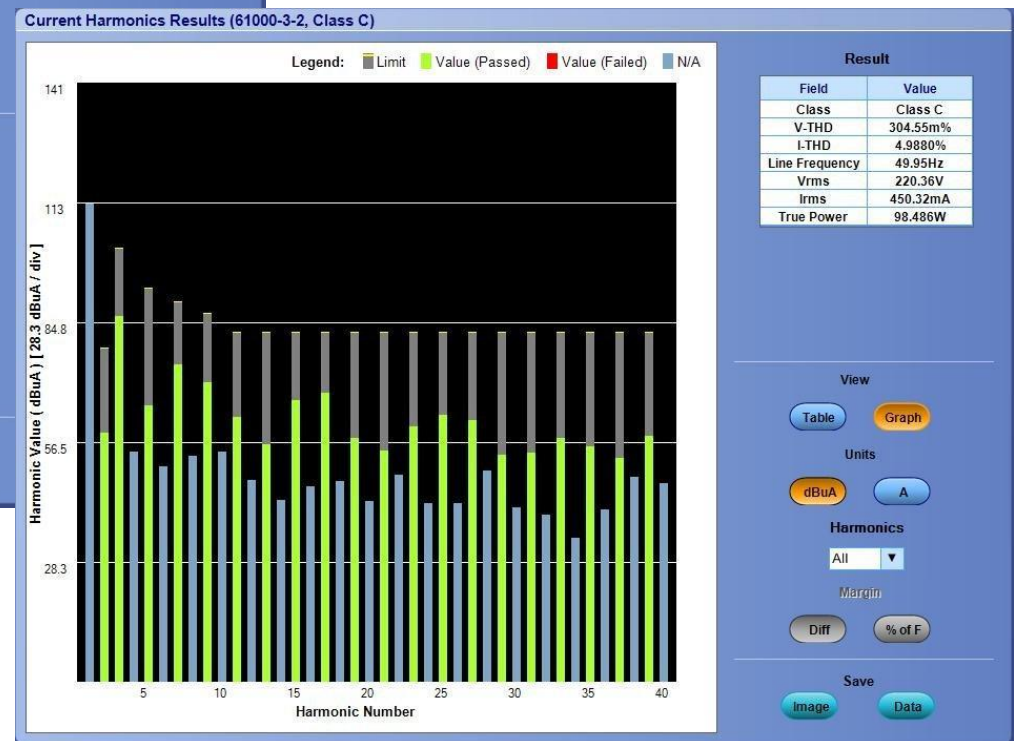
# Full power Harmonic contents

32

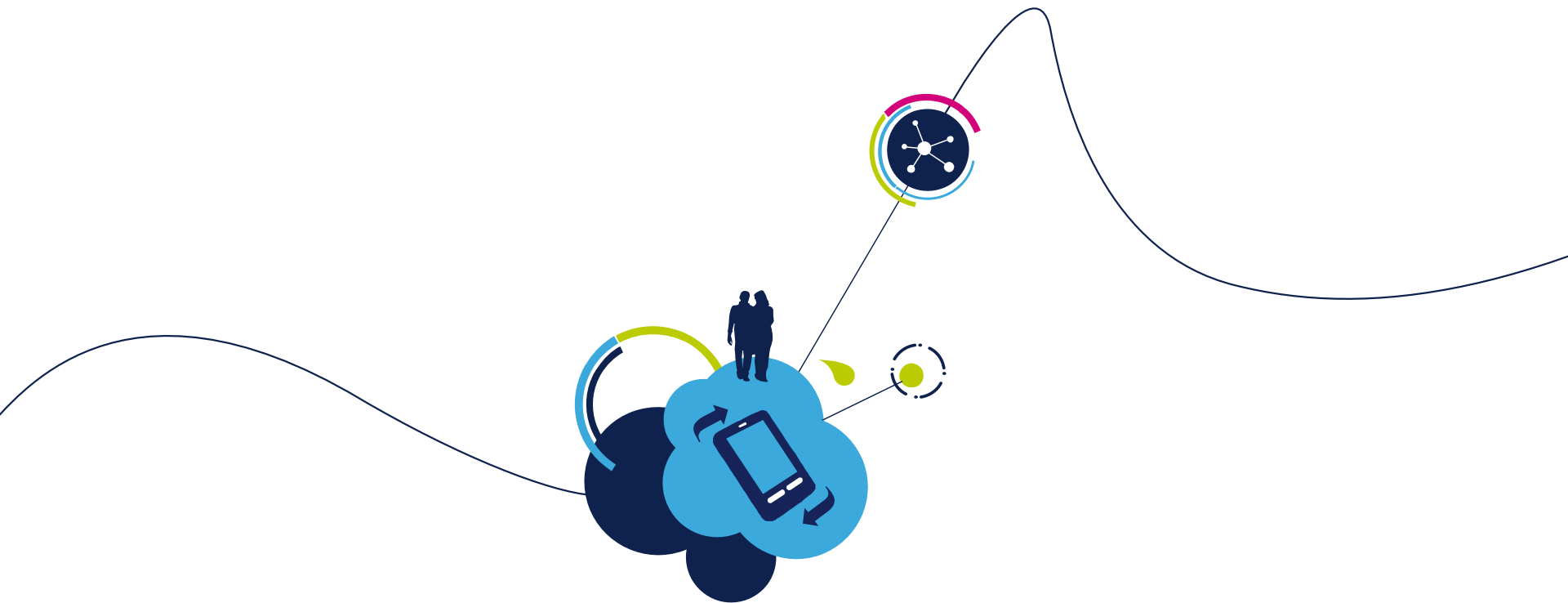


110 Vac

220 Vac



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# FW Application Library

# Why using the FW library

34

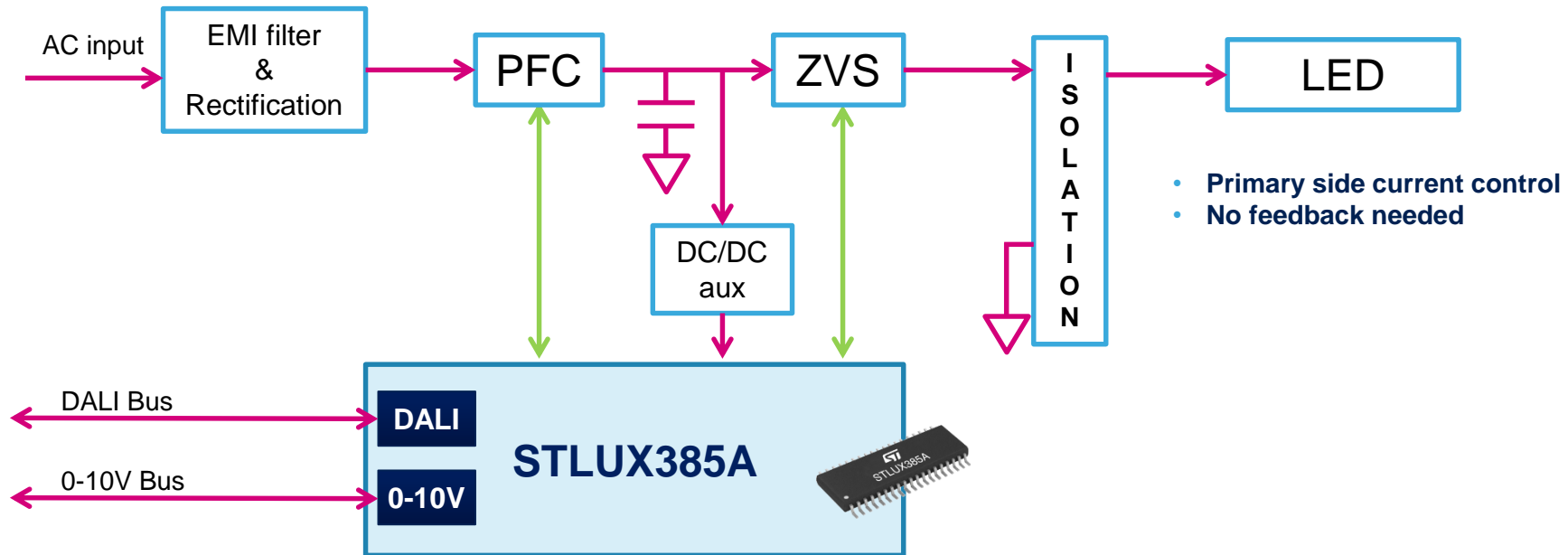
- FW library implements PSR power conversion stage
  - Integrates PFC and HB control algorithms
  - STLUX385A SMEDs configured and updated at run-time
- Fully customizable
  - Configuration via serial interface or software application layer
  - Parameters stored in EEPROM
  - 50+ configurable parameters
- Fast time-to-market
  - Easy to develop application on top of the library
  - Focus on application differentiation

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# Block schematic

35



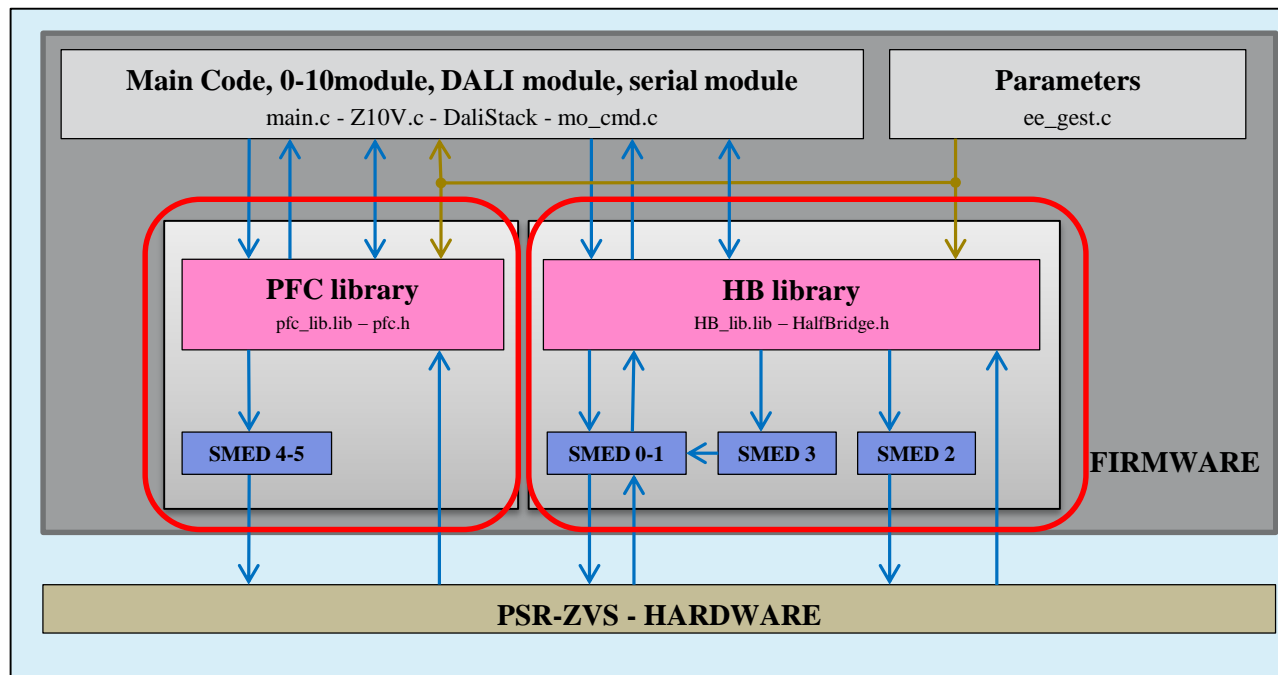
- **STLUX385A signals:**
  - Input voltage for Uvlo&startup
  - **PFC** output voltage for loop regulation
  - **PFC** gate driving signal
  - **ZVS** resonant current for control loop, output voltage for protection
  - **ZVS** HB and relevant dimming control signals
  - **DALI** frame – interpreter, response and execution
- **Secondary components:** Rectifier and capacitor (no extra active components)

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# Library Implementation

36

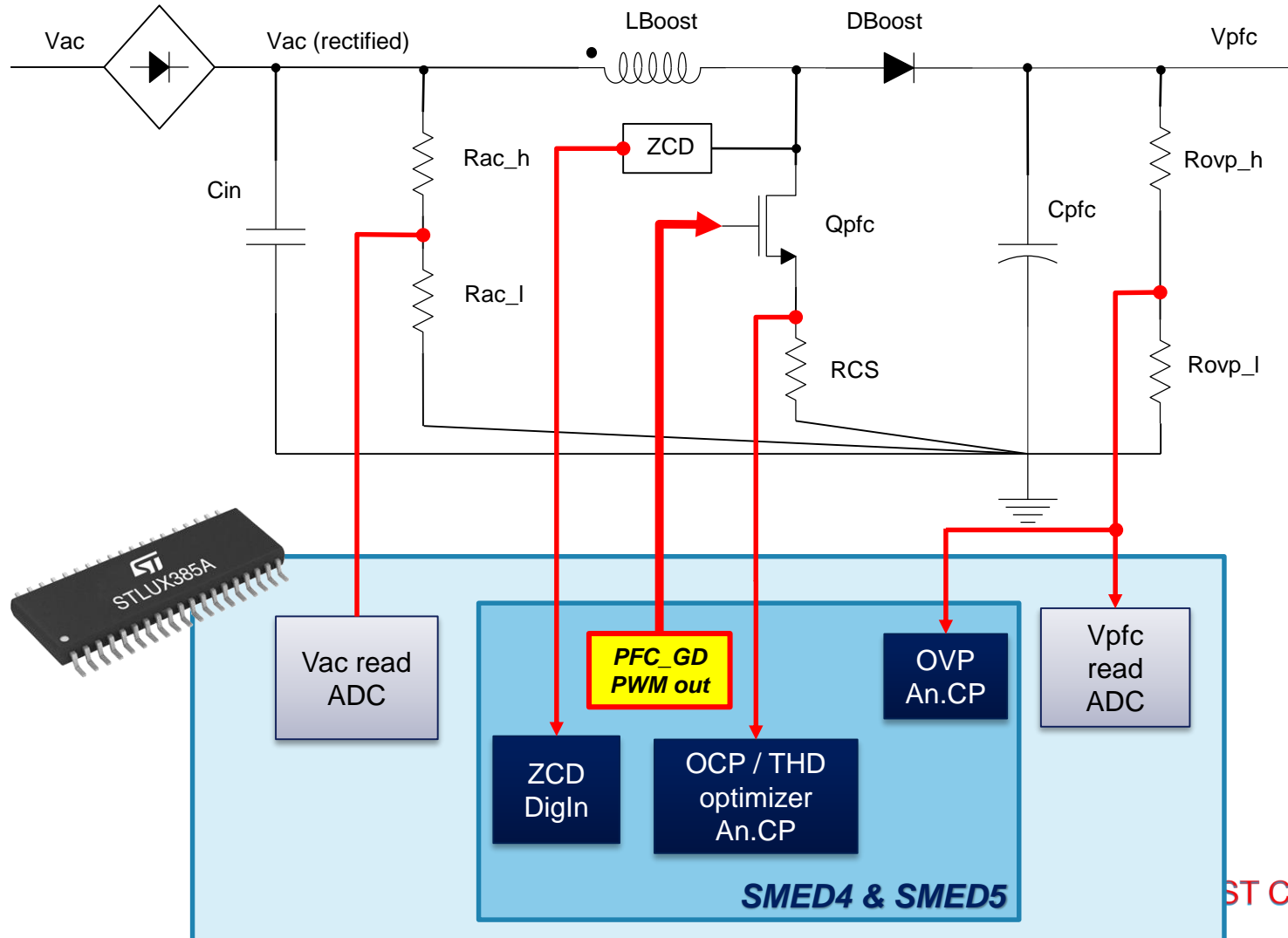
- Two independent firmware module: one for PFC, one for Half Bridge ZVS
- PFC and HB-ZVS Hardware adaptation using modifiable parameters



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# PFC - Schematic

37

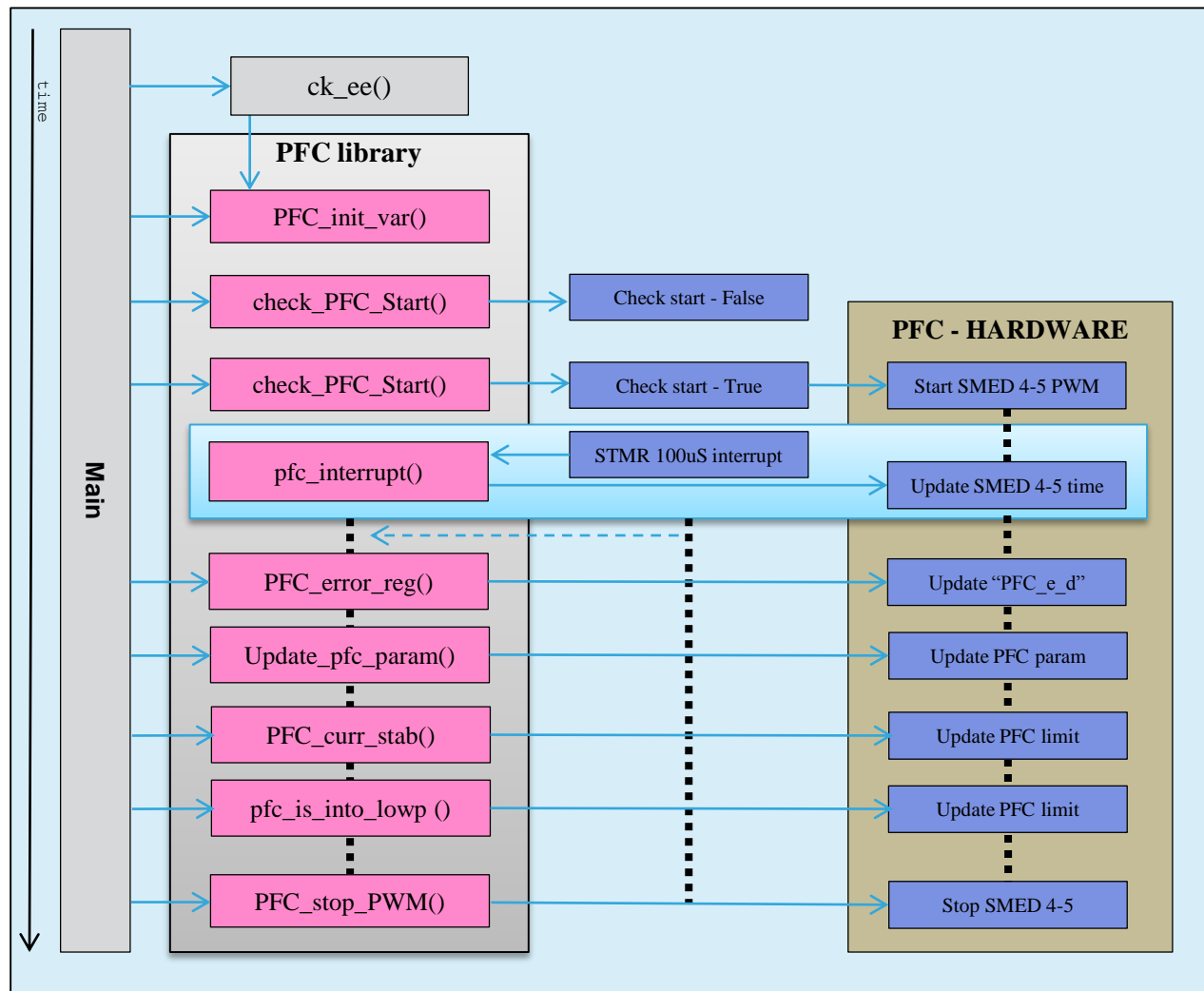


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# PFC – Library Implementation

38

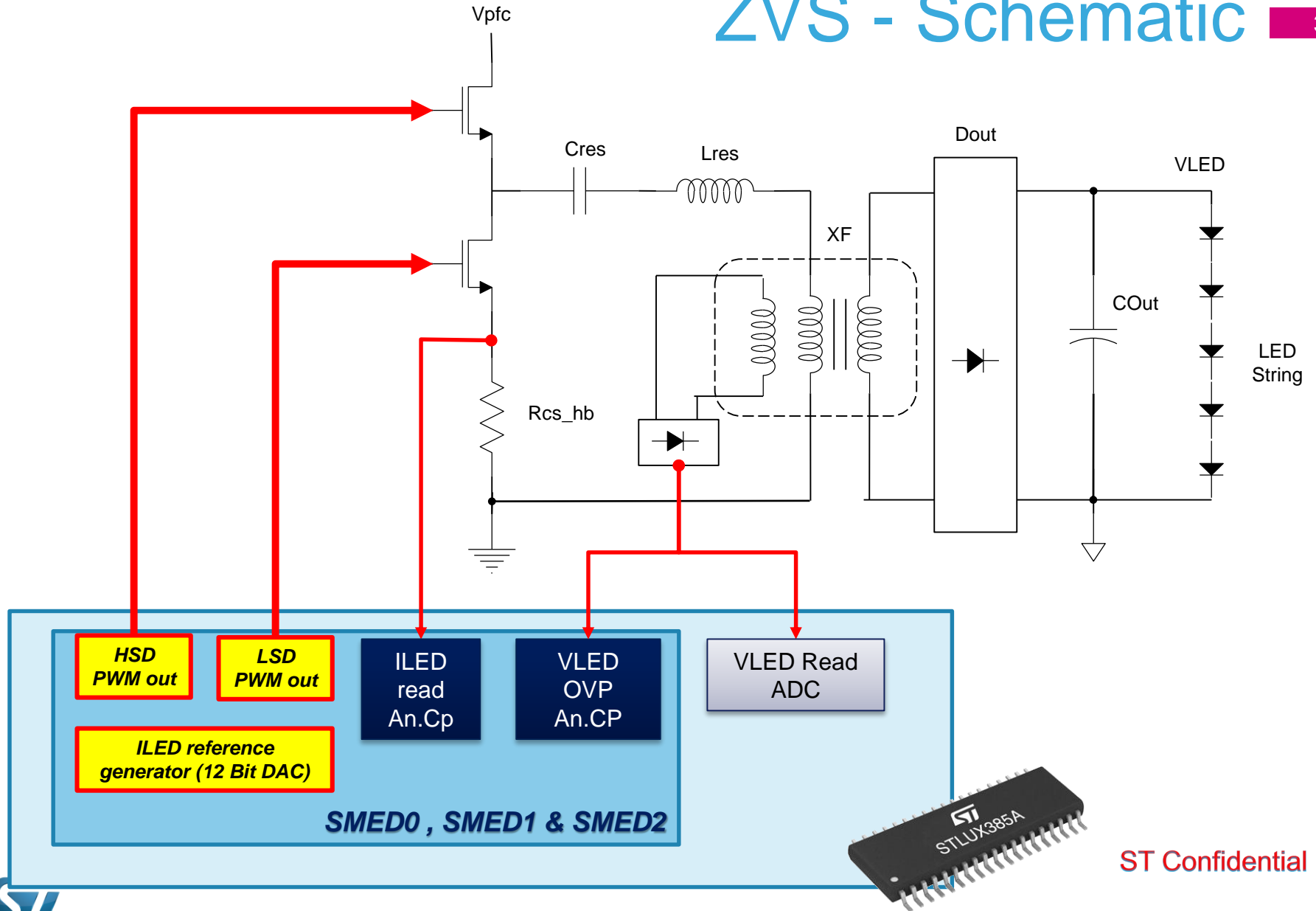
- PFC parameters apply during start-up
- PFC control using simple subroutine
- PFC Start/Stop under User control
- Automatic update PFC control loop using interrupt
- PFC library control SMED4-5 behavior



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# ZVS - Schematic

39

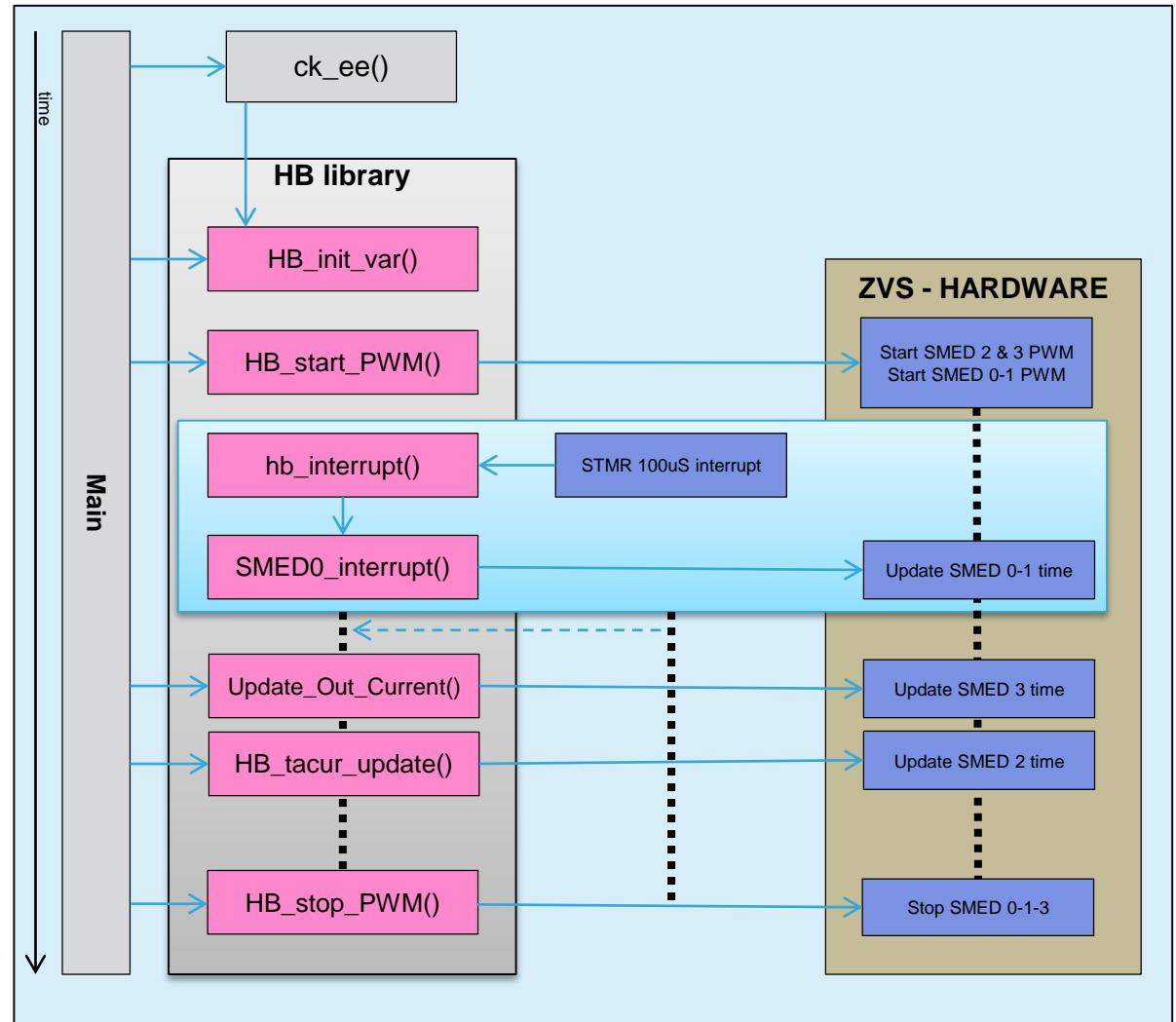


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# HB-ZVS – Library Implementation

40

- HB parameters apply during start-up
- HB start/stop under User control
- Automatic HB control loop using only interrupt
- Subroutine to manage the output current
- HB-ZVS library control SMED0-1, SMED2 and SMED3 behavior



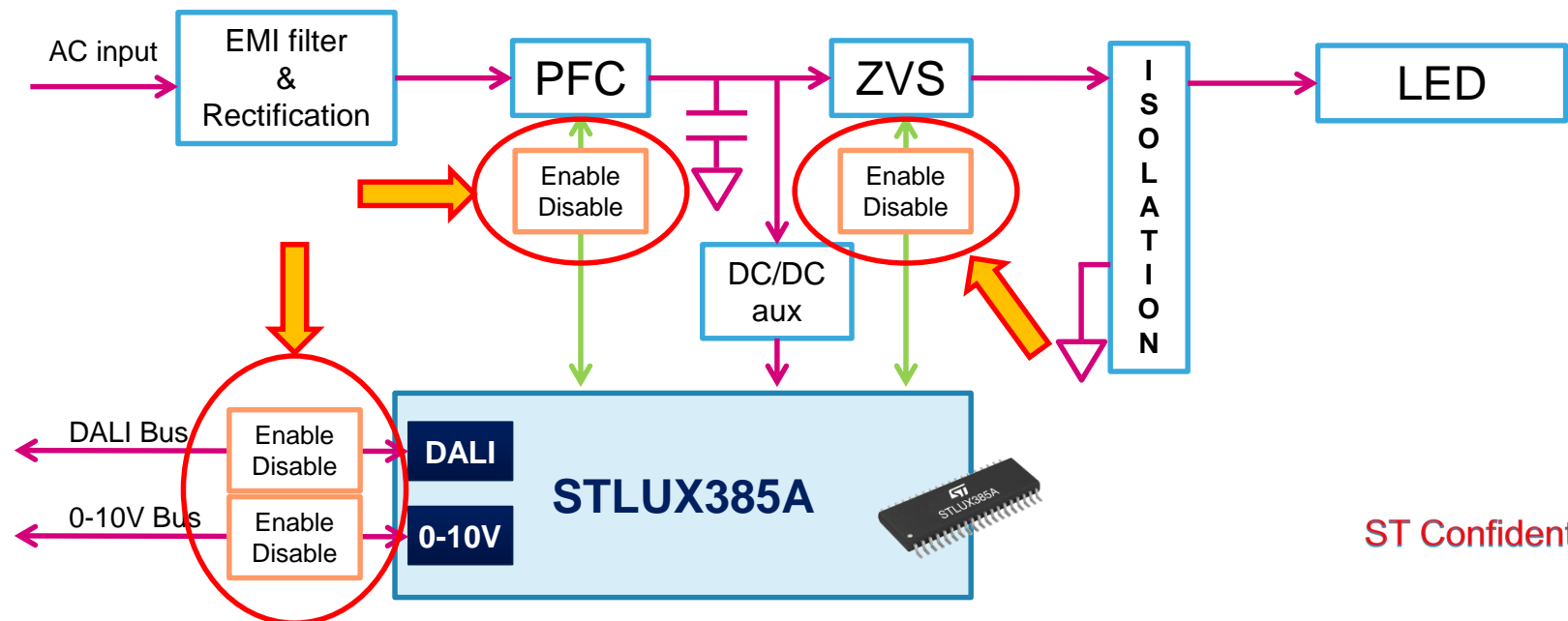
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- Three configurable parameters area:
  - Application parameters: enable the ROP code protection, enable/disable interfaces or library function
  - PFC parameters: output level, start-up current limitation, three zone level definition, OCP level protection, Vac input level start/stop, PFC uvlo level, etc.
  - HB parameters: max. ON time (limit the output power), no load level intervention, HIGH side delay trimming, propagation delay mismatch compensation, etc.
- Some parameters is modifiable, some other is fixed
  - Parameters is modifiable using serial command and is apply during start-up
  - Fixed parameters is modifiable using external resistor.
- When the parameters customization is approved, duplication is simple using “standard” read/download procedure.

# Application Parameters

42

- Application modifiable parameters:
  - Enable or Disable globally all the board functionality (debug mode)
  - Enable the ROP Code protection
  - Enable/Disable the PFC and/or the Half Bridge functionality
  - Enable/Disable the DALI interfaces or, mutually exclusive, the 0-10V interfaces
  - Enable/Disable the Half Bridge loop compensation, usable to working into HB open loop → HB fixed frequency.





- PFC parameters modifiable by serial line:
  - Impose the THD time optimizer, to increase/relax or remove the PFC THD optimizer
  - Personalize the Over Current Protection level
  - Personalize the PFC Start-up voltage level
  - Define the PFC Input Under Voltage Protection level
  - Define the PFC Output Over Voltage primary level
  - Define the PFC Output Under Voltage Protection level
  - Define the PFC Maximum ON time to limit the maximum output power variation
  - Define the delay before detect the input Vac missing
- PFC parameters frizzed by hardware (resistor):
  - PFC output voltage definition
  - PFC input voltage definition
  - Last resource to Over Voltage protection (apply directly into SMED)

- HB Parameters modifiable by serial line:
  - Half Bridge maximum frequency
  - Half Bridge minimum frequency
  - No load level; to modify the maximum output voltage level
  - Propagation delay mismatch compensation; if change the HB driver
  - Trimming the Half Bridge HIGH side delay; if change the HB driver
  - Dead Time apply to the HB stage
- HB parameters frizzed by hardware (resistor):
  - Output current; to modify the maximum output current, modify the shunt resistors (and also the output transformers if necessary).

**Thank you  
very much  
for your attention**