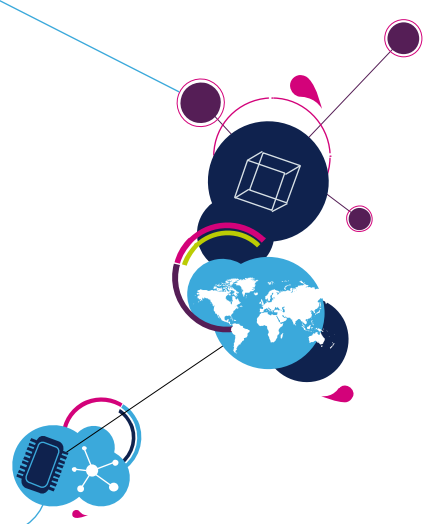
STLUX385A in primary side controlled LED applications

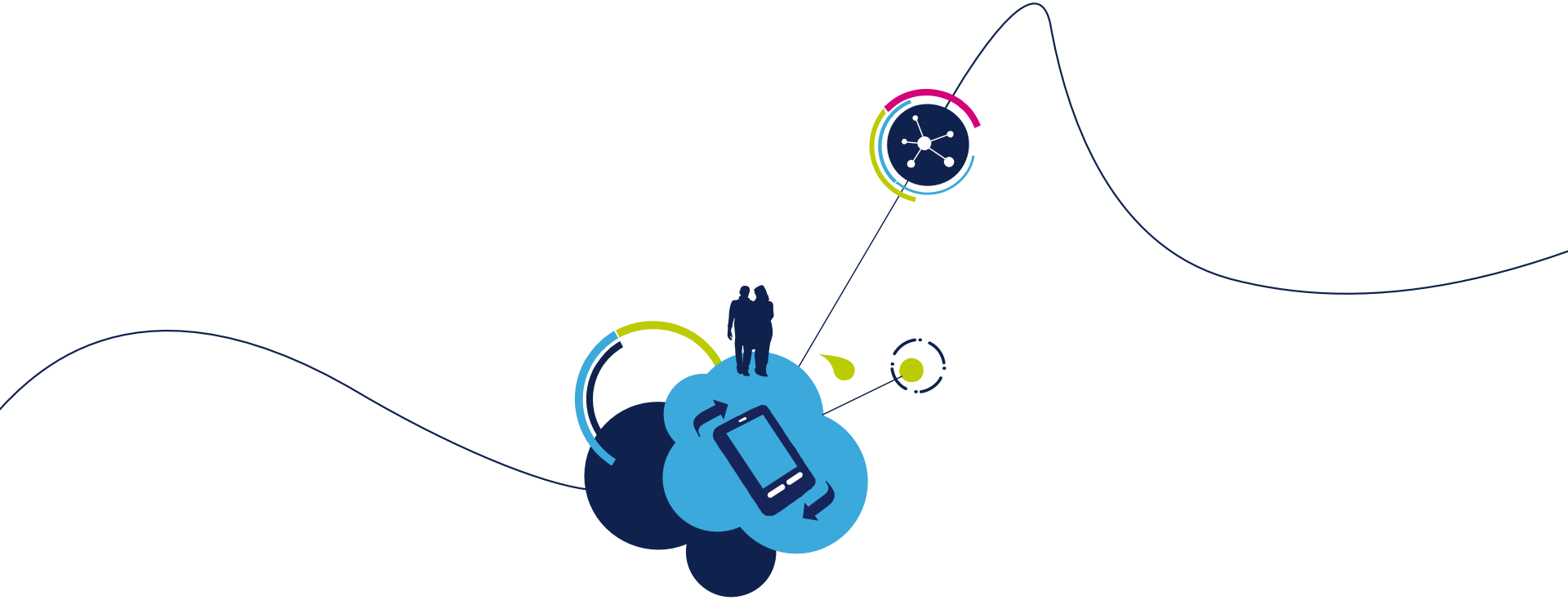


Using STLUX385A on primary side control single100W LED channel

STEVAL-ILL066V1

life.augmented

ST Confidential



Primary side controlled LED driver

Target application

- Street lighting and Tube replacement
  - Wide-range input
  - Single string output (100V or 200V max.)
  - 100W maximum output power - down to 1W
  - 1 A maximum output current - down to 10mA (500mA on 200V version)
  - DALI interfaces on board - standard IEC62386-102-207 – LED
  - Insulated 0-10 V interface alternative to DALI.

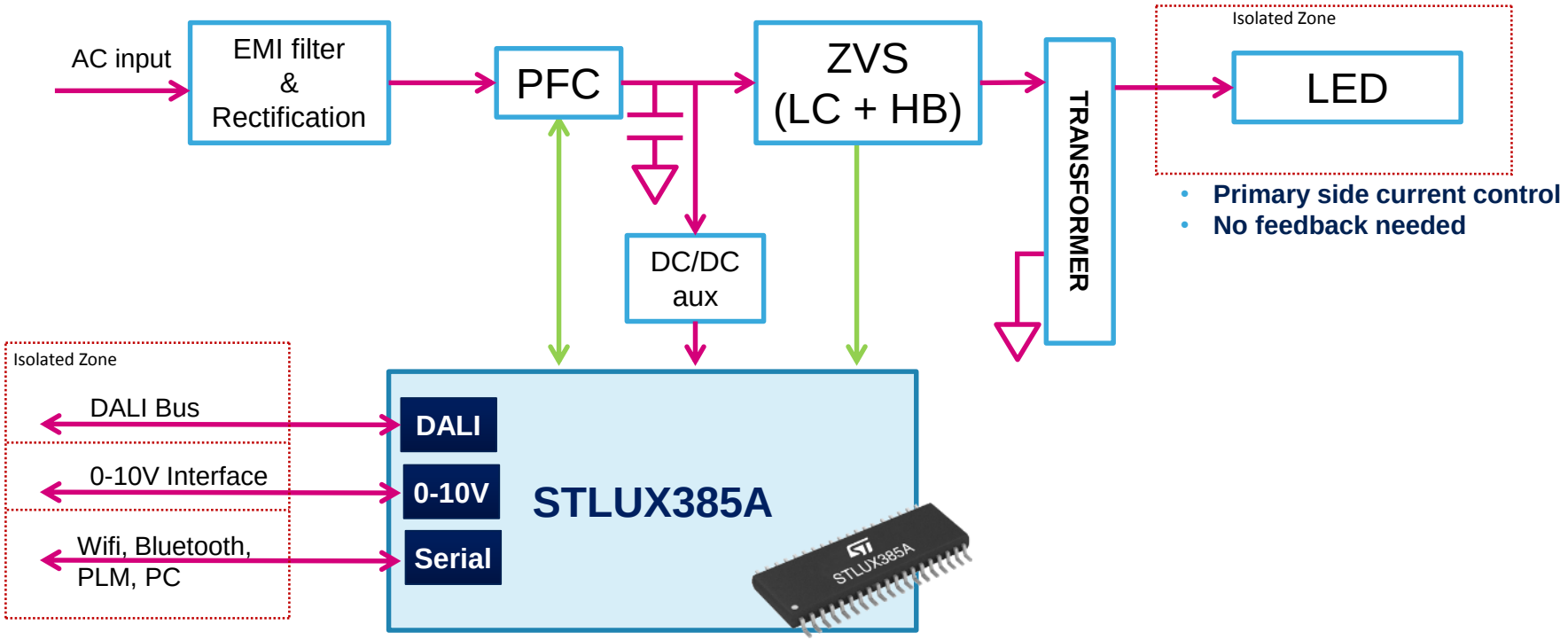
Board Characteristics

- Input: 90~265 Vac
- Output: 100 V - 1 A max [200 V – 500mA] (100W)
- Current precision: better than 5% from 50W to 100W output
- Control line: by Serial and DALI bus (Opt: isolated 0-10V)
- Power efficiency: more than 92%

- Digitally controlled single chip solution for: PFC+LC+DALI
- Primary side regulation of LED current
- Extremely low power when output LED are turned off by DALI command (**lower than 250 mW**)
- Operating temperature from -40 to +105ºC

- Two Layers PCB
- Dimension - 270x50x35 mm (LxWxH)

Block schematic

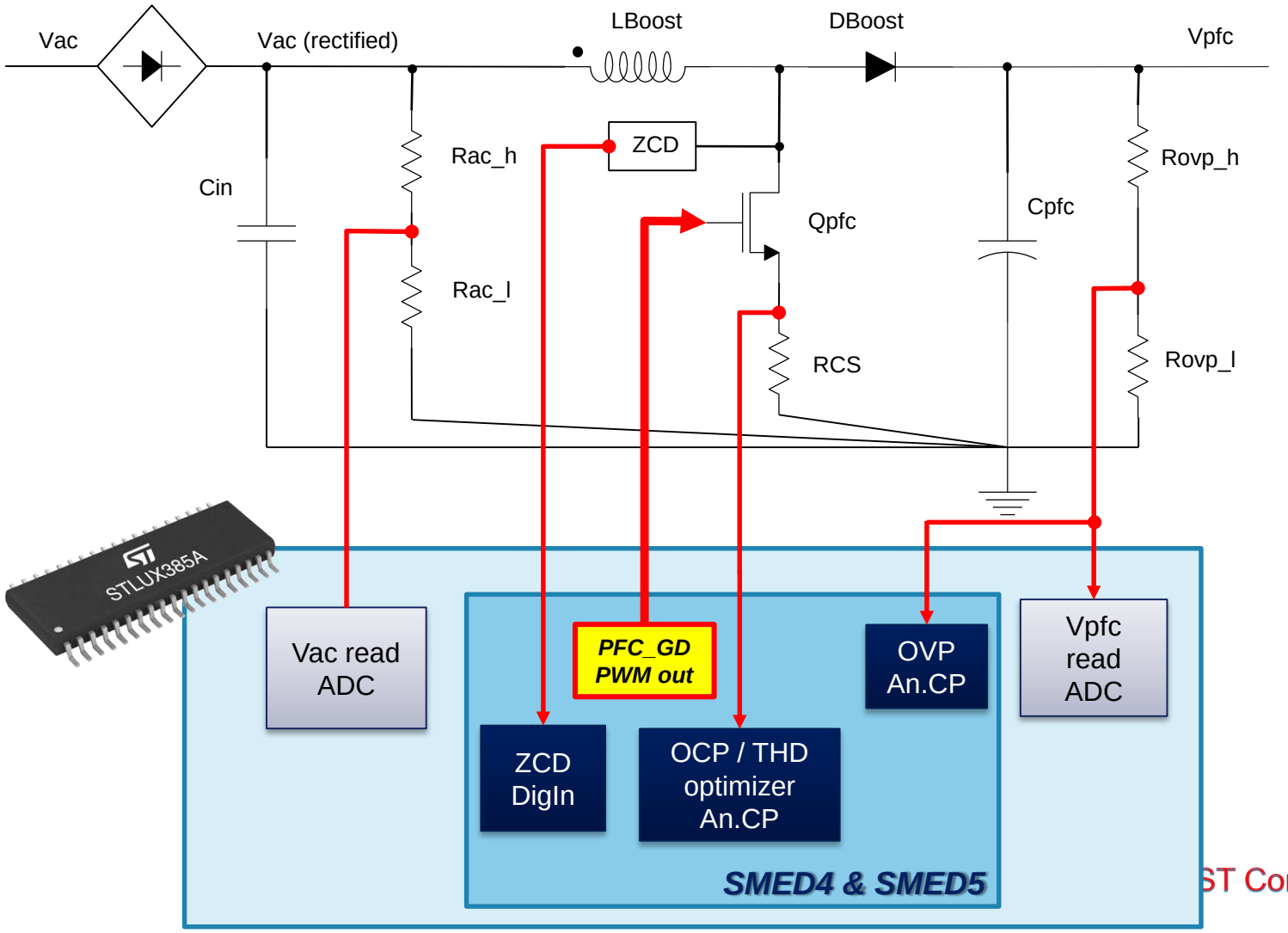


- **Key products**
  - **STLUX385A digital controller**
  - STF19NM50N (PFC stage)
  - STD12NM50ND (ZVS stage)
  - PM8841/51D (PFC driver)
  - VIPer06XS (aux DC/DC)
  - L6388ED (ZVS driver)

- **STLUX385A signals:**
  - Input voltage for Uvlo&startup
  - **PFC** output voltage for loop regulation
  - **PFC** gate driving signal
  - **ZVS** resonant current for control loop, output voltage for protection
  - **ZVS** HB and relevant dimming control signals
  - **DALI** frame – interpreter, response and execution

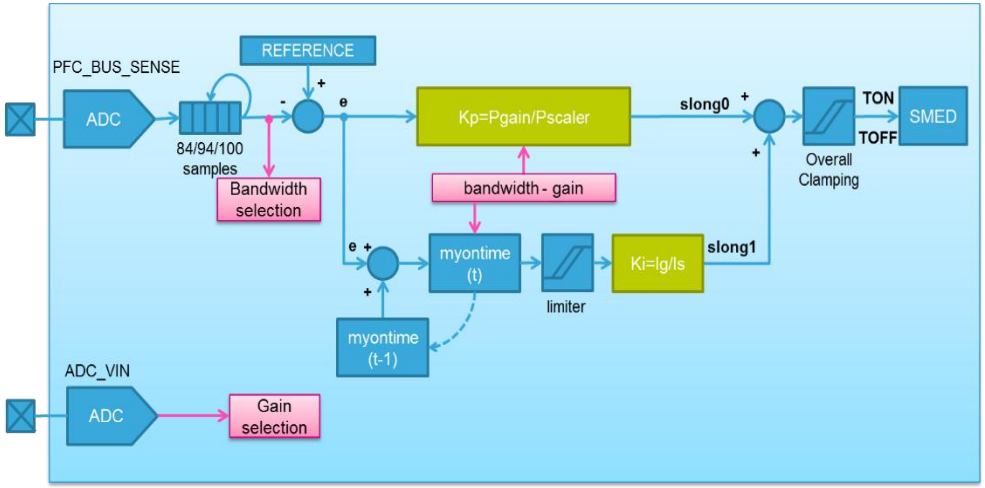
- **Secondary components:**
  - Rectifier and capacitor (no extra active components)

PFC - Schematic



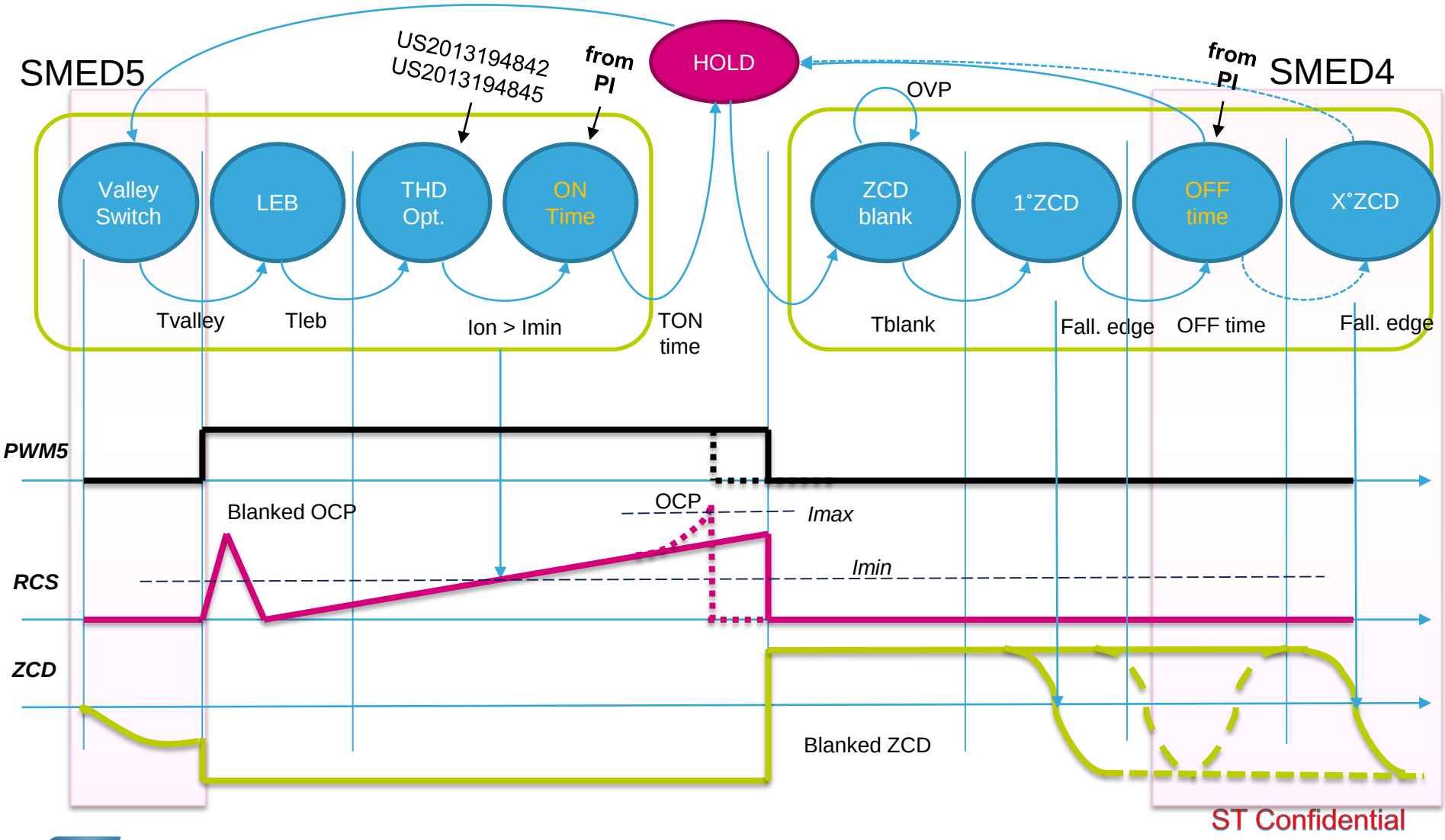
PFC - Implementation

- PFC - PI control mode
  - Transition Mode PFC
  - 10KHz PFC error acquisition
  - AC cycle regulation
  - Digital Programmable PI algorithm
  - Adaptable Error Gain
  - Internal compensation algorithm
  - Programmable output voltage

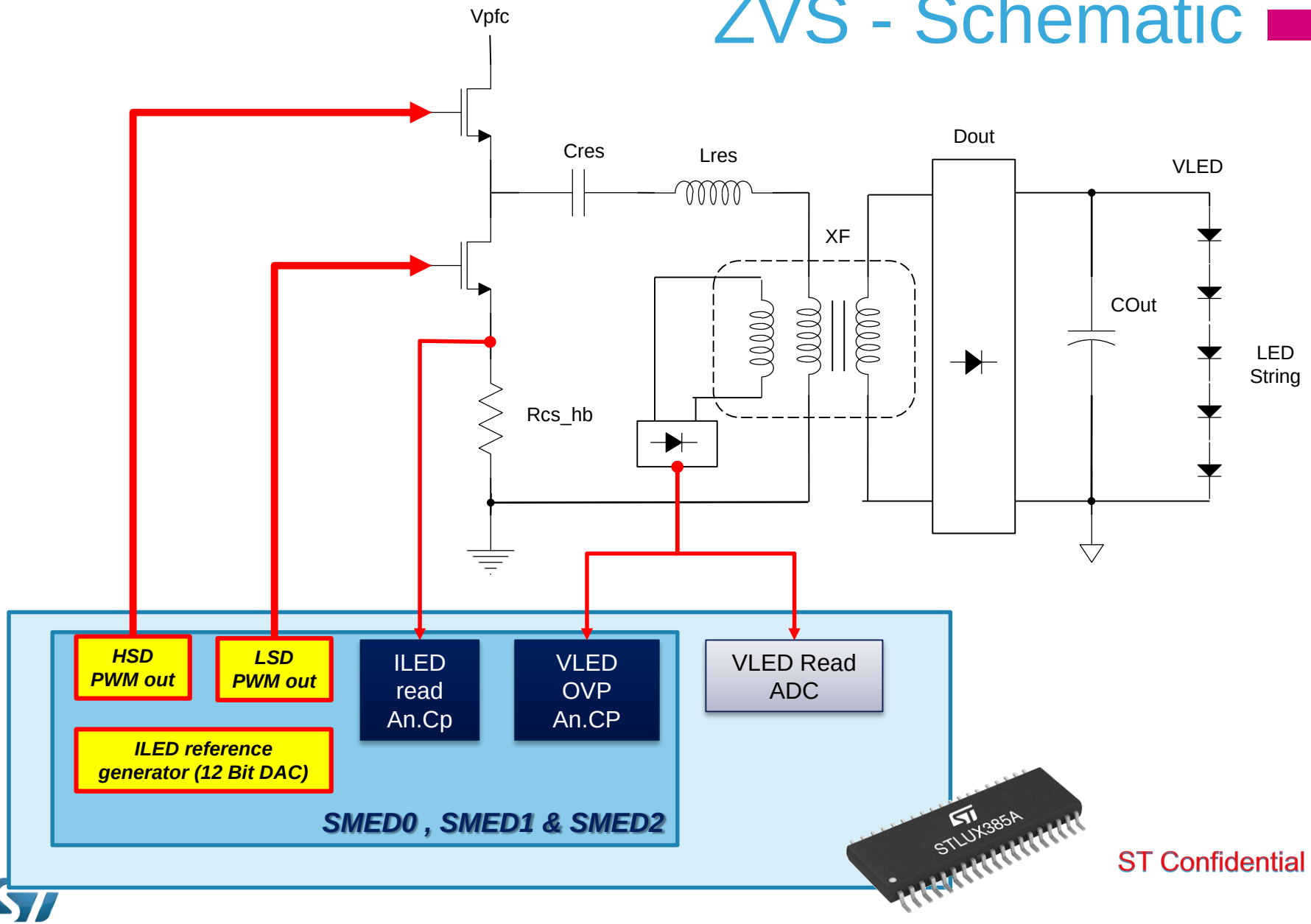


- Fast OVP (no FW intervention using SMED)
- Fast UVLO and Brownout protections (using SMED)
- Fast adaptable OCP protection (better max. output power limiting)
- Controlled start-up ramp

PFC –implementation - SMED

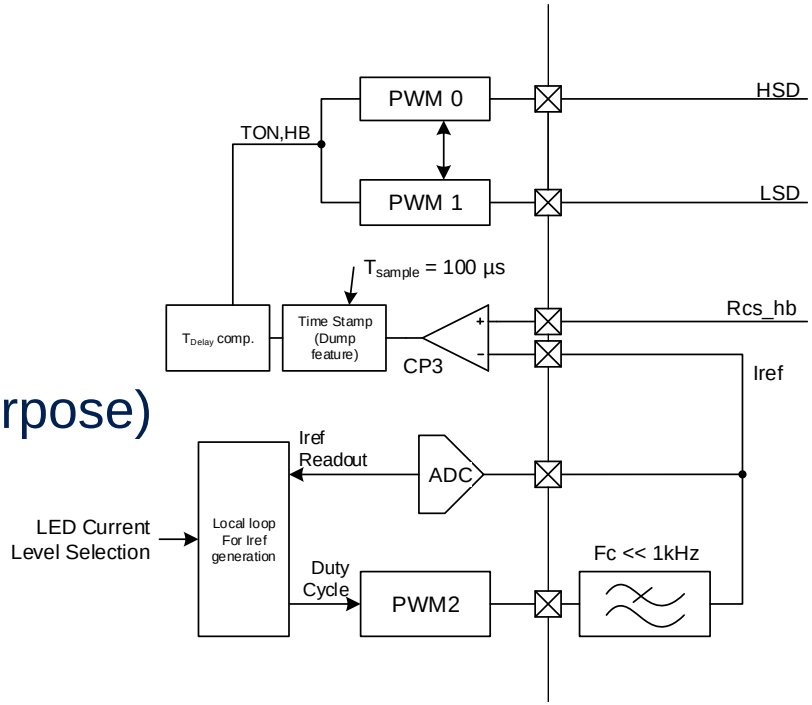


ZVS - Schematic



ZVS - Implementation

- Zero Voltage Switch – resonant LC topology
- Frequency range: from 70KHz to 350KHz
- Output LED current regulated by primary side (1 A to 10mA)
  - Primary current regulated by internal algorithm (12 bit resolving)
  - Loop regulation sampling time:100uS
  - FW based Soft start
  - Innovative Algorithm to reduce the minimum current level
- Automatic ramping time (for DALI purpose)
- Output over-current protection
- Output short circuit protected
- Output no load protection



HB – Implementation - SMED

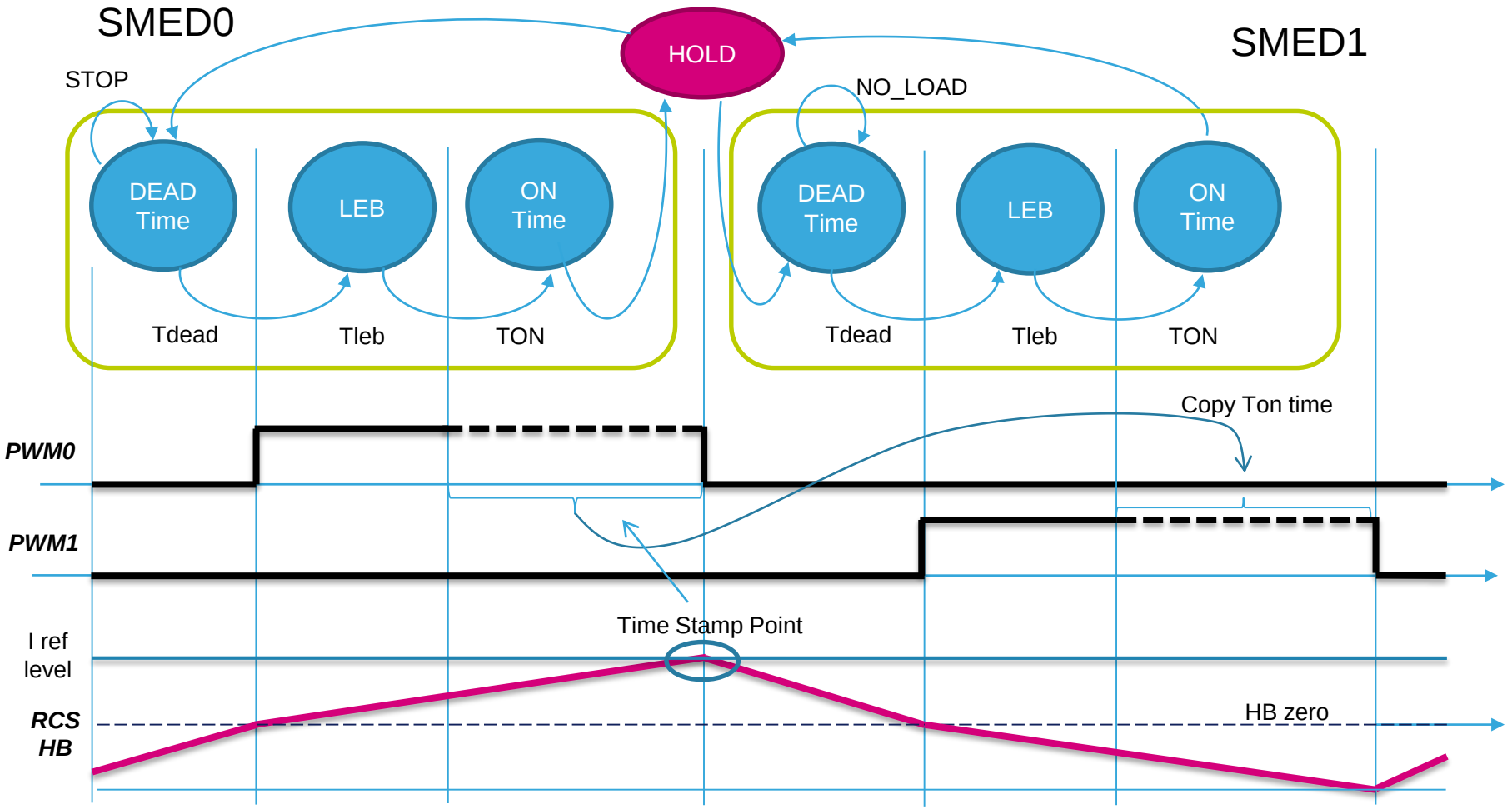
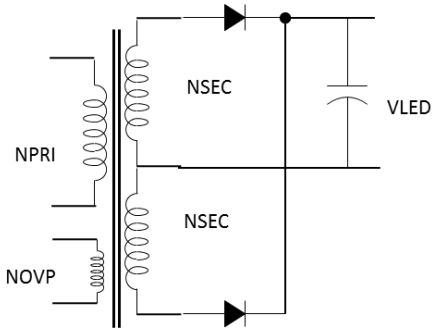


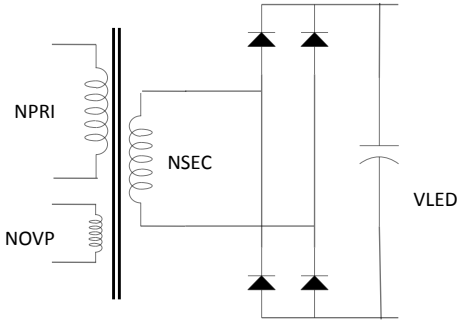
Figure not in scale

ZVS – Versions selection

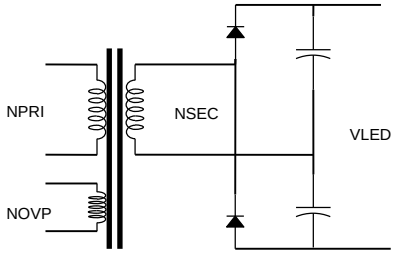
- Using one of the two rectification networks the following versions can be selected without further FW / HW modifications:
  A. 100 V – 1 A
  B. 200 V – 0.5 A
  C. 400 V – 0.25 A (not implemented into demoboard)



A



B

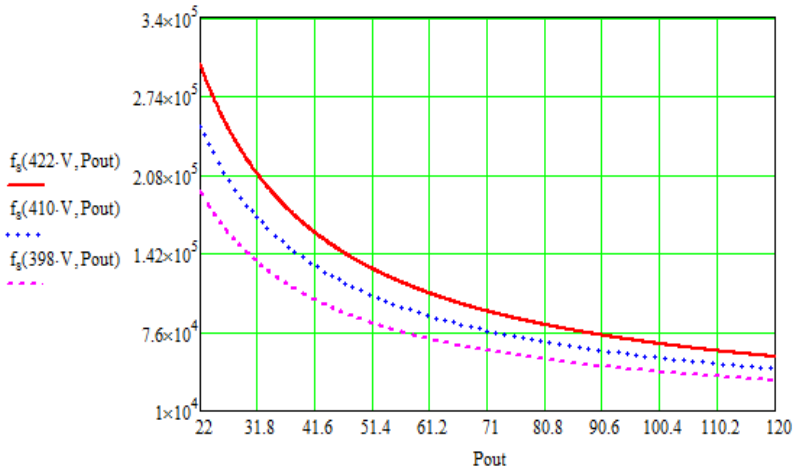


C

Output Power Variability

- Variation of output voltage and output current results into frequency variation
- Hyperbolic characteristics limits the minimum output power to roughly 40% of full power.

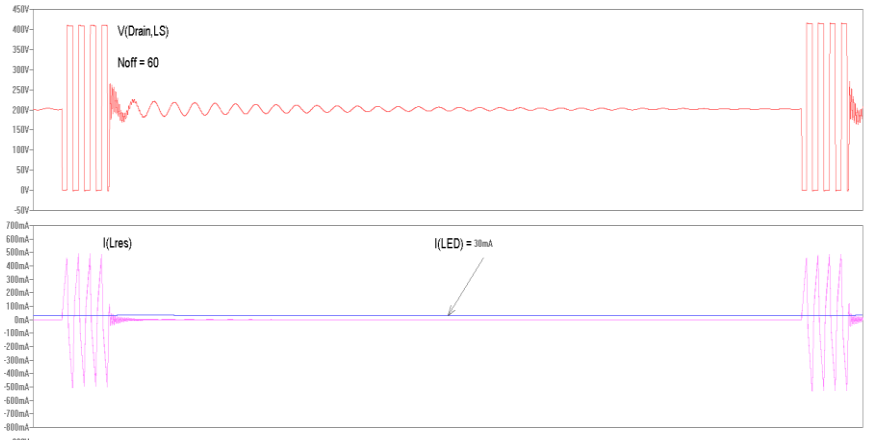
- Fixed output current / variable output voltage Fixed output voltage / variable output current applications are directly addressed.
- Innovative algorithm to address Variable Current and voltage or dimmable solutions is implemented.
  (min power down to <10% already reached)
- Flicker free analog dimming

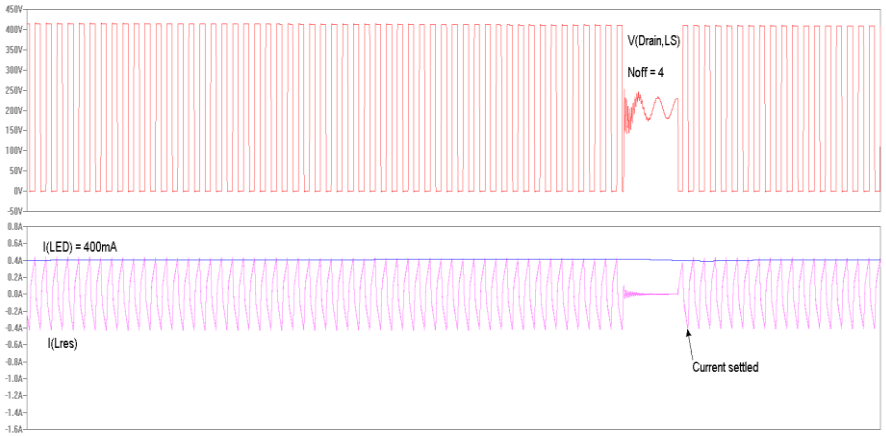


Patent: US 2015/0003117A1

Dimming algorithm

- Two operating regions are identified
  - Peak current control area:
    - To reduce the current starting from max current until a minimum noise-free current level is reached.
    - Resulting into variable frequency with different variation ranges depending on Vout.
  - Skipping cycle area
    - A number over a certain amount of HB cycles (currently 112) are skipped to further reduce the output current.
    - This set-up allows to obtain a minimum current lower than 10 mA (100 Vout)

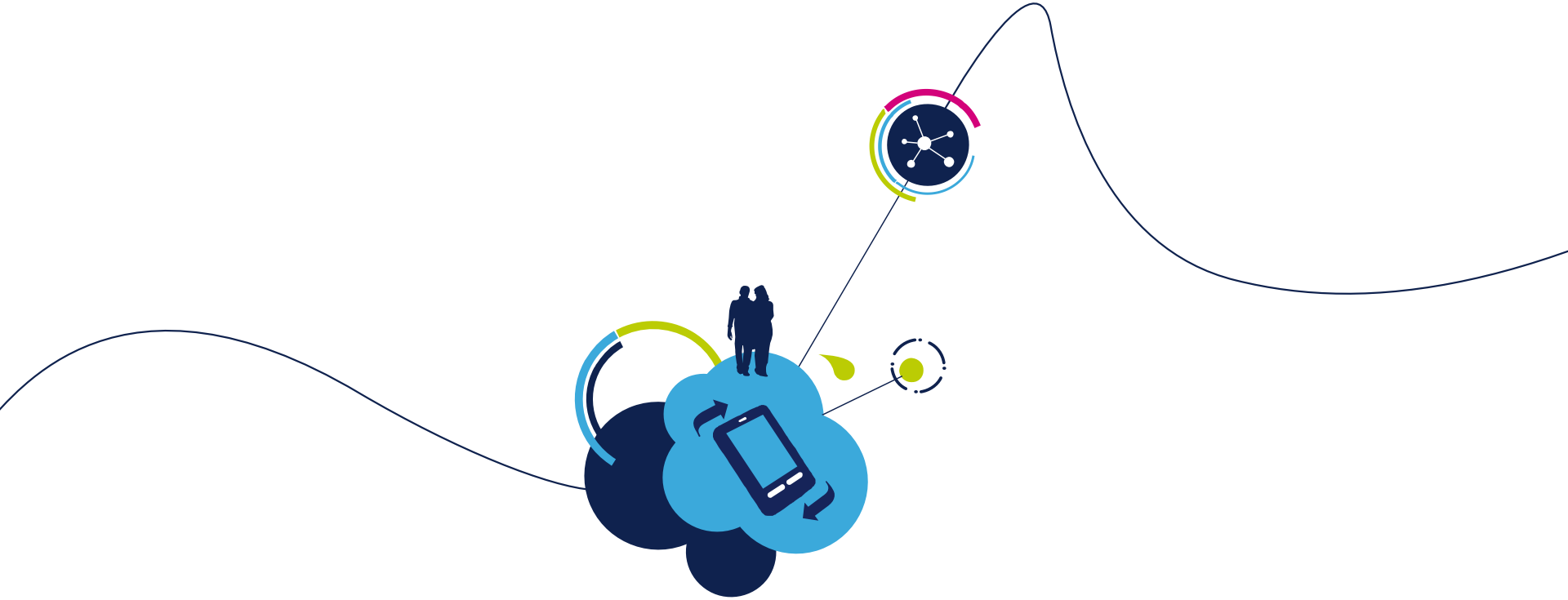




Patent: US 2015/0003117A1

DALI - Implementation

- Manchester decoder by dedicated HW peripheral
  - Start – Stop – Staffing and de-staffing – Bit validation without FW intervention
  - 16 bit input register (available 24 bit) – 8 bit output register
  - Interfaces failure - 500mS timing by HW
- Dali protocol
  - IEC62386- 102 and 207 implementation (Standard device type 6 – LED)
- Very low power consumption when DALI command “setup output LED off” is received:
  - Smart low power management



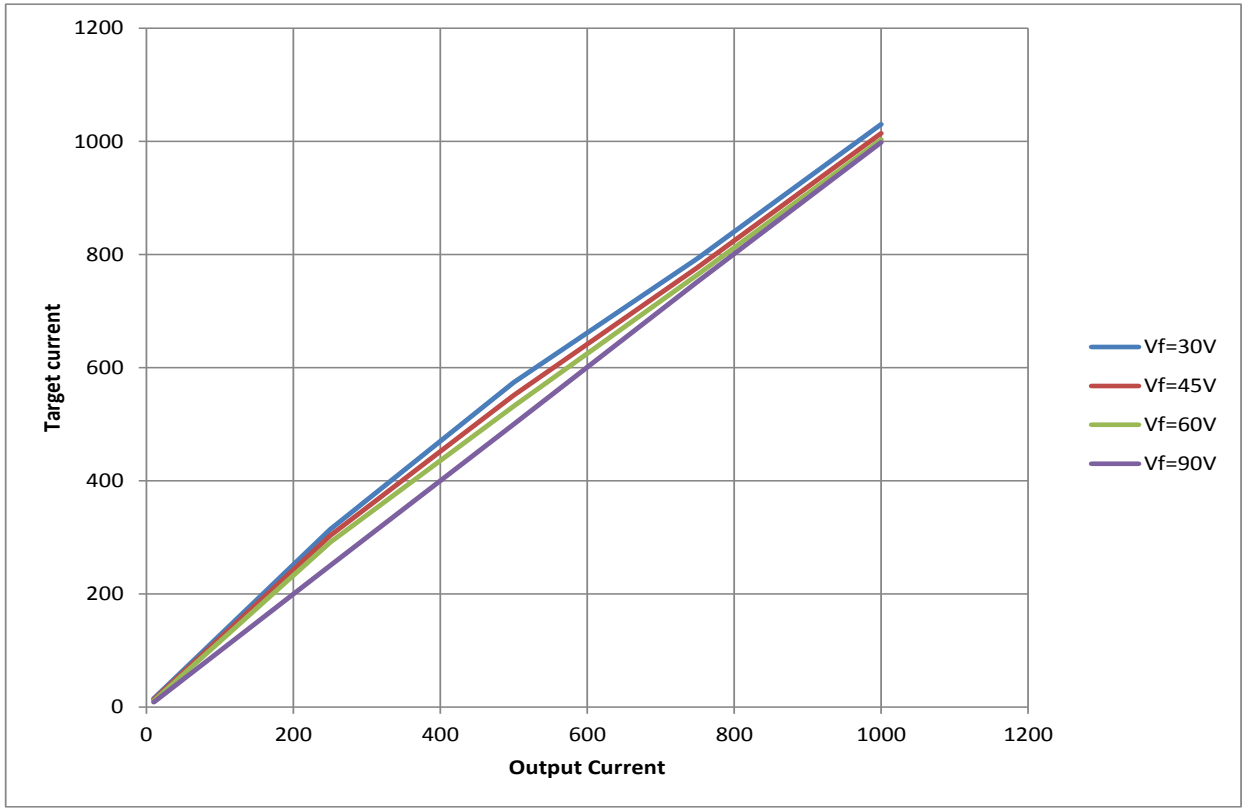
Results

Results summary

- Secondary side current precision within 5 %
- Power Factor: higher than 0.98 when output power is above 50W
- THD: below 10% when output power is above 50W
- Higher efficiency: more than 92% at maximum power
- Low input power when in standby: below 200 mW

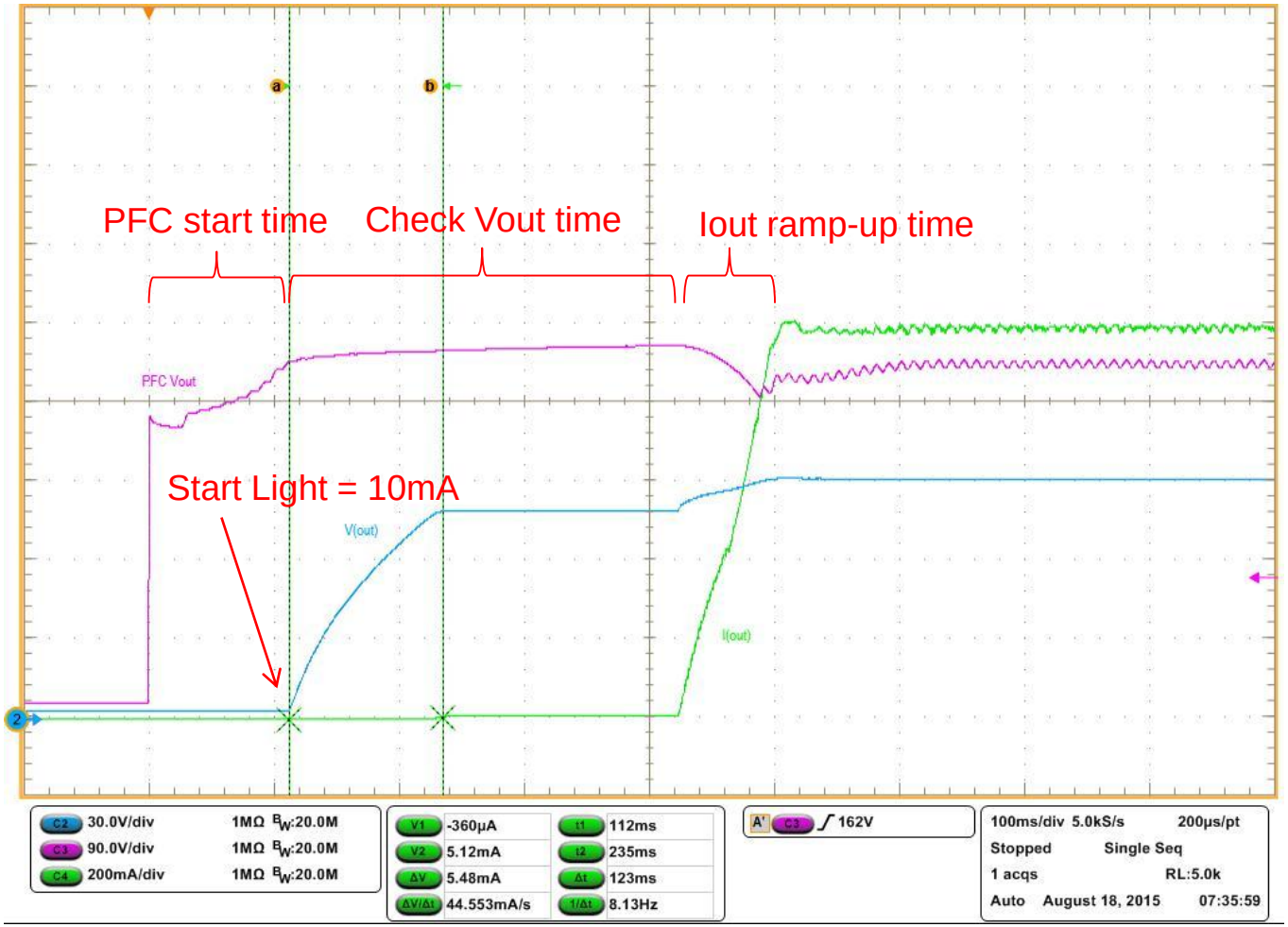
- NOTE: Using FW revision V3R35

Output current regulation summary



Nominal output current	Vf=30V	Vf=45V	Vf=60V	Vf=75V	Vf=90V
DALI	mA	mA	mA	mA	mA
1%	10	15	13	11	10	8.5
25%	250	314	303	291	273	250
50%	500	574	551	532	516	500
75%	750	793	777	764	754	752
100%	1000	1030	1014	1003	998	998

Application start-up

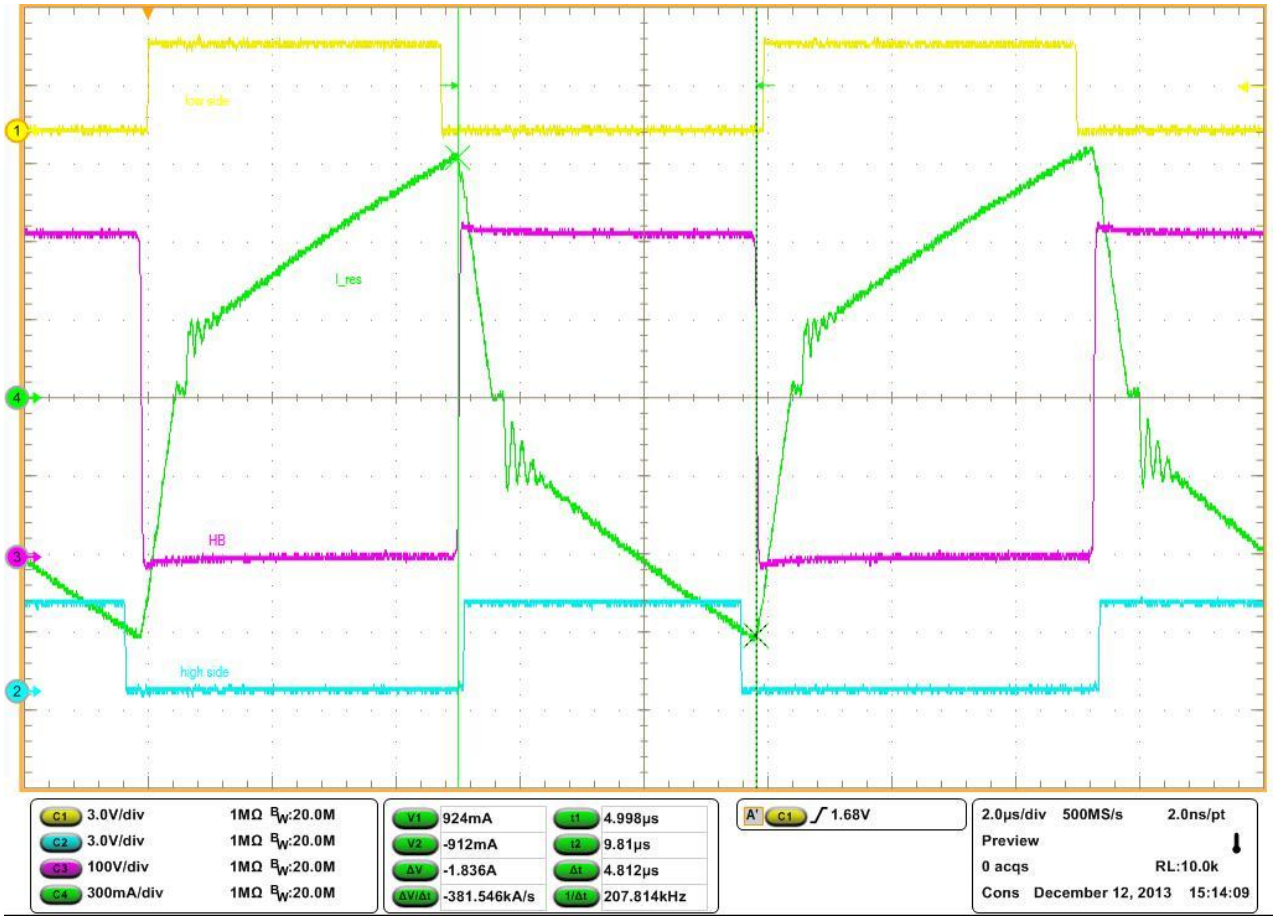


PFC Vout

Vout

Iout

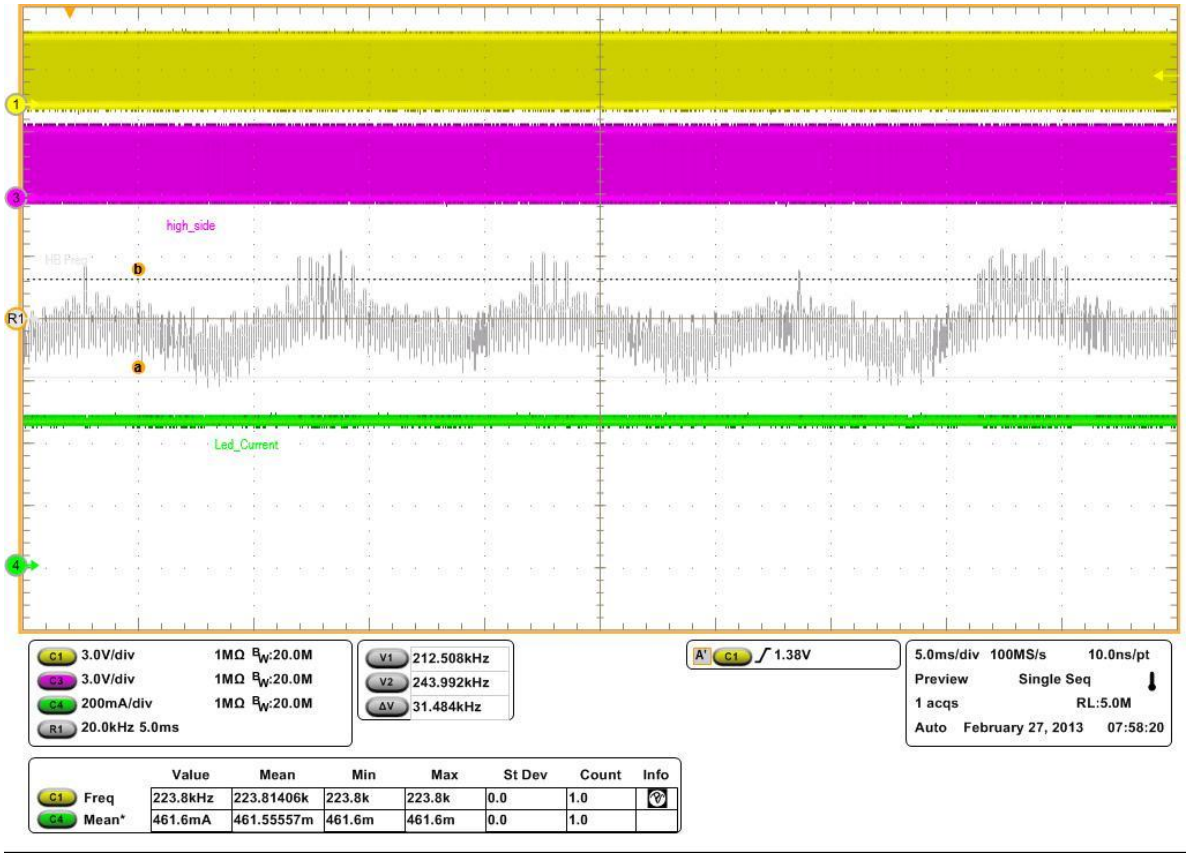
Output current regulation



Primary side signals:

- High side (yellow)
- Low side (blue)
- Resonant current (green)
- HB middle point (violet)

Output current regulation

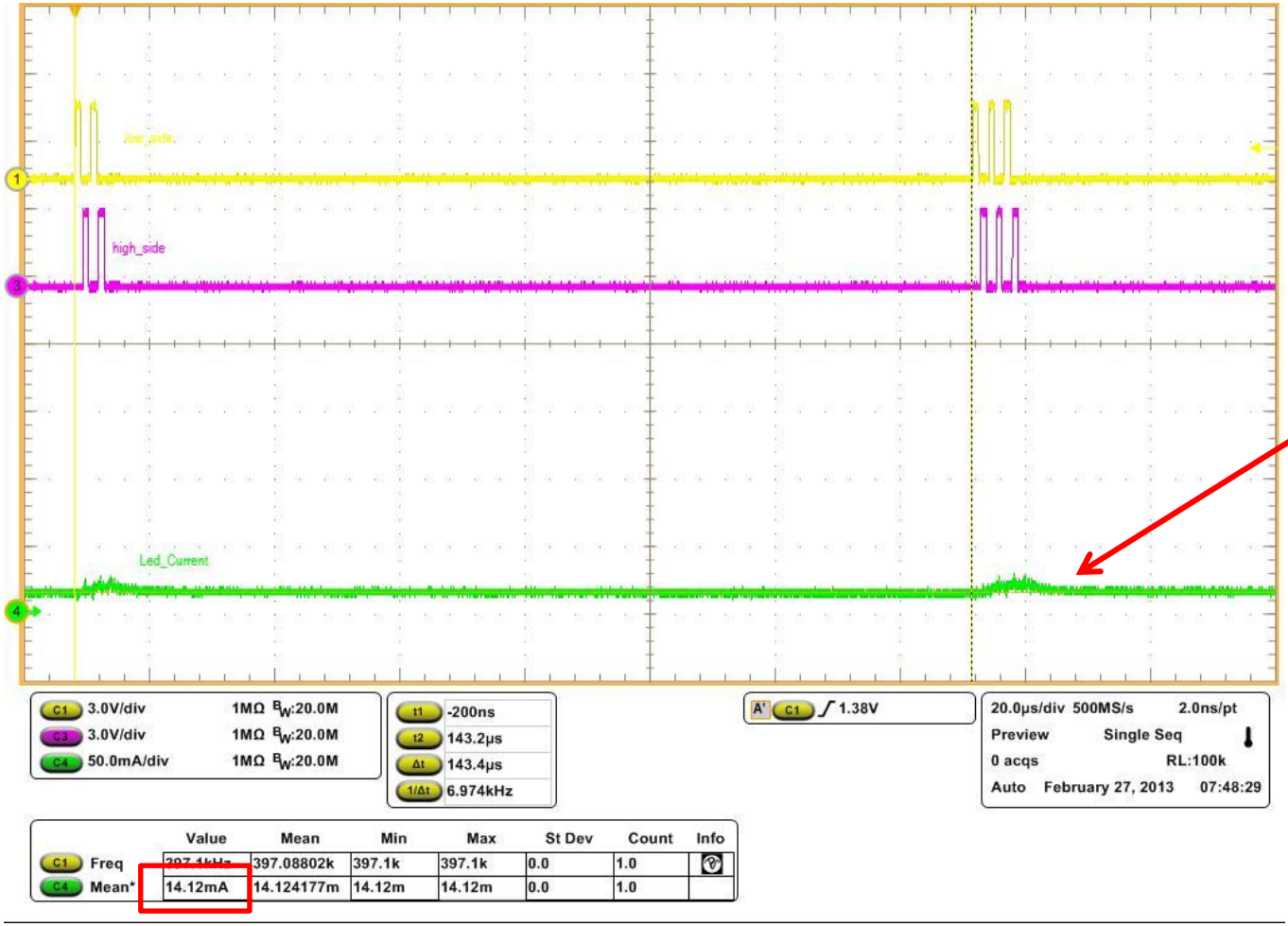


The current is here regulated with peak current mode.

Grey trace depicts the frequency variation having a 100Hz ripple, that is absent into output current (green trace)

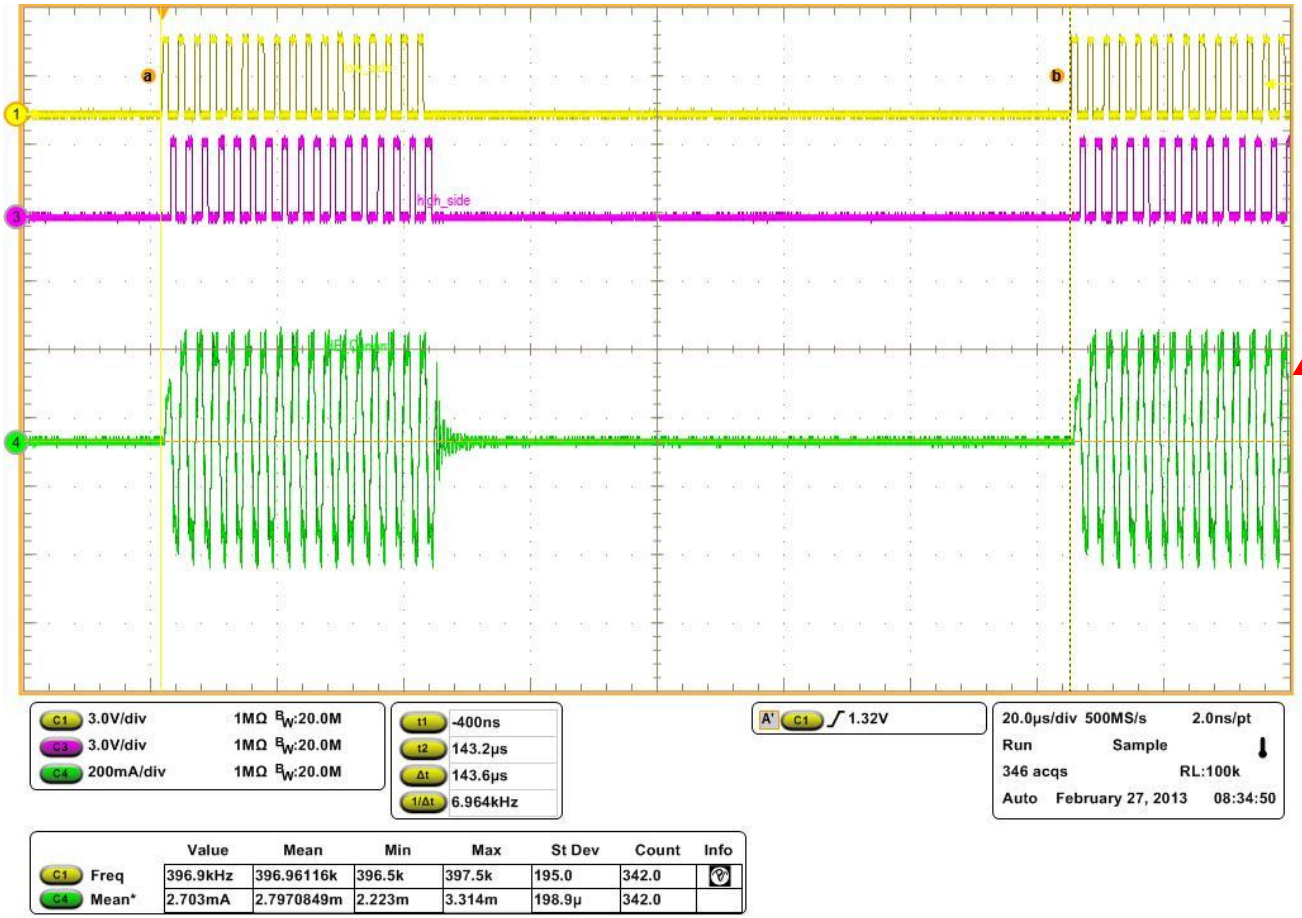
Skipping cycle – 2 skipped over 112

Skipping cycle – 107 skipped over 112



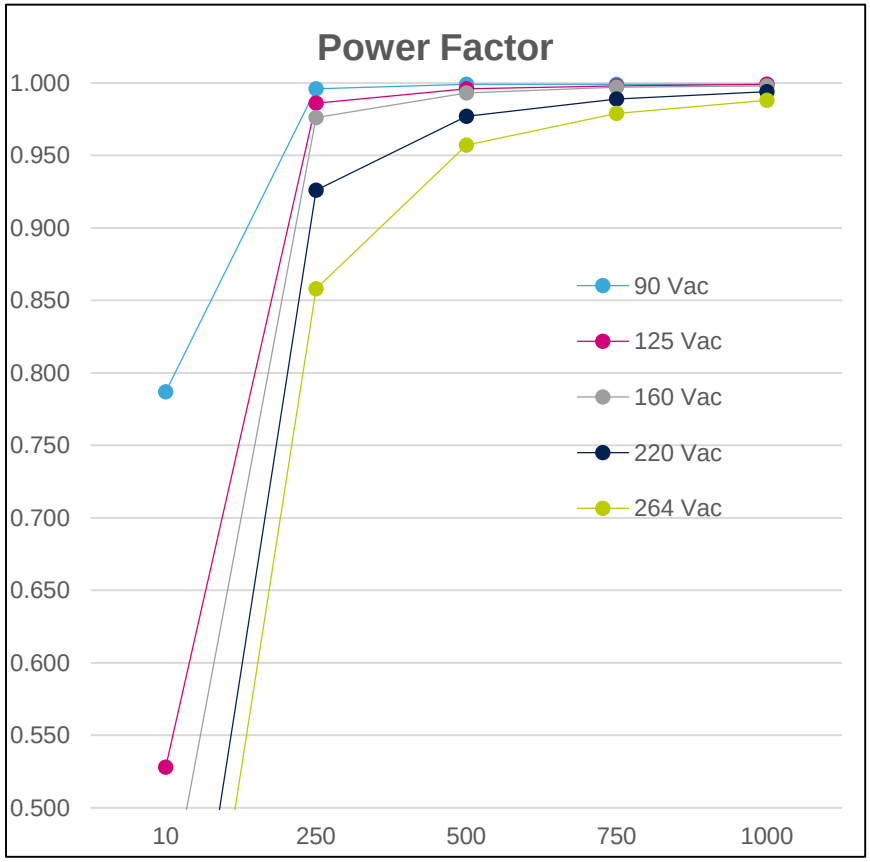
Ripple free

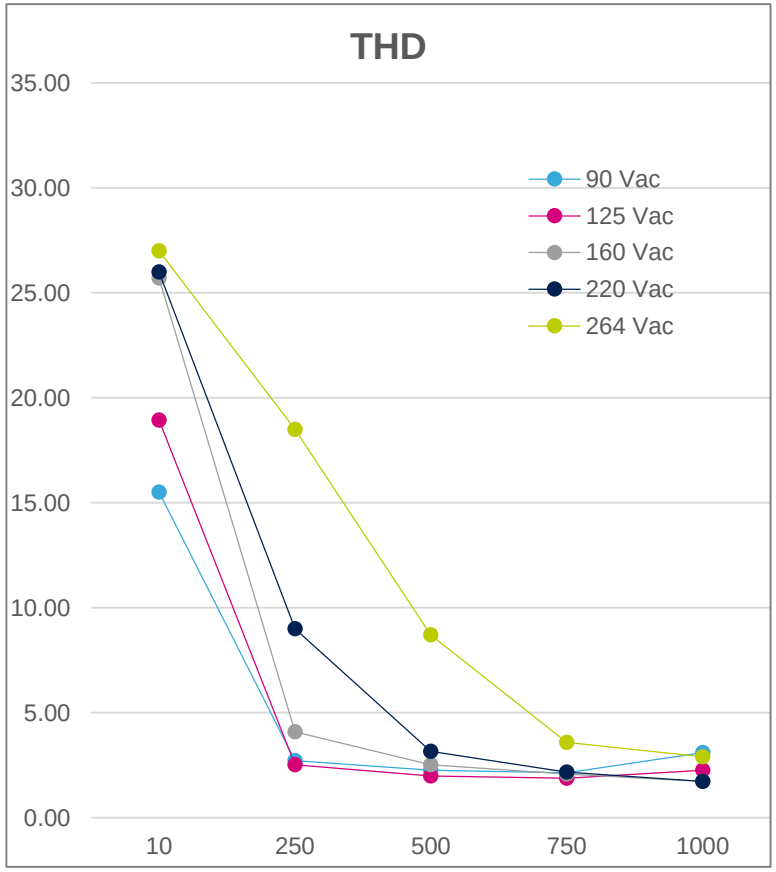
Skipping cycle – 30%



RESONANT CURRENT

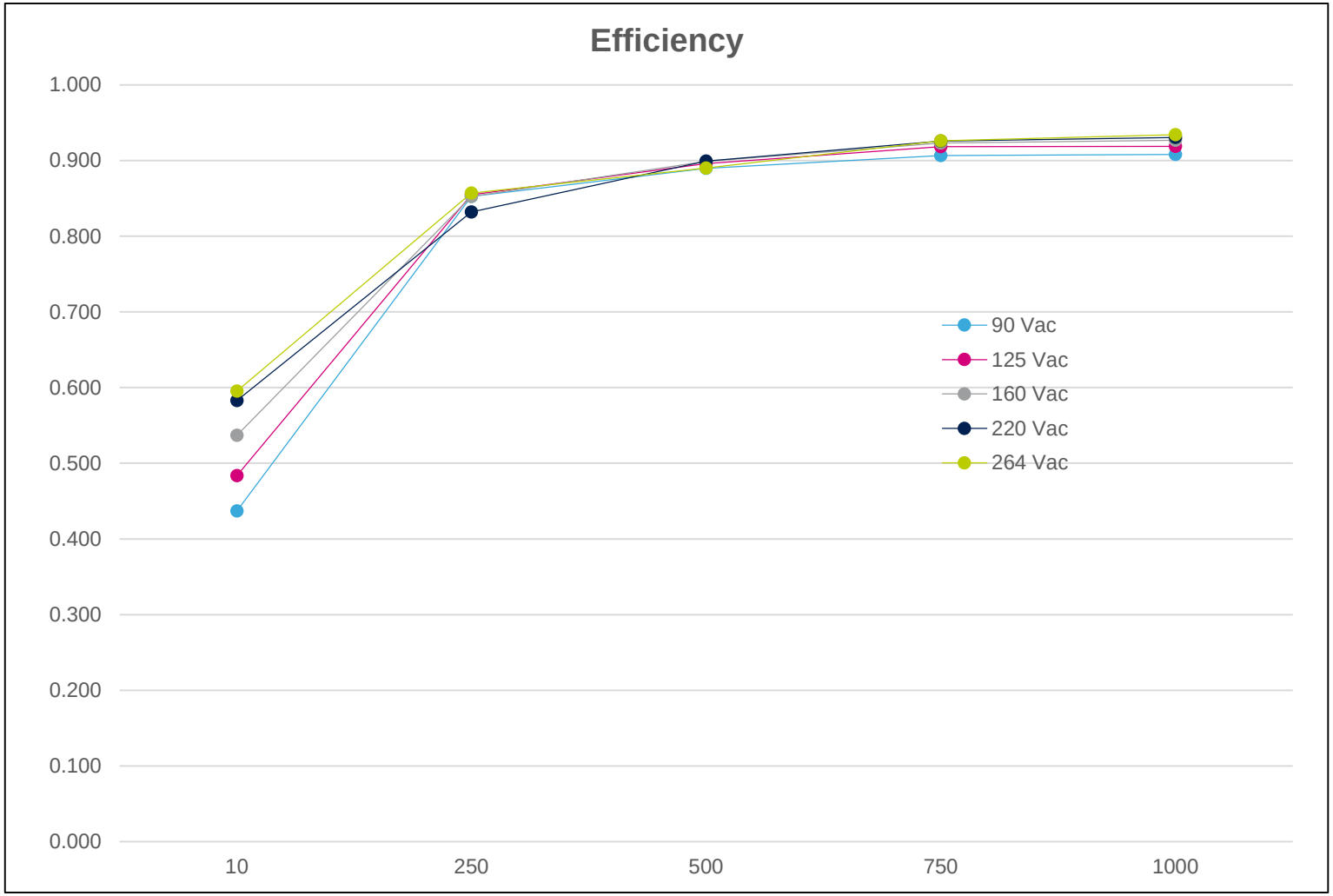
Power factor and THD summary



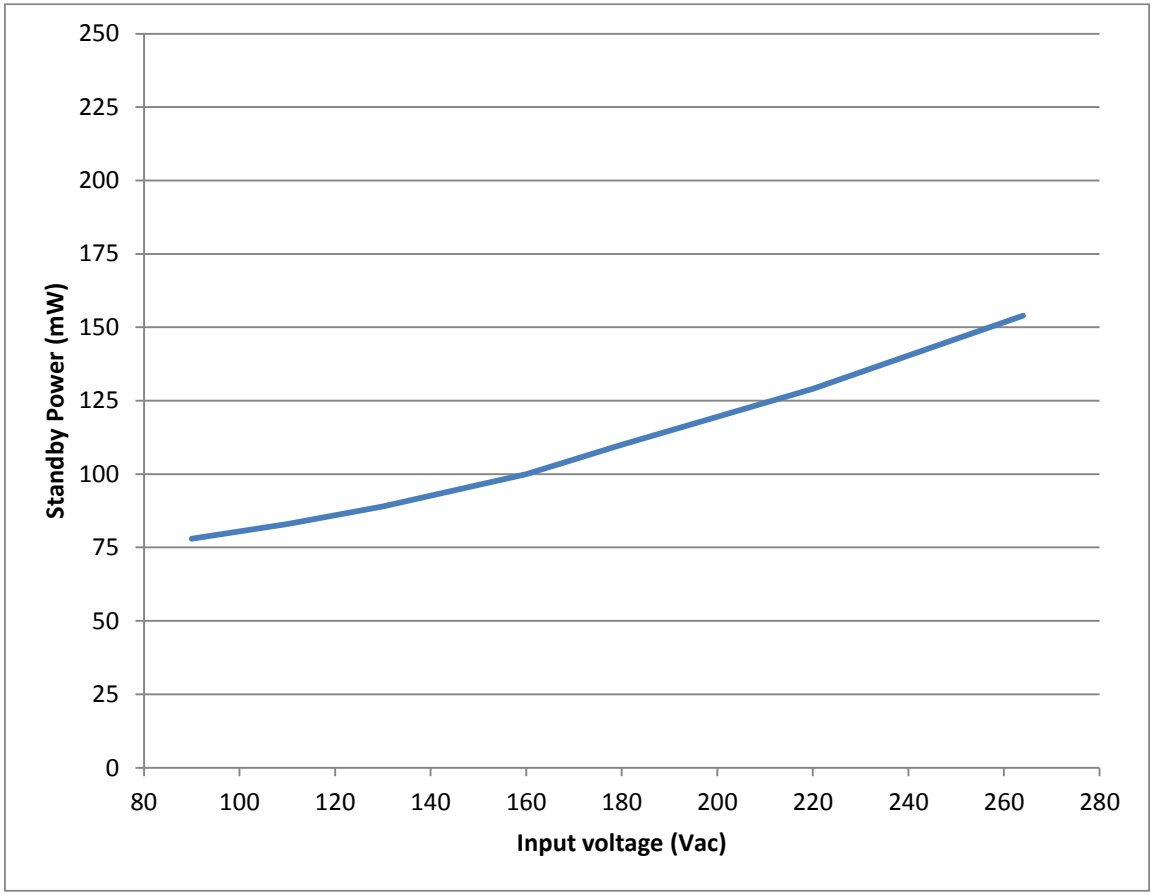


PF and THD values versus output power for different input voltages

Overall Efficiency summary

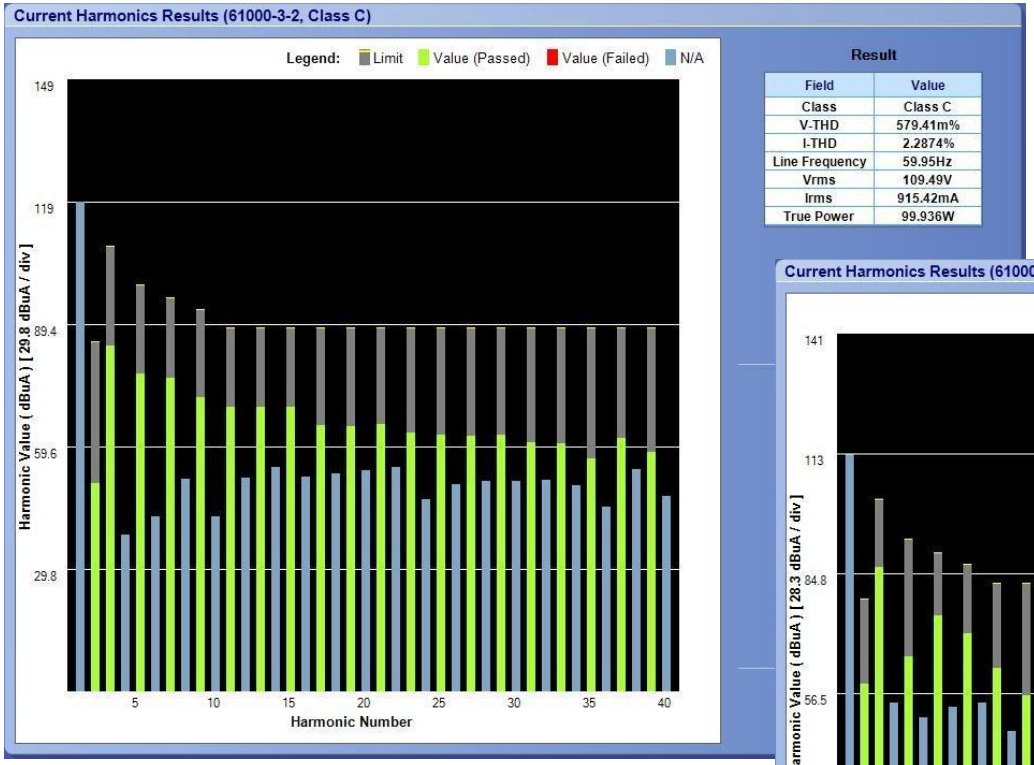


Standby Power summary

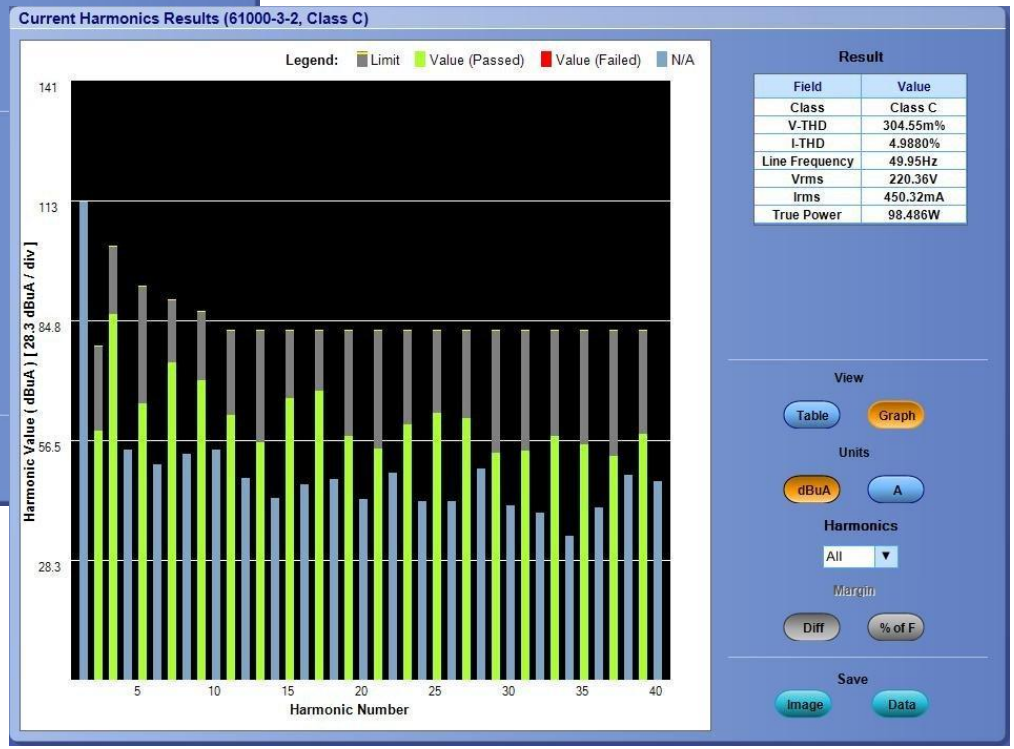


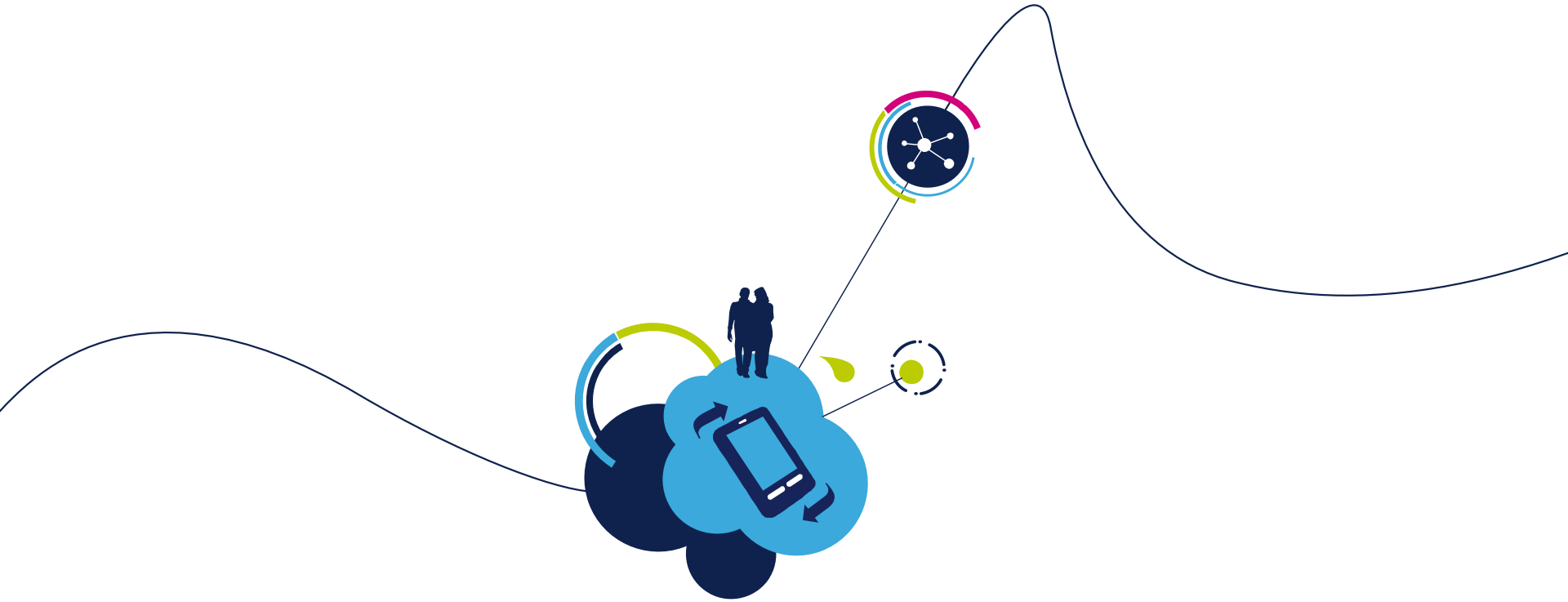
Full power Harmonic contents

110 Vac



220 Vac



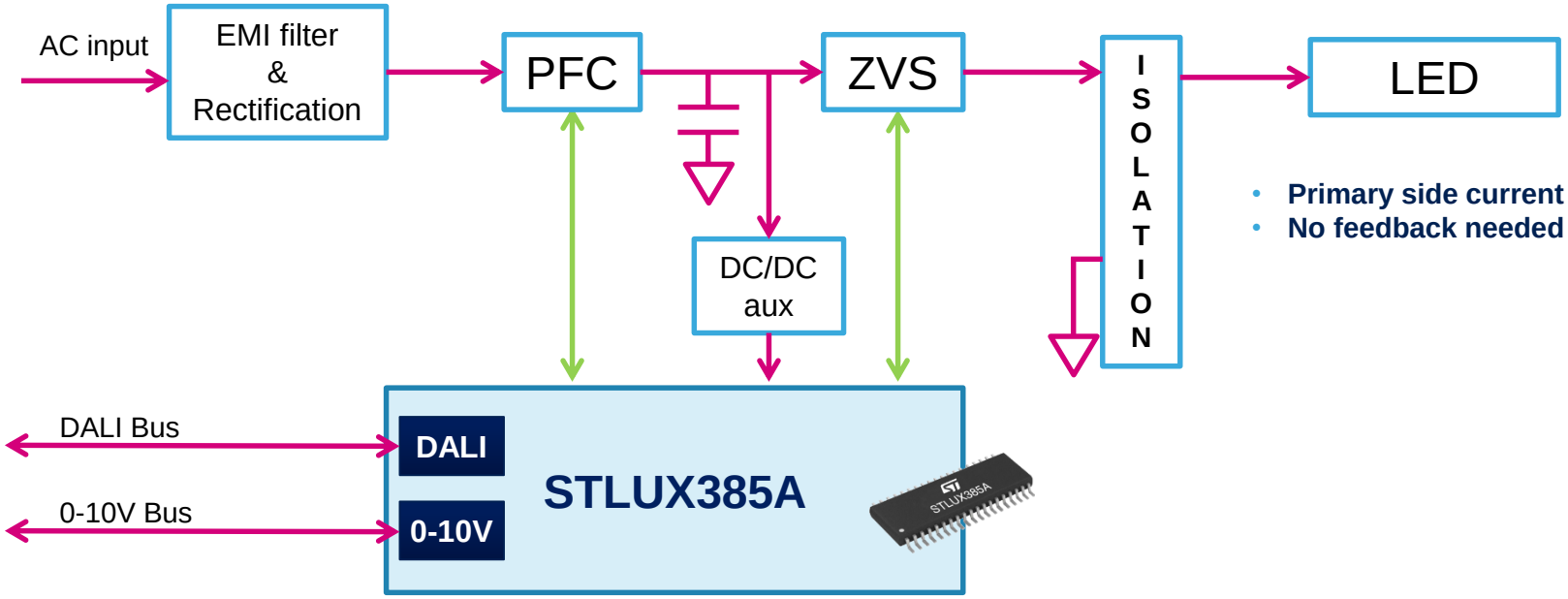


FW Application Library

Why using the FW library

- FW library implements PSR power conversion stage
  - Integrates PFC and HB control algorithms
  - STLUX385A SMEDs configured and updated at run-time
- Fully customizable
  - Configuration via serial interface or software application layer
  - Parameters stored in EEPROM
  - 50+ configurable parameters
- Fast time-to-market
  - Easy to develop application on top of the library
  - Focus on application differentiation

Block schematic

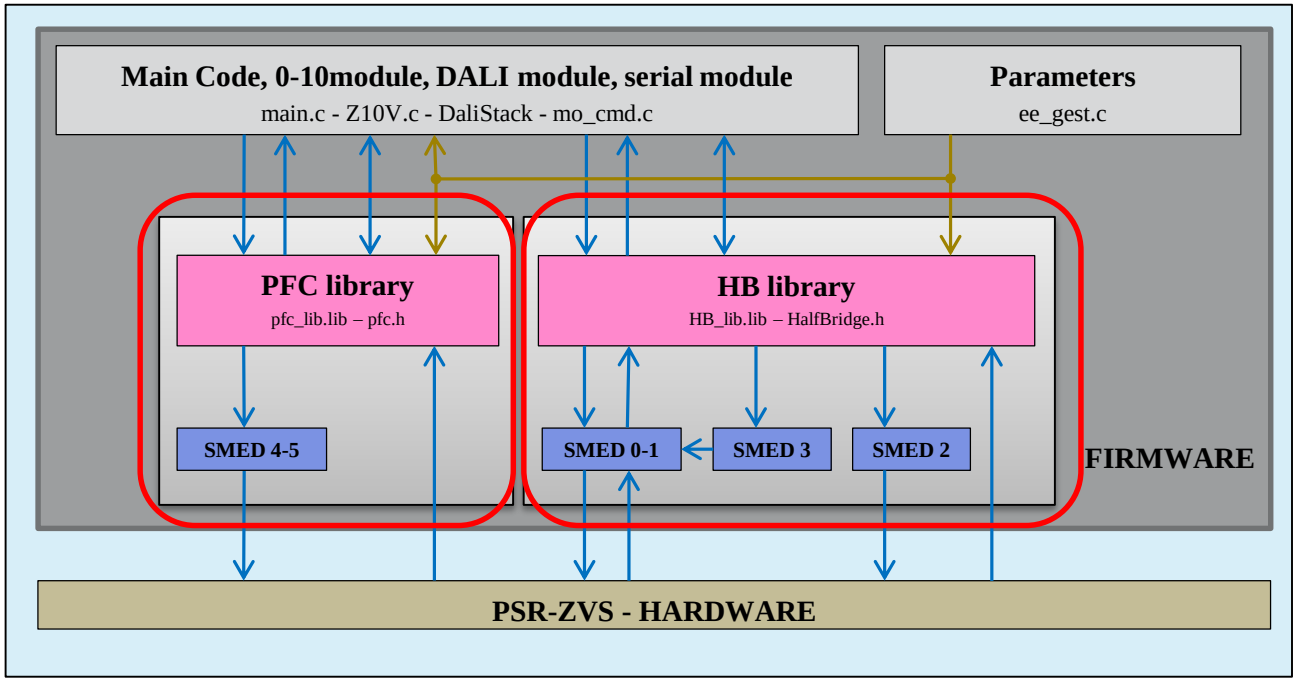


- **Primary side current control**
- **No feedback needed**

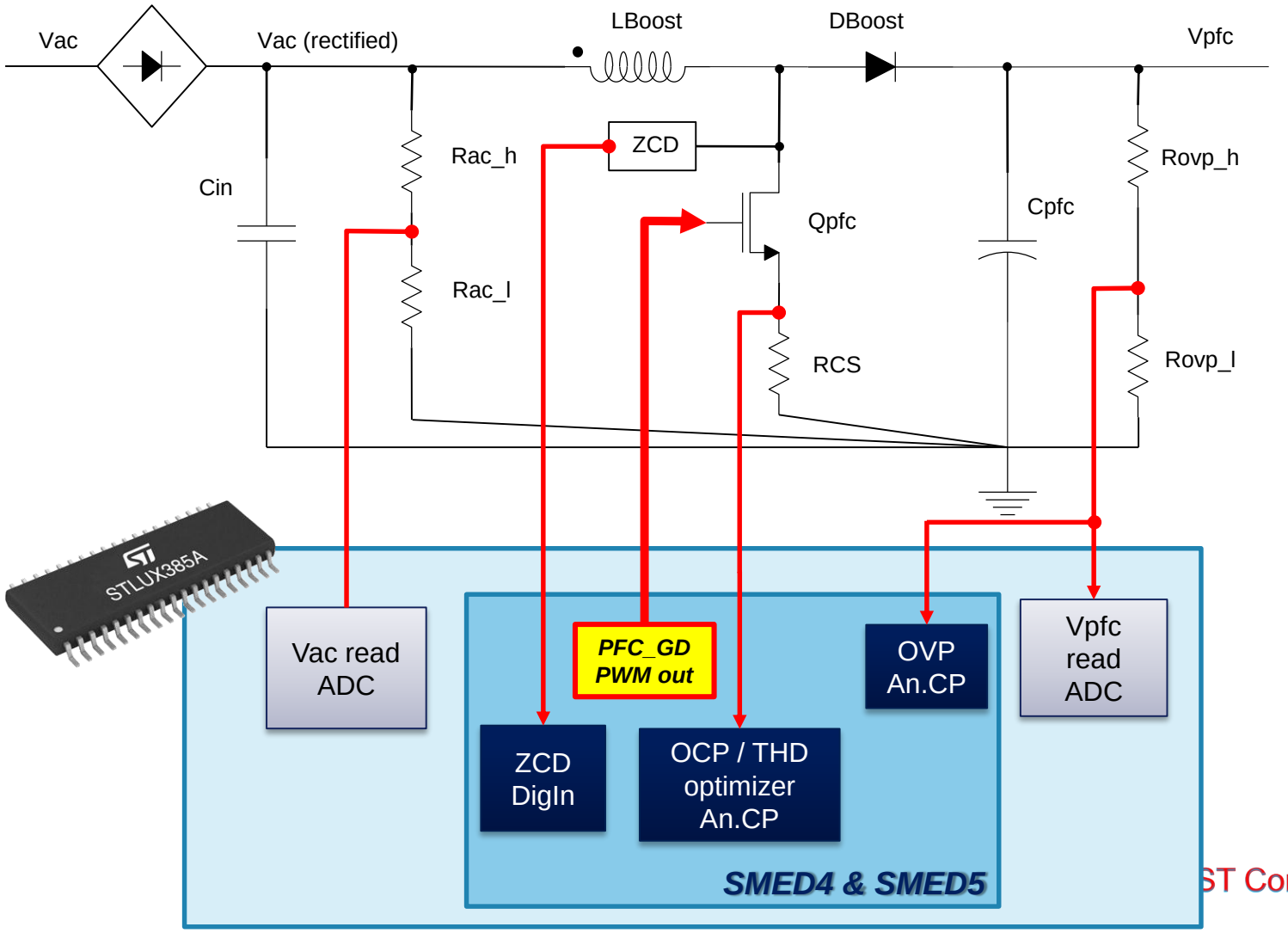
- **STLUX385A signals:**
  - Input voltage for Uvlo&startup
  - **PFC** output voltage for loop regulation
  - **PFC** gate driving signal
  - **ZVS** resonant current for control loop, output voltage for protection
  - **ZVS** HB and relevant dimming control signals
  - **DALI** frame – interpreter, response and execution
- **Secondary components: Rectifier and capacitor (no extra active components)**

Library Implementation

- Two independent firmware module: one for PFC, one for Half Bridge ZVS
- PFC and HB-ZVS Hardware adaptation using modifiable parameters

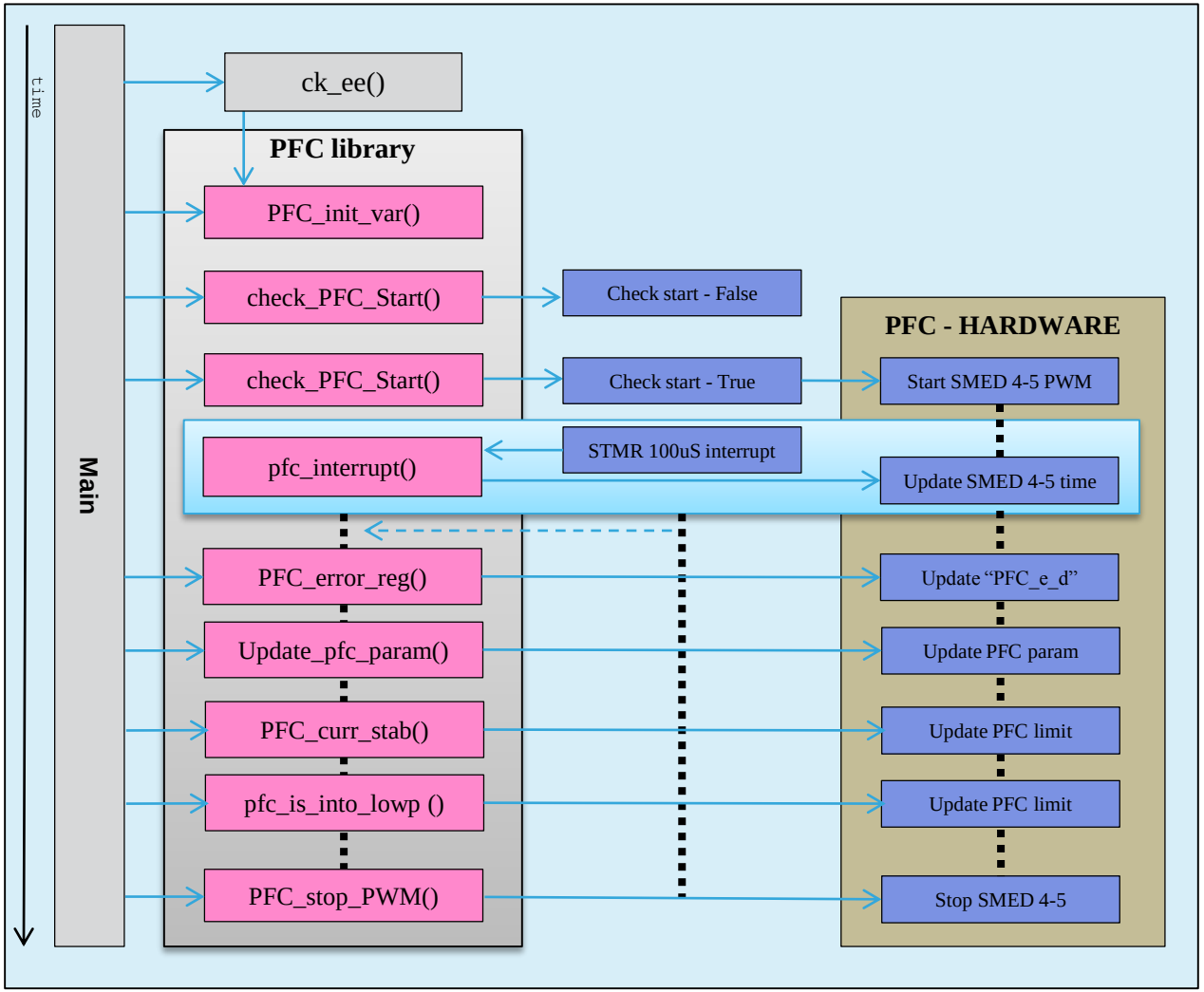


PFC - Schematic

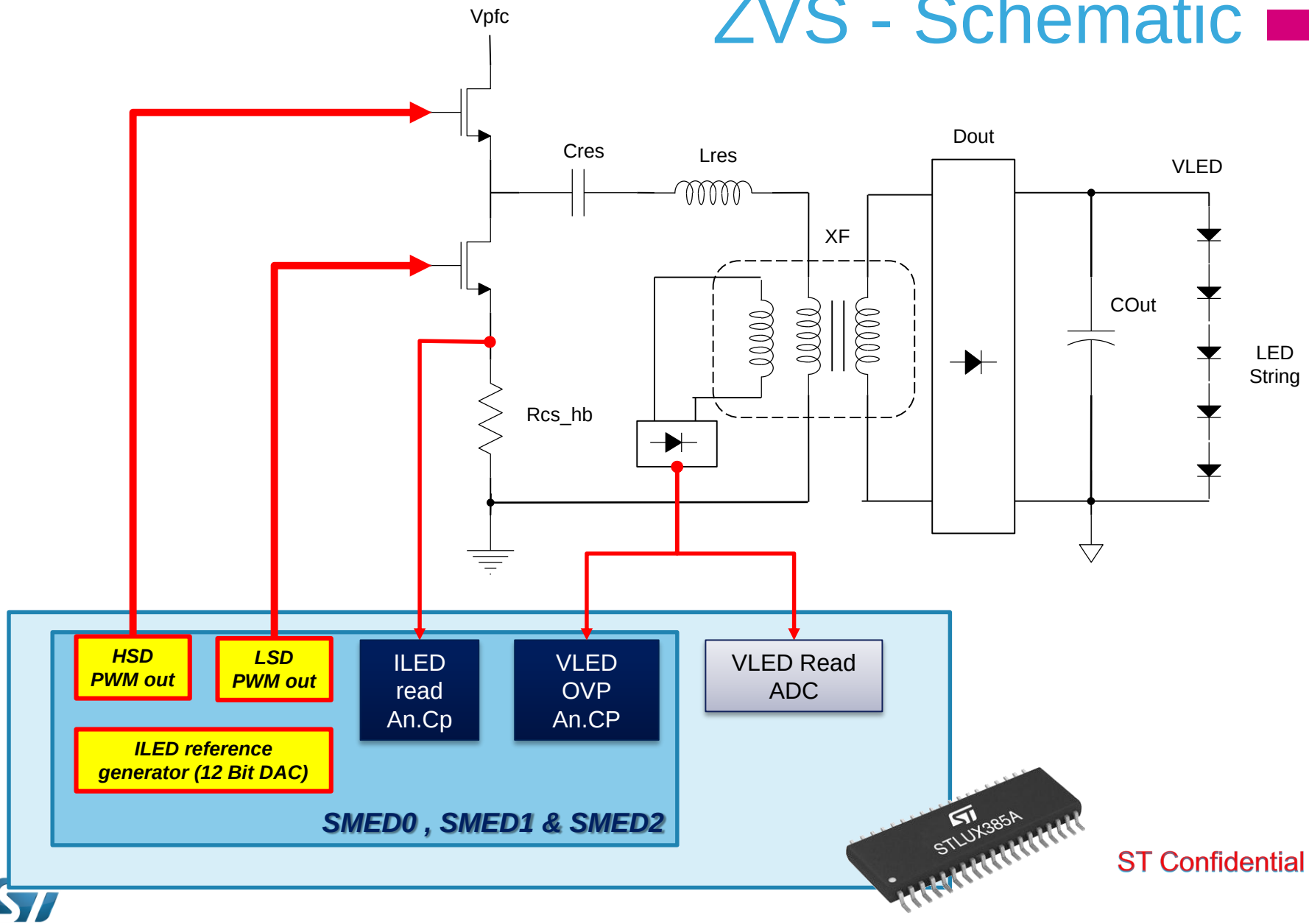


PFC – Library Implementation

- PFC parameters apply during start-up
- PFC control using simple subroutine
- PFC Start/Stop under User control
- Automatic update PFC control loop using interrupt
- PFC library control SMED4-5 behavior

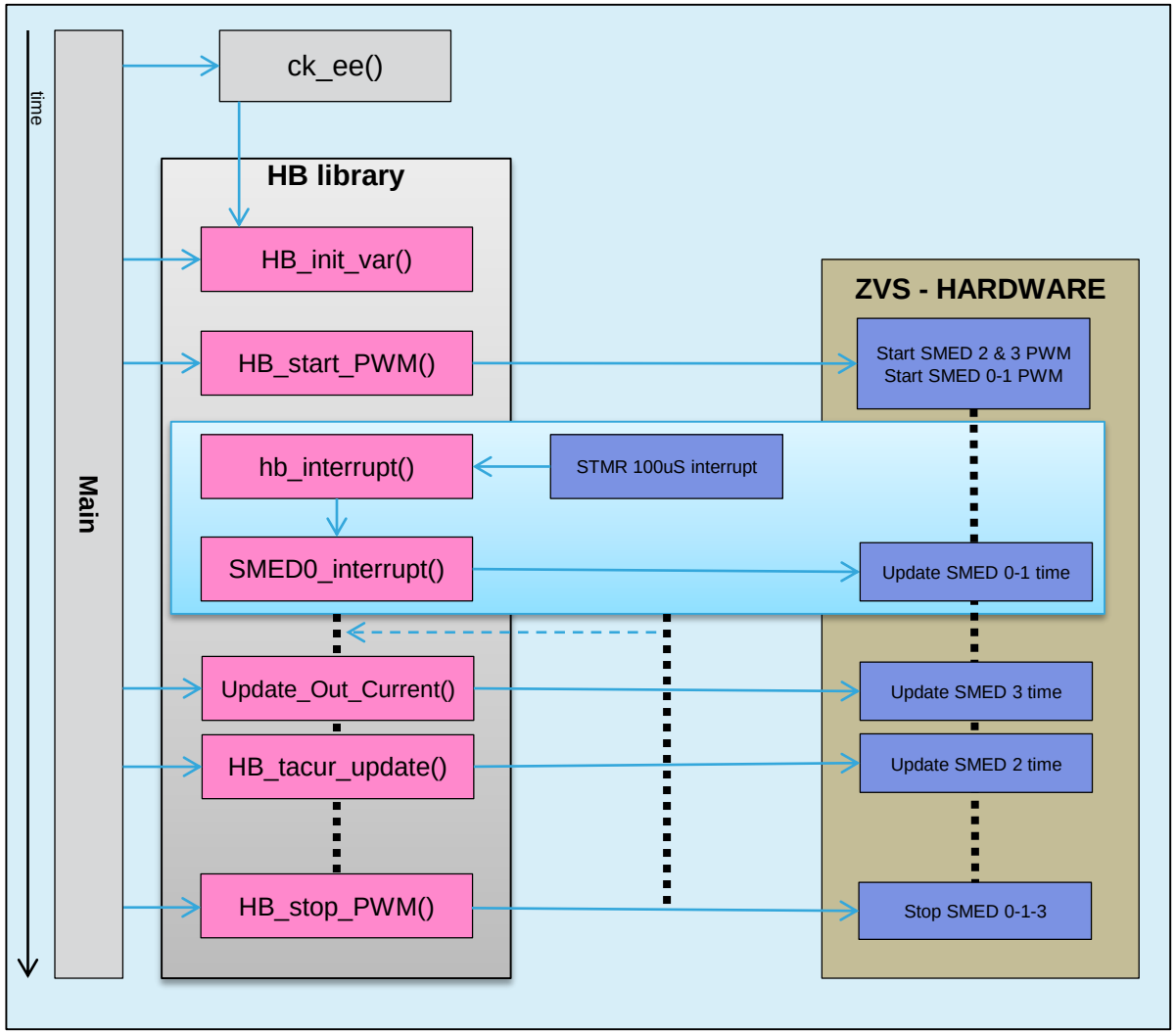


ZVS - Schematic



HB-ZVS – Library Implementation

- HB parameters apply during start-up
- HB start/stop under User control
- Automatic HB control loop using only interrupt
- Subroutine to manage the output current
- HB-ZVS library control SMED0-1, SMED2 and SMED3 behavior

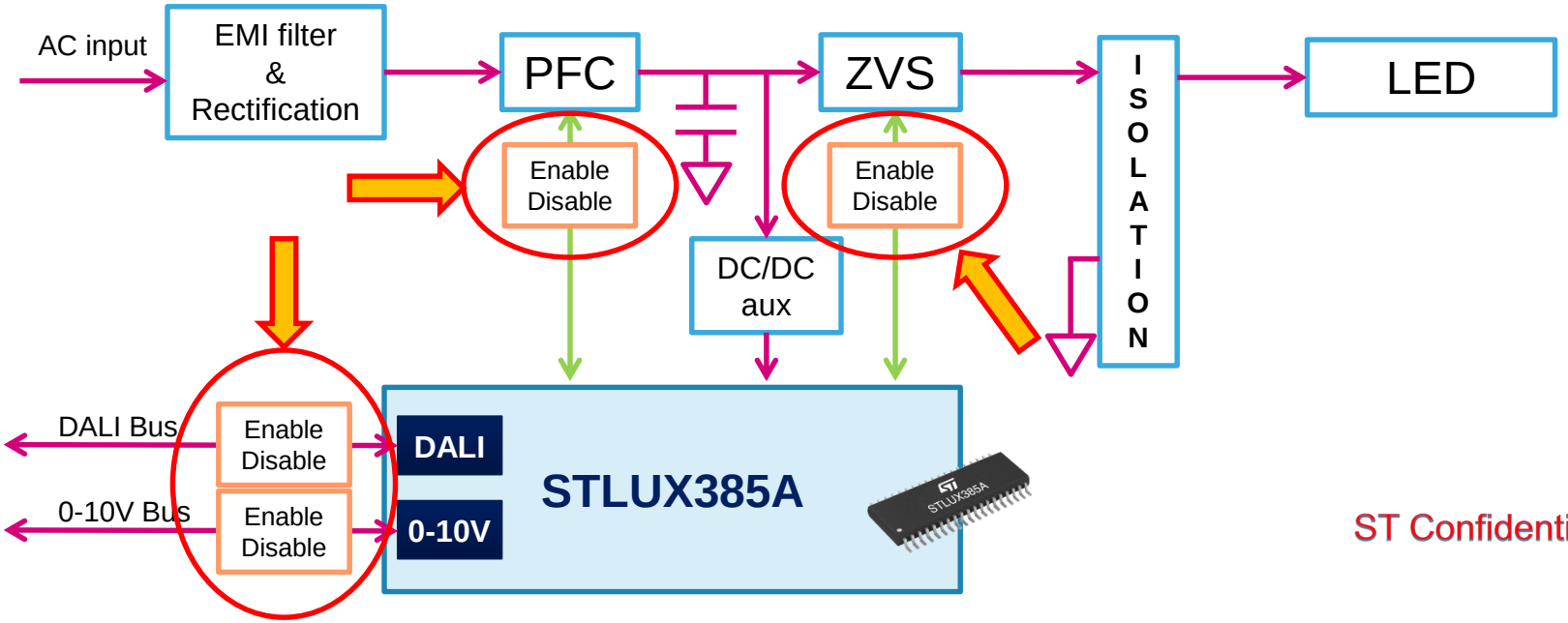


Parameters

- Three configurable parameters area:
  - Application parameters: enable the ROP code protection, enable/disable interfaces or library function
  - PFC parameters: output level, start-up current limitation, three zone level definition, OCP level protection, Vac input level start/stop, PFC uvlo level, etc.
  - HB parameters: max. ON time (limit the output power), no load level intervention, HIGH side delay trimming, propagation delay mismatch compensation, etc.
- Some parameters is modifiable, some other is fixed
  - Parameters is modifiable using serial command and is apply during start-up
  - Fixed parameters is modifiable using external resistor.
- When the parameters customization is approved, duplication is simple using “standard” read/download procedure.

Application Parameters

- Application modifiable parameters:
  - Enable or Disable globally all the board functionality (debug mode)
  - Enable the ROP Code protection
  - Enable/Disable the PFC and/or the Half Bridge functionality
  - Enable/Disable the DALI interfaces or, mutually exclusive, the 0-10V interfaces
  - Enable/Disable the Half Bridge loop compensation, usable to working into HB open loop → HB fixed frequency.



PFC Parameters

- PFC parameters modifiable by serial line:
  - Impose the THD time optimizer, to increase/relax or remove the PFC THD optimizer
  - Personalize the Over Current Protection level
  - Personalize the PFC Start-up voltage level
  - Define the PFC Input Under Voltage Protection level
  - Define the PFC Output Over Voltage primary level
  - Define the PFC Output Under Voltage Protection level
  - Define the PFC Maximum ON time to limit the maximum output power variation
  - Define the delay before detect the input Vac missing
- PFC parameters frizzed by hardware (resistor):
  - PFC output voltage definition
  - PFC input voltage definition
  - Last resource to Over Voltage protection (apply directly into SMED)

HB Parameters

- HB Parameters modifiable by serial line:
  - Half Bridge maximum frequency
  - Half Bridge minimum frequency
  - No load level; to modify the maximum output voltage level
  - Propagation delay mismatch compensation; if change the HB driver
  - Trimming the Half Bridge HIGH side delay; if change the HB driver
  - Dead Time apply to the HB stage
- HB parameters frizzed by hardware (resistor):
  - Output current; to modify the maximum output current, modify the shunt resistors (and also the output transformers if necessary).

Thank you very much for your attention